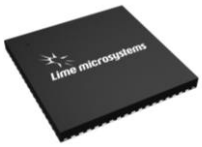
LMS8001A



Up/Down RF Frequency Shifter

SUMMARY FEATURES

- Single chip up/down RF frequency shifter with continuous coverage up to 10 GHz RF output range
- Four independent RF paths all driven by the same LO
- Fully differential signals
- Few external components
- Low voltage operation, 1.2 and 1.8V. Integrated LDOs to run on a single 1.8 V supply
- 56 pin QFN package
- Serial Port Interface
- Power down control available via ENABLE pins and/or equivalent SPI registers
- Synchronous loading of pre-set operation profiles by GPIO pins. More options are also available using corresponding SPI registers
- LO can be generated by on chip PLL or external LO from dedicated RF LO input pin
- Integrated on chip PLL loop filter
- Low power consumption

APPLICATIONS

- Extending Lime transceiver chips set family RF frequency range up to 10 GHz.
- Converting homodyne into heterodyne transceiver architecture for more stringent IF filtering of blockers, interferers and adjacent channels
- Converting MIMO transceiver into multiple independent transceivers
- Carrier aggregation

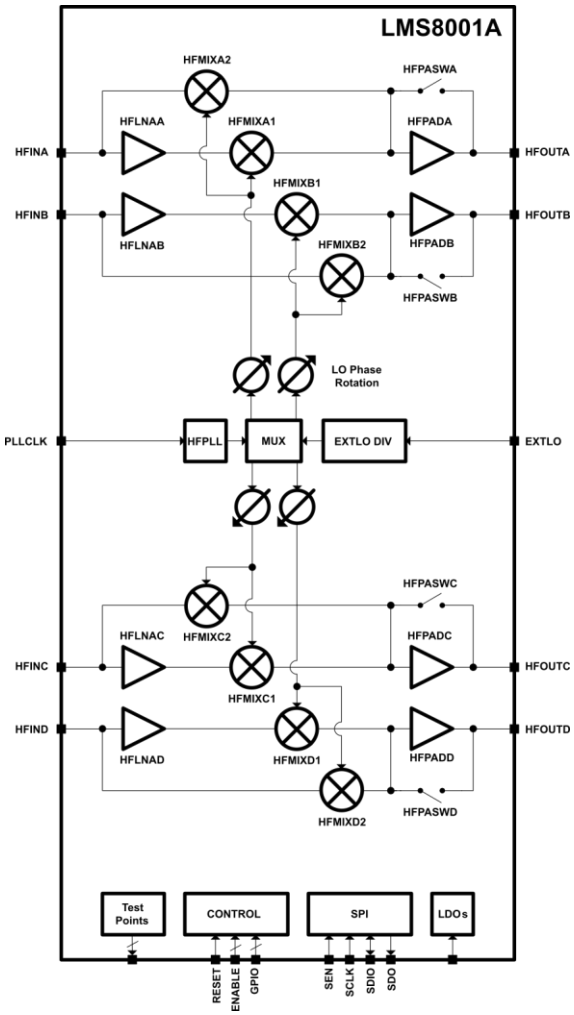


Figure 1: Structure of LMS8001A up/down RF frequency shifter

GENERAL DESCRIPTION

LMS8001A is designed to extend RF frequency range of LMS7002M and LMS6002D Lime FPRF transceivers. However it can bring more flexibilities in system design and implementation as will be shown in the following application examples.

The structure of LMS8001A is shown in Figure 1. It contains Low Noise Amplifiers (HFLNA), mixers (HFMIX), Power Amplifier Drivers (HFPAD) and PLL (HFPLL). All blocks are designed to run at very high frequencies (up to 10 GHz). There are four up/down frequency shift channels (A, B, C and D), each driven by the same LO from either HFPLL or external pin. There are also switches within each chain used to configure LMS8001A for different modes of operation. Chains can be configured by powering-down of appropriate blocks. Each channel can independently be configured to run in one of the following modes:

- TX mode: HFLNA and HFMIX1 are powered-down; HFMIX2 is enabled.
- RX mode: HFMIX2 is powered-down; HFPAD may be bypassed and powered down.
- Mixer only mode: HFLNA and HFMIX1 are powered-down; HFMIX2 is enabled; HFPAD is bypassed and powered down.
- Amplifier mode: HFMIX1 and HFMIX2 are powered down. No frequency conversion.
- No pass mode: all switches within the channel are open and all blocks are powered down.

Additionally the LMS8001A provides on chip low drop out voltage regulators (LDOs) to provide the required voltages to each part of the chip allowing operation from a single supply from 1.8V.

The RF and LO lines are differential throughout the whole chip.

HFMIX is a passive mixer that can be used either by itself or with HFPAD or HFLNA or any combination of these. HFPAD provides programmable gain. Similarly, HFLNA provides programmable gain and also helps to improve NF of the system.

HFPLL is a low phase noise fully self-contained fractional-N mode synthesizer covering 300 MHz to 9.2 GHz. It includes voltage controlled oscillator (VCO), programmable feedback divider (FBDIV) with delta sigma modulator (DSM), programmable feed forward divider (FFDIV), phase frequency detector (PFD), charge pump (CP), on chip loop filter and lock detector. The synthesizer can be operated in either integer or fractional mode. Integer mode has the lowest phase noise. Fractional mode allows for fine adjustment of operational frequency. Alternatively, fine frequency control is also possible to implement by using fractional-N PLL or NCO of LMS7002M. Although the HFPLL is a fully self-contained synthesizer, it is also possible to use an external synthesizer. The HFPLL loop filter includes a fast lock mode to allow fast change of frequencies.

The chip is fully configurable via Serial Port Interface (SPI). Basic options of operation are also controllable via the chip pins.

Parameter	Min.	Typ.	Max.	Unit	Condition/Comment
Operating Temperature Range	-40	25	85	°C	
Storage Temperature Range	-65	25	125	°C	
HFPLL VCO Operating Frequency Range	4.1		9.2	GHz	
HFPLL Operating Range	0.3		9.2	GHz	Min depends on feed forward divider
HFPLL Frequency Resolution			38.14	Hz	At 40 MHz PLL reference clock. No reference prescaler engaged. Feed forward division set to 1.
HFPLL Reference Clock	10	40	70	MHz	For continuous LO frequency range. No reference prescaler engaged.
Analog Supply Voltage, High (VDDAH)	1.71	1.8	1.89	V	Used for HFPAD
Analog Supply Voltage, Low (VDDAL)	1.2	1.25	1.3	V	Generated using integrated LDOs
Digital Core Supply Voltage	1.1	1.2	1.3	V	
TX Mode Supply Current			250 @ 1.2V 220 @ 1.8V	mA	All channels (A, B, C and D) active. LNA not active. HFPAD max current. LO IQ generation.
RX Mode Supply Current			250 @ 1.2V 250 @ 1.8V	mA	All channels (A, B, C and D) active. HFPAD bypassed. HFLNA max current. LO IQ generation.
Digital Peripheral (IO) Supply Voltage	1.71	2.5	3.6		
Output 1-dB Compression Power		7		dBm	CW
External LO Divider Range	1		16		Power of 2 step size
SPI Clock Frequency			50	MHz	

Table 1: General specifications

Parameter	Min.	Typ.	Max.	Unit	Condition/Comment
RF Channel Frequency Range	0.8		10	GHz	
HFLO Leakage		TBD	-35	dBc	TBC
HFPAD					
Frequency Range	0.8		10	GHz	Tunable band, set by external matching circuit.
Gain (G_{NOM})				dB	Depends on the output matching network and gain control value. Typically maximum linearity is achieved at gain levels 7 – 10 dB. Higher gains can be achieved at the cost of reduced linearity.
Gain Control Range	G_{NOM}-15		G_{NOM}	dB	
Gain Control Step		1		dB	
Output					Differential. Easy to match to 50 Ω single ended. Output is open-drain.
NF			6	dB	
Output IP3		20			
Output 1-dB Compression Power		10			CW
Bypass IIP3	15	20		dBm	Depends on the final channel architecture and output matching.
Supply		1.8		V	
Current			50	mA	Per HFPAD. Proportional to Gain control value.
HFLNA					
Frequency Range	0.8		10	GHz	Tunable band set by external matching circuit.
Primary Frequency Range	3.8		6.0	GHz	Performance outside of this range will gradually deteriorate
Gain (G_{NOM})		15		dB	“Primary” frequency range. Gain outside of this range will deteriorate.
	5				Complete frequency range
Gain Control Range	G_{NOM}-8		G_{NOM}	dB	
Gain Control Step		0.5	1.0	dB	
NF			3	dB	@ Maximum gain. “Primary” frequency range.
			5	dB	Complete frequency range.
IIP3		+5		dBm	@ Maximum gain. “Primary” frequency range.
IP1dB		-5		dBm	@ Maximum gain. “Primary” frequency range.
Supply		1.8		V	
Current			45	mA	Per LNA.
HFMIX					
IIP3		+15		dBm	In high LO drive at 4.8GHz.
Conversion Loss			7	dB	Single side band.
NF		8		dB	Single side band.
Supply		1.2		V	
Current			20	mA	Per Mixer. Drivers. Scales with LO frequency.

Table 2: General RF specifications (**to be updated**)

Parameter	Min.	Typ.	Max.	Unit	Condition/Comment
VCO Operating Frequency Range	4.1		9.2	GHz	
PLL Operating Range	0.30		9.2	GHz	Min depends on feed forward divider.
Frequency Resolution			38.14	Hz	At 40 MHz PLL reference clock. No reference prescaler engaged. Feed forward division set to 1.
Reference Clock	10	40	70	MHz	For continuous LO frequency range. No reference prescaler engaged.
881.5 MHz Phase Noise 1 kHz offset 10 kHz offset 100 kHz offset 1 MHz offset		 -103.1 -108.9 -112.5 -132.7		dBc/Hz	
4.1 GHz Phase Noise 1 kHz offset 10 kHz offset 100 kHz offset 1 MHz offset		 -90.4 -95.3 -101.3 -120.7		dBc/Hz	
8.0 GHz Phase Noise 1 kHz offset 10 kHz offset 100 kHz offset 1 MHz offset		 -84.7 -94.5 -94.3 -115.7		dBc/Hz	
Reference Spurious Outputs			-60	dBc	
Other Spurious Outputs			-60	dBc	
Settling time			10 50	µs	To 5 kHz (In fast lock mode) To 250 Hz
LO Phase Rotation Step		90		degrees	Up to 4.6 GHz
LO Phase Rotation Accuracy		+/- 8		degrees	At 4.0GHz
Current			20 @ 1.8V	mA	VCO Core
			50 @ 1.2V	mA	Charge Pump & Dividers
			120 @ 1.2V	mA	LO Distribution Max, 4 channels, 4 IQ generation blocks. Scales with number of channels and IQ generation blocks.

Table 3: HFPLL specifications

APPLICATION EXAMPLES

A very flexible solution using single LMS7002M and four LMS8001A chips is shown in Figure 2. Only one LMS8001A up/down frequency shift channel is used in order to get more flexibility in RF frequency selection. Unused channels can be left unconnected and powered down. External PA and other details of Figure 1 are not shown for clarity. Each RX chain has its own dedicated LMS8001A configured in RX mode. Each TX chain has its own dedicated LMS8001A configured in TX mode. LMS8001 chains are configured by switches and/or power-down of blocks (illustrated as grayed in Figure 2). RXLNA3 input of both RX chains is broad band matched for sniffing application, for example. It can sniff up to 3.8 GHz range. RXLNA1 and RXLNA2 inputs of both RX chains can be matched to the same or different frequencies/Bands as required.

There are two SAW filters in each RX chain. One after antenna is used as Band selection filter. IF SAW is in fact a channel select filter and can help enormously to filter out unwanted adjacent channels and blockers. There are two additional matching networks. One matches antenna to LMS8001A input and another LMS8001A output to IF SAW filter. RF switch selects LMS8001A output to RXLNA1 or RXLNA2 path since only one LNA can be active at a given time.

Architecture of TX paths is similar only the signal direction is reversed. IF SAW can be used to further filter out in Band spurs coming from LMS7002M. These are within the specification level however for some more demanding applications this option can be very useful.

This architecture offers to implement following options

By setting RXHFA = RXHFB and TXHFA = TXHFB (RXHFA != TXHFA or RXIF != TXIF) then the system implements 2x2 MIMO FDD with the frequency range extended up to 12 GHz. 2x2 MIMO TDD is also simple to implement by having RXHFA = RXHFB = TXHFA = TXHFB and RXIF = TXIF, covering the same up to 12 GHz range.

FDD/TDD SISO mode can be achieved using the same setup as above, by just powering down one RX and one TX chain (RX B and TX B for example) of LMS7002M and removing IF and HF off chip components related to these. Powering down one TX and one RX chain in LMS7002M and removing unused IF and HF off chip components saves a lot of current as well as space. Frequency coverage is the same (up to 12 GHz).

In case of RXHFA != RXHFB and TXHFA != TXHFB where RXIF and TXIF may or may not be the same, system is capable of receiving two different frequencies/Bands and transmit at two different

frequencies/Bands. In fact, the system behaves as two independent transceivers, covering as before up to 12 GHz range. This setup can be used in carrier aggregation applications. If transmitting at two different frequencies/Bands of two received and aggregated carriers is not required, unused TX chain of LMS7002M and related IF/HF off chip components can be powered down or removed saving space and supply current.

The architecture shown in Figure 2 can further be cost optimized for the applications which do not require such flexibility. For example, extending frequency range of LMS7002M 2x2 MIMO capability can be achieved by using single LMS8001 but engaging all four RF channels. Two channels should be configured in RX mode and another two In TX mode. Up link/down link RF frequency separation will be implemented by LMS7002M.

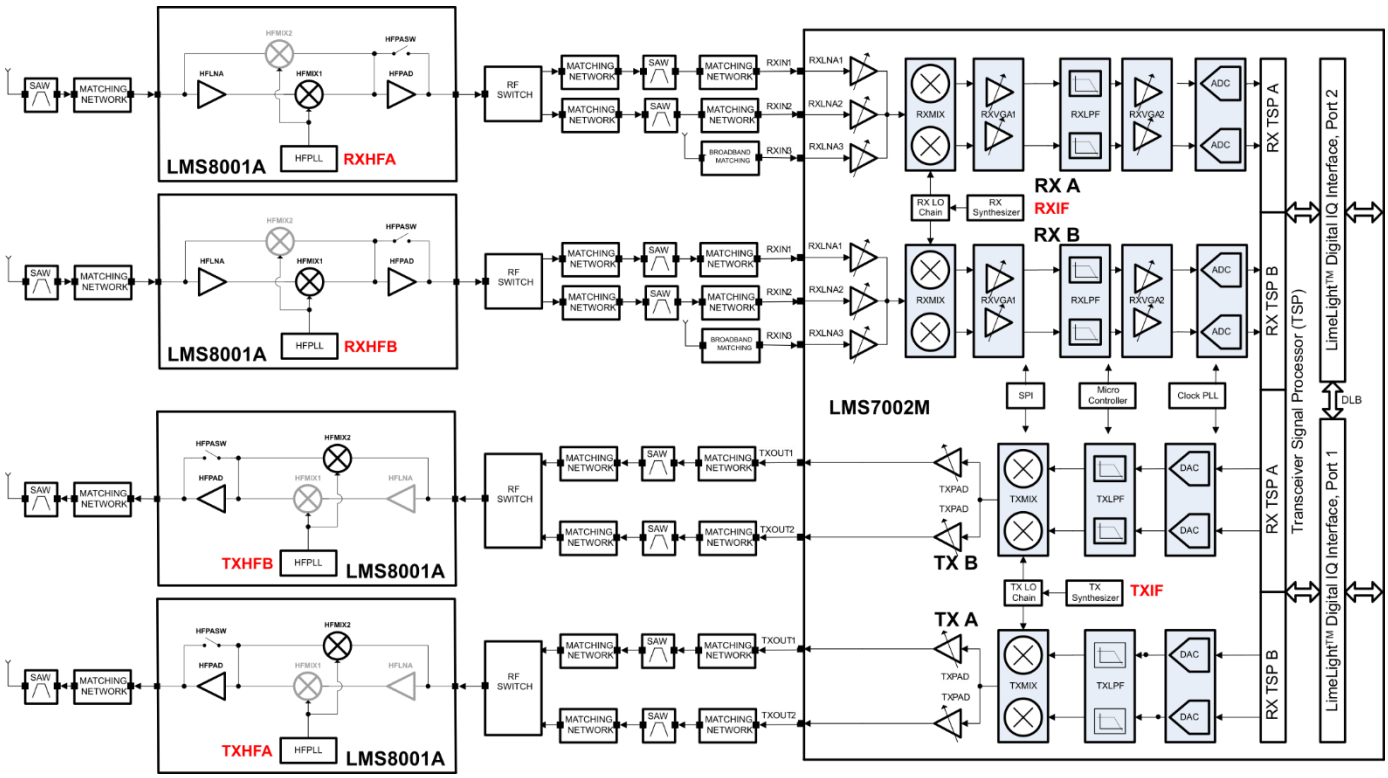
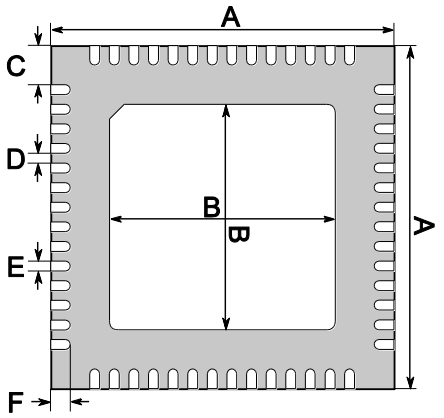


Figure 2: The most flexible LMS7002M and LMS8001A connectivity

PACKAGE OUTLINE AND PIN DESCRIPTION



A	7.0 mm
B	4.6 mm
C	0.8 mm
D	0.2 mm
E	0.2 mm
F	0.4 mm

Figure 3: Package Drawing, QFN package, 56-pin, 7mm x 7mm (top view)

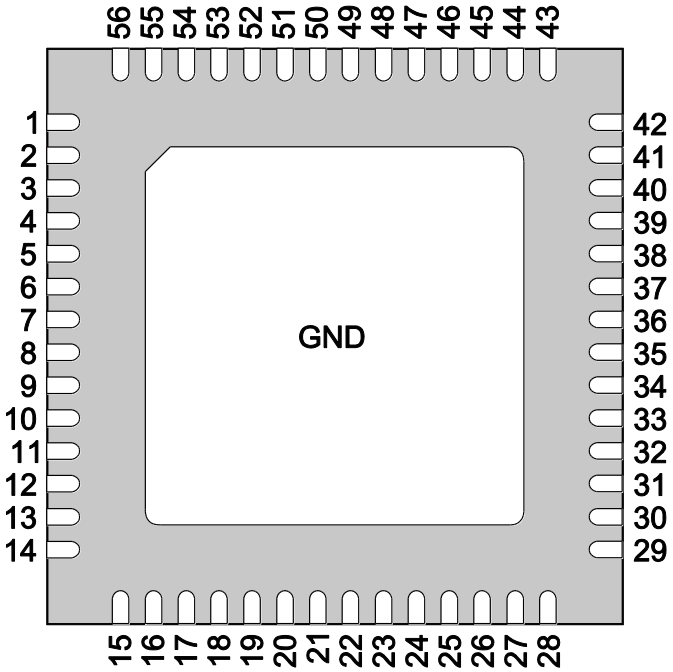


Figure 4: Pin-out

Pin	Name	Type	Description	Notes
GND	GND	GROUND	Ground. Connect paddle to good ground with as many as possible vias to ensure proper RF grounding.	
1	NC	NC	Not connected	
2	EXTLO_P	RF IN	External LO +	
3	VDD18_BIAS	Analog supply	1.8 V supply voltage for bias.	
4	HFINA_N	RF IN	Channel A RF input -	
5	HFINA_P	RF IN	Channel A RF input +	
6	VDD_HFINA	Analog supply	Supply voltage for Channel A LNA.	
7	VDD_HFINAB	Analog supply	1.8 V supply voltage for LDOs providing LNA supply for Channels A & B.	
8	VDD_HFINB	Analog supply	Supply voltage for Channel B LNA.	
9	HFINB_P	RF IN	Channel B RF input +	
10	HFINB_N	RF IN	Channel B RF input -	
11	SPI_SEN	DIG I	SPI SEN	
12	SPI_SDIO	DIG I/O	SPI SDIO	
13	SPI_SCLK	DIG I	SPI SCLK	
14	SPI_SDO	DIG O	SPI SDO	
15	GPIO8	DIG I/O	GPIO 8 pad	
16	VDD_DIG_IO	Digital supply	Supply voltage for digital IO output drivers	
17	VDD12_DIG_CORE	Digital supply	Supply voltage for digital core. Generated by on-chip LDO.	
18	RESETN	DIG I	Chip reset. Active low.	
19	HFOUTB_P	RF OUT	Channel B RF output +	
20	HFOUTB_N	RF OUT	Channel B RF output -	
21	VDD12_LOBUFB	Analog supply	Supply for channel B LO buffer. Generated by on-chip LDO.	
22	VDD18_LOBUFBC	Analog supply	Supply voltage for channel B & C LO buffer LDOs.	
23	VDD12_LOBUFC	Analog supply	Supply for channel C LO buffer. Generated by on-chip LDO.	
24	HFOUTC_N	RF OUT	Channel C RF output -	
25	HFOUTC_P	RF OUT	Channel C RF output +	
26	GPIO0	DIG I/O	GPIO 0	
27	GPIO1	DIG I/O	GPIO 1	
28	GPIO3	DIG I/O	GPIO 3	
29	GPIO2	DIG I/O	GPIO 2	
30	GPIO5	DIG I/O	GPIO5	
31	GPIO4	DIG I/O	GPIO4	
32	GPIO6	DIG I/O	GPIO6	
33	GPIO7	DIG I/O	GPIO7	
34	HFINC_N	RF IN	Channel C RF input -	
35	HFINC_P	RF IN	Channel C RF input +	
36	VDD_HFINC	Analog supply	Supply voltage for Channel C LNA.	
37	VDD_HFIN_CD	Analog supply	1.8 V supply voltage for LDOs providing LNA supply for Channels C & D.	
38	VDD_HFIND	Analog supply	Supply voltage for Channel D LNA.	
39	HFIND_P	RF IN	Channel D RF input +	
40	HFIND_N	RF IN	Channel D RF input -	
41	VDD18_VCO	Analog supply	1.8 V supply for VCO.	
42	VDD18_PLL	Analog supply	1.8 V supply for three on-chip PLL LDOs.	
43	VDD12_PLL_CP	Analog supply	1.2 V supply for PLL charge pump. Generated by on-chip LDO.	
44	VDD12_PLL_DIV	Analog supply	1.2 V supply for PLL divider. Generated by on-chip LDO.	
45	VDD12_PLL_CLK_BUF	Analog supply	1.2 V supply for LO distribution. Generated by on-chip LDO.	
46	HFOUTD_P	RF IN	Channel D RF output +	
47	HFOUTD_N	RF IN	Channel D RF output -	
48	VDD12_LOBUFD	Analog supply	Supply for channel D LO buffer. Generated by on-chip LDO.	
49	VDD18_LOBUFAD	Analog supply	Supply voltage for channel A & D LO LDOs.	
50	VDD12_LOBUFA	Analog supply	Supply for channel A LO buffer. Generated by on-chip LDO.	
51	HFOUTA_N	RF IN	Channel A RF output -	
52	HFOUTA_P	RF IN	Channel A RF output +	
53	PLLCLK	CLOCK	PLL reference clock.	
54	REXT	ANALOG	External 10 kΩ resistor.	
55	GLOBAL_PD	DIG I	Global power down.	
56	EXTLO_N	RF IN	External LO -	

Table 4: Pin descriptions

TYPICAL APPLICATION

Typical application circuit of LMS8001A RF matched to connect to LMS7002M is given in Figure 5.

To be added

Figure 5: Typical application circuit

ORDERING INFORMATION

Model	Temperature Range	Package Description
LMS8001	-40ºC to +85ºC	
LMS8001-REEL	-40ºC to +85ºC	
LMS8001-EVB		Evaluation board

REVISION HISTORY

The following table shows the revision history of this document:

Date	Version	Description of Revisions
23/02/2014	1.0.0	Initial version created.
21/05/2014	2.0.0	Additional up/down frequency channel added. Specification tables updated. Application diagrams updated accordingly.
22/05/2014	2.0.1	External LO divider added
	2.0.2	Two more RF channels added. LO phase rotation block added. Specification tables updated.
31/10/2014	3.0.2	Formatting corrected.
04/02/2015	3.0.3	Specification tables updated. Internal structure updated.
18/02/2015	3.0.4	Phase noise updated.
04/06/2015	3.0.5	Supply voltages and current consumption updated.
05/06/2015	3.0.6	Spec tables updated for clarity.
05/10/2015	4.0.1	Separated LMS8001A and LMS8001B datasheets. Added package description and pin-out information.
08/02/2016	4.0.2	Removed the reference prescaler feature. Updated the phase noise.
31/05/2016	4.0.3	Updated with PLL related measurement results.
	4.0.4	Updated with measurement data
30/09/2019	4.0.5	Added phase rotation step information

NOTICE OF DISCLAMER

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