

CONTROLLED IMPEDANCE

GENERAL PARAMETERS:

Top layer copper foil thickness: 17.5 um

Dielectric thickness from Top to L2 = 173um (6.8 mils)

Dielectric between Top layer and 2nd layer relative permittivity (Er): 4.2

Bottom layer copper foil thickness: 17.5 um

Dielectric thickness from L11 to Bottom = 173um (6.8 mils)

Dielectric between L11 layer and Bottom layer relative permittivity (Er): 4.2

Ground plane distance to trace on Bottom layer: 0.1mm

CALCULATIONS:

RF (Top)

RF (Bottom)

USB3.0 (Top)

Top layer copper foil thickness: 17.5 um

Track width = 0.325 mm (12.795 mils)

Dielectric thickness from Top to L2 = 173um (6.8 mils)

Dielectric between Top layer and 2nd layer relative permittivity (Er): 4.2

Approximate microstrip line impedance = 49.99 Ohms (+/- 10% tolerance)

100 Ohm coupled microstrip line (Top layer) characteristics:

Top layer copper foil thickness: 17.5 um

Track width = 0.2 mm (6.8 mils)
Track spacing = 0.14 mm (5.51 mils)

Track width/spacing ratio = 1.428

Dielectric thickness from top to L2 = 173um (6.8 mils)
Dielectric between Top layer and 2nd layer relative permittivity (Er): 4.2

Approximate coupled microstrip line impedance = 100.752 Ohms (+/- 10% tolerance)

50 Ohm coplanar waveguide with GND (Bottom layer) characteristics:

Bottom layer copper foil thickness: 17.5 um

Track width = 0.254 mm (10 mils)

Distance to GND: 0.1 mm (3.937 mils)

Dielectric thickness from Bottom to L11 = 173um (6.8 mils)

Dielectric between Bottom layer and L11 relative permittivity (Er): 4.2

Approximate microstrip line impedance = 49.99 Ohms (+/- 10% tolerance)

90 Ohm coupled microstrip line (Top layer, without GND) characteristics:

Top layer copper foil thickness: 17.5 um

Track width = 0.2 mm (6.8 mils)

Track spacing = 0.1 mm (3.93 mils)

Track width/spacing ratio = 2

Dielectric thickness from Top to 2nd layer = 173um (6.8 mils)

Dielectric between Top layer and 2nd layer relative permittivity (Er): 4.2

Approximate coupled microstrip line impedance = 90.5 Ohms (+/- 10% tolerance)

90 Ohm coupled microstrip line (Bottom layer) characteristics:

Bottom layer copper foil thickness: 17.5 um

Track width = 0.2 mm (6.8 mils)

USB3.0 (Bottom) Track spacing = 0.1 mm (3.93 mils)

Track width/spacing ratio = 2

Dielectric thickness from L11 to Bottom layer = 173um (6.8 mils)

Dielectric between L11 layer and Bottom layer relative permittivity (Er): 4.2

Approximate coupled microstrip line impedance = 90.5 Ohms (+/- 10% tolerance)

VERY IMPORTANT NOTES:

- 1) 0.35mm ring and 0.2mm drill via-in-pads (IC1) must be resin filled with metal cap
- 2) Solder mask: DARK BLUE, both sides, halogen free, glossy finish (NOT matte)
- 3) Silkscreen: white epoxy ink, halogen free, both sides. No silkscreen on pads.
- 4) DRCs must be run on Gerber files before building boards
- 5) Hole diameters are final manufactured diameters INCLUDING HOLE METALIZATION.
- 6) Minimum track spacing: 0.1 mm
- Minimum track width: 0.1 mm
- 8) Material:
- 7) There are plated and non-plated holes on the PCB
- IT-180A

PCB vendor to silkscreen UL and RoHS compliance marks, vendor logo and date code on bottom where shown Copper weight: External layers 0.5 oz+plating

- 9) Electrical test: 100 % netlist.
- 10) Boards are to be individually bagged.
- Total PCB thicknes: 1.6mm +/- 10%

 Via type #1

 Via type #2 (In pad, resin filled with metal cap)

 O.2mm drill O.4mm ring

 O.2mm drill O.4mm ring

 O.2mm drill O.4mm ring

 ASM TOP: Assembly top

 ASM BOT: Assembly bottom

 Mechanical 13: Component 3D body

USB3.0

STACKUP:

GERBER LAYER NAMES:

PP 6.8mil

CORE

CORE

PP 6.8mil

GTO Silkscreen
GTS Soldermask
(halogen free)
GTL 0.5oz+plating

G1 0.1oz

G2 0.1oz

G3 0.1oz

G4 0.1oz

G5 0.1oz

G6 0.1oz

G7 0.1oz

G8 0.1oz

G9 0.1oz

G10 0.1oz

GBL 0.5oz+plating
GBS Soldermask
(halogen free)

GBP Bottom solder pa

GBO Silkscreen

□ DC POWER JACK

Board Cutout

-11,84cm-

-10,00cm⁻

TH via

Top-Bot

ELECTRICAL LAYERS:

Top: RF/GND

L3: PWR/Signal/GND

L4: Signal/PWR/GND

L2: GND

L5: PWR/GND

L8: Signal

L9: Signal

L11: GND

L6: Signal/GND

L10: CLK/Signal