What is the LimeSDR

Danny Webster

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LimeSDR and The LMS7002M

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'Hackable'

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LMS7002M

FPGA

Cyclone IV

PCIe Link

USB3 Link

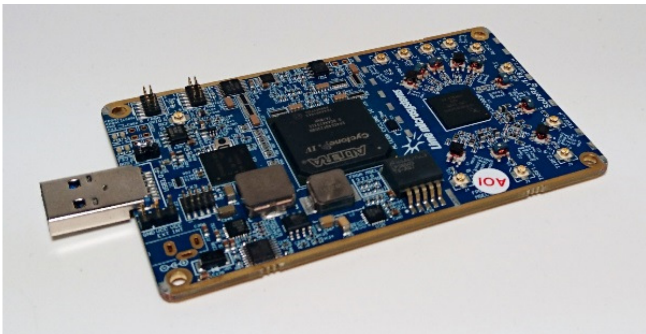
Open Source Software/Apps

COMPUTER

Multicore
GHz Processor
And Memory

WiFi/Ethernet/ ADSL Network

Radio is more than just a chip. Performance is critically linked to RF antennas, filtering and matching which end user selects/modify



LMS7002M

- 2nd Generation All CMOS Transceiver
- Low Power <2W
- Originally designed for 4G MIMO Femto and Pico Cell applications.
  - Home base stations
  - 64-QAM OFDM
  - 2.5dB NF
  - -15dBm CW Blocker
  - Requires external PA for Femto/Pico Applications

- Designed with Digital Predistortion for 4G in mind
  - PCIE version of LimeSDR
    - USB3 5Gb/s->640MB/s->80Ms/s
  - >50MHz IF Bandwidth
    - TX IF Bandwidth 100MHz
    - RX IF Bandwidth 80MHz
  - High speed ADC/DAC >100Ms/s
    - DAC 640Ms/s
    - ADC 160Ms/s
  - High speed digital interface
    - 120Ms/s MIMO DDR CLK=480, MCLK=240
    - 160Ms/s SISO DDR CLK=640, MCLK=160

LMS7002M FPRF Transceiver Block Diagram

High level of integration, including dual 12-bit ADC and DAC

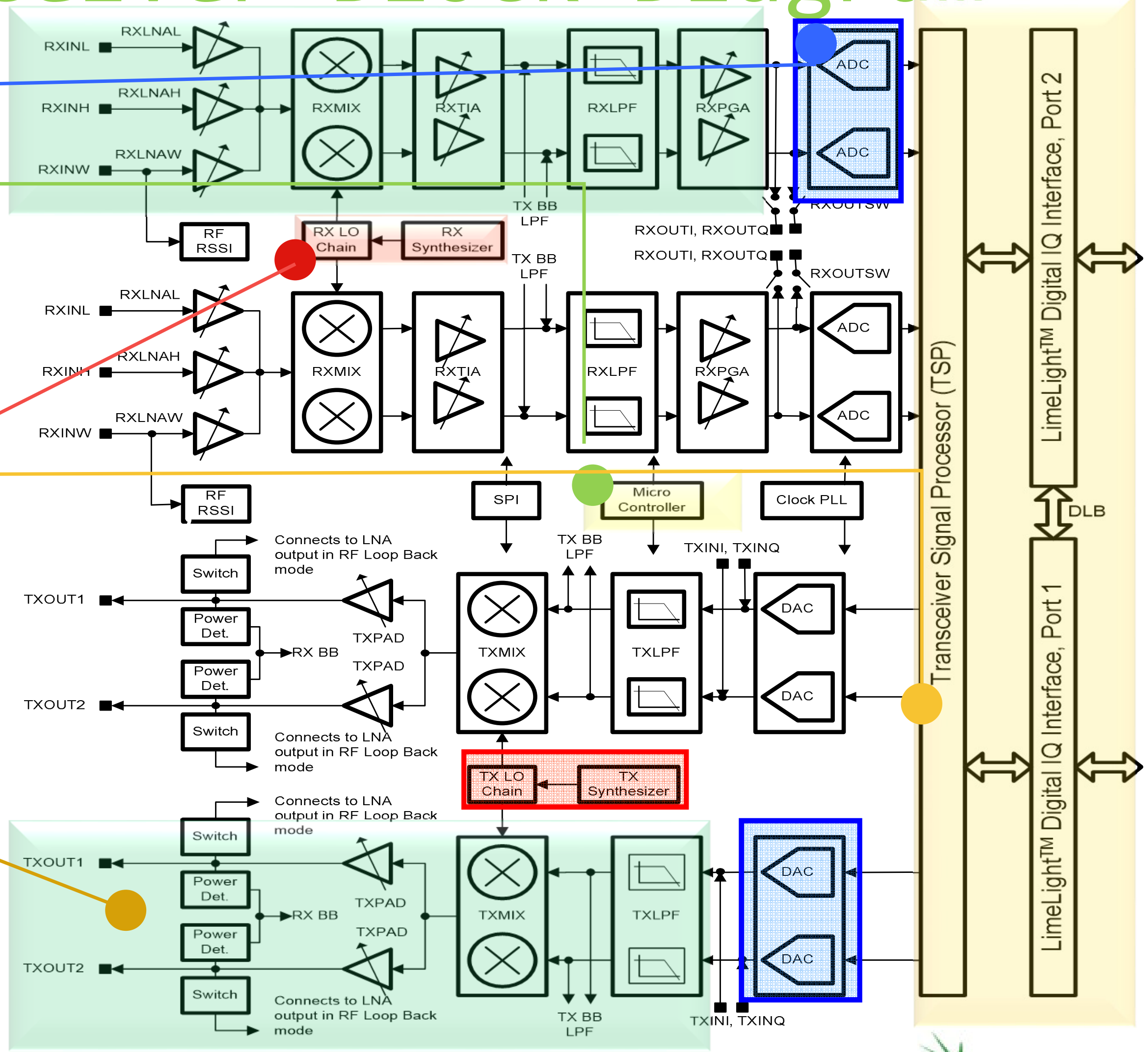
Integrated 8051 MCU

Transceiver Signal Processor block and LimeLight interface

Frequency

100KHz – 3.8GHz

Highly configurable RF gain and IF filter with numerous bypass options



LMS7002M

Field Programmable RF

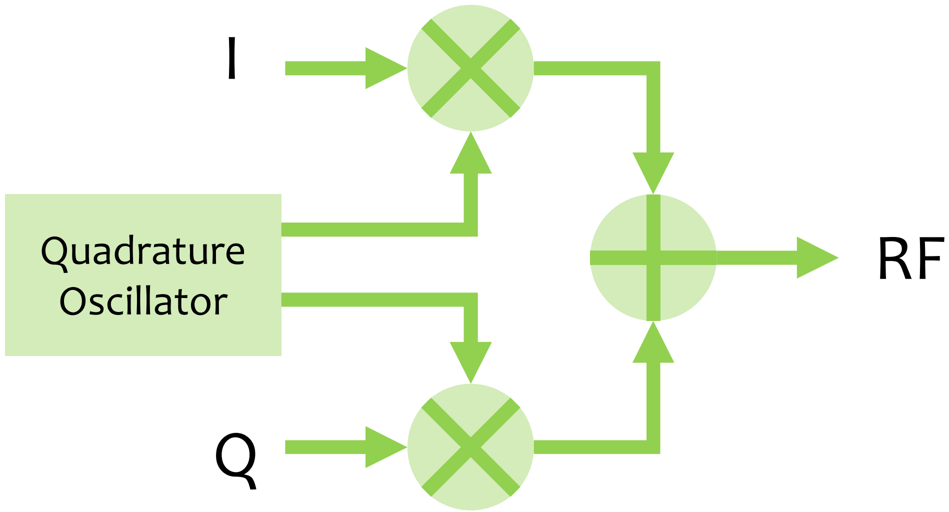
LMS7002M is very complicated!!!!

- **Lets break it down a bit**
- **MIMO Transeiver**
  - Up to 2 TX channels can operate simultaneously
  - Up to 2 RX channels can operate simultaneously.
- **Each TX channel**
  - 2 outputs
  - Low band (for <2.5GHz)
  - High band
- **Each RX channel**
  - 3 Inputs
  - Low band (opt for 800MHz)
  - Wide band (general purpose)
  - High band (opt for 2-3.8 GHz)
- **Synthesisers x3**
  - SXT – TX Synthesiser
  - SXR – RX Synthesiser
  - CLKGEN – Digital Circuits
- **Now let's explore the details, gradually…**

2. The Analogue Half of the LMS7002M

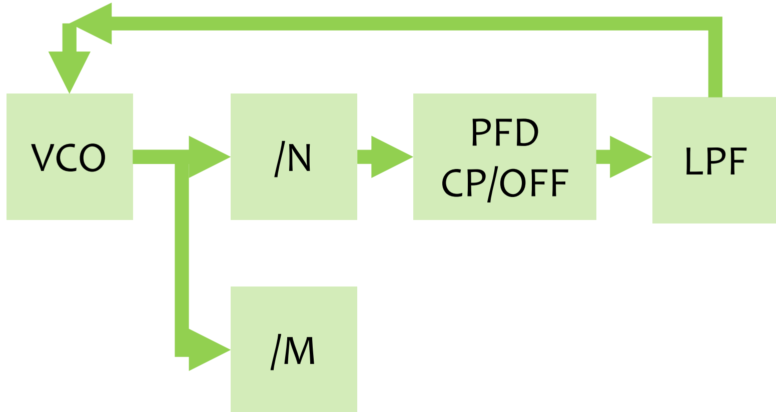
Simplified Vector (Homodyne) Transmitter

- **Homodyne 1930s**
  - Commonly called Zero IF
  - Similar to Hartley SSB Modulator
- **Analogue I,Q input signal**
  - describes a time varying vector of amplitude and phase described by Cartesian co-ordinates {I,Q}
  - Usually generated by software.
- **Frequency Mixer**
  - Converts I,Q into RF



Lime RF Synthesisers

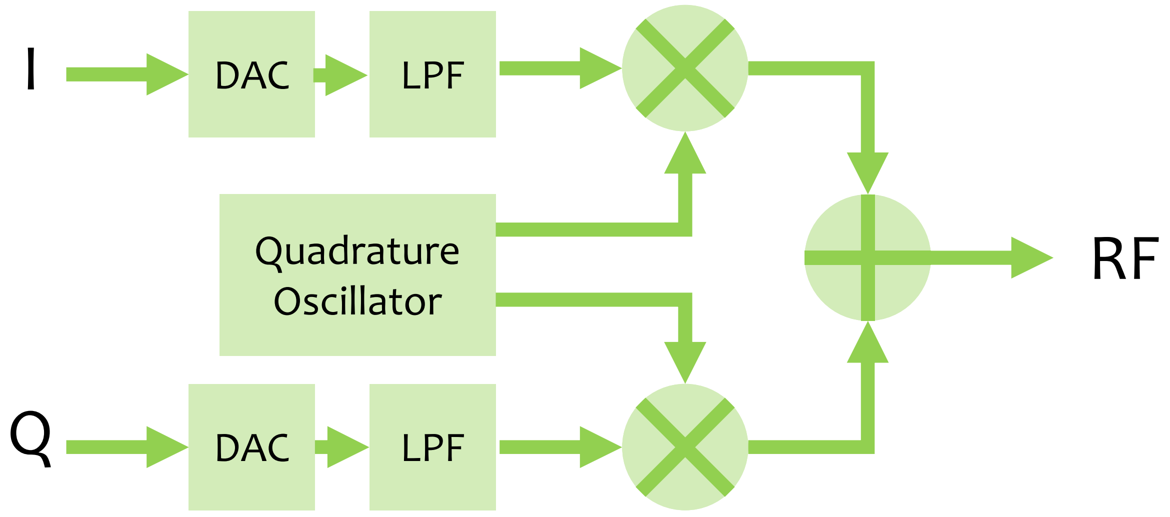
- **30.72MHz TXCO (Note boundary spurs)**
- **Typically -90dBc Phase Noise Plateau**
  - -100dBc with very low noise LDOs and very low phase noise TXCO
- **Integrated Phase Noise (LimeSDR)**
  - 0.14deg 100MHz
  - 0.17deg 215MHz (1024 QAM)
  - 0.31deg 500MHz
  - 0.46deg 850MHz (256 QAM)
  - 0.98deg 2145MHz (64 QAM)
  - 1.32deg 450MHz
- **Typically -155dBc Far out phase noise**



- **Delta Sigma Fractional N Type Synthesiser**
- **Programmable charge pump**
- **Programmable offset current**
- **Programmable loop filter**
- **TDD Mode SXT drives TX and RX**

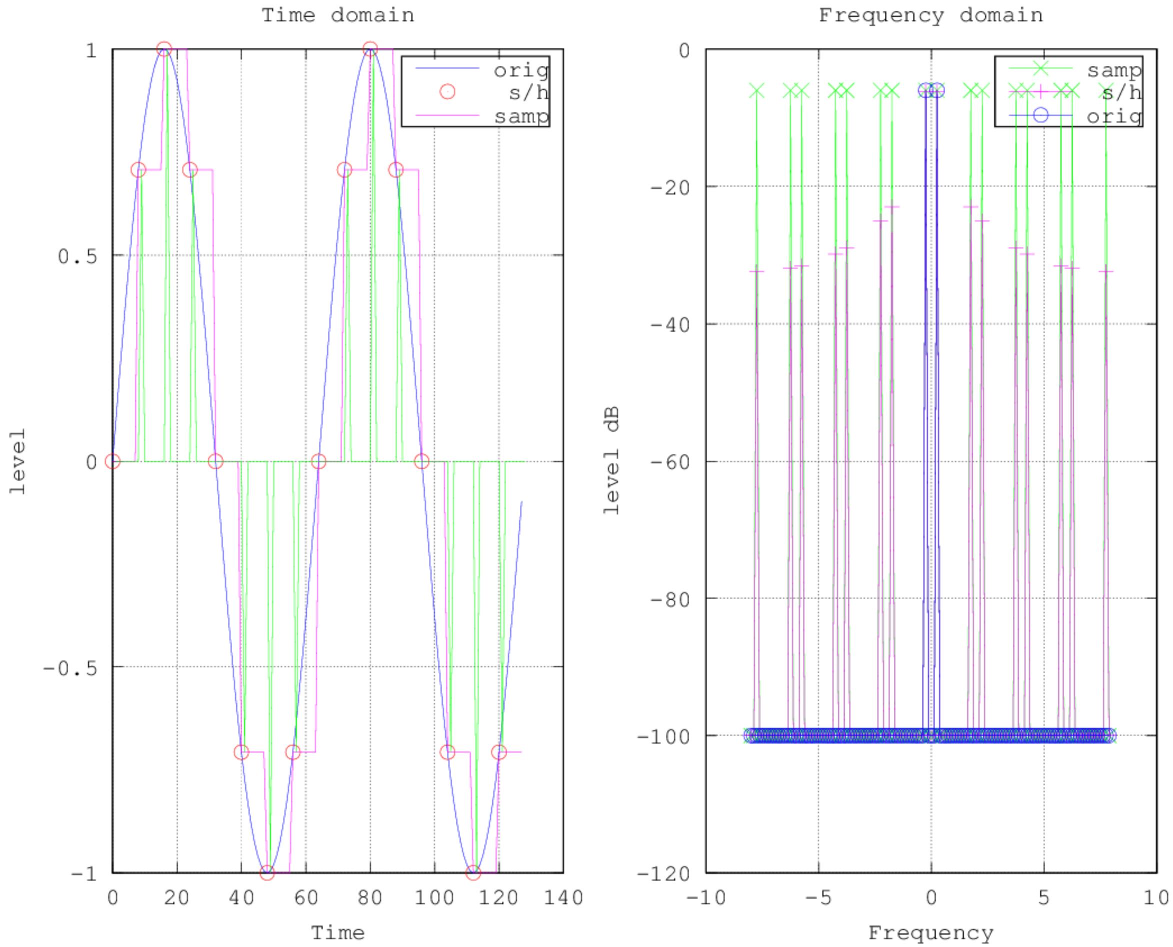
Digital Vector Transmitter

- **Digital I,Q data**
  - Converted to analogue by Digital to Analogue Converter (DAC)
  - DAC output cleaned by Low Pass Filter
    - Removes Aliases



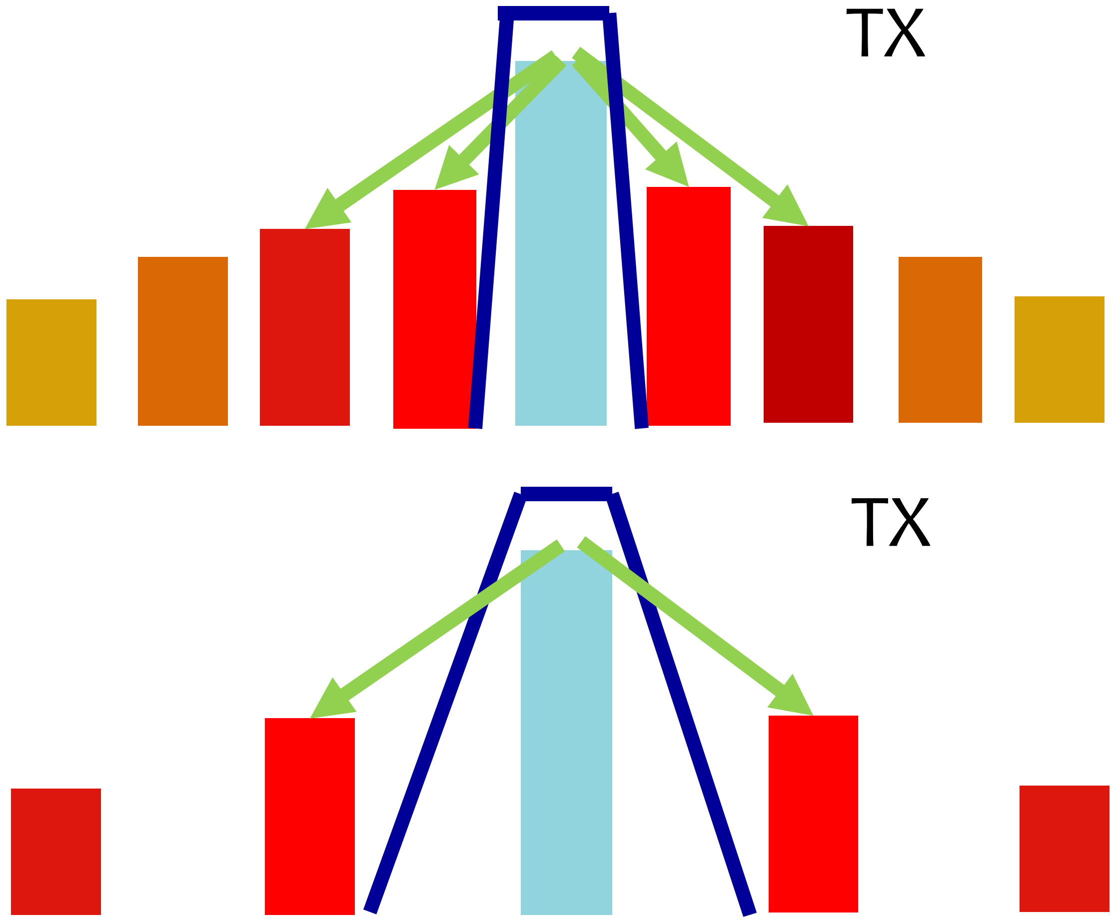
Sampled Data Systems and Nyquist

- **Sampled data systems**
  - look at a waveform only at fixed moments in time,
  - Points usually equally spaced.
- **Nyquist Sampling**
  - Signal frequency less than sampling rate
- **Reconstructed signal**
  - Sample and Hold
  - Aliases occur at frequencies above the sample rate.



Aliasing and the Adjacent Channel TX

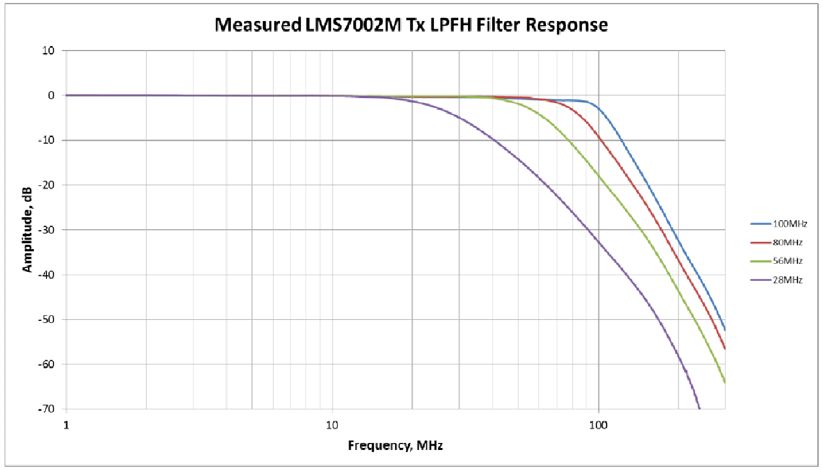
- **TX**
  - Aliases lead to transmitting interference in adjacent channels.
  - Not easy to filter.
  - Bad Neighbour!!!
- **What happens if we double the sampling rate?**
  - Oversampling
  - Aliases are further away.
  - Filter specification can be relaxed



Lime microsystems

LimeSDR TX Active Filters

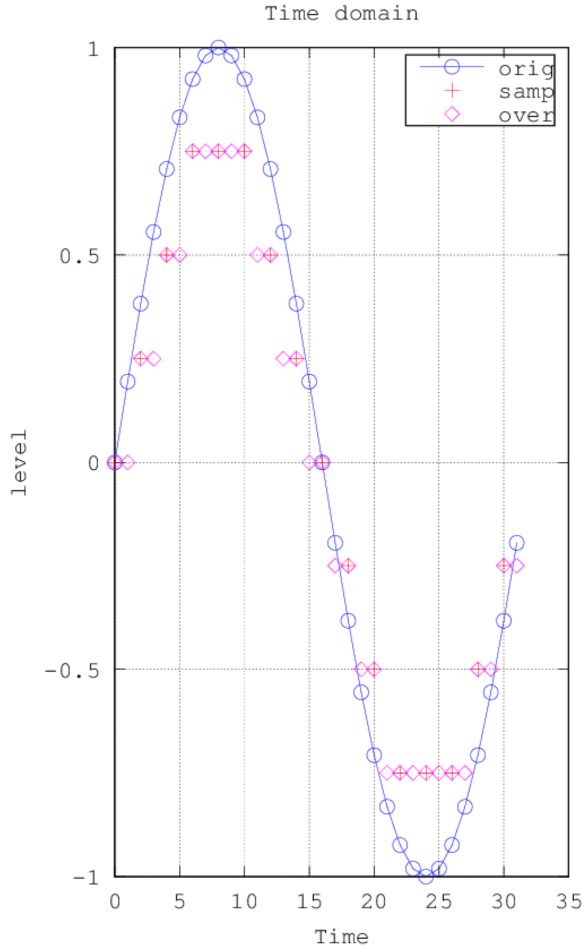
- **LPFL**
  - 4^{th} Order Chebychev
  - Optional Real Pole
- **LPFH**
  - 2^{nd} Order Butterworth

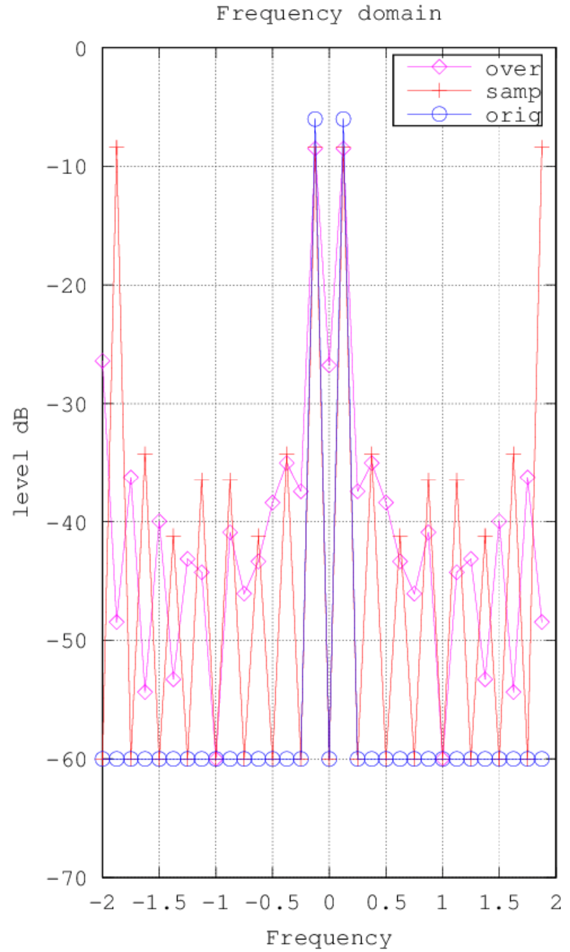


Quantisation and Noise

- **ADCs/DACs finite number of bits.**
  - Quantised data never completely accurate.
  - LMS7002M ENOB>=9 bit.
    - >56dB Dynamic Range
- **Illustrate with 3 bit ADC**
  - 8 levels available
  - Not all levels are normally used
  - Almost every sample point contains some error.
  - Looks like noise spread over the frequency domain.
  - Over sample to reduce noise.
    - 1 bit for ever x4 oversampling

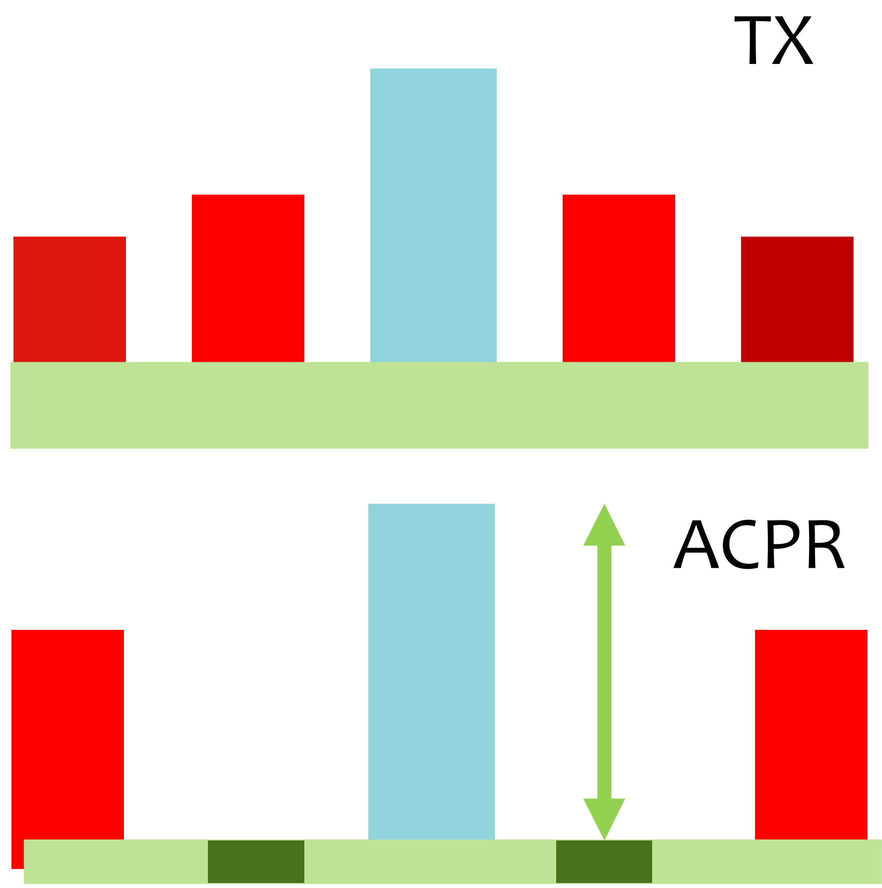
$$DR = 6.02 * N + 1.76dB$$





TX Oversampling and Quantisation Noise

- **Oversampling**
  - Reduces quantisation noise
  - Removes aliases away from signal
  - Improving Adjacent Channel Power Ratio (ACPR)
  - Good Neighbour
- **LimeSDR**
  - Intended to work with high oversampling.
  - E.g. 3G/4G Base station
    - Data Rate 30.72Ms/s
    - TX 245.76Ms/s x8 Oversample
    - RX 61.44Ms/s x2 Oversample



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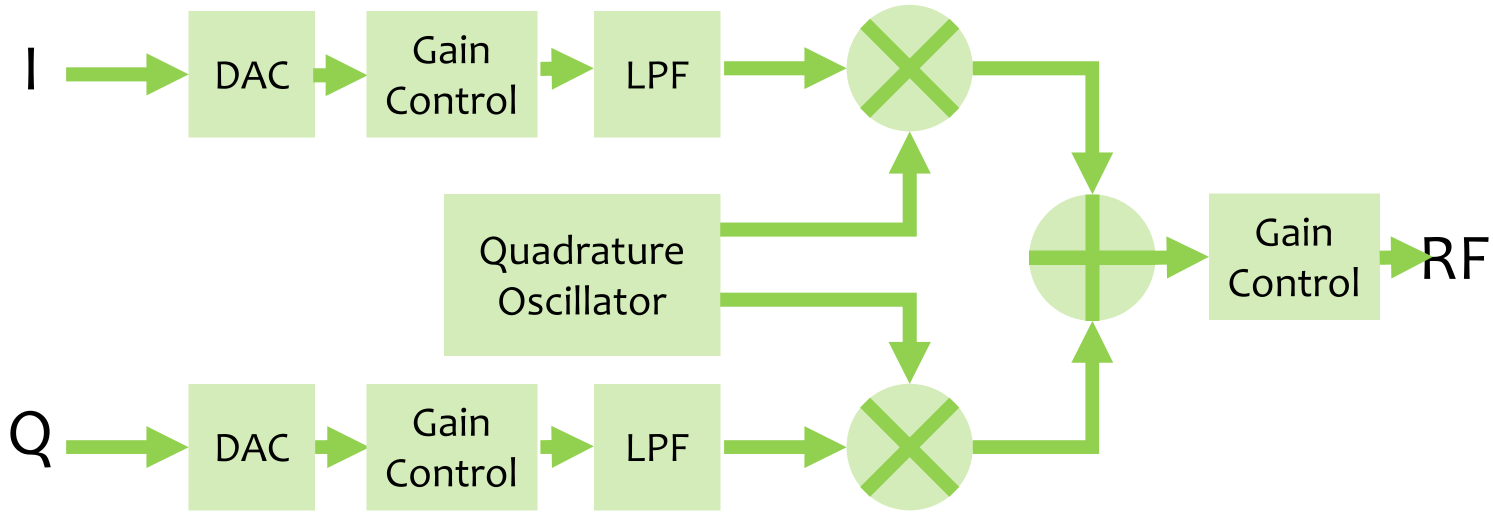
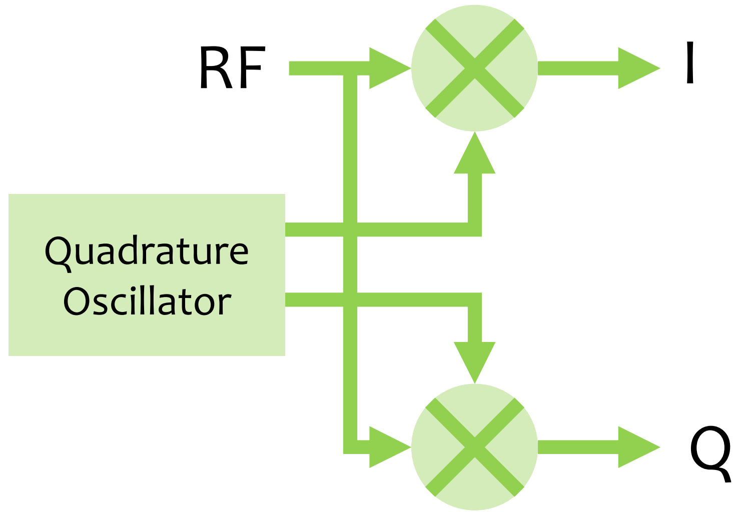
Digital Vector Transmitter

- **DACs and Mixers work best with optimum signal levels.**
  - Need gain control at input of mixer
    - LMS7002M TXIAMP
  - Need gain control to vary output level.
    - LMS7002M TXPAD
    - Power ramping for TDD systems e.g. GSM/EDGE
    - Power control for multiple access systems e.g. W-CDMA and LTE



Digital Vector Receiver

- **Zero IF Receiver**
  - Image Rejecting Mixer
- **Quadrature outputs processed by baseband.**
  - Noise of I and Q uncorrelated.
  - Better SNR



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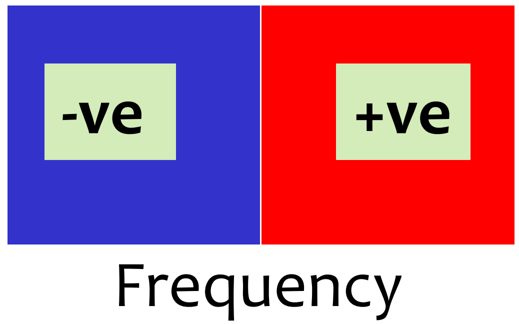
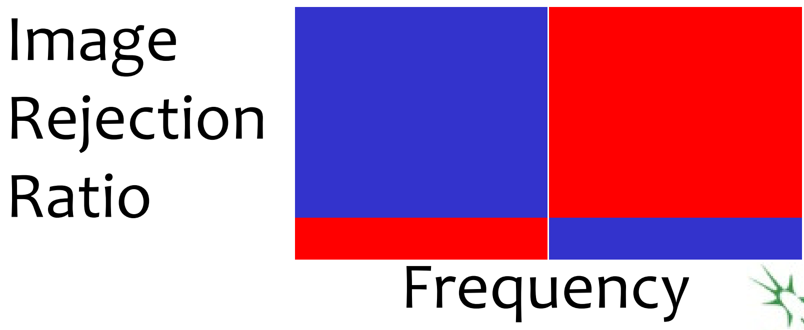
The Image Rejection Problem

- **Real modulation signals**
  - Positive frequency different to negative frequency.
- **Hetrodyne Type Receivers**
  - Image separated from Wanted signal by a frequency gap.
- **Homodyne Type Receivers**
  - Image shares the same frequency space.
  - Image frequencies looks like a “noise floor” to the wanted signal.
  - Image rejection affects SNR and EVM
  - Correct by calibration and digital techniques

Perfect Signal

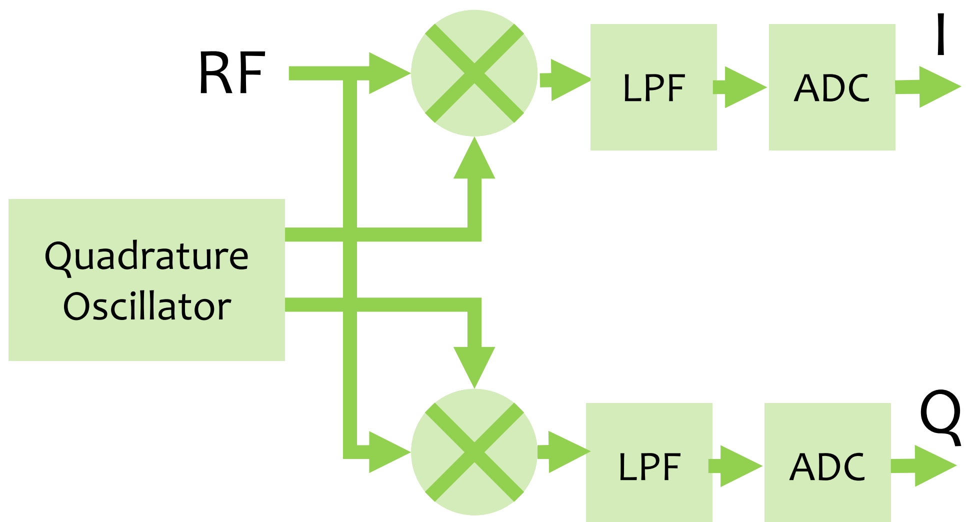


Real Received Signal



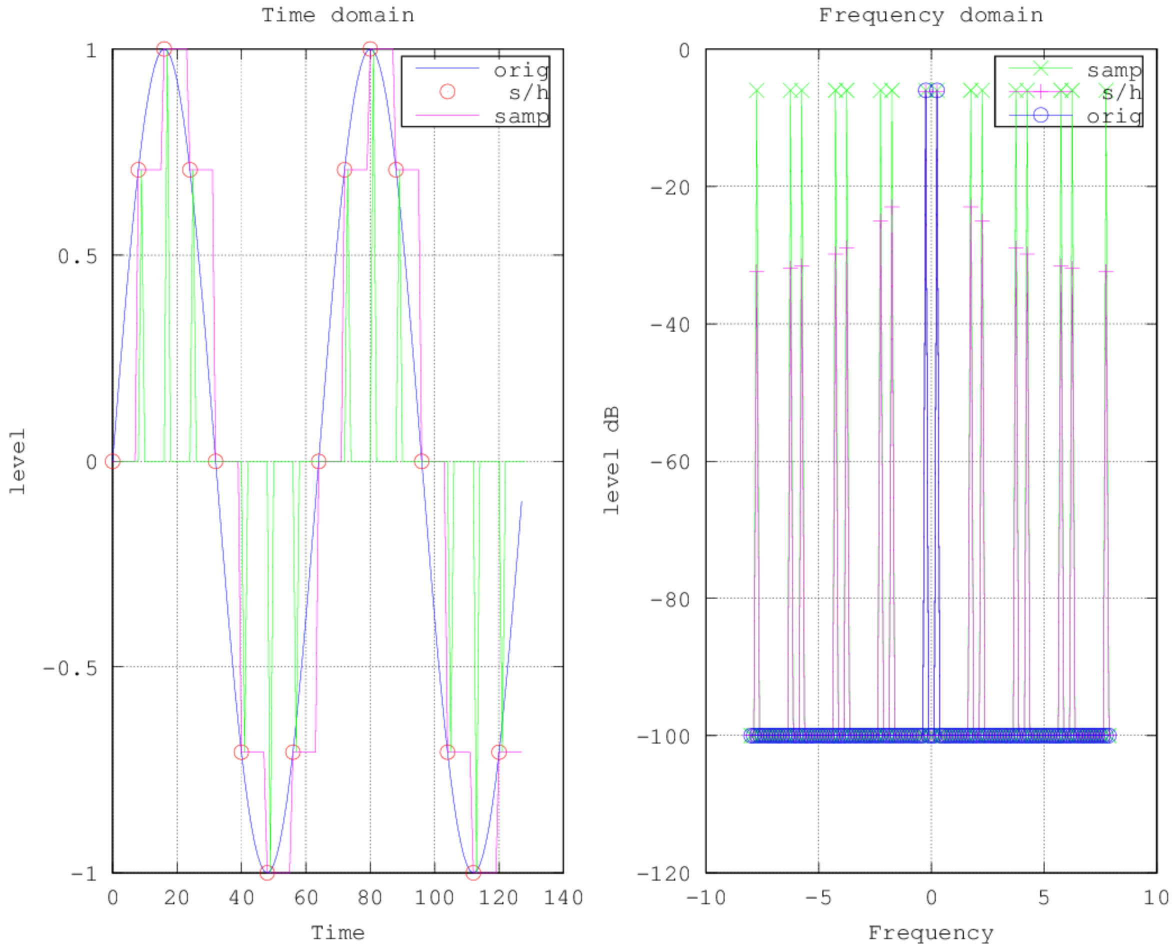
Digital Vector Receiver

- **I and Q channels filtered before quantisation.**
  - Prevents aliases
  - Reduces noise
- **Analogue to Digital Converters**
  - Convert analogue IF signals to digital.



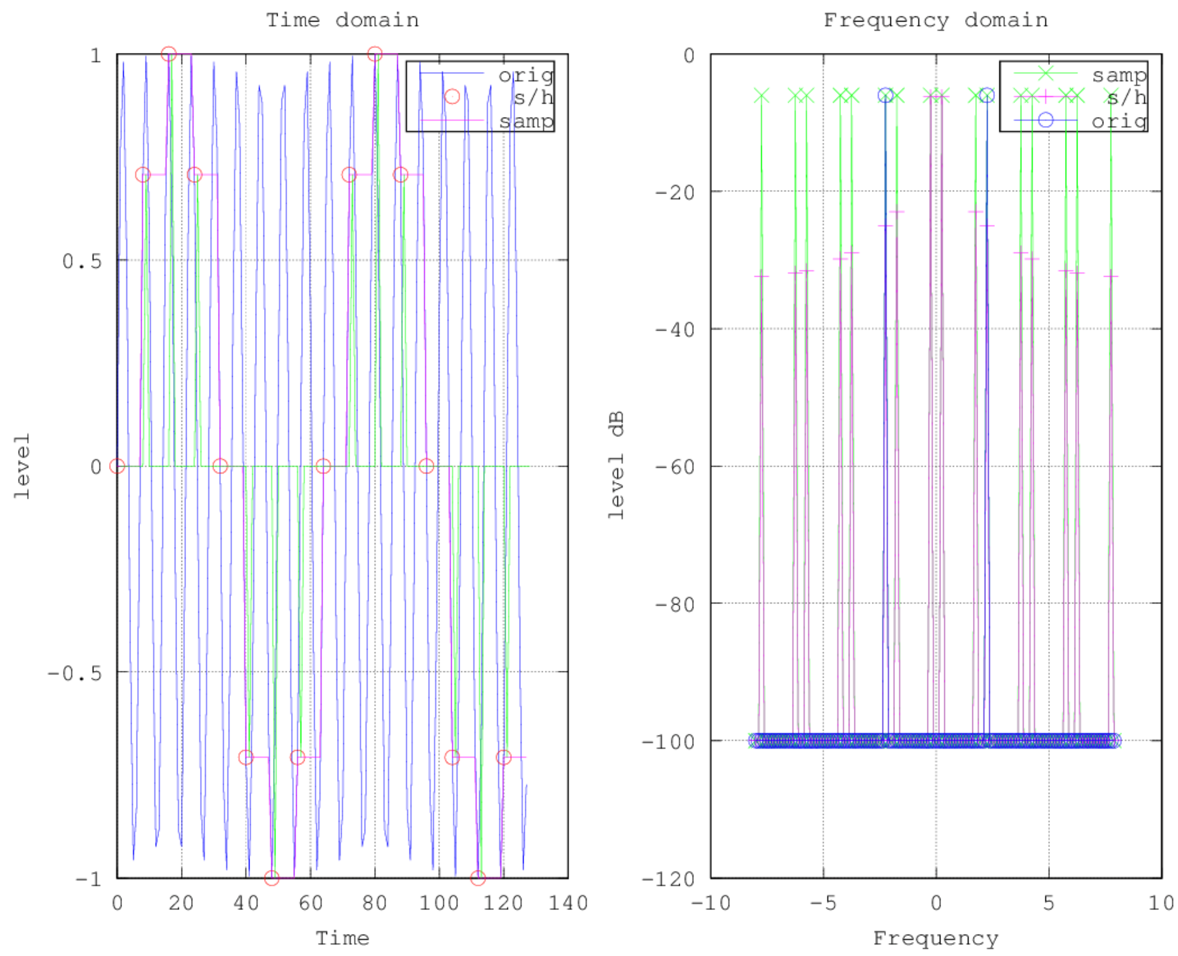
The wanted signal digitised

- **ADC Reverse of DAC process**
- **Almost…**
  - All aliases seen equally.
  - Unlike sample and hold case.



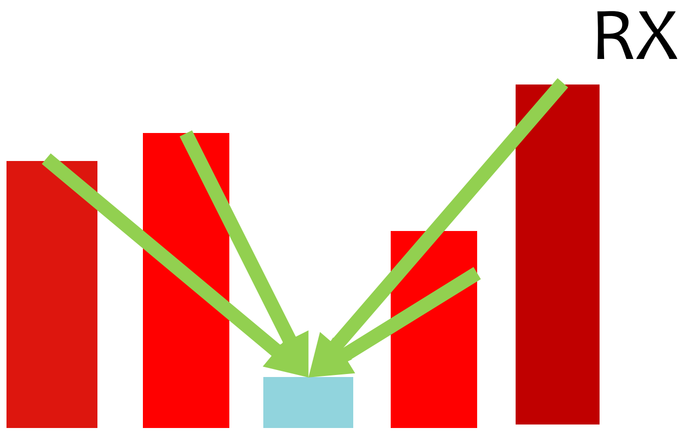
Let’s meet an alias signal

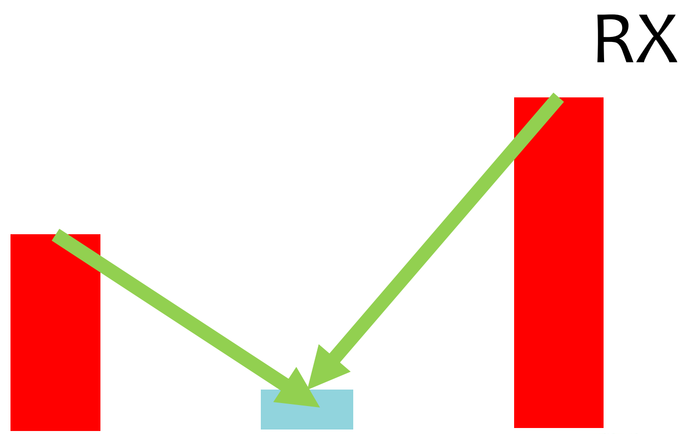
- **If we violate Nyquist Sampling,**
  - injecting an input signal whose frequency is higher than the sampling rate.
  - Cannot tell it apart from a signal that was lower than the Nyquist Sampling Rate.
- **Must filter before sampling to prevent interference.**



Aliasing and the Receiver

- **Adjacent channels are superimposed on the wanted signal degrading sensitivity.**
  - Common figure of merit Adjacent Channel Rejection.
- **Performance improved by**
  - Analogue IF filtering before ADC
  - Oversampling of ADC to move alias outside the bandwidth of IF and RF channel filters
- **Real Systems**
  - Adjacent channel rejection is a function of ADC bits, IF filtering and Forward Error Correction Coding.





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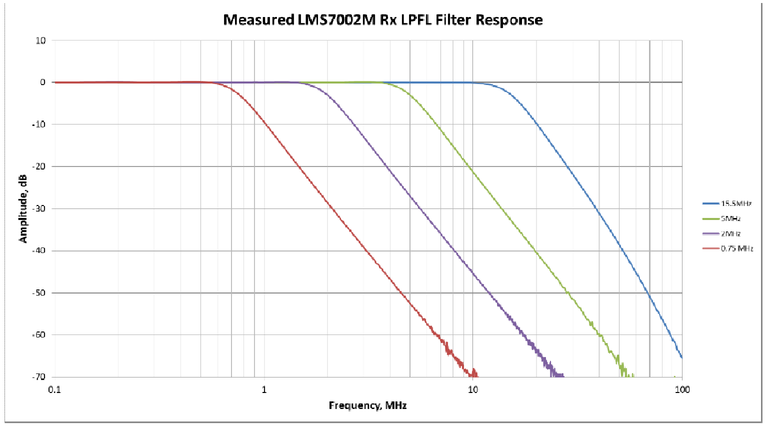
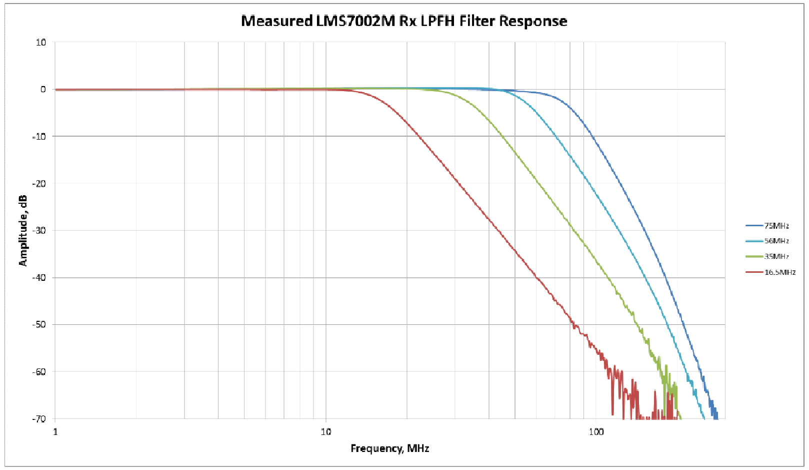
LimeSDR RX Active Filters

- **Nominal Filter Spec**
  - 0.5dB Ripple Chebychev
  - 3rd Order
  - TIA – Real Pole
  - LPFL/H – Complex Pole Pair
  - Ratio of TIA and LPF capacitance set filter shape.





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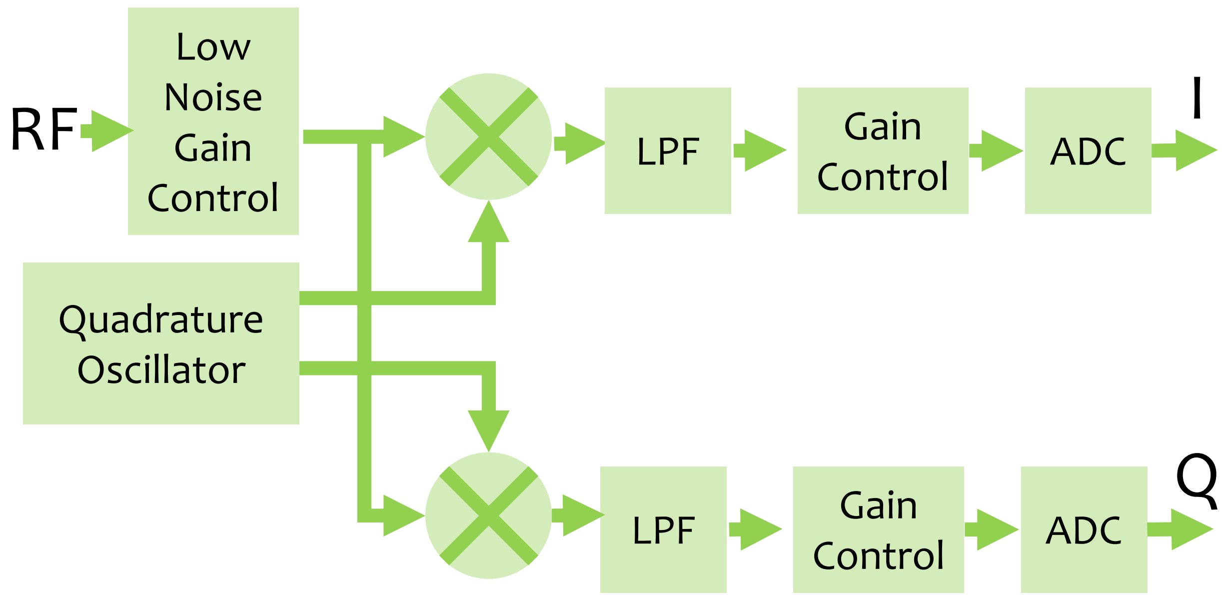
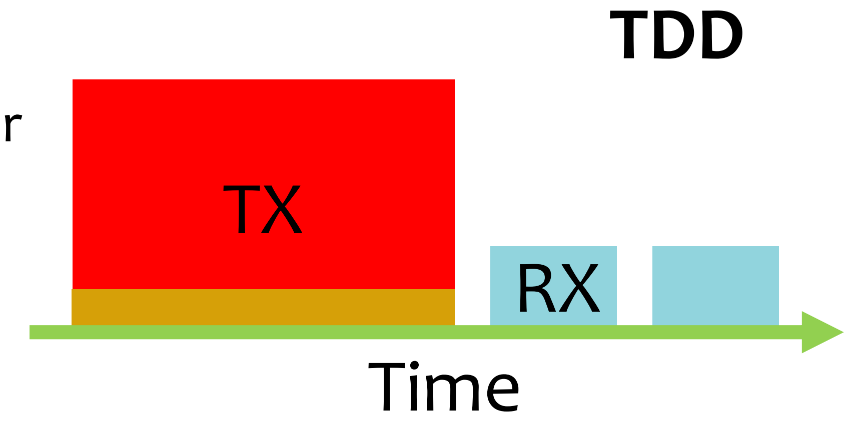
Digital Vector Receiver

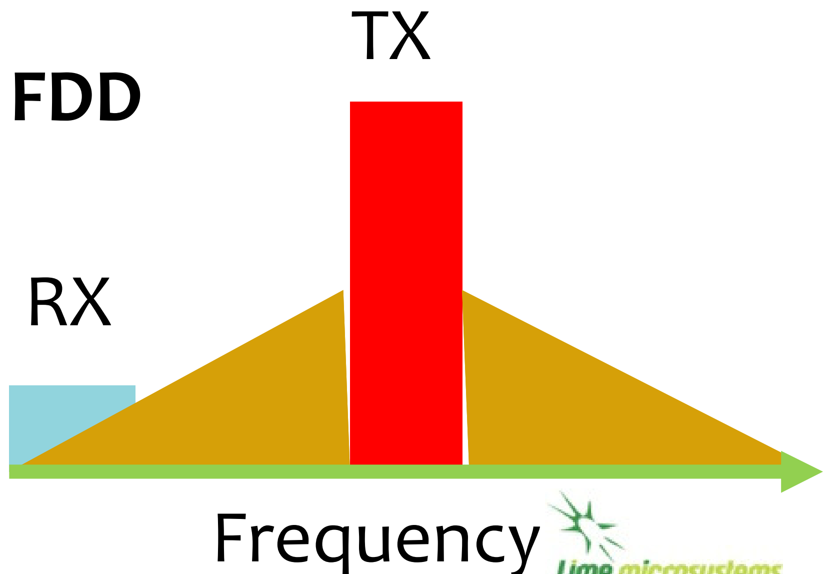
- **Mixers give best performance when levels are right.**
  - Variable gain Low noise LNA before mixer.
  - Avoid Mixer Overload for best dynamic range.
- **ADCs like big signals**
  - Variable gain before ADC (PGA)



TX Phase Noise Problem

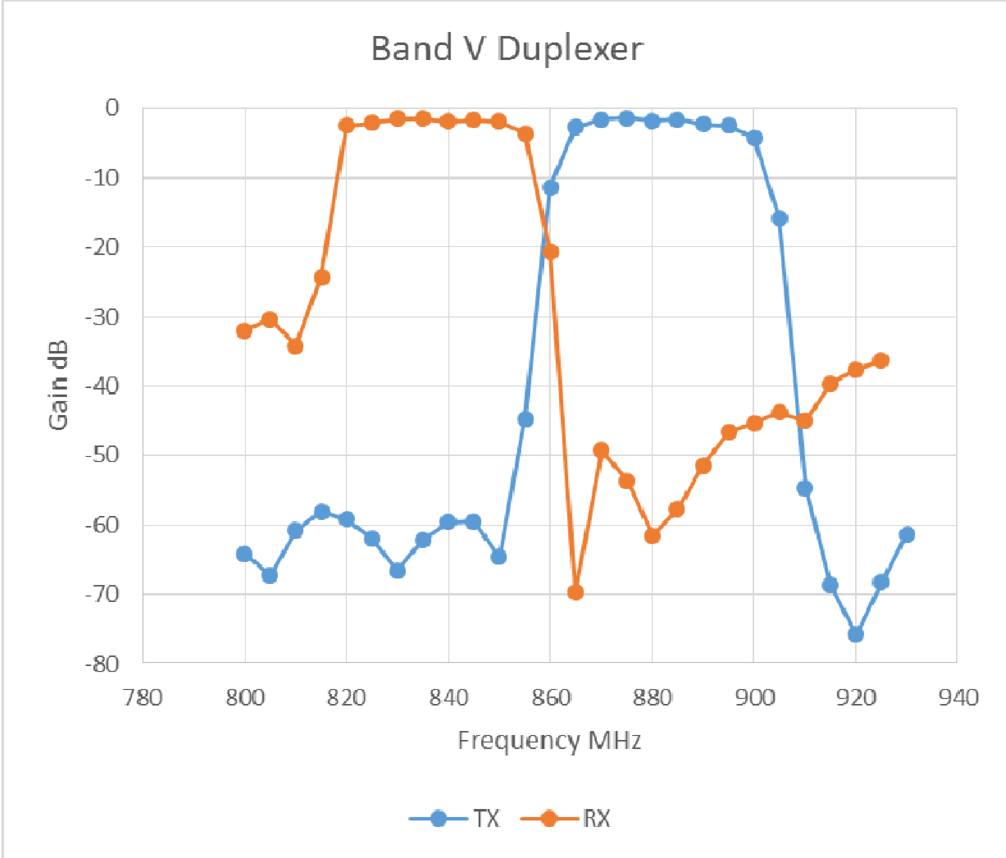
- **Your TX is often your worst interference signal**
  - Out of Band Noise, Quantisation and Active Filter
  - Far Out Phase Noise
  - Can deafen receiver, especially if TX is amplified before transmission and share antenna.
- **Time Division Duplexing (TDD)**
  - Transmitter switched off during receiving.
  - Cannot receive or transmit continuously!
- **Frequency Division Duplexing (FDD)**
  - Transmit and receive at different frequencies.
  - Duplexer filter to isolate TX and RX. Typ 50dB
  - +25dBm-155dBc-50dB=-180dBm/Hz (Below thermal noise+NF -171.5dBm/Hz)





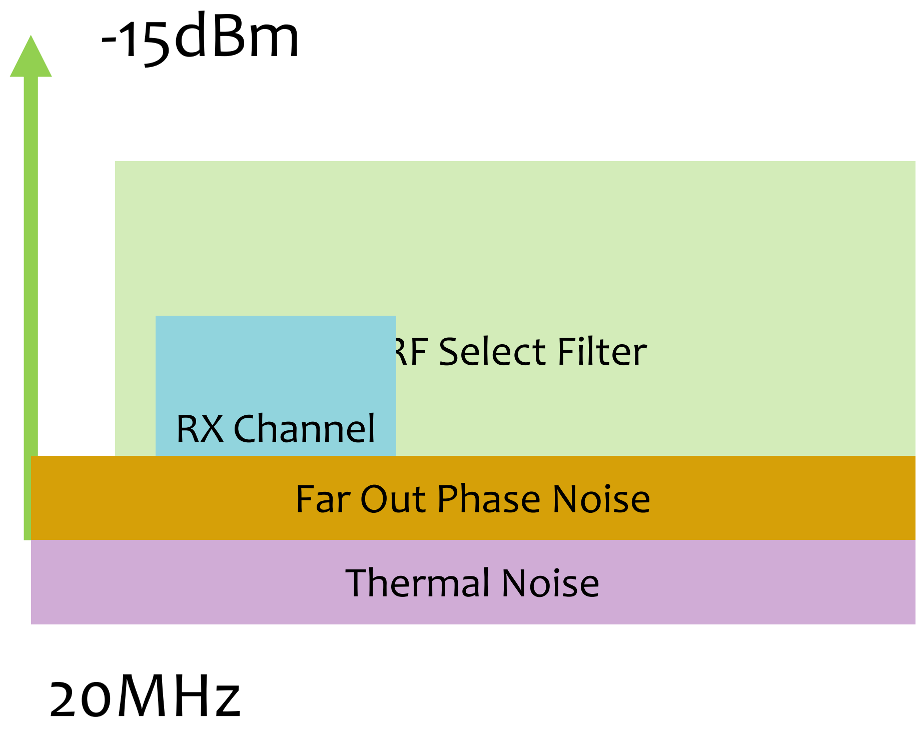
Example SAW Duplex Filter

- **Duplexer isolates TX and RX from one another, whilst sharing the same antenna.**
- **Low cost SAW Duplexer filters are commonly used in handsets and femto cell base stations.**
- **SAW filters are often essential for good performance radio.**
- **Expensive cavity filters used in high power transmitters.**



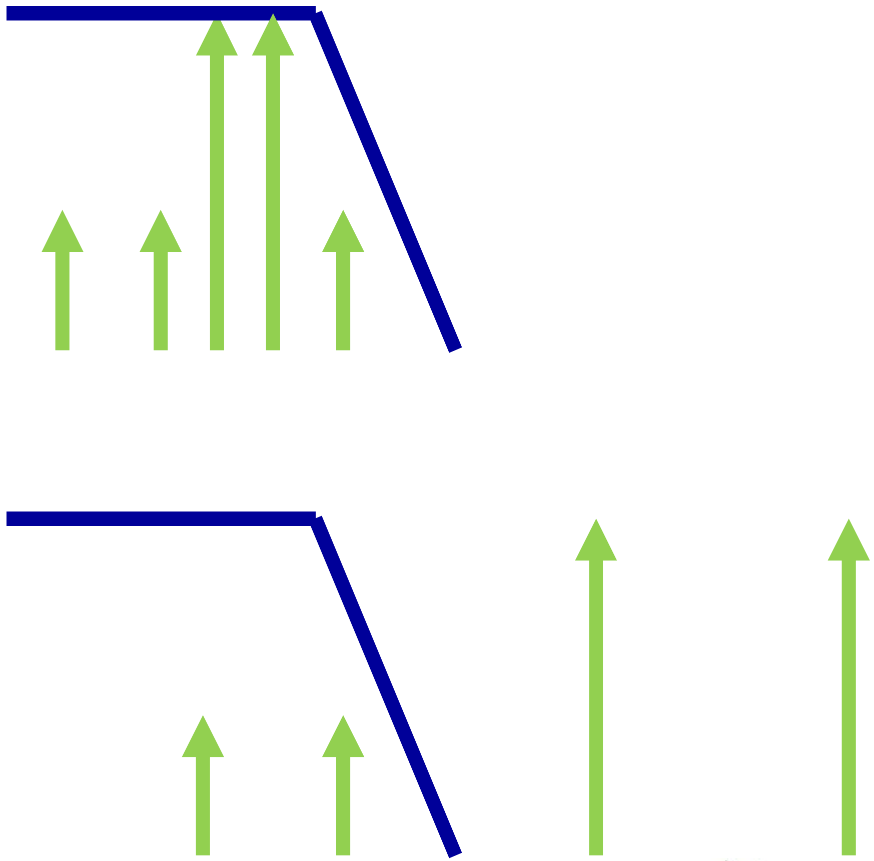
RX Phase Noise Problem

- **3G/4G Blocker Requirement**
- **-15dBm CW Blocker 20MHz from band edge of RF filter.**
- **RF SAW Filter provide partial filtering of CW Blocker 5-20dB and 2dB loss.**
- **P1dB of LNA >-25dBm**
- **Far out phase noise of synthesiser must be around -155dBc**
- **Phase Noise -20dBm-155dBc=-175dBm/Hz**
- **Thermal Noise -174dBm+2.5dB+2dB+0.5dB**
  - =-169dBm/Hz (NF=2.5dB)
- **Loose about <1dB sensitivity**



Rx Inband and Out of Band IIP3

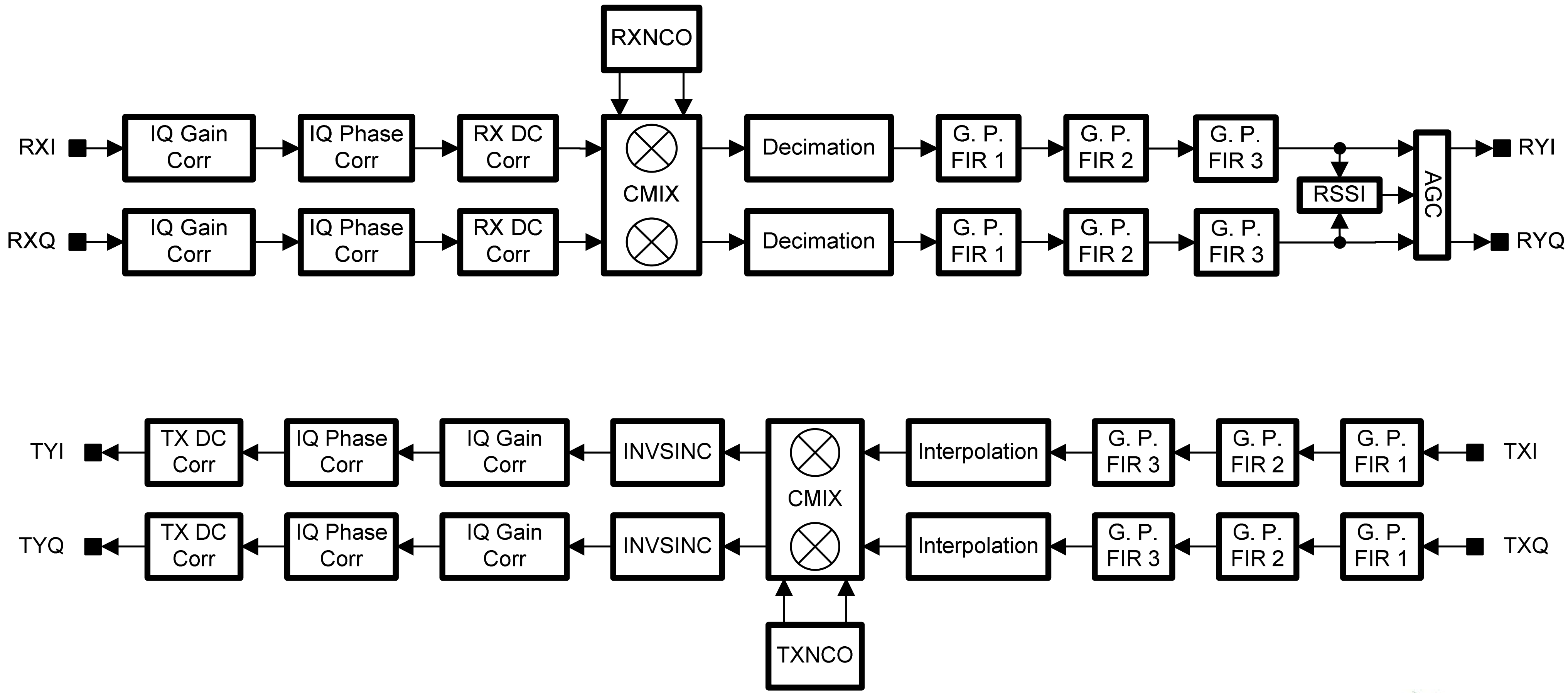
- **LMS7002M has very linear mixer and LNA.**
- **Inband IIP3/IIP2 limited by P1dB of system**
  - Gain sensitive
- **Out of band IIP3/IIP2 limited by P1dB of LNA and Mixer**
  - LNAL 915MHz LPF 600kHz
  - IIP3=+5.5dBm IIP2>48dBm
  - LNAH 1980MHz LPF 2.5MHz
  - IIP3=10.8dBm IIP3>40dBm



Lime microsystems

3. The Digital Half of the LMS7002M

LMS7002M FPRF Transceiver Signal Processing TSP

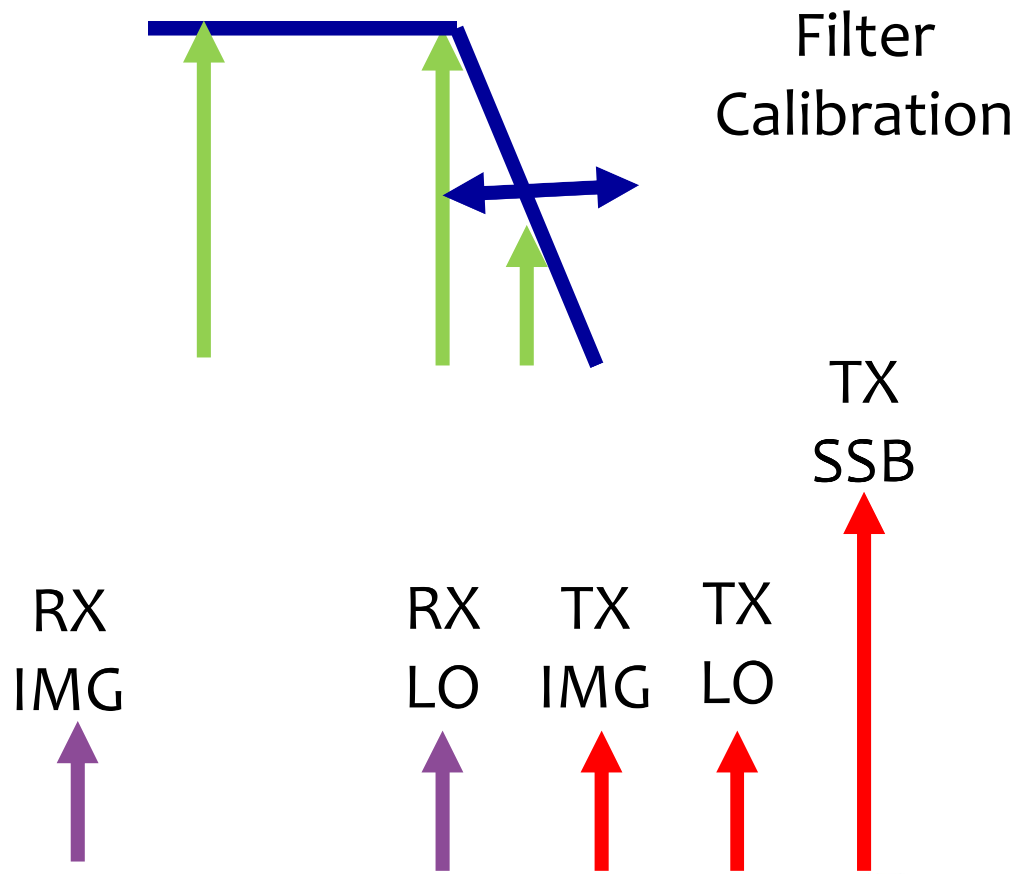


Digital Filtering

- **Inverse Sync (TX)**
  - Sample and Hold has a frequency peak as signal approaches half sample rate.
  - Inverse Sync corrects for this.
- **Interpolation (TX) and Decimation (RX)**
  - Want slowest possible data rate into the LimeSDR to minimise data processing
  - Want fastest sample rate for DAC/ADC
  - Interpolation=Upsampling+Filter
  - Upsampling [P1,P2,P3]-->[P1,0,P2,0,P3,0]
  - Decimation=Filter+Subsampling
  - On chip decimation and interpolation allow data rate conversion.
- **General Purpose FIR Filters**
  - Allows additional filtering
    - Upto 160 taps
  - Usually low pass
  - High pass and band pass are possible
  - Available taps depends on Decimation and Interpolation rates.
  - Filter coefficients can easily be designed in Octave or Matlab.

NCO, Complex Mixer, Test Signals and Calibration

- **Numerically Controlled Oscillator**
  - Programmable precision quadrature digital oscillator
  - Can be used as a test signal
- **Complex Mixer + NCO**
  - Can be used as low IF receiver
- **Filter bandwidth Calibration**
  - Baseband Loop back
- **Image Rejection Calibration**
  - RF Loop back
  - I Q gain and phase adjusted
- **TX/RX LO Leakage Cancellation**



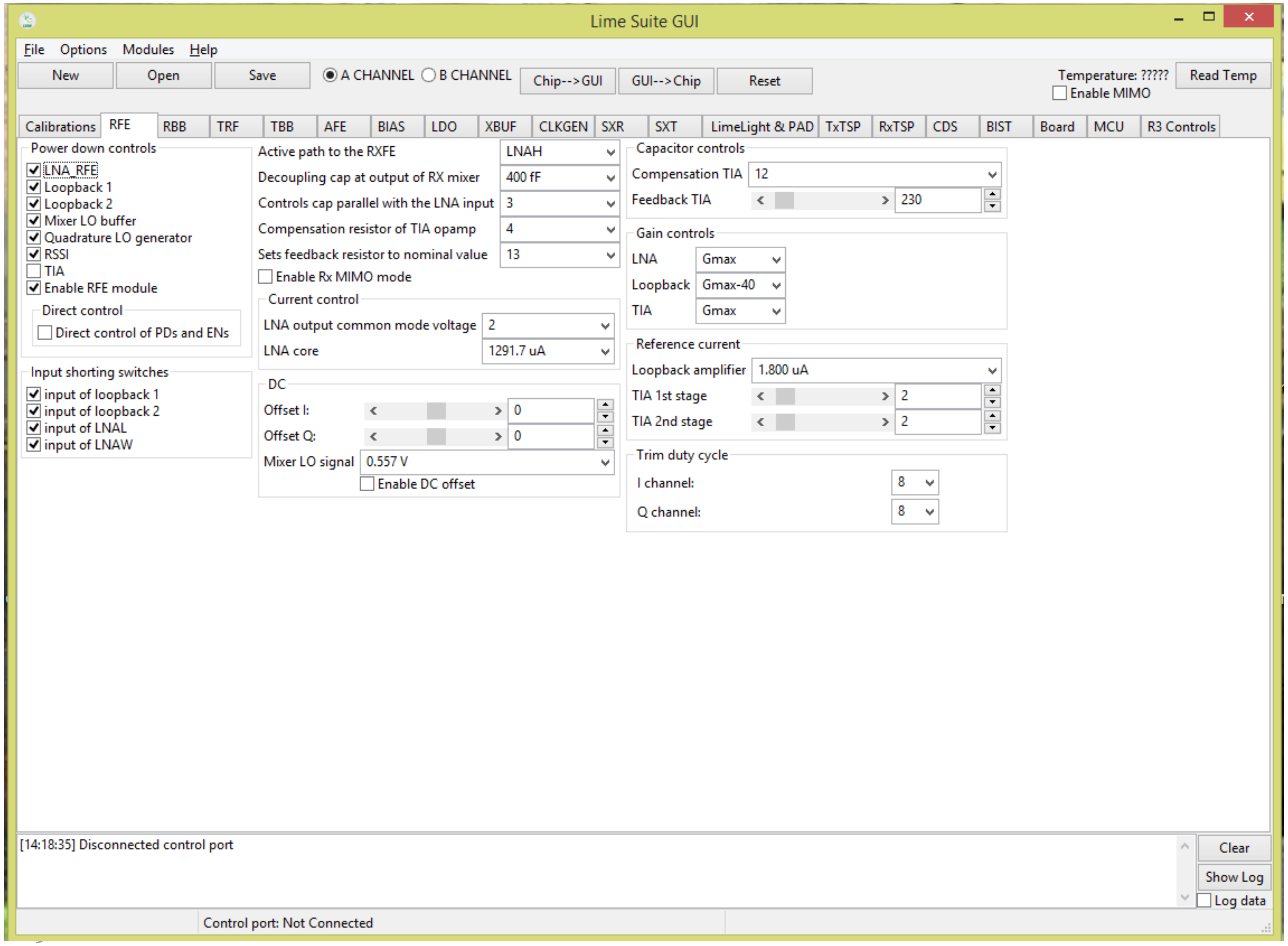
Other Digital Features

- **Digital AGC**
  - Intended for Repeater type applications.
- **Digital RSSI**
  - Intended for calibration and software controlled AGC.
- **DC Register load in Tx TSP**
- **8051 Based MCU**
  - Can execute calibration loops

4. The LimeSuiteGUI

LimeSuiteGUI

- **Access to ALL registers of LMS7002M**
- **Controls grouped into sections.**
  - MIMO Controls have A and B channel
- **We will use this software in our practical session.**

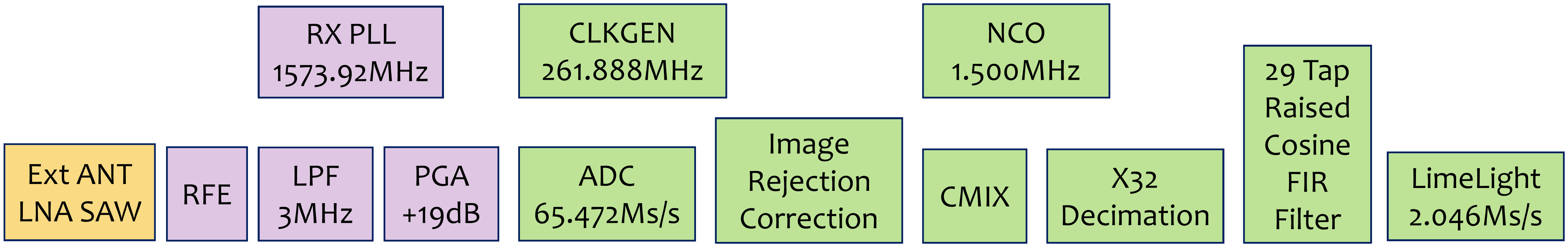


5. Using the LimeSDR Well

Tips on Using LimeSDR Well

- **Always start from a working .ini file.**
- **Try out settings using FFT Viewer and known waveforms.**
- **Make frequency plan of SDR clocks**
  - Signal Bandwidth
  - Adjacent Channel Issues
  - ADC/DAC Rates → CLKGEN
  - Interface Rate→Dec/Int Factors
- **Set up for best dynamic range**
  - Use sufficient PGA gain for ADC to just see noise floor.
  - Reduce LNA gain until signal to noise just begins to degrade.
- **RF Match TX and RX for best output power and sensitivity.**
  - Best LNA NF match usually a little away from best S11 match.
- **Typical settings for 900MHz 20MHz BW**
  - LNA = MaxGain-9
  - TIA = MaxGain
  - PGA = 0dB
  - CLKGEN ~ 250MHz

LimeSDR GPS Receiver: using the LMS7002M Rx TSP



- **SAW filter in external ANT/LNA/SAW unit.**
- **LNA Gain at maximum, but can be reduced to improve interference tolerance.**
- **Analogue IF Filter programmed to 3MHz.**
  - 3rd order filter to minimise analogue filter noise.
- **Digital clock generator programmed to 261.888MHz**
- **ADC Clock programmed to 65.472Ms/s**
  - Oversampling increases number of effective bits by 4.5 bits.

- **Image rejection correction gives 50dB rejection of any image band noise and interference.**
- **Use Low IF to avoid calibration drift.**
- **Low IF to Zero IF with on chip NCO running at 1.5MHz into complex mixer. RX PLL=1573.92MHz.**
- **Use x32 decimation to reduce output data rate to 2.046Ms/s.**
- **Programme FIR filter to be 29 tap Raised Cosine to limit noise bandwidth**

6. The FPGA

Modifying the LimeSDR FPGA

- **FPGA**
  - provides interface between USB controller and LMS7002M Radio.
  - provides RAM waveform playback.
- **Can I alter the FPGA - Yes**
- **Resources**
  - X116 18 bit multipliers,
  - x4 PLLs, 39k gates 1134kb RAM
- **Altera design tools**
  - Free for Cyclone 4E
  - Download from Altera
- **Code for the LimeSDR FPGA**
  - open source.
  - Download from Myriad RF
- **Design Environment**
  - Quartus Prime 16.1 Lite
- **Code modules**
  - VHDL, Verilog, Schematic or IP Blocks
- **Design test benches for code.**
  - VHDL or Verilog
- **Logic Synthesis**
- **Simulate**
  - Model Sim
- **Place and route**
- **Timing Analysis**
- **Download**