



Not your grandfather's ADC: RF sampling ADCs offer advantages in systems design

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Introduction

The data converter has acted as the bridge between the analog (real) world and the digital world for a few decades now. Starting with discrete elements that took up multiple rack spaces and burnt lots of power (like the DATRAC 11-bit 50-kSPS Vacuum Tube ADC at 500W!), they have morphed into highly integrated monolithic silicon ICs [1]. Ever since the first commercial data converters were made, the insatiable need for faster and faster data rates meant that the data converter development had to keep pace. The latest avatar of the ADC is the RF sampling ADC with sampling speeds in the GHz realm.

Advances in architecture development coupled with the rapid increase in semiconductor technology enabled the implementation of Analog/Digital Converters (ADC) in monolithic silicon form. Since the 1990s, CMOS technology has been able to keep pace with the quality of discrete analog circuits that make up the building blocks of a data converter. Integrating the building blocks into a monolithic piece of silicon enables more power and space efficient designs. Moore's Law now not only applied to digital IC designs, but also to analog designs [2]. One only need to observe the past two decades (mid '90s - present) to see this rapid growth in technology. This growth in technology has spurred the need for faster and faster data conversion, leading to development of data converters with higher and higher bandwidths.

Over the years, the silicon technology has advanced enough such that it is now possible to economically design A/D Converters (ADCs) with a lot more powerful digital processing. Earlier generation ADC designs used very little digital circuitry, primarily used for error correction and digital drivers. The new family of GSPS (Giga Sample Per Second) converters (also known as RF Sampling ADCs) are enabled using sophisticated 65nm CMOS technology, and can pack a lot more digital processing power to enhance the ADC's performance. This enables the data converter to morph from an "A-d-C" (Big A, small D converter) in the mid 90's and the 2000s to an "a-D-C" (small A, big D converter). This does not mean that the analog circuitry and its performance has shrunk, but the amount of digital circuitry has increased drastically to complement the analog performance.

These added features allow the ADC to do a lot of digital processing in the ADC silicon at speed and

take up some of the digital processing load from the FPGA. This opens a whole lot of other possibilities to the systems designer. Now, using one of these new state-of-the-art GSPS ADCs, a systems designer only need to design one hardware for a multitude of platforms, and effectively use software to reconfigure the SAME hardware to suit the new application.

Enhanced Digital Processing at speed

The combination of ever shrinking geometries in the CMOS processes combined with advanced design architectures meant that for the first time, ADCs could use digital processing techniques to improve their performance. The breakthrough was achieved in the early 1990s and ADC designers haven't looked back since [1]. As the silicon processes improved (from 0.5 μ m, 0.35 μ m, 0.18 μ m and 65nm) the speed of conversion improved. But as geometries shrunk, the transistors while getting faster (leading to higher bandwidths), offered slightly inferior characteristics in terms of performance for analog designs, like Gm (transconductance). This was compensated by adding more and more correction logic. However, silicon was still expensive enough that the amount of digital circuitry inside the ADC was still comparatively modest. The block diagram of one such example is shown below in Figure 1.



Figure 1 : Early generation monolithic ADC with minimal digital error correction logic

With the advancement in silicon technology to deep sub-micron geometries like 65nm, the economics of scale have made it possible to add a lot of digital processing in the data converter in addition to running the core much faster (1GSPS or higher) [2]. This is a breakthrough advancement on second inspection. Usual digital signal processing is either handled by ASICs or FPGAs depending on the system performance and cost requirements. ASICs being application specific require large sums of money for development.

Hence, designers usually run the ASIC designs for a long time to extend the return on investment in the ASIC development. FPGAs are a cheaper alternative to ASICs and do not require the huge development budgets. However, since FPGAs try to be everything for everybody, their signal processing capability is hampered by speed and power efficiency. This is understandable since they offer a level of flexibility and re-configurability that the ASICs just cannot offer.

Figure 2 shows a block diagram of a RF Sampling ADC (also known as a GSPS ADC) with configurable digital processing blocks.



Figure 2 : GSPS ADC with digital processing blocks

The new generation of GSPS ADCs will revolutionize radio designs because they bring a lot of flexibility to the design table, some of which are discussed below.

Digital Processing at Speed

Digital Processing at Speed

Earlier generation of radios would use a mixture of analog mixers and cascaded Digital Down Converters (DDCs) in order to bring the signal down to baseband for processing. This involved a lot of hardware (analog mixing) and power (in analog and in DDCs in the ASIC/FPGA). With the new generation of RF Sampling ADCs the DDCs can be run at speed inside the ADC using full-custom digital logic. This means that the processing is much more power efficient.

I/O Flexibility via JESD204B

The new generation of RF Sampling ADCs not only have GSPS sampling capability, but also have eschewed the dated LVDS outputs for high-speed serial interface. The new JEDEC JESD204B specification allows the digital output data to be transmitted via CML (Current Mode Logic) at high lane rates of up to 12.5Gbps/lane. This offers a high level of I/O flexibility. For example, the ADC can function in full bandwidth mode and transmit the digital data on multiple lanes, or use one of the available DDCs and transmit the decimated and processed data on one lane as long as the output lane rate stays below 12.5Gbps/lane.

Scalable Hardware Design

The use of the DDCs offers a new level of flexibility in the hardware design side. The systems designer can now “freeze” the hardware design of the ADC and FPGA, and with minimal changes, reconfigure the system for a different bandwidth as long as the ADC can support it. For example, a radio may be designed as a full bandwidth ADC (RF Sampling ADC), or as an IF Sampling ADC (Intermediate Frequency band ADC) using the available DDC. The only change in the system would be on the RF side where some minimal additional mixing may be needed for the IF ADC. The majority of the change would be in software required to configure the ADC for the new bandwidth. However, the ADC + FPGA hardware design can pretty much stay the same. This offers a “reference” hardware design that can address many platforms and their requirements with software being the only variable.

Other extra features

The high level of integration that the deep sub-micron CMOS process allows has ushered in an era

where more and more features are being built into the ADC. Some of these features include fast detect CMOS outputs that allow for efficient AGC (Automatic Gain Control), Signal Monitoring (like a Peak Detector), etc. All of these features aid in the systems design by reducing external components and reducing design time

Communications Receiver Design made flexible

A very common use case for the ADC is in a communications receiver system design. There have been many publications on software defined radio (SDR) and a communications receiver using an ADC which is outside the scope of this discussion. A block diagram representation of an older generation radio receiver is shown in Figure 3 [1].



Figure 3 : Wideband Digital Receiver for Cellular Radio

Normal specifications for GSM radio receiver require a Noise Spectral Density (NSD) of at least about -153dBFS/Hz or better in the ADC. As is well known, the NSD is connected to the SNR of the ADC by the following equation [3]:



Where,

SNR is in dBFS

f_s = ADC sample rate

Conventional software radio design **Conventional software radio design**

In a wideband radio application, it is not uncommon to see bands of up to 50MHz being sampled and converted at once. In order to properly digitize a 50MHz band, an ADC would be required that should sample at least five times the bandwidth, or at ~250MHz. Plugging in the numbers in to the equation above, the required SNR for such an ADC to hit the NSD specification of -153dBFS/Hz would be around 72dBFS.

Figure 4 below shows the frequency plan employed to effectively sample the 50MHz band using the 250MSPS ADC. The figure also shows the location of the second and third harmonic bands.



Figure 4 : Frequency plan for the 50MHz wideband radio using a 250MSPS ADC

Any sampled frequency by the ADC will fall in the first Nyquist (DC - 125MHz) band of the ADC. This phenomenon is called aliasing, and hence the frequencies including the band of interest, its second and third harmonics effectively “fold” back or alias into the first Nyquist band. This is shown in Figure 5 below.



Figure 5 : Useable band shown in the first Nyquist with second and third harmonics

In addition to the NSD specification, the cellular communication standards like GSM, LTE, LTE-A etc. have other stringent requirements on SFDR or Spurious Free Dynamic Range. This specification puts a lot of pressure on a front end design that is capable of attenuating the unwanted signals when sampling the signals in the band of interest.

Keeping in mind the SFDR specification, the Anti-Aliasing Filter requirements for the front end design for the conventional radio become very hard to hit. The best Anti-Aliasing Filter (AAF) solution that will satisfy SFDR specification would be to implement a band pass filter. Usually these band pass filters are of the order of 5 or higher. A suitable ADC that can satisfy the SNR (or NSD) and SFDR requirements of such an application would be the AD9467, 16-bit 250MSPS Analog-Digital Converter [4]. The front end design for the cellular radio application using the AD9467 would like the one shown in Figure 6.



Figure 6 : Front end design showing the amplifier, the anti-aliasing filter and ADC at 250MSPS

The frequency response of the AAF that will satisfy the SFDR requirements is shown in Figure 7. The implementation of this system is not impossible, but poses a lot of design challenges. The band pass filter is one of the hardest filters to implement as it involves a lot of components. Component

selection is key in this case as any mismatch between the components is going to result in unwanted spurs (SFDR) in the ADC output. In addition to the complexity, any impedance mismatch is going to affect the gain flatness of the filter. A considerable design effort is required in order to optimize this filter design to meet the pass-band flatness and stop-band rejection requirements.



Figure 7 : Band pass response of the front end shown in Figure 6

Though the implementation of the front end for such a radio design can be complicated, it does work as shown by the SNR/SFDR performance across frequency plot shown in Figure 8. An FFT at 205MHz is shown in Figure 9. However, the system implementation is made complicated by:

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- The filter design.
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- The FPGA having to dedicate I/O ports to capture the LVDS data (16 pairs) which makes PCB design complicated.
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- Having to set aside additional processing power in the FPGA to do the digital signal processing.



Figure 8 : SNR/SFDR vs. frequency for the 16-bit 250MSPS ADC design shown in Figure 6



Figure 9 : FFT at 205MHz for the 16-bit 250MSPS ADC design shown in Figure 6

RF Sampling ADCs simplify (and speed up) design
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The RF Sampling ADC approach uses the technique of oversampling and then decimating the data to improve the dynamic range [5]. The speed advantage offered by the deep sub-micron CMOS technology coupled with the dense digital integration capabilities have spurred the new era of RF sampling ADCs that can do a lot more heavy lifting than just plain analog-digital conversion. These ADCs have a lot more digital circuitry that enables the processing of signals at speed.

To a systems designer, this means ease of implementation and other flexibilities that has hitherto been part of the ASIC/FPGA domain. The same radio design example above can be implemented using an RF Sampling ADC. The AD9680 (ADI's 14-bit, 1GSPS JESD204B, Dual A/DI Converter) is one of a new breed of RF Sampling ADCs that also have additional digital processing power [6] (See AD9860 at IMS2015 at ADI's booth# 3036). The NSD for this ADC at full sample rate (1GSPS) is ~67dBFS [3]. This SNR is not of a concern yet as will be made evident later on. The band of interest is the same as before, but the frequency plan on the RF Sampling ADC Nyquist zones is much simpler as shown in Figure 10 below. This is because this ADC is sampling at 4 times (1GHz) compared to the example described earlier (250MHz).



Figure 10 : Frequency plan for the 50MHz wideband radio using a 1GSPS ADC

It is evident from the frequency plan that this is a much simpler plan to implement than the one shown in Figure 4. The AAF requirements are also relaxed as shown in Figure 11. In this approach the idea is to use a simple analog front end design and leave the digital processing blocks inside the RF Sampling ADC to do the heavy signal processing.



Figure 11 : AAF implantation for the 1GSPS ADC

The benefit of oversampling basically “spreads” out the frequency plan across the Nyquist zone which is 4 times bigger than the 250MSPS Nyquist. This tremendously relaxes the filtering requirements and a simple 3rd order low-pass filter will suffice as opposed to the band pass filter used in the 250MSPS ADC implementation. The simplified AAF implementation using an RF Sampling ADC is shown in Figure 12.



Figure 12 : Front end design showing the amplifier, the anti-aliasing filter and ADC at 1GSPS

Figure 13 below shows the low-pass filter response. The band pass response is also shown as a comparison. The low-pass filter achieves a better pass-band flatness and is easier to manage in terms of component mismatch. It is also easier to implement in terms of matching impedances. Moreover, the cost of the system is reduced because of the lower component count. This simplicity in the front-end design could lead to reduced design times.



Figure 13 : AAF comparisons for 250MSPS ADC and 1GSPS ADC

The fact that the modern RF Sampling ADCs pack a lot more digital processing capabilities means that the digital processing can be done at speed inside the ADC itself. As discussed in this article before, this leads to a power efficient and I/O efficient design. Now, the systems designer can use the unused JESD204B transceivers of his/her FPGA to service data coming from other RF Sampling ADCs which have already processed the data (A-D conversion, filtering and decimation). This makes it possible to use the FPGA resources efficiently, while increasing the number of channels in the radio design.

ADC as a Digital Mixer

Using the DDCs, the ADC can be used as a “digital mixer” to tune to any IF the design may require. In this example, the same frequency plan as discussed above is used. So a Decimate-by-4 option with Real mixing is used to demonstrate the ADCs performance. This is shown in Figure 14.



Figure 14 : RF sampling at 1GSPS with DDC set to Decimate - by - 4

In normal (or full bandwidth) mode, the AD9680's SNR is about 66-67dBFS. But when the DDCs are in operation and the decimation ratio is set to 4, there is an additional 6dB of processing gain that is attained [3]. This ensures that the dynamic range performance is maintained. Since the RF Sampling ADC samples at 4x the original sample rate, the harmonics are “spread” out as shown in Figure 10. The DDCs in the RF Sampling ADC ensure that the decimation filter “digitally” attenuates the unwanted signals. However, the harmonics (higher order or other) that fall in the “band of interest” will still show since the DDCs let them through.

This could be caused by the amplifier artifacts or the low pass filter not having enough attenuation. The low pass filter can be redesigned as per system requirements to meet the “other spur” spurious performance. Figure 15 below shows the SNR/SFDR vs. input frequency for the 1GSPS ADC. As is clear from the data, the use of DDCs improve SNR (by 6dB due to the processing gain) and SFDR. When running in full bandwidth mode, the SFDR is usually limited by the second or third harmonic, whereas in the DDC mode (with decimate-by-4), it is the “worst other harmonic”.

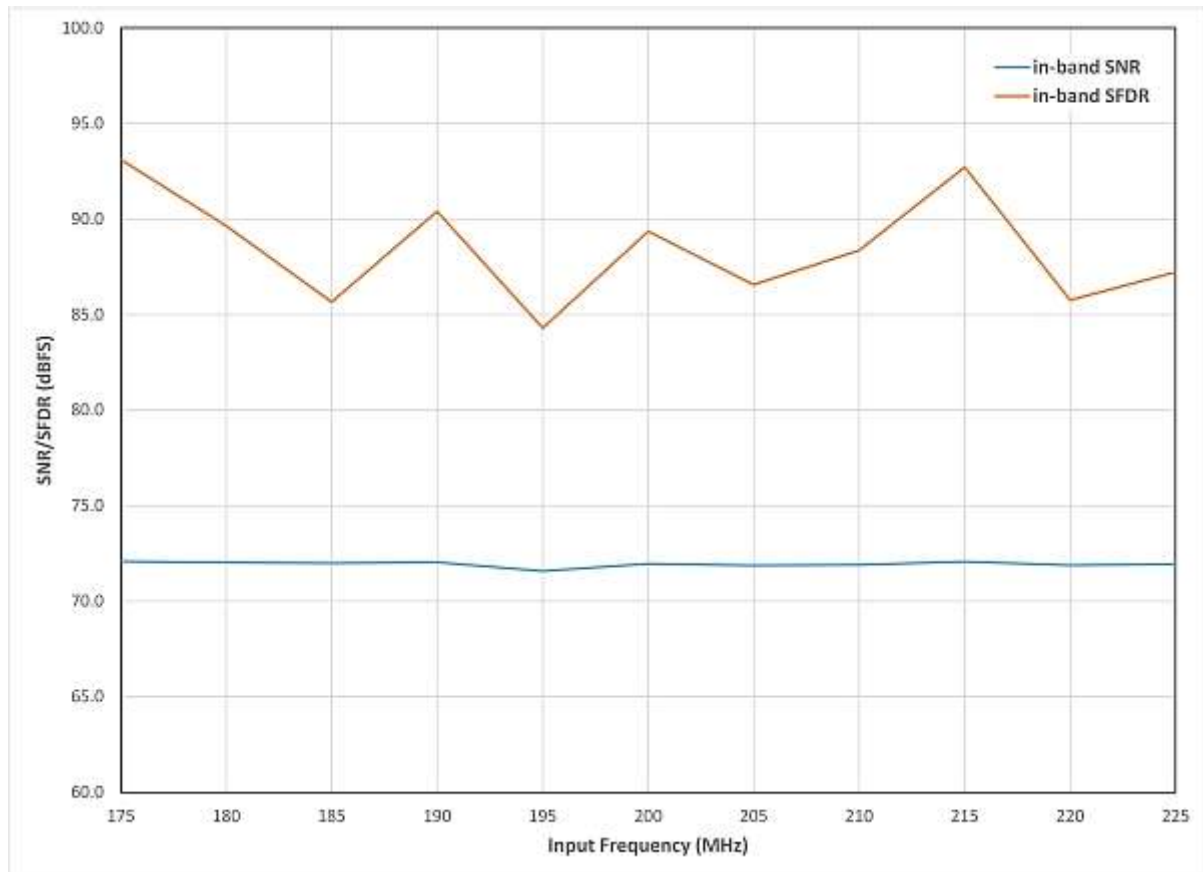


Figure 15 : SNR/SFDR vs. frequency for the 14-bit 1GSPS ADC design shown in Figure 12

An FFT of the decimated output is shown in Figure 16. When using the DDCs, care must be taken to make sure that the “band of interest” is processed correctly. In this case, the NCO was tuned to 200MHz so that the “band of interest” falls in the center of the decimated Nyquist. The DDCs offer the convenience of eliminating the unwanted frequencies in the spectrum. This results in a lower processing overhead for the FPGAs. For comparison, the FFT for the AD9680 under normal (full bandwidth) operation is shown in Figure 17.



Figure 16 : 205MHz FFT on the 1GSPS ADC with decimation-by-4; NCO tuned to 200MHz



Figure 17 : 205MHz FFT on the 1GSPS ADC in Full bandwidth mode

The figures show that the DDCs in addition to improving “in-band” noise performance, also provides a clean spectrum devoid of unwanted harmonics. Since the DDCs filter and decimate the data (to 250MSPS), they also reduce the output lane rate, which results in flexible options for the JESD204B serial interface. This lets the systems designer choose between a high lane rate (more expensive), low I/O count FPGA or a low lane rate (less expensive) high I/O count FPGA.

Conclusion

To sum up, RF Sampling ADCs offer a unique advantage in systems design that would not have been possible a few years ago. The industry is looking to accelerate the design and implementation of infrastructure to cope with the need for higher bandwidth. Design times and budgets are shrinking and a need for a scalable, reconfigurable architecture that is more software driven lends itself to the new norm. The increased need for bandwidth is also coupled with the need for higher capacity. This puts additional strain on the FPGA I/Os, which the RF Sampling ADC can counter by the use of its internal DDCs.

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