Open Source FPGA toolchains

PRELIMINARY REPORT

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Contents

0.1 Platforms Tested

For the purpose of this evaluation, the platforms selected should have at least 7K LUTs and having active or under development open-source tool-chains or, as a last resort, free toolchains.

1. Lattice ICE40
   Devboard: TinyFPGA BX
   FPGA: ICE40LP8K

2. Lattice ECP5
   Devboard: ECP5 Evaluation Board
   FPGA: LFE5UM5G-85F-8BG381

3. Xilinx Artix-7
   Devboard: Digilent Arty A7-100T Development Board
   FPGA: XC7A100T-1CSG324C

4. Intel Cyclone-V
   Devboard: DE0-CV
   FPGA: Cyclone V 5CEBA4F23C7N

0.2 Toolchains

0.2.1 IceStorm (iCE40)

IceStorm is used for iCE40 bitstream creation. It relies on yosys for synthesis and NextPNR for place and route.

Supports all package variants of LP1K, LP4K, LP8K and HX1K, HX4K, HX8K, LP384 and UltraPlus devices.

Does not support iCE40 LM, Ultra and UltraLite

0.2.2 Trellis (ECP5)

Project Trellis enables a fully open-source flow for ECP5 FPGAs using Yosys for Verilog synthesis and nextpnr for place and route. Project Trellis itself provides the device database and tools for bitstream creation.

The following features are currently working in the Yosys -> nextpnr -> Trellis flow.

- Logic slice functionality, including carries
- Distributed RAM inside logic slices
- All internal interconnect
- Basic IO, including tristate, using TRELLIS_IO primitives. LPF files and DDR inputs/outputs
- Block RAM, using either inference in Yosys or manual instantiation of the DP16KD primitive
- Multipliers using manual instantiation of the MULT18X18D primitive.
  Inference and more advanced DSP features are not yet supported.
- Global networks (automatically promoted and routed in nextpnr)
- PLLs
- Transcievers (DCUs)

0.2.3 NextPNR

NextPNR is a portable FPGA place and route tool that aims to be a vendor neutral, timing driven, FOSS FPGA place and route tool.

Currently NextPNR supports:

- Lattice iCE40 devices through project IceStorm
- Lattice ECP5 devices through project Trellis, currently experimental
- "generic" back-end for user-defined architectures, currently experimental
- Xilinx 7 Series could be supported in the future through project X-Ray

0.2.4 X-Ray (Xilinx 7)

Project X-Ray documents the Xilinx 7-Series FPGA architecture to enable development of open-source tools.

0.2.5 Symbiflow

Symbiflow aims to be an open source flow for generating bitstreams from Verilog.

Since it uses Yosis, icestorm, trellis, xray and nextpnr for each of the supported platforms, device support at the same level as the underlying projects.

0.2.6 IceStudio

IceStudio is a visual editor for open FPGA boards. Built on top of the Icestorm project using Apio.

It implements Graphic design -> Verilog, PCF -> Bistream -> FPGA

It supports the following devices:

- HX1K
- HX8K
- LP8K
- UP5K

It is the easiest to setup as it handles all the toolchain and device drivers downloads and it comes as an AppImage.

0.2.7 Intel Quartus Prime Lite Edition and ModelSim - Intel FPGA Starter Edition

This is the official software from Intel. The Lite edition comes with a free license and there is a Linux version.

0.2.8 Vivaldo

This is the official software from Xilinx. The HL WEBPack edition does not require a license and there is a Linux version.

0.2.9 CubicBoard

Cubicboard claims to be an open-source FPGA project for the Cyclone-V family.

They do provide Open Hardware under Apache 2.0 license although source files are for Protel/Altium EDA.

The provided software is a VirtualBox image of Ubuntu having Intel Quartus preinstalled.

0.3 Available features

Based on the current project progress, implemented features are shown in tables 1, 2 and 3

	IceStorm	**Trellis**	**X-Ray**
Logic	Yes	Yes	Yes
Block RAM	Yes	Yes	Partial

Table 1: Basic Tiles

	IceStorm	**Trellis**	**X-Ray**
DSP	Yes	Yes	No
Hard Blocks	Yes	Yes	No
Clock Tiles	Yes	Yes	No
I/O Tiles	Yes	Yes	Partial

Table 2: Advanced Tiles

	IceStorm	**Trellis**	**X-Ray**
Logic	Yes	Yes	Yes
Clock	Yes	Yes	No

Table 3: Routing

References

Repos

https://github.com/cliffordwolf/icestorm.git
https://github.com/YosysHQ/nextpnr
https://github.com/SymbiFlow/prjtrellis
https://github.com/SymbiFlow/prjxray
https://github.com/YosysHQ/yosys
https://github.com/FPGAwars/icestudio
https://github.com/FPGAwars/apio