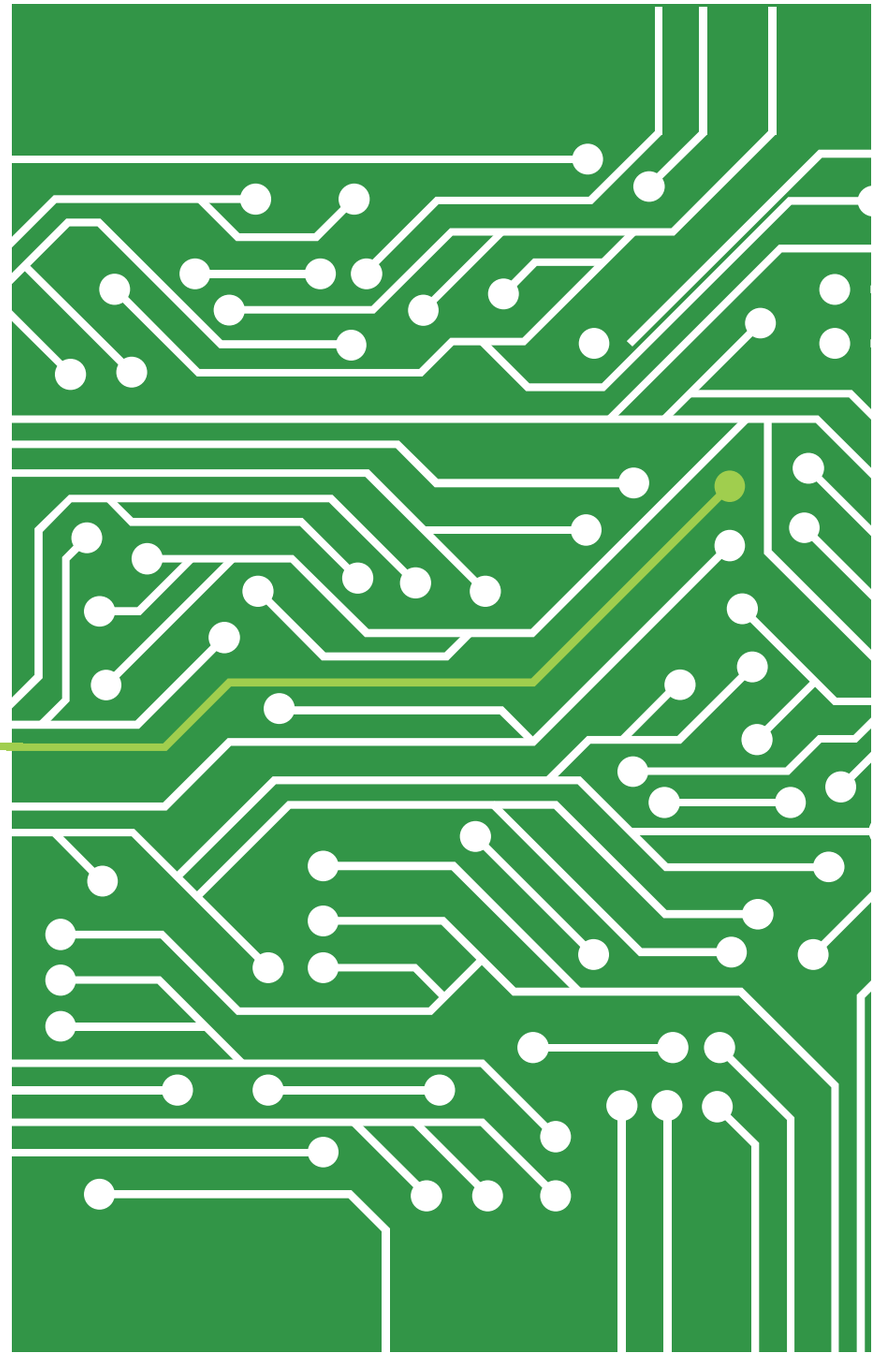
Lime microsystems

Vodafone CrowdCell Course:

LMS7002M Deep Dive

Lime Microsystems| FPRF company

Guildford, Surrey, United Kingdom



LMS7002M FPRF Transceiver Block Diagram

High level of integration, including dual 12-bit ADC and DAC

Integrated 8051 MCU

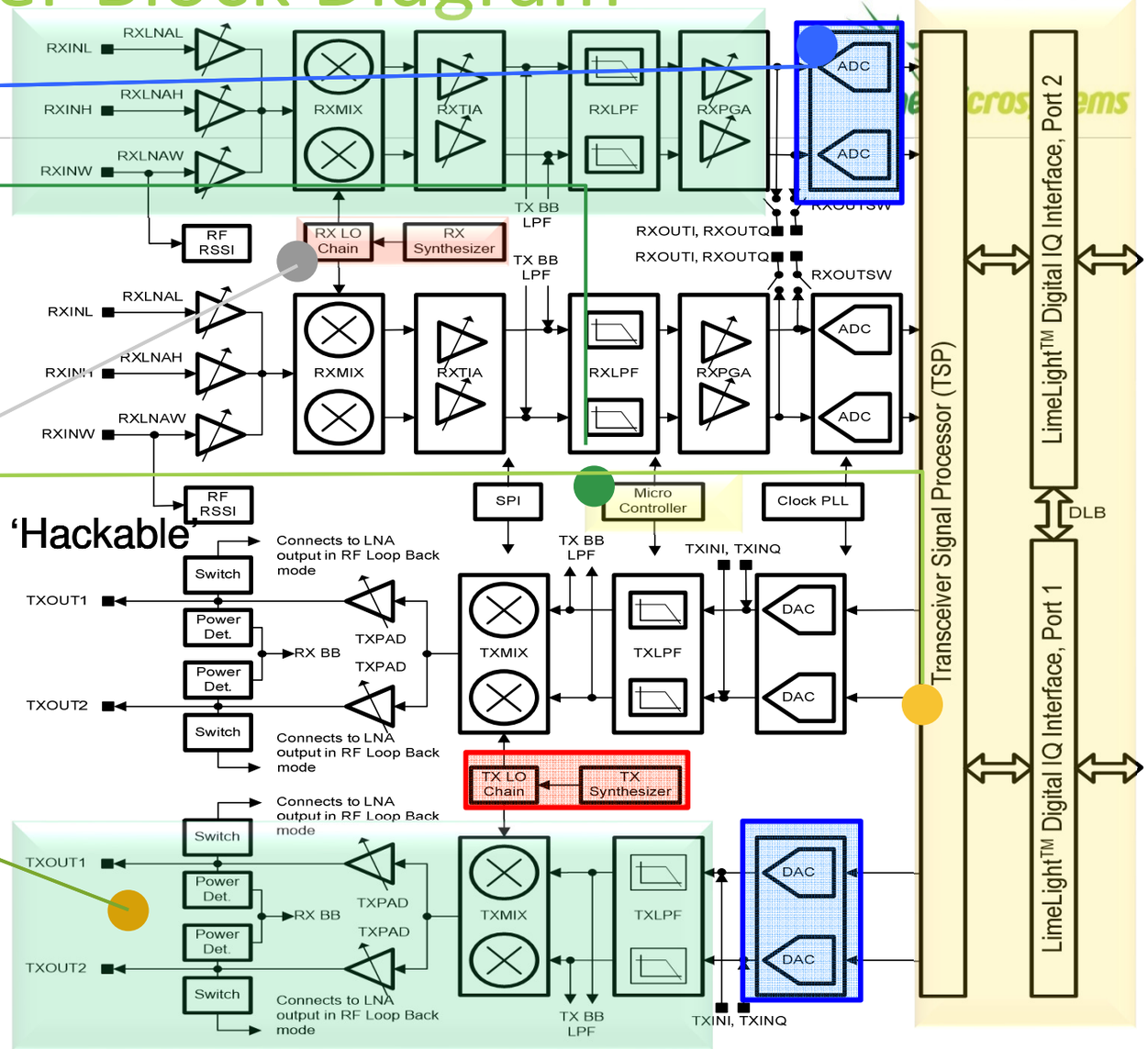
Transceiver Signal Processor block and LimeLight interface

Frequency

100KHz – 3.8GHz

Field Programmable RF

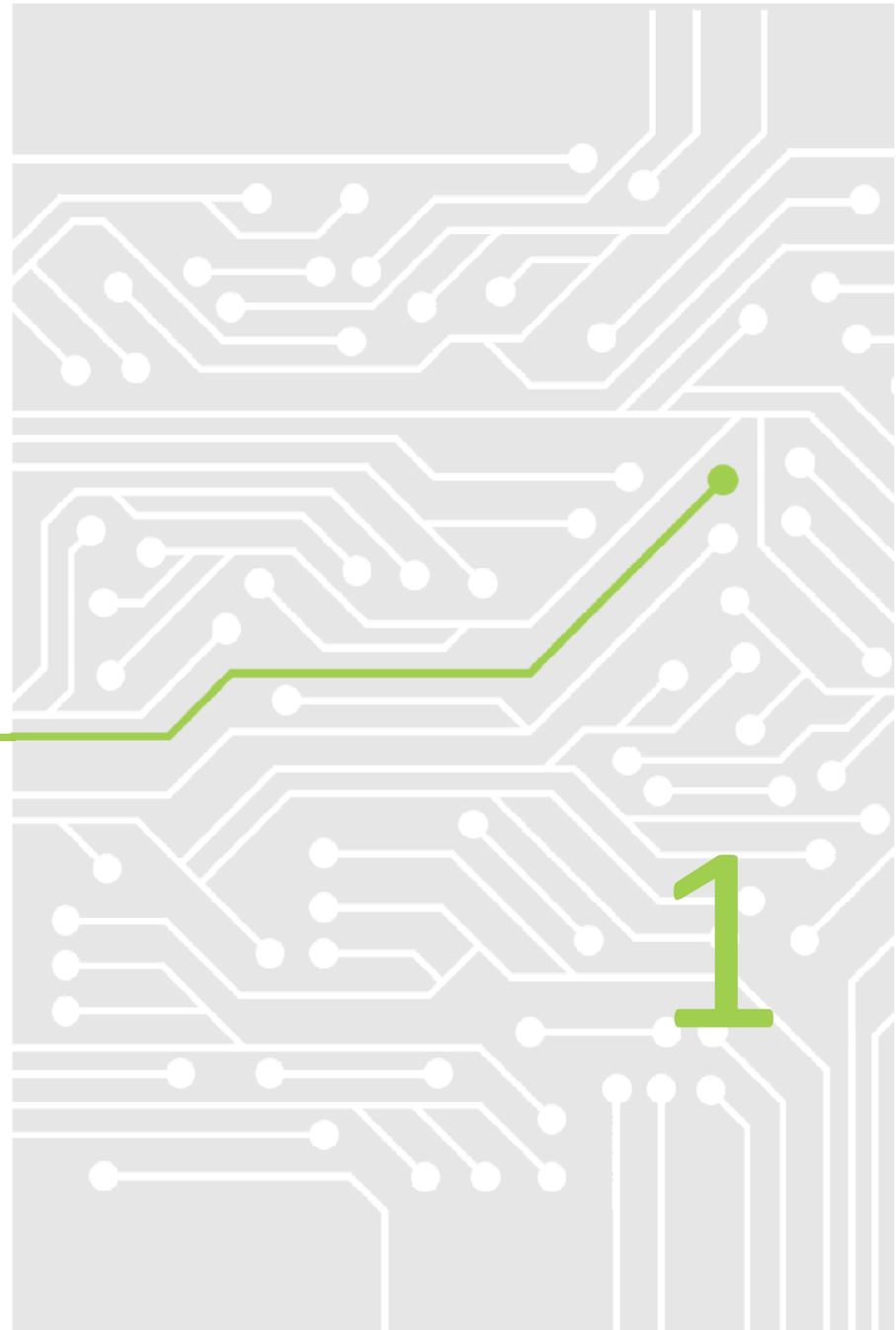
Highly configurable RF gain and IF filter with numerous bypass options



Introduction

1. **The Basic Vector Modulator**
2. **RF Quadrature Synthesiser**
3. **Digital Vector Transmitter (Analogue Parts)**
4. **Digital Vector Receiver (Analogue Parts)**
5. **Digital Baseband**
6. **LimeSuite**
7. **FPGA**
8. **Using the SDR Well**

The Vector Modulator



Simplified Vector (Homodyne) Transmitter

Homodyne 1930s

- Commonly called Zero IF
- Similar to Hartley SSB Modulator

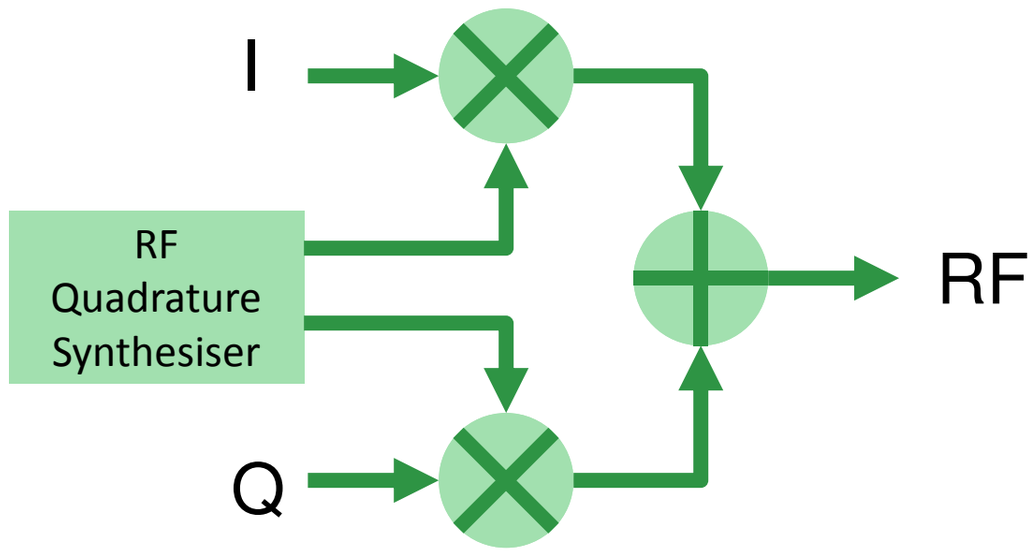
Analogue I,Q input signal

- describes a vector of amplitude and phase described by Cartesian co-ordinates {I,Q}
- Usually generated by software.

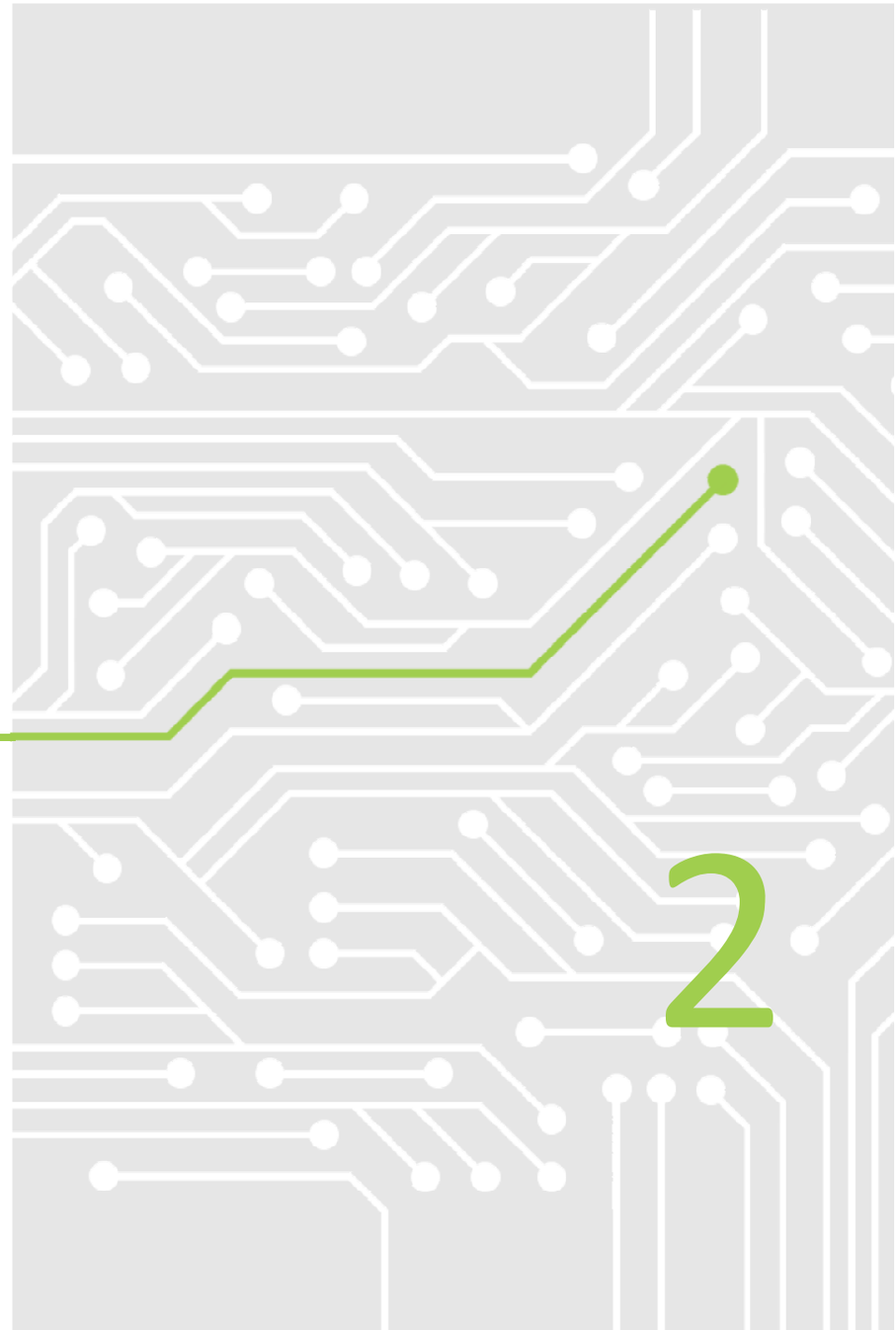
Frequency Mixers

- Converts I,Q into RF signal

For digital modulation I and Q vary with time.



RF Quadrature Synthesiser

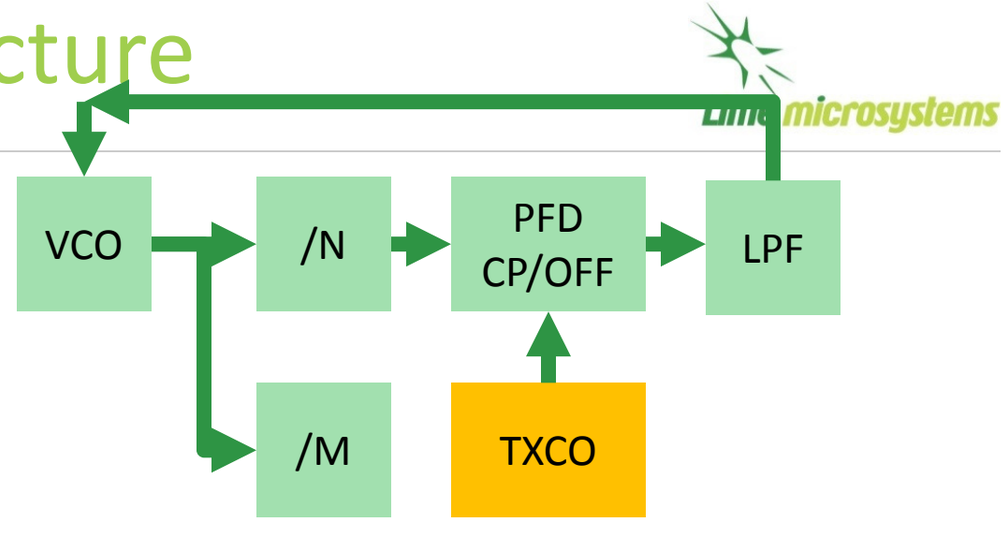


LMS7002M RF Synthesisers

LMS7002M – Three synthesisers

- SXT – Generates arbitrary RF frequency for Transmitter
  - Resolution approx. 16Hz
- SXR – Generates arbitrary RF frequency for Receiver
  - For FDD systems, Tx and Rx frequencies are usually offset by say 50MHz.
- CLKGEN – Generates timings
  - DAC
  - ADC
  - Baseband
  - LimeLight interface
- Special TDD mode where SXT drives both Transmitter and Receiver.

Lime RF Synthesiser Structure



30.72MHz TXCO (Note boundary spurs)

Typically -90dBc Phase Noise Plateau

- -100dBc with very low noise LDOs and very low phase noise TXCO

Integrated Phase Noise (LimeSDR)

- 0.14deg 100MHz
- 0.17deg 215MHz (1024 QAM)
- 0.31deg 500MHz
- 0.46deg 850MHz (256 QAM)
- 0.98deg 2145MHz (64 QAM)

Far out phase noise

- Typically -158dBc at 50MHz Offset

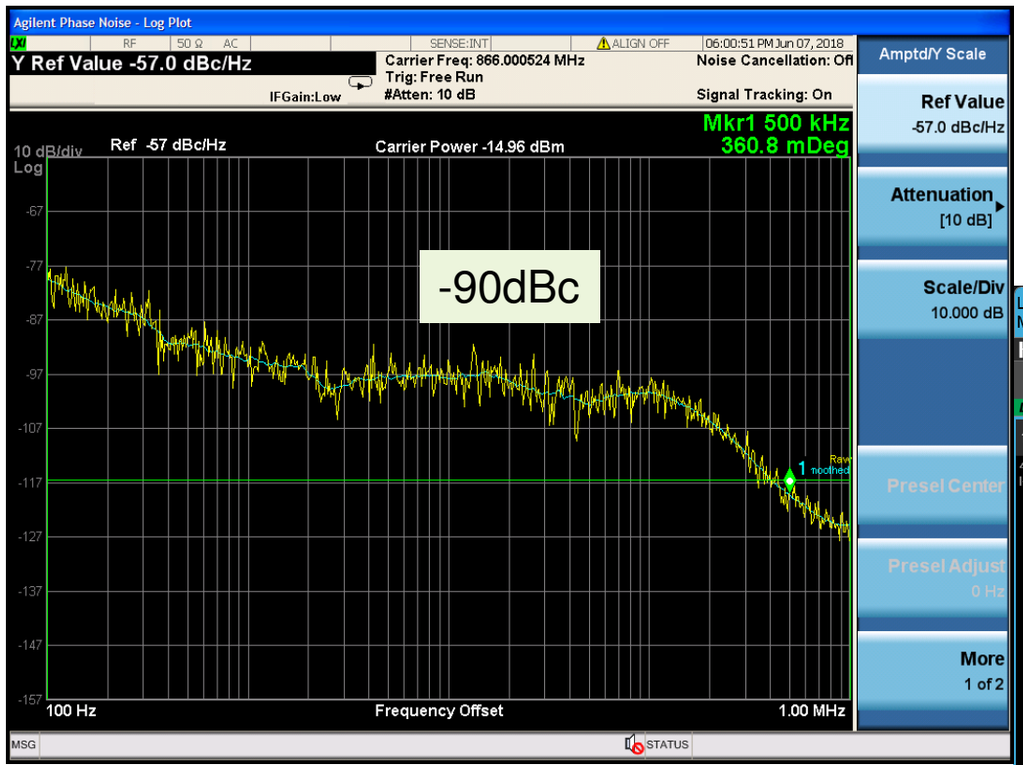
Delta Sigma Fractional N Type Synthesiser

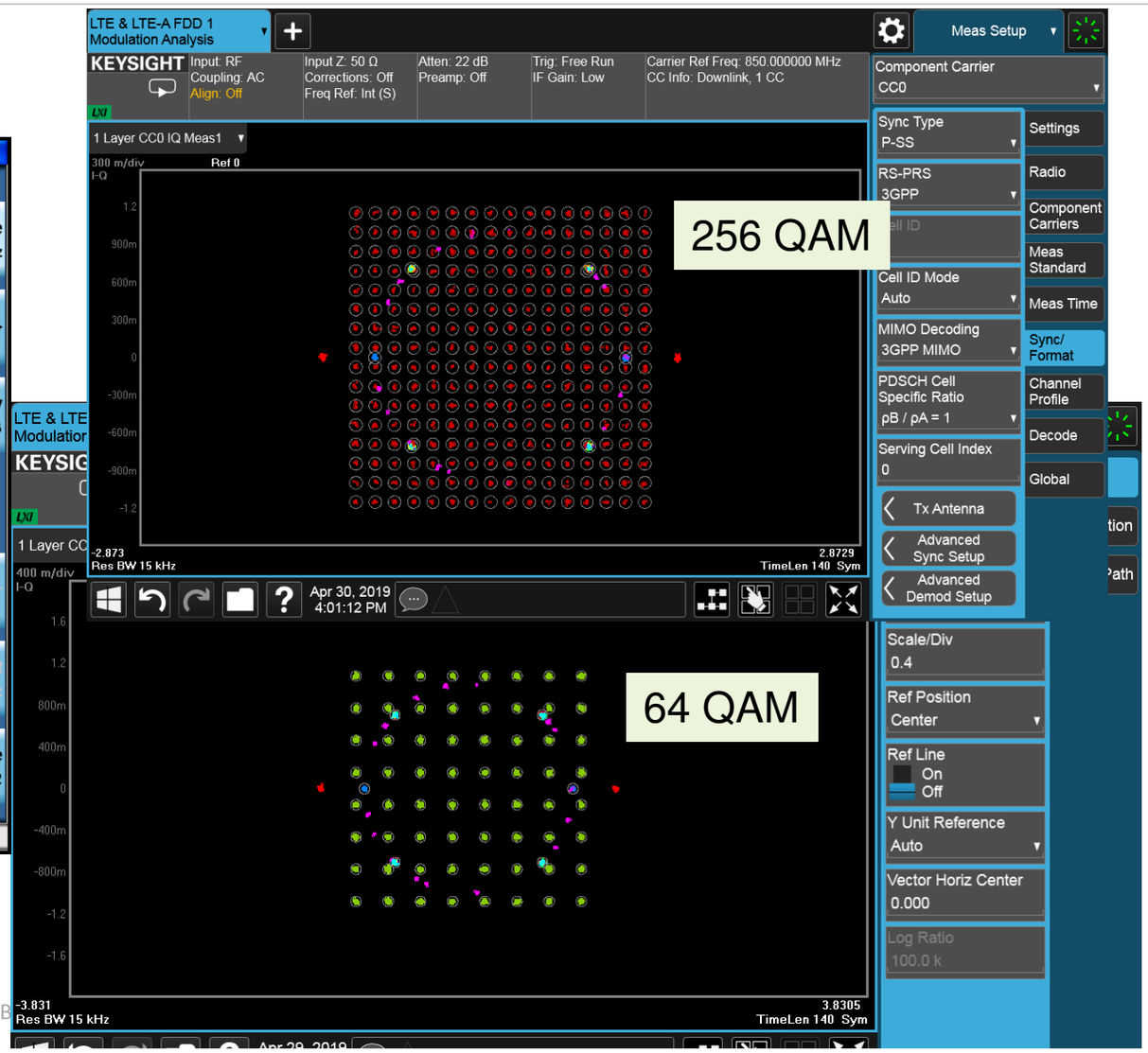
Programmable charge pump

Programmable offset current

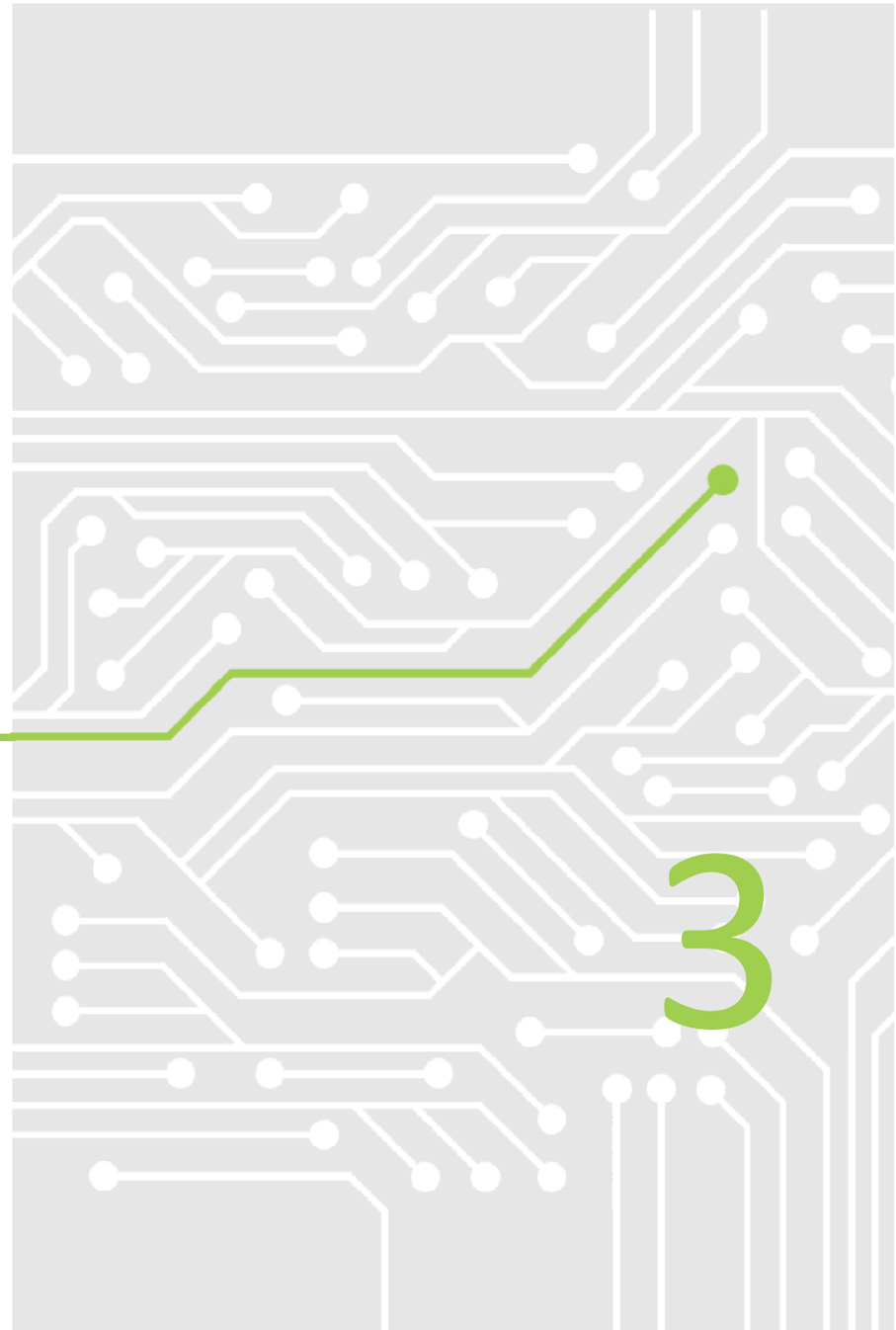
Programmable loop filter

Synthesiser performance at 866MHz





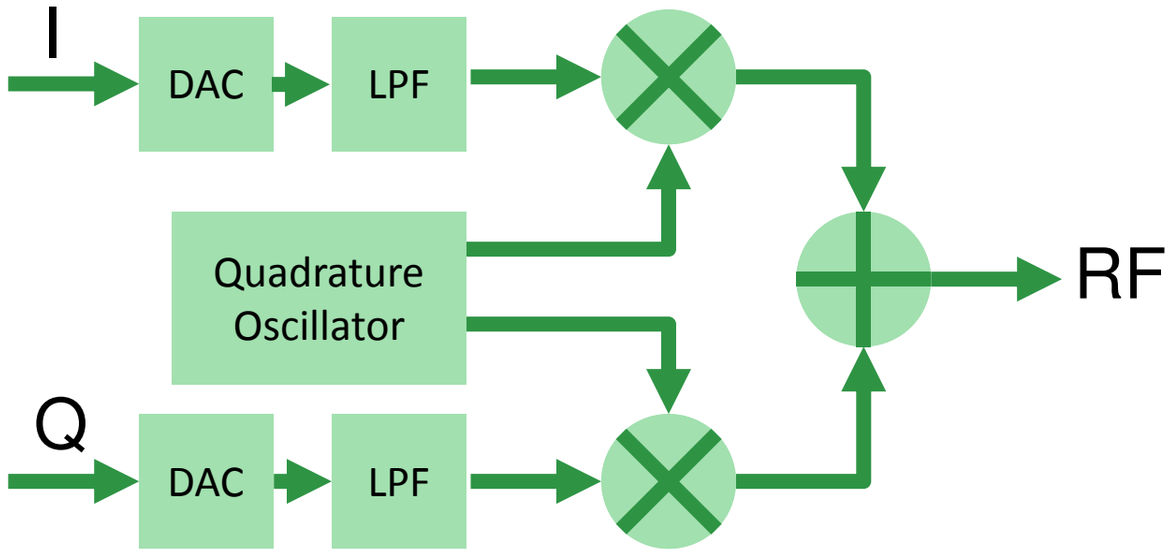
Digital Vector Transmitter



Digital Vector Transmitter

Digital I,Q data

- Converted to analogue by Digital to Analogue Converter (DAC)
- DAC output cleaned by Low Pass Filter
- Removes Aliases



Sampled Data Systems and Nyquist

Sampled data systems

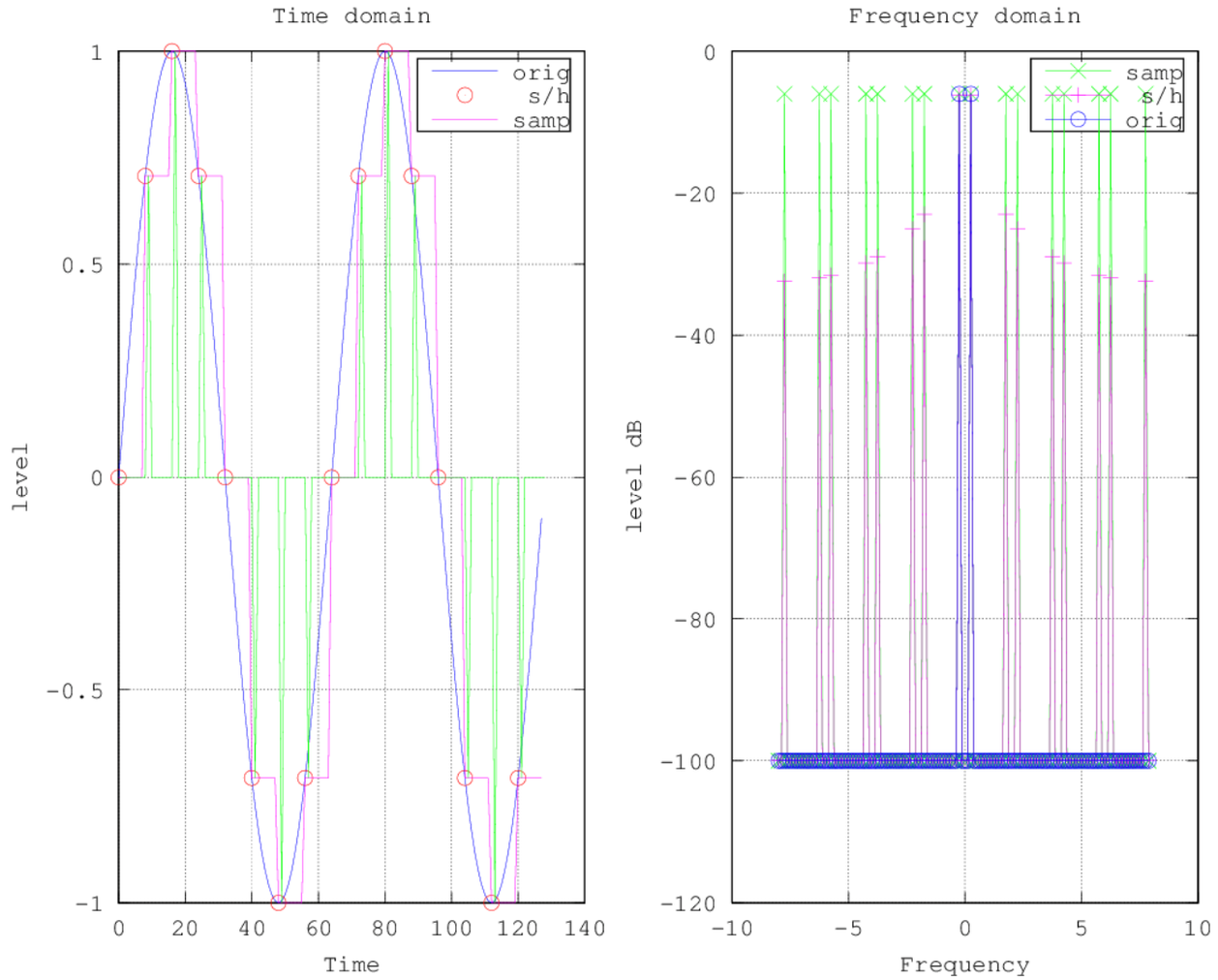
- look at a waveform only at fixed moments in time,
- Points usually equally spaced.

Nyquist Sampling

- Input signal frequency less than sampling rate

Reconstructed signal

- Sample and Hold
- **Aliases** occur above the sample rate.



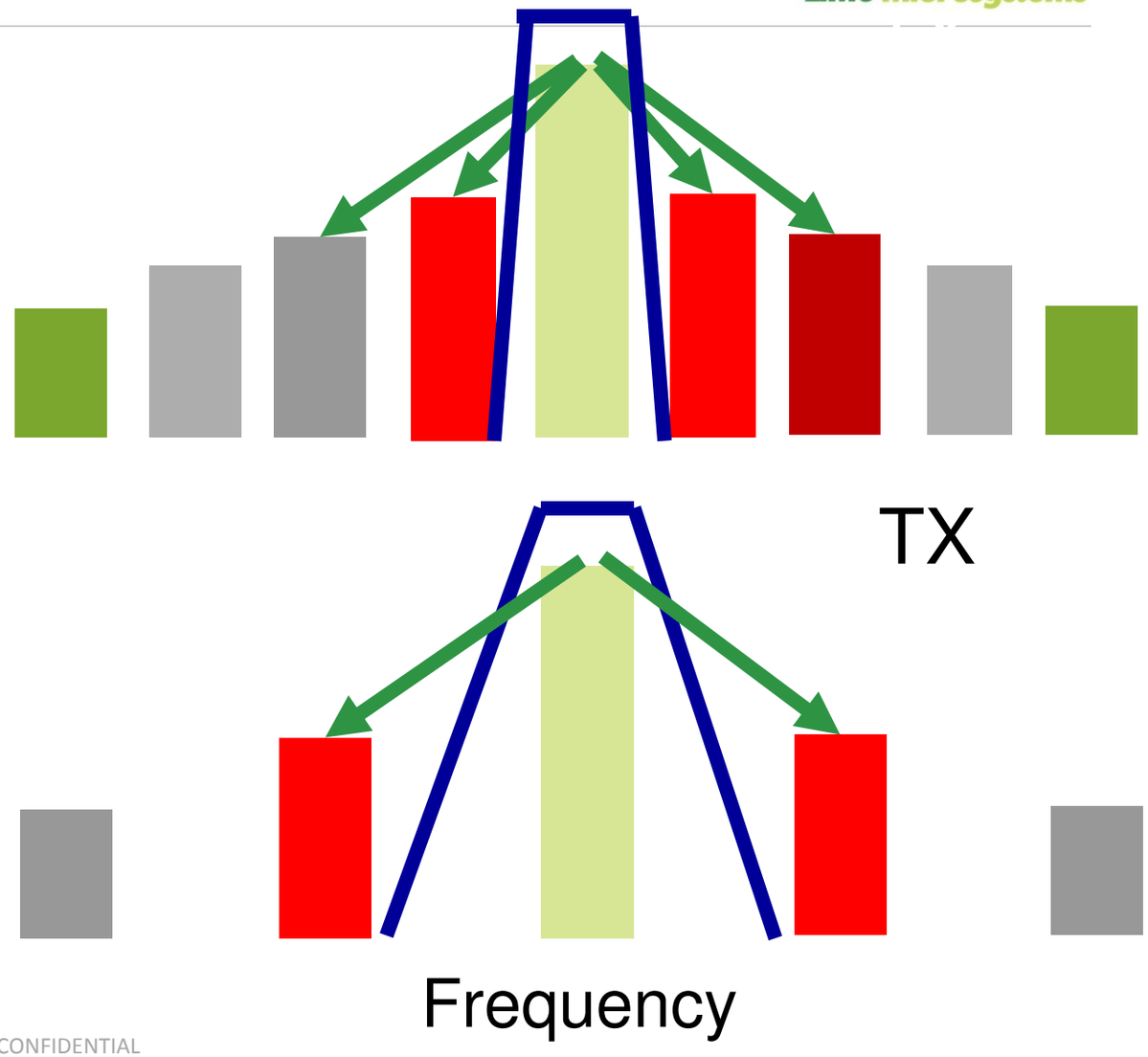
Aliasing and the Adjacent Channel TX

TX

- Aliases lead to transmitting interference in adjacent channels.
- Not easy to filter.
- Bad Neighbour (ASBO from OFCOM)

What happens if we double the sampling rate?

- Oversampling
- Aliases are further away.
- Filter specification can be relaxed



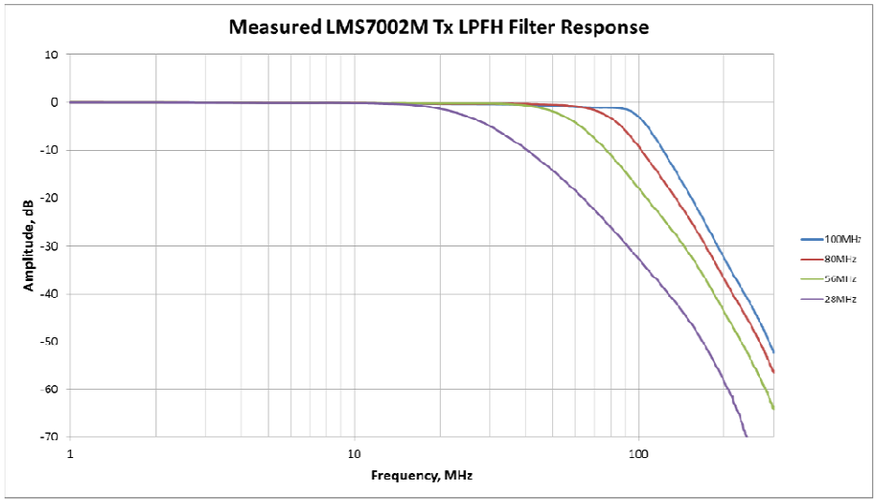
LimeSDR TX Active Filters

LPFL

- 4th Order Chebychev
- Optional Real Pole

LPFH

- 2nd Order Butterworth



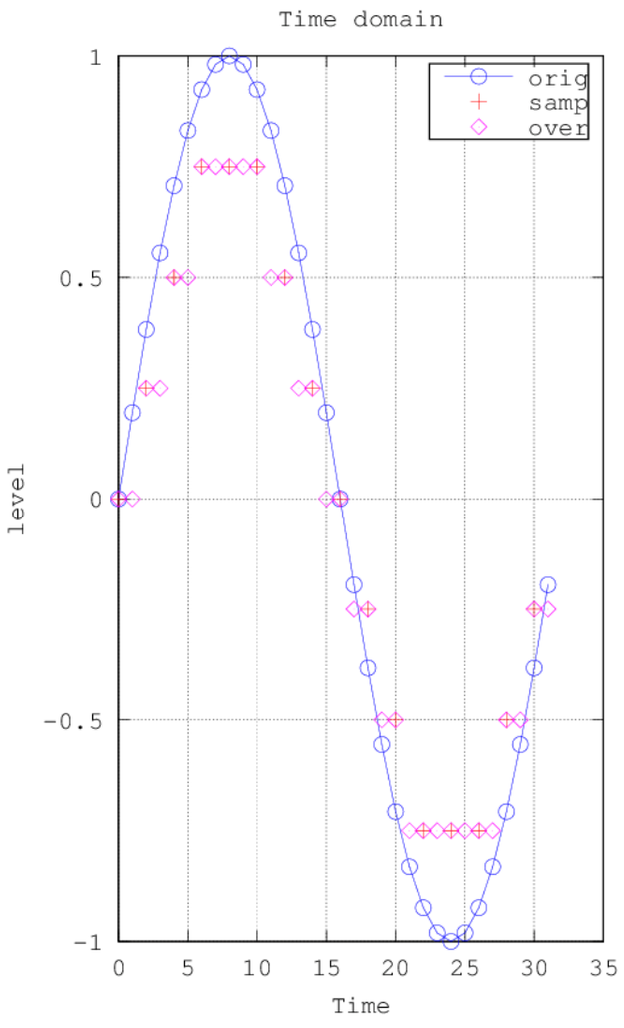
Quantisation and Noise

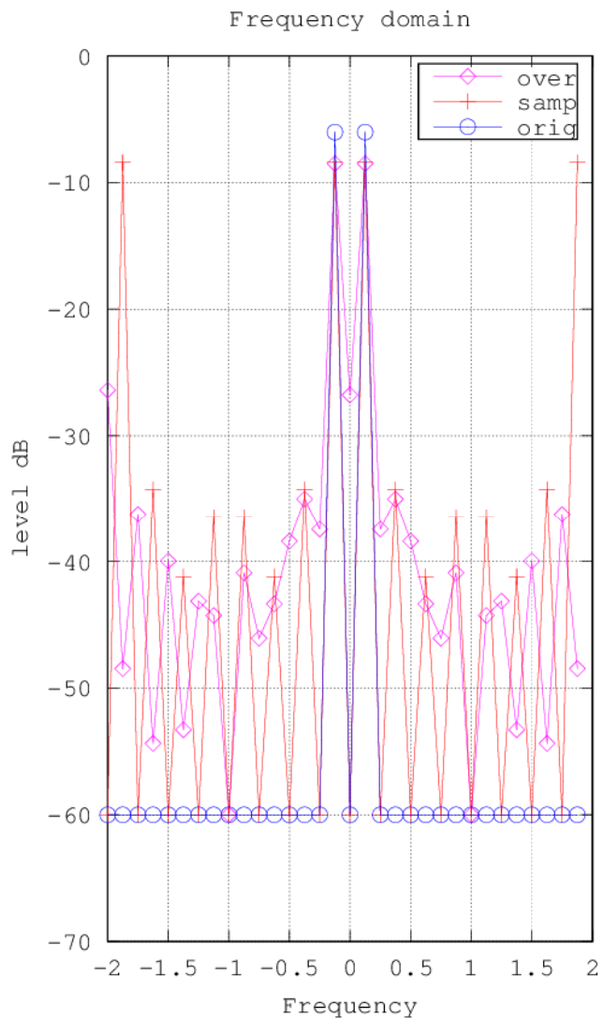
ADCs/DACs finite number of bits.

- Quantised data never completel accurate.
- LMS7002M ENOB>=9 bit.
- >56dB Dynamic Range

Illustrate with 3 bit ADC

- 8 levels available
- Not all levels are normally used!
- Every sample point contains an error.
- Looks like noise spread over the frequency domain.
- Over sample to reduce noise.
- 1 bit for ever x4 oversampling





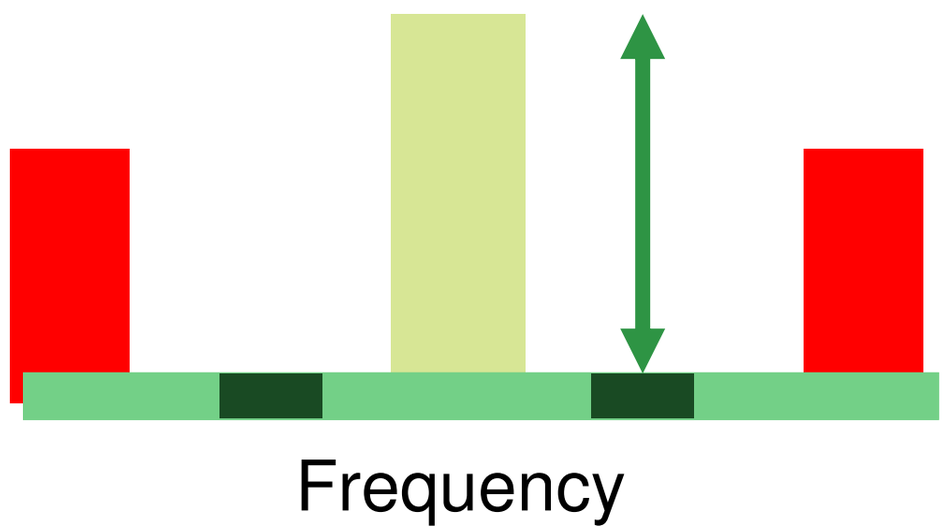
TX Oversampling and Quantisation Noise

Oversampling

- Reduces quantisation noise
- Removes aliases away from signal
- Improving Adjacent Channel Power Ratio (ACPR)
- Good Neighbour

LimeSDR

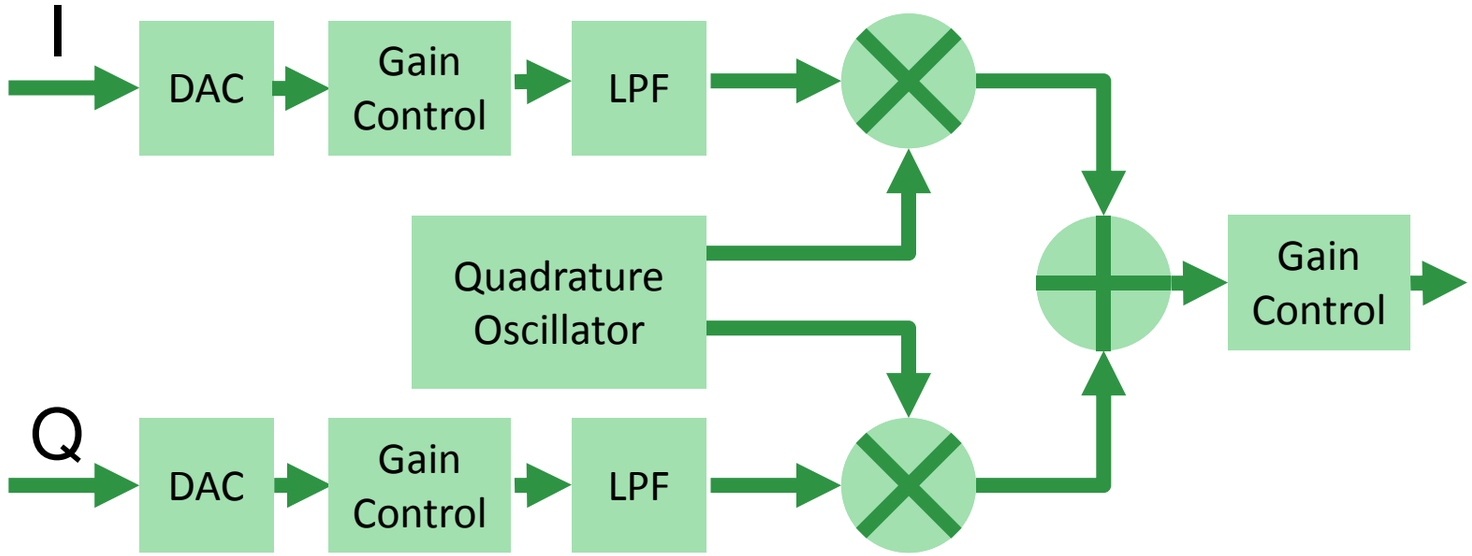
- Intended to work with high oversampling.
- E.g. 3G/4G Base station
- Data Rate 30.72Ms/s
- TX 491.52Ms/s x16 Oversample
- RX 122.88Ms/s x4 Oversample



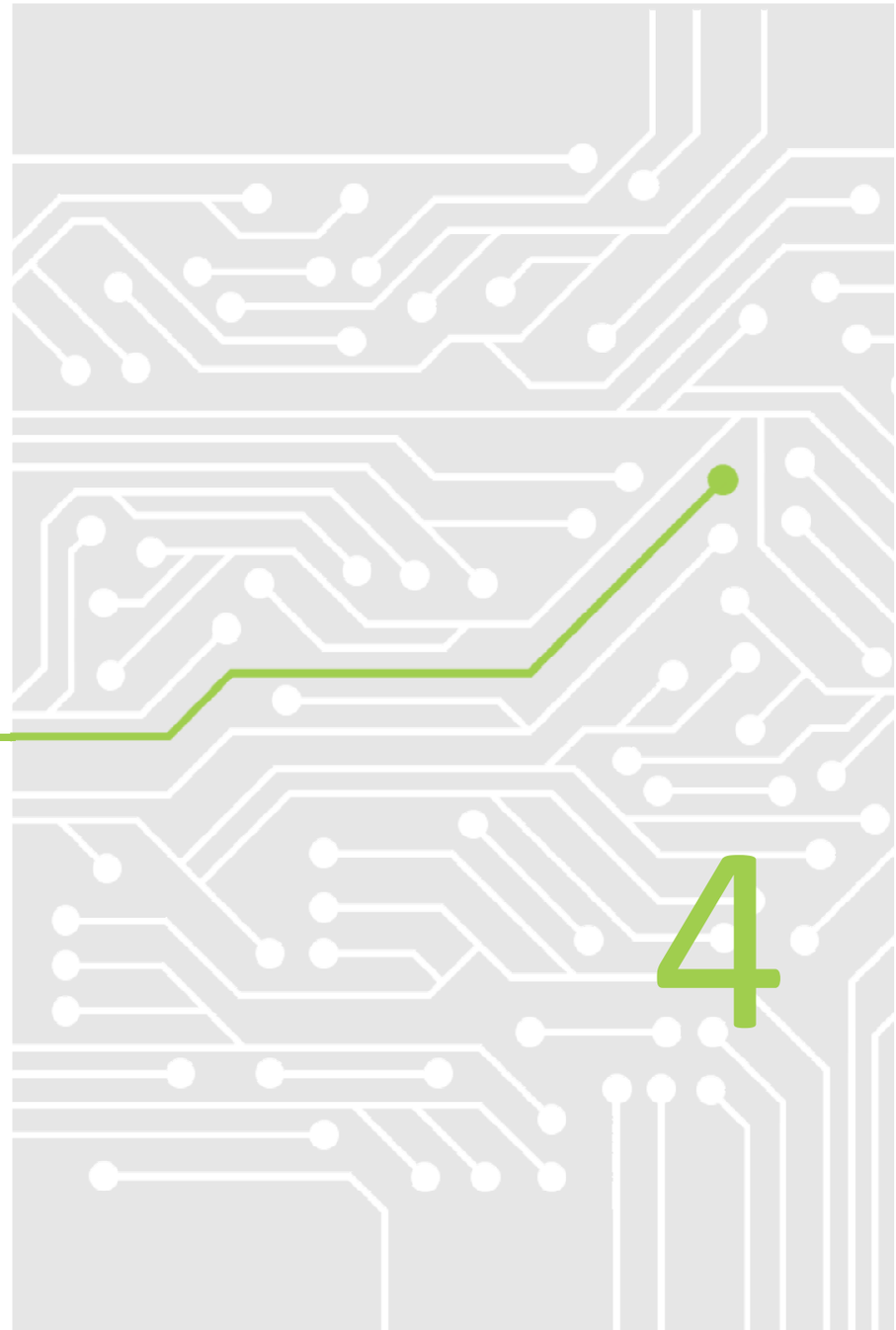
Digital Vector Transmitter

DACs and Mixers work best with optimum signal levels.

- Need gain control at input of mixer
  - LMS7002M IAMP (0-63)
- Need gain control to vary output level.
  - LMS7002M TPAD (50dB)
  - Power ramping for TDD systems e.g. GSM/EDGE
  - Power control for multiple access systems e.g. W-CDMA



Analogue Receiver



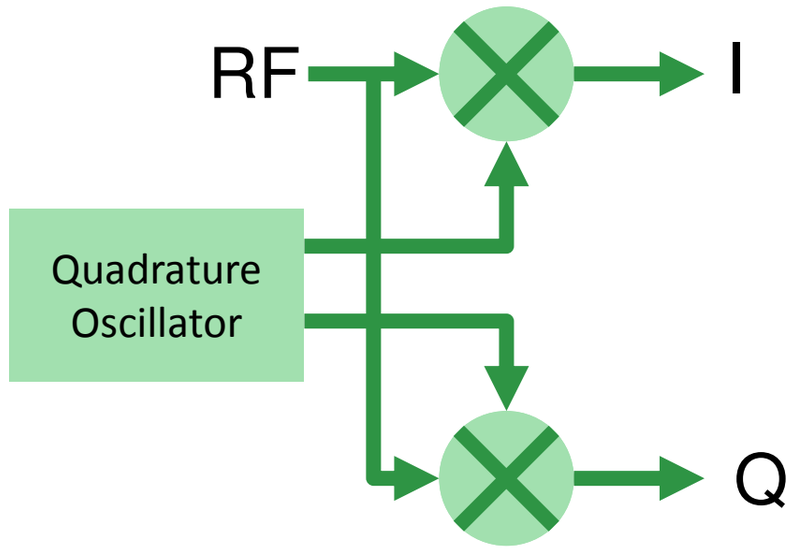
Digital Vector Receiver

Zero IF Receiver

- Image Rejecting Mixer

Quadrature outputs processed by baseband.

- Noise of I and Q uncorrelated.



The Image Rejection Problem

Real modulation signals

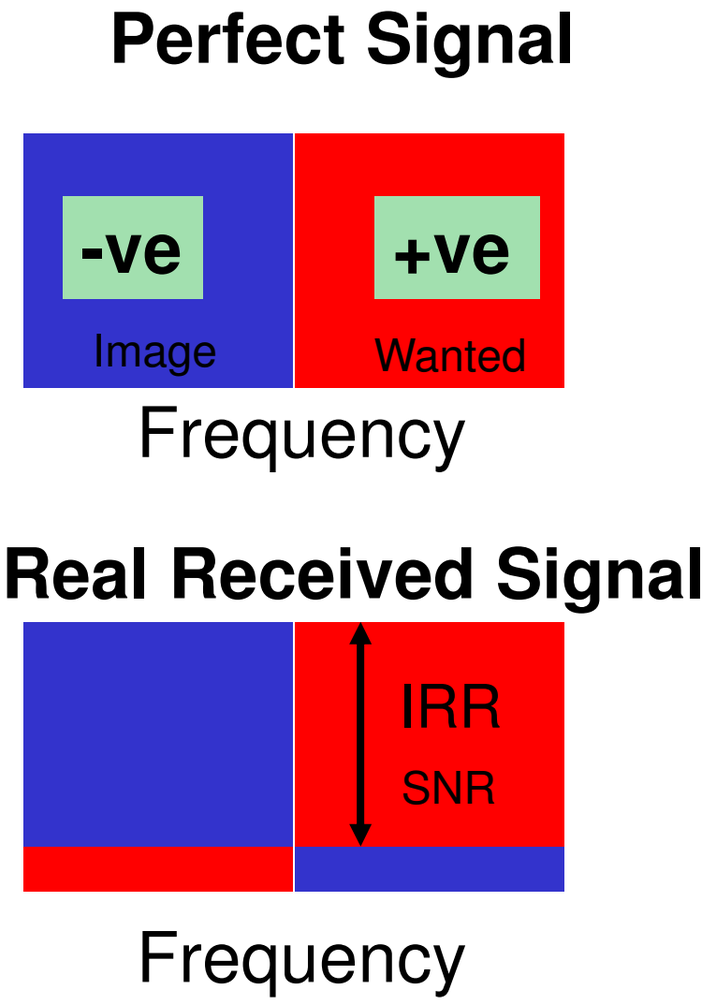
- Positive frequency different to negative frequency.

Hetrodyne Type Receivers

- Image separated from Wanted signal by a frequency gap.
- Can filter out the image.

Homodyne Type Receivers

- Image shares the same frequency space.
- Image leakage looks like noise floor to the wanted signal.
- So Image Rejection Ratio IRR directly affects inband SNR and EVM
- Can be corrected by calibration and digital techniques



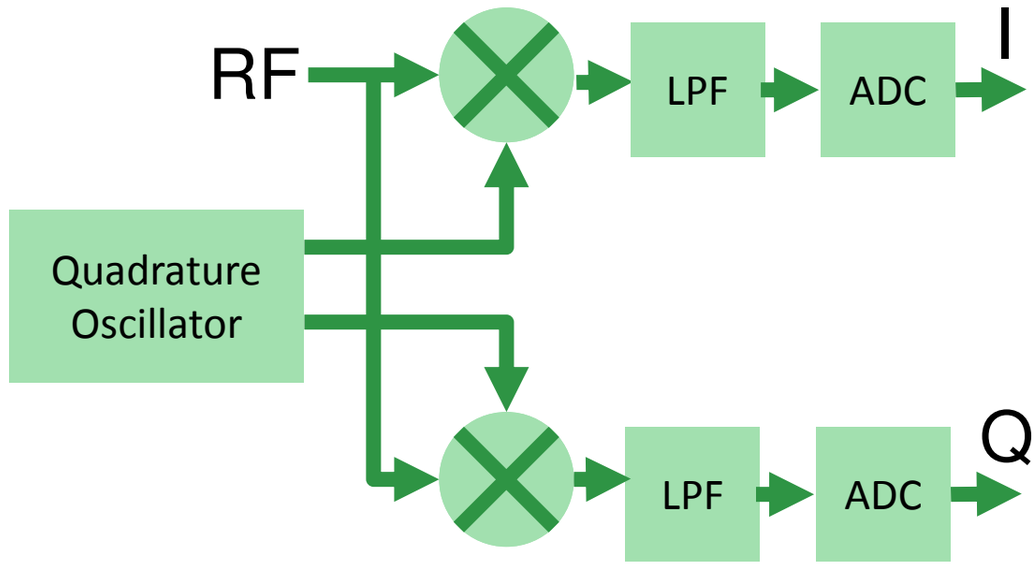
Digital Vector Receiver

I and Q channels filtered before quantisation.

- Prevents aliases
- Reduces noise

Analogue to Digital Converters

- Convert analogue IF signals to digital.

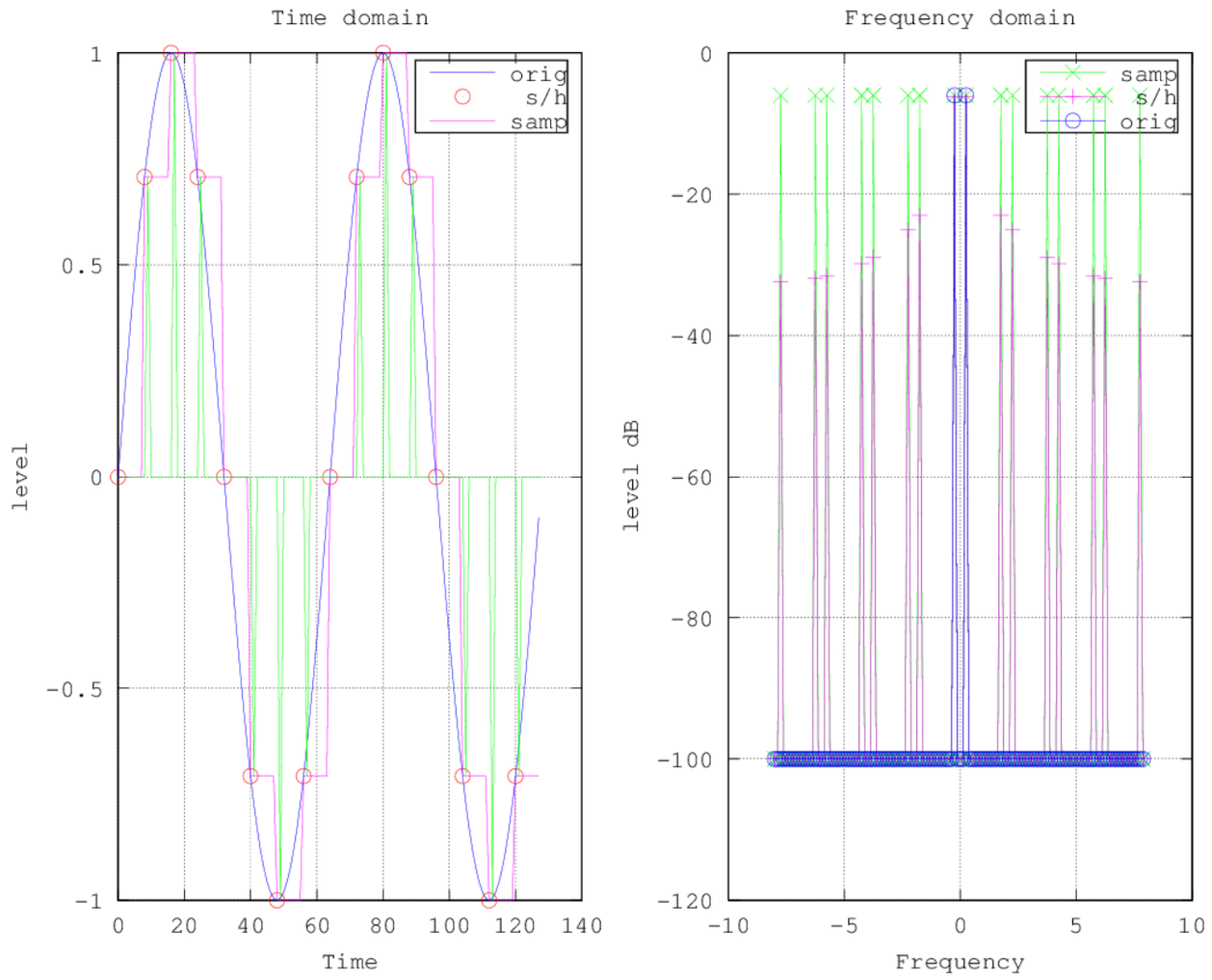


The wanted signal digitised

ADC Reverse of DAC process

Almost…

- Sampled signals are vulnerable to aliases.
- All ADC aliases seen equally.
  - Unlike sample and hold case.

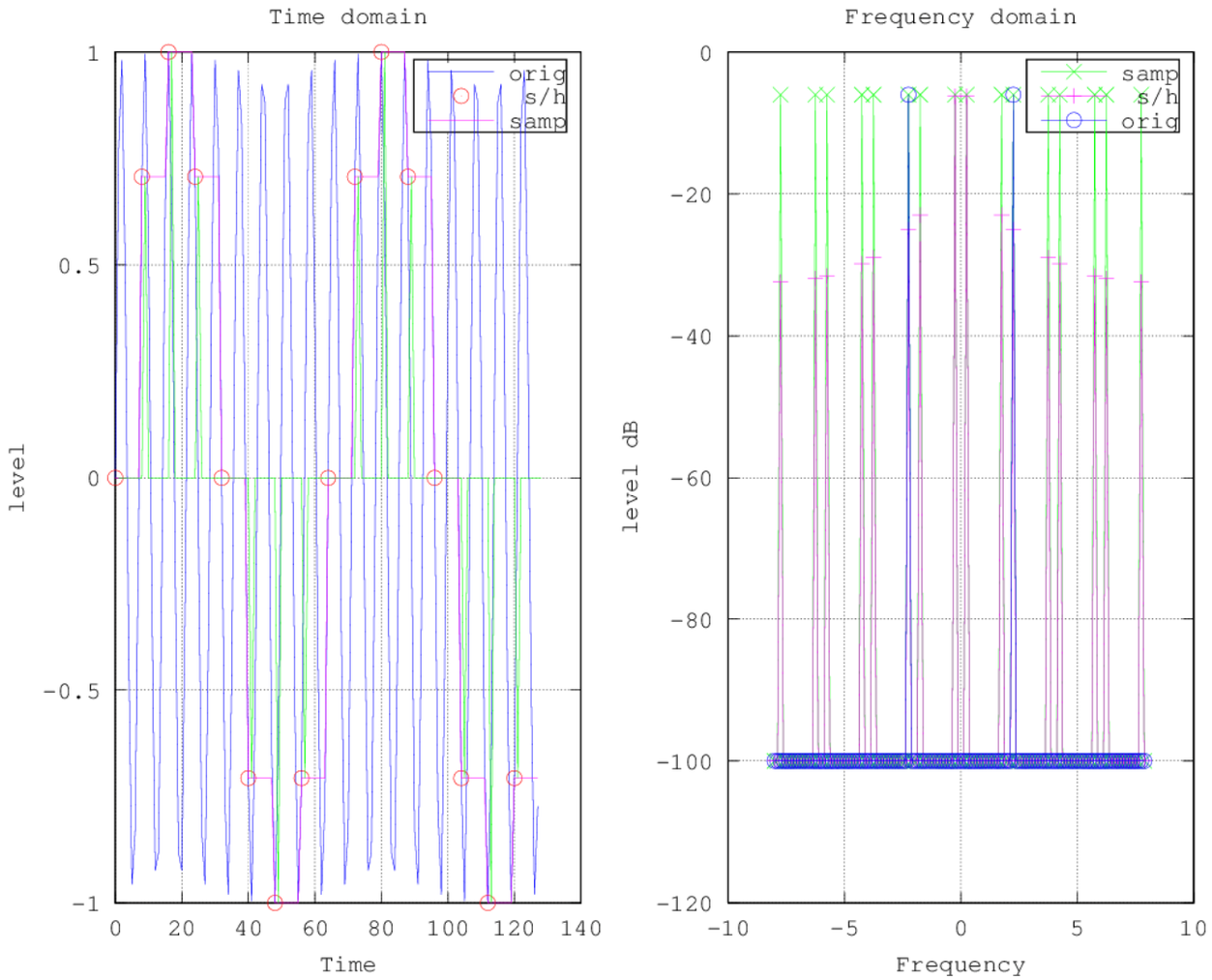


Let’s meet an alias signal

If we violate Nyquist Sampling…

- injecting an input signal whose frequency is higher than the sampling rate.
- Cannot tell it apart from a signal that was lower than the Nyquist Sampling Rate.

<u>Must filter before sampling</u> to prevent interference.



Aliasing and the Receiver

Adjacent channels are superimposed on the wanted signal degrading sensitivity.

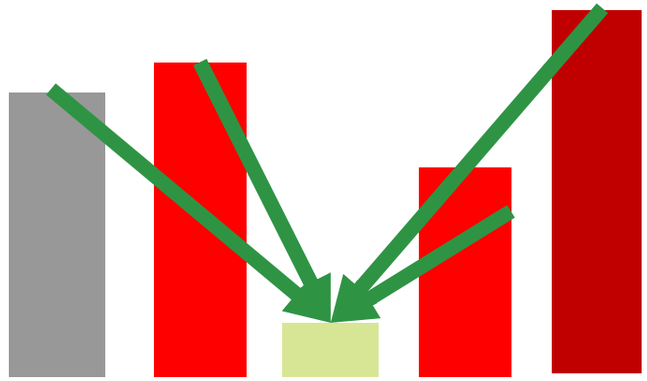
- Common figure of merit Adjacent Channel Rejection.

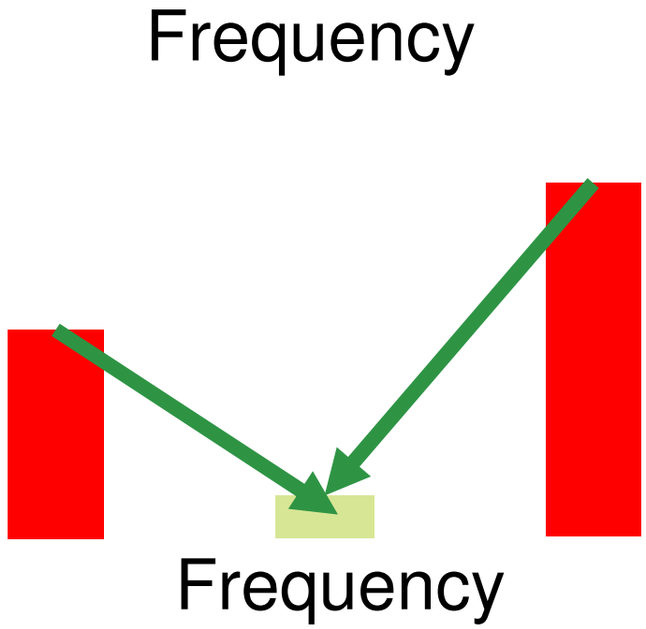
Performance improved by

- Analogue IF filtering before ADC
- Oversampling of ADC to move alias outside the bandwidth of IF and RF channel filters

Real Systems

- Adjacent channel rejection is a function of ADC bits, IF filtering and Forward Error Correction Coding.

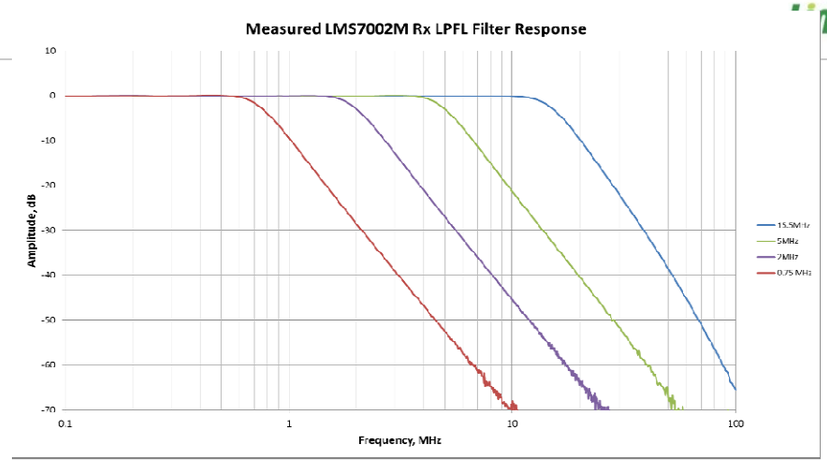


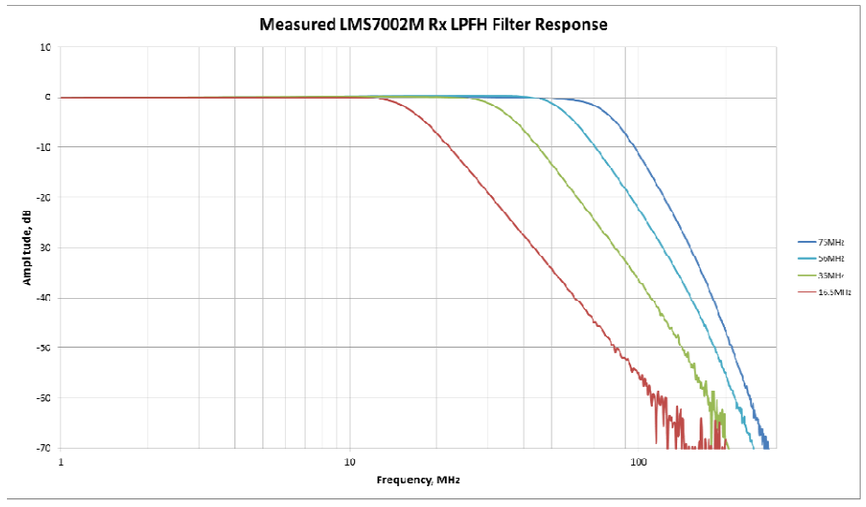


LimeSDR RX Active Filters

Nominal Filter Spec

- 0.5dB Ripple Chebychev
- 3rd Order
- TIA – Real Pole
- LPFL/H – Complex Pole Pair
- Ratio of TIA and LPF capacitance set filter shape.





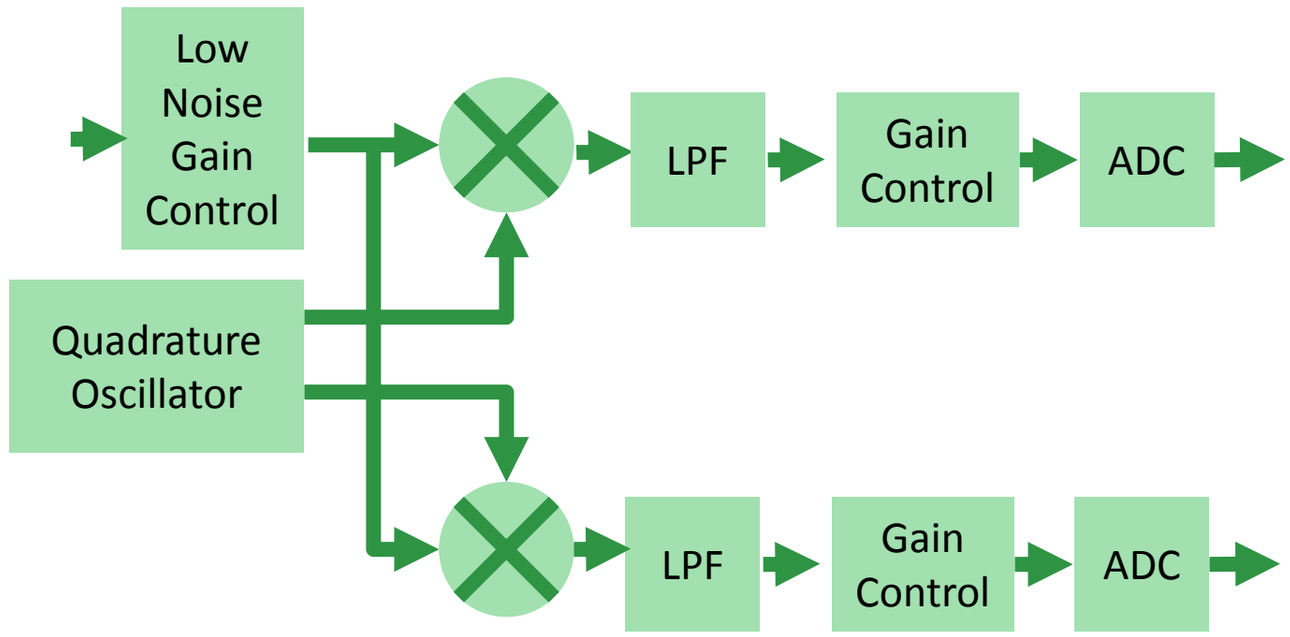
Digital Vector Receiver

Mixers give best performance when levels are right.

- Variable gain Low noise LNA before mixer. (30dB)
- Avoid Mixer Overload for best dynamic range.

ADCs like big signals

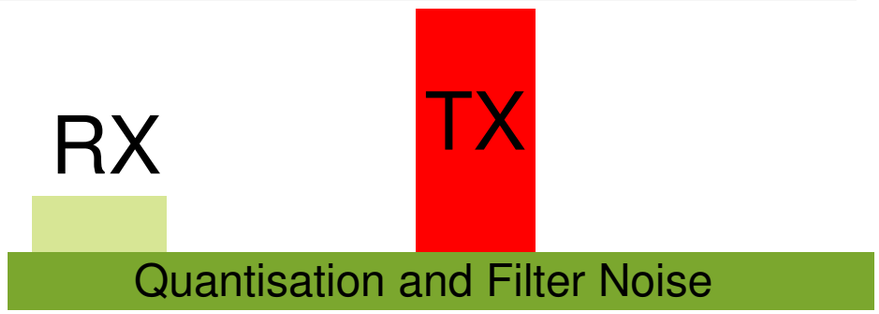
- Variable gain before ADC (PGA) -18 to +19dB



TX Out of Band Noise Problem

FDD – TX is often your worst interference signal

- Quantisation and Active Filter Noise
- Far Out Phase Noise
- Can deafen receiver, especially if TX is amplified before transmission.

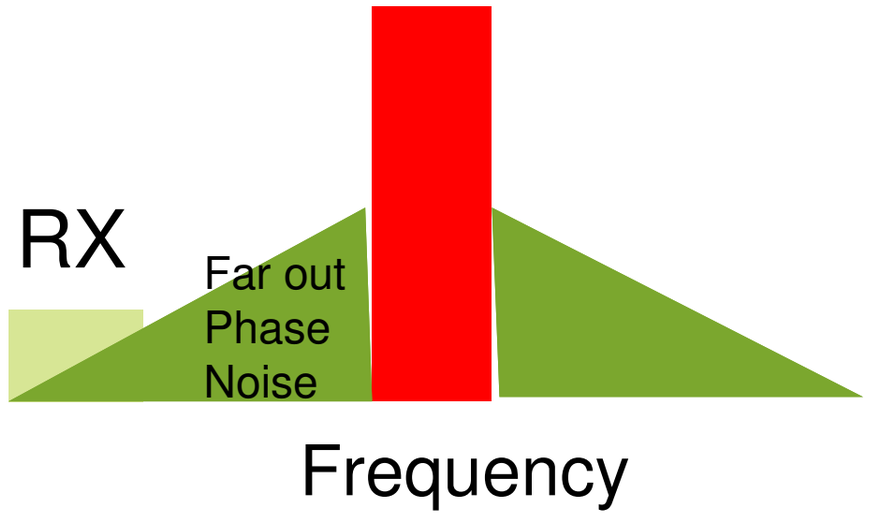


Time Division Duplexing (TDD)

- Transmitter switched off during receiving.
- Cannot receive or transmit continuously!

Frequency Division Duplexing (FDD)

- Transmit and receive at different frequencies.
- Duplexer filter to isolate TX and RX. Typ 50dB
- +25dBm-155dBc-50dB=-180dBm/Hz (Below thermal noise+NF -171.5dBm/Hz)

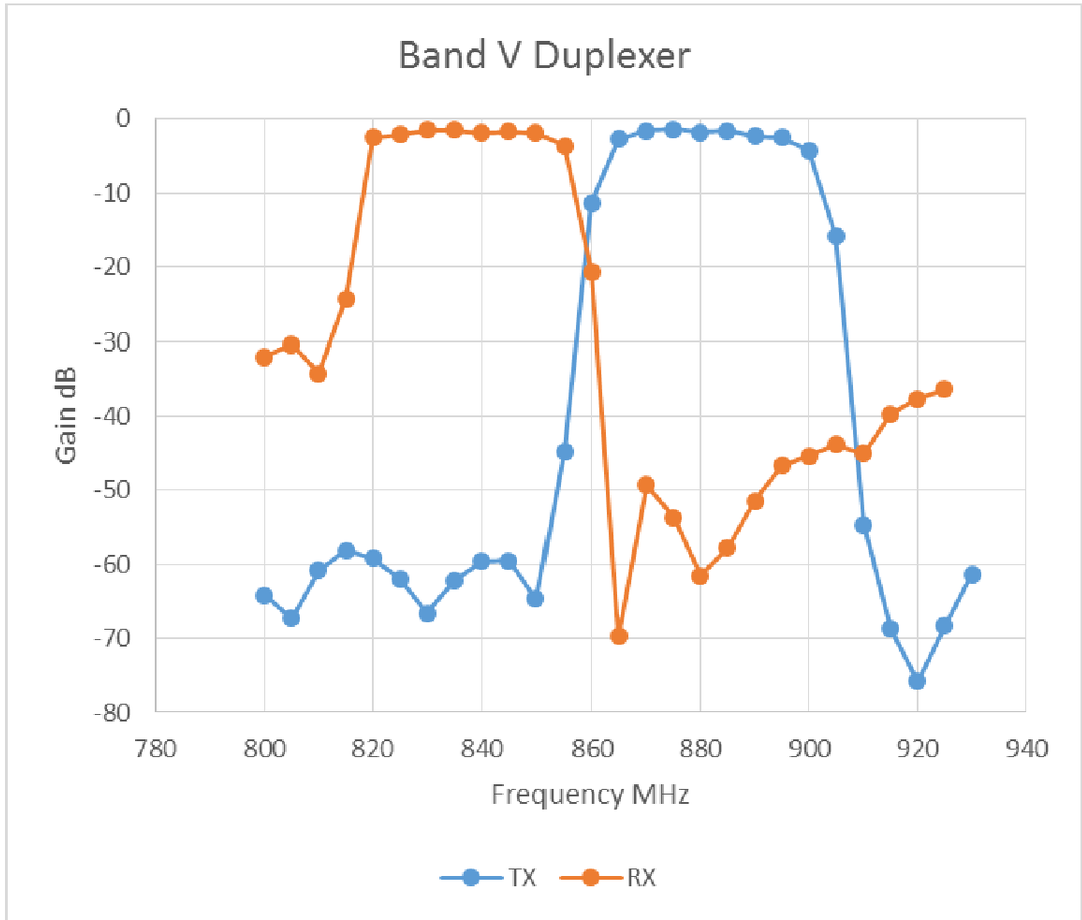


Example FDD SAW Duplex Filter

Duplexer isolates TX and RX from one another, whilst sharing the same antenna.

Low cost SAW Duplexer filters are commonly used in handsets and femto cell base stations.

Expensive cavity filters used in high power transmitters.



RX Phase Noise Problem

3G/4G "Femto-Cell" Blocker Requirement

- -15dBm CW Blocker 20MHz from band edge of RF filter.

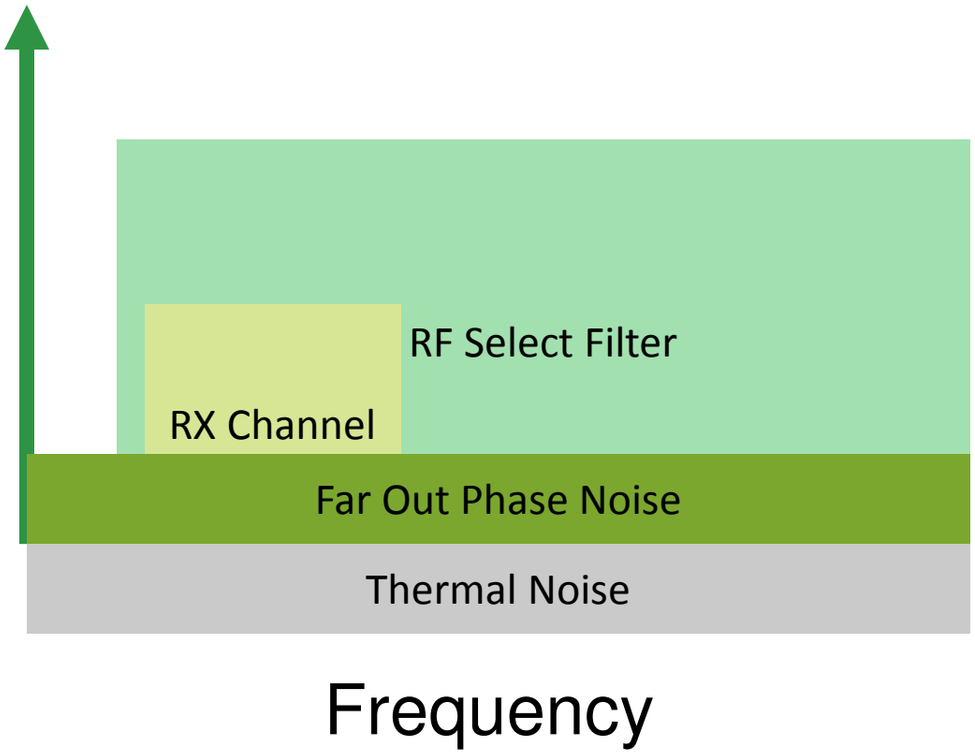
RF Filter provide partial filtering of CW Blocker

- 5-20dB and 2dB loss.

P1dB of LNA >-25dBm

- Far out phase noise of synthesiser must be around -155dBc
- Phase Noise -20dBm-155dBc=-175dBm/Hz
- Thermal Noise -174dBm+2.5dB+2dB+0.5dB
- =-169dBm/Hz (NF=2.5dB)

Loose about <1dB sensitivity



Rx Inband and Out of Band IIP3

Receivers are vulnerable to distortion signals

- E.g. Large out of band signals
- Vulnerability measured using 2-tone distortion

LMS7002M has very linear mixer and LNA.

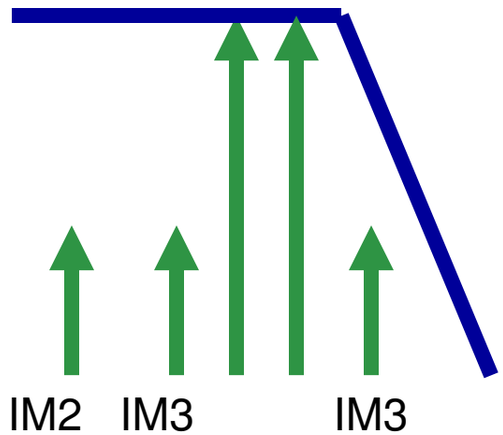
Inband IIP3/IIP2 limited by P1dB of system

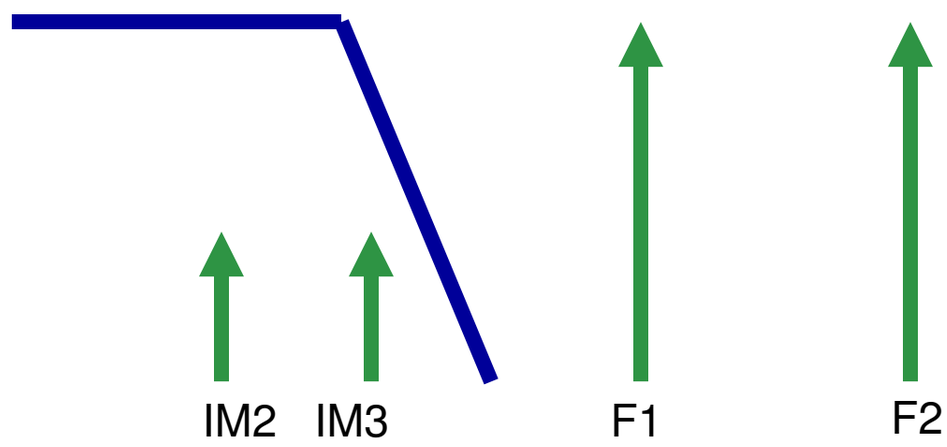
- Gain sensitive

Out of band IIP3/IIP2 limited by P1dB of LNA and Mixer

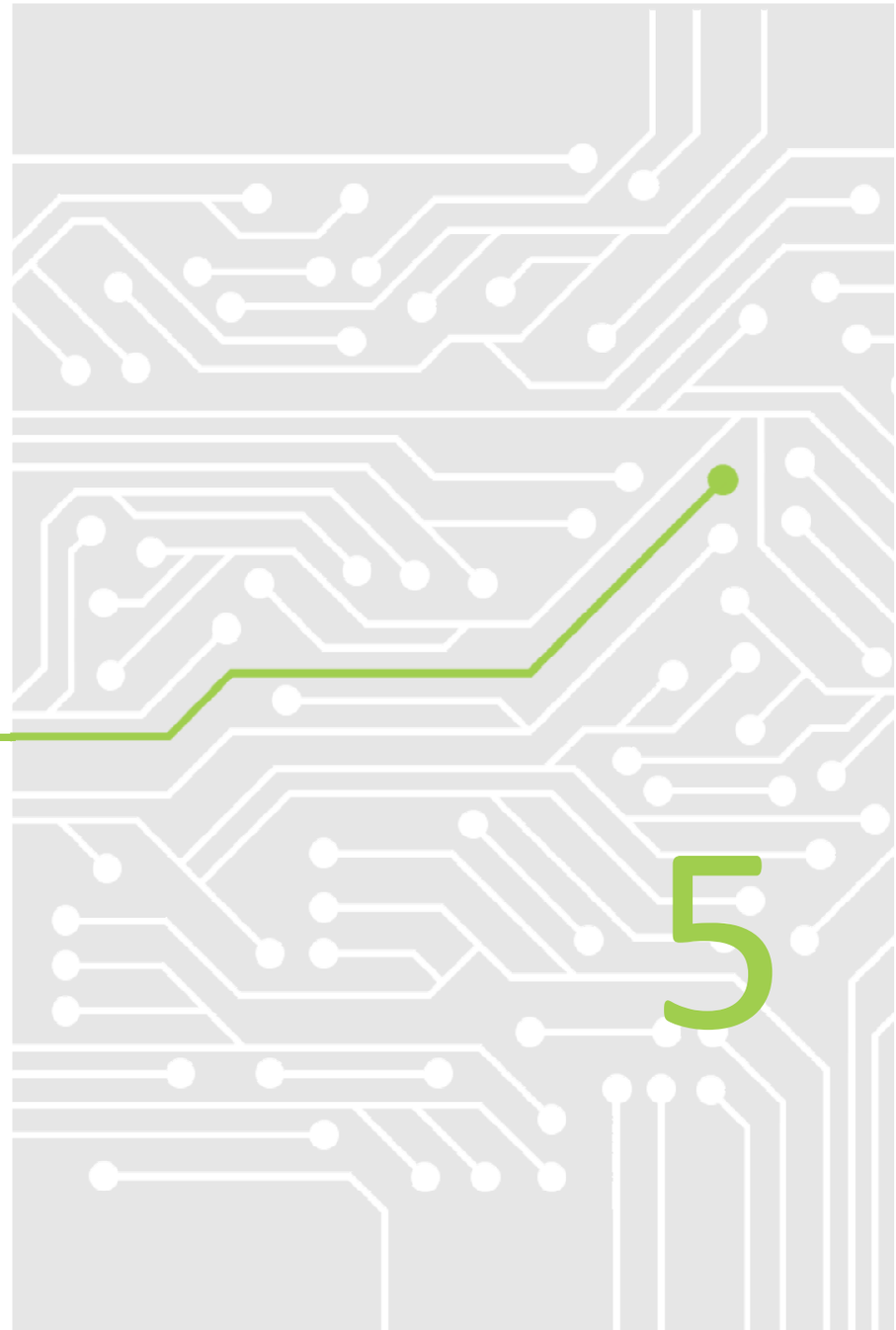
- LNAL 915MHz LPF 600kHz
- IIP3=+5.5dBm IIP2>48dBm

- LNAH 1980MHz LPF 2.5MHz
- IIP3=10.8dBm IIP3>40dBm

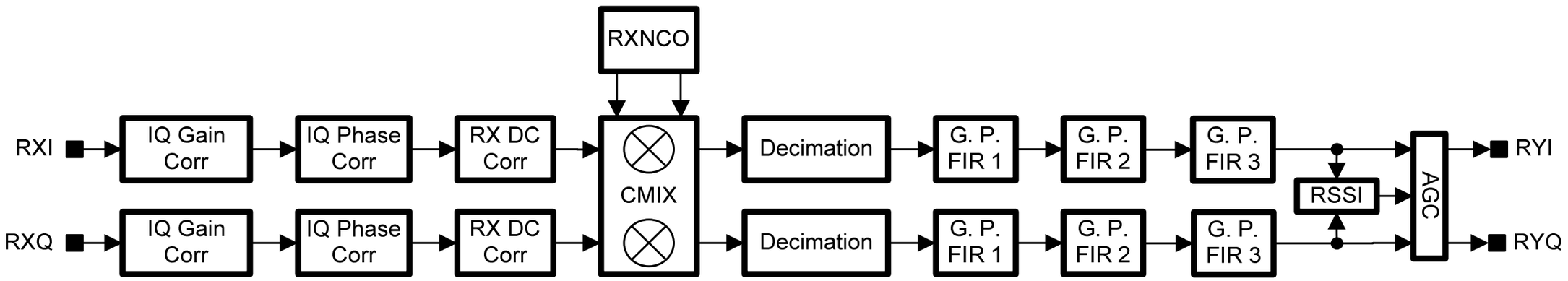


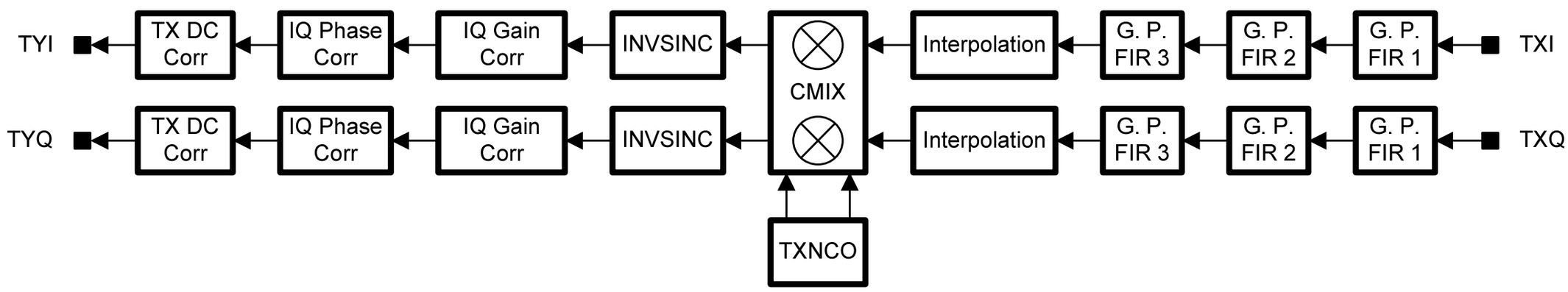


Digital Baseband



LMS7002M FPRF Transceiver Signal Processing TSP





Digital Filtering

Inverse Sync (TX)

- Sample and Hold has a frequency peak as signal approaches half sample rate.
- Inverse Sync corrects for this.

Interpolation (TX) and Decimation (RX)

- Want slowest possible data rate into the LimeSDR
- Want fastest sample rate for DAC/ADC
- Interpolation=Upsampling+Filter
  - Upsampling [P1,P2,P3]-->[P1,0,P2,0,P3,0]
- Decimation=Filter+Subsampling
- On chip decimation and interpolation allow data rate conversion.

General Purpose FIR Filters

- Allows additional filtering
- Usually low pass
- High pass and band pass are possible
- Available taps depends on Decimation and Interpolation rates.
- Filter coefficients can easily be designed in Octave or Matlab.

NCO, Complex Mixer, Test Signals and Calibration

Numerically Controlled Oscillator

- Programmable precision quadrature digital oscillator
- Can be used as a test signal

Complex Mixer + NCO

- Can be used as low IF receiver
- Can be used for fast frequency hopping <50us
- Can be used Filter bandwidth Calibration
  - Baseband Loop back

Other Digital Features

Digital AGC

- Intended for Repeater type applications.

Digital RSSI

- Intended for calibration and software controlled AGC.

DC Register load in Tx TSP

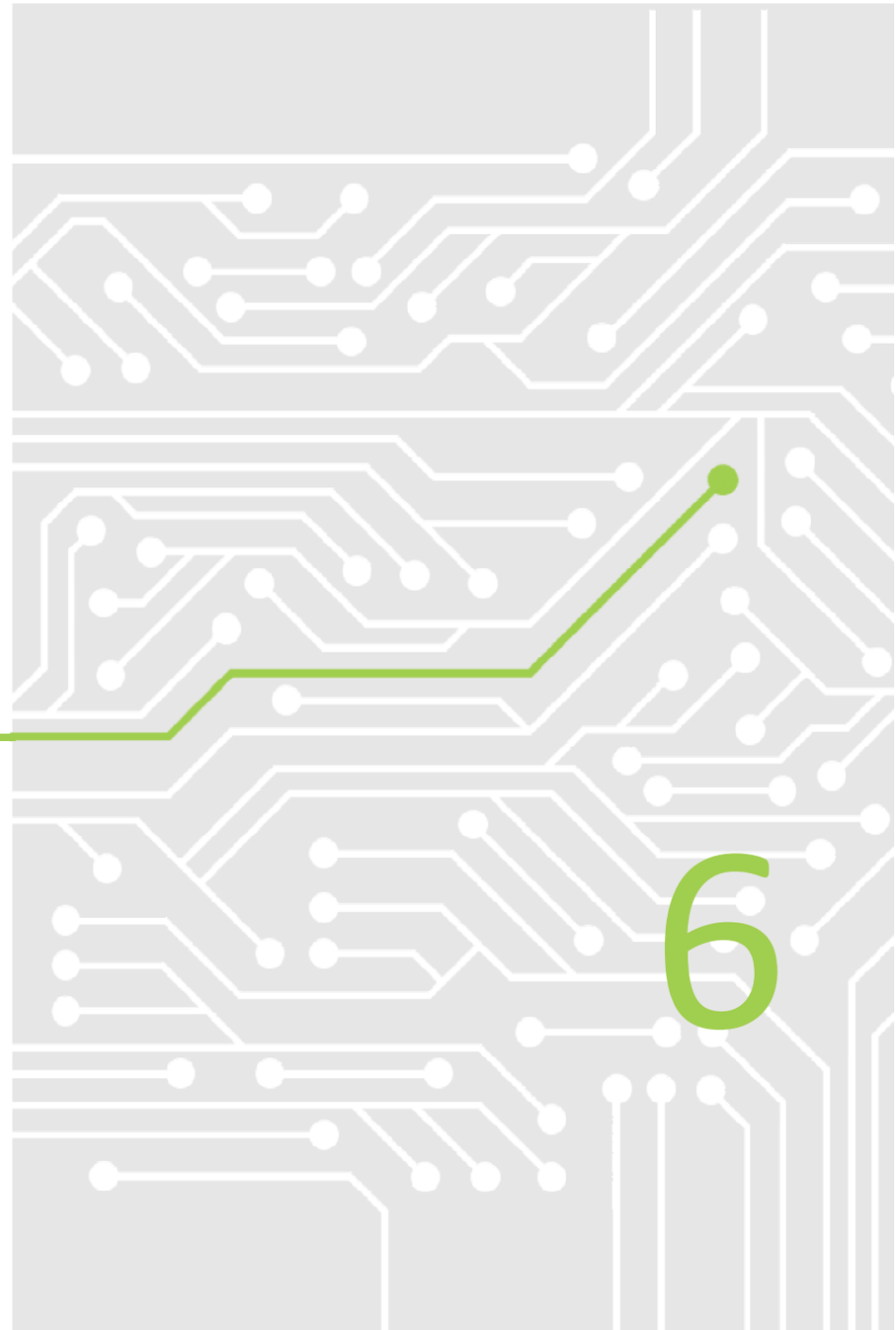
8051 Based MCU

- Calibration loops

LimeLight interface

- LimeSDR preconfigured to match published FPGA gateware.
- For custom FPGA designs allows flexibility in timing and sample ordering.

LimeSutie GUI



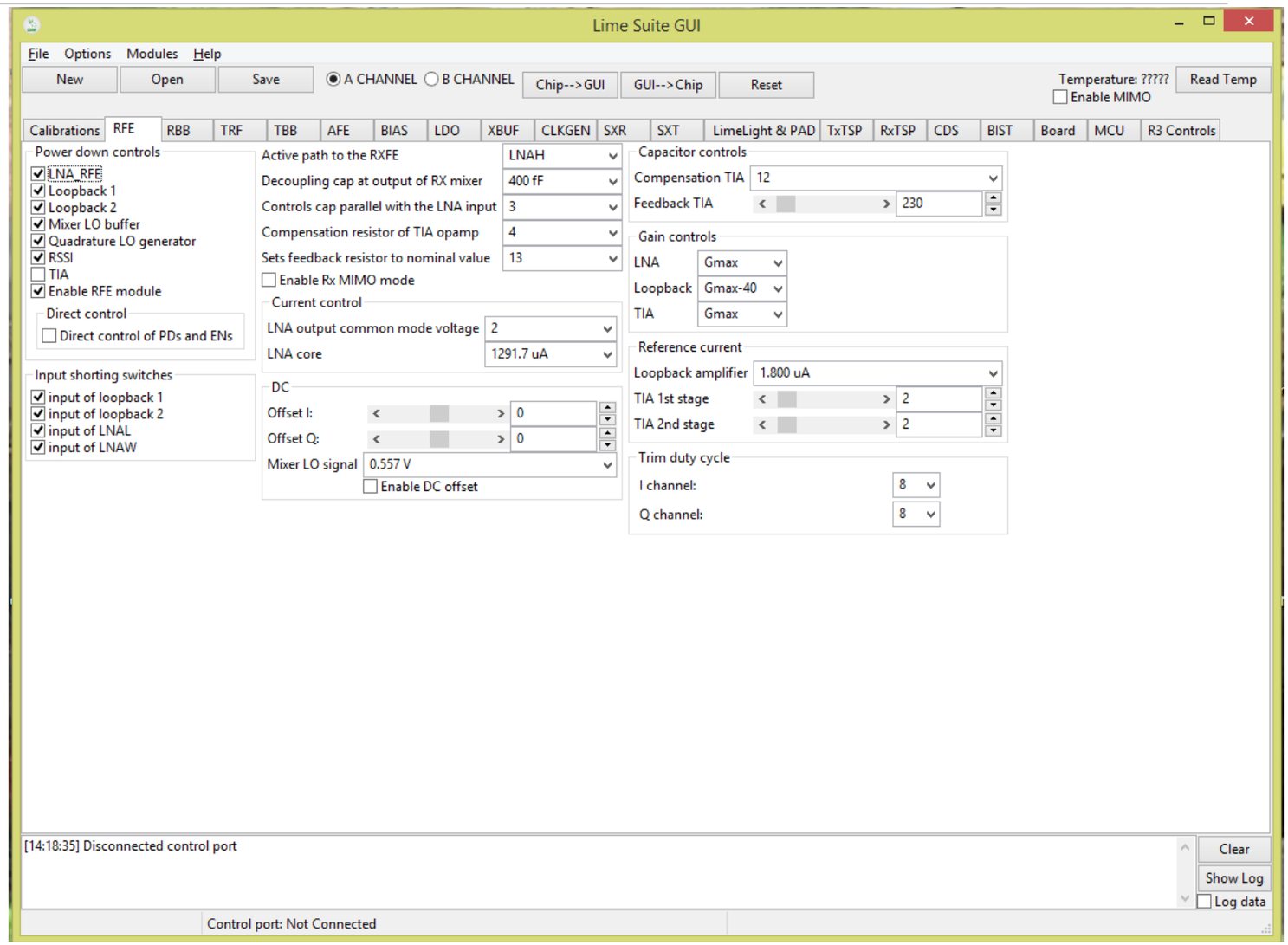
LimeSuiteGUI

Access to ALL registers of LMS7002M

Controls grouped into sections.

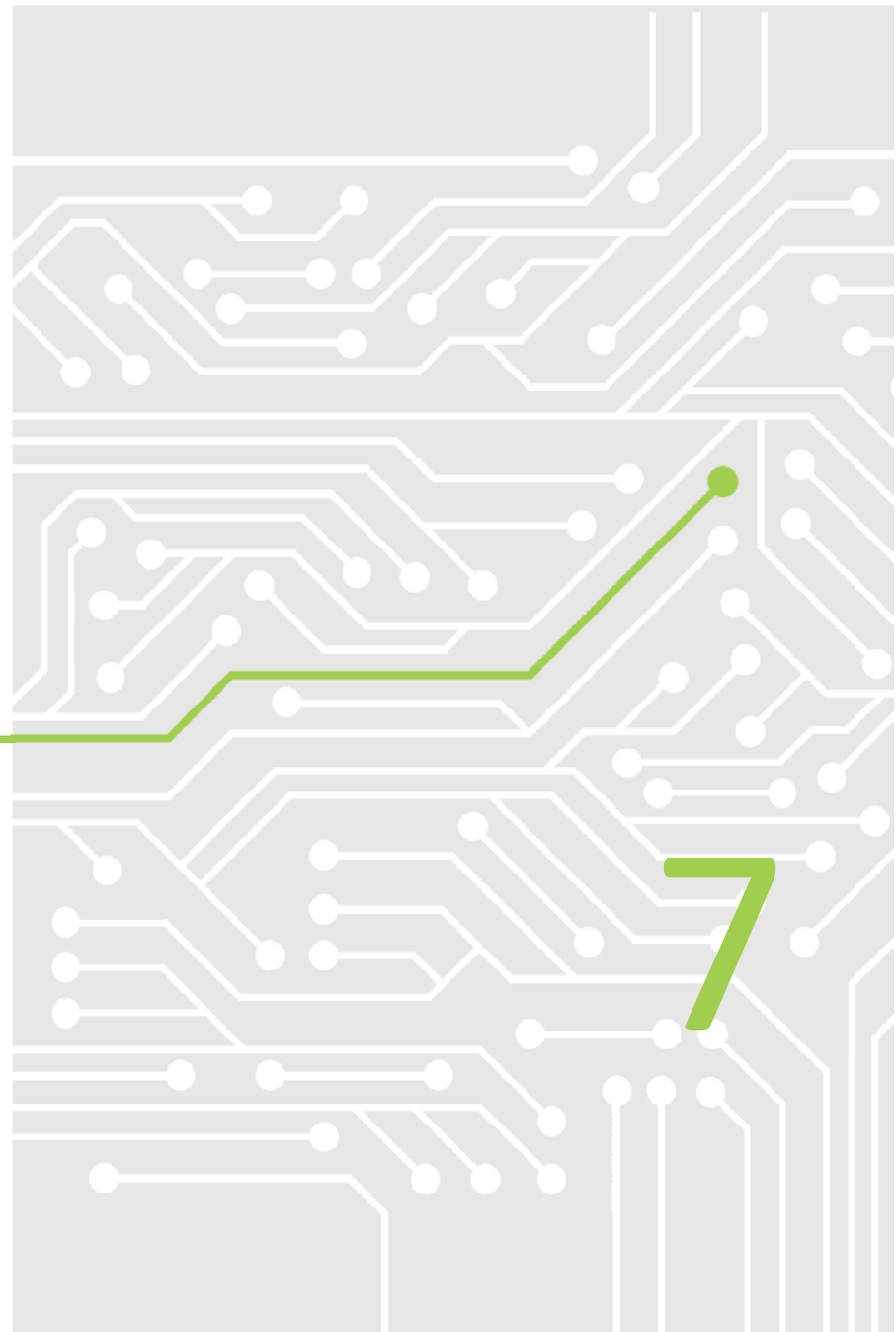
- MIMO Controls have A and B channel

We will use this software in our practical session.



Lime microsystems

LimeSDR FPGA



Modifying the LimeSDR FPGA

FPGA

- Currently provides interface between USB controller and LMS7002M Radio.
- Also provides RAM controller for waveform playback.

Can I alter the FPGA?

- Yes

Altera design tools

- Free for Cyclone 4E
- Download from Altera

Code for the LimeSDR FPGA

- open source.
- Download from Myriad RF

Design Environment

- Quartus Prime 16.1 Lite

Code modules

- VHDL, Verilog, Schematic or IP Blocks

Design test benches for code.

- VHDL or Verilog

Logic Synthesis

Simulate

- Model Sim

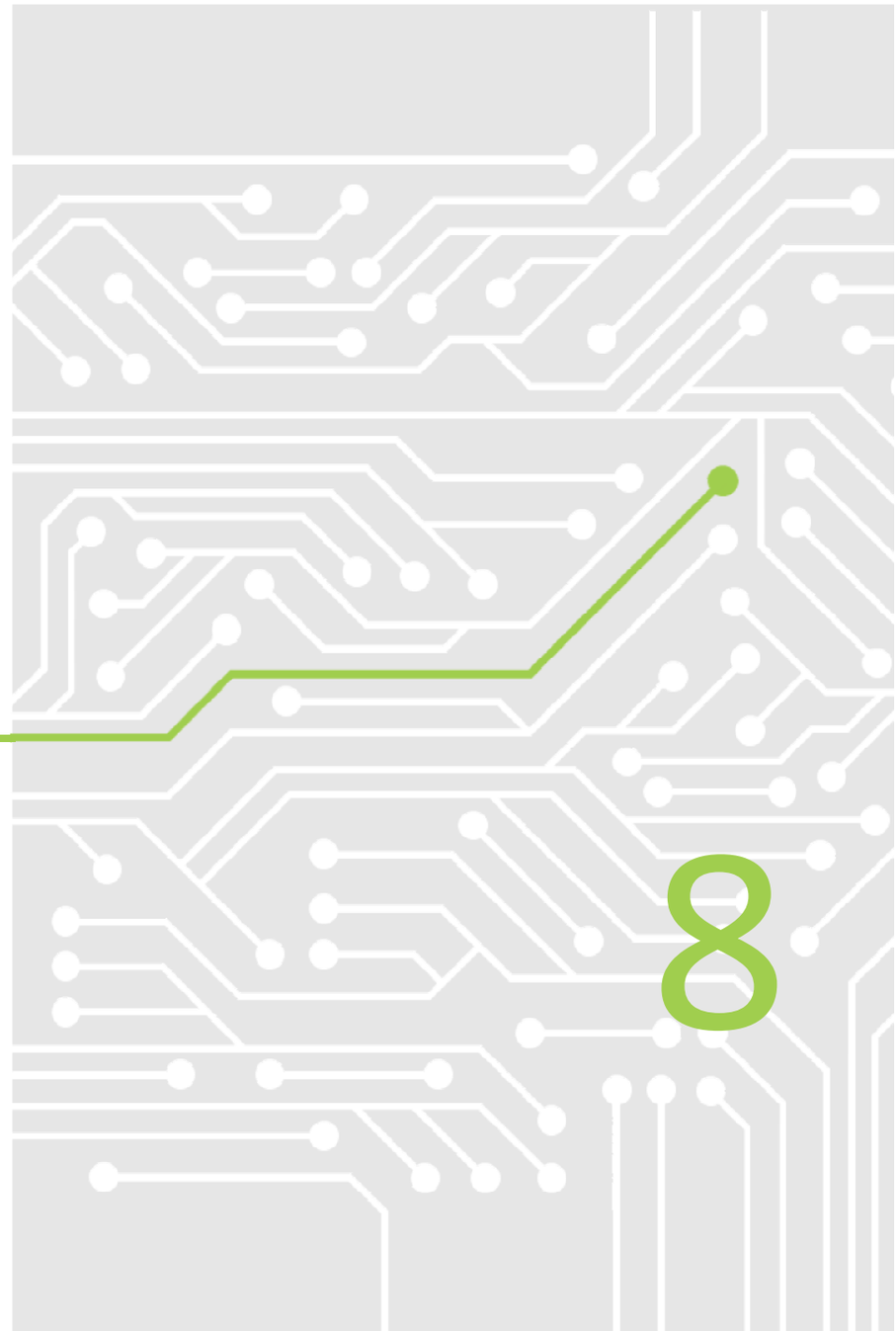
Place and route

Timing Analysis

Download

Lime microsystems

Using the SDR Well



Tips on Using LimeSDR Well

Always start from a working .ini file.

Try out settings using FFT Viewer and known waveforms.

Make frequency plan of SDR clocks

- Signal Bandwidth
- Adjacent Channel Issues
- ADC/DAC Rates → CLKGEN
- Interface Rate→Dec/Int Factors

Set up for best dynamic range

- Use sufficient PGA gain for ADC to just see noise floor.
- Reduce LNA gain until noise floor just increases.

RF Match TX and RX for best output power and sensitivity.

- Best NF match usually a little away from best S11 match.

Typical settings for 900MHz 20MHz BW

- LNA = MaxGain-9
- TIA = MaxGain or -3dB
- PGA = -3dB
- CLKGEN ~ 250MHz

Make use of the automatic calibration tools in the MCU

- Tx IQ and LO leakage, filter calibration
- Rx IQ and DC offset, filter calibration