SID++

“Like RISC-V but better in every way”
-Rob Coons Probably (Definitely) 2023

Sid-ple code

RESTRICTIONS

- C code
- Single input, single output
- No multiplication or division

Describe our processor

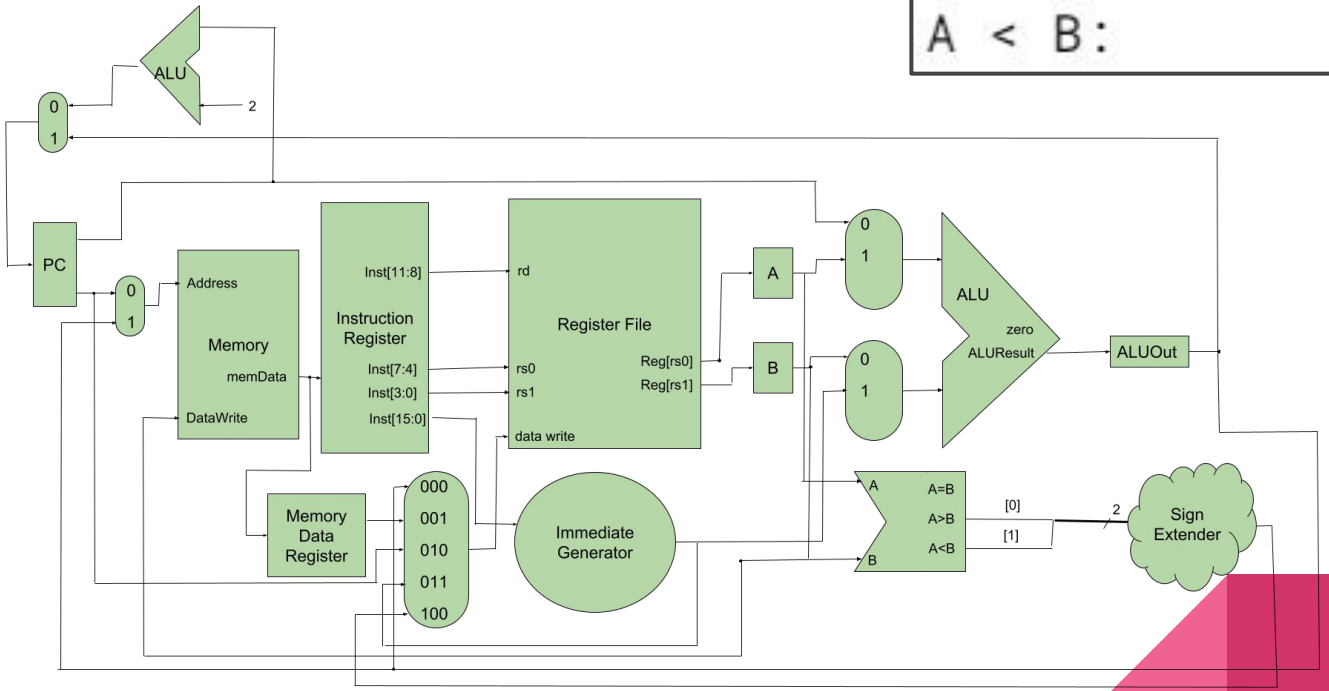
- RISC-V inspired
- Focus on maximizing immediates
  - B type - Can reach every possible instruction
  - I type - 8 bit immediate
- Multi(ish) cycle

Unique aspects of design

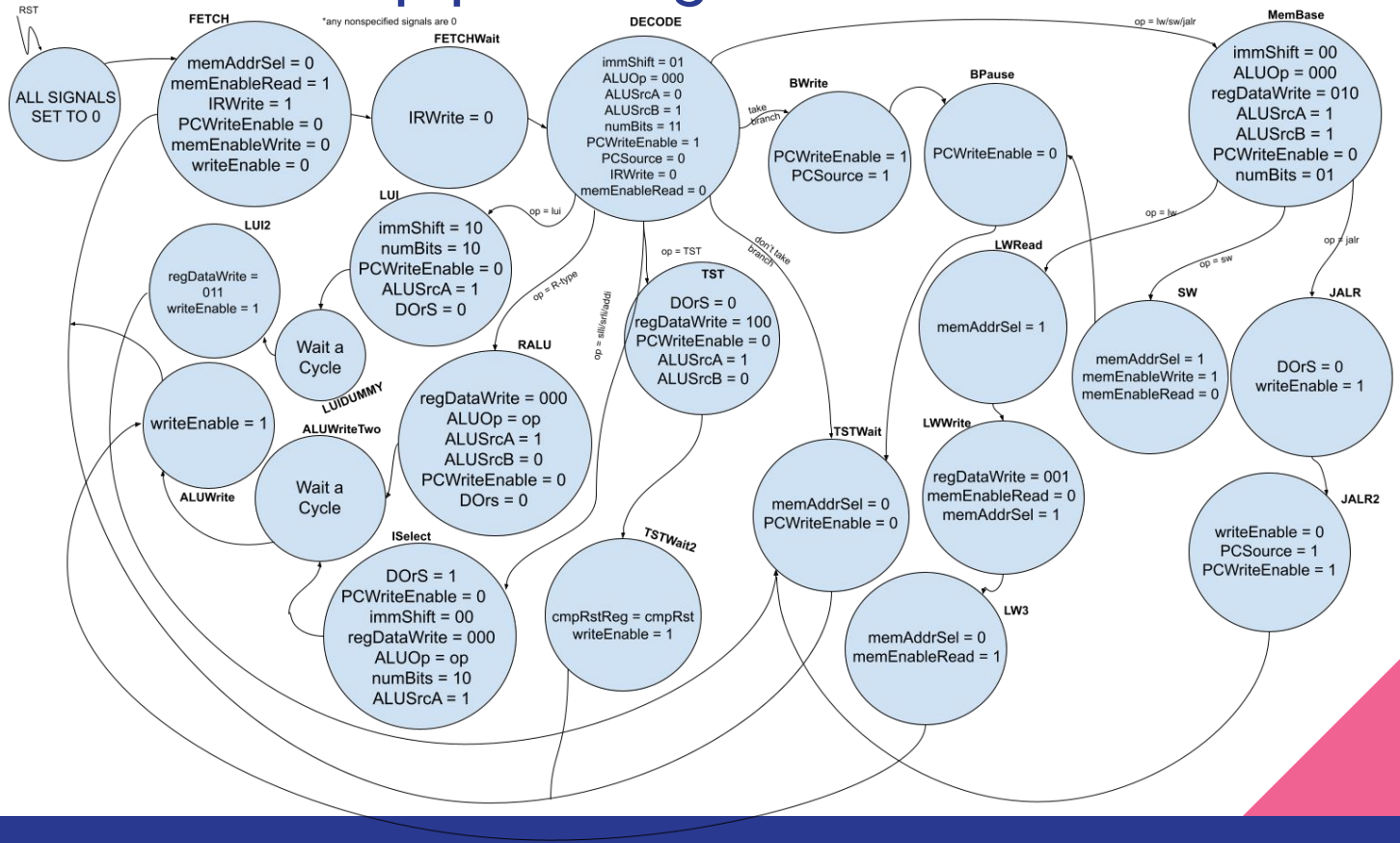
- TST then Branch
  - Comparator
- Allows instructions between
- Half pipe-lining

Datapath - Compare Unit

A = B:	00
A > B:	01
A < B:	10



FSM- Half pipe-lining



What we would do differently

- Keep largely the same
- Challenge ourselves
  - The dream of pipelining (partially realized)
  - Multi-Core
  - Run relPrime visually on FPGA

What went well/poorly

- Initial single cycle implementation
- Unfortunate timing
- Meeting 1-2+ times a week between milestones
- Initial language design

Unique Problems

- jalr/jal
  - No PC relative jumping, only branching
  - Extra instructions between test or loading the address into a register
- comparator amount of bits
  - Registers are 16 bit, but the comparator outputs 2 bits
- jalr -> lui
  - Jumping to lui doesn’t work, need a no-op

Data

Total Storage = 128 Bytes

Total Logic Elements = 1,084

Total Memory Bits = 524,288

Total Registers = 555

Total Instructions = 71,565

Total Cycles = 378,443

Average CPI = 5.288

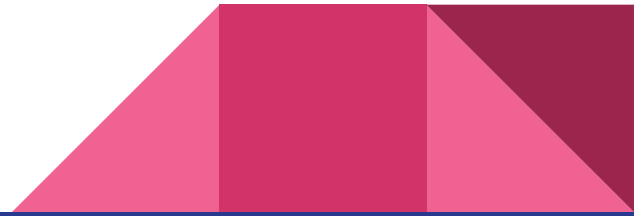
Cycle Time = 10.5 nS

Clock Frequency = 94.8 MHz

Flow Status	Successful - Mon May 22 19:14:37 2023
Quartus Prime Version	18.1.0 Build 625 09/12/2018 SJ Lite Edition
Revision Name	processorDatapath
Top-level Entity Name	CPU
Family	Cyclone IV E
Total logic elements	1,084 / 22,320 (5 %)
Total registers	555
Total pins	34 / 80 (43 %)
Total virtual pins	0
Total memory bits	524,288 / 608,256 (86 %)
Embedded Multiplier 9-bit elements	0 / 132 (0 %)
Total PLLs	0 / 4 (0 %)
Device	EP4CE22E22C6
Timing Models	Final

	Fmax	Restricted Fmax	Clock Name	Note
1	94.8 MHz	94.8 MHz	CLK	
2	159.54 MHz	159.54 MHz	controlUnit:UTT|current_state.MemBase	
3	159.69 MHz	159.69 MHz	controlUnit:UTT|current_state.DECODE	
4	170.18 MHz	170.18 MHz	ALUOpReg[0]	
5	621.12 MHz	621.12 MHz	controlUnit:UTT|current_state.FETCH	

Demo - start with code, do crazy add sids here



Sid Code Time

QUESTIONS