Page Map Arithmetic

- (v+p) bits in virtual address
- (m+p) bits in physical address
- 2^v # of virtual pages
- 2^m # of physical pages
- 2^p bytes per physical page
- 2^{m+p} bytes in physical memory
- (m+3) *2^v bits in the page table:
- typical page size: 4~16KB
- typical (v+p): 32 bit, 64 bit
- typical (m+p): 30~40 bits (1GB~1TB)

Example:Page Map Arithmetic

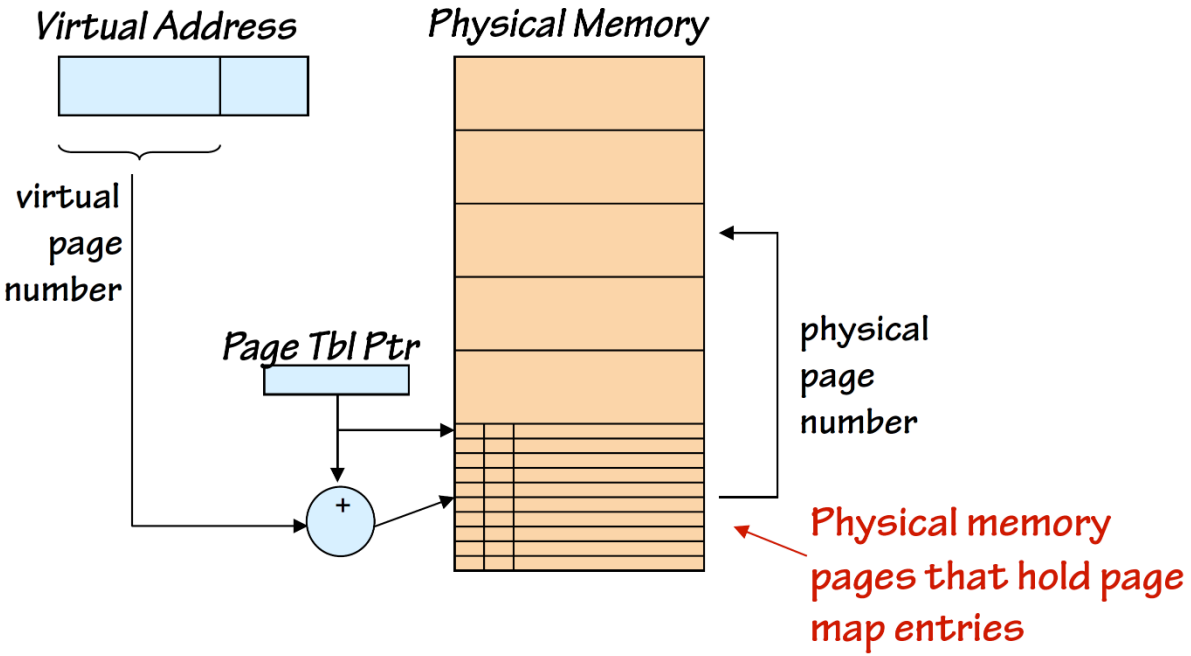
- Suppose:
  - 32-bit virtual address
  - Page size: 4KB
    - 2^{12}
  - RAM max: 1GB
    - 2^{30}
- Then:
  - # Physical pages: 2^{18} 256K
  - # Virtual pages: 2^{20}
  - # PTE (page table entries): 2^{20}
  - # bits in page table: $(18+3)*2^{20}$
- Use SRAM for page table???
  - 21Mbit ➔ 3MB

Memory Technologies

	Capacity	Latency	Cost/GB
Registers	1000s of bits	20 ps	$$$$
SRAM	~10KB-10MB	1-10 ns	~$1000
DRAM	~10GB	80 us	~10
Hard disk	~1TB	10 ms	~0.10

Where to store the page table?

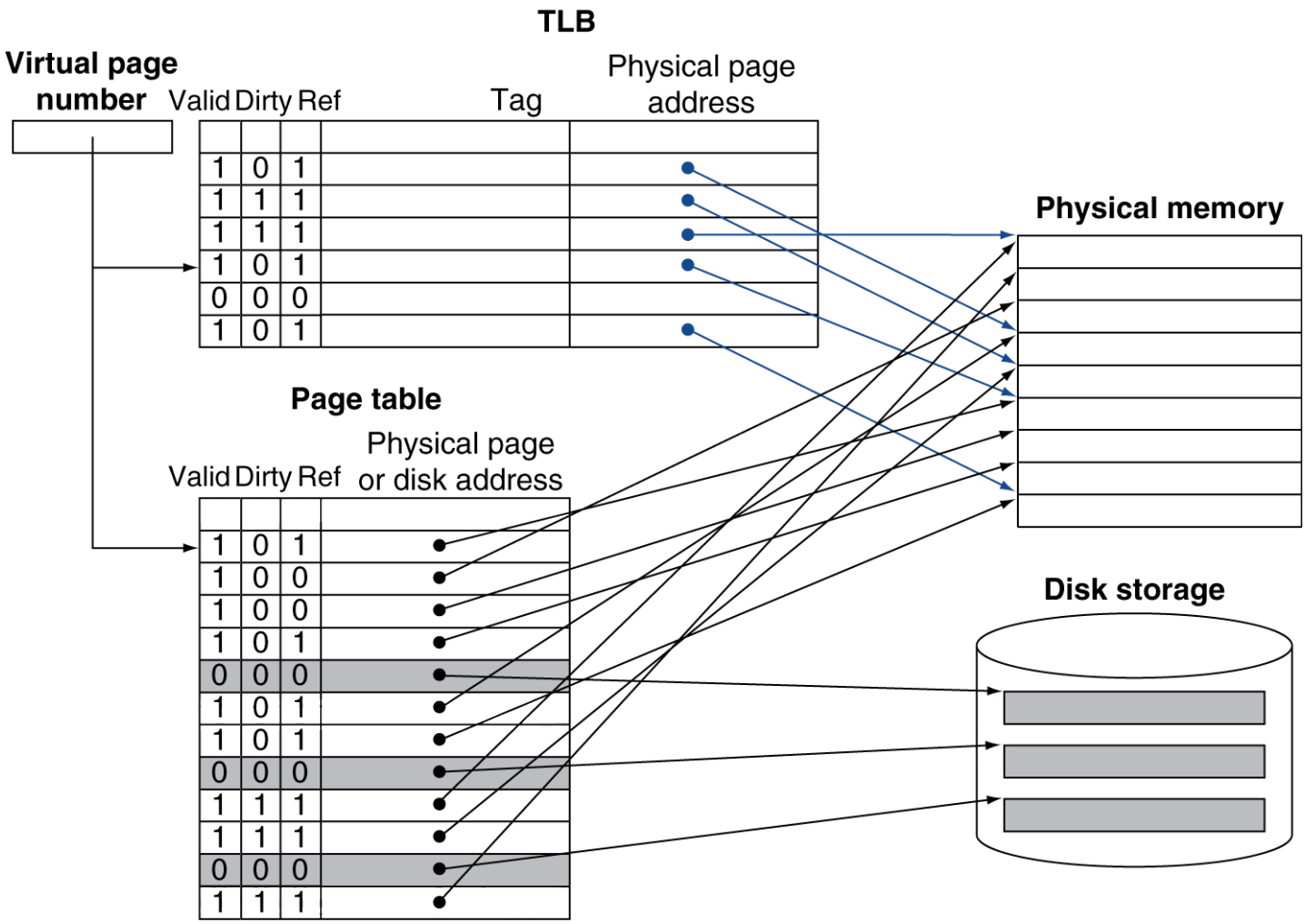
- Small page tables can choose dedicated SRAM
- But expensive for big ones
- Solution: move page table to main memory
- Problem: each memory reference now takes 2 accesses



Speed up Translation with a TLB

- Problem: 2 accesses for each memory reference
- Solution: Cache the page table entries
- Translation Look-aside Buffer (TLB)
  - Small full/set-associative hardware cache in MMU
  - lookup by VPN(virtual page number.)

Fast Translation Using a TLB



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  - 32-bit virtual address
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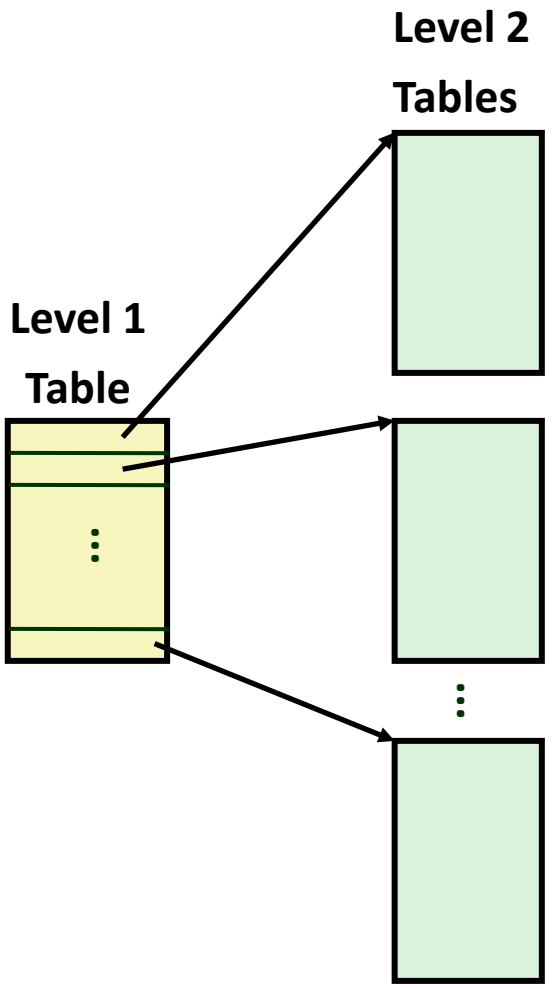
- Then:
  - # Virtual pages: 2^{20}
  - # PTE (page table entries): 2^{20}
- How about 64 bit virtual address?

Multi-Level Page Tables

- Problem: 2^{20} virtual pages not necessary all valid or used, but 2^{20} PTEs always in main memory
- Common solution: multi-level page table
- Example: 2-level page table

Multi-Level Page Tables

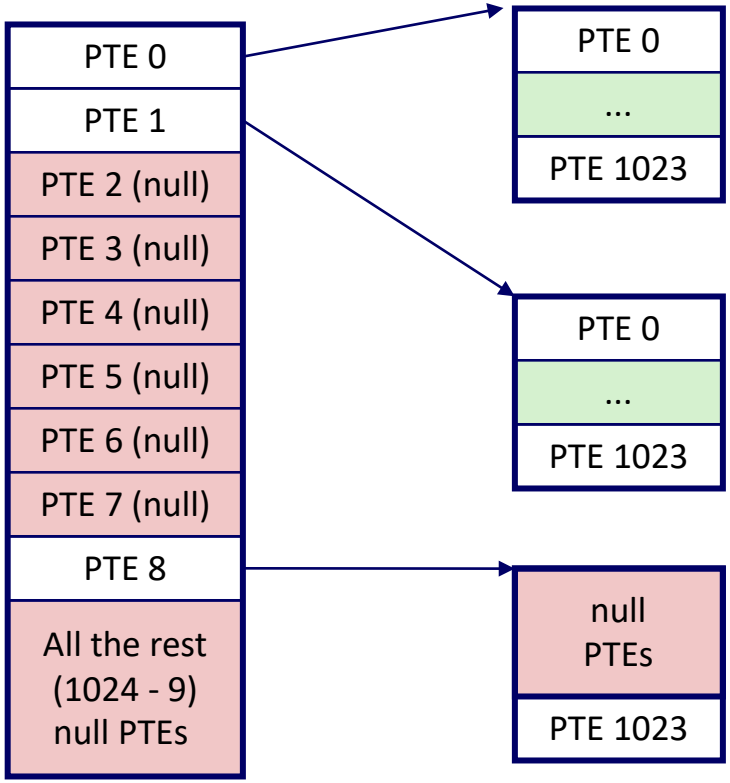
- Example: 2-level page table
  - Level 1 table: each PTE points to a Level 2 of page table
  - Level 2 table: each PTE provides the translation to physical address



A Two-Level Page Table Hierarchy

Level 1
page table
Outer table: 1024 PTEs

Level 2
page tables
Inner table: 1024PTEs each



Now, how about 64 bit addresses?
Multilevel Page Tables