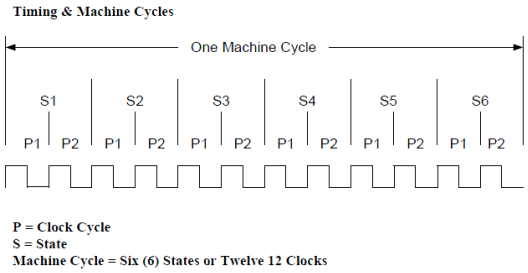
For the **8051** (12 clock cycles version for CG3207) that you are required to emulate, two clock cycles are required to perform a single discrete operation, where 1 machine cycle consists of 12 clock cycles and 6 states.



A state is the basic time interval to either:

(1) Fetch an op-code byte (In S1 or S4, the op-code is latched onto the IR)
(2) Decode an op-code byte (The decoder must determine how big the instruction is)
(3) Execute an op-code or write a data byte

Normally, two program fetches are generated during one machine cycle (in S1 or S4). The extra fetch (S4) is discarded if the instruction being executed doesn't need more code bytes. Execution is completed at the end of S6.