Additional Tutorial Questions for Chapters 2 to 4

Q1.
Is the following statement true or false?

```
create_clock_ -period 10  [get_ports CLK1]
set_input_delay -max 2.3 -clock CLK1 [get_ports IN1]
```

specify the input arrival time of 2.3 time units for port IN1 on a combinational design.

(a) True; (b) False.

Q2.
What does the following primitive define?

```
primitive ex (c, b, a);
        output c;
        reg c;
        input a, b;
        table
                a b : c ;
                0 0 : 0 ;
                0 1 : 1 ;
                1 1 : 1 ;
                1 0 : 1 ;
        endtable;
endprimitive
```

(a) A toggle flip-flop.
(b) An AND gate.
(c) A XOR gate.
(d) An OR gate
(e) None of the above.

Q3.
Is the following statement true or false?

```
create_clock -period 20 [get_ports CLK1]
set_output_delay -min -1.7 –clock CLK1 [all_outputs]
```

The above commands set the setup time of 1.7 time units relative to the rising edge of "CLK1" for all output ports in the design.

(a) True; (b) False.

Q4.
Is the following statement true or false?

set_input_delay specifies the input arrival time of a signal on pins or input ports relative to a clock signal.

(a) True;(b) False.

Q5.
Is the following statement true or false?
For a register, the input data can be changed immediately at the input pin after the active clock transition.

(a) True;(b) False.

Q6.
Is the following statement true or false?
Static timing analysis determines whether a circuit meets timing constraints without having to simulate clock cycles.

(a) True;(b) False.

Q7.
Is the following statement true or false?
The design environment describes the conditions that the circuit will operate within.
(a) True;(b) False.

Q8.
Is the following statement true or false?
The underscore character (_) is legal anywhere in an identifier.

(a) True; (b) False.

Q9.
Is the following statement true or false?
Parameter is defined by Verilog as a type of variable declared within the module structure.

(a) True; (b) False.

Q10.
Is the following statement true or false?
The procedure must contain the key words "begin" and "end".

(a) True; (b) False.

Q11.
Is the following statement true or false?
One of the different between "always" and "initial" is that always block can repeat based on control/sensitivity list but initial block executes once.
(a) True; (b) False.

Q12.

Is the following statement true or false?

In the procedural assignments, LHS can be nets.

(a) True; (b) False.

Q13.

Is the following statement true or false?

A Scalar "wire" is the default data type in Verilog.

(a) True; (b) False.

Q14.

Is the following statement true or false?

Synthesis tool produces gate-level code or circuit net lists.

(a) True; (b) False.

Q14.

What best defines a "cell-based ASIC"?

(a) An FPGA that has Configurable Logic Block cells.
(b) A chip design produced using a set of predesigned logic-gate cells.
(c) A gate array with predefined transistor cells.