NATIONAL UNIVERSITY OF SINGAPORE

EXAMINATION FOR

(Semester II: 2010/2011)

CG2007/EE2007E – MICROPROCESSOR SYSTEMS

April/May 2011 - Time Allowed: 2 Hours

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **FOUR** (4) questions and comprises **NINE** (9) printed pages. Selected information from the necessary data sheets is provided at the end of each question.

2. Answer all **FOUR** (4) questions. All questions carry equal marks.

3. This is a CLOSED BOOK examination.

4. Programmable calculators are NOT allowed.

SECTION A.
Q.1

(a)

(i) In order to access every byte location in a 2MB RAM memory, the minimum number of address lines required is _____.

(ii) To access 16 words starting from an odd address location followed by accessing 8 bytes from another odd address location, 8086 consumes _____ bus cycles.

(iii) In the micro-architecture of 8086, the execution unit is responsible for fetching the required datum and instructions from memory. (True/False)? _____

(iv) The number of bytes allocated when you declare "MYSPACE DB 20DUP(1,2,4DUP(?,0,0,1),6))" is _____.

(v) Assume DS = 1120, SI = 2498 and AX = 17FE. The contents of memory location 13698H after the execution of "MOV [SI], AX" is 17. (True/False)? _____

(10 marks)

(Q.1 continues on Page 3)

(b) Consider the following two multiword numbers.

DATA1 = 1123456789011111H and DATA2 = 1111109876543211H

(i) Use DQ (quad words) directive to define the above multiword numbers clearly in your data segment. Also define a variable DATA3 to hold your result.

(5 Marks)

(ii) Write an assembly code that adds the above multiword numbers and saves the result in DATA3. Write only the part that captures your logic and you need not use any interrupts. You need not write the code as a Procedure.

Hint: ADC instruction adds the contents of source register, destination register and the CF contents.

(10 Marks)

Q.2

(a)

(i) The DD directive is used to allocate memory locations that are _____ bytes.

(ii) A word and byte data are stored in consecutive locations. The time taken to access the word data first and then the byte data is longer than the time taken to access the byte data first and then the word data by the 8086 CPU. Choose one of the following. (a) True (b) False (c) Does not matter (d) Inadequate information

(iii) A byte data is received from a communication port whose address is 89H. How do you read the data byte from that port and check if its bit 1 is a '1'?

(iv) Let DATA1 = 25H and DATA2 be defined as "DATA2 DB ?". Then to copy the DATA1 to DATA2, one of the ways suggested is "MOV DATA2, DATA1". (True/False)? _____

(v) Let CF = 0 and CX = FFFF. Then an instruction INC CX will modify the CF to _____.

(10 Marks)

(b) Write a simple code sequence to determine the largest number from an unordered array of sixteen 8-bit numbers continuously stored in memory locations starting at offset 0500H in the segment 2000H. Wherever necessary provide comments to explain the logic in your code.

Hint: You need not define the data segment explicitly and you may start your code by initializing the DS register with 2000H.

(15 Marks)

SECTION B.

Q.3

(a)

(i) A computer specification says that it has 1GB main memory. The type of main memory is _____ (a) SRAM (b) DRAM (c) Flash Memory (d) Hard Disk.

(ii) To access a register in an I/O device, a microprocessor will use all the bits of its address bus to generate a chip select signal to choose the device, then it uses only the lower portion of the address bus to generate the offset of the register in the device. Choose one of the following: (a) True (b) False (c) Insufficient information (d) Partly true _____.

(iii) We can use bits 0-3 in port B of an 8255 chip to control 4 LED lights, and use bits 4-7 in port B of an 8255 chip to read 4 sensor signals. The 8255 chip is configured in the I/O mode. Choose one of the following: (a) True (b) False (c) Insufficient information (d) Partly true _____.

(iv) What is the BHE\ value when an 8086 processor executes the following operation? _____.

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MOV AX, 2896H
MOV [4000H], AX
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(v) Datum stored in the odd bank memory chip of an 8086 processor system will use the lower 8 bits of the 8086 data bus. Choose one of the following: (a) True (b) False (c) Insufficient information (d) Partly true _____.

(10 marks)

(Q.3 continues on Page 6)

(b)

We are building a small 8086 microprocessor system. The system uses the following memory chips and peripherals: two 8K*8 ROM chips and two 8K*8 RAM chips.

(i) Draw the memory address maps for all the memory chips used in the system.

(7 marks)

(ii) Based on the address maps from your answer in Q.3b(i), find out the logic function of the chip select signal CS\ for each of the memory chips, respectively.

(8 marks)

Q.4

(a)

(i) The Interrupt Request Register (IRR) has the value 0000 0101, the Interrupt Mask Register (IMR) is configured with the value 0000 0001, and the ICW2 register is configured with the value of 0001 0000. Determine the interrupt type number _____ that will be given to the granted I/O device.

(ii) Interrupt controller 8259 chips use _____ to pass the interrupt type number information of hardware interrupts to a processor.

(iii) Modern processors have used super-pipelining to achieve low power. Choose one of the following: (a) True (b) False (c) Insufficient information (d) Partly true _____.

(iv) A 4-way set associative cache will have a _____% probability for a cache block in a cache set not to be replaced in a cache replacement operation.

(v) An interrupt mask will be used if a microprocessor does not want to be disturbed. Choose one of the following: (a) True (b) False (c) Insufficient information (d) Partly true _____.

(10 marks)

(Q.4 continues on Page 8)

(b)

(i) Find the port addresses for the command register and the mode set register of DMA Controller 8237 if the chip select signal CS\ of 8237 is activated by A7-A4= 1010.

(3 marks)

(ii) We want to move 1KB of data from memory address 3000H:5000H to an I/O device. Determine the configuration values for the command register and the mode set register. The bit definitions for 8237 registers are shown in Figure 4.b1- Figure 4.b2.

(8 marks)

(iii) Write a program segment for 8237 to move the data as specified in Q.4b(ii) by using the port addresses calculated in Q.4b(i).

(4 marks)

(Q.4 is continued on Page 9)

D7	D6	D5	D4	D3	D2	D1	D0

- D0 selects memory-to-memory mode. 1: enabled. 0: disable.
- D1=1, channel 0 address hold is enabled. D1= 0 to disable.
- If D2=1, the DMA controller is off. D2=0 the DMA controller is on.
- D3 determines whether a DMA cycle contains two (compressed) or four (normal) clock cycles. D3=1 for compressed and D3=0 for normal.
- D4=1 for rotating priority and D4=0 for fixed priority.
- D5 is used in normal timing to extend the write pulse. D5=1 is the extended write selection, while D5=0 is late write selection.
- D7-D6 program the polarities of the DREQ inputs and DACK outputs.
  D6=0: DREQ sense active high, D6=1: DREQ sense active low
  D7=0: DACK sense active low, D7=1: DACK sense active high

Figure 4.b1 The bit definitions for the 8237 Command Register.

D7	D6	D5	D4	D3	D2	D1	D0

- D1-D0 select the channel to operate on.
  00 = channel 0 select, 01= channel 1 select, 10 = channel 2 select and 11 = channel 3 select
- D3-D2 select the operation. 00 = verify transfer, 01 = write transfer, 10 = Read transfer
- D4 selects auto-initialization. D4=1 enable autoinitialization, D4=0 disable.
- D5 selects address increment/decrement mode. D5=1 decrement, D5=0 increment
- D7-D6 select modes of operation.
  00: Demand mode select (transfer data until the DREO becomes inactive)
  01 Single mode select (release HOLD after each byte data transfer)
  10 Block mode select (automatically transfer the number of bytes in the count register)
  11 Cascade mode select (more than one 8237 is present in a system)

Figure 4.b2 The bit definitions for the 8237 Mode Set Register.

END OF PAPER