CG 2007 Microprocessor Systems
Lecture 10

Direct Memory Access

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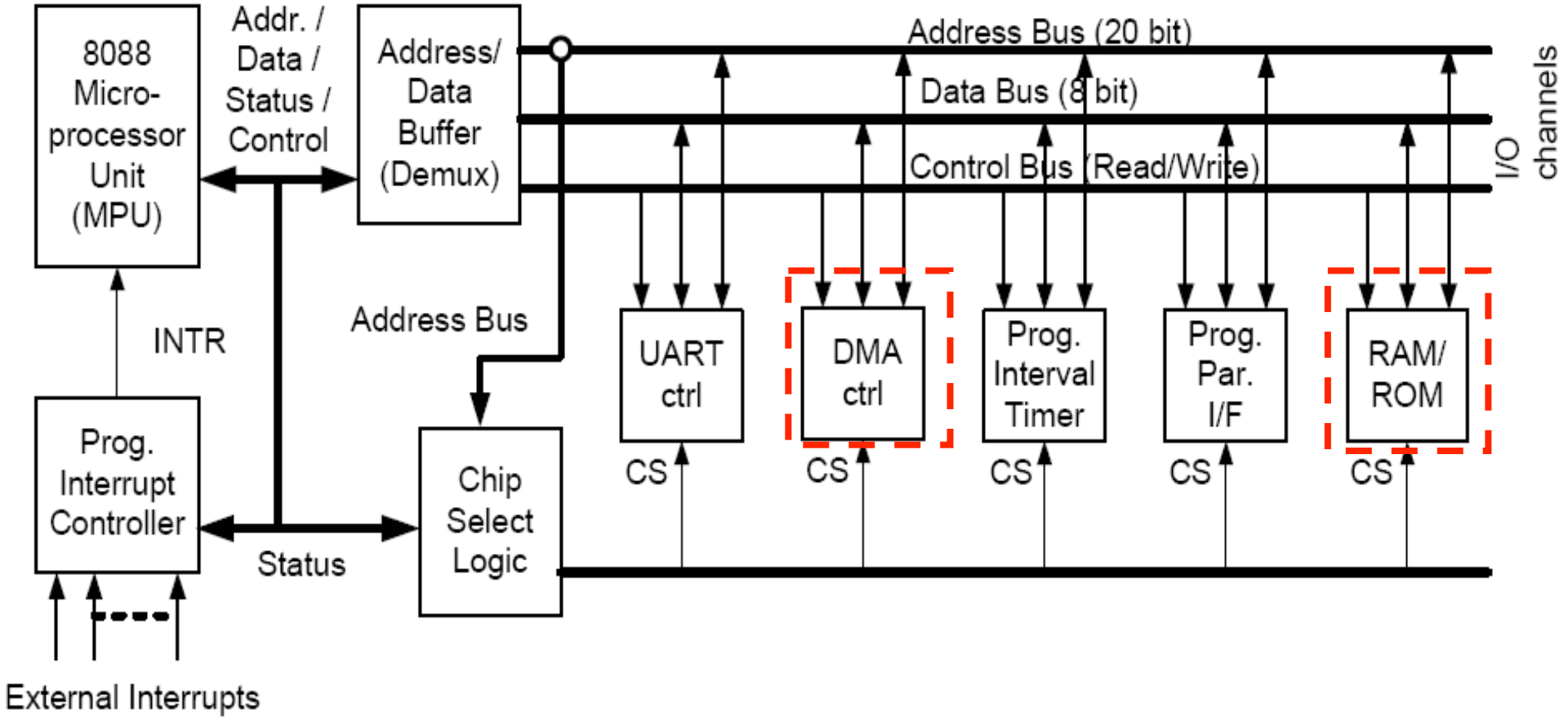
Lecture 10: Objectives and Outline

- **Objectives**
  - Understand Direct Memory Access (DMA) concepts and develop DMA applications

- **Outline**
  - DMA Concepts
  - DMA System
  - DMA Controller 8237

Simplified System Architecture of an IBM Compatible PC



Outline: Direct Memory Access

- DMA Concepts
- Intel 8086/8088 DMA System
- DMA Controller 8237

Transfer Bulk Data Efficiently with DMA

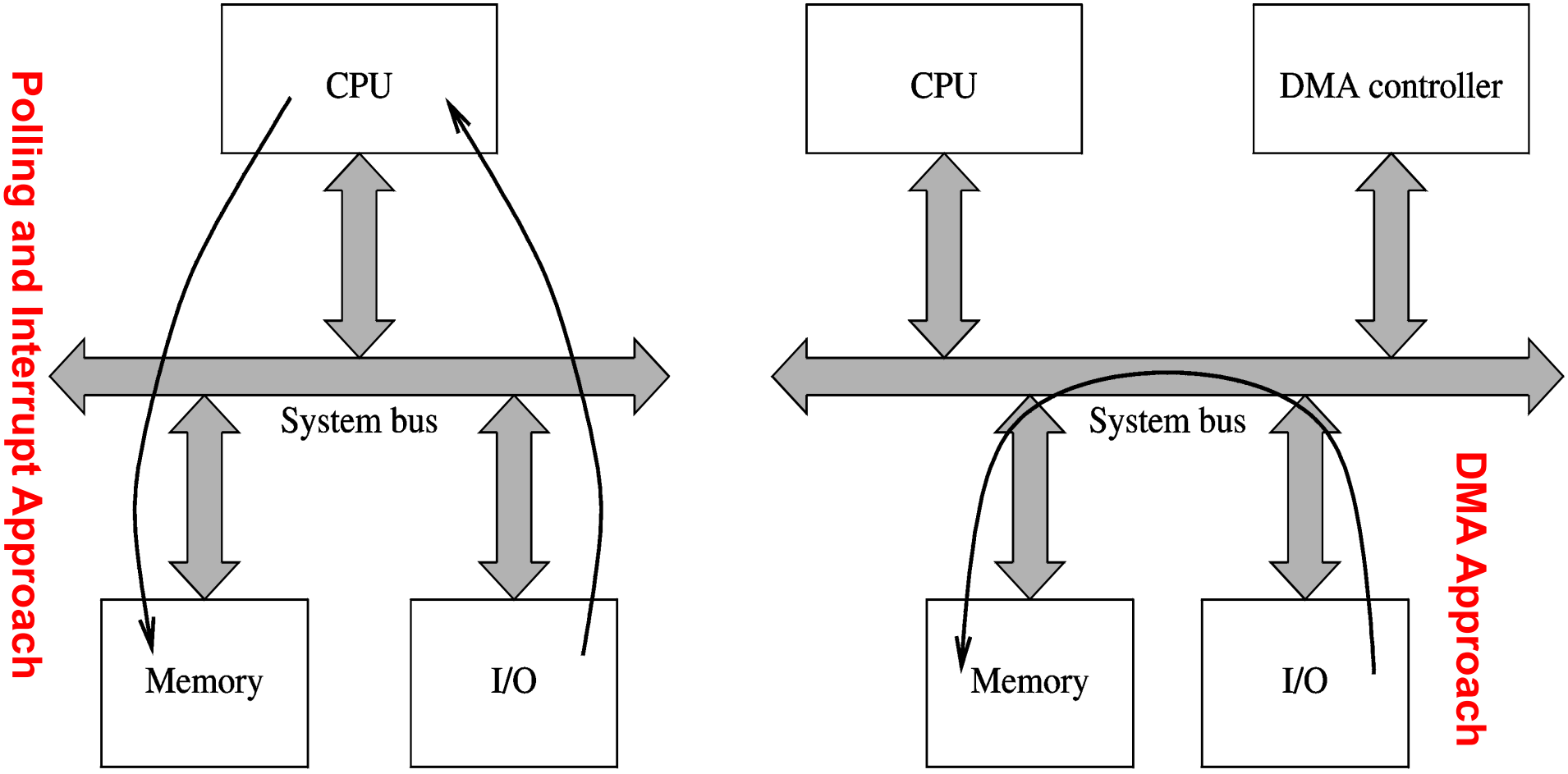
- From time to time, we need to transfer bulk data between memory and I/O devices, such as floppy disk or CRT display.

- It wastes a lot of time for the CPU just transfer data from source to destination using polling or interrupt driven data transfer.

- The alternative way of transferring bulk data is the direct memory access (DMA) technique, in which the data is transferred directly between memory and I/O devices under the control of a DMA controller

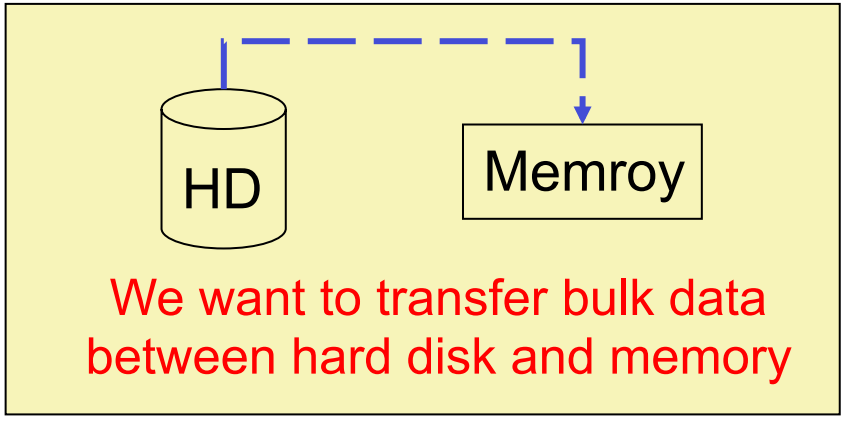
- A DMA controller is designed to complete the bulk data transfer much faster than the CPU.

DMA: Direct Transfer Between I/O and Memory

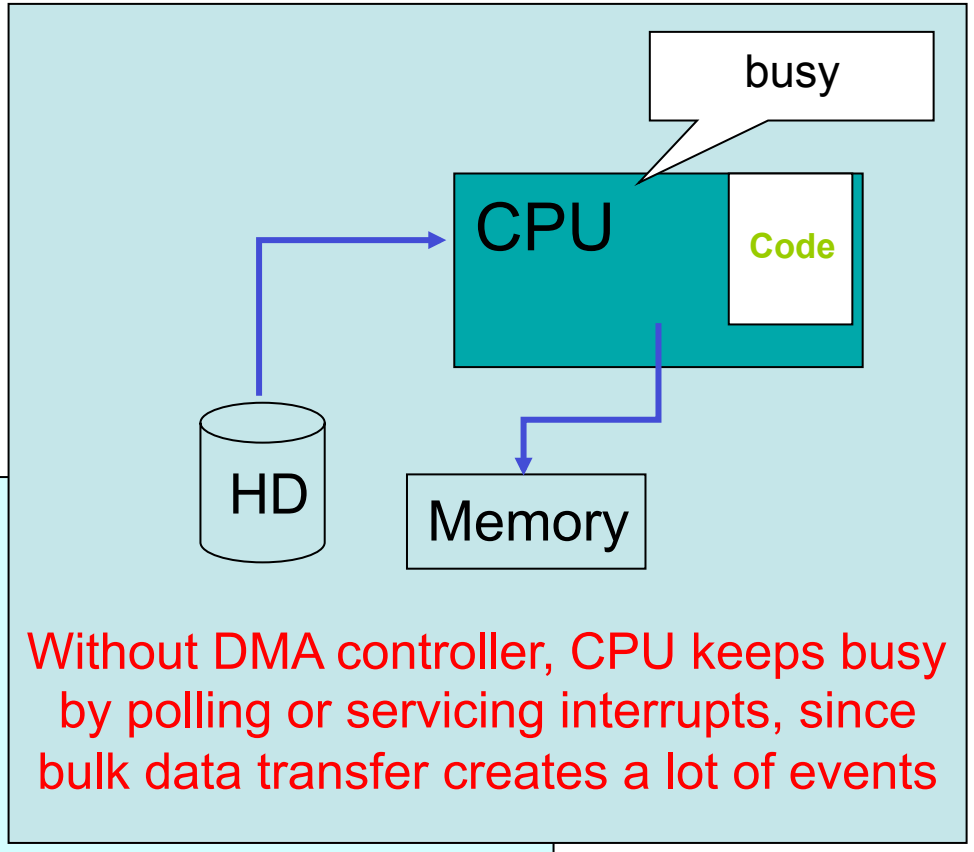


Polling and interrupt based data transfers need CPU to take part in, while DMA transfer does not!

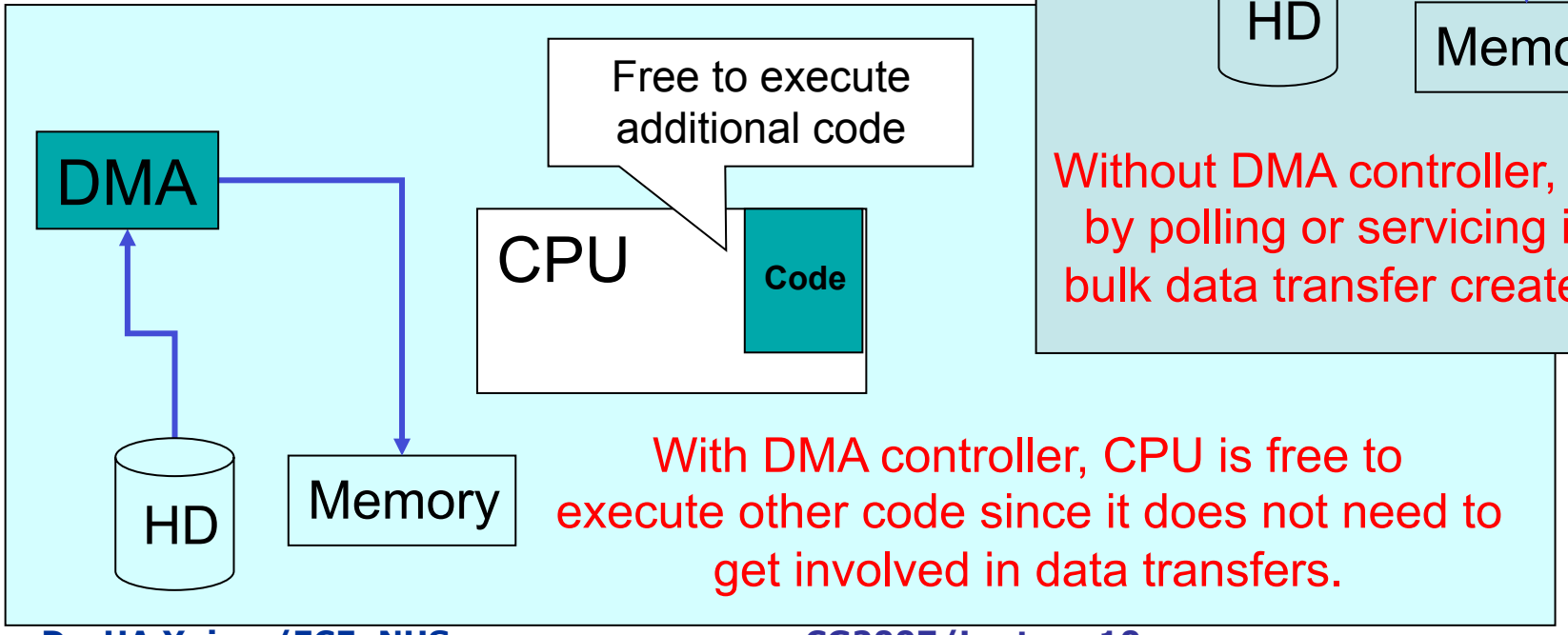
DMA Transfer Frees CPU



We want to transfer bulk data between hard disk and memory



Without DMA controller, CPU keeps busy by polling or servicing interrupts, since bulk data transfer creates a lot of events



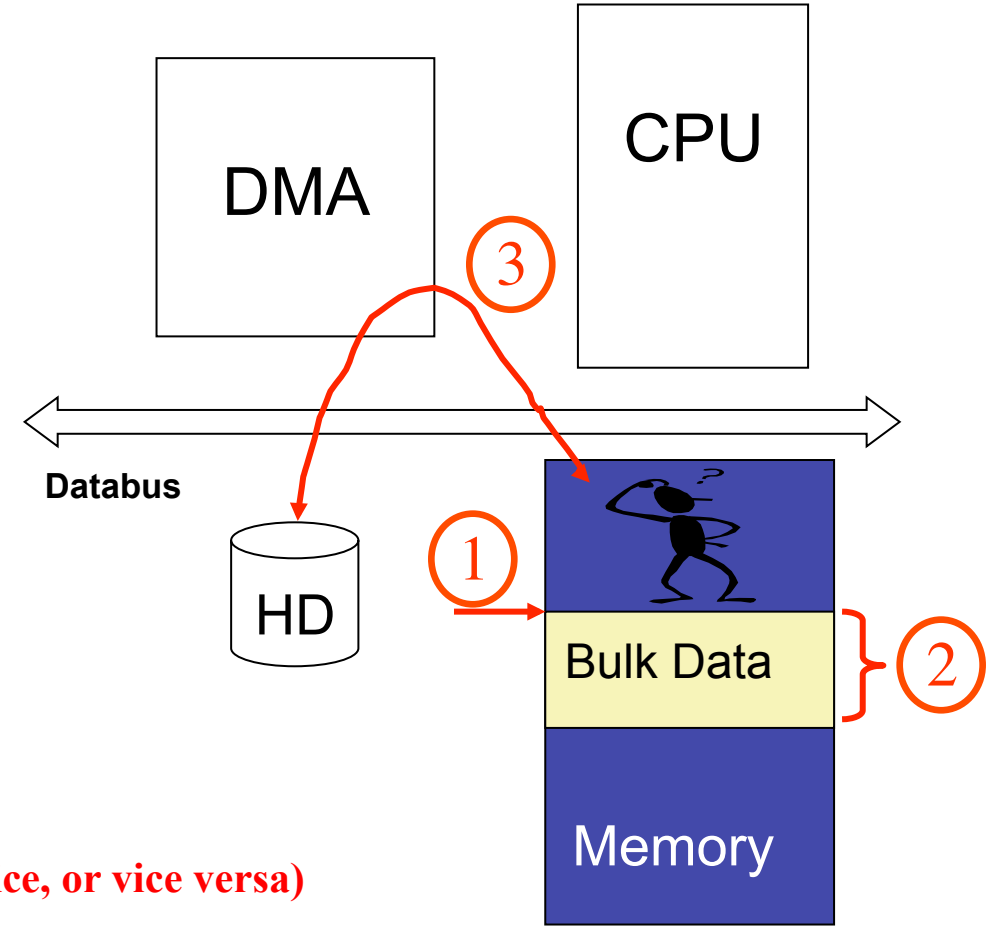
With DMA controller, CPU is free to execute other code since it does not need to get involved in data transfers.

Comparison of the Three Ways of Data Transfer

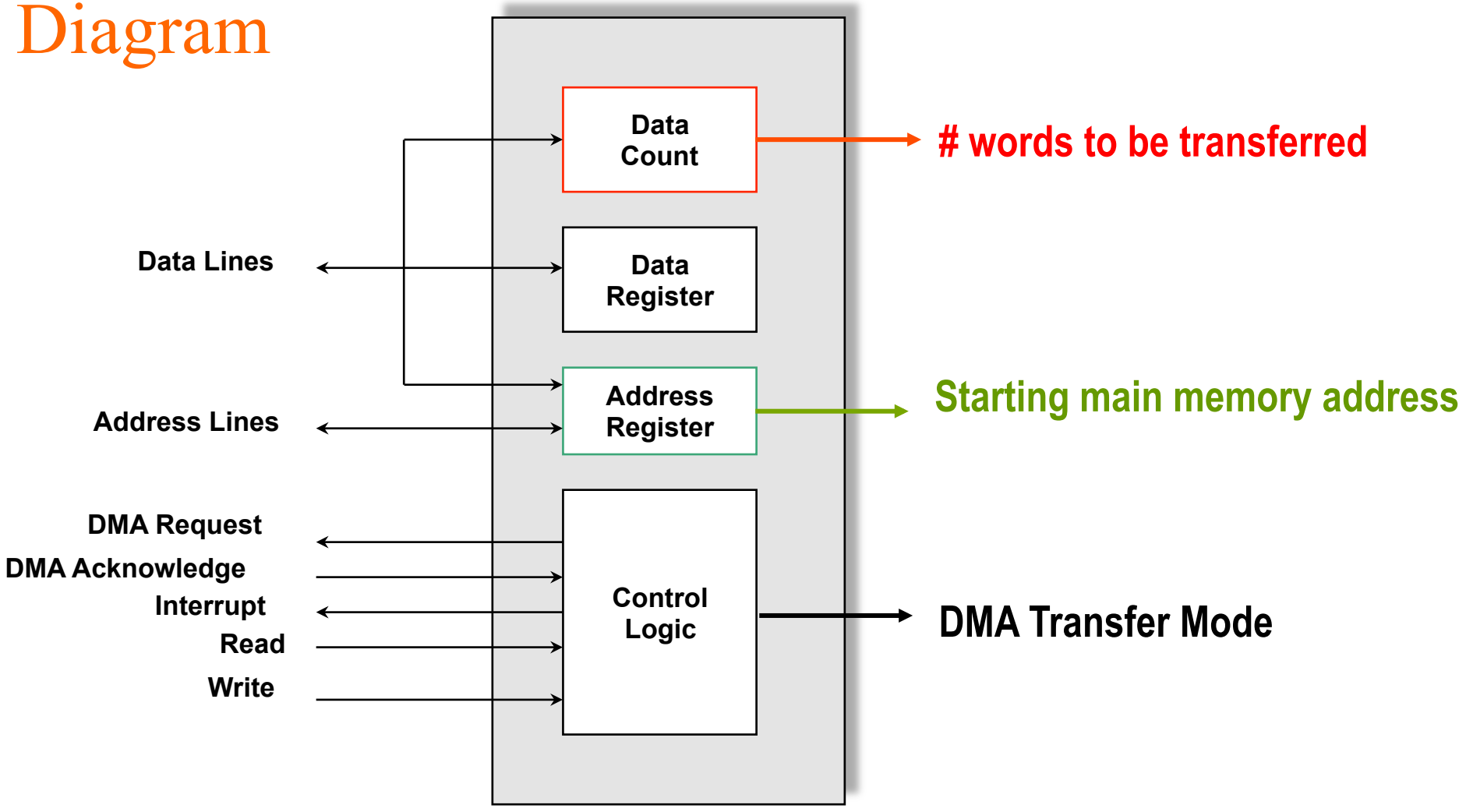
- **Polling Approach**
  - Processor polls I/O device for data
  - Keeps processor busy and wastes resources
- **Interrupt Approach**
  - I/O interrupts processor
  - Processor transfers data from/to memory
  - Processor is only busy when there is interrupt
  - Not good when interrupts are quite frequent in bulk data transfer
- **DMA Approach**
  - DMA Controller transfers data from/to memory
  - Controller only interrupts processor when transfer finishes
  - Good in bulk data transfer

DMA Controller

- **DMA transfer is implemented using a DMA controller**
  - DMA controller
    - **Acts as slave to processor**
    - **Receives instructions from processor**
    - **Example: Reading from an I/O device**
  - Processor gives details to the DMA controller
    1. **Main memory starting address**
    2. **Number of bytes to transfer**
    3. **Transfer mode (memory → I/O device, or vice versa)**



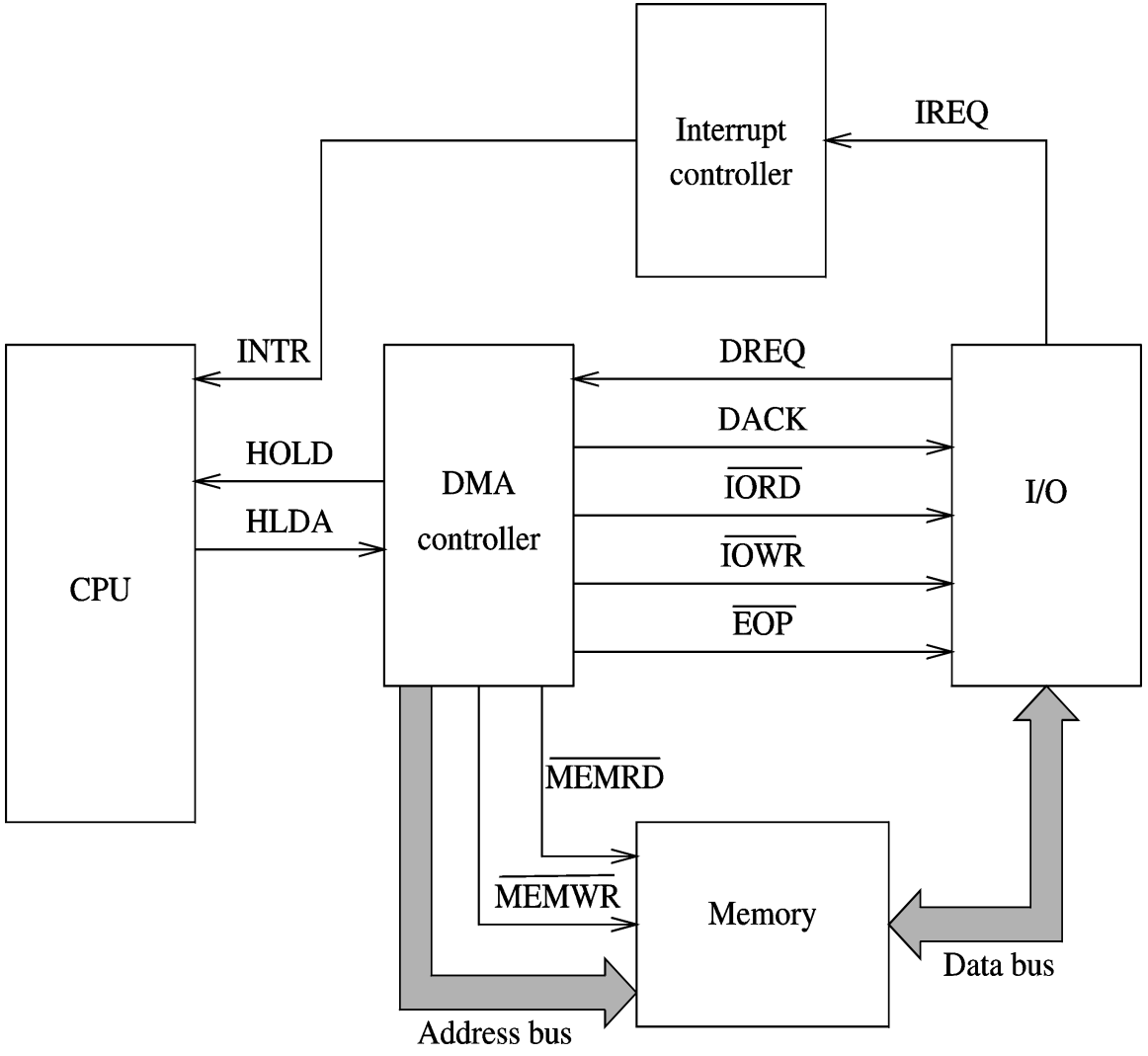
Typical DMA Controller Block Diagram



Outline: Direct Memory Access

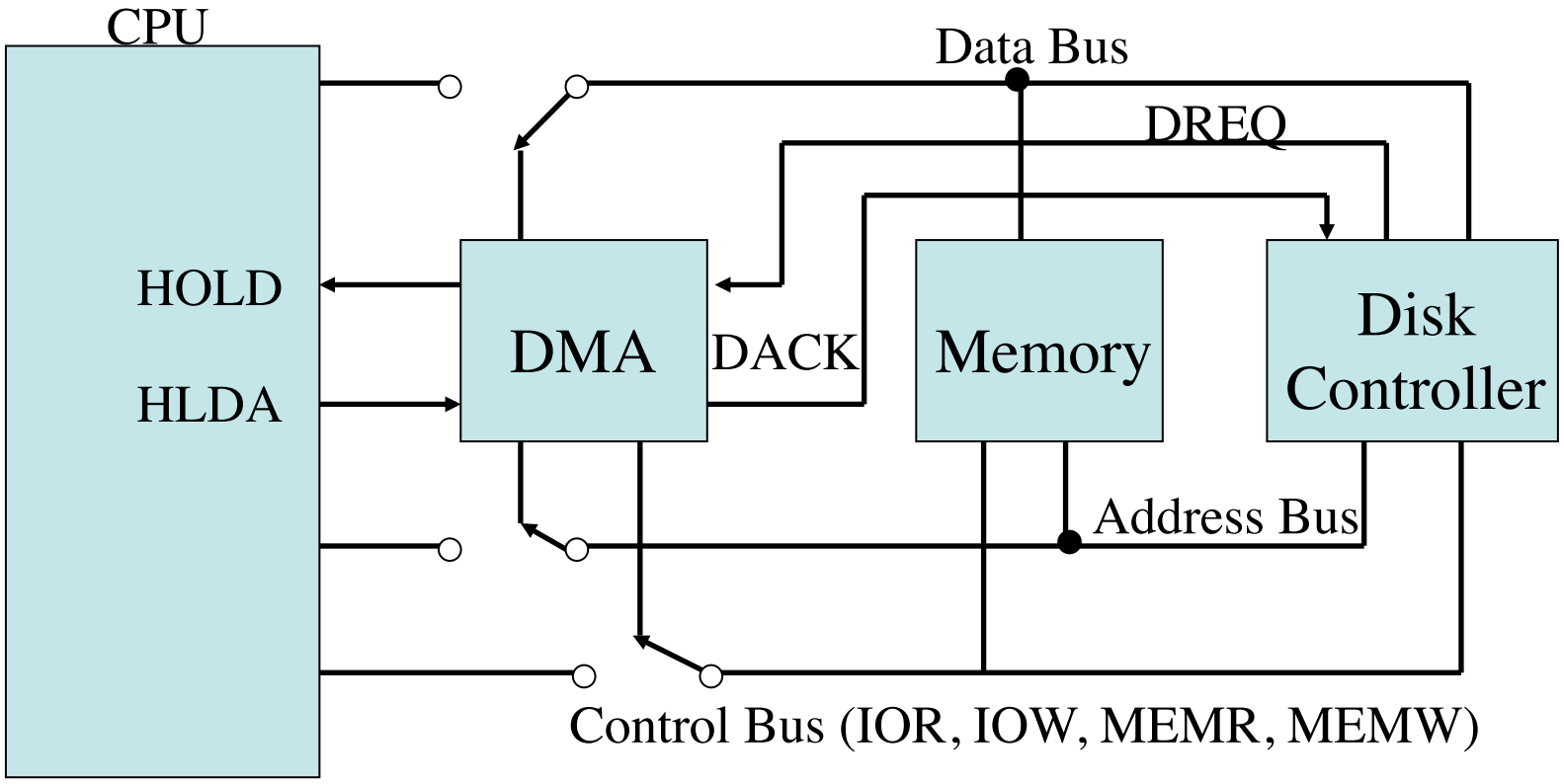
- DMA Concepts
- Intel 8086/8088 DMA System
- DMA Controller 8237

Intel 8086/8088 DMA System

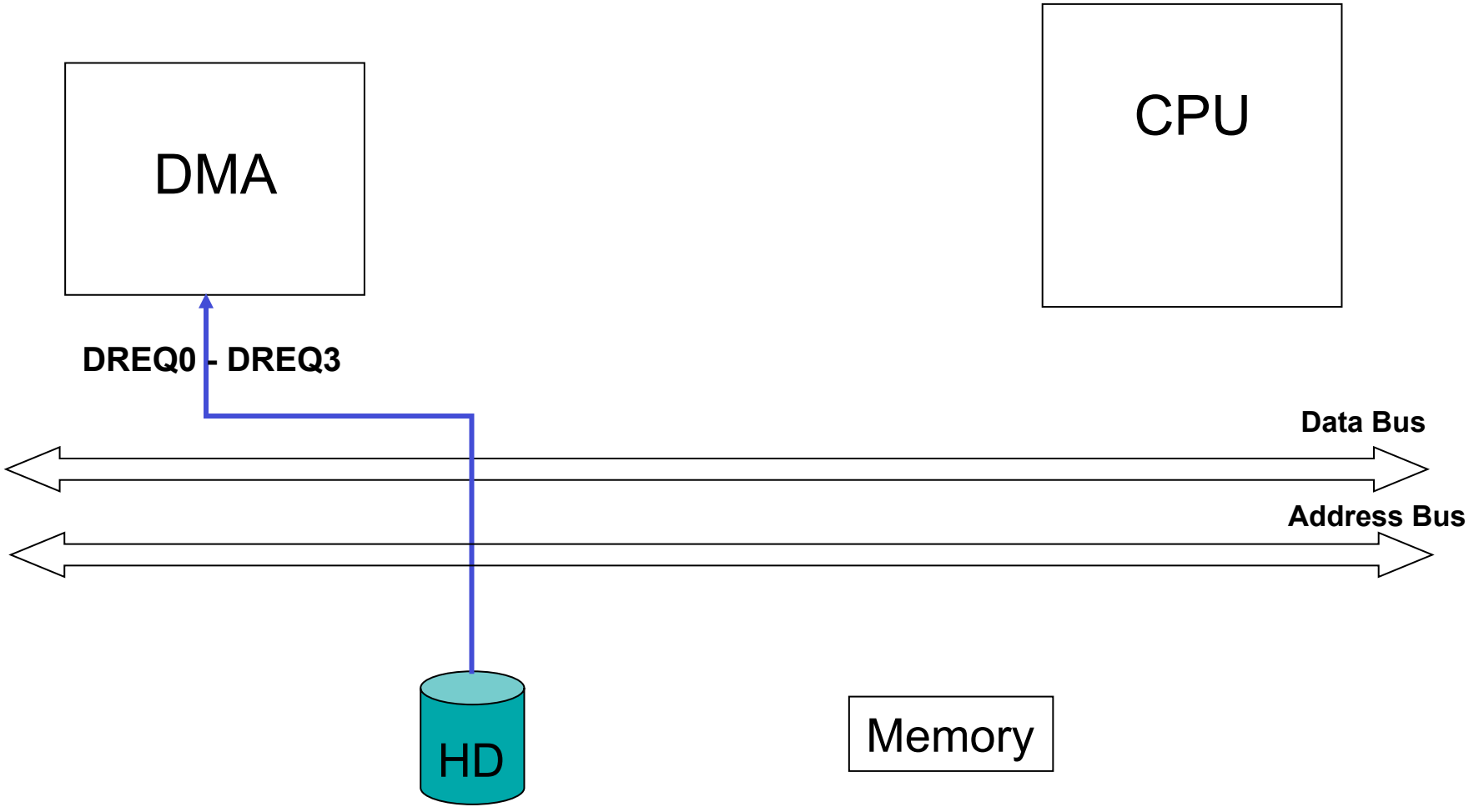


- **DMA System consists of 5 main components: I/O, memory, DMA controller, CPU and interrupt controller.**
- **I/O devices and memory can have direct data transfer under the control of DMA controller.**
- **During the DMA transfer, CPU can be freed to execute other tasks.**
- **After the DMA transfer finishes, the CPU can be notified by an interrupt.**

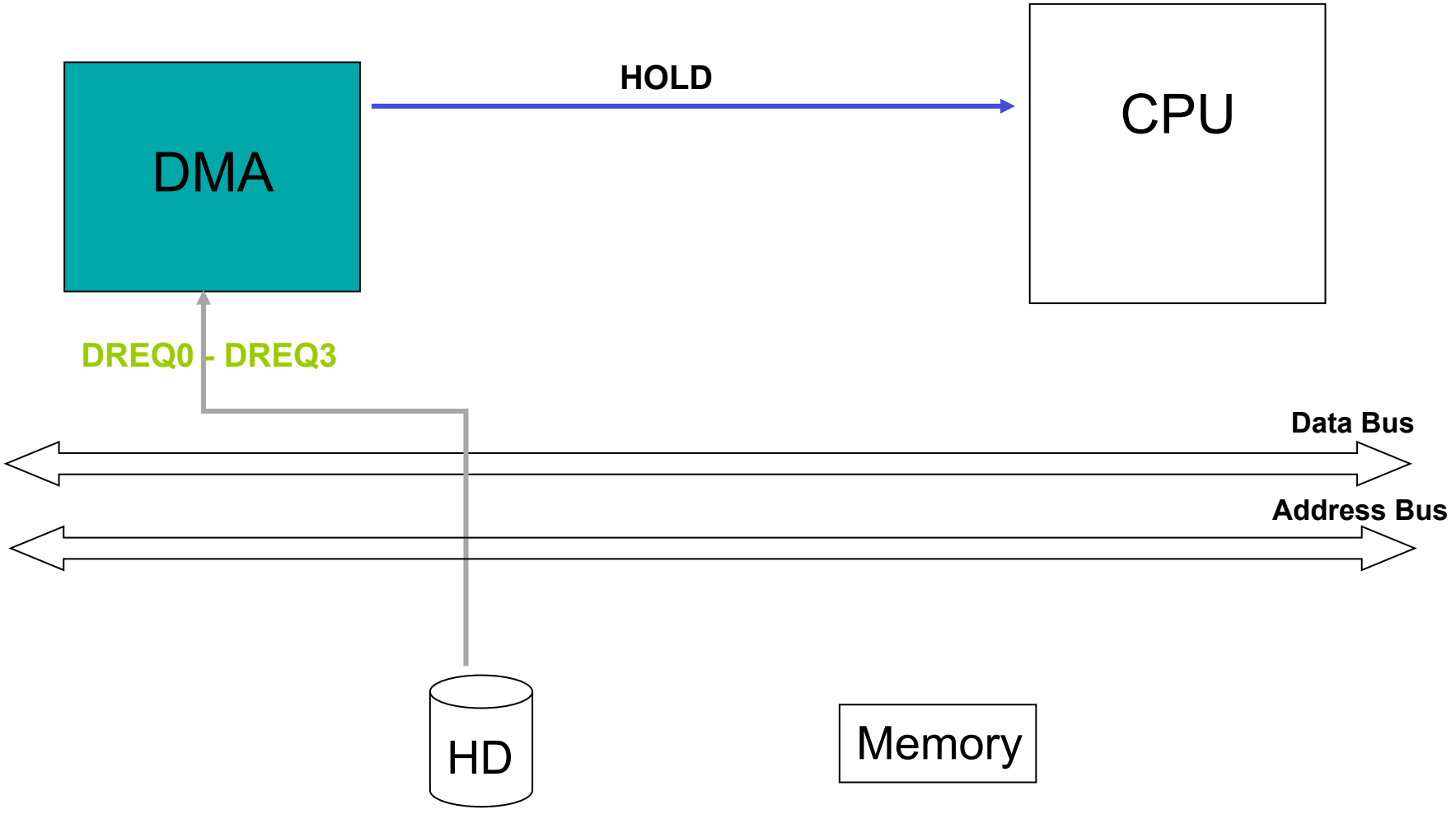
DMA Usage of System Bus



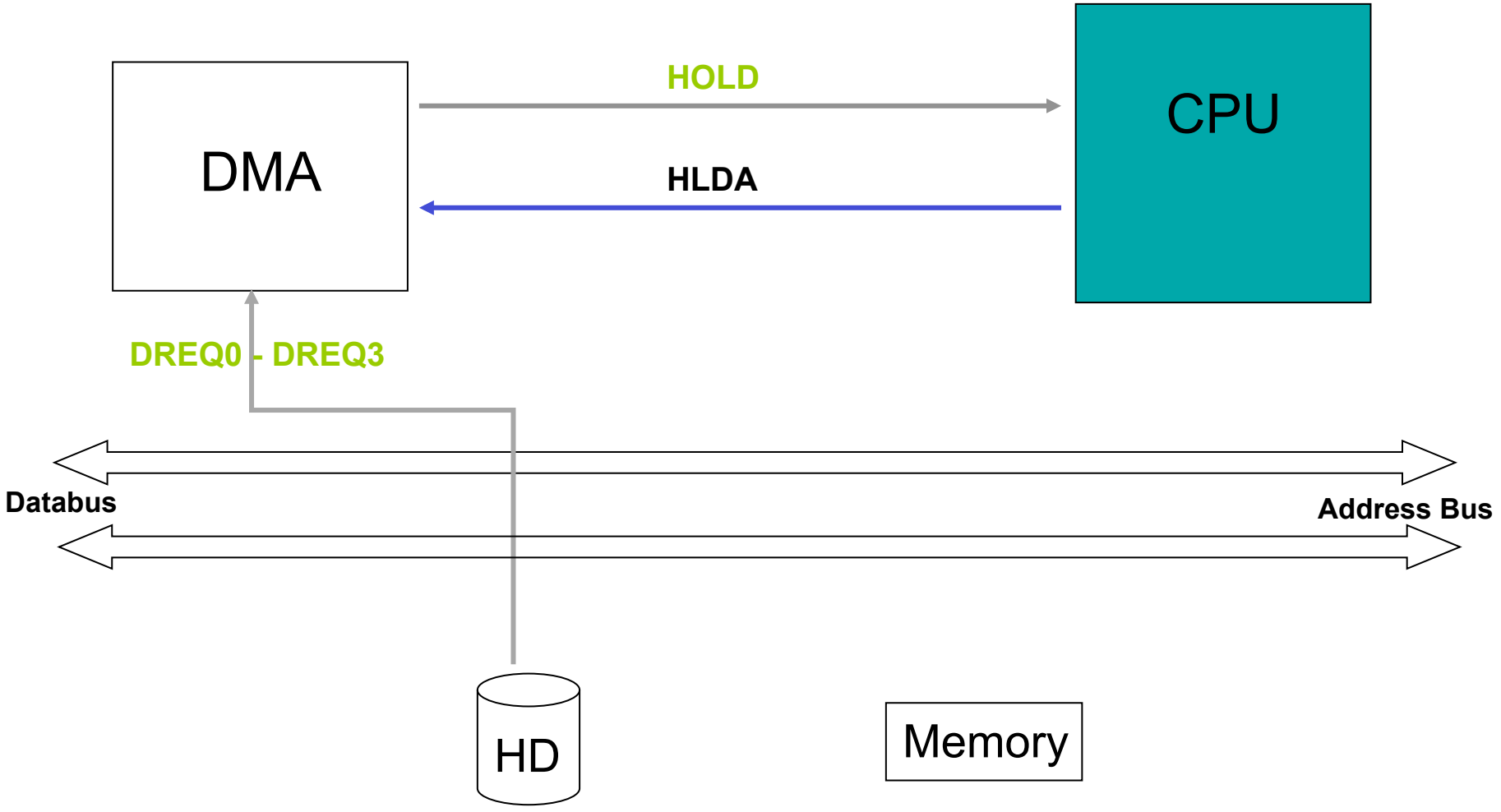
Step 1: I/O Issues a DREQ to DMA



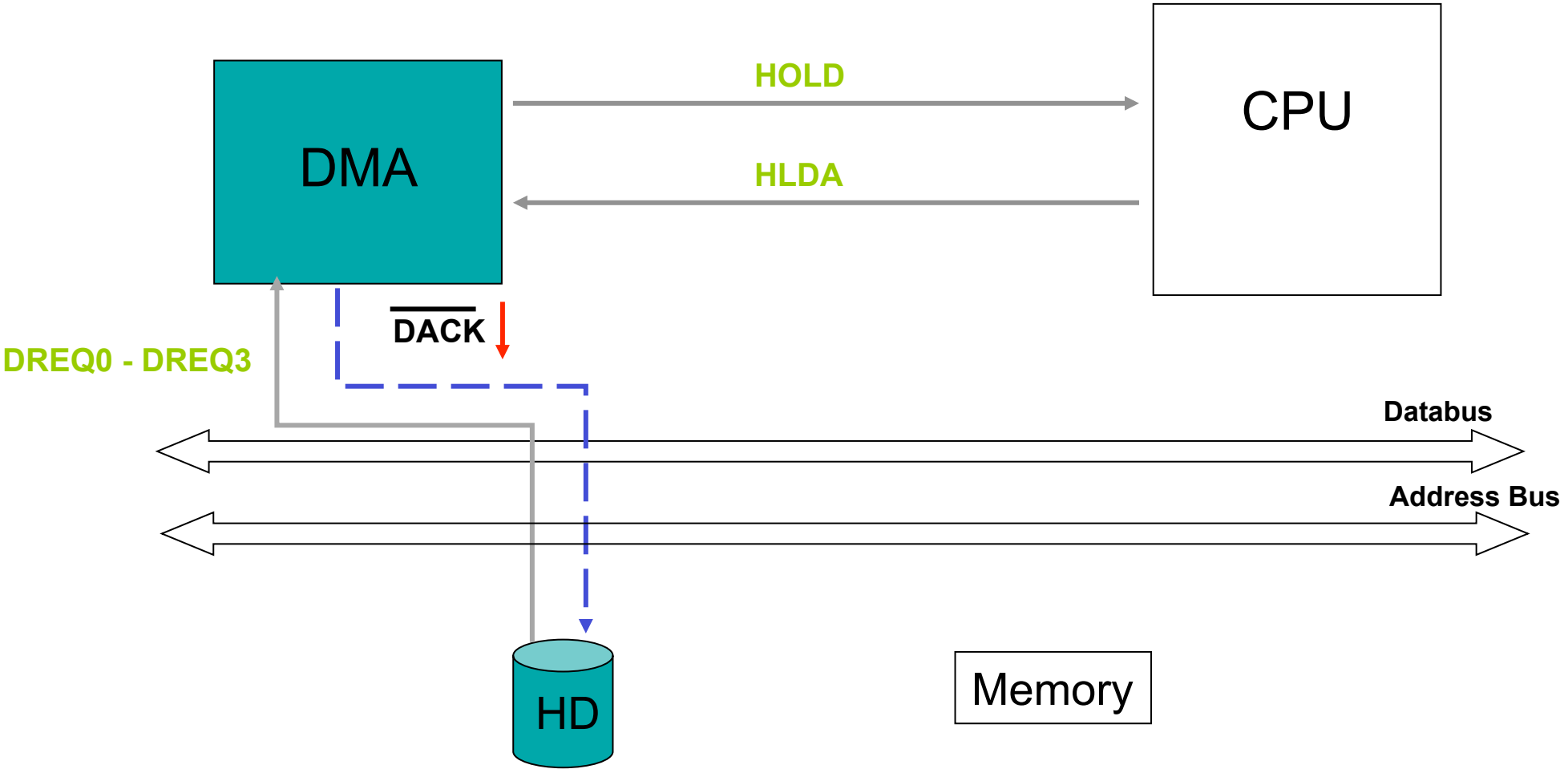
Step 2: DMA Sends HOLD to CPU



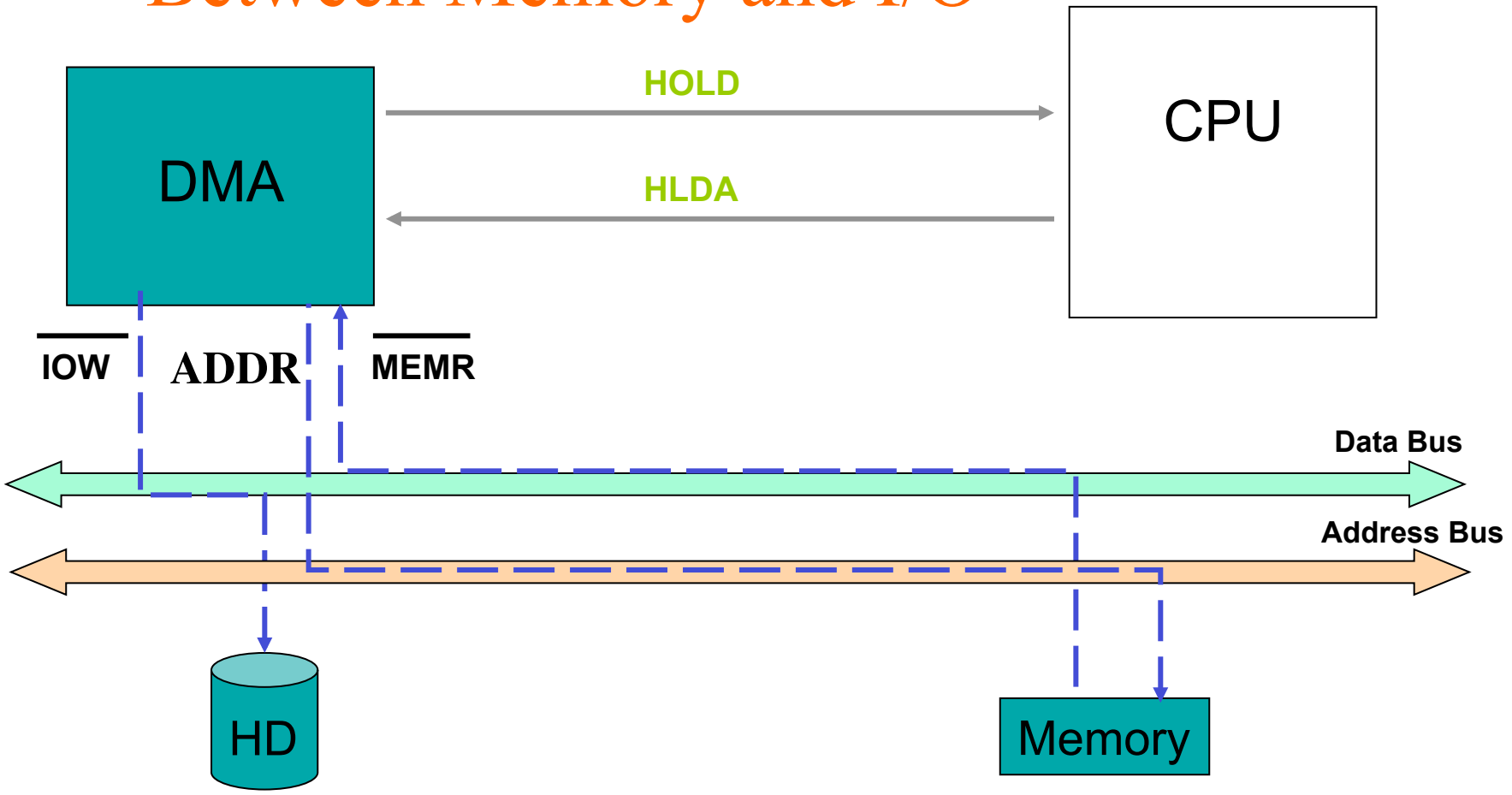
Step 3: CPU Grants HLDA to DMA



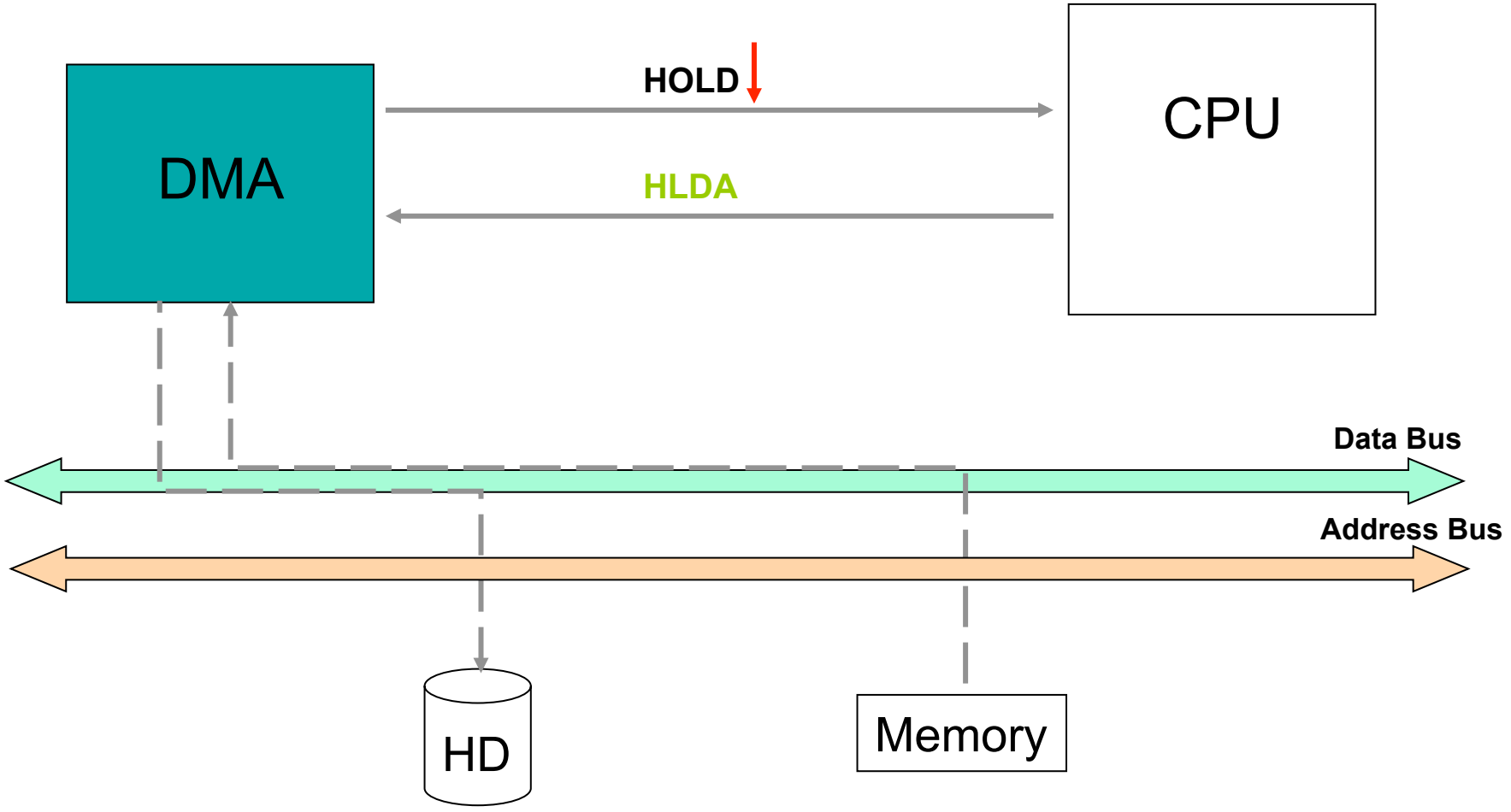
Step 4: DMA Activates $\overline{\text{DACK}}$ to I/O



Step 5: DMA Starts Transfer Between Memory and I/O



Step 6: DMA Ends Transfer



Outline: Direct Memory Access

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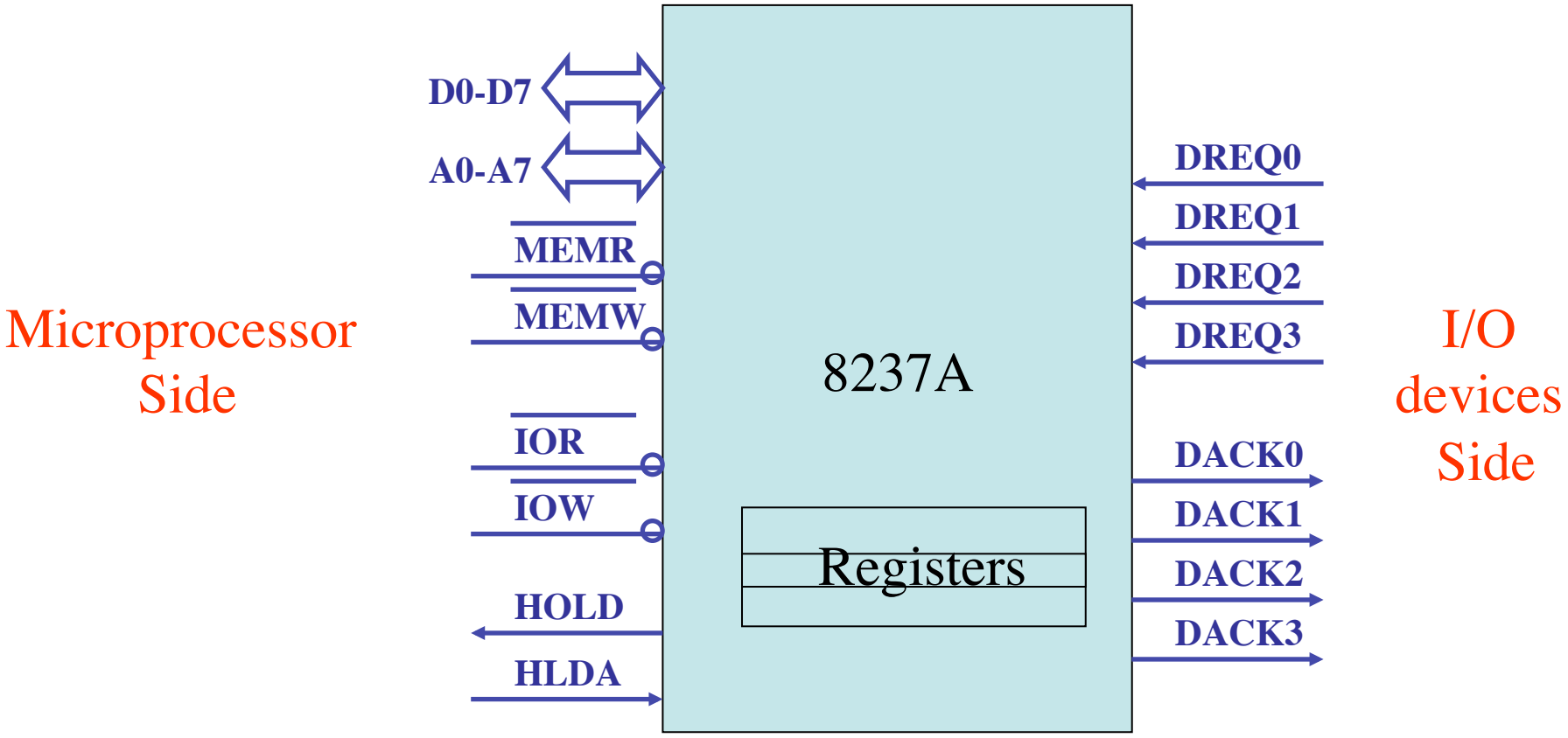
8237 DMA Controller



Registers in the DMA Controller 8237

CAR: DMA Current Address Register, stores the starting memory location which will be accessed by the DMA channel;

CWCR: Current Word Count Register, is used to specify the required number of type data transfer;

CR: Command Register, programs the operation of DMA controller.

SR: Status Register, contains the status for the four DMA channels.

MR: Mode Register, programs the mode of operation for a channel.

BR: Bus Request Register is used to request a DMA transfer via software.

MSR: Mask Register clears or sets all of the masks of channels.

Accessing 8237 Registers

- **We need to set registers to start a DMA transfer under the control of controller 8237.**
  - 1 Address Register for each channel
  - 1 Counter Register for each channel

  There are 4 channels in the DMA controller
  - 1 Mode Set Register for all the 4 channels
  - 1 Command Register for all the 4 channels
  - 1 Status Register for all the 4 channels

We need at least set 4 registers to start a DMA transfer for a channel x. They are channel x Address Register, channel x Count Register, Mode Set Register, Command.

8237 DMA Current (Base) Address Register

DMA Current (Base) Address Register (CAR) is a 16-bit register that stores the lower 16-bit physical address of the starting memory location which will be accessed by the DMA channel.

For example, if the starting memory address is 2000H:5000H = 25000H, you need to fill 00H to its LSB port and 50H to its MSB port. Please note that DAR's LSB port and MSB port share the same I/O address.

The higher 4-bit (2H) will be separately handled by 8237. (This knowledge point is not required in the exam but interested students can refer to pg 463 and Figure 15-13 in the textbook for more details.)

	D7	D6	D5	D4	D3	D2	D1	D0
LSB	A7	A6	A5	A4	A3	A2	A1	A0
MSB	A15	A14	A13	A12	A11	A10	A9	A8

8237 Current (Base) Word Count Register

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- The 16-bit Current (Base) Word Count Register is used to decide when the data transfer through a DMA channel should stop after the required number of DMA cycles.

- The current word count register is initialized with the binary equivalent of the number of required DMA cycles minus one. For example, if you want to move 2KB data, the data in CWCR should be 2KB-1=07FFH. As a result, 07H should be assigned to MSB of CWCR and FFH should be assigned to LSB of CWCR.

- After each DMA cycle, the CWCR content will be decremented by one and finally becomes zero.

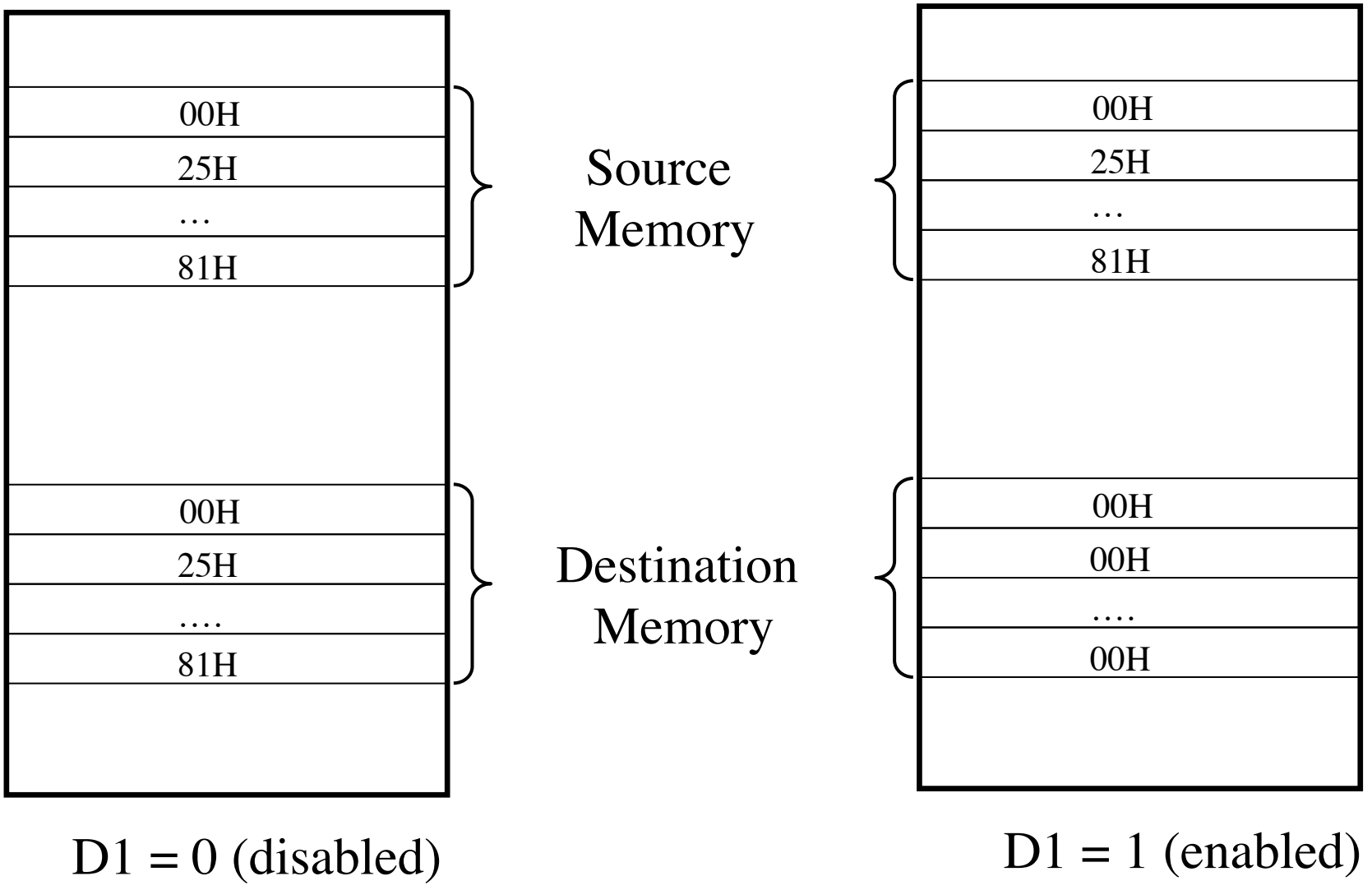
	D7	D6	D5	D4	D3	D2	D1	D0
LSB	C7	C6	C5	C4	C3	C2	C1	C0
MSB	C15	C14	C13	C12	C11	C10	C9	C8

8237 Command Register

- The Command Register programs operation of the 8237
- D0 selects memory-to-memory mode. 1: enabled, 0: disable.
- D1=1, channel 0 address hold is enabled. D1= 0 to disable.
- If D2=1, the DMA controller is off. D2=0 the DMA controller is on.
- D3 determines whether a DMA cycle contains two (compressed) or four (normal) clock cycles. D3=1 for compressed and D3=0 for normal.
- D4 selects priority for the four DMA channel DREQ inputs. D4=1 for rotating priority and D4=0 for fixed priority.
- D5 is used in normal timing to extend the write pulse. D5=1 is the extended write selection, while D5=0 is late write selection.
- D7-D6 program the polarities of the DREQ inputs and DACK outputs.
  D6=0: DREQ sense active high, D6=1: DREQ sense active low
  D7=0: DACK sense active low, D7=1: DACK sense active high

D7	D6	D5	D4	D3	D2	D1	D0
DK	DQ	WS	FRP	NCT	CDE	ADE	MDE

D1 Bit: Memory Address Hold

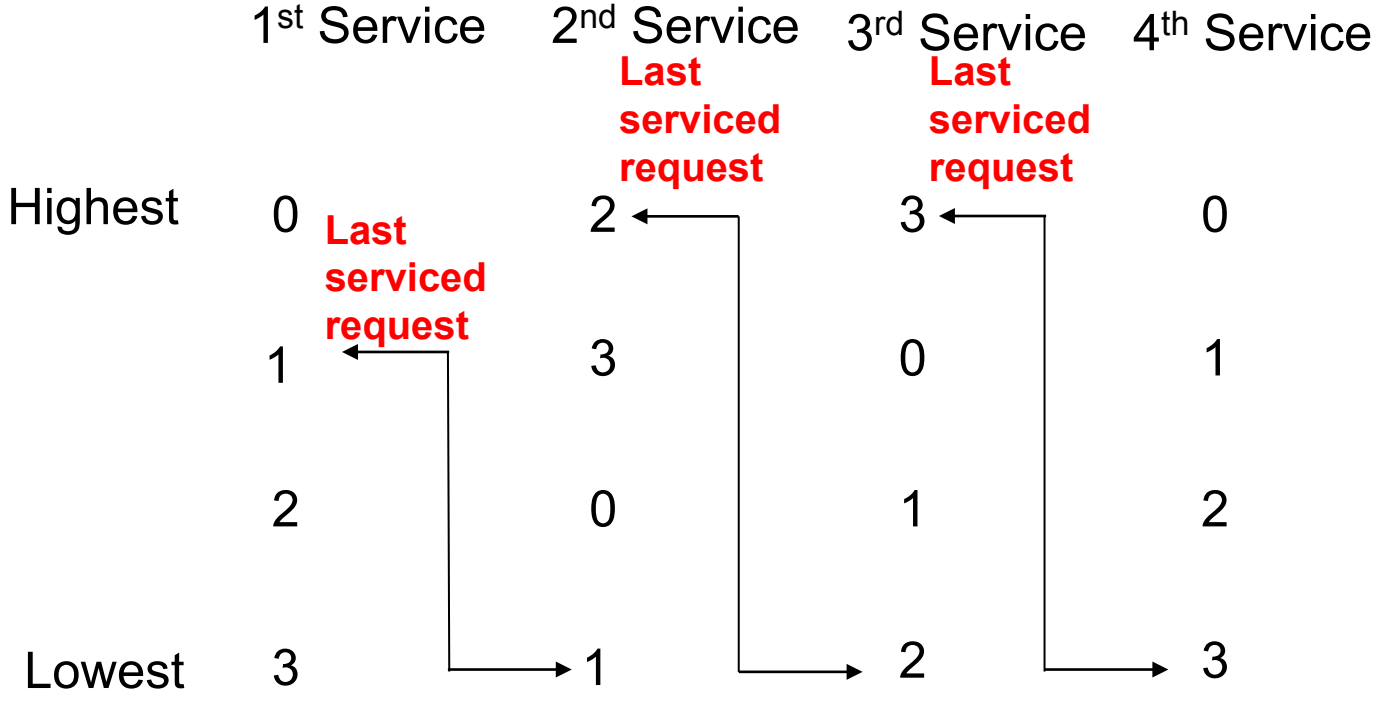


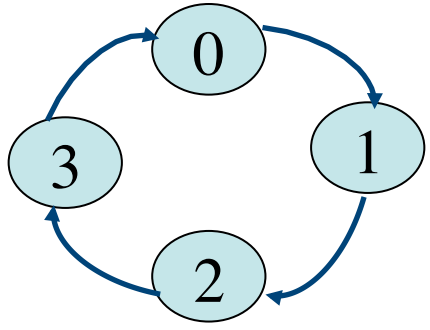
Rotating Priority

- **The channel with priority *P* served in the current service will be given the lowest priority in the next service. For example, if channel 1 is served in the 1st service, it will become the lowest priority in the 2nd service.**

- **The next highest priority channel will be the channel with priority *P-1* in this service. For example, channel 2 will get the highest priority since it has one level lower priority compared to channel 1 in the 1st service.**

- **The rest channels get the priorities rotated.**





8237 Mode Set Register

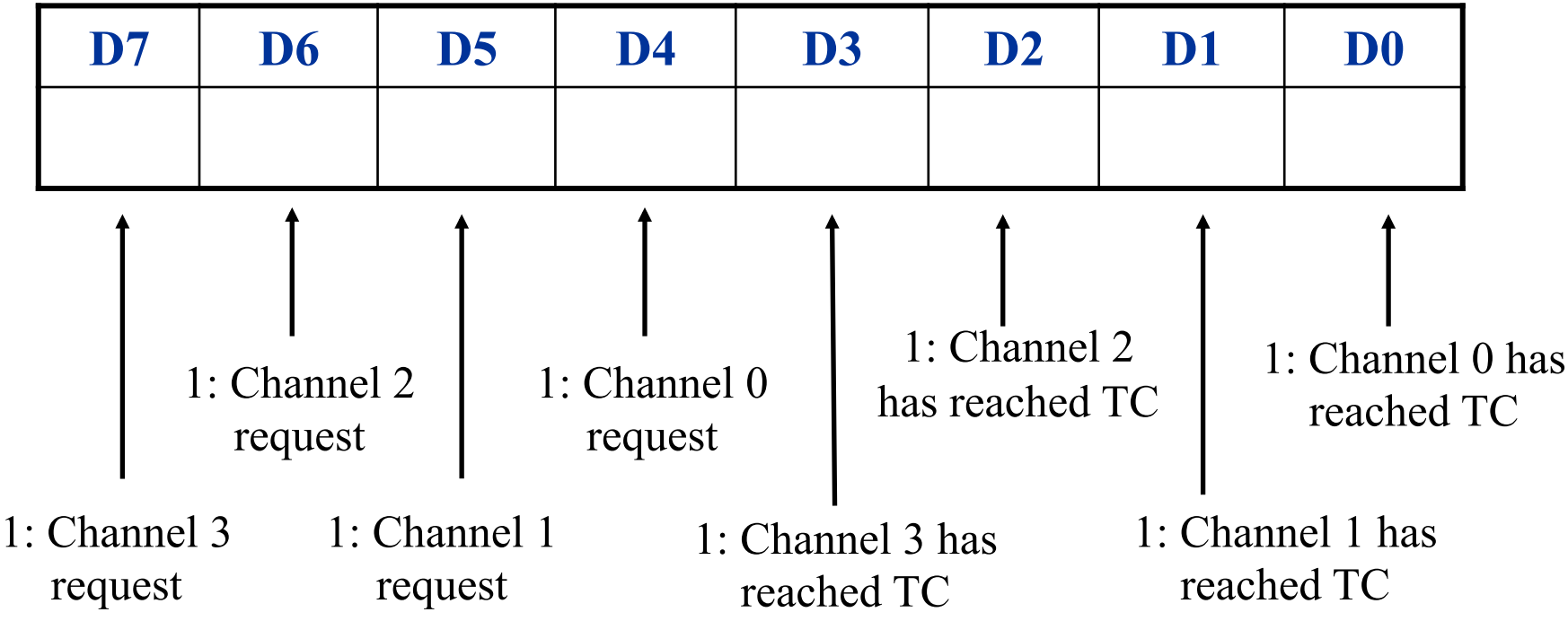
- The Mode Set Register programming the mode of operation for a 8237 channel.
- D1-D0 select the channel to operate on.
  00 = channel 0 select, 01= channel 1 select, 10 = channel 2 select and 11 = channel 3 select
- D3-D2 select the operation. 00 = verify transfer, 01 = write transfer, 10 = Read transfer
- D4 selects auto-initialization. D4=1 enable autoinitialization, D4=0 disable.
- D5 selects address increment/decrement mode. D5=1 decrement, D5=0 increment
- D7-D6 select modes of operation.
  00: Demand mode select (transfer data until the DREQ becomes inactive)
  01 Single mode select (release HOLD after each byte data transfer)
  10 Block mode select (automatically transfer the number of bytes in the count register)
  11 Cascade mode select (more than one 8237 is present in a system)

D7	D6	D5	D4	D3	D2	D1	D0
MS1	MS0	ADI	AI	OM1	OM0	CS1	CS0

8237 Status Register

- **The lower order 4 bits of this register contain the count status for the four individual channels.**

- **The higher order 4 bits of this register contain the request status for the four individual channels.**

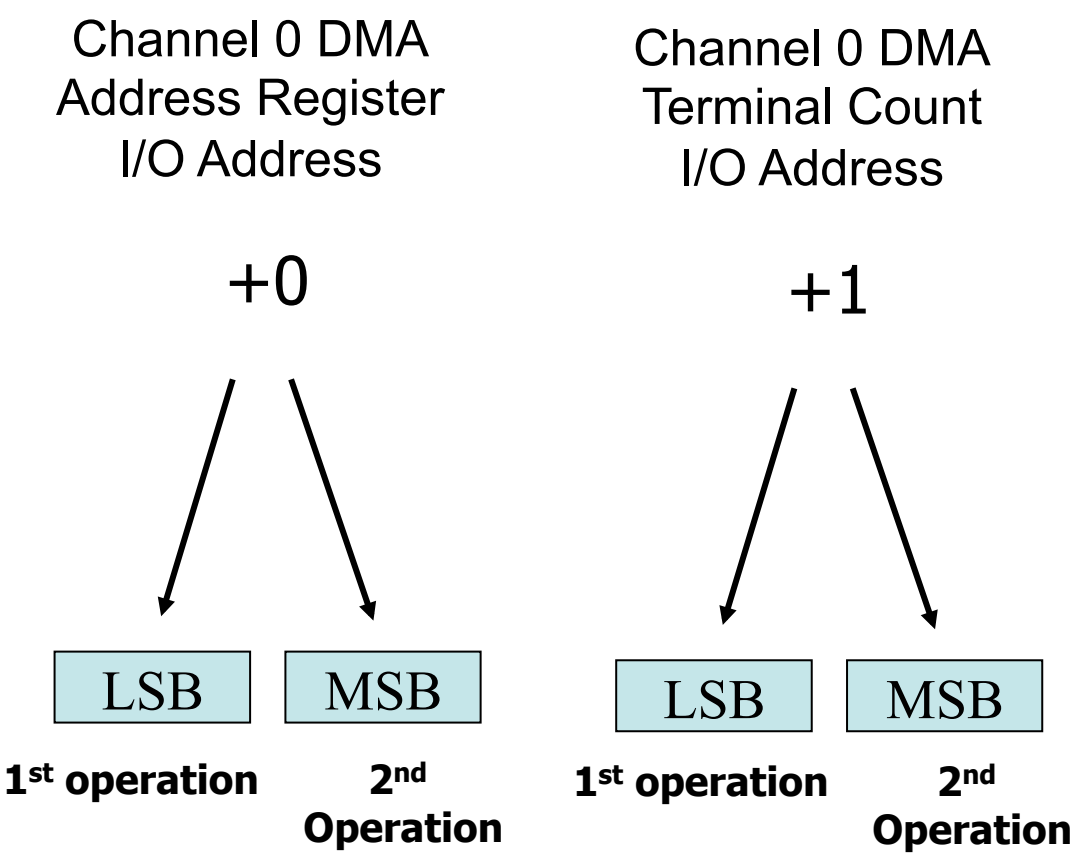


I/O Port for 8237 Registers

Register	Byte	I/O Address Offset
CH-0 DMA Address	LSB/MSB	+0
CH-0 Terminal Count	LSB/MSB	+1
…	…	…
CH-3 DMA Address	LSB/MSB	+6
CH-3 Terminal Count	LSB/MSB	+7
Command/Status Register		+8
Mode Set Register		+11

Suppose channel 0 DMA Address Register has an I/O address 80H, then the Command Register (only be written) should has an I/O address 88H, and the Status Register (only be read) should has an I/O address 88H as well. Mode set Register has a port address of 8BH. The above port address offsets should be remembered by heart!

I/O Ports of the 8237 DMA Controller



The LSB and MSB of a DMA Address Registers (DAR) or Terminal Count Registers in 8257 share the same I/O address. Depending on the operation sequence, the LSB and MSB will be differentiated.

For example, if channel 0 DMA Address Register I/O address is 80H, and the starting address of the memory block to be accessed using DMA is 5000H.

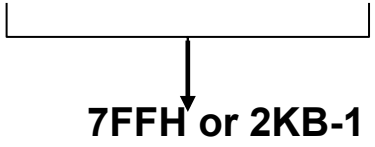
```
MOV AL, 00H ; assign LSB
OUT 80H, AL  ; to channel 0 DAR
MOV AL, 50H ; assign MSB
OUT 80H, AL  ; to channel 0 DAR
```

Example Code to Use 8237

8237 Initialization for the following mode: enable channel 0; disable autoinitilization; normal timing, disable rotating priority. We want to move 2KB of data from an I/O device to memory address 2000:5000H = 25000H. Assume port address for the address register of channel 0 is 80H.

```
MOV AL, 00H;        Load lower byte of DMA Address Register of channel 0
OUT 80H, AL;
MOV AL, 50H;        Load higher byte of DMA Address Register of channel 0
OUT 80H, AL;
MOV AL, FFH;        Load lower byte of Terminal Count Register of channel 0
OUT 81H, AL;
MOV AL, 07H;        Load higher byte of Terminal Count Register of channel 0
OUT 81H, AL;
MOV AL, 84H;        Mode Set Register Initialization (1000 0100) write to memory with block mode
OUT 8BH, AL;        Mode Set Register Initialization should be after DAR and TCR initialization
MOV AL, 0;          normal timing, disable rotating priority
OUT 88H, AL;        Write to command Register the above modes
```

Mode Set Register = 1000 0100 = 84 H; Command Register = 00H; DMA Address Register = 5000H;
Terminal Count Register = 0000 0111 1111 1111 = 07FFH;



Only require you to know how to use CAR, CWCR, MR and CR of 8237!