DURING THE CG3207 FINAL DEMONSTRATION

(1) When the examiner comes to assess your project, the FPGA should already be able to show the task you intend to demonstrate
(2) Hand in **two** completed hardcopies of the ***CG3207 Final Demonstration Form (2012).*** Printing on both sides of the paper is strongly encouraged.
(3) Hand in your **project report** to the examiner
(4) You have been provided with two FPGA, such that you can download your bit files to one FPGA while the other one is being used for demonstration purposes. This might be useful if your ROM is not enough to show all parts of your program and you have split your program into more than one bit files. Usually, each team will be given around 5 to 10 minutes for their demonstration

SUBMISSIONS

(1) As requested by the lecturer, you should hand in one hardcopy of your report during the demo.
(2) Additionally, a single zipped file must be uploaded to the IVLE workbin under the folder ***2012 - CG3207 Project Submission***. The following requirement should be met, and failure to do so can involve missing out project marks:
    a. Softcopy items are to be uploaded to IVLE by Friday **16th November 2012 23.55 hrs**
    b. Only **one zipped file per team**, which follows **this exact naming** scheme: ***2012-CG3207-Team XX***, where ***XX*** is your team number. For example: 2012-CG3207-Team 02 is the zipped file uploaded by team 02
    c. The **zipped file must contain**:
        i. The report, that was submitted as a hardcopy during the demo day, in PDF format
        ii. Your whole Xilinx project folder **(Ensure that i8051_top_summary.html is available in the project folder)**
        iii. Your C program project folder (Ensure that the .C source file and the .hex file are present in the folder). Alternative third party compiling programs can also be used, but the source file and the hex file must be provided
        iv. Any additional files/images/documents that you feel could be helpful in the grading process
        v. The completed softcopy version of ***CG3207 Final Demonstration Form (2012)*** in PDF format
    d. Ensure that your VHDL project has already been synthesised before the upload. This will allow us to view the summary report and all other reports directly without the need for us to re-synthesised the program
    e. Ensure that the bit file can be created by us, without the need for any modification, when we click on ***Generate Programming File***

REPORT CONTENTS

The report should give the reader a clear view that you have understood what has been done throughout the project and that you have understood what is happening inside the 8051, and particularly focusing on items that might help to distinguish your project from others. It can (none are compulsory):

(1) include the implementation description of the most difficult instruction(s) that you have implemented
(2) include a description and simulation sample on how stimuli in the Xilinx test bench was used to test the written C / ASM program instead of directly testing on the FPGA
(3) mention about interrupts, timers, serial port, optimisations, additional VHD modules and external memory if they have been used, and how they were demonstrated through the FPGA if applicable
(4) indicate feasible optimisation methods for your computer architecture
(5) contain contents as mentioned in the ***CG3207 Final Demonstration Form (2012)***
(6) have a conclusion and indication of how the CG3207 project module can be improved

The report can be 4 to 10 pages, font size 8 to 12, with single line space. Feel free to use additional dozens of pages as required: there is no penalty. **Codes copied directly from VHDL must be avoided in the report.**