EE4415:
Integrated Circuits Design

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Course Websites & Ref. Books

- http://ivle.nus.edu.sg
- Jan M. Rabaey, Anantha Chandrakasan, and Borivoje Nikolic, "Digital Integrated Circuits", 2E, Prentice-Hall.
- Sung-Mo Kang, and Yusuf Leblebici, "CMOS Digital Integrated Circuits: Analysis and Design", 3E, McGraw Hill.
- Himanshu Bhatnagar, "Advanced ASIC Chip Synthesis Using Synopsys Design Compiler,Physical Compiler, and PrimeTime", Kluwer Academic Publishers, 2002.
- Stephen Brown Zvonko Vranesic, "Fundamentals of Digital Logic with Verilog Design", McGraw Hill.

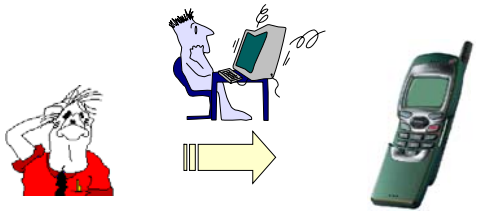
Topics Covered

The first part covers the digital IC design including:

- Introduction to IC design
- ASIC Design Methodology
- Synthesis Basics using Synopsys
- Design exercises = 30% CA

What Is IC Design ?

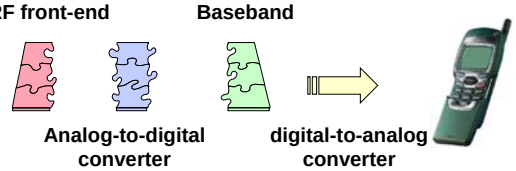
IC design is a process of the transformation of an idea into a manufacturable device that carries out an intended function.



Design Classification

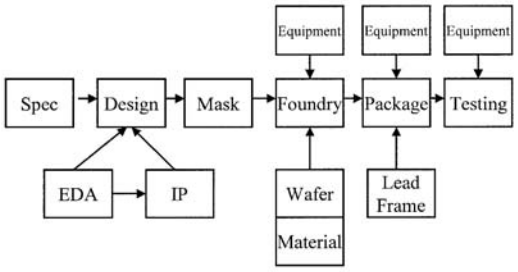
- Analog design.
- Mixed-Signal design.
- Digital design.

RF front-end **Baseband**



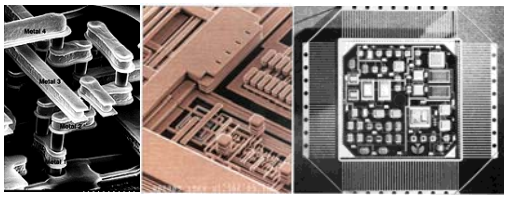
Analog-to-digital converter **digital-to-analog converter**

Semiconductor Industry



Introduction to Digital IC Design

- Why is designing digital ICs different today than it was before?
- Will it change in future?



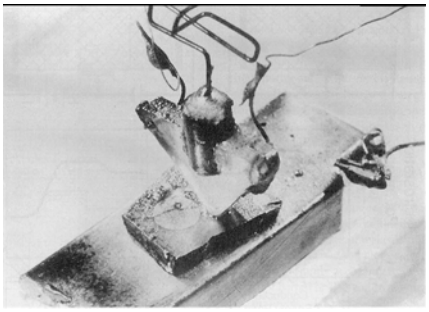
The First Computer

The Babbage Difference Engine (1832)

25,000 parts
cost: ? 7,470

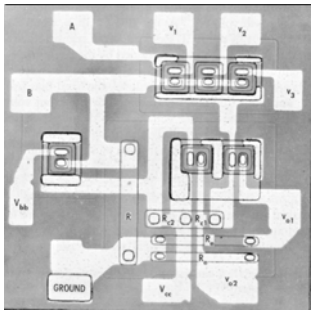
ENIAC : The first electronic computer (1946)

The Transistor Revolution



First transistor
Bell Labs, 1948

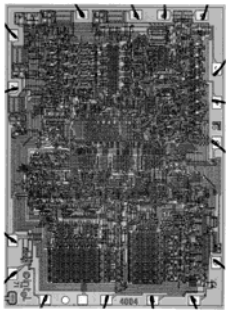
The First Integrated Circuits



Bipolar logic 1960's

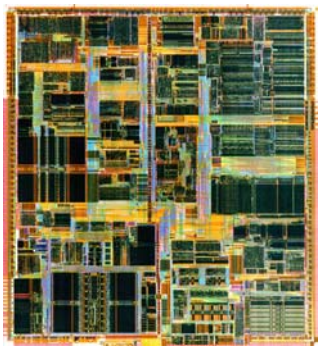
ECL 3-input Gate
Motorola 1966

Intel 4004 Micro-Processor



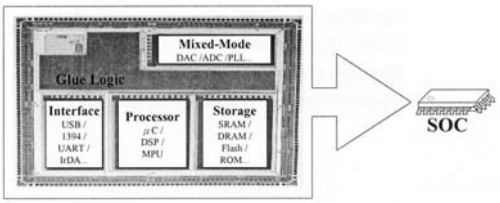
1971
1000 transistors
1 MHz operation

Intel Pentium (IV) microprocessor



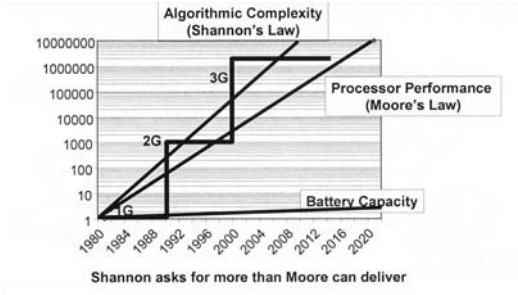
The Trend in IC Design

- System integration : moving from board to chip → System-on-Chip (SoC)
- What is SoC ?



The Challenges

- The algorithmic driving force →design complexity

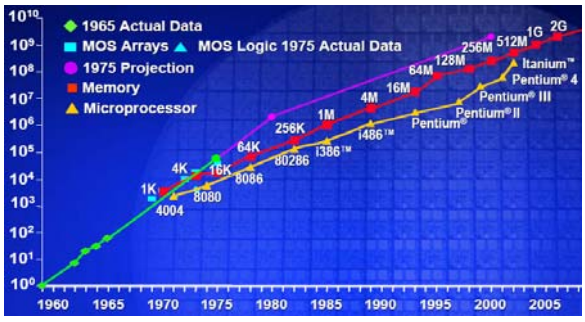


Moore's Law

- In 1965, Gordon Moore noted that the number of transistors on a chip doubled every 18 to 24 months.
- He made a prediction that semiconductor technology will double its effectiveness every 18 months

Number of Transistors per Die

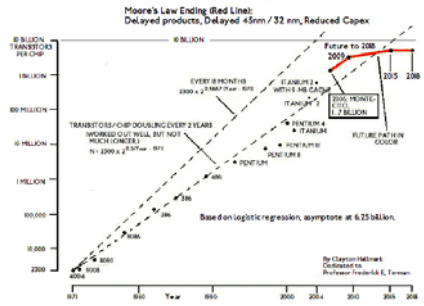
Source: ISSCC 2003 G. Moore "No exponential is forever, but 'forever' can be delayed"



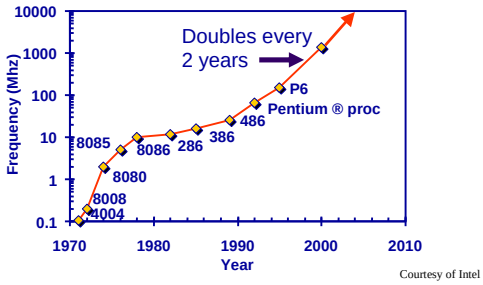
Moore's Law

	Year of introduction	Transistors
4004	1971	2,250
8008	1972	2,500
8080	1974	5,000
8086	1978	29,000
286	1982	120,000
386™	1985	275,000
486™ DX	1989	1,180,000
Pentium®	1993	3,100,000
Pentium II	1997	7,500,000
Pentium III	1999	24,000,000
Pentium 4	2000	42,000,000

Moore's Law Ending?

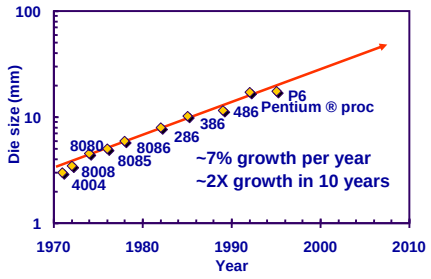


Microprocessor Clock Frequency



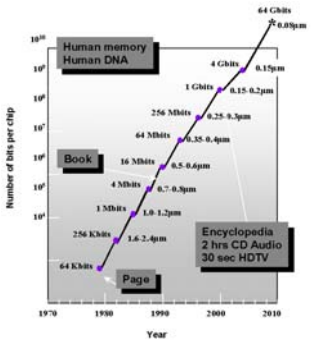
Courtesy of Intel

Die Size Growth

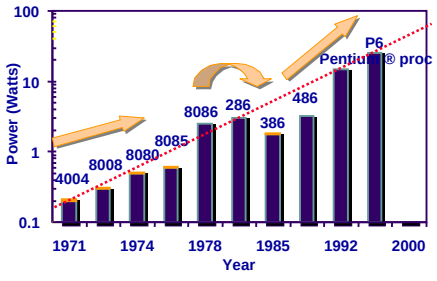


Courtesy of Intel

Evolution in Complexity

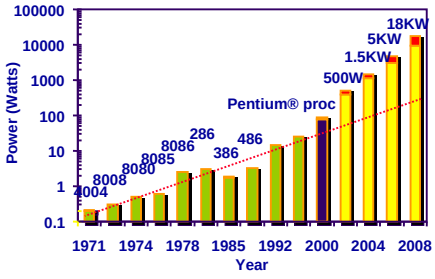


Power Dissipation



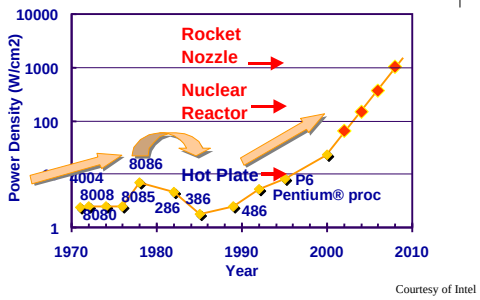
Courtesy of Intel

Power: a Major Problem



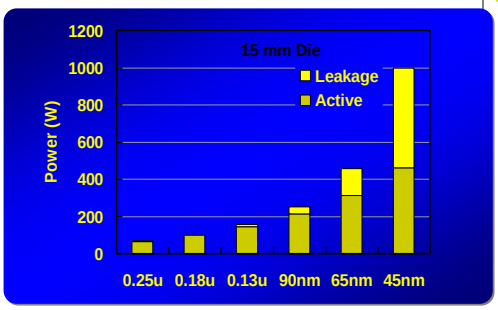
Courtesy of Intel

Power Density



Courtesy of Intel

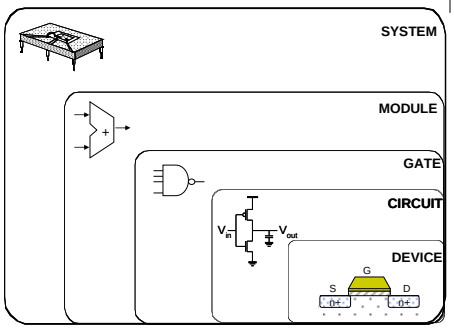
The Power Crisis



Technology Scaling

- Technology shrinks by ~0.7 per generation
- With every generation can integrate 2x more functions on a chip; chip cost does not increase significantly
- Cost of a function decreases by 2x
- But …
  - How to design chips with more and more functions?
  - Design engineering population does not double every two years…
- Hence, a need for more efficient design methods
  - Exploit different levels of abstraction

Design Abstraction Levels



Considerations in IC Design

- Chip size (cost)
- Operation speed (value)
- Power consumption (energy efficiency)
- Manufacturability
- Testability
- Reliability
- Time-to-market
- Constrains in design