NATIONAL UNIVERSITY OF SINGAPORE

EXAMINATION FOR

(Semester II: 2009/2010)

CG1108 – ELECTRICAL ENGINEERING

April / May 2010 - Time Allowed: 2 Hours

INSTRUCTIONS TO CANDIDATES

1. This paper contains **FOUR (4)** questions and comprises **SIX (6)** printed pages.
2. All questions are compulsory. Answer **ALL** questions.
3. This is a **CLOSED BOOK** examination.
4. Programmable calculators are not allowed.

Q.1 (a) Use Ohm's law, KVL, and KCL to find V_x in Fig. 1(a).

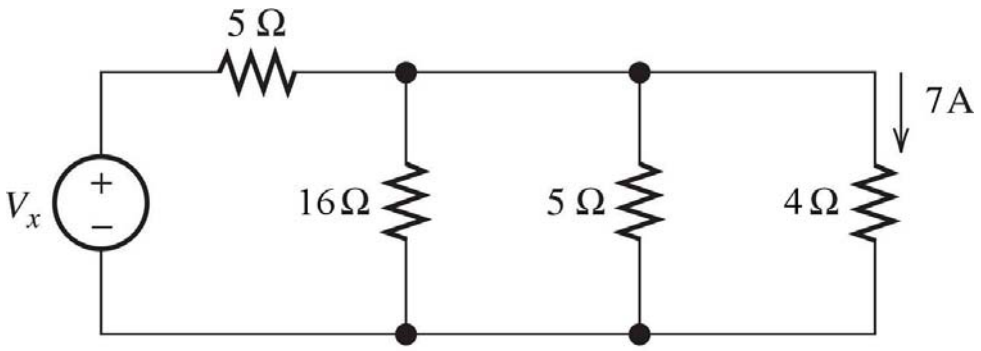

Fig. 1(a)

(8 marks)

(b) Determine the values of v_x and i_y in Fig. 1(b).

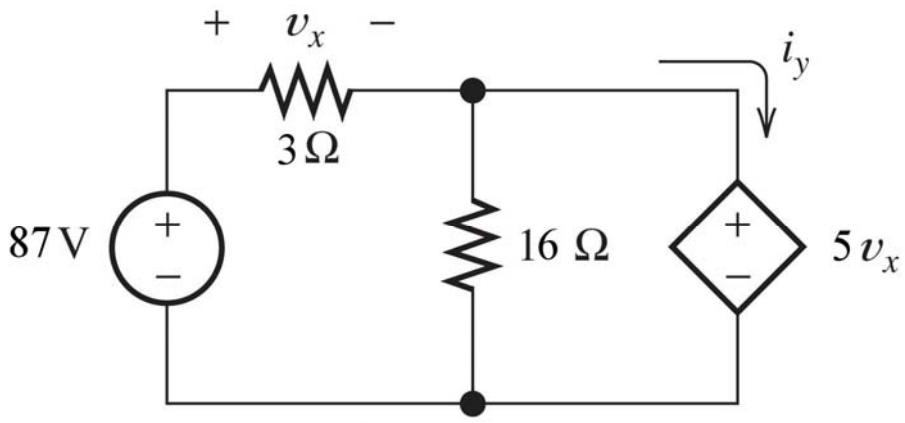

Fig. 1(b)

(8 marks)

Q.1 is continued on Page 3

(c) The circuit in Fig. 1(c) is the electrical model for an electronic megaphone, in which the 8 Ω resistance models a loudspeaker, the source V_x and the 5 kΩ resistance represent a microphone, and the remaining elements model an amplifier. Given that the power delivered to the 8 Ω resistance is 8 W, determine the current circulating in the right-hand loop of the circuit. Also, determine the value of the microphone voltage V_x.

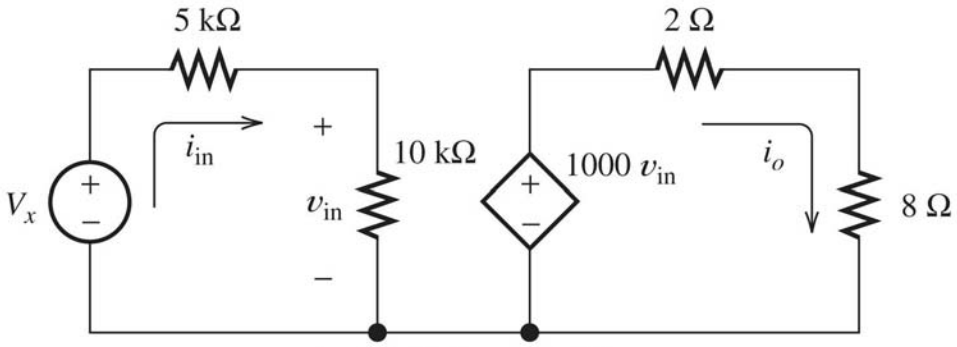

Fig. 1(c)

(9 marks)

Q.2 (a) Find the values of v and i in Fig. 2(a).

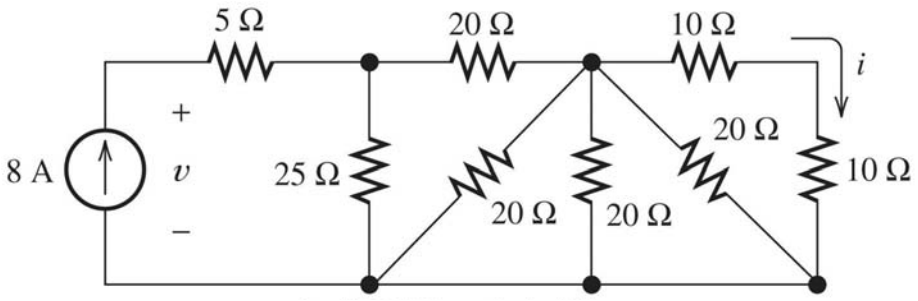

Fig. 2(a)

(8 marks)

(b) Find the values of i_1 and i_2 in Fig. 2(b). Find the power for each element in the circuit, and state whether each is absorbing or delivering energy.

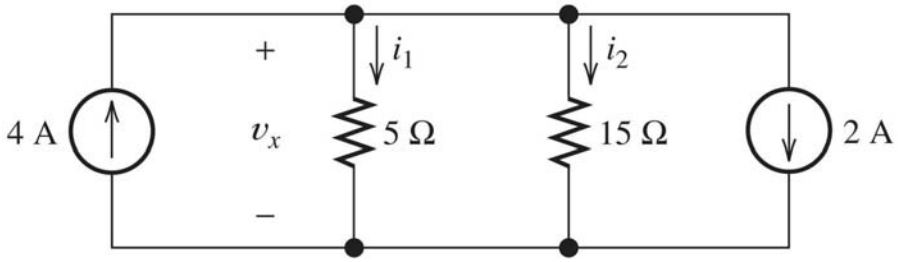

Fig. 2(b)

(8 marks)

Q.2 is continued on Page 4

(c) Find the Thévenin and Norton equivalent circuits for Fig. 2(c).

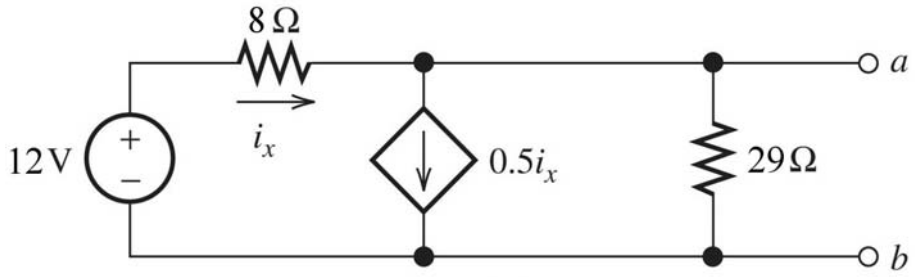

Fig. 2(c)

(9 marks)

Q.3 (a) A logic circuit has four inputs and one output. The output becomes TRUE when two or more of the inputs are TRUE, else the output becomes FALSE.

(i) Construct the TRUTH TABLE for the logic circuit.

(5 marks)

(ii) Use KARNAUGH map to obtain the MSOP (Minimum Sum of products) for the circuit.

(5 marks)

(iii) Implement the circuit using NAND gates only.

(5 marks)

(b) Two inverters, each made of a MOSFET and a 1kΩ resistor, are connected as shown in Fig. 3(a). A TTL signal (V_A) is input to the first inverter at point A, as given in Fig. 3(b).

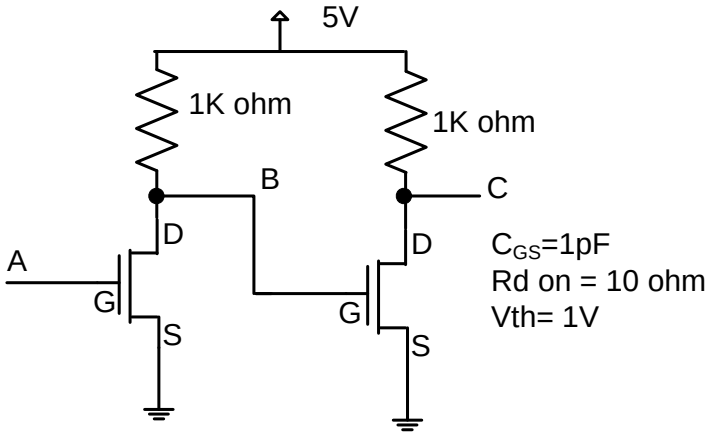

Fig. 3(a)

Q.3 is continued on Page 5

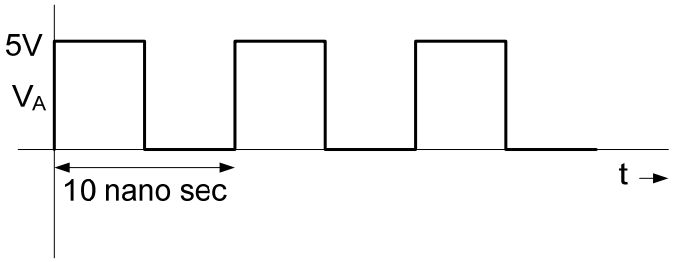

Fig. 3(b)

(i) Draw the wave forms at the points B and C.
(Hint: MOSFET becomes ON when Vgs > V_{th})

(5 marks)

(ii) Find the falling time delay between signals at point A and at point C. The necessary parameters of the MOSFETs are given in Fig. 3(a).

(5 marks)

Q.4 (a) In the circuit given in Fig. 4(a), supply voltage is 240V (RMS). The values of resistor *R*=5Ω and inductor *L* = 1mH.

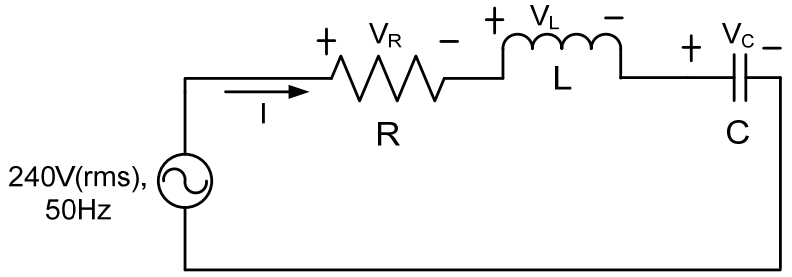

Fig. 4(a)

(i) For the circuit given in Fig. 4(a), find the value of capacitance *C* for which magnitude of *I* will be maximum. Find this maximum RMS value of the current.

(5 marks)

(ii) Taking the supply voltage as the reference phasor, draw the phasor diagram showing the voltage drops across all the elements and the current *I,* using the capacitance *C* obtained in part (i).

(5 marks)

Q.4 is continued on Page 6

(b) A load with specifications of 1 kW and 0.87 lagging power factor is connected to a 240V, 50Hz main supply.

(i) Determine the RMS current drawn by the load operating at full load.

(3 marks)

(ii) This load can be represented by a series R-L circuit. Find the resistance and inductance of the equivalent R-L series circuit.

(8 marks)

(iii) Find the value of the reactive element that must be connected in parallel to this load so that the over all power factor seen by the supply becomes unity at full load.

(4 marks)

END OF PAPER