NATIONAL UNIVERSITY OF SINGAPORE

EXAMINATION FOR

(Semester II: 2007/2008)

EE4415/EE4415E – INTEGRATED DIGITAL DESIGN

April/May 2008 - Time Allowed: 2 Hours

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **Four** (4) questions and comprises **Six** (6) printed pages.
2. Answer all questions.
3. All questions carry equal marks.
4. This is a CLOSED BOOK examination
5. Take $\mu_0 = 4\pi \times 10^{-7}\ H/m$
   $\varepsilon_0 = 8.85 \times 10^{-12}\ F/m$

Q.1 Consider the inverter circuit shown in Fig. Q1.1 where the voltage waveform shown in Fig. Q1.2 is applied to input V_i.

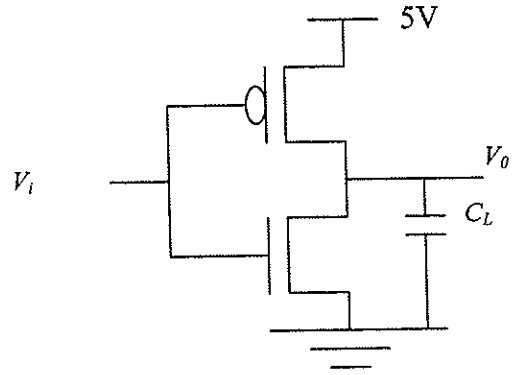

Fig. Q1.1

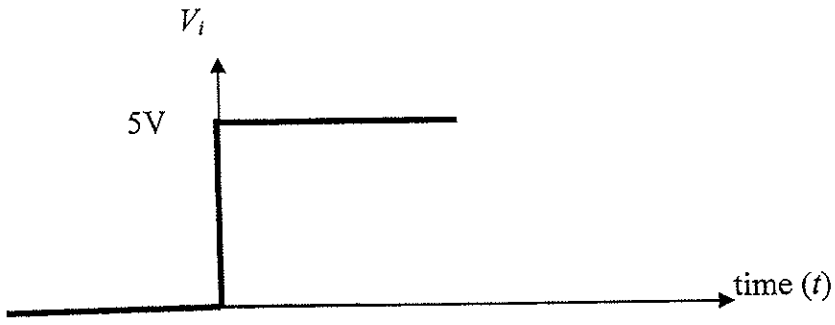

Fig. Q1.2

The waveform shown in Fig. Q1.2 has a 5V step at t=0. V_i is 0V for $t < 0$ and stays constant at 5V for $t > 0$. Assume that the subthreshold currents for all the devices in Fig. Q1.1 are zero. For the devices shown in Fig. Q1.1, V_{GS} and V_{DS} are the gate to source and drain to source voltages, respectively. Furthermore, the drain current I_d in the linear and saturation regions for both the devices is given respectively by

$$I_d = \beta\{(V_{GS} - V_T)V_{DS} - 0.5V_{DS}^2\}(1 + \lambda V_{dsat}) \text{ linear region } (|V_{GS}| \geq |V_T|, |V_{DS}| \leq |V_{dsat}|),$$

$$I_d = \frac{\beta (V_{GS} - V_T)^2}{2}(1 + \lambda V_{DS}) \quad \text{saturation region } (|V_{GS}| \geq |V_T|, |V_{DS}| \geq |V_{dsat}|),$$

and $V_{dsat} = (V_{GS} - V_T)$,

where the magnitude of the threshold voltage V_T = 1V for both devices. With the help of this information, derive an expression for the time for the output V_0 to fall from 5V to 3V in terms of the model parameters λ, β and the load C_L.

(25 marks)

Q.2 Consider a single transistor version of a transmission gate shown in Figure Q2. The input to this transmission gate is connected to the left device terminal which is driven by an inverter on the left, while the output is taken from the right terminal of the device. Clock ϕ is connected to the gate of this device. For what logic level of ϕ would input be transmitted to the output? Is there any logic degradation problem with this gate? Explain.

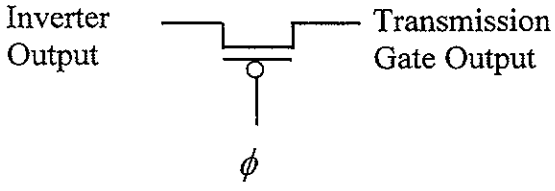

Figure Q2

In this part of the question, use the dotted sheet provided and colour pencils to draw a custom layout of the transmission gate shown in Figure Q2 along with the inverter on the left with built in ease to route ground and power lines. Obey all λ based design rules. Use a scale of 2λ = spacing between dots and conform to standard colour codes. The standard colour codes are brown for n-well, black for contact, blue for the only metal layer, red for polysilicon, green for n-type source-drain (NSD) and purple for p-type source-drain (PSD). Choose device dimensions of W = 4λ and L = 2λ for all devices. In the λ based design rules, the n-well coverage of PSD is 3λ, the unconnected PSD-NSD spacing is 8λ, the minimum dimension/spacing of metal, poly, NSD, PSD and contact is 2λ, the coverage of contact by connecting layers is λ on all sides, the poly extension beyond NSD/PSD is 2λ and poly to NSD/PSD contact spacing is 2λ.

(25 marks)

Q.3 (a) Explain briefly the oxidation process step and elaborate on at least two of its uses.
(5 marks)

(b) Explain how read and write operations are performed, and how storage is achieved using the static random access memory cell shown in Figure Q3. What is the function of two p-channel transistor pairs?
(10 marks)

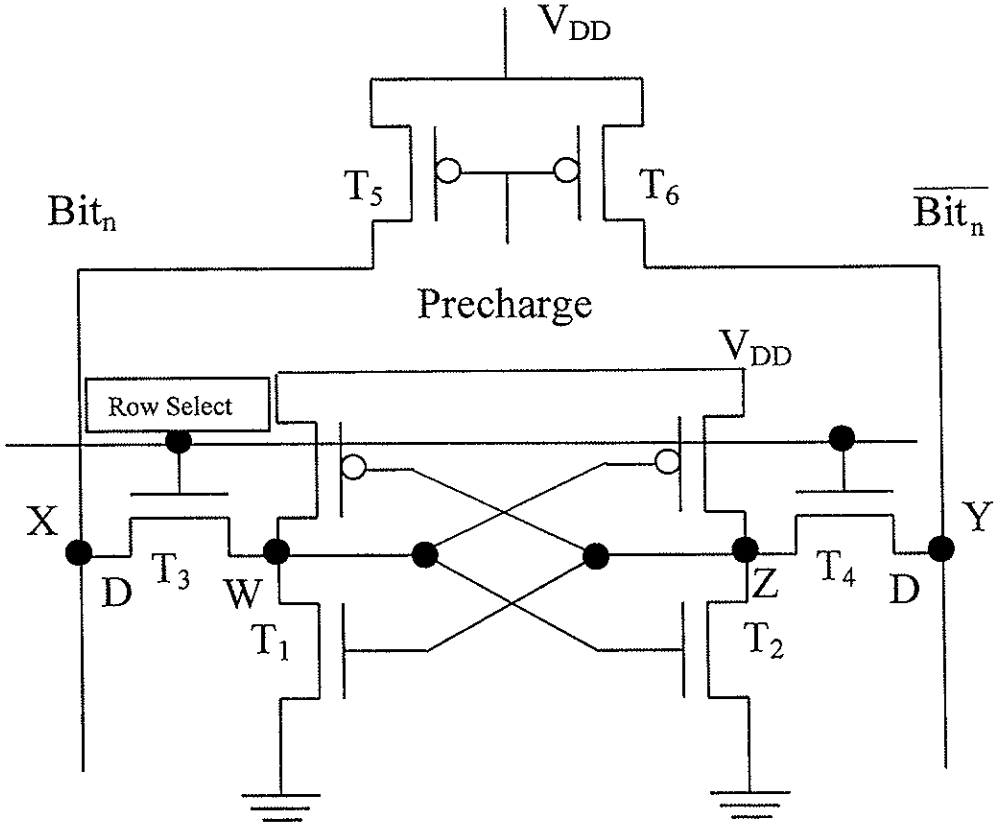

Figure Q3

(c) What is an ASIC? List three types of ASIC.
(5 marks)

(d) What is design partitioning in the ASIC design? List at least 3 partitioning strategies for synthesis.
(5 marks)

Q.4 (a) Correct the errors in the following Verilog code.

Line	Verilog Code
1	module Count(clk, reset, cnt-state)
2	parameter n = 4;
3	input clk, reset;
4	output [n-1:0] cnt-state;
5	
6	always @(posedge clk)
7	if(reset)
8	cnt-state = 4'b0000;
9	else
10	case (cnt-state)
11	begin
12	4'b0000:cnt-state = 4'b0001;
13	4'b0001:cnt-state = 4'b0010;
14	4'b0010:
15	4'b0011:cnt-state = 4'b0100;
16	end;
17	end;
18	endmodule;

(6 marks)

(b) Draw the schematic for the following Verilog code.

```
module exam_Q4(out, in1, in2, sel);
    input in1, in2, sel;
    output out;

    AND U1 (a,in1, sel_b);
    AND U2 (b,in2,sel);
    NOT U3 (sel_b, sel);
    OR U4(out,a,b);

endmodule
```

(5 marks)

(Q4 continues on page 6.)

Q.4 (c) Given the following conditions for the circuit shown in Figure Q4.
The worst delay for circuit block U1 is 3ns. The setup times for FF1 and FF2 are 1ns. T_{CLK_Q} for FF1 and FF2 are 0.8ns.

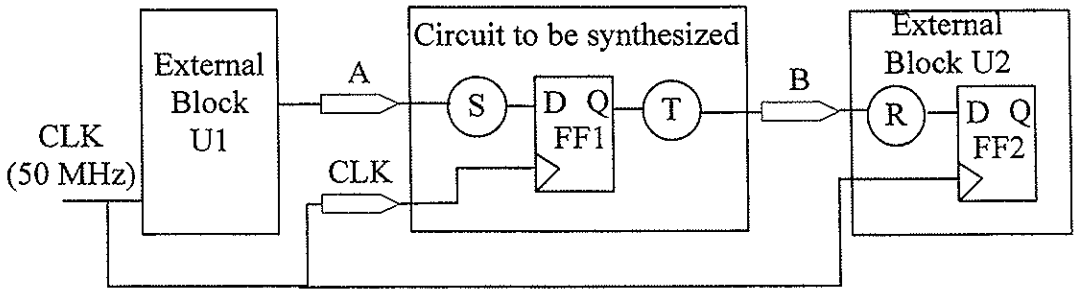

Figure Q4

(i) Write a DC script to constrain the circuit blocks S and T.

(5 marks)

(ii) What is the maximum delay for circuit block S if there is a clock uncertainty of 0.5ns?

(3 marks)

(ii) What is the maximum delay for circuit block T?

(3 marks)

(iii) What is the minimum delay for the circuit block S if the hold time for FF1 is 2ns and minimum external circuit delay is 1 ns? Assume that there is no clock uncertainty.

(3 marks)

END OF PAPER