Tutorial

(1) Try layout of 2-input and 3-input NOR gate. Only one layer of metal is allowed. Use stick diagram and a dot paper. Here are design rules to be used stated in simple English. Obey all λ based design rules. Use a scale of 2λ = 1 dot spacing or less and conform to standard colour codes. The standard colour codes are brown for n-well, black for contact, blue for the only metal layer, red for polysilicon, green for n-type source-drain (NSD) and purple for p-type source-drain (PSD). Choose device dimensions of W = 4λ and L = 2λ for all devices. In the λ based design rules, the n-well coverage of PSD is 3λ, the unconnected PSD-NSD spacing is 8λ, the minimum dimension/spacing of metal, poly, NSD, PSD and contact is 2λ, the coverage of contact by connecting layers is λ on all sides, the poly extension beyond NSD/PSD is 2λ and poly to NSD/PSD contact spacing is 2λ.

(2) For analytic delay and fall time derivation in the CMOS inverter, model is modified to include inversion charge distribution effects. The new model is specified in the equation below. Derive the delay and fall time expressions using this model. Check your results when δ is zero by comparing with the expressions in the notes.

$$I_D = 0 \qquad \text{for } V_{GS} \le V_T$$

$$I_D = \frac{W}{L}\mu C_{ox}\left[(V_{GS} - V_T)V_{DS} - \frac{1}{2}(1+\delta)V_{DS}^2\right]$$

$$\text{for } V_{GS} > V_T,\ V_{DS} \le V_{DS}'$$

$$I_D = \frac{W}{L}\mu C_{ox}\left[\frac{(V_{GS} - V_T)^2}{2(1+\delta)}\right]$$

$$\text{for } V_{GS} > V_T,\ V_{DS} \ge V_{DS}'$$

$$\text{where } V_{DS}' = \frac{(V_{GS} - V_T)}{(1+\delta)},$$

and δ is determined by the inversion charge distribution in the channel.

(3) An inverter is driving a load of 100fF. Use simple formula of delay $= t_{d1} + t_{d2} = \frac{1.61C_L}{\beta_n V_{DD}}$ for calculation. For 65nm technology, μC_{ox} = 1.2mA/V^2 and

power voltage = 1.2V. Find W and L so that the delay is 10ps. What is the intrinsic capacitance that will add to the load if one uses this W and L? What will be the capacitance at the input now?

(4) Implement C_k and S_k in CMOS technology. You can output inverted functions for ease and there is no need to show inverter.

$C_k = (A_k + B_k)C_{k-1} + A_kB_k$

$S_k = \overline{C_k}(A_k + B_k + C_{k-1}) + A_kB_kC_{k-1}$