EE4415 Tutorial for Chapter 2

Q1.

The ASIC design is mostly based on digital standard cells. What of the following statement describes an ASIC design flow?

(a) Design entry ->simulation->logic synthesis->clock tree generation->floor planning->post-layout simulation-> routing->circuit extraction->simulation.
(b) Design entry->logic synthesis->optimization->simulation->partitioning->layout->post-layout simulation->go back to design entry for further optimization.
(c) System level design->RTL coding->simulation->logic synthesis->design for test->partitioning->floor planning and placement->routing->circuit extraction->post-layout simulation.
(d) System level design->HDL coding->translation->optimization->mapping->partitioning->flooring planning->placement->routing->post-layout simulation.
(e) None of the above.

Q2.

What steps are involved in Synthesis using Design Compiler ?

(a) Syntax checking->mapping to GTech->optimization.
(b) Translation ->constrain the design->mapping
(c) Translation -> optimization->mapping
(d) Read in the file->convert HDL code to circuit->constrain the design
(e) None of the above.

Q3.

Most of digital synthesis is done by an Electronic Design Automation (EDA) tool such as Design Compiler (DC) from Synopsys. What of the following statement is true with regarding to DC?

(a) The quality of RTL code is not important as the DC can help optimize the circuit.
(b) The RTL code can be written by any available Verilog statement as the DC is capable of translating them into circuits.
(c) Both synchronous and asynchronous circuits can be synthesized by the DC.
(d) DC is capable to handle circuits with very large number of gates, so there is no need to partition the circuits.
(e) None of the above is true.