NATIONAL UNIVERSITY OF SINGAPORE

EXAMINATION FOR

(Semester I: 2010/2011)

EE2007 – MICROPROCESSOR SYSTEMS

November/December 2010 - Time Allowed: 2 Hours

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **FOUR** (4) questions and comprises **NINE** (9) printed pages. Selected information from the necessary data sheets is provided at the end of each question.

2. Answer all **FOUR** (4) questions. All questions carry equal marks.

3. This is a CLOSED BOOK examination.

4. Programmable calculators are NOT allowed.

SECTION A.
Q.1

(a)

(i) A K-bit microprocessor can access no more than 2^K byte locations. Choose one of the following: (a) True (b) False (c) Insufficient information (d) Partly true _____

(ii) A CPU with 24 address lines can access _____Megabytes of memory.

(iii) Let CS = 1500 H. If IP currently points to the physical address 15230 H, then IP is loaded with _____ H.

(iv) What is the result of the arithmetic operation? Indicate the status of the CF, AF, ZF and SF flags after the execution of the arithmetic instruction.

```
MOV AL, 9CH
MOV DH, 64H
ADD AL, DH
```

(v) A data-byte is received from a hardware port whose address is 89H. What will be the most common instruction you will use to detect if the bit position 3 is a '1' in the received data-byte?

(10 marks)

(Q.1 continues on Page 3)

(b) Write an assembly code to determine the largest number from an unordered array of sixteen one-byte numbers stored in an array NUMS from an offset address 0500H.

(i) Describe the logic behind your design. You may use a flow-chart or clearly describe in words.

(5 Marks)

(ii) Write only the code that implements your logic. You may assume that data segment and the required data are all defined. You need not refer to any interrupts.

(6 Marks)

(iii) Describe clearly in a step-by-step manner how you would implement your logic if you wish to write it as a procedure. There is no need to rewrite your code.

(4 marks)

Q.2

(a)

(i) Let the current contents of CX = FFFF H and the CF = 1. Now, after the execution of 'INC CX' instruction, the contents of CX and CF would be _____ and _____, respectively.

(ii) A 16-bit microprocessor with 20-bit address lines can access more memory locations than a 20-bit microprocessor with 16-bit address lines. (True/False)? _____

(iii) The interrupt pointers (CS and IP addresses) of the INT type **N** can be obtained from locations _____ through _____, respectively.

(iv) Consider a statement TABLE DB 100 DUP(0,100DUP(1,2),0,3). Number of bytes reserved would be _____.

(v) Assume the following: DS=4500, SS=2000, BX = 2100, DI=8500, BP = 7814, AX = 2512. Show the exact physical memory location where AX is stored after each of the following instructions is executed. All values re in hex.

(1) MOV [BX]+20, AX
(2) MOV [DI] +4, AX
(3) MOV [BP]+12,AX

(10 Marks)

(b) Write a simple code sequence to generate a delay of ***10 minutes*** using an 8086 system that runs on ***10MHz*** frequency. Assume that the MOV, DEC / INC, and NOP instructions take **4, 2, and 3 cycles** respectively. Also, assume that all jump instructions take **16 cycles.**

(i) First show a basic code sequence that generates a certain amount of delay. This depends on your code. What is the number of clock cycles required for executing your basic code once?

(5 Marks)

(ii) Use your basic code designed above in Q.2 (b)(i) in generating ***10 minutes*** delay. Show only the part of the code that implements your logic to generate the required delay. You may assume any other required data.

(10 Marks)

SECTION B.

Q.3

(a)

(i) A modern processor has a 32-bit data bus. In this system, _____ banks of memory chips will be needed to fully exploit the 32-bit data bus.

(ii) The first 8 bits of data bus and address bus of 8086/8088 processor are shared for the reason of _____.

(iii) We can use bit 2 in port B of an 8255 chip to control a LED light in the Bit/Set Reset (BSR) mode. Choose one of the following: (a) True (b) False (c) Insufficient information (d) Partly true _____.

(iv) What is the BHE\ value when an 8086 processor executes the following operation? _____.

```
MOV AL, 28H
MOV [4001H], AL
```

(v) A boot sector is the first piece of code that will be stored in a ROM and executed by a processor. Choose one of the following: (a) True (b) False (c) Insufficient information (d) Partly true _____.

(10 marks)

(Q.3 continues on Page 6)

(b)

We are building a small 8088 microprocessor system. The system uses the following memory chips and peripherals: one 8K*8 ROM chip, one 8K*8 RAM chip, one 8250 UART chip, and one 8255 programmable peripheral interface chip.

(i) Draw the memory and I/O address maps for all the memory and peripheral chips used in the system. We use the isolated memory and I/O address map. Assume the base address for the peripheral chips is 100H and all the peripheral chips are mapped to a continuous address range. The order of peripheral chips in this address map should be 8250 and 8255, from the lower address to the higher address. (Hints: 8250 needs 8 I/O addresses, and 8255 needs 4 I/O addresses).

(7 marks)

(ii) Based on the address maps from your answer in Q.3b(i), find out the logic function of the chip select signal CS\ for each of the memory and peripheral chips, respectively.

(8 marks)

Q.4

(a)

(i) Assume the starting address of the interrupt vector for IRQ_3 input is 0000H:002CH, the ICW2 register of 8259 Programmable Interrupt Controller is set to the value of _____.

(ii) Both software interrupts and hardware interrupts need to use the 8259 chip ICW2 register. Choose one of the following: (a) True (b) False (c) Insufficient information (d) Partly true _____.

(iii) Pipelining improves only the throughput, but not the latency of a system. Choose one of the following: (a) True (b) False (c) Insufficient information (d) Partly true _____.

(iv) A _____ way set associative cache will have a 75% probability for a cache block in a cache set not to be replaced in a cache replacement operation.

(v) Rotating priority is not as fair as the random priority scheme in DMA operations. Choose one of the following: (a) True (b) False (c) Insufficient information (d) Partly true _____.

(10 marks)

(Q.4 continues on Page 8)

(b)

(i) Find the port addresses for ICW1-ICW4 and OCW1- OCW3 if chip select signal CS\ of 8259 is activated by A7-A1= 0010010.

(3 marks)

(ii) Calculate the values for Initialization Command Words (ICWs) ICW_1-ICW_4 that you would use to initialize an 8259A for the following mode: single, level triggered; only one 8259A; 8088/8086 system; IR2 is assigned "INT 52H"; in slave buffered mode with normal EOI and not in special fully nested mode. The bit definitions for ICW_1-ICW_4 are shown in Figure 4.b1- Figure 4.b4.

(8 marks)

(iii) Write a program segment to initialize the 8259 using the port addresses calculated from Q.4b(i) and the ICW values decided from Q.4b(ii).

(4 marks)

(Q.4 is continued on Page 9)

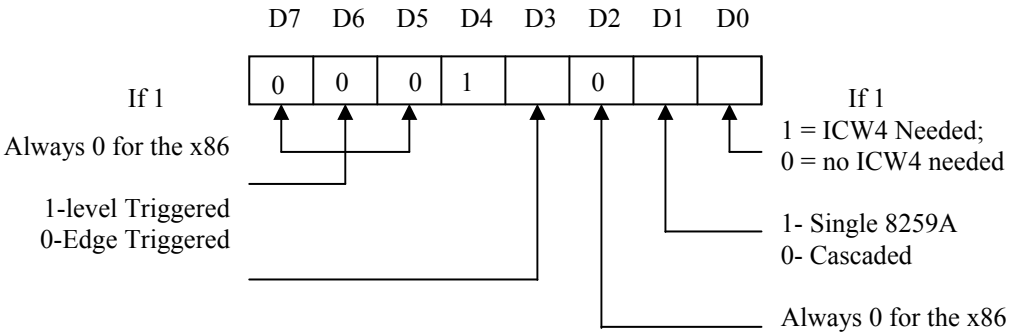

Figure 4.b1: ICW_1

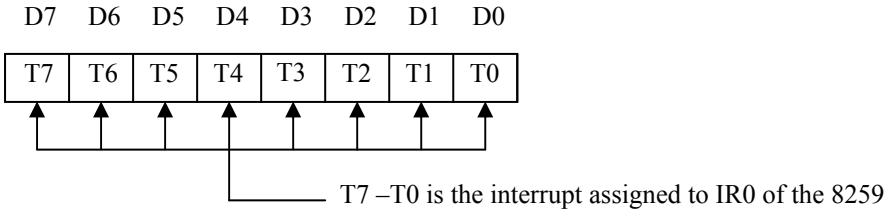

Figure 4.b2: ICW_2

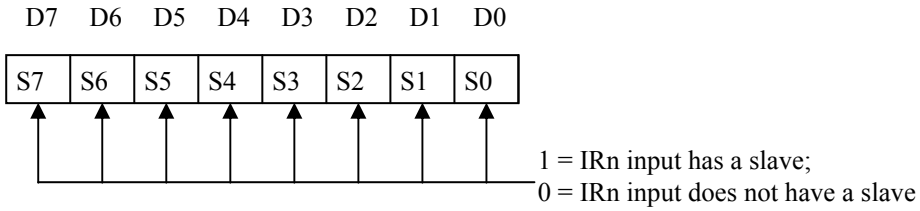

Figure 4.b3: ICW_3

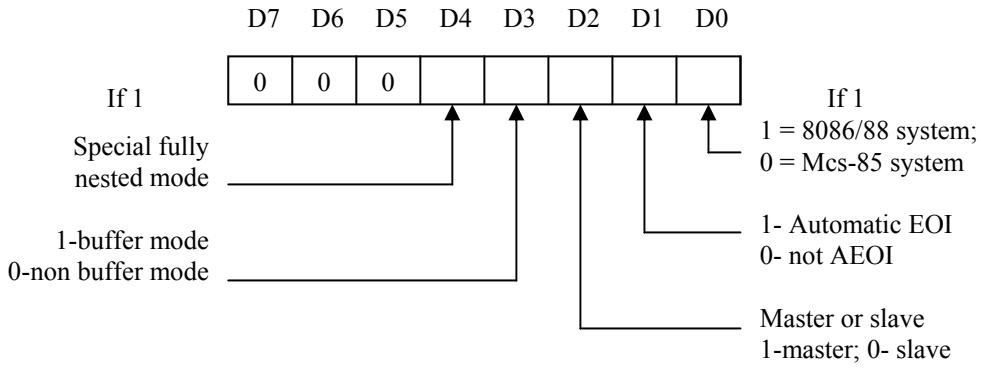

Figure 4.b4: ICW_4

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