**NATIONAL UNIVERSITY OF SINGAPORE**

**EXAMINATION FOR**

(Semester II: 2004/2005)

**EE4415 – INTEGRATED DIGITAL DESIGN**

April/May 2005 - Time Allowed: 2 Hours

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INSTRUCTIONS TO CANDIDATES:

1. This paper contains **Four** (4) questions and comprises **FIVE** (5) printed pages.
2. Answer all questions.
3. All questions carry equal marks.
4. This is a CLOSED BOOK examination
5. Take $\mu_0 = 4\pi \times 10^{-7}\ H/m$
   $\varepsilon_0 = 8.85 \times 10^{-12}\ F/m$

Q.1 Consider the inverter circuit shown in Fig. Q1.1 where the voltage waveform shown in Fig. Q1.2 is applied to input $V_i$.

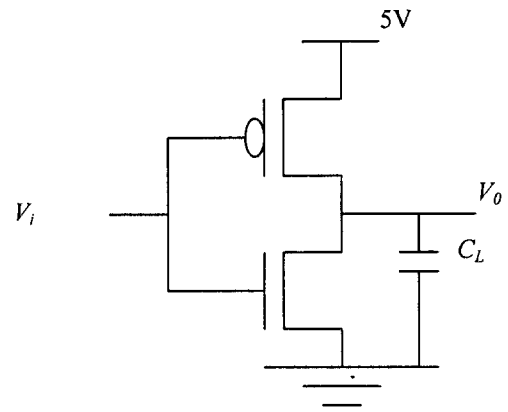


Fig. Q1.1


Fig. Q1.2

The waveform shown in Fig. Q1.2 has a 5V step at $t$=0. $V_i$ is 5V for $t < 0$ and stays constant at 0V for $t > 0$. Assume that the subthreshold currents for all the devices in Fig. Q1.1 are zero. For the devices shown in Fig. Q1.1, $V_{GS}$ and $V_{DS}$ are the gate to source and drain to source voltages, respectively. Furthermore, the drain current $I_d$ in the linear and saturation regions for both the devices is given respectively by

$$I_d = \beta[(V_{GS} - V_T)V_{DS} - 0.6V_{DS}^2] \quad \text{linear region } (|V_{GS}| \geq |V_T|, |V_{DS}| \leq |V_{dsat}|),$$

$$I_d = \frac{\beta(V_{GS} - V_T)^2}{2.4} \quad \text{saturation region } (|V_{GS}| \geq |V_T|, |V_{DS}| \geq |V_{dsat}|),$$

$$V_{dsat} = \frac{(V_{GS} - V_T)}{1.2},$$

where the magnitude of the threshold voltage $V_T$ = 1V for both devices. With the help of this information, derive an expression for the time for the output $V_0$ to rise from 0.2V to 4.8V in terms of the model parameter $\beta$ and $C_L$. Explain briefly how would this analysis would alter if subthreshold currents are not necessarily zero.

(25 marks)

Q.2 (a) Explain how the read, write operations are performed and storage is achieved using the dynamic random access memory cell shown in Fig Q2.1. Why is this cell dynamic and needs a refresh?

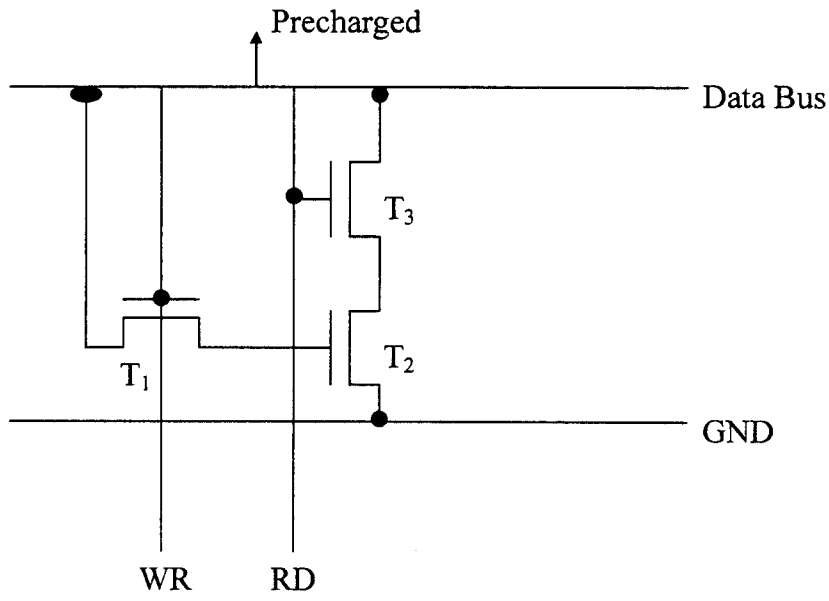


Fig. Q2.1

(7 marks)

(b) In this part of the question, use graph paper and colour pencils to draw a custom layout of the cell shown in Fig. Q2.1, with a built-in ease to route WR, RD, data and ground lines. Include appropriate substrate connection. Obey all $\lambda$ based design rules. Use a scale of $2\lambda$ = 1 cm or less and conform to standard colour codes. The standard colour codes are brown for n-well, black for contact, blue for the only metal layer, red for polysilicon, green for n-type source-drain (NSD) and purple for p-type source-drain (PSD). Choose device dimensions of $W = 4\lambda$ and $L = 2\lambda$ for all devices. In the $\lambda$ based design rules, the n-well coverage of PSD is $3\lambda$, the unconnected PSD-NSD spacing is $8\lambda$, the minimum dimension/spacing of metal, poly, NSD, PSD and contact is $2\lambda$, the coverage of contact by connecting layers is $\lambda$ on all sides, the poly extension beyond NSD/PSD is $2\lambda$ and the poly to NSD/PSD contact spacing is $2\lambda$.

(15 marks)

(c) Explain briefly the voltage loss problem that occurs when a single transistor transmission gate is used.

(3 marks)

Q.3 (a) Explain briefly the ion implantation step used in silicon processing and the associated channeling effect.

(6 marks)

(b) Explain briefly the principle behind the operation of carry select adder with the help of a block diagram. Indicate briefly the advantages and disadvantages of this architecture.

(7 marks)

(c) Explain briefly the main steps involved in an application-specific integrated circuits (ASIC) design flow with the help of a block diagram.

(7 marks)

(d) Assume that an ASIC chip is synthesized using the Design Compiler. Explain briefly the steps involved in the logic synthesis and how the design specifications are met.

(5 marks)

Q.4 Given the following design specifications:

| | |
|---|---|
| Clock speed : | 100MHz |
| Voltage : | 1.8V ±0.18V |
| Operating Temperature : | 0°C to 125°C |
| Technology Library : | core_slow.db |
| Operating Conditions Library : | opcon.db |
| Symbol Library : | core.sdb |

(a) Define the following Design Compile library setup variables:
target_library,
link_library,
symbol_library.

(6 marks)

(b) Develop a script in Design Compiler to constrain the circuits, shown in Fig. Q4.2. Assume that the setup requirement for external circuit is 5 ns and the clock of the circuit is 100 MHz with 50% duty cycle.

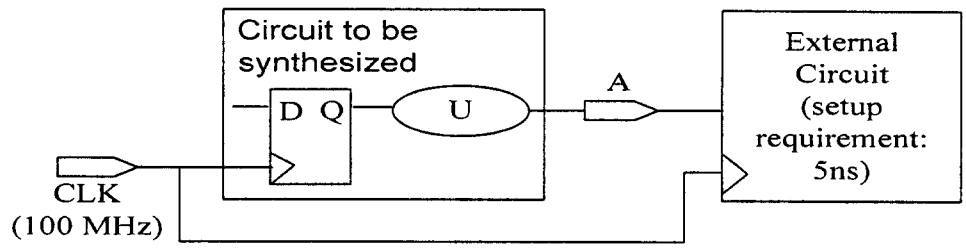


Fig. Q4.2

(6 marks)

**Q.4 is continued on Page 5.**

(c) Listed below is a Verilog code that uses an "*if*" statement to create combinational logic. The synthesized circuit should achieve the following function: outputA=inputC if inputA and inputB are both at logical "1"; outputA is set to high impedance if inputA and inputB are at other logical values. (i) Study the code and determine whether it achieves the desired function. Justify your answer. (ii) Correct the code if there are any errors; (iii) Synthesize the Verilog code into a circuit.

```
module  question_4c (inputA, inputB, inputC, outputA);
input inputA, inputB, inputC;
output outputA;
reg outputA;

always@(inputA or inputB or inputC)
begin
      if (inputA & inputB)
          outputA = inputC;
end
endmodule
```

(13 marks)

**END OF PAPER**