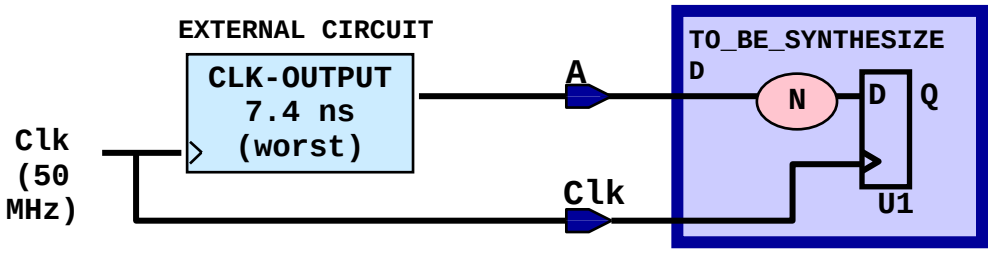
EE4415 Tutorial for Chapter 4

Q1. The circuit shown below is constrained by:

create_clock -period 20 [get_ports Clk]

set_input_delay -max 7.4 -clock Clk [get_ports A]



What is the maximum allowed time for circuit N?

(a) 7.4 ns, (b) 12.6 ns, (c) 20 ns, (d) none of the above.

Q2. Consider the following code.

```
always@(posedge clock)
    C <= A+B;
```

If it is synthesized with the following constraints

```
create_clock -period 10 -waveform {0 5} clock
set_clock_uncertainty –setup 1.0 clock
set_input_delay –max 2.0 -clock clock [remove_from_collection \
[all_inputs] [get_ports clock]]
```

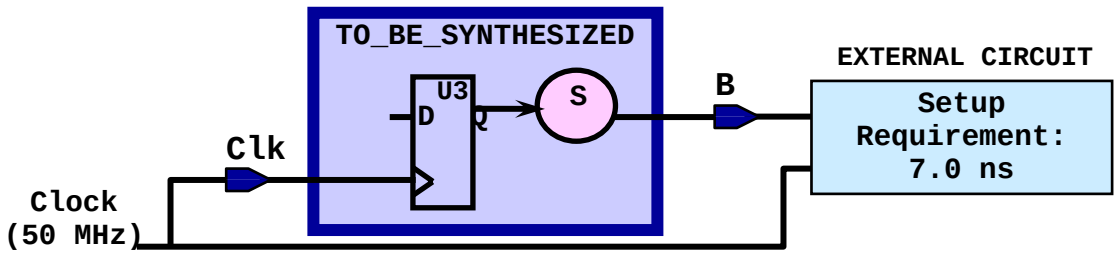
then what is the maximum allowed delay for the logic A+B if the setup time for the flip-flops with output C is 1 ns?

(a) A. 1 ns
(b) B. 4 ns
(c) C. 6 ns
(d) D. 10 ns
(e) E. None of the above

Q3. The circuit shown below is constrained by:

create_clock -period 20 [get_ports Clk]

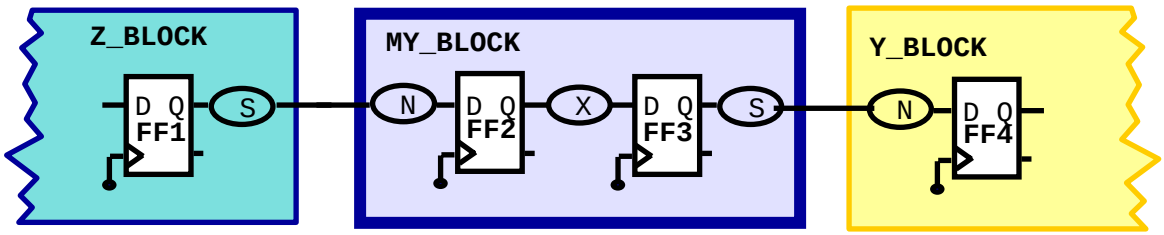
set_output_delay -max 7.0 -clock Clk [get_ports B]



What is the maximum allowed time for circuit S?

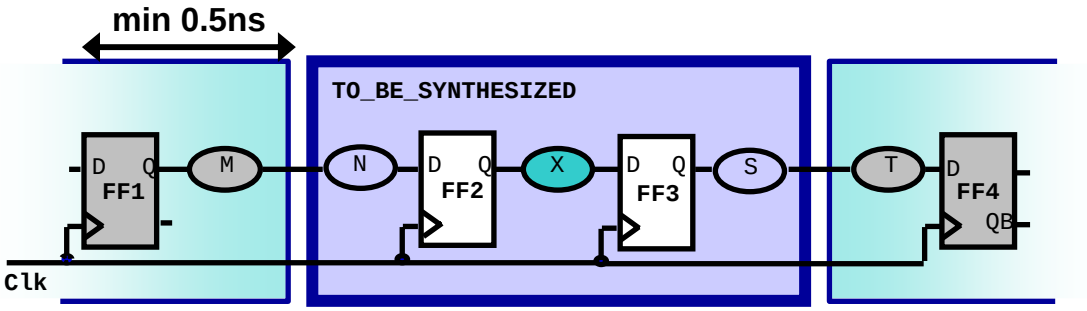
(a) 20 ns, (b) 13 ns, (c) 7 ns, (d) none of the above.

Q4. In the circuit below, the clock period is 20 ns. What are the time budgets for circuits N, X, and S? (Assume delays for FF1, FF2, FF3, and FF4 are zero).



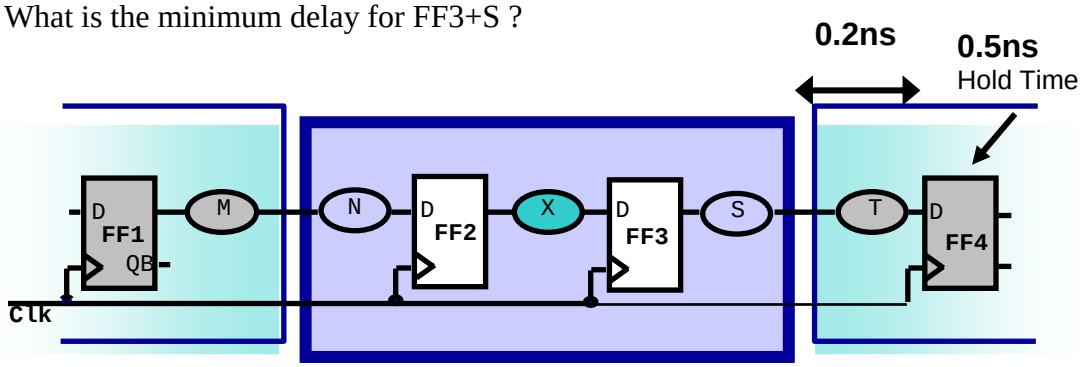
(a) T_N= 12ns, T_X=12ns, T_S= 12ns; (b) T_N= 8ns, T_X=12ns, T_S= 8ns; (c) T_N= 8ns, T_X=20ns, T_S= 8ns; (d) Can't decide.

Q5. Assume the clock period is 10ns, the fastest arrival time for circuit M and FF1 is 0.5ns. What is the minimum delay allowed for N if FF2 has T_{HOLD} = 1ns?



(a) 9.5 ns, (b) 9 ns, (c) 8.5 ns, (d) 1 ns, (e) none of the above.

Q6. In the circuit below, assume the clock period is 5ns and the hold time of FF4 is 0.5ns. What is the minimum delay for FF3+S ?



(a) 4.3ns, (b) 0.5 ns, (c) 0.3 ns, (d) 0.2 ns, (e) none of the above.