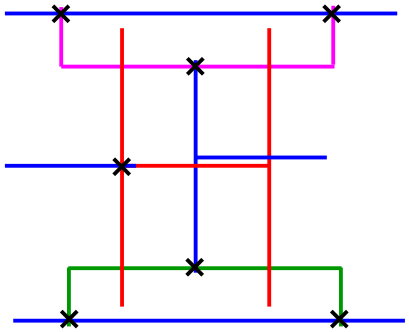
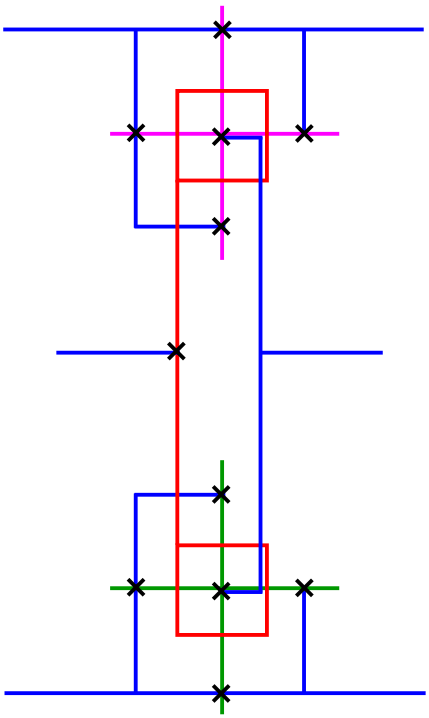
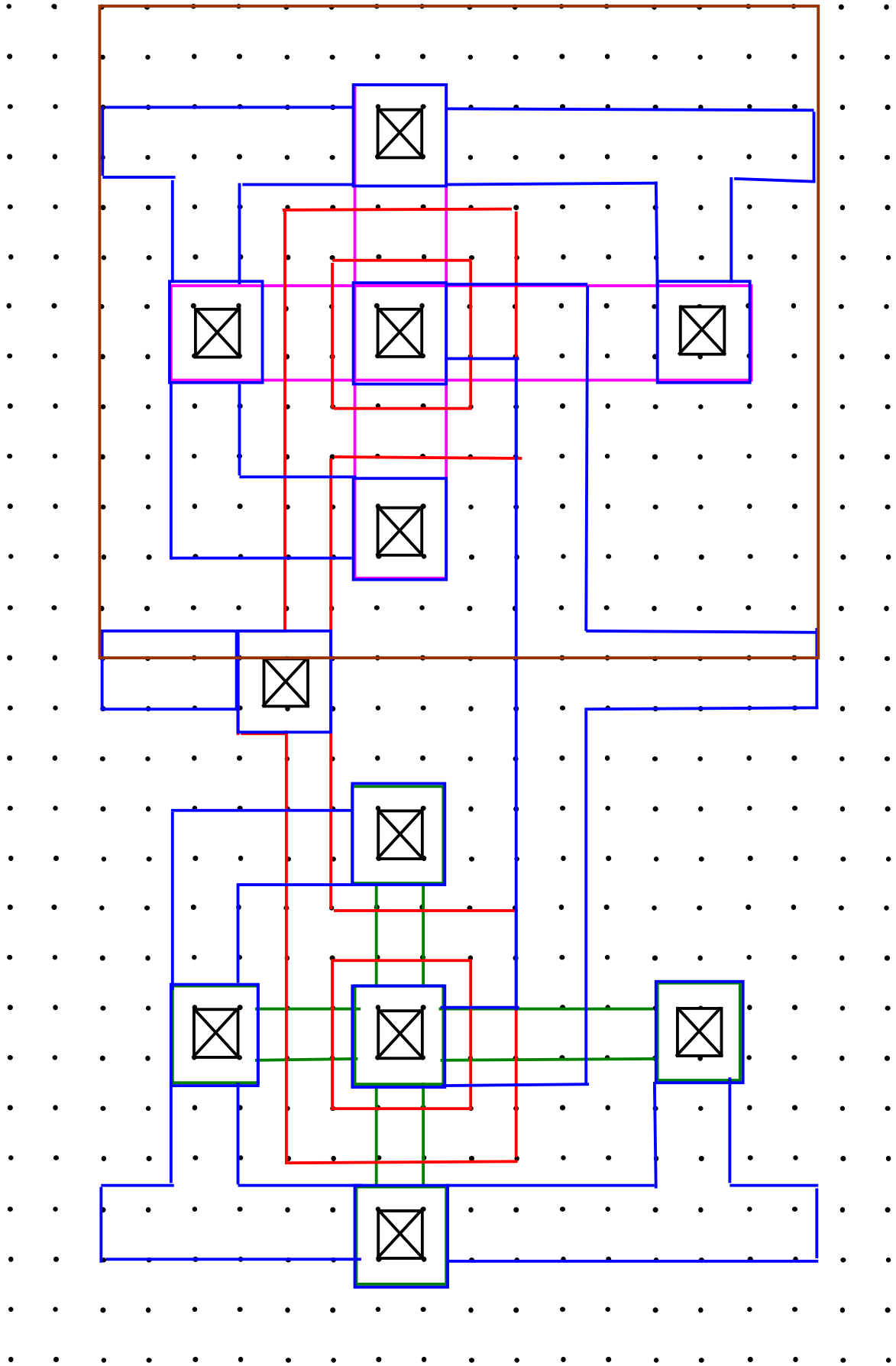
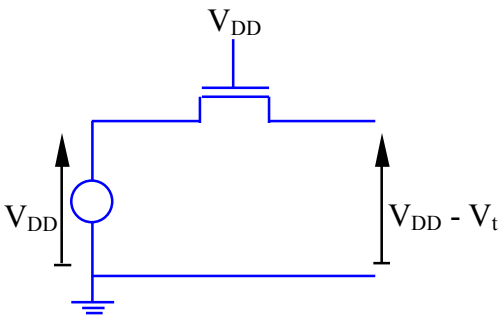
Big inverter



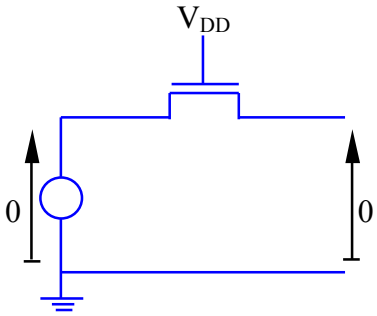




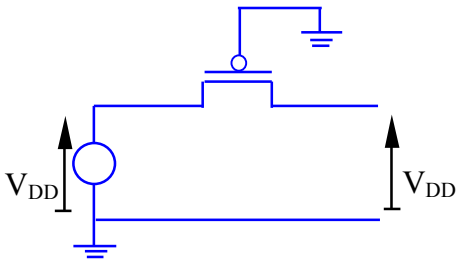
Transmission Gate Logic



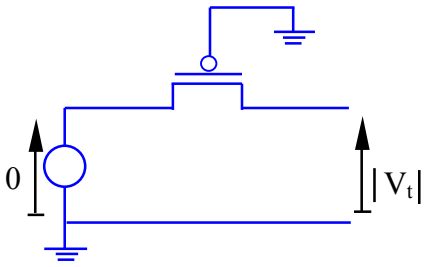
"1" is degraded



"0" is good



"1" is good



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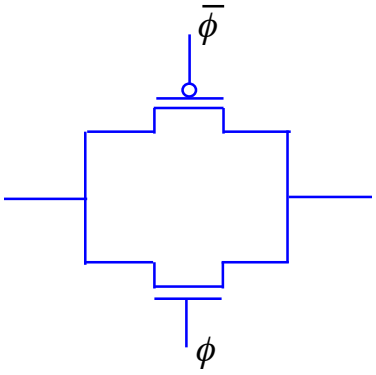
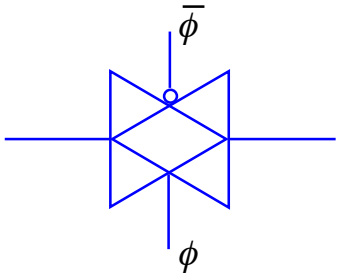
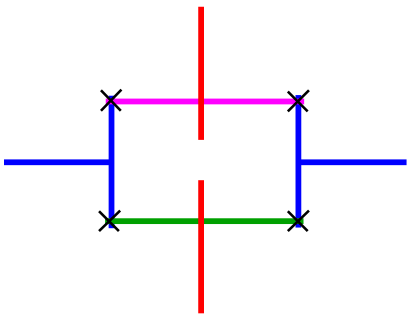
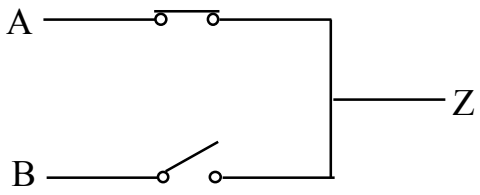
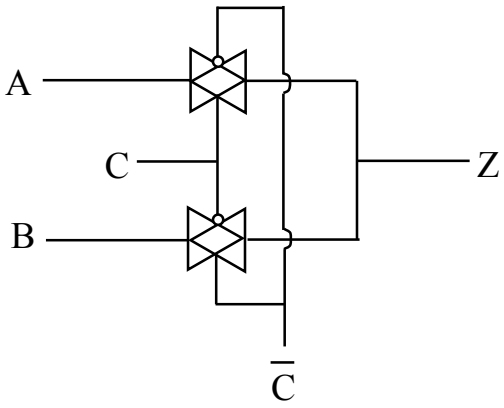


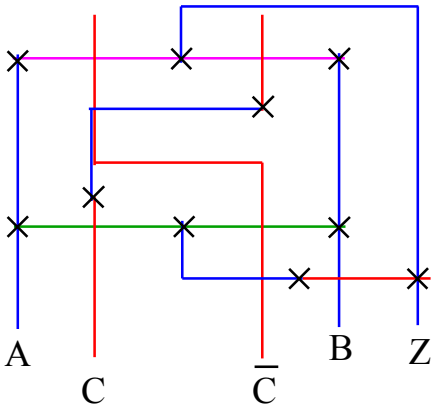


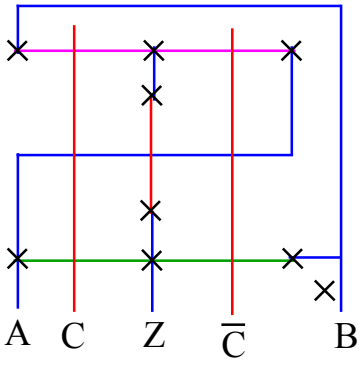


Multiplexer

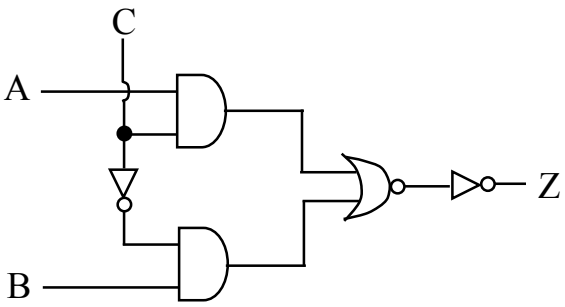








Combinational logic multiplexer



In summary, processing step tolerances, lithography alignment uncertainty and reliability consideration dictate design rule.

The design rules are technology independent and simple.

Any CMOS logic can be implemented by first designing logic zero pull down path with nMOS devices and then construction of pMOS complementary network.

Any circuit implementation layout plan is first done with a stick diagram and then full layout can be done staring from one of the edges.