NATIONAL UNIVERSITY OF SINGAPORE

EXAMINATION FOR

(Semester II: 2005/2006)

EE4415/EE4415E – INTEGRATED DIGITAL DESIGN

April/May 2006 - Time Allowed: 2 Hours

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **Four** (4) questions and comprises **Six** (6) printed pages.
2. Answer all questions.
3. All questions carry equal marks.
4. This is a CLOSED BOOK examination
5. Take $\mu_0 = 4\pi \times 10^{-7}\ H/m$
   $\varepsilon_0 = 8.85 \times 10^{-12}\ F/m$

Q.1 Consider the inverter circuit shown in Figure Q1 where the output voltage is taken at the common drain and the input voltage is applied to the common gate.

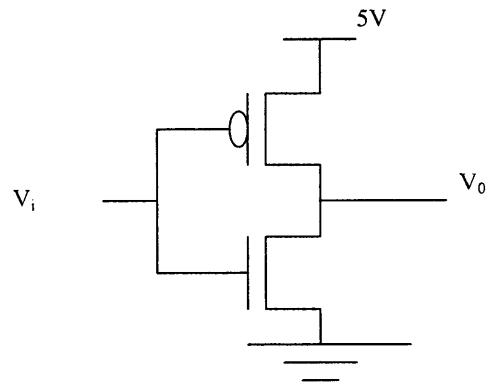

Figure Q1

(a) Indicate five pairs of operating regions the n-channel and p-channel devices go through when the input voltage V_i switches from 0 to 5V. Hence explain a major benefit CMOS technology compared to the other technologies.

(8 marks)

(b) In this part, assume that the subthreshold currents for all the devices in Figure Q1 are zero. For the devices shown in Figure Q1, V_{GS} and V_{DS} are the gate to source and drain to source voltages, respectively. Furthermore, the drain current I_d in the linear and saturation regions for both the devices is given by

$$I_d = \beta[(V_{GS} - V_T)V_{DS} - 0.5V_{DS}^2] \quad \text{linear region } (|V_{GS}| \geq |V_T|, |V_{DS}| \leq |V_{dsat}|),$$

$$I_d = \frac{\beta(V_{GS} - V_T)^2}{2} \quad \text{saturation region } (|V_{GS}| \geq |V_T|, |V_{DS}| \geq |V_{dsat}|),$$

and $V_{dsat} = (V_{GS} - V_T)$,

where the magnitude of the threshold voltage $V_T = 1$V for both devices. Also, β for n-channel and p-channel devices are given by $400\mu A/V^2$ and $100\mu A/V^2$, respectively. With the help of this information and answer of part (a),

(i) Calculate the switching input voltage V_{inv} of the inverter when both devices are in the saturation region.

(ii) Calculate V_o when input assumes values 0.1V above and below the switching voltage calculated in (i).

(iii) Sketch V_o versus V_i plot labeling clearly all accurately calculated values. What additional two input voltages would you choose to improve the accuracy of this plot? Give your reasons briefly.

(17 marks)

Q.2 (a) Explain how the read and write operations are performed, and how storage is achieved using the dynamic random access memory cell shown in Figure Q2. Why is cell dynamic and needs a refresh?

(7 marks)

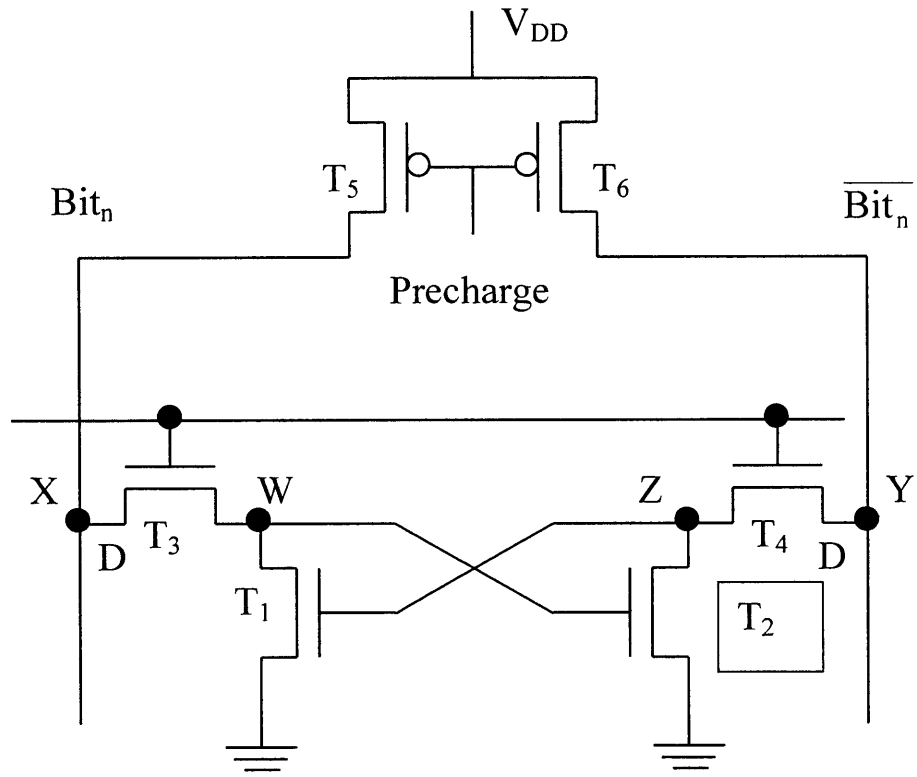

Figure Q2

(b) In this part of the question, use graph paper and colour pencils to draw a custom layout of the RAM cell shown in Figure Q2 without the precharge transistors, with a built-in ease to route common connected gates in polysilicon layer, Bit_n and $\overline{Bit_n}$ and ground lines in the only metal layer. Obey all λ based design rules. Use a scale of $2\lambda = 1$ cm or less and conform to standard colour codes. The standard colour codes are brown for n-well, black for contact, blue for the only metal layer, red for polysilicon, green for n-type source-drain (NSD) and purple for p-type source-drain (PSD). Choose device dimensions of $W = 4\lambda$ and $L = 2\lambda$ for all devices. In the λ based design rules, the n-well coverage of PSD is 3λ, the unconnected PSD-NSD spacing is 8λ, the minimum dimension/spacing of metal, poly, NSD, PSD and contact is 2λ, the coverage of contact by connecting layers is λ on all sides, the poly extension beyond NSD/PSD is 2λ and poly to NSD/PSD contact spacing is 2λ.

(18 marks)

Q.3 (a) Explain briefly the dopant segregation effect in silicon processing.

(4 marks)

Q.3 (b) Explain briefly the principle behind the operation of carry skip adder with the help of a block diagram. Indicate briefly advantages and disadvantages of this architecture.

(9 marks)

Q.3 (c) The modern digital integrated circuit design is based on digital standard cells. A cell based design flow includes logic and physical designs. Draw a cell based design flow that includes the main tasks in logic and physical designs.

(5 marks)

Q.3 (d) Most of digital synthesis is done by an Electronic Design Automation (EDA) tool such as Design Compiler (DC). With the help of a block diagram, explain briefly the operational steps which occur in the DC during synthesis.

(7 marks)

Q.4 (a) A combination logic circuit is shown in Figure Q4a. Given Verilog gate-level primitives "and(output, input_1, input_2, input_3)" and "not(output, input)", develop a Verilog module to describe the circuit.

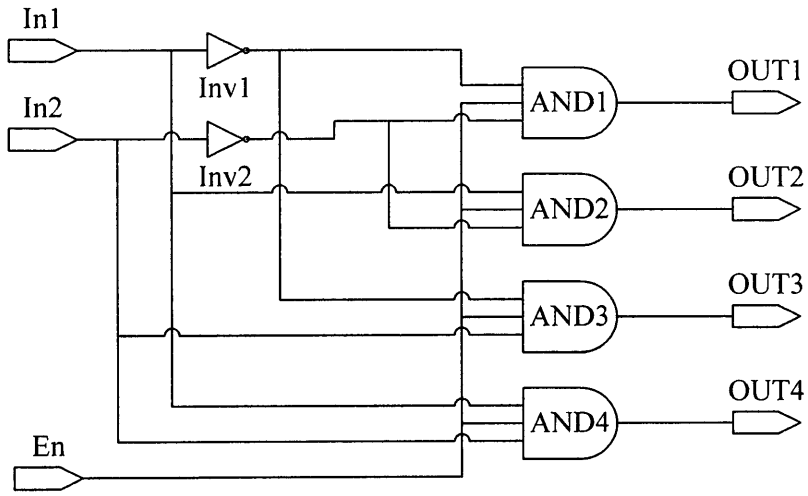

Figure Q4a

(7 marks)

(b) Write a DC script to constrain the setup time of circuits, shown in Figure Q4b. Assume that the clock period is 20ns with 50% duty cycle and skew of 0.1ns.

Q.4 continued on next page

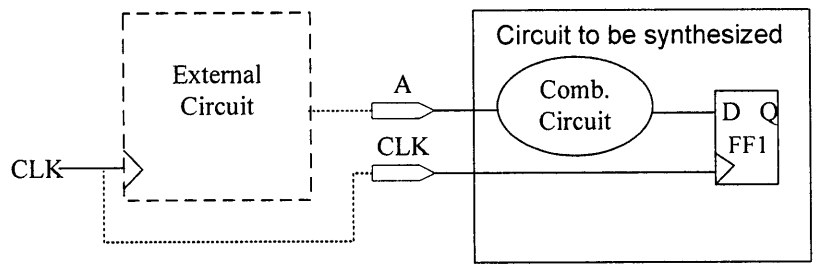

Figure Q4b

(7 marks)

(c) If the flip-flop FF1 in the circuit, shown in Figure Q4b, has a hold time of 1 ns and the fastest arrival time from the external logic to the input port "A" is 0.2ns, what is a minimum delay allowed for the combination circuit?

(5 marks)

(d) Two sections of Verilog statements are given below. Are these two statements functionally equivalent? Justify your answer.

Verilog statement A:

```
module muxA (w, s1, s2, f);
    input [ 1:0] w;
    input s1,s2;
    output f;
    reg f;

    always@(w or s1 or s2)
      begin
        if (s1)
          f <= w[0];
        if (s2)
          f <= w[1];
      end

endmodule
```

Q.4 continued on next page

Verilog statement B:

```
module muxB (w, s, f);
    input [ 1:0] w;
    input s1,s2;
    output f;
    reg f;

    always@(w or s1 or s2)
        if (s1)
          f <= w[0];
        else if (s2)
          f <= w[1];

endmodule
```

(6 marks)

END OF PAPER