NATIONAL UNIVERSITY OF SINGAPORE

EXAMINATION FOR

(Semester II: 2006/2007)

EE4415/EE4415E – INTEGRATED DIGITAL DESIGN

April/May 2007 - Time Allowed: 2 Hours

INSTRUCTIONS TO CANDIDATES:

1. This paper contains **FOUR** (**4**) questions and comprises **SIX** (**6**) printed pages.
2. Answer all questions.
3. All questions carry equal marks.
4. This is a CLOSED BOOK examination
5. Take $\mu_0 = 4\pi \text{ x } 10^{-7}\ H/m$
   $\varepsilon_0 = 8.85 \text{ x } 10^{-12}\ F/m$

Q.1 For both part (a) and (b), assume that the time delay is directly proportional to the load capacitance and inversely proportional to the transistor (W/L).

(a) Consider the inverter circuit shown in Figure Q1a where the output voltage is taken at the common drain and the input voltage is applied to the common gate. There is no external load connected to the inverter. Mr. X simulates this circuits and finds out that the delay at the output is about 20ps. He is not satisfied with this performance. Based on the common knowledge that the circuit delay will improve in tandem with increasing device (W/L) ratios, he increases (W/L) ratio of both transistors by factor of 10. To his surprise, he finds that the delay has only marginally improved. With the help of a simple layout diagram, explain in detail why this is the case.

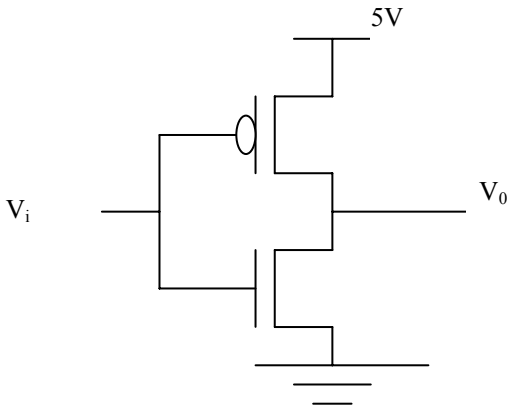

Figure Q1a

(8 marks)

(b) Consider a chain of inverters driving a large load as indicated in Figure Q1b where there are x stages and each inverter β increased by a factor $M^{\frac{1}{x}}$ which automatically raises input capacitive load of a particular stage by the same factor. Input load of the first stage is C. Given that the delay of an inverter with a size parameter β driving a capacitance C is t, derive an expression for the delay of each of the stages shown in Figure Q1b. Hence derive an expression for total delay T at the output and optimum number of stages that minimizes T.

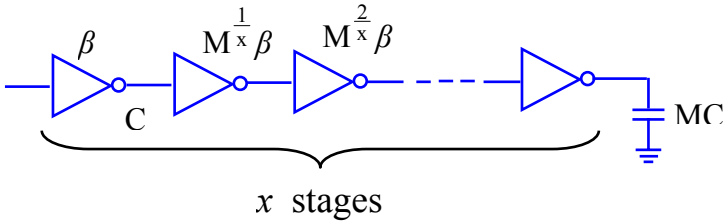

Figure Q1b

(17 marks)

Q.2 Consider a single transistor version of a transmission gate shown in Figure Q2. The input to this gate at drain is driven by an inverter on the left and the output is taken at the right terminal of the device. Clock ϕ is connected to the gate of this device.

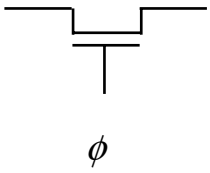

Figure Q2

In this part of the question, use dotted sheet provided and colour pencils to draw a custom layout of the transmission gate shown in Figure Q2 along with the inverter on the left with built in ease to route and power lines. Obey all λ based design rules. Use a scale of 2λ = spacing between dots and conform to standard colour codes. The standard colour codes are brown for n-well, black for contact, blue for the only metal layer, red for polysilicon, green for n-type source-drain (NSD) and purple for p-type source-drain (PSD). Choose device dimensions of W = 4λ and L = 2λ for all devices. In the λ based design rules, the n-well coverage of PSD is 3λ, the unconnected PSD-NSD spacing is 8λ, the minimum dimension/spacing of metal, poly, NSD, PSD and contact is 2λ, the coverage of contact by connecting layers is λ on all sides, the poly extension beyond NSD/PSD is 2λ and poly to NSD/PSD contact spacing is 2λ.

(25 marks)

Q.3 (a) Explain briefly the lithography step in silicon processing.

(5 marks)

Q.3 (b) Explain how read and write operations are performed, and how storage is achieved using the dynamic random access memory cell shown in Figure Q3a. Why is the cell dynamic and needs refresh?

(8 marks)

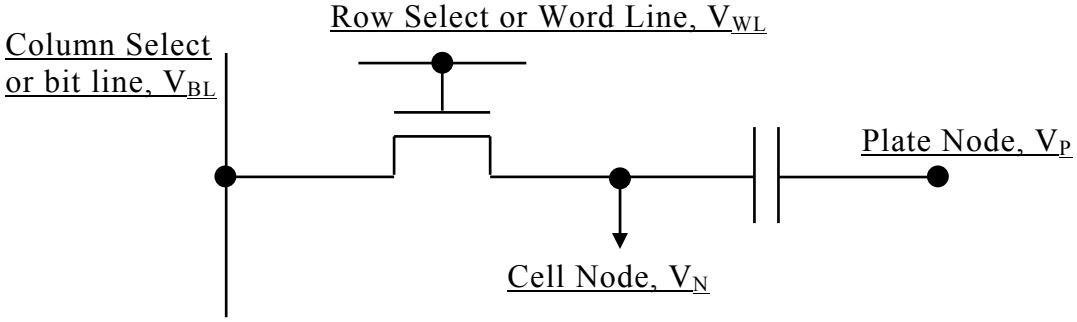

Figure Q3a

(**Q3 continued on next page**)

Q.3 (c) Suppose you are going to compile a design using Synopsys Design Compiler (DC). The design contains two Verilog source files, e.g. top.v and decimation.v. Figure Q3b shows the file structure for the design, where csm018.db and csm018.sdb are technology library files, comb.ddc is a Verilog module required by decimation.v. Generate a DC setup file under directory "project20071" to initialized DC.

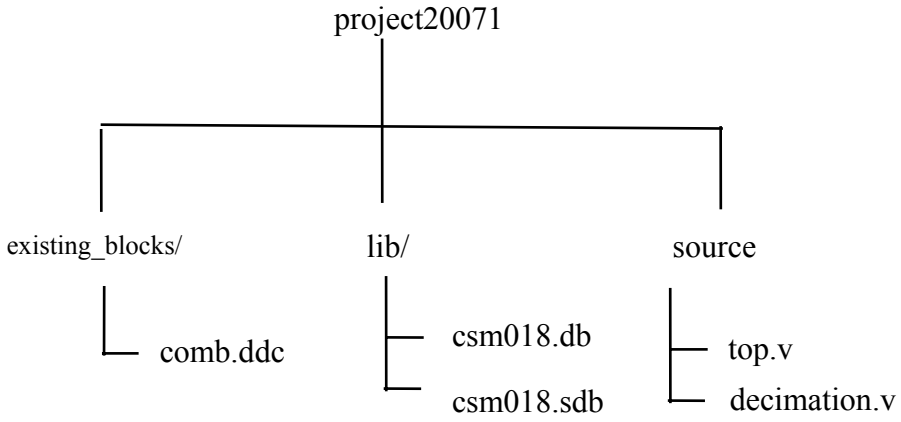

Figure Q3b

(3 marks)

Q.3 (d) What are the main steps involved in DC synthesis?

(3 marks)

Q.3 (e) A Verilog module is listed below.

```
module comb_logic(in_1,in_2,out);
  input in_1, in_2;
  output out;
  wire a, b;

  nand U1 (a,in_1, in_2);
  or U2 (out, a, b);
  not U3 (.inv_out(b), .inv_in(in_2));

endmodule
```

Implement the circuit according to the given code and indicate design, cells, ports, pins, and nets on your circuit.

(6 marks)

Q.4 (a) Assume that the clock skew and clock network latency from CLK port to FF1 in the circuit shown in Figure Q4a are 0.5 ns and 1 ns, respectively.

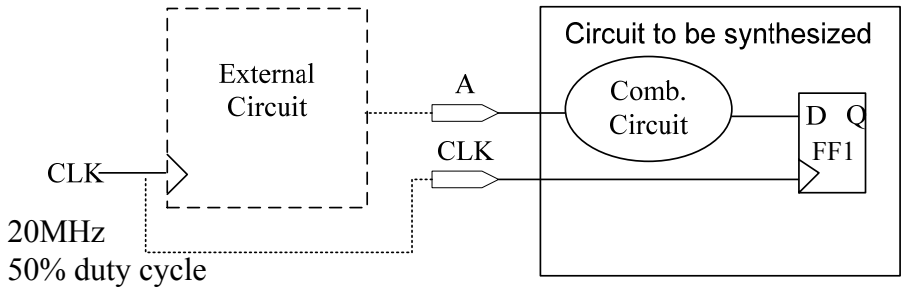

Figure Q4a

(i) Write a DC script to constrain the setup time of Comb Circuit. Assume that the maximum external circuit delay is 25 ns.

(5 marks)

(ii) What is the maximum delay for Comb Circuit if the setup time for FF1 is 5 ns?

(3 marks)

(iii) What is the minimum delay for Comb Circuit if the hold time for FF1 is 5 ns and minimum external circuit delay is 2 ns,

(3 marks)

(iv) How to constrain the setup time of Comb Circuit if the delay of the external circuit is unknown? In this case, what is the maximum delay for the Comb Circuit if setup time for FF1 is 5 ns?

(4 marks)

(b) A Verilog module, addition.v, is given below. What the values of in1, in2, in3, out1 and out2 at time units 5, 15 and 25, respectively, if it is simulated by a Verilog simulator?

```
module addition;
reg in1,in2, in3;
reg [3:0]out1,out2;
   initial
   begin
     # 0 in1=0;
     # 0 in2=0;
     # 0 in3=0;
     # 10 in1 = 1;
     # 10 in2 = 1;
     # 10 $finish;
   end
```

(**Q4(b) continued on next page)**

```
   always @(in1 or in2 or in3)
   begin
      out1 <= in1+in2;
      out2 <= out1+in3;
    end

initial
$monitor ("%d, in1=%b, in2=%b, in3=%b,out1=%b, out2=%b",
$time, in1,in2,in3,out1,out2);

endmodule
```

(10 marks)

END OF PAPER