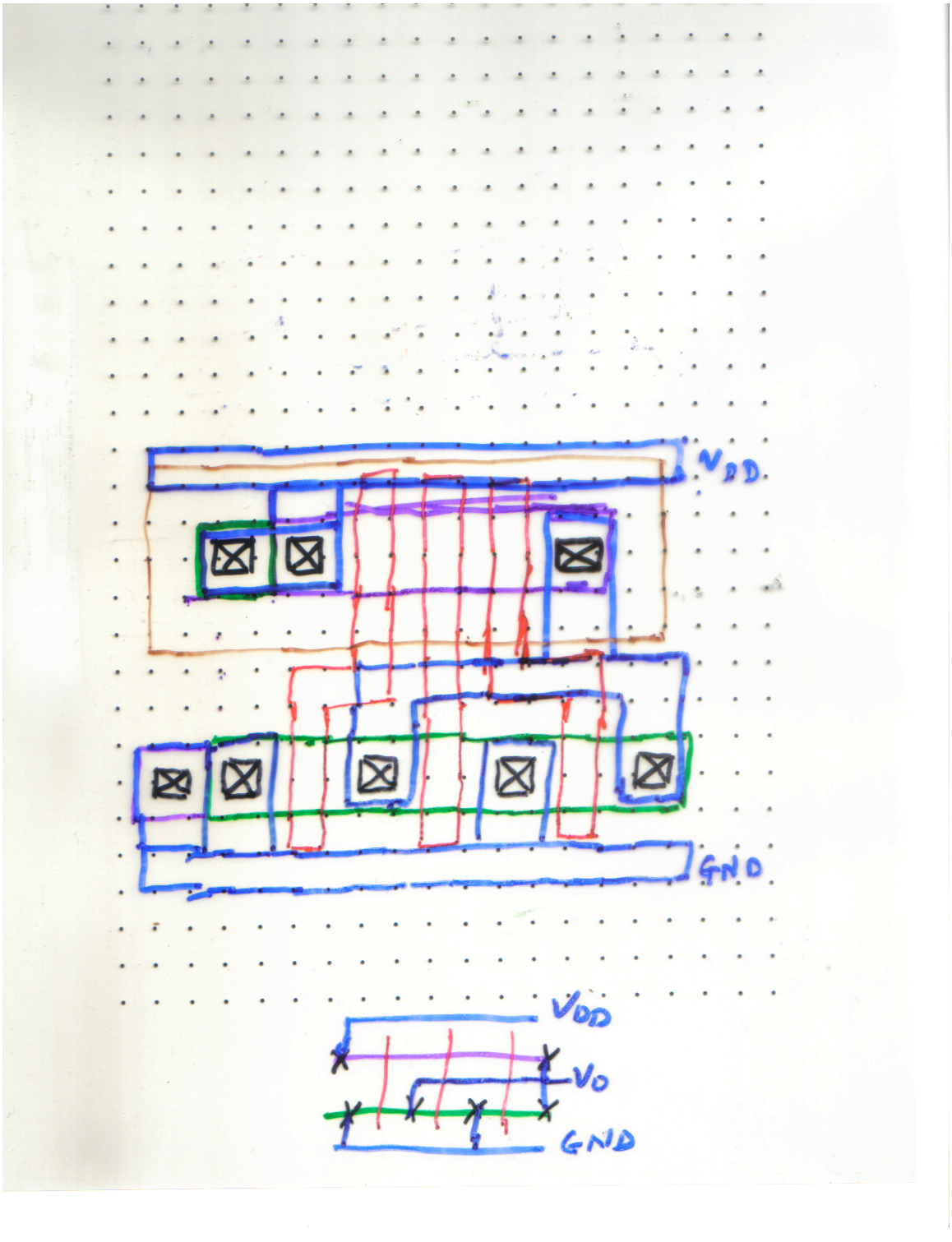
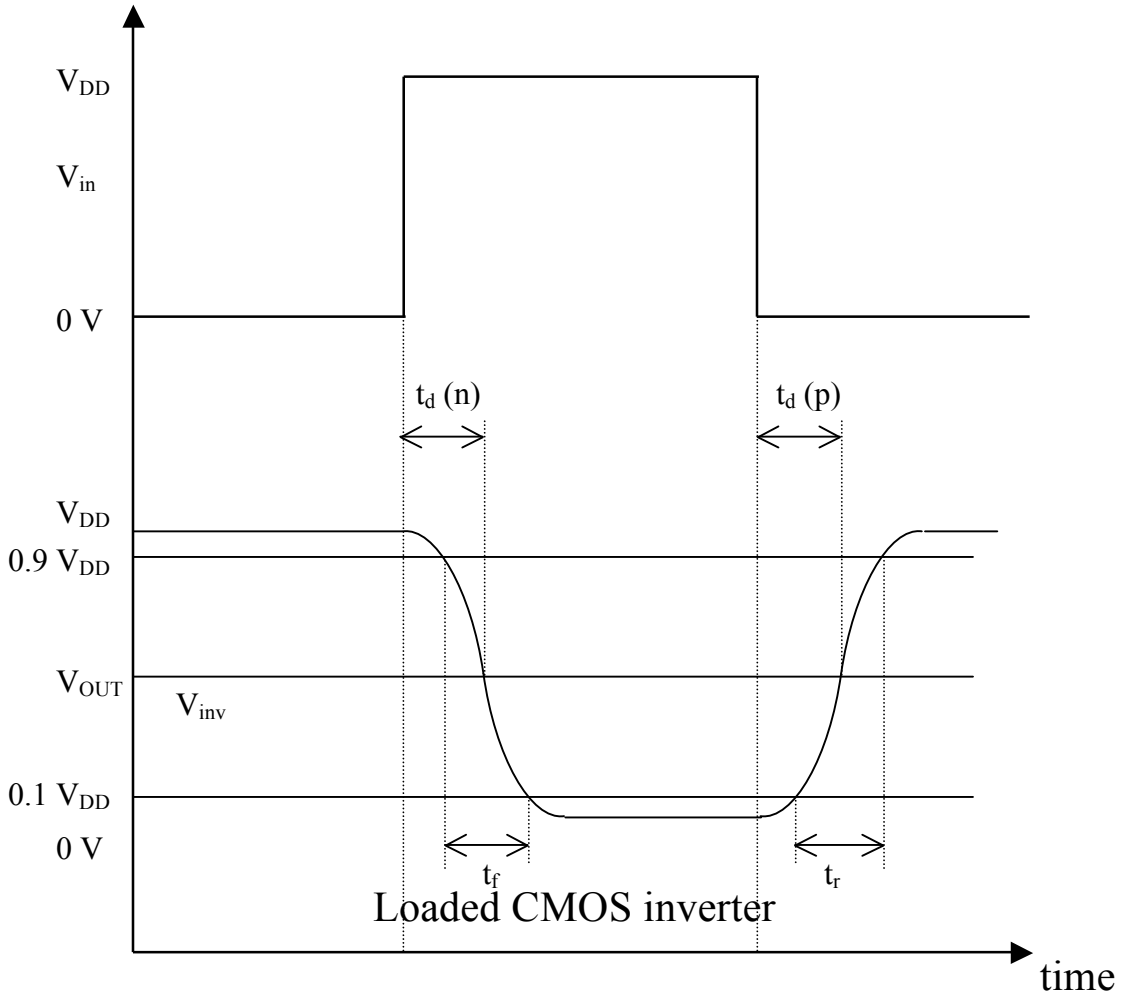
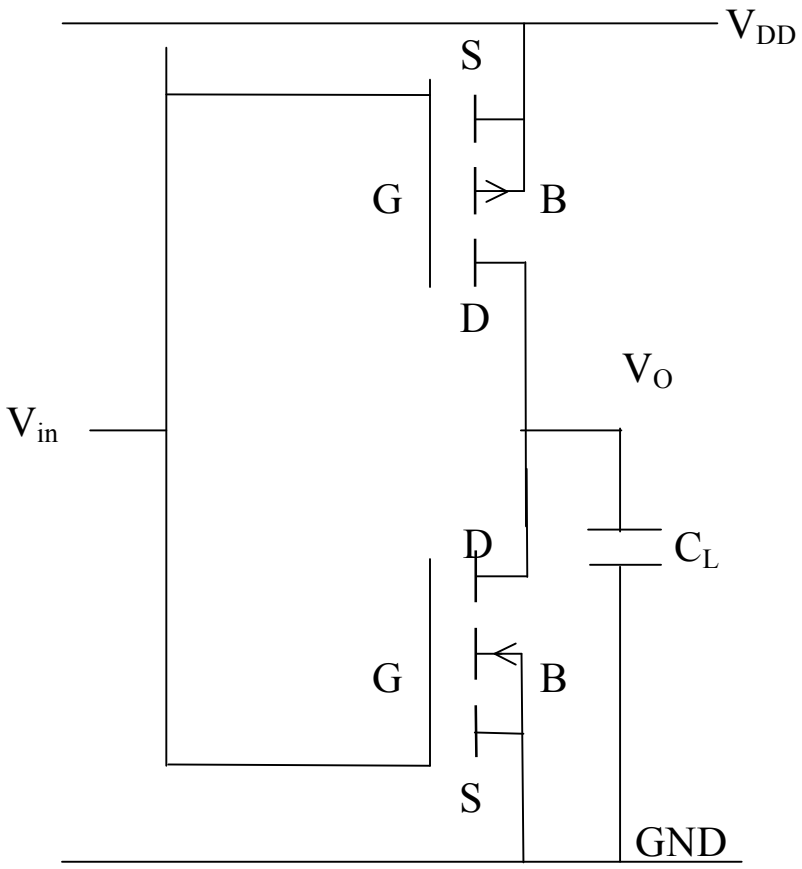
Problem 1: 3 input NOR layout



Problem 2:

Normally, the inverter has to drive a load. This could be an external load or loading from inverter's own diffusion capacitance, capacitance from gates driven or interconnect capacitance. You already know the recipes to find and estimate these capacitances. Due to the presence of this load, a step edge pulse at the input will have rounded edges at the output. The timing quantities fall time t_f , rise time t_r and delay time t_d are defined in the next figure like in the notes.





Initially, when input switches from 0 to V_{DD}, n transistor is turned on as $V_{DS} = V_{DD}$ and $V_{GSn} = V_{DD} > V_{tn}$ for it. At $V_{in} = V_{DD}$, p channel transistor is totally off. Hence the n-channel device is pulling the output down.

The n-channel device is in saturation if

$$V_{DS} \geq (V_{GSn} - V_{tn}) / (1 + \delta_n),$$

i.e.
$$V_O \geq \frac{V_{DD} - V_{tn}}{1 + \delta_n}$$

Hence for output voltages from V_{DD} to $(V_{DD} - V_{tn}) / (1 + \delta_n)$, the n-channel device is in saturation.

For the capacitor this forms the discharge current. If it takes time t_{d1} for the output voltage to fall from V_{DD} to $(V_{DD} - V_{tn}) / (1 + \delta_n)$, charge balancing yields

$$\text{charge } \Delta Q = t_{d1} \bullet I_{ds} = C_L \Delta V = \frac{C_L (V_{DD} \delta_n + V_{tn})}{1 + \delta_n},$$

as the change in capacitor voltage is

$$|\Delta V| = V_{DD} - \frac{(V_{DD} - V_{tn})}{1 + \delta_n}$$

$$= \frac{V_{DD}\delta_n + V_{tn}}{1 + \delta_n}$$

$$t_{d1} = \frac{C_L (V_{DD}\delta_n + V_{tn})}{I_{ds} (1 + \delta_n)} = \frac{2 C_L (V_{DD}\delta_n + V_{tn})}{\left(\frac{W_n}{L_n}\right) \mu_n C_{ox} (V_{DD} - V_{tn})^2}$$

after substituting saturation current expression for the n-channel device current.
For typical $V_{tn} = 0.2\ V_{DD}$ and $\delta_n \approx 0$, we have

$$t_{d1} = \frac{2 C_L}{\beta_n} \frac{0.2 V_{DD}}{0.64 V_{DD}^2} = \frac{0.625 C_L}{\beta_n V_{DD}}$$

where $\beta_n = \left(\frac{W_n}{L_n}\right) \mu_n C_{ox}$

For V_O between $\frac{V_{DD} - V_{tn}}{1 + \delta_n}$ and the switching voltage V_{inv}, the n-channel device is in the linear region. Hence the pull down current (linear region n-channel device current) is a function of V_O. Hence we have to integrate incremental delays to get total delay t_{d2} in this region.

$$t_{d2} = -C_L \int_{\frac{V_{DD} - V_{tn}}{1+\delta_n}}^{V_{inv}} \frac{d V_O}{I_{ds}}$$

But for any V_O in this region,

$$I_{ds} = \left(\frac{W_n}{L_n}\right) \mu_n C_{ox} V_O \left[(V_{DD} - V_{tn}) - \frac{1}{2}(1 + \delta_n) V_O\right]$$

$$\therefore t_{d2} = -\frac{C_L}{\beta_n} \int_{\frac{V_{DD} - V_{tn}}{1+\delta_n}}^{V_{inv}} \frac{d V_O}{\left[(V_{DD} - V_{tn}) - \frac{1}{2}(1 + \delta_n) V_O\right] V_O} = -\frac{C_L}{\beta_n} I^*$$

Here $\beta_n = \left(\frac{W_n}{L_n}\right) \mu_n C_{ox}$.

$$I^* = \frac{(1 + \delta_n)}{2 (V_{DD} - V_{tn})} \int_{\frac{V_{DD} - V_{tn}}{1+\delta_n}}^{V_{inv}} \left\{ \frac{2}{V_O (1 + \delta_n)} + \frac{1}{\left[(V_{DD} - V_{tn}) - \frac{1}{2}(1 + \delta_n) V_O\right]} \right\} d V_O$$

using method of partial fractions.

$$I^* = \frac{1}{(V_{DD} - V_{tn})}\left\{\ln\left[\frac{V_{inv}}{\left(\frac{V_{DD} - V_{tn}}{1+\delta_n}\right)}\right] + \ln\frac{(V_{DD} - V_{tn})}{2\left[(V_{DD} - V_{tn}) - \frac{1}{2}(1+\delta_n)V_{inv}\right]}\right\}$$

where

$$V_{inv} = V_{tn} + \frac{V_{DD} - V_{tn} - V_{tp}}{1 + \sqrt{\frac{\left(\frac{W_n}{L_n}\right)\mu_n(1+\delta_n)}{\left(\frac{W_p}{L_p}\right)\mu_p(1+\delta_p)}}}$$

Which can be found by equating saturation currents of the two devices when $V_{in} = V_{inv}$. Thus, t_{d2} can, in principle be found.

Under simplified assumption that

$V_{tn} = 0.2\ V_{DD}$, $V_{inv} \approx 0.5\ V_{DD}$,

$\delta_n \approx \delta_p \approx 0$, we have

$$I^* = \frac{1}{0.8\,V_{DD}}\left[\ln\frac{0.5\,V_{DD}}{0.8\,V_{DD}} + \ln\frac{0.8\,V_{DD}}{2(0.8-0.25)V_{DD}}\right]$$

$$I^* = -\frac{1}{0.8\,V_{DD}}\ln\frac{1.1}{0.5} = -\frac{0.986}{V_{DD}}$$

Hence,

$$t_{d2} = -\frac{C_L}{\beta_n}\left(-\frac{0.986}{V_{DD}}\right) = \frac{0.986\,C_L}{\beta_n\,V_{DD}}$$

Thus, accurate estimation of load is needed to get the delay. The total delay t_d is given by

$$t_d = t_{d1} + t_{d2} = \frac{1.61\,C_L}{\beta_n\,V_{DD}}$$

To calculate fall time t_f, notice that we need to account for voltage fall from $0.9\ V_{DD}$ to $0.1\ V_{DD}$ for the output voltage. Hence in the first region where $0.9V_{DD} \le V_O \le \frac{V_{DD} - V_{tn}}{1+\delta_n}$ and n-channel device is in saturation, the method for t_{d1} calculation can be applied to give

$$|\Delta V| = V_{DD} - \frac{(V_{DD} - V_{tn})}{1+\delta_n} - 0.1V_{DD}$$

$$= \frac{0.9V_{DD}\delta_n + V_{tn} - 0.1V_{DD}}{1+\delta_n}$$

$$t_{f1} = \frac{2\,C_L\,(V_{tn} - 0.1V_{DD} + 0.9\,\delta_n V_{DD})}{\beta_n\,(V_{DD} - V_{tn})^2}$$

Hence for simplified case of

$V_{tn} = 0.2\ V_{DD}$ and $\delta_n = 0$, we have

$$t_{f1} = \frac{0.313\,C_L}{\beta_n\ V_{DD}}$$

t_{f2} can be calculated with the same technique as that of t_{d2} except for lower limit changing to $0.1\ V_{DD}$ from the switching voltage V_{inv}.

$$t_{f2} = -\frac{C_L}{\beta_n} \int_{\frac{V_{DD}-V_{tn}}{1+\delta_n}}^{0.1V_{DD}} \frac{d\,V_O}{\left[(V_{DD} - V_{tn}) - \frac{1}{2}(1+\delta_n)V_O\right] V_O}$$

$$= -\frac{C_L}{\beta_n}\frac{1}{(V_{DD} - V_{tn})}\left\{\ln\left[\frac{0.1V_{DD}}{\left(\frac{V_{DD}-V_{tn}}{1+\delta_n}\right)}\right] + \ln\left[\frac{(V_{DD} - V_{tn})}{2\left(V_{DD} - V_{tn} - \left(\frac{0.1V_{DD}}{2}\right)(1+\delta_n)\right)}\right]\right\}$$

Again for simplified case of

$V_{tn} = 0.2\ V_{DD}$ and $\delta_n = 0$, we have

$$t_{f2} = -\frac{C_L}{\beta_n}\frac{1}{0.8\,V_{DD}}\left[\ln\frac{0.1V_{DD}}{0.8\,V_{DD}} + \ln\frac{0.8\,V_{DD}}{2\times 0.75V_{DD}}\right]$$

$$t_{f2} = \frac{C_L}{\beta_n}\frac{1}{0.8\,V_{DD}}\ln\frac{1.5}{0.1} = \frac{3.39\,C_L}{\beta_n\ V_{DD}}$$

Hence $t_f = t_{f1} + t_{f2} = \frac{3.7\,C_L}{\beta_n\ V_{DD}}$.

Hence accurate estimation of C_L is the key to obtain accurate delay estimation.

The similar expressions can be derived for t_r with $\delta_n \rightarrow \delta_p$, $V_{tn} \rightarrow V_{tp}$, $V_{inv} \rightarrow V_{inv}$, $V_{tp} \approx -0.2\ V_{DD}$.

We have $$t_r = \frac{3.7\,C_L}{\beta_p\ V_{DD}}.$$

Hence for equal rise and fall time, $\beta_n \approx \beta_p$ or

$$\frac{W_n}{W_p} \bullet \frac{L_p}{L_n} \approx \frac{\mu_p}{\mu_n} \text{ or } \frac{W_p}{L_p} \approx (2 \text{ to } 3)\frac{W_n}{L_n}$$

which is a fairly well known result.

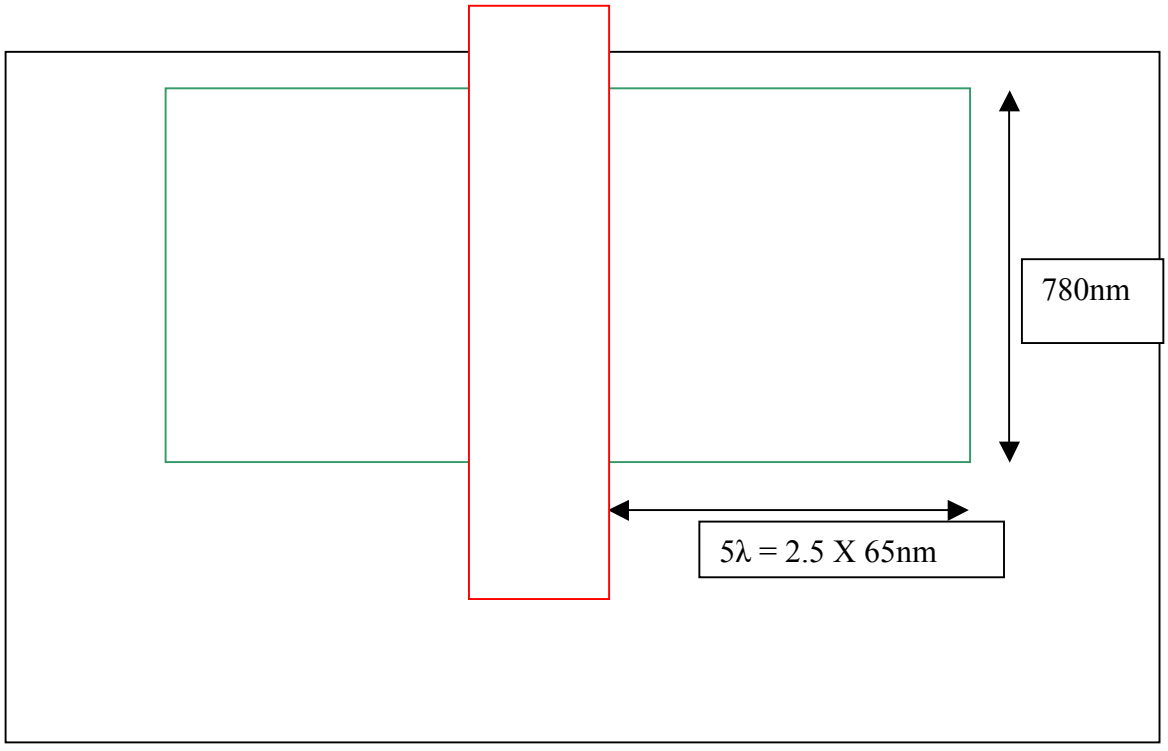
Problem 3: From problem 2, $t_d = t_{d1} + t_{d2} = \dfrac{1.61\,C_L}{\beta_n\, V_{DD}}$.

Here $C_L = 100\text{fF}$, $V_{DD} = 1.2\text{V}$, $\beta_n = \left(\dfrac{W_n}{L_n}\right)\mu_n\, C_{ox}$.

Also, $\mu_n\, C_{ox} = 1.2\text{mA/V}^2$, $t_d = 10\text{ps}$. As technology is 65 nm, we expect $L = 2\lambda = 65\text{nm}$.

Therefore $10\times10^{-12} = \dfrac{1.61\times100\times10^{-15}}{\dfrac{W}{L}\times1.2\times10^{-3}\times1.2}$. Hence $\dfrac{W}{L} = 11.18 \approx 12$ as widths are normally restricted to an integer multiple of L in design. Hence W = 780 nm.

To estimate diffusion parasitic, we neglect interconnect capacitance as it is small and in absence of bias, use zero bias to get conservative load value. Both area capacitance and peripheral capacitance that depend on perimeter of the drain needs to be considered. A simple layout will be as shown both transistors.



Hence Area of drain for each transistor = 0.78 X 2.5 X 0.065 square microns and perimeter = 2(0.78 + 2.5X0.065) micron.
Hence zero bias C
= 2 X 0.78 X 2.5 X 0.065 X0.1 + 2(0.78 + 2.5X0.065)X0.8 + 2(0.78 + 2.5X0.065)X0.9
= 3.23 fF which is only a small contribution.

At the input end, the capacitance will be WL*poly over gate area cap
= 2X0.78 X 0.065 X 1.918 = 0.194 fF which is also quite low.