EE4415 Tutorial for Chapter 3

Q1. What is the data sequence produced by the following logic?

```
always@(posedge clock)  begin
                A = B;
                B = A;
end
```

If initially (A, B) = (1, 0), over 4 clock periods (including the initial one when A=1) the logic sequence at A will be.

(a) 1000
(b) 1010
(c) 1001
(d) 1111
(e) None of the above

Q2. Consider the module below.

```
module prefix_xor_4(x,a);
        input [3:0] a;
        output [3:0] x;
        xor x1(x[1],a[0],a[1]);
        xor x2(x[2],x[1],a[2]);
        xor x3(x[3],x[2],a[3]);
endmodule
```

Suppose the above module is simulated using VCS. The new inputs arrive at t=100ns, at what simulation time would the results be available?

(a) 100ns, (b) 101ns, (c) 103 ns, (d) 103ns

Q3. Consider the following verilog code fragment

```
module D-flip-flop (clock, D, Q);
    input clock, D;
    output Q;
    always @ (posedge clock) Q <= D;
endmodule

module top;
        D-flip-flop u1 (clock, D, Q);
endmodule
```

Which of the following correctly declares clock, D, and Q, within module "top" based on the information given above?

(a) reg clock, D, Q;
(b) wire clock, D, Q;
(c) tri clock, D, Q;
(d) trireg clock, D, Q;
(e) None of the above.

Q4. It is often valuable to simulate the chip function in a high level language such as C or Matlab before starting the logic design because:

(a) It saves overall time to establish that the algorithm to be implemented in the chip is fully debugged before starting hardware design.
(b) It is trivial to convert C to Verilog.
(c) It moves the job of hardware optimization to the high level "algorithm" people who know the most about the intrinsic parallelism of Hardware.
(d) The instructor in your University course on ASIC design said to do it this way and you always do exactly as he advises.
(e) It is not valuable.

Q5. What kind of hardware is this?

```
module WhatIsThis1(out,control,a,b,c,d);
   input[1:0] control;
   input a, b, c, d;
   output out;
   reg [1:0]  out;
   always @( control or a or b or c or d )
   begin
            case ( control )
            0 0: out = a;
            0 1: out = b;
            1 0: out = c;
            1 1: out = d;
            endcase
   end
endmodule
```

(a) sequential circuit, (b) latches, (c) Multiplexer, (d) None of the above.

Q6. Given following module

```
module WhatLoop(a,b);
    input [7:0] b;
    output a;
    reg [2:0] a;
    reg [2:0] i;
    integer s;
    initial begin
    s = 0;
    for(i=0; i<8; i=i+1) s = s + b[i];
    a = s;
```

```
    #5;
    end
endmodule
```

Is this code workable and synthesizable?

(a) Workable, synthesizable;
(b) Not workable, synthesizable;
(c) Workable, not synthesizable;
(d) Not workable, not synthesizable

Q7. Consider the following module,

```
module path_delay(out,in);
    input [3:0] in;
    output [3:0] output;
    xor u1(output [1], in [0], in [1]);
    xor x2(output [2], output [1], in [2]);
    xor x3(output [3], output [2], in [3]);
endmodule
```

Suppose that each gate has a delay of 1ns. How long would it take to compute the result?
(a)1ns, (b)2ns, (c)3ns, (d)4ns.

Q8. What are the values of d, e, f, and g at time=25, if the following code is simulated by VCS?

```
module WhatAreValues;
    reg a = 0 ,b = 0, c = 0;
    reg d,e,f,g;

    initial begin
    # 10 a = 1;
    # 10 b = 1;
    # 10 $finish;
    end

    always @(a, b, c) begin
    d = a & b;
    e = d | c;
    end

    always @(a, b, c) begin
    f <= a & b;
    g <= f | c;
    end
endmodule
```

(a) d=x, e=x, f=x, g=x;
(b) d=x, e=0, f=0, g=x;
(c) d=0, e=0, f=0, g=x;
(d) d=1, e=1, f=1, g=0.

Q9. What are the values of d, e, f, and g at time=5, if the following code is simulated by VCS?

```
module WhatAreValues;
    reg a = 0 ,b = 0, c = 0;
    reg d,e,f,g;
    initial begin
    # 10 a = 1;
    # 10 b = 1;
    # 10 $finish;
    End

    always @(a, b, c) begin
    d = a & b;
    e = d | c;
    end

    always @(a, b, c) begin
    f <= a & b;
    g <= f | c;
    end
endmodule
```

(a) d=1, e=x, f=0, g=1;
(b) d=x, e=x, f=x, g=x;
(c) d=x, e=0, f=1, g=x;
(d) d=x, e=1, f=x, g=0.
(e) None of the above.

Q10. What are the values of d, e, f, and g at time=15, if the following code is simulated by VCS?

```
module WhatAreValues;
   reg a = 0 ,b = 0, c = 0;
   reg d,e,f,g;

   initial begin
   # 10 a = 1;
   # 10 b = 1;
   # 10 $finish;
   End
```

```
    always @(a, b, c) begin
    d = a & b;
    e = d | c;
    end

    always @(a, b, c) begin
    f <= a & b;
    g <= f | c;
    end
endmodule
```

(a) d=x, e=x, f=x, g=x;
(b) d=x, e=0, f=0, g=x;
(c) d=0, e=0, f=0, g=x;
(d) d=1, e=1, f=1, g=0.