CMOS Inverter Technology

In this half of the module, you will learn to

- Design of cells to implement logic functions.
- To analyze and improve functionality and speed of the cells.
- Understand how the CMOS circuits are realized on Silicon and do physical layout.

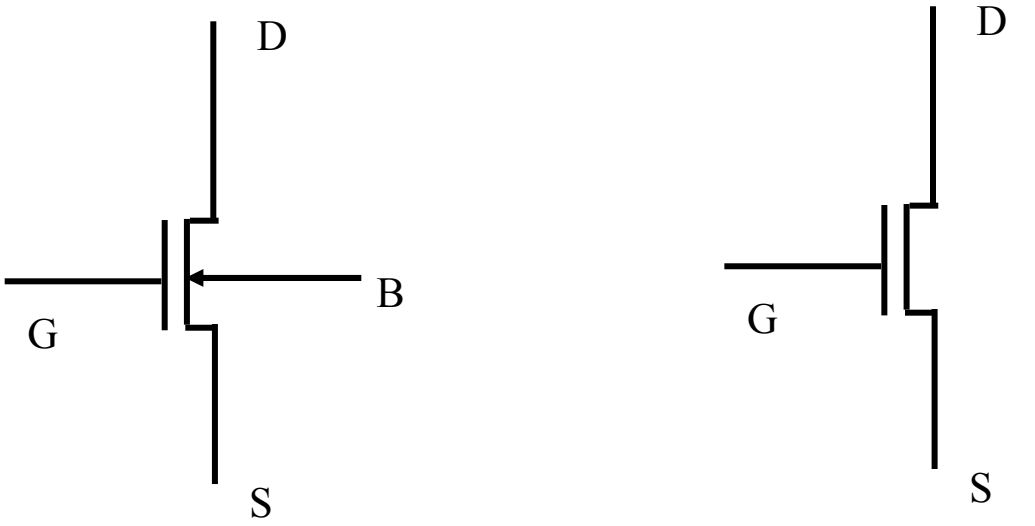
In this lecture, you will learn to

- Design inverter cell.
- Analyze switching and speed of the inverter.

Basic Notations

● In CMOS technologies, both n-type (n-channel) and p-type (p-channel) Metal Oxide Semiconductor field effect transistors (MOSFETs) are used.

● For MOSFETs, S denotes Source, D the Drain, G the Gate and B the body or substrate terminals. Small or capital letters are equivalent for voltages.

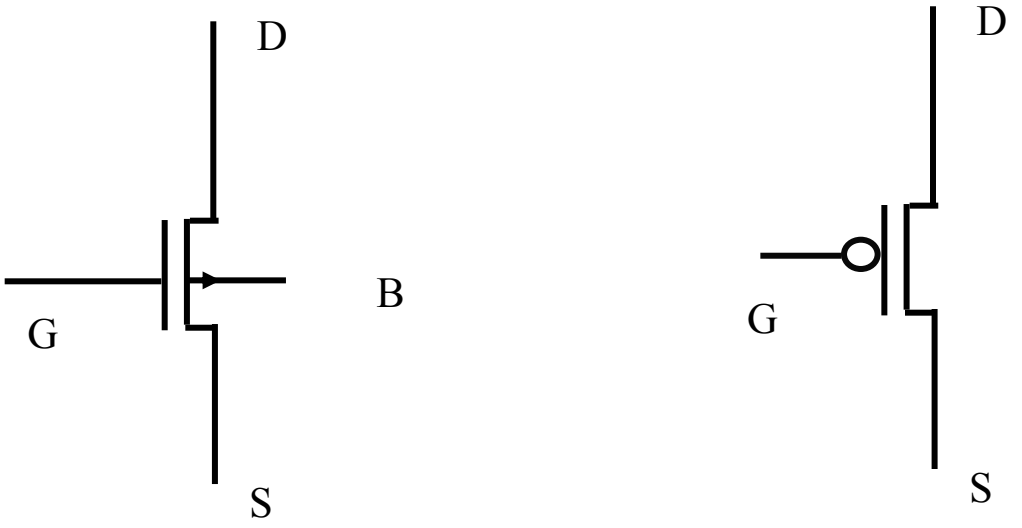


● n-type transistor : substrate is p-doped (acceptor type) and is connected to -ve supply.

● For simplicity, as substrate bias is usually fixed, removal of substrate (body) contact leads to the compact notation on the right.

Basic Notations

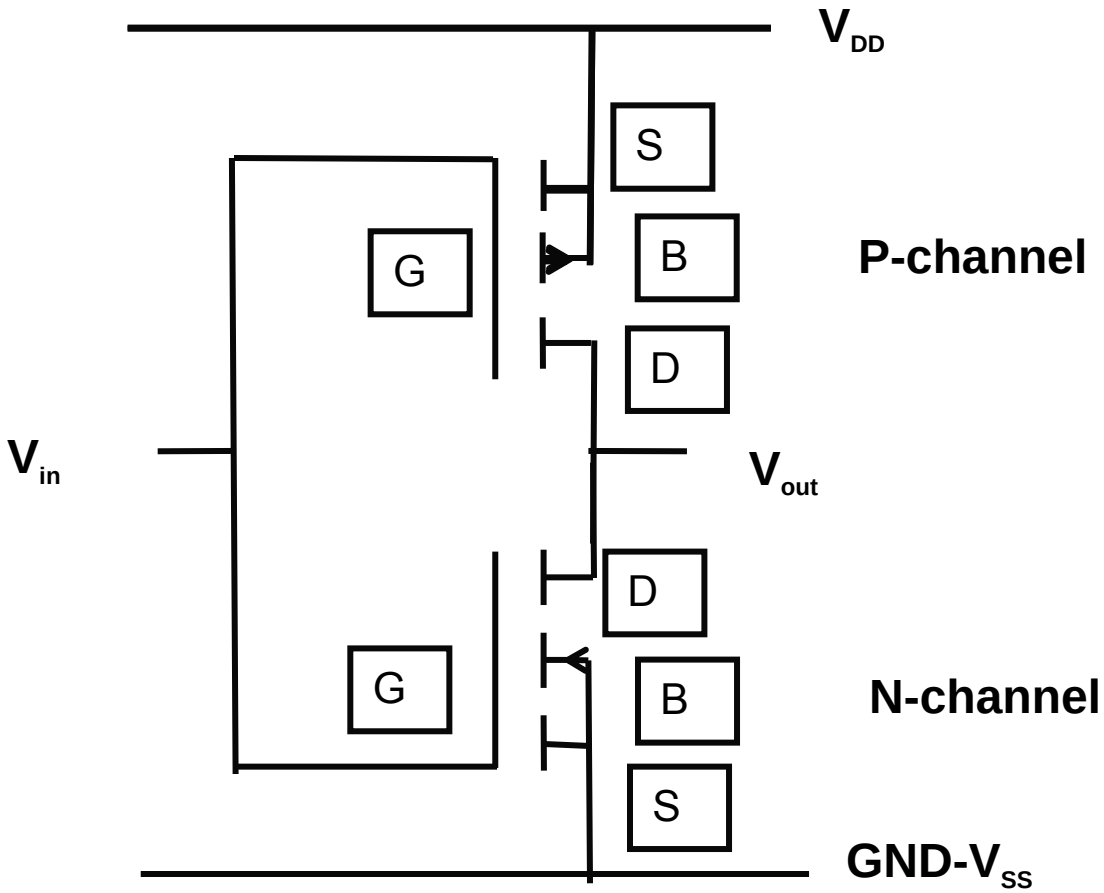
- p-type transistor : substrate is n-doped (donor type) and is connected to +ve supply.
- For simplicity, as substrate bias is usually fixed, removal of substrate (body) contact leads to the compact notation on the right.



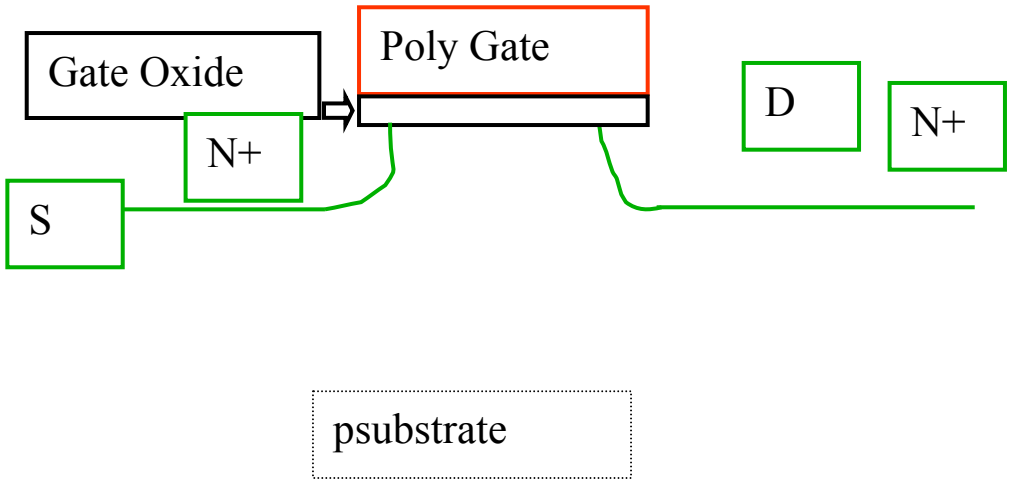
Basic Notations

● The following circuit shows another way to represent 4 terminal MOS device (MOSFET).

● Basic simplest circuit block in CMOS technology is an inverter that uses both devices. The schematic of CMOS inverter is shown below.

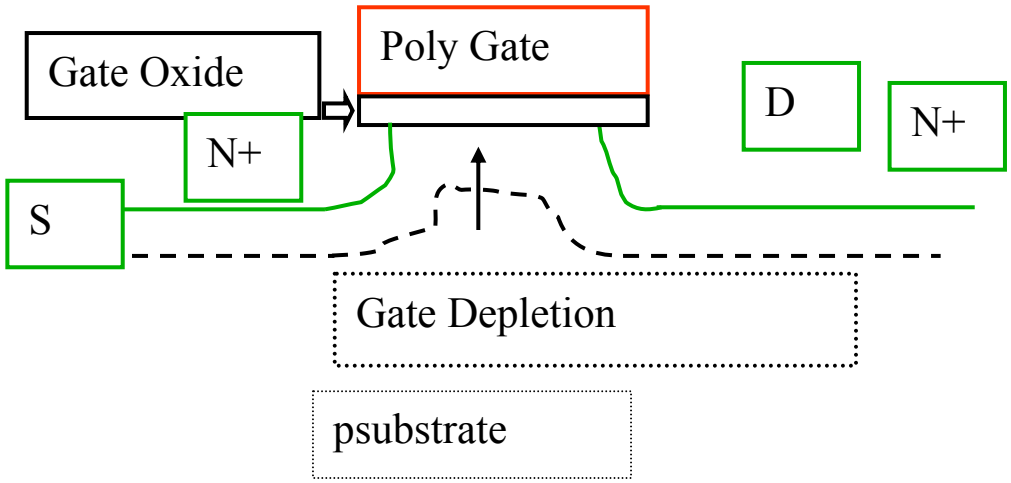


Basic n-channel MOS Device Desription



- Thin gate oxide always desirable for better gate control. As thin as 1.2 nm for technologies below 0.1 micron.
- Polysilicon gate for self alignment that helps to achieve a better process integration (clarified later).
- Heavily doped source drain regions for low resistance.
- Low resistance metal connections for source, drain, body (same as substrate or well or tub - different notations).

Basic n-channel MOS Device Desription



- If V_{GS} is negative, holes in the substrate will be attracted to Si-SiO_2 interface. Accumulation.

- As V_{GS} increases, the interface comes out of accumulation and the gate depletion (or space charge region) shown by dashed line under the gate becomes deeper.

- If V_{GS} increases further, eventually the device enters the regime of strong inversion where there is a large electron concentration (opposite to the substrate carriers holes) below the oxide. The gate depletion now stops growing. The threshold voltage of MOS device is defined as the V_{GS} that leads to strong inversion. After this V_{GS}, the device conducts with the help of the electrons for positive V_{DS}.

Basic n-channel MOS Device Desription

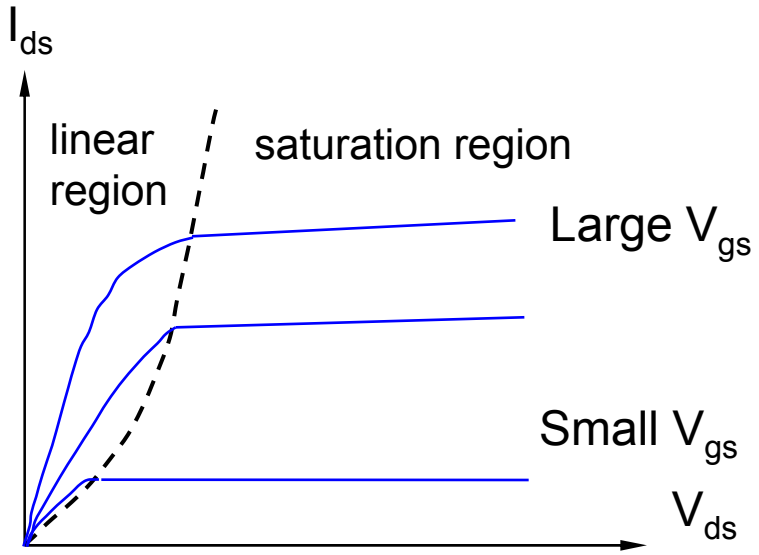
- P-channel device has opposite relative voltages, has P+ (heavily p doped) source-drains, and n-type substrate. Both devices are used in CMOS technology which is our focus. P-channel device normally carries less current for similar dimension compared to n-channel due to lower mobility of holes.

- For designers, it is important to know how the drain current I_D changes when V_{GS} and V_{DS} change. Under simplified assumptions, analytic expressions for this current can be derived which we will use for design

- I-V plots and analytic expressions will now be discussed followed by cell design and timing calculations with parasitic (unwanted capacitors and resistors which cannot be removed) estimation.

- Much later, we will move on to study how to fabricate these devices so that you have basic knowledge on what determines device limitations and design rules and how to logically develop layout of a circuit to implement it in Silicon.

MOS Transistor Characteristics



- Simple Model: cut-off region : $V_{gs} - V_t < 0$

$I_{ds} = 0$

(V_t is the threshold voltage, also denoted as V_{TN} for n-channel MOSFET and V_{TP} for p-channel MOSFET. Normally, $V_{TN} > 0$ and $V_{TP} < 0$).

In the linear region where $0 \le V_{ds} \le \left(V_{gs} - V_t\right)$,

$$I_{ds} = \beta\left[\left(V_{gs} - V_t\right)V_{ds} - \frac{V_{ds}^2}{2}\right]$$

MOS Transistor Characteristics

In the saturation region where $V_{ds} \geq \left(V_{gs} - V_t\right) > 0,$

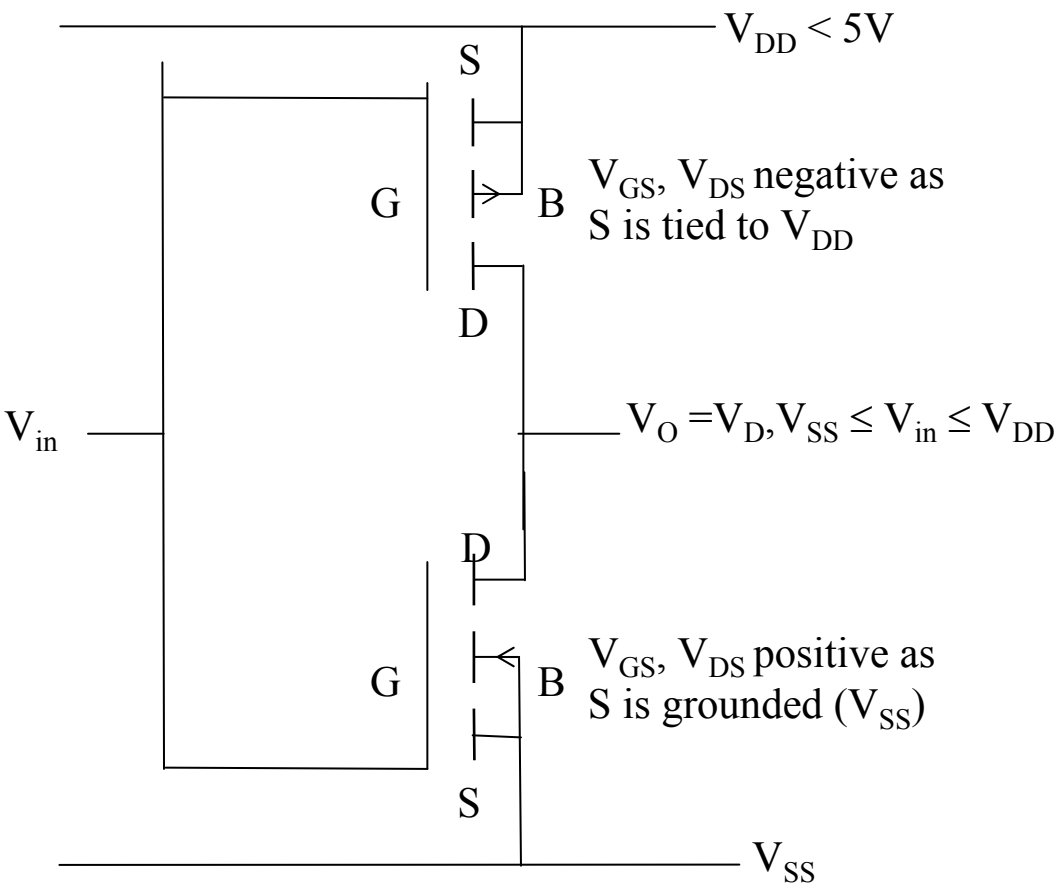
$$I_{ds} = \frac{\beta}{2}\left(V_{gs} - V_t\right)^2$$

where $\beta = \frac{\mu\varepsilon}{t_{ox}}\left(\frac{W}{L}\right)$

μ : effective surface mobility of charge carrier.
ε : permittivity of gate insulator.
tox : thickness of gate insulator.
W : channel width.
L : channel length.

Basic Operation of an Inverter

- The schematic of CMOS inverter is repeated below.



- If $V_{in} = 0$, then n-channel device is off.
- Hence there is no current through the n-channel device and consequently through the p-channel device (by KCL).
- For the p-channel device, $V_{GS} = V_G - V_S = -V_{DD}$. Hence, it is turned on.
- The only consistent voltage, where $V_{GS} = -V_{DD}$ and p-channel device current is zero, is V_{DS} (p-channel) = 0 i.e. $V_O = V_{DD}$.
- Thus, if $V_{in} = 0$, $V_O = V_{DD}$.

Basic Operation of an Inverter

- On the other hand, if $V_{in} = V_{DD}$, then $V_{GS} = 0$ for the p-channel device.
- Since $V_{GS} \leq V_{TP}$ is a necessity for it to conduct, the device is off.
- Hence, there is no current through the n-channel device which is turned on by $V_{in} = V_{DD} \geq V_{TN}$.
- Again, for this to be consistent, V_{DS} (n-channel) = 0 or $V_O = 0$.
- Hence if $V_{in} = V_{DD}$, $V_O = 0$.

- Thus it is clear that the circuit here performs a job of an inverter with $V_{in} = 0$ or $V_{in} = V_{DD}$. When input switches from say 0 to V_{DD}, output switches from V_{DD} to 0.
- The devices are in different regions of operation during the switch. The switching of the inverter now will be discussed.

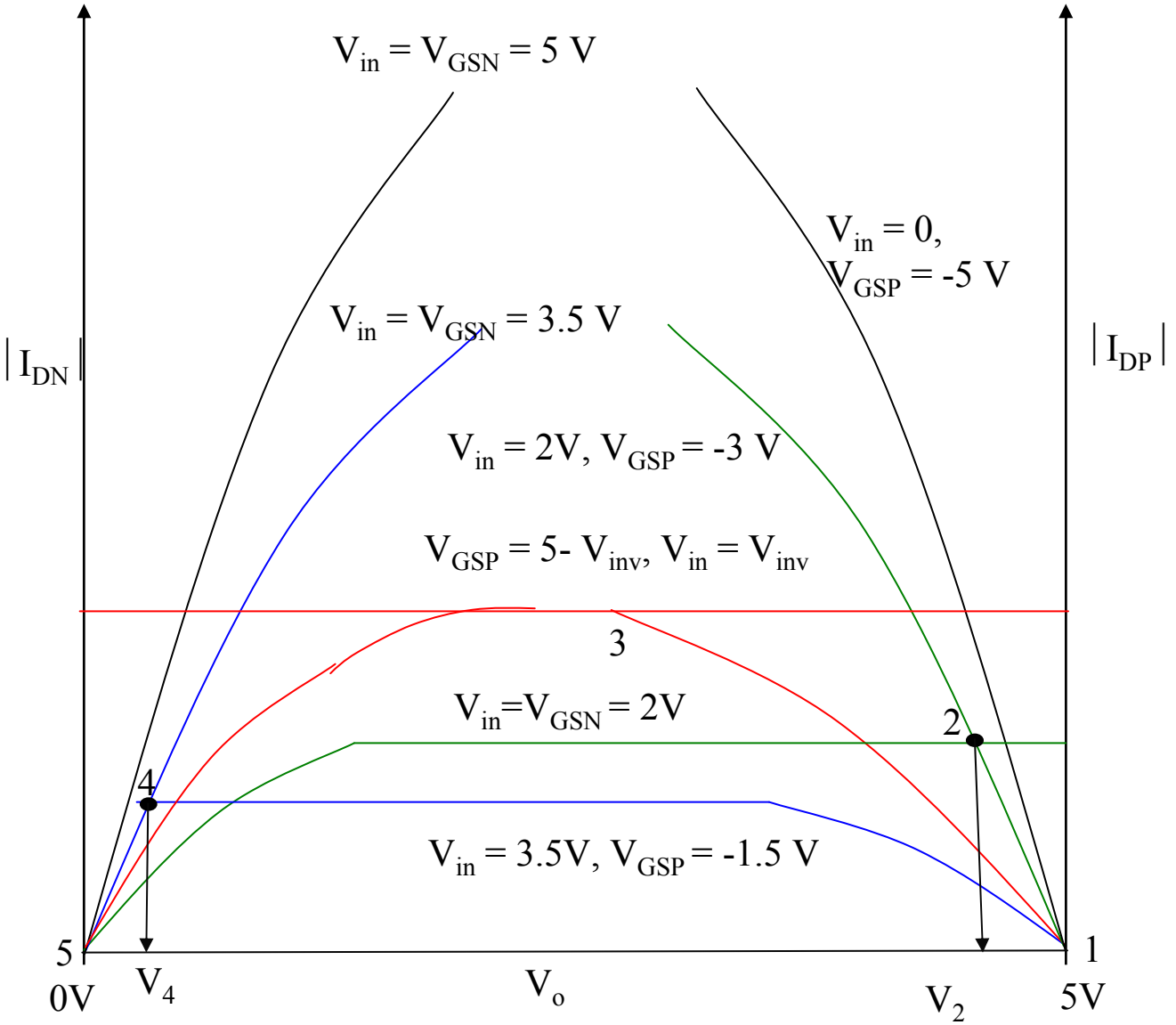
Switching Characteristics of the Inverter

● As V_{in} changes, these devices go through five different combinations of regions of operation. These combinations are indicated below.

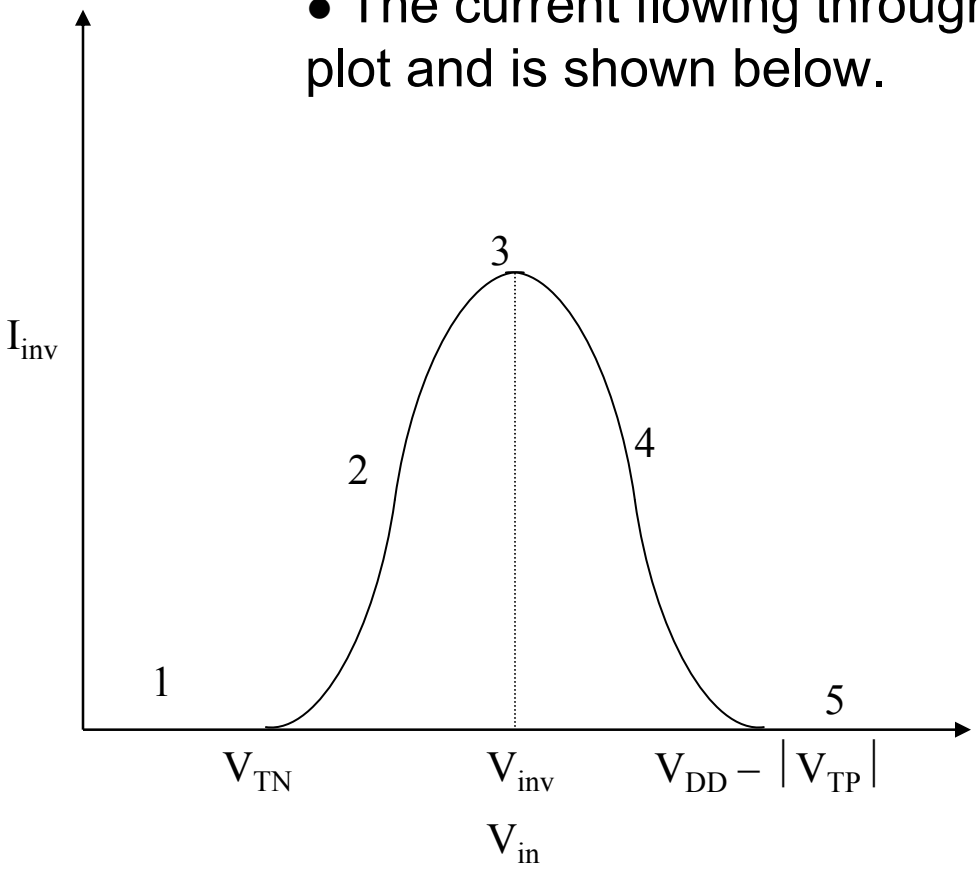
1. $0 \leq V_{in} \leq V_{TN}$ n-channel off, p-channel on
2. $V_{TN} < V_{in} < V_{inv}$ p-channel linear, n-channel saturation
3. $V_{in} = V_{inv}$ Both in saturation
4. $V_{inv} < V_{in} < V_{DD} - V_{TP}$ n-channel linear, p-channel saturation
5. $V_{DD} - V_{TP} \leq V_{in} \leq V_{DD}$ p-channel off, n-channel on

Where V_{inv} is called as switching voltage. The characteristics are derived based on the fact that both MOSFETs in the inverter here carry the same amount of current.

Plot of Switching Characteristics of the Inverter



Switching Characteristics of the Inverter



- The current flowing through the inverter can be read from the plot and is shown below.

- One can notice that for a step V_{in}, the current only flows for a short time. If input is changing in a finite time, the current will flow through the inverter, which peaks at V_{inv}.

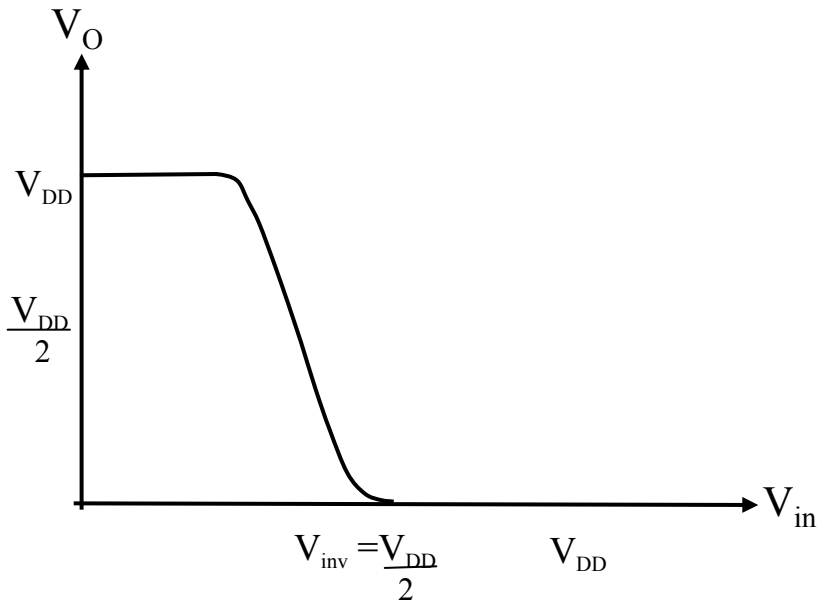
- This inverter will consume lower amount of power compared to circuits that continuously conduct such as bipolar or NMOS, as there is no current for some voltages.

- If there is no switching (DC), there is no power consumption, in principle, a huge benefit for VLSI which made CMOS dominant.

- In reality, there is some power consumption due to sub-threshold currents, reverse biased diode currents and continuous running clocks.

Switching Characteristics of the Inverter

- The Voltage Response is as shown.



- Most change occurs near V_{inv} as the current here is the largest and aids in a fast transition.

Switching Characteristics of the Inverter

- Switching voltage of the inverter.
- At switching voltage, the saturation current of n- and p- channel devices are equal.
- Assume that the threshold voltages of n- and p- transistors have the same magnitudes. Then

For n-transistor in saturation, $I = \frac{\beta_n}{2}(V_{in} - V_t)^2$

For p-transistor in saturation, $I = \frac{\beta_p}{2}(V_{DD} - V_{in} - V_t)^2$

For switching at $V_{in} = \frac{V_{DD}}{2}$, $I = \frac{\beta_n}{2}\left(\frac{V_{DD}}{2} - V_t\right)^2 = \frac{\beta_p}{2}\left(\frac{V_{DD}}{2} - V_t\right)^2$

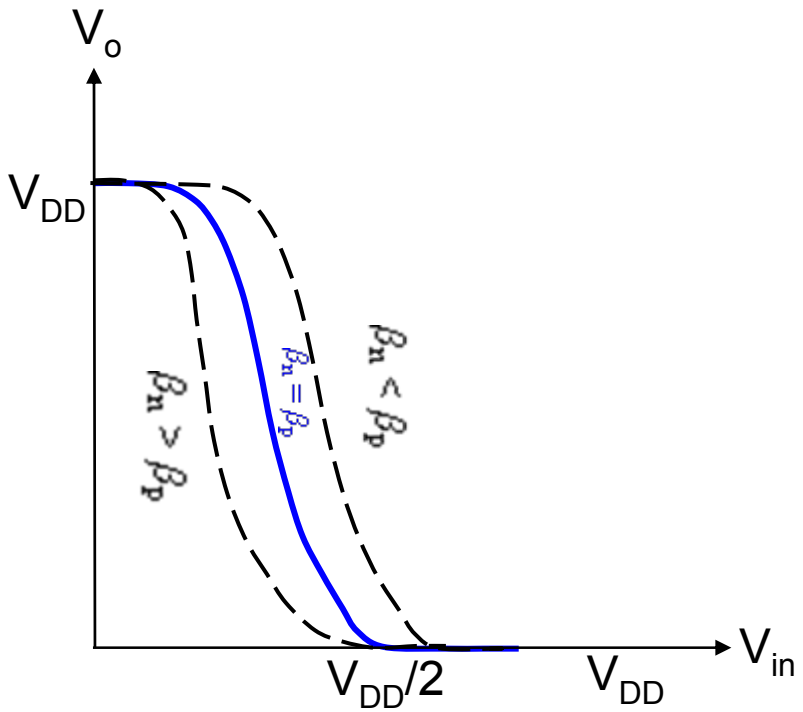
$$i.e.\ \beta_n = \beta_p$$

Switching Characteristics of the Inverter

$$\beta_n = \beta_p \Rightarrow \frac{\mu_n \varepsilon}{t_{ox}} \frac{W_n}{L_n} = \frac{\mu_p \varepsilon}{t_{ox}} \frac{W_p}{L_p} \Rightarrow \frac{W_p}{W_n} = \frac{\mu_n}{\mu_p}$$

as normally $L_n = L_p$ in CMOS digital design.

$\therefore \frac{W_p}{W_n} \approx 2$ based on elctron and hole moblities.



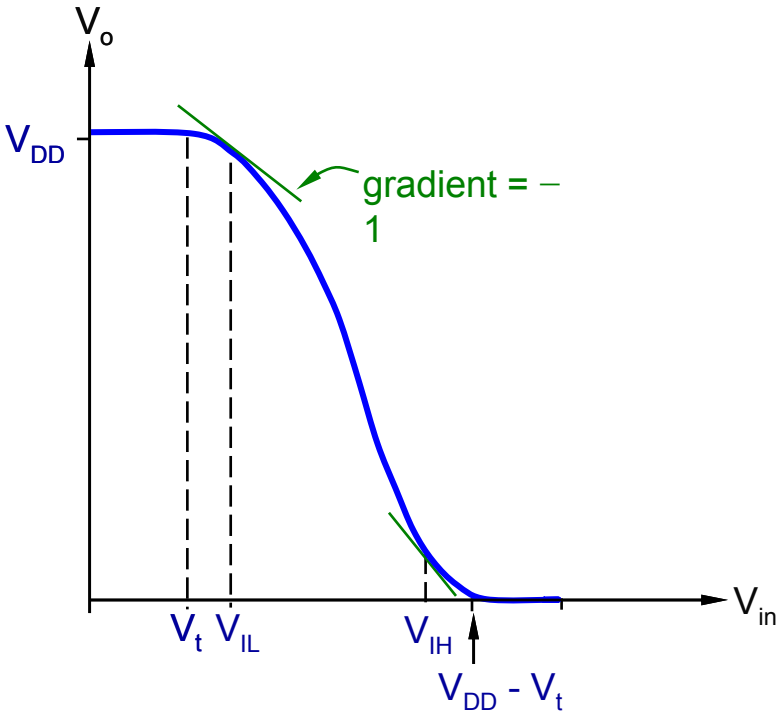
- The effect of sizes is best depicted in the figure.

Any observations?

Switching Characteristics of the Inverter

- Noise margin in digital circuits is very important and should be as large as possible.

- It can be easily deduced from output response as the output is not likely to switch if magnitude of dV_o/dV_{in} is <1.



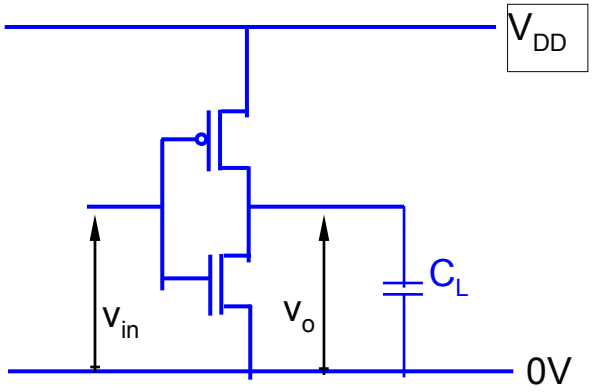
- V_{IL} = maximum LOW input voltage
- V_{IH} = minimum HIGH input voltage
- Noise margin (low) = V_{IL}
- Noise margin (high) = $V_{DD} - V_{IH}$

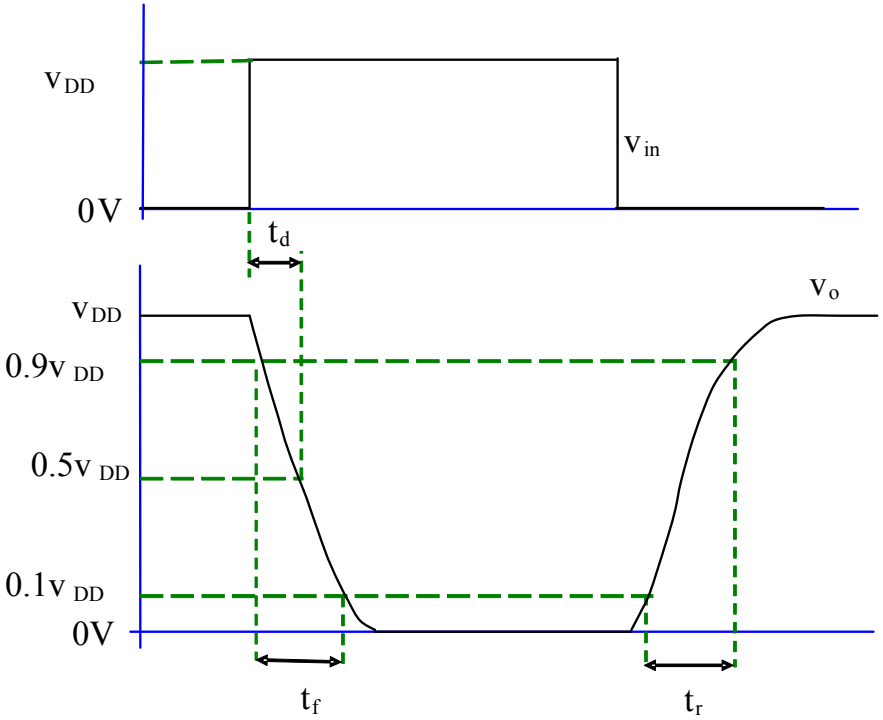
Switching Characteristics of the Inverter

Loaded CMOS inverter

- The above conditions in switching studies are all ideal. Normally, CMOS inverter will have parasitic resistances and capacitances attached to the output node. Hence principle of operation of inverter alters a bit.

- The loaded CMOS inverter and its response is shown below.





- We define: t_d : delay time

t_f : fall time and t_r : rise time

Switching Characteristics of the Inverter

- If input was at low voltage, the output is high and the capacitor CL holds the charge to maintain this high voltage.

- If input now switches instantaneously to high, the capacitor voltage does not change instantaneously as this requires infinite current. Instead, at the switching time, both the gate voltage and the drain voltage are a high for the NMOS transistor which turns on.

- The NMOS device current will discharge the capacitor to zero after a delay time. This is the reason NMOS device is called as a pull down device.

- Once the output voltage reaches zero, NMOS transistor stops conducting as $V_{DS} = 0$. The output stays at zero volts after this delay and there is no current in the circuit.

- Exactly opposite cycle occurs when input becomes low and PMOS device charges the capacitor to raise output voltage to the power supply voltage. Similarly, PMOS device is called as a pull up device.

- Now we can estimate dynamic power dissipation quite easily during one switching cycle.

Power consumption of the Inverter

- **Dynamic power**

- Charging and discharging of load capacitance determines the dynamic power consumption.

- If the load capacitance is C, the charge stored is CV_{DD}. energy supplied by V_{DD} in one full switching cycle is CV_{DD}. If the switching frequency is f, the power dissipated (energy drawn from power source in unit time) is fCV_{DD}^2.

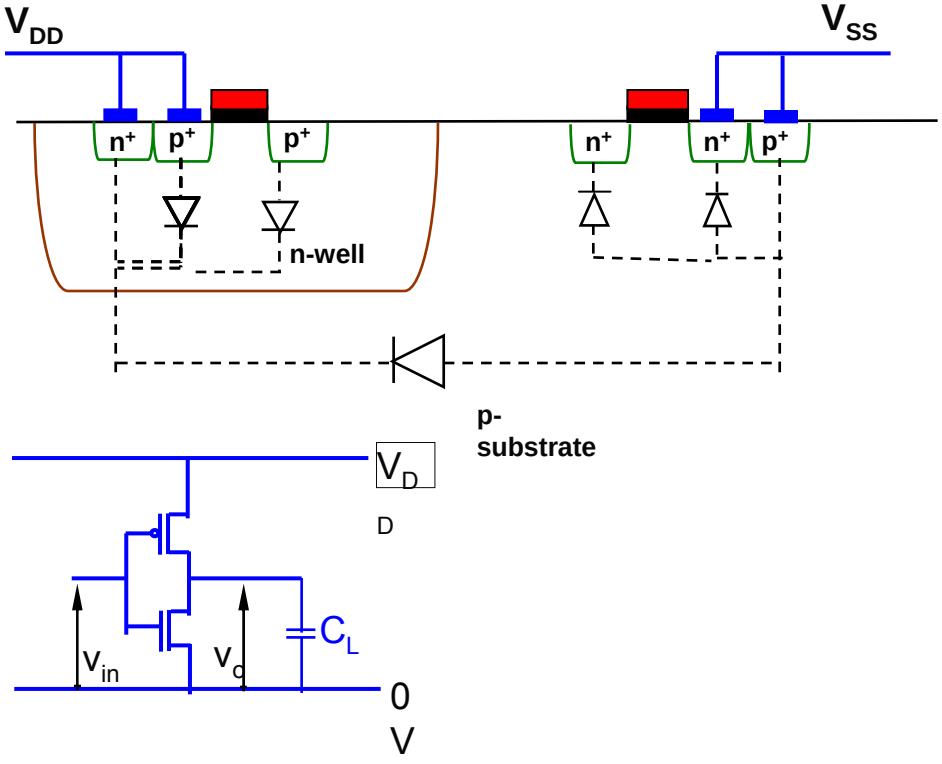
How we can minimize dynamic power consumption?

Power consumption of the Inverter

- **Static power consumption when there is no switching**

- Ideally, there should be no power consumption if there is no switching activity.

- Let us look at the inverter cross section using simple device structure where both p-MOS and n-MOS devices are included.



- All diodes here are reversed biased and both MOSFETs are off when there is no switching.

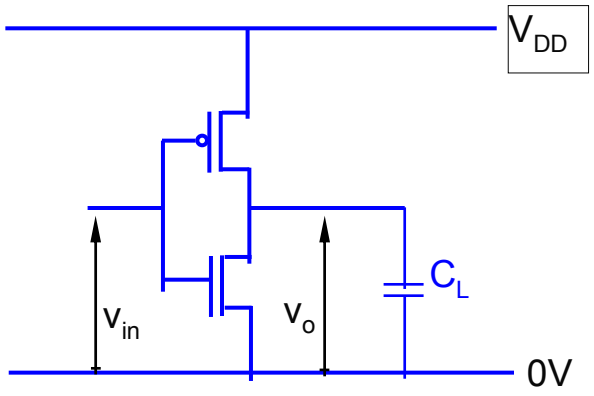
- Reverse bias diodes leak currents giving a part of static power.

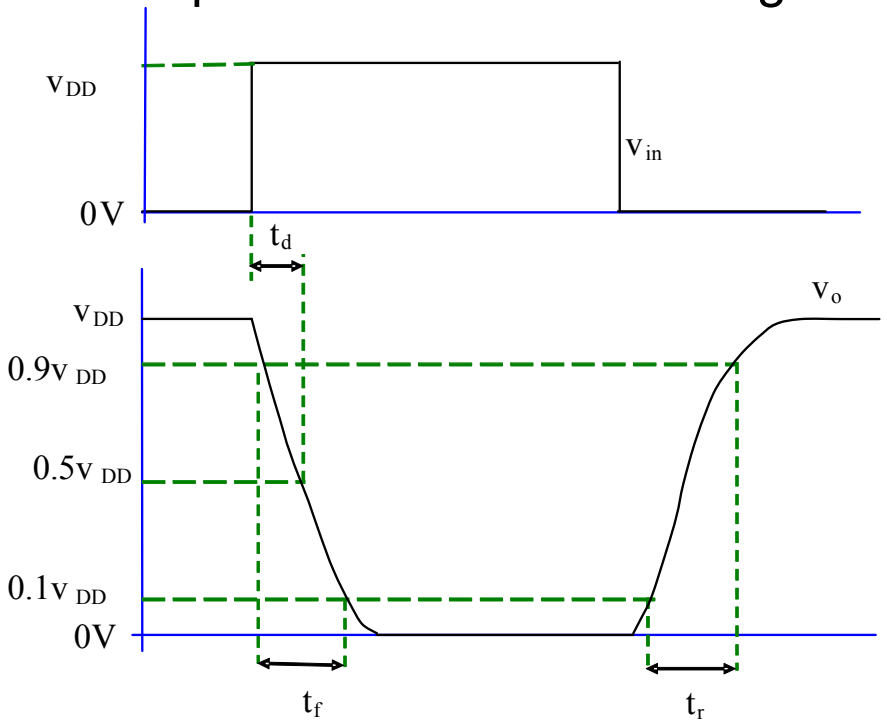
- If output is high, n drain of the n-MOS device is at V_{DD} and the gate is at 0V. Such n-MOSFET can leak current as drain voltage is large. The leakage of MOSFET is becoming higher as they shrink. It is around 100nA/micron for technologies <100nm.

- **How we can minimize static power consumption?**

Switching Speed of the Inverter

- The loaded CMOS inverter and its response is shown below again.





- We define: t_d : delay time

  t_f : fall time and t_r : rise time

- What are factors that will determine switching speed?

- The times in these transitions are clearly determined by load, capacitive or resistive, and MOSFET currents. Hence it is important to determine this load and MOSFET currents for which we will use the simple model described. However, the treatment will be similar with any model. Primary timing comes from capacitive load and hence we will only consider this load.