NATIONAL UNIVERSITY OF SINGAPORE

SCHOOL OF COMPUTING
EXAMINATION FOR

SEMESTER 1 (2001-2)

CS2271: INTRODUCTION TO EMBEDDED SYSTEMS

November 2001 **Time Allowed 2 Hours**

INSTRUCTIONS TO CANDIDATES

1. This examination paper consists of **ONE (1)** part and comprises **SIX (6)** printed pages.

2. This paper consists of six (6) structured questions. Do all six questions. Write all your answers in the answer booklet.

3. This is an **OPEN BOOK** examination.

QUESTION 1 (10%)

(a) If you want to implement the following logic functions with a 4 x k x 2 PLA, what is the **minimum** value of k? Justify your answer. 5%

$F1 = (A, B, C, D) = \sum m\ (0, 2, 4, 6, 8, 10)$

$F2 = (A, B, C, D) = \sum m\ (4, 6, 8, 10, 12, 14)$

(b) If you want to implement the above logic functions with a 4 x k x 2 PAL, where each OR gate is connected to k/2 AND gate outputs, what is the **minimum** value of k? Justify your answer. 5%

QUESTION 2 (15%)

(a) Write a Handel-C program fragment to find the maximum element of a 16-element array (where each element is 8-bit unsigned integer) in $(\log_2 N+1) = 5$ clock cycles. Also describe informally the reasoning behind your code. 10%

(b) Assume that we don't care about the cycle time, that is, we can have really long combinational circuit delay. What is the minimum number of clock cycles required for a Handel-C program to find the maximum element of a 16-element array (where each element is 8-bit unsigned integer)? Assume there is no duplication in the array. Justify your answer. 3%

(c) Handel-C allows you to swap two elements in one clock cycle as shown in the following code fragment:

```
par { a = b; b = a;}
```

Describe how the swapping is done in hardware with the help of a timing diagram. 2%

QUESTION 3 (20%)

(a) Write ARM assembly language code for the following program fragment. Assume g is a global variable. 10%

```
int foo(int x1) { return (x1 +5);}
baz () { g = g + 1;}
int scum (int x2) { return foo(x2);}
main (){ g = scum (3); baz (); }
```

(b) Write SHARC assembly language code for the above program fragment. 10%

QUESTION 4 (20%)

Assume three periodic processes P1 = (3, 9, 9), P2 = (5, 18, 18), and P3 = (4, 12, 12).

(a) Demonstrate that a feasible schedule based on **fixed** priorities exists or prove that one cannot exist. 10%

(b) Give a schedule following the EDF policy with minimum number of context switches. 10%

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QUESTION 5 (15%)

(a) Suppose data transfer between hard disk and CPU takes place though DMA. Assume that the initial setup of a DMA transfer takes 1000 clock cycles for the processor, and assume that the handling of the interrupt at DMA completion requires 1000 clock cycles for the processor. The hard disk has a transfer rate of 16MB/sec. If the average transfer from the disk is 128KB, what fraction of a 1GHz processor's cycles per second is consumed if the disk is actively transferring 100% of the time? Ignore any impact from bus contention between the processor and the DMA controller. 5%

(b) Discuss the disadvantages of DMA transfer for a hard real-time system. 2%

(c) Assume an A/D converter is supplying samples at 44.1 kHz. 5%

(i) How much time is available per sample for CPU operations?

(ii) If the interrupt handler executes 100 instructions obtaining the sample and passing it onto the application routine, how many instructions can be executed by the application routine per sample on a 20MHz ARM processor that executes 1 instruction per cycle?

(d) Assume a network with bandwidth of 100Mbits/second has a sending overhead of 230 microseconds and a receiving overhead of 270 microseconds. Assume one machine wants to send a 1000 byte message to another (including header) and the message format allows 1000 bytes in a single message. Calculate the total latency to send the message from one machine to another. What is the effective bandwidth of this system? (Effective bandwidth is defined as (message size) / (total latency)). 3%

QUESTION 6 (20%)

(a) Below is a program fragment that computes an integer approximation to *sqrt(n)* for *n*, a non-negative integer.

```
a = 0;
while ((a + 1)^2 <= n)
    a = a+1;
```

Suppose that the first assignment takes 1 time unit, the second (incrementing *a* by 1) takes 2 time units, evaluating the Boolean expression takes 3 time units, and the control statement (*while*) takes 1 time unit. Give the best case and worst case execution time of the program when n is in the range $6 < n < 17$ 5%

(b) Consider a processor P1 running at frequency f1 and voltage V1. Consider another processor P2 identical to P1 except that it runs at frequency f2 = f1/2 and voltage V2 = V1/2. Suppose P1 takes 15 time units to complete task A whose deadline is 40 time units later. 5%

(i) Which processor will you choose if you want to consume minimum energy while meeting the deadline?

(ii) For Intel XScale processor, one can dynamically change the voltage. Suppose that the processor frequency is proportional to the voltage. For example, if voltage is halved, frequency is halved as well. Assume that the processor is running only one periodic real-time task at a time. Suggest a dynamic energy management technique for XScale processor such that energy consumption is minimized while meeting the deadline.

(c) Give an example of each of the following types of real-time systems. 4%

(i) hard and critical

(ii) soft and critical

(ii) hard and non-critical

(iv) soft and non-critical

(d) What kind of tool should you use to setup a breakpoint at every "cache miss" event for an embedded system? 2%

(e) The assembler employs a two-pass algorithm to resolve the labels. Suggest the unique feature of the class of programs for which the second pass is not required. 2%

(f) Why do you think most embedded systems do not need to use dynamically linked libraries? 2%

END OF PAPER