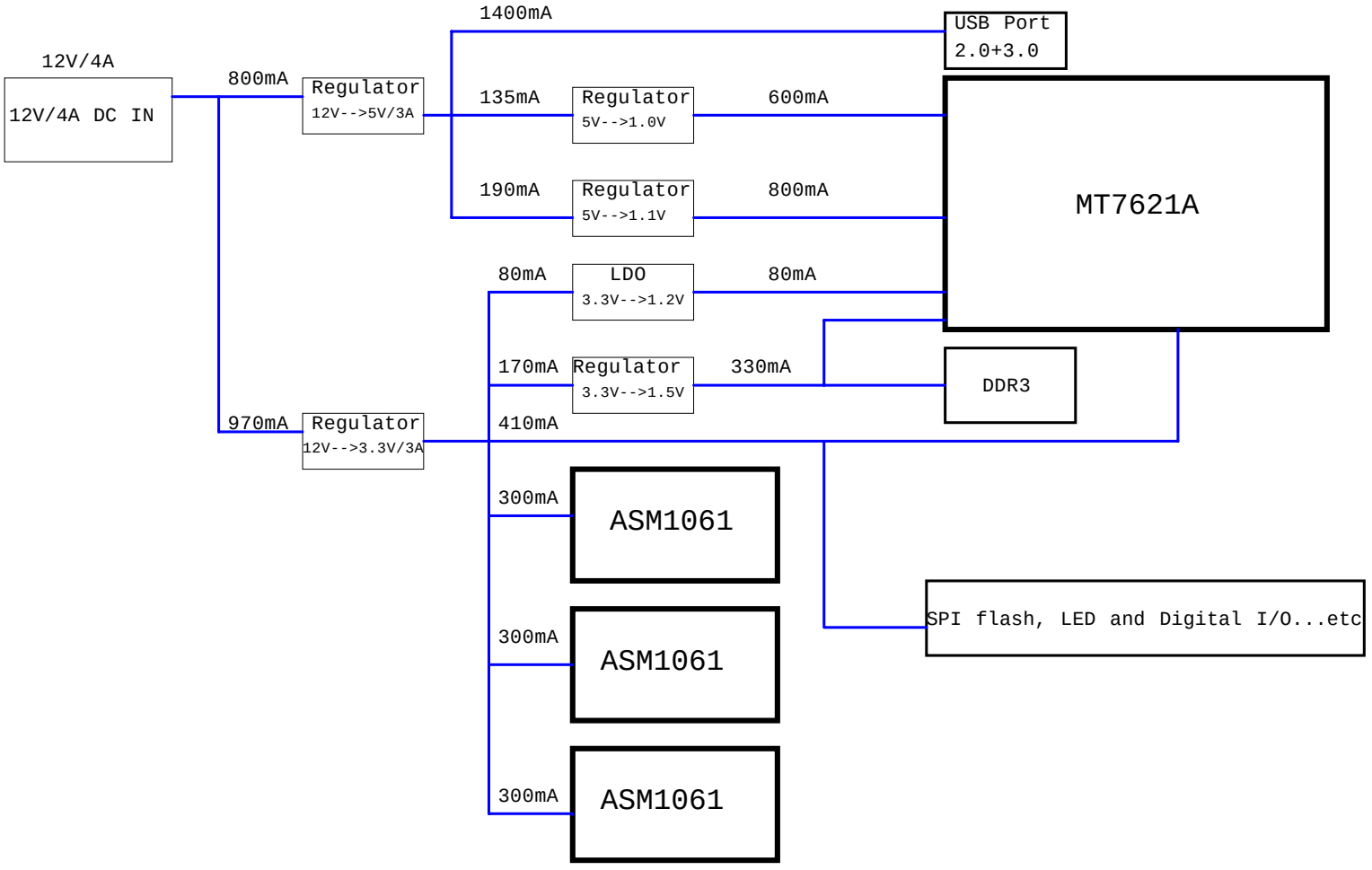
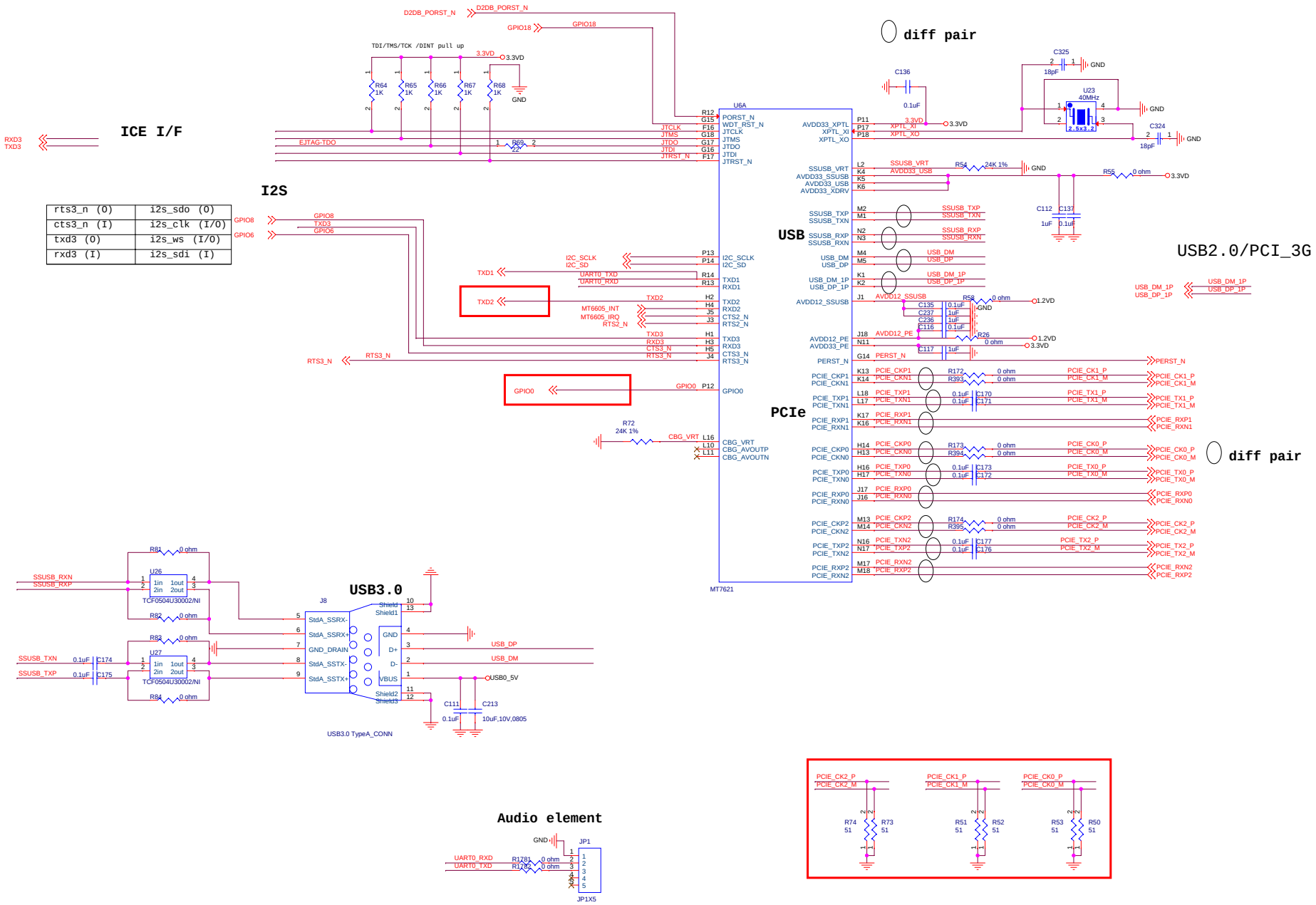

12V/4A
12V/4A DC IN
800mA
Regulator
12V-->5V/3A
970mA
Regulator
12V-->3.3V/3A
1400mA
USB Port
2.0+3.0
135mA
Regulator
5V-->1.0V
600mA
190mA
Regulator
5V-->1.1V
800mA
MT7621A
80mA
LDO
3.3V-->1.2V
80mA
170mA
Regulator
3.3V-->1.5V
330mA
DDR3
410mA
300mA
ASM1061
300mA
ASM1061
300mA
ASM1061
SPI flash, LED and Digital I/O...etc


ICE I/F
RXD3
TXD3
I2S
rts3_n (O) i2s_sdo (O)
cts3_n (I) i2s_clk (I/O)
txd3 (O) i2s_ws (I/O)
rxd3 (I) i2s_sdi (I)
GPIO8
GPIO6
TXD3
GPIO6
D2DB_PORST_N
GPIO18
TDI/TMS/TCK /DINT pull up
3.3VD
R64 1K
R65 1K
R66 1K
R67 1K
R68 1K
GND
EJTAG-TDO
R69 22
U6A
JTCLK
JTMS
JTDO
JTDI
JTRST_N
PORST_N
WDT_RST_N
TXD1
TXD2
RTS3_N
GPIO0
CBG_VRT
R72 24K 1%
CBG_AVOUTP
CBG_AVOUTN
I2C_SCLK
I2C_SD
UART0_TXD
UART0_RXD
MT6605_INT
MT6605_IRQ
RTS2_N
CTS2_N
CTS3_N
MT7621
diff pair
C136 0.1uF
C325 18pF
C324 18pF
U23 40MHz
2.5x3.2
XPTL_XI
XPTL_XO
USB
SSUSB_VRT
SSUSB_TXP
SSUSB_TXN
SSUSB_RXP
SSUSB_RXN
USB_DM
USB_DP
USB_DM_1P
USB_DP_1P
AVDD33_USB
R54 24K 1%
R55 0 ohm
C112 1uF
C137 0.1uF
USB2.0/PCI_3G
AVDD12_SSUSB
R58 0 ohm
1.2VD
C135 0.1uF
C237 1uF
C236 1uF
C116 0.1uF
AVDD12_PE
AVDD33_PE
R26 0 ohm
C117 1uF
PERST_N
PCIe
PCIE_CKP1
PCIE_CKN1
PCIE_TXP1
PCIE_TXN1
PCIE_RXP1
PCIE_RXN1
PCIE_CKP0
PCIE_CKN0
PCIE_TXP0
PCIE_TXN0
PCIE_RXP0
PCIE_RXN0
PCIE_CKP2
PCIE_CKN2
PCIE_TXP2
PCIE_TXN2
PCIE_RXP2
PCIE_RXN2
R172
R393
R173
R394
R174
R395
C170
C171
C173
C172
C177
C176
0 ohm
0.1uF
USB3.0
J8
StdA_SSRX-
StdA_SSRX+
GND_DRAIN
StdA_SSTX-
StdA_SSTX+
Shield
Shield1
Shield2
Shield3
GND
D+
D-
VBUS
USB_DP
USB_DM
USB0_5V
C111 0.1uF
C213 10uF,10V,0805
USB3.0 TypeA_CONN
R81 0 ohm
R82 0 ohm
R83 0 ohm
R84 0 ohm
U26
U27
TCF0504U30002/NI
SSUSB_RXN
SSUSB_RXP
SSUSB_TXN
SSUSB_TXP
C174 0.1uF
C175 0.1uF
Audio element
JP1
JP1X5
UART0_RXD
UART0_TXD
R1781 0 ohm
R1782 0 ohm
R74 51
R73 51
R51 51
R52 51
R53 51
R50 51

DDR3/DDR2 Interface
The pinout is differenet
when use DDR3 and DDR2

diff pair

Test Pad for signal measurement

U6B

MT7621

Nand Flash/ SD-XC/SPI Flash

SD Card Slot

DIP SPI Flash

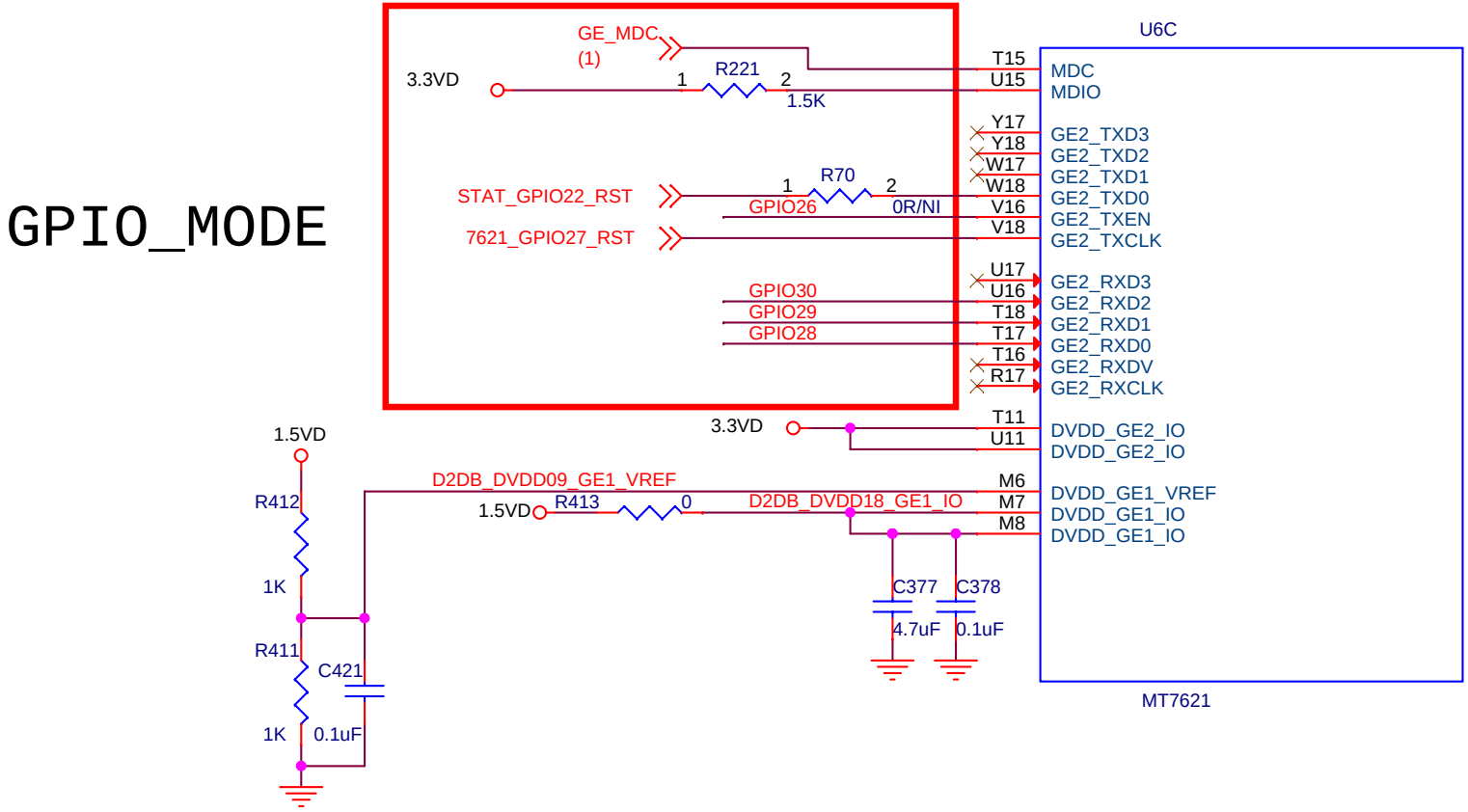
SMD SPI Flash

spi_cs0 (I/O)	nd_cs_n (O)
spi_cs1 (I/O)	nd_we_n (O)
spi_clk (I/O)	nd_re_n (O)
spi_miso (I/O)	nd_d[4] (I/O)
spi_mosi (I/O)	nd_d[5] (I/O)
spi_wp (I/O)	nd_d[6] (I/O)
spi_hold (I/O)	nd_d[7] (I/O)

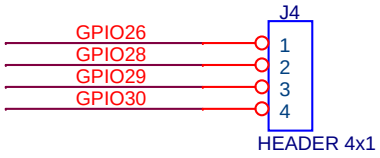
sd_wp (I)	nd_wp (O)
sd_clk (I/O)	nd_rb_n (I)
sd_cd (I)	nd_cle (O)
sd_cmd (I/O)	nd_ale (O)
sd_data[0] (I/O)	nd_d[0] (I/O)
sd_data[1] (I/O)	nd_d[1] (I/O)
sd_data[2] (I/O)	nd_d[2] (I/O)
sd_data[3] (I/O)	nd_d[3] (I/O)

RGMII Interface

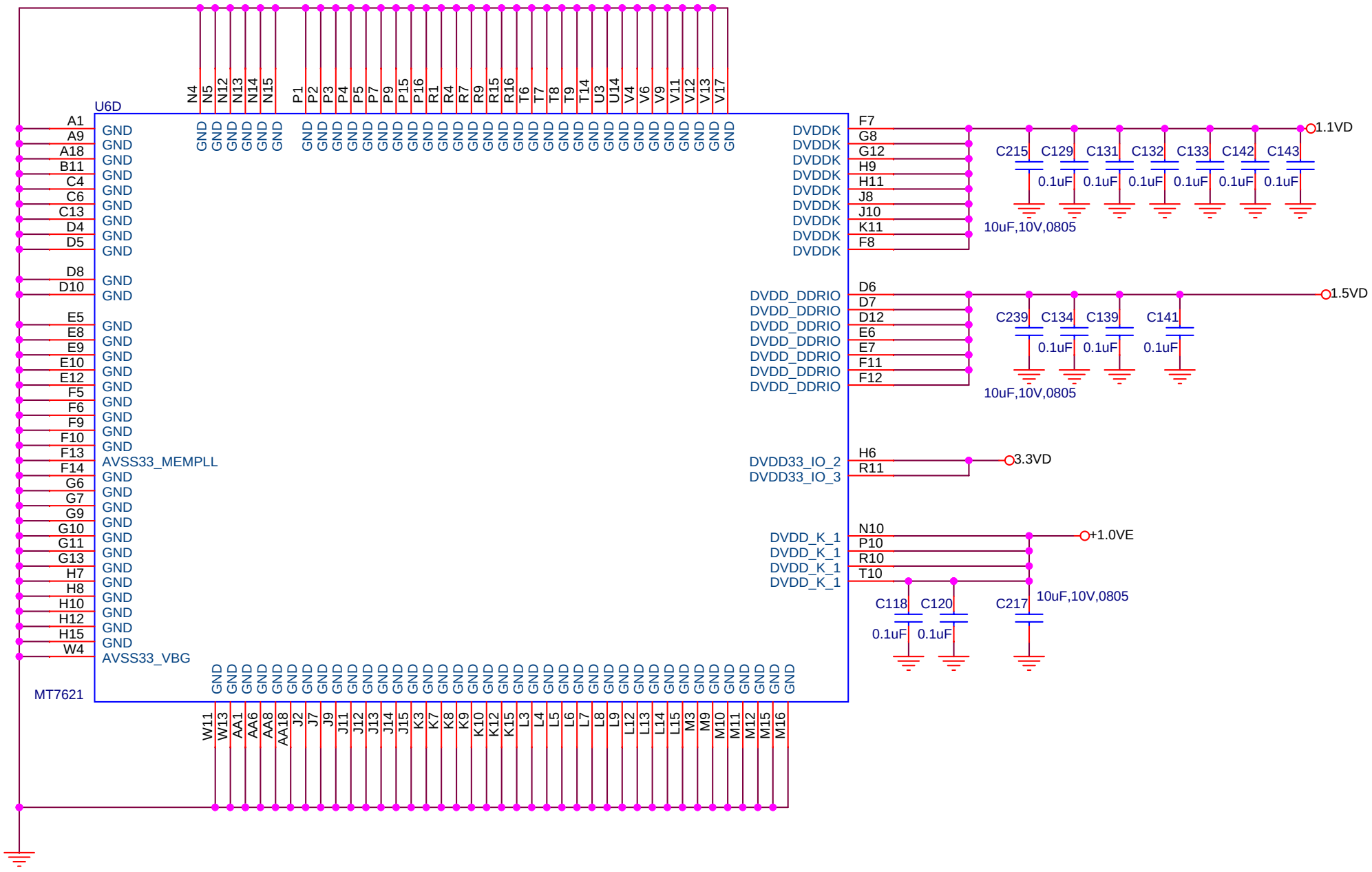
GPIO_MODE



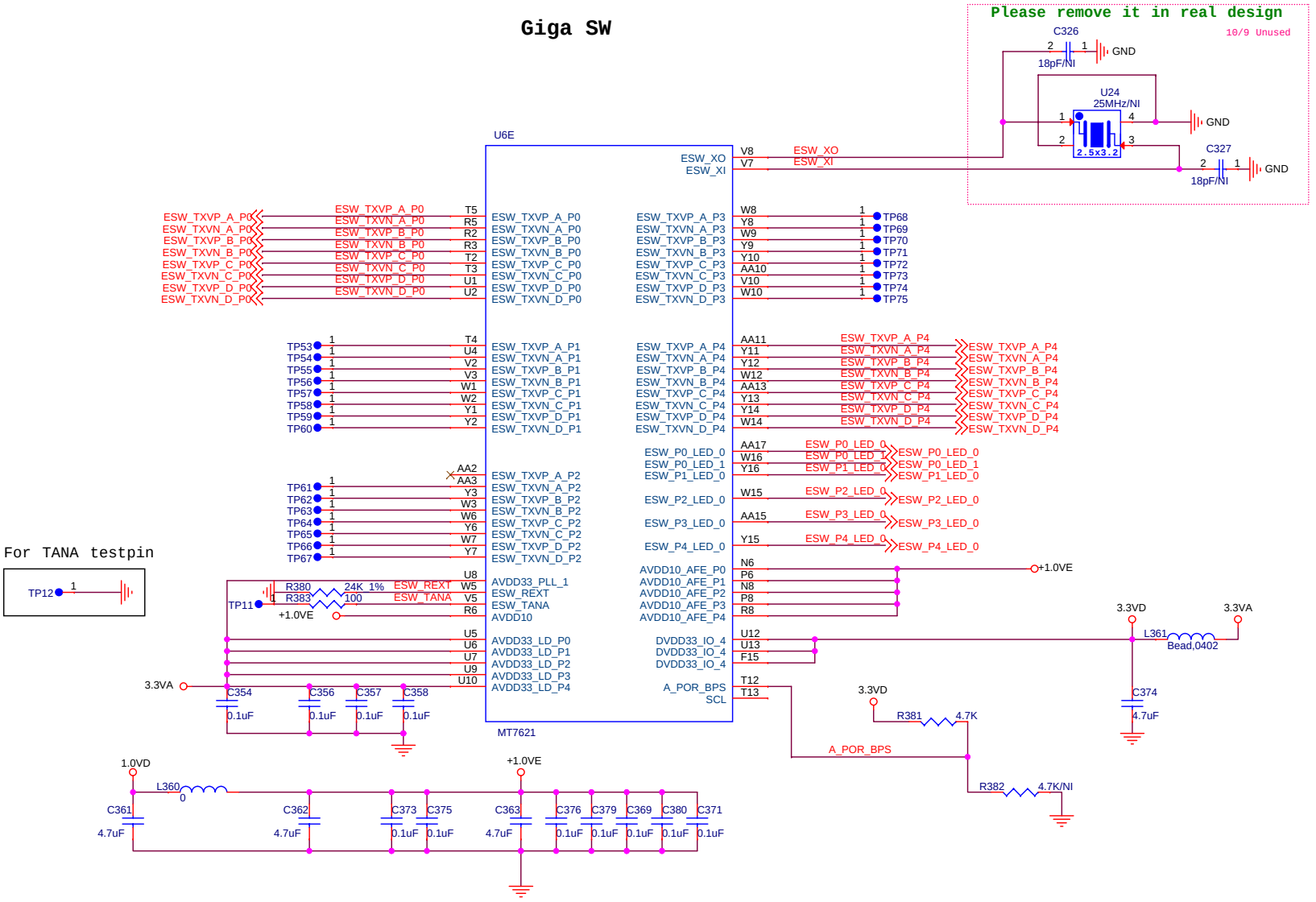
GPIO PART



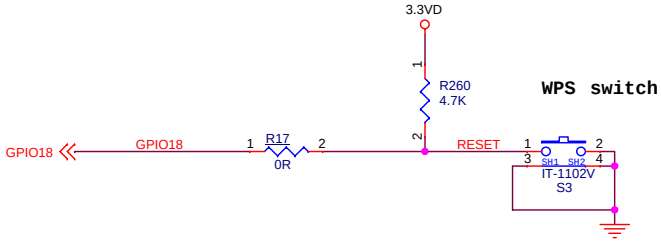
MT7621 Power



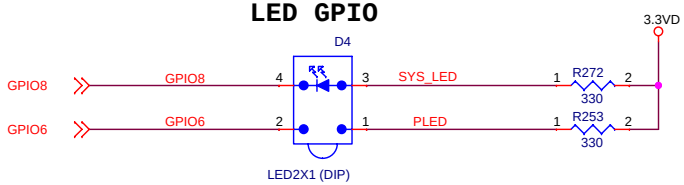
Giga SW


Please remove it in real design
10/9 Unused
C326
18pF/NI
GND
U24
25MHz/NI
2.5x3.2
C327
18pF/NI
U6E
MT7621
ESW_XO
ESW_XI
ESW_TXVP_A_P0
ESW_TXVN_A_P0
ESW_TXVP_B_P0
ESW_TXVN_B_P0
ESW_TXVP_C_P0
ESW_TXVN_C_P0
ESW_TXVP_D_P0
ESW_TXVN_D_P0
ESW_TXVP_A_P3
ESW_TXVN_A_P3
ESW_TXVP_B_P3
ESW_TXVN_B_P3
ESW_TXVP_C_P3
ESW_TXVN_C_P3
ESW_TXVP_D_P3
ESW_TXVN_D_P3
TP68
TP69
TP70
TP71
TP72
TP73
TP74
TP75
ESW_TXVP_A_P1
ESW_TXVN_A_P1
ESW_TXVP_B_P1
ESW_TXVN_B_P1
ESW_TXVP_C_P1
ESW_TXVN_C_P1
ESW_TXVP_D_P1
ESW_TXVN_D_P1
ESW_TXVP_A_P4
ESW_TXVN_A_P4
ESW_TXVP_B_P4
ESW_TXVN_B_P4
ESW_TXVP_C_P4
ESW_TXVN_C_P4
ESW_TXVP_D_P4
ESW_TXVN_D_P4
ESW_P0_LED_0
ESW_P0_LED_1
ESW_P1_LED_0
ESW_P2_LED_0
ESW_P3_LED_0
ESW_P4_LED_0
ESW_REXT
ESW_TANA
AVDD10
AVDD10_AFE_P0
AVDD10_AFE_P1
AVDD10_AFE_P2
AVDD10_AFE_P3
AVDD10_AFE_P4
AVDD33_PLL_1
AVDD33_LD_P0
AVDD33_LD_P1
AVDD33_LD_P2
AVDD33_LD_P3
AVDD33_LD_P4
DVDD33_IO_4
DVDD33_IO_4
DVDD33_IO_4
A_POR_BPS
SCL
For TANA testpin
TP12
TP11
R380 24K 1%
R383 100
+1.0VE
3.3VA
3.3VD
L361 Bead,0402
C354 0.1uF
C356 0.1uF
C357 0.1uF
C358 0.1uF
C374 4.7uF
R381 4.7K
R382 4.7K/NI
1.0VD
L360 0
C361 4.7uF
C362 4.7uF
C373 0.1uF
C375 0.1uF
C363 4.7uF
C376 0.1uF
C379 0.1uF
C369 0.1uF
C380 0.1uF
C371 0.1uF

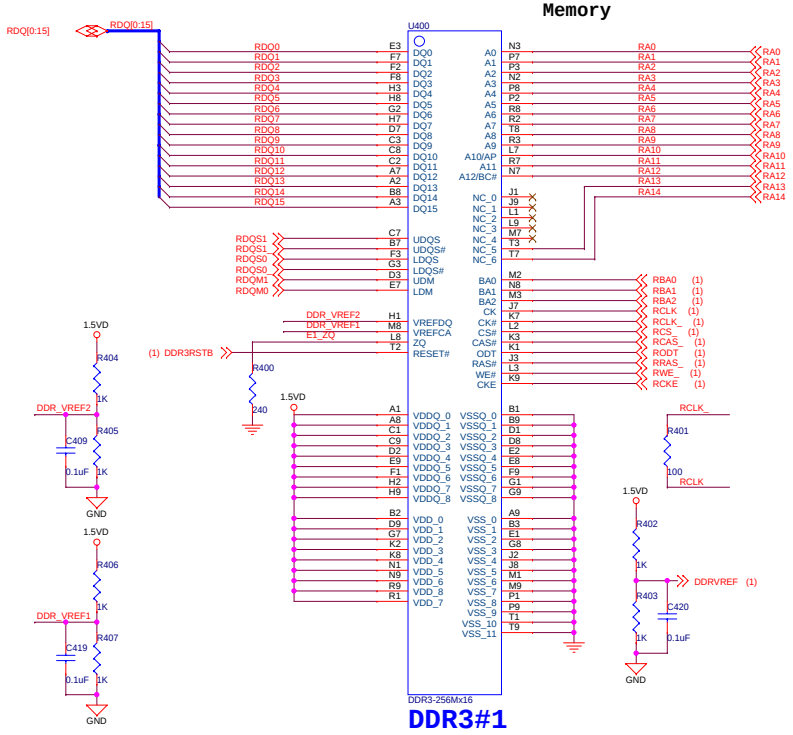
GPIO18/WPS/RESET

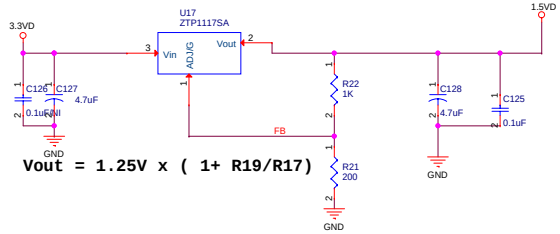


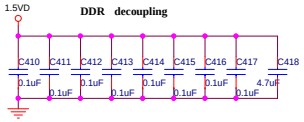
LED GPIO

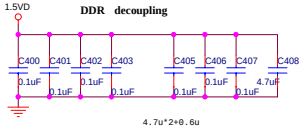


Memory


RDQ[0:15]
U400
DDR3-256Mx16
DDR3#1
1.5VD
GND
DDR_VREF2
DDR_VREF1
(1) DDR3RSTB
R400
240
R404
R405
R406
R407
C409
C419
0.1uF
1K
R401
100
RCLK
R402
R403
C420
DDRVREF (1)


3.3VD
U17
ZTP1117SA
Vin
Vout
ADJ/G
1.5VD
C126
C127
4.7uF
0.1uF
R22
1K
R21
200
FB
C128
C125
GND
Vout = 1.25V x (1+ R19/R17)


1.5VD
DDR decoupling
C410
C411
C412
C413
C414
C415
C416
C417
C418
0.1uF
4.7uF

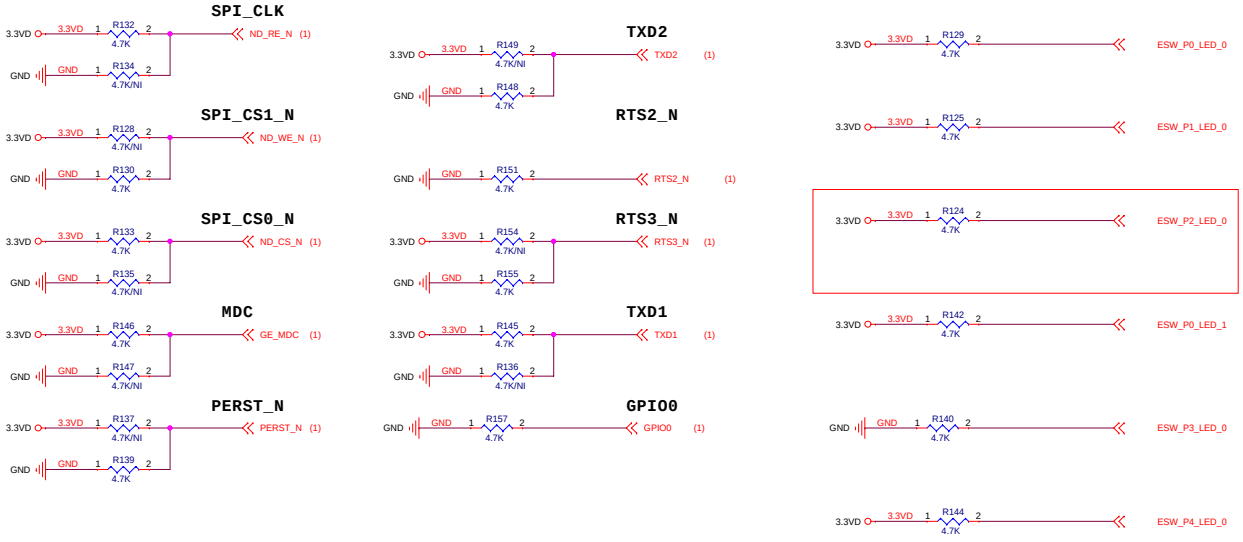

1.5VD
DDR decoupling
C400
C401
C402
C403
C405
C406
C407
C408
0.1uF
4.7uF
4.7u*2+0.6u

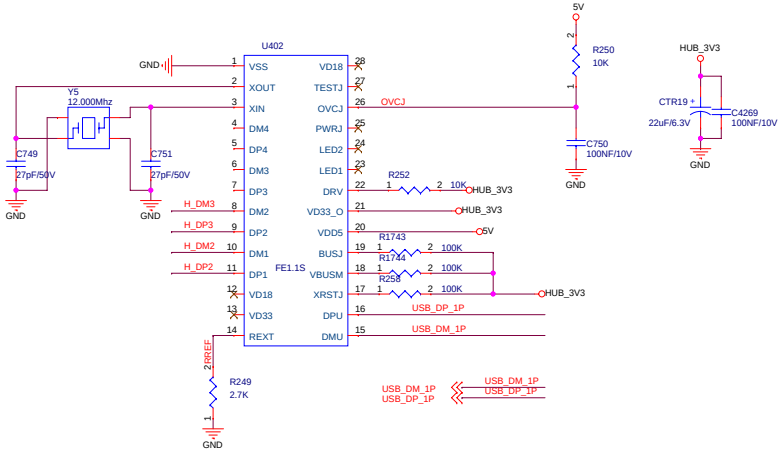
Boot Strapping

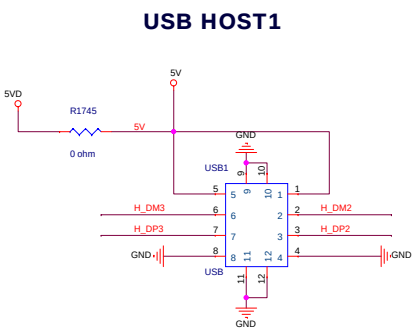
Pin Name	Description	Value	
SPI_CLK	DRAM_FROM_EE	For non scan mode: 0: DRAM/PLL configuration from EEPROM **1: DRAM configuration from Auto Detect**	For FT mode: 0: SUTIF 1: 3-wire SPI
{SPI_CS1_N, SPI_CS0_N, MDC }	XTAL_MODE	000: 20 MHz, Self Oscillation mode 001: 20 MHz, Single end input 010: 20 MHz, differential input **011: 40 MHz, Self Oscillation mode**	100: 40 MHz, Single end input 101: 40 MHz, differential input 110: 25 MHz, Self Oscillation mode 111: 25 MHz, Single end input
PERST_N	OCP_RATIO	**0: 1:3** 1: 1:4	
TXD2	DRAM_TYPE	**0: DDR3** 1: DDR2	
{RTS2_N, RTS3_N, TXD1, GPIO0}	CHIP_MODE[3:0]	0000: Normal / Boot from SPI 4-byte address and XTAL clock 0001: Normal / Boot from ROM (NAND page 2k+64 bytes) **0010: Normal / Boot from SPI 3-byte address** 0011: Normal / Boot from SPI 4-byte address 0100: iNIC RGMI / Boot from ROM 0101: iNIC MII / Boot from ROM 0110: iNIC RVMII / Boot from ROM 0111: iNIC PHY / Boot from ROM 1000: iNIC RGMII / Boot from ROM and XTAL clock 1001: Normal / Boot from internal SRAM 1010: Normal / Boot from ROM (NAND page 2k+128 bytes) 1011: Normal / Boot from ROM (NAND page 4k+128 bytes) 1100: Normal / Boot from ROM (NAND page 4k+224 bytes) 1101: Debug mode 1110: Scan mode 1111: Final Test	

Giga Switch Hardware Trap

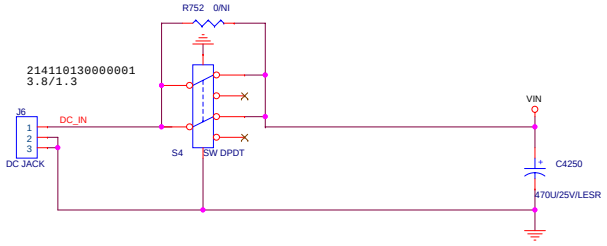
Pin Name	Trap	Fuction	Description	Default
P0_LED_0	HWTRAP[0]	HT_CHIP_MODE[0]	chip_mode[3:0] 4'b0000: IDDQ mode 4'b0001: IOTEST mode 4'b0010: NANDTREE mode 4'b0011: RING mode (both IO and std-cell) 4'b0100: MBIST 4'b0101: SCAN mode (internal) 4'b0110: SCAN-COMP mode (compression) 4'b0111: SCAN-MBIST-OLT mode 4'b1000: AFE-OLT mode 4'b1001: GPHY ATE mode 4'b1010: GPHY ADUMP mode 4'b1011: GPHY ADUMP probe mode 4'b1100: Reserved 4'b1101: Reserved 4'b1110: bootup probe mode 4'b1111: normal mode	4'b1111
P1_LED_0	HWTRAP[1]	HT_CHIP_MODE[1]		
P2_LED_0	HWTRAP[2]	HT_CHIP_MODE[2]		
P0_LED_1	HWTRAP[3]	HT_CHIP_MODE[3]		
P3_LED_0	HWTRAP[9]	HT_XTAL_FSEL[0]	External Crystal Frequency Selection xtal_freq_sel[1:0] 2'b01: 20MHz 2'b10: 40MHz 2'b11: 25MHz	2'b10
P4_LED_0	HWTRAP[10]	HT_XTAL_FSEL[1]		



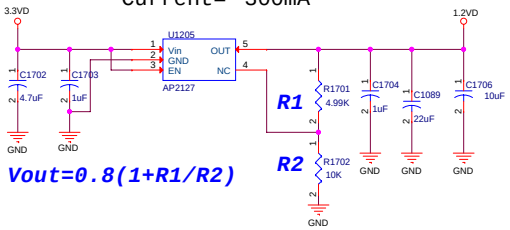

U402
FE1.1S
VSS
XOUT
XIN
DP4
DM3
DP3
DM2
DP2
DM1
DP1
VD18
VD33
REXT
VD18
TESTJ
OVCJ
PWRJ
LED2
LED1
DRV
VD33_O
VDD5
BUSJ
VBUSM
XRSTJ
DPU
DMU
GND
YS
12.000Mhz
C749
27pF/50V
C751
27pF/50V
H_DM3
H_DP3
H_DM2
H_DP2
R252
10K
HUB_3V3
R1743
100K
R1744
100K
R253
100K
5V
R250
10K
C750
100NF/10V
OVCJ
USB_DP_1P
USB_DM_1P
2REF
R249
2.7K
HUB_3V3
CTR19
22uF/6.3V
C4269
100NF/10V


USB HOST1
5VD
R1745
0 ohm
5V
GND
USB1
USB
H_DM3
H_DP3
H_DM2
H_DP2
GND

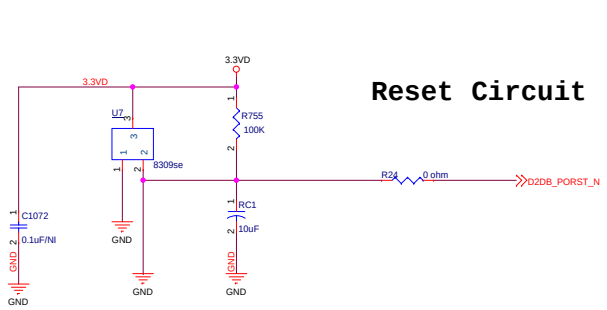
System Power



For USB/PCIe PHY Power (1.2V)
Current= 300mA

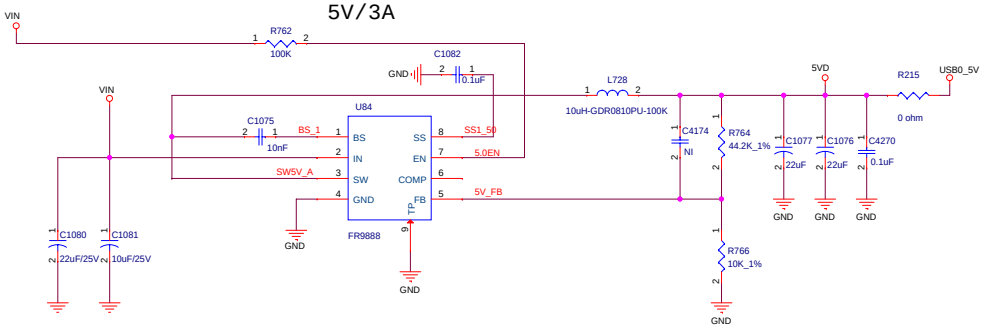


Vout=0.8(1+R1/R2)



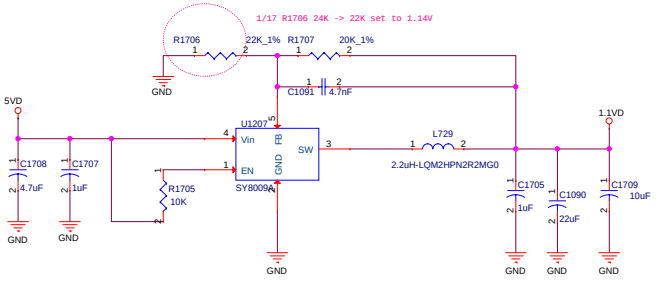
Reset Circuit

5V/3A

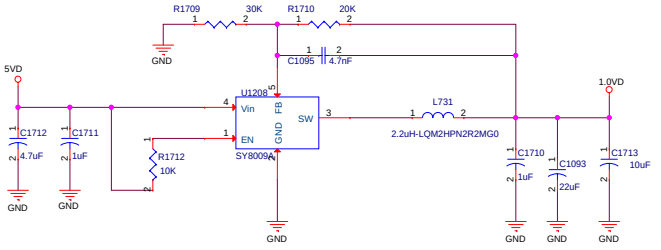


Vout=0.92(1+R255/R256)

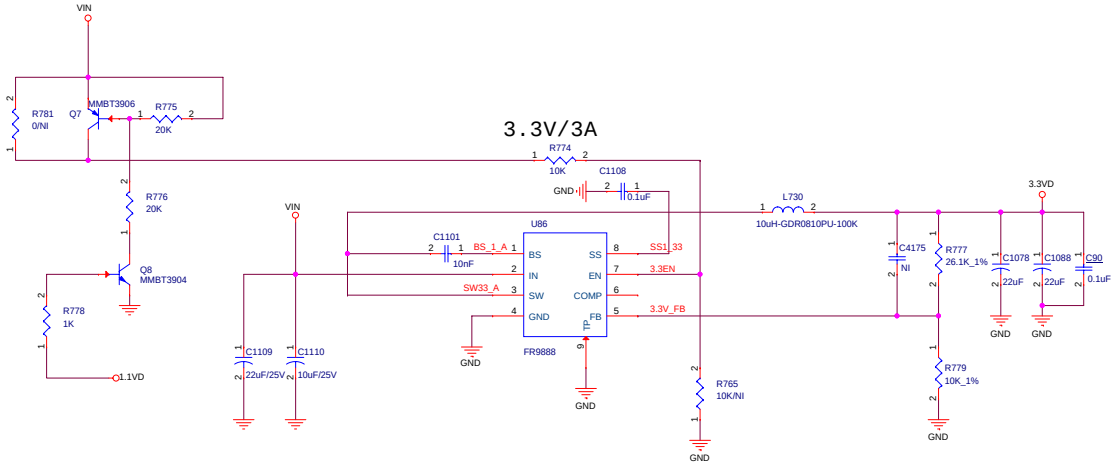
1.14V/1.5A



1.0V/1.5A

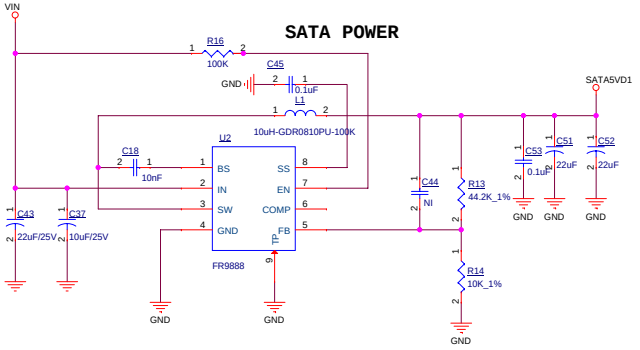


3.3V/3A

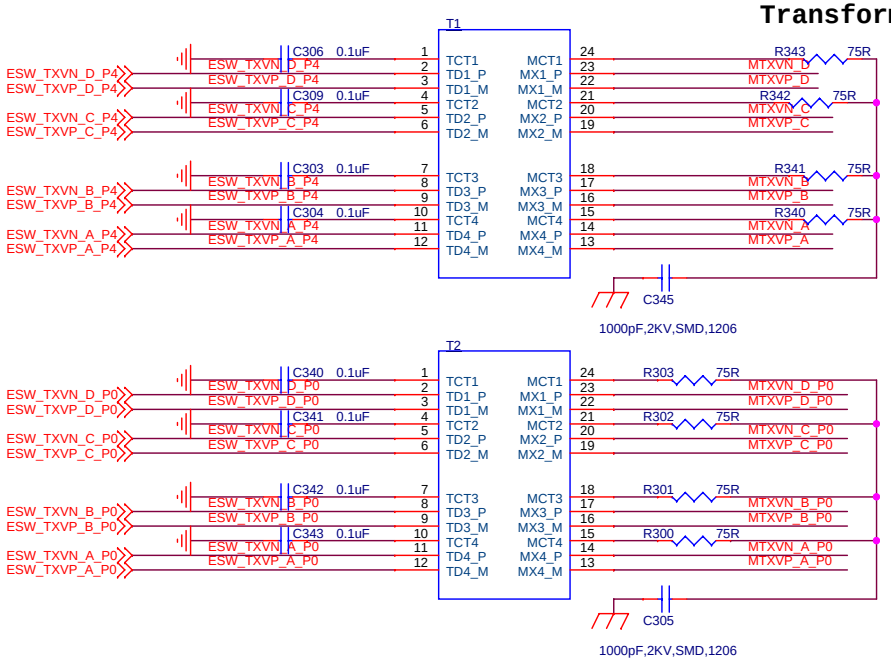


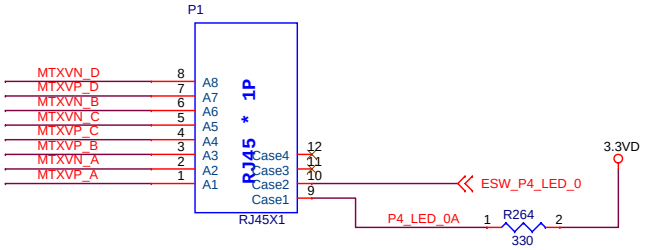
Vout=0.92(1+R251/R252)

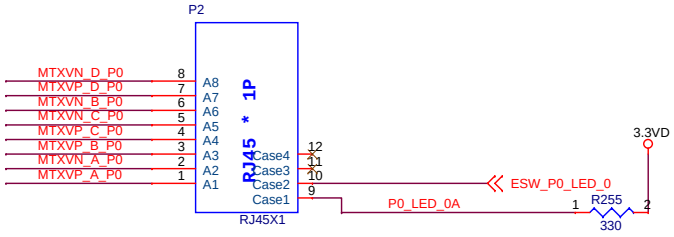
SATA POWER



Transformer

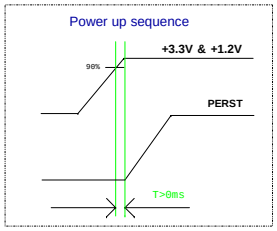




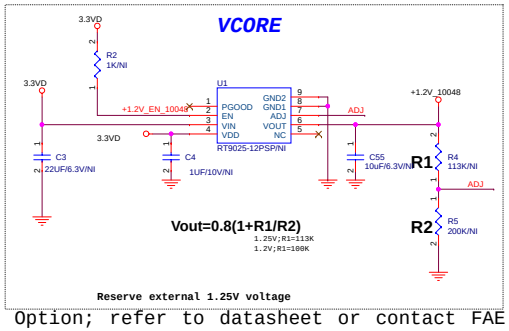


PCIe to SATA

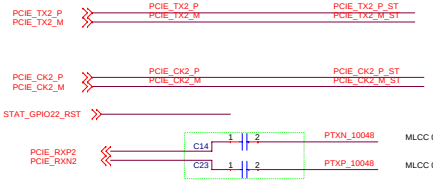
Power up sequence



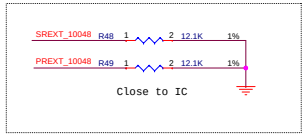
VCORE



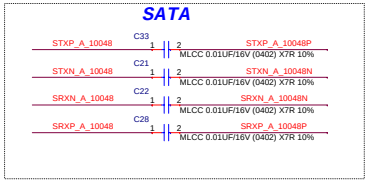
Option; refer to datasheet or contact FAE

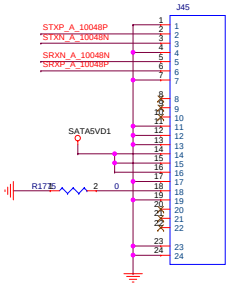


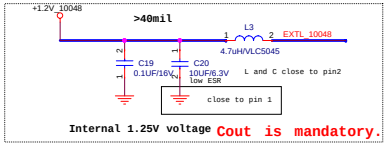
Close to PCIe Slot
X7R/0402 type



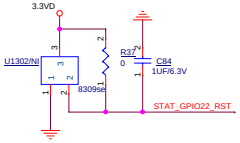
SATA

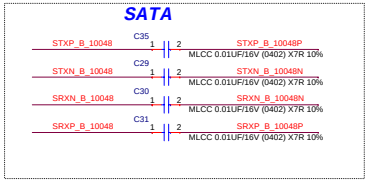


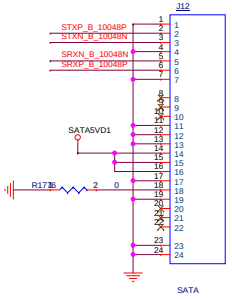




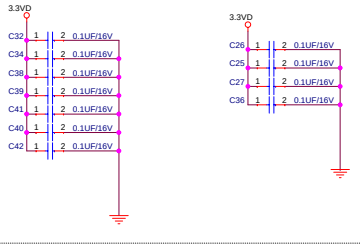
Internal 1.25V voltage **Cout is mandatory.**

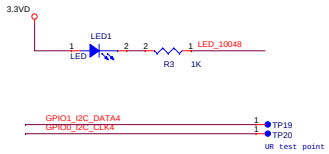


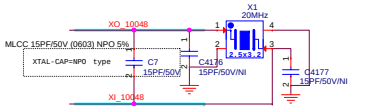




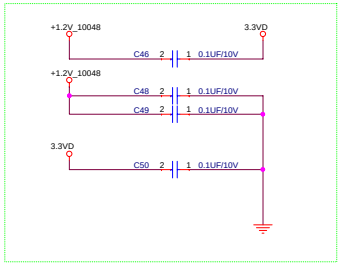
Close to ASM1061







XI & XO follow differential layout rule for Min. jitter



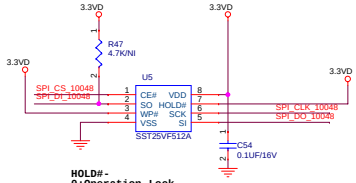
H/W Strapping

refer to datasheet:

SPI_DO
0: Spin up by H/W
1: Spin up by S/W

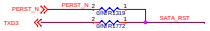
SPI ROM

refer to support list

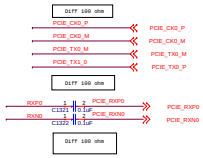


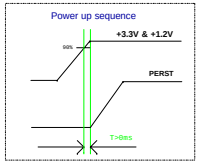
HOLD#-
0:Operation Lock
1:Normal Operation

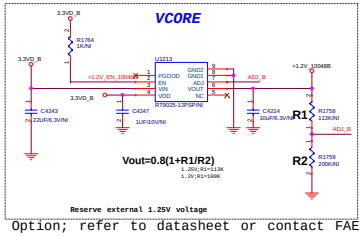
PCIe to SATA



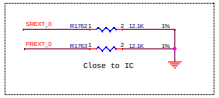
Close to PCIe Slot

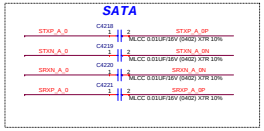


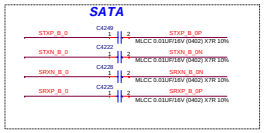


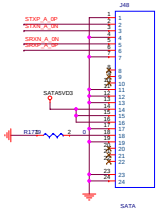


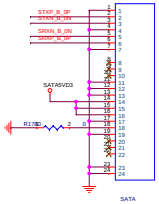
Option; refer to datasheet or contact FAE

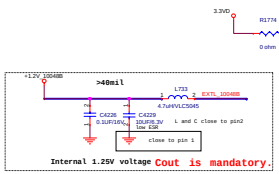


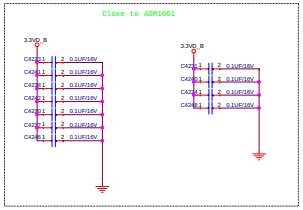


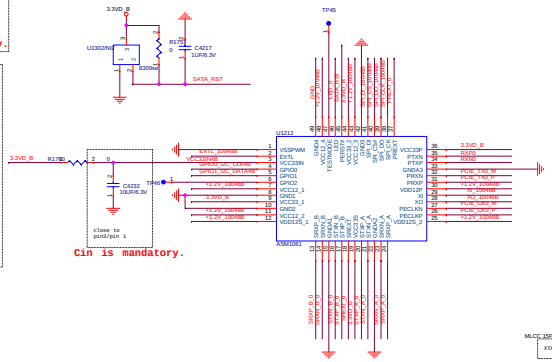


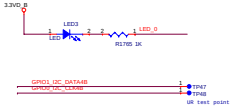


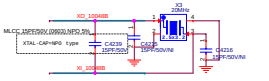


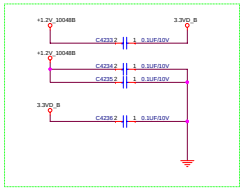








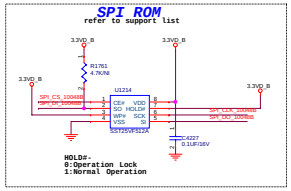




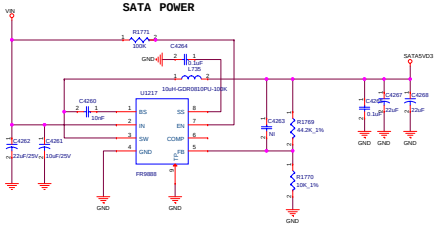
H/W Strapping

refer to datasheet:

SPI_DO
0: Spin up by H/W
1: Spin up by S/W

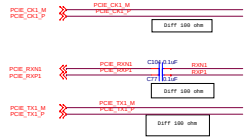


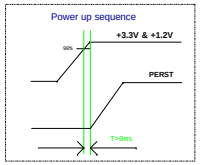
SATA POWER

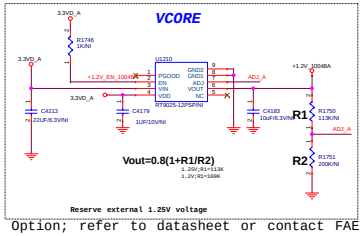


PCIe to SATA

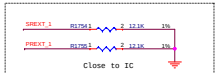
Close to PCIe Slot

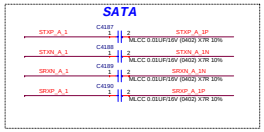


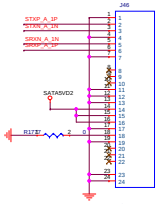


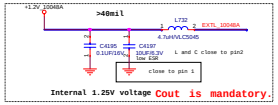


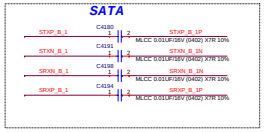
Option; refer to datasheet or contact FAE

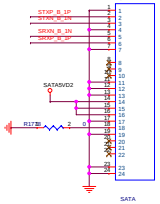


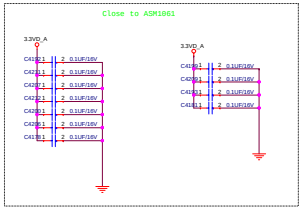


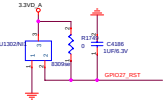


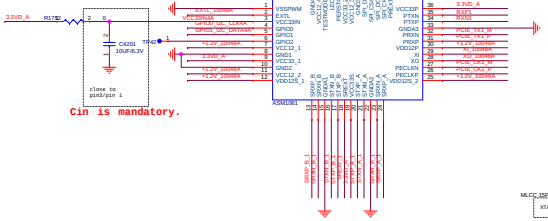


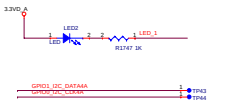


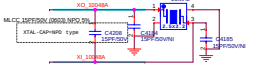




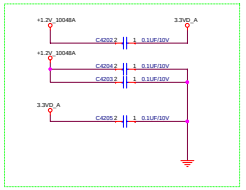








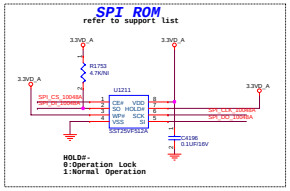
X1 & XO follow differential layout rule for Min. jitter



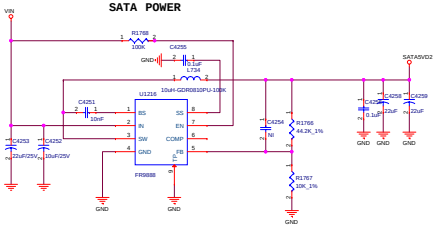
H/W Strapping

refer to datasheet:

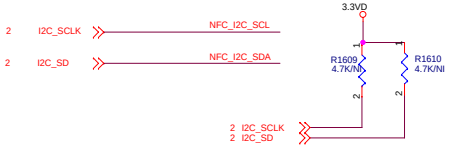
SPI_DO
0: Spin up by H/W
1: Spin up by S/W



SATA POWER




MT6605_INT
NFC_EINT
1
TP49
2 MT6605_IRQ
NFC_IRQ
1
TP50


3.3VD
2 I2C_SCLK
NFC_I2C_SCL
2 I2C_SD
NFC_I2C_SDA
R1609
4.7K/NI
R1610
4.7K/NI
2 I2C_SCLK
2 I2C_SD