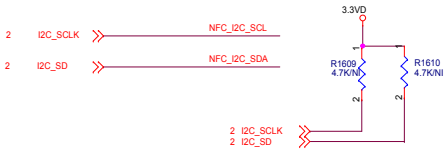
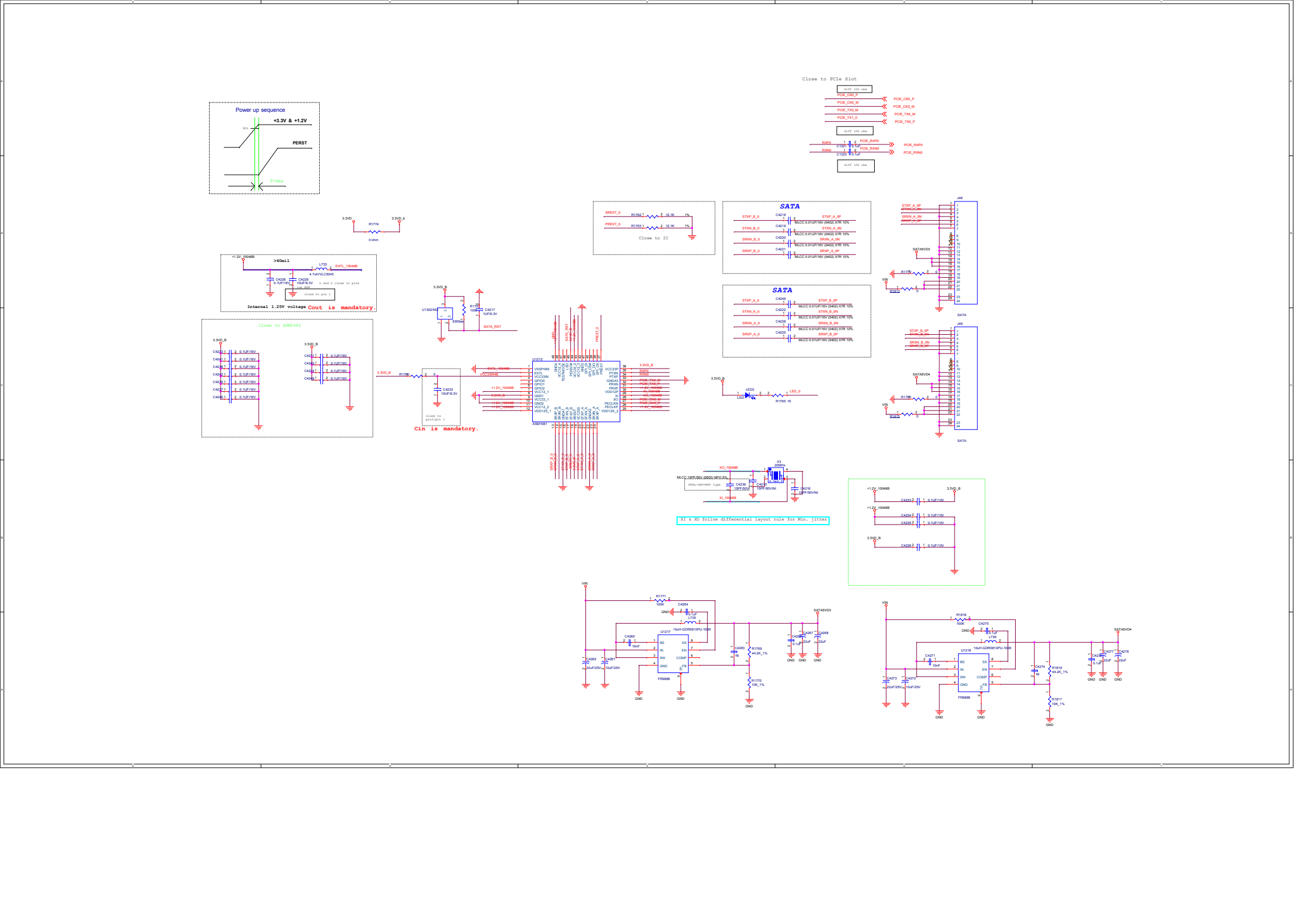
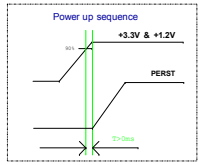
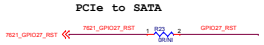

MT6605_INT
NFC_EINT
1
TP49
2 MT6605_IRQ
NFC_IRQ
1
TP50


3.3VD
2 I2C_SCLK
NFC_I2C_SCL
2 I2C_SD
NFC_I2C_SDA
R1609
4.7K/NI
R1610
4.7K/NI
2 I2C_SCLK
2 I2C_SD

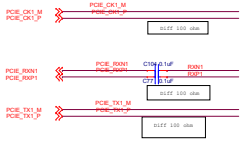

Power up sequence
+3.3V & +1.2V
PERST
T>0ms
Close to PCIe Slot
diff 100 ohm
PCIE_CK0_P
PCIE_CK0_M
PCIE_TX0_M
PCIE_TX0_P
PCIE_TX1_0
PCIE_RXP0
PCIE_RXN0
C1321 0.1uF
C1322 0.1uF
SATA
STXP_A_0
STXN_A_0
SRXN_A_0
SRXP_A_0
STXP_B_0
STXN_B_0
SRXN_B_0
SRXP_B_0
MLCC 0.01UF/16V (0402) X7R 10%
J48
J49
SATA5VD3
SATA5VD4
R1775
R1776
R1777
R1778
SREXT_0
PREXT_0
R1762 12.1K 1%
R1763 12.1K 1%
Close to IC
3.3VD
3.3VD_b
R1774
0 ohm
+1.2V_1004BB
>40mil
L733
EXTL_1004BB
4.7uH/VLC5045
C4228 0.1UF/16V
C4229 10UF/6.3V
L and C close to pin2
low ESR
close to pin 1
Internal 1.25V voltage Cout is mandatory.
Close to ASM1061
3.3VD_B
C4221 0.1UF/16V
C4222 0.1UF/16V
C4223 0.1UF/16V
C4224 0.1UF/16V
C4225 0.1UF/16V
C4226 0.1UF/16V
C4227 0.1UF/16V
C4228 0.1UF/16V
C4229 0.1UF/16V
C4230 0.1UF/16V
C4231 0.1UF/16V
U1302/N2
R1779 100K
C4217 1UF/6.3V
SATA_RST
R1780 0
C4232 10UF/6.3V
close to pin3/pin 1
Cin is mandatory.
U1212
ASM1061
VSSPWM
EXTL
VCC33IN
GPIO0
GPIO1
GPIO2
VCC12_1
GND1
VCC33_1
VCC33
VCC12_2
VDD12S_1
VCC33P
PTXN
PTXP
GNDA3
PRXN
PRXP
VDD12P
X1
X2
PECLKN
PECLKP
VDD12S_2
PCIE_TX0_M
PCIE_TX0_P
PCIE_CK0_M
PCIE_CK0_P
PCIE_RX0_M
PCIE_RX0_P
XO_1004BB
XI_1004BB
X3
25MHz
C4238 15PF/50V/NI
C4239 15PF/50V
C4216 15PF/50V/NI
MLCC 15PF/50V (0603) NPO 5%
XTAL-CAP-SMD type
XI & XO follow differential layout rule for Min. jitter
LED3
LED_0
R1765 1K
+1.2V_1004BB
3.3VD_B
C4253 0.1UF/10V
C4254 0.1UF/10V
C4255 0.1UF/10V
C4256 0.1UF/10V
VIN
R1771 100K
C4264 0.1uF
L735
10uH-GDR0810PU-100K
U1217
FR9888
C4265 10nF
C4262 22uF/25V
C4261 10UF/25V
C4263 NI
R1769 44.2K_1%
R1770 10K_1%
C4267 22uF
C4268 22uF
C4269 0.1uF
GND
SATA5VD3
R1818 100K
C4275 0.1uF
L736
C4271 10nF
C4273 22uF/25V
C4272 10UF/25V
C4274 NI
R1816 44.2K_1%
R1817 10K_1%
C4277 22uF
C4278 22uF
C4276 0.1uF
SATA5VD4

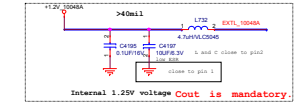
PCIe to SATA

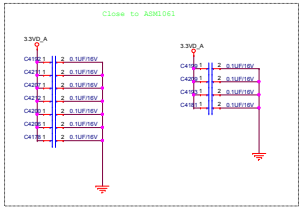


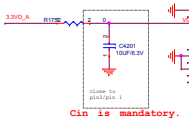


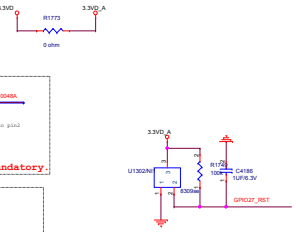
Close to PCIe Slot

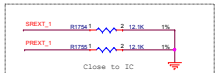


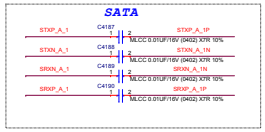


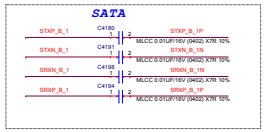


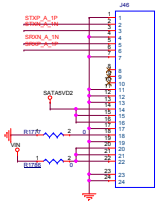


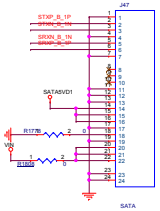


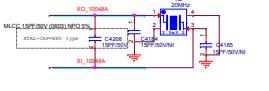




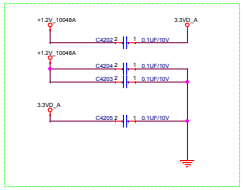


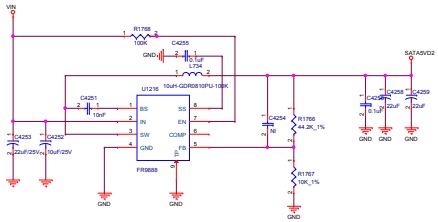


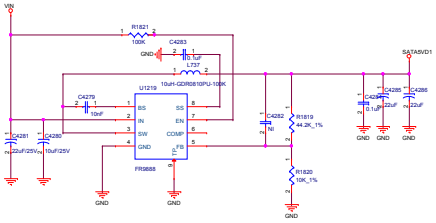




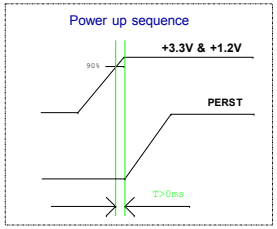
X1 & X2 follow differential layout rule for Min. jitter







PCIe to SATA



PCIE_TX2_P
PCIE_TX2_M
PCIE_TX2_P
PCIE_TX2_M
PCIE_TX2_P_ST
PCIE_TX2_M_ST
PCIE_CK2_P
PCIE_CK2_M
PCIE_CK2_P
PCIE_CK2_M
PCIE_CK2_P_ST
PCIE_CK2_M_ST
STAT_GPIO22_RST
PCIE_RXP2
PCIE_RXN2
C14 PTXN_10048 MLCC 0.1UF/16V (0402) X7R 10%
C23 PTXP_10048 MLCC 0.1UF/16V (0402) X7R 10%
Close to PCIe Slot
X7R/0402 type

SREXT_10048 R48 12.1K 1%
PREXT_10048 R49 12.1K 1%
Close to IC

SATA
STXP_A_10048 C33 MLCC 0.01UF/16V (0402) X7R 10% STXP_A_10048P
STXN_A_10048 C21 MLCC 0.01UF/16V (0402) X7R 10% STXN_A_10048N
SRXN_A_10048 C22 MLCC 0.01UF/16V (0402) X7R 10% SRXN_A_10048N
SRXP_A_10048 C28 MLCC 0.01UF/16V (0402) X7R 10% SRXP_A_10048P

SATA
STXP_B_10048 C35 MLCC 0.01UF/16V (0402) X7R 10% STXP_B_10048P
STXN_B_10048 C29 MLCC 0.01UF/16V (0402) X7R 10% STXN_B_10048N
SRXN_B_10048 C30 MLCC 0.01UF/16V (0402) X7R 10% SRXN_B_10048N
SRXP_B_10048 C31 MLCC 0.01UF/16V (0402) X7R 10% SRXP_B_10048P

J45
STXP_A_10048P
STXN_A_10048N
SRXN_A_10048N
SRXP_A_10048P
SATA5VDA
R1775 0
VIN
R1800 0
SATA

J12
STXP_B_10048P
STXN_B_10048N
SRXN_B_10048N
SRXP_B_10048P
SATA5VD0
R1776 0
VIN
R1804 0
SATA

+1.2V_10048
>40mil
L3 4.7uHVLC5045
EXTL_10048
C19 0.1UF/16V
C20 10UF/6.3V low ESR
L and C close to pin2
close to pin 1
Internal 1.25V voltage **Cout is mandatory.**

Close to ASM1061
3.3VD
C32 C34 C38 C39 C41 C40 C42 0.1UF/16V
C26 C25 C27 C36 0.1UF/16V

3.3VD
U1302/NI
R27 100K
C84 1UF/6.3V
8309se
STAT_GPIO22_RST

3.3VD R8 0
C24 10UF/6.3V
close to pin3/pin 1
Cin is mandatory.

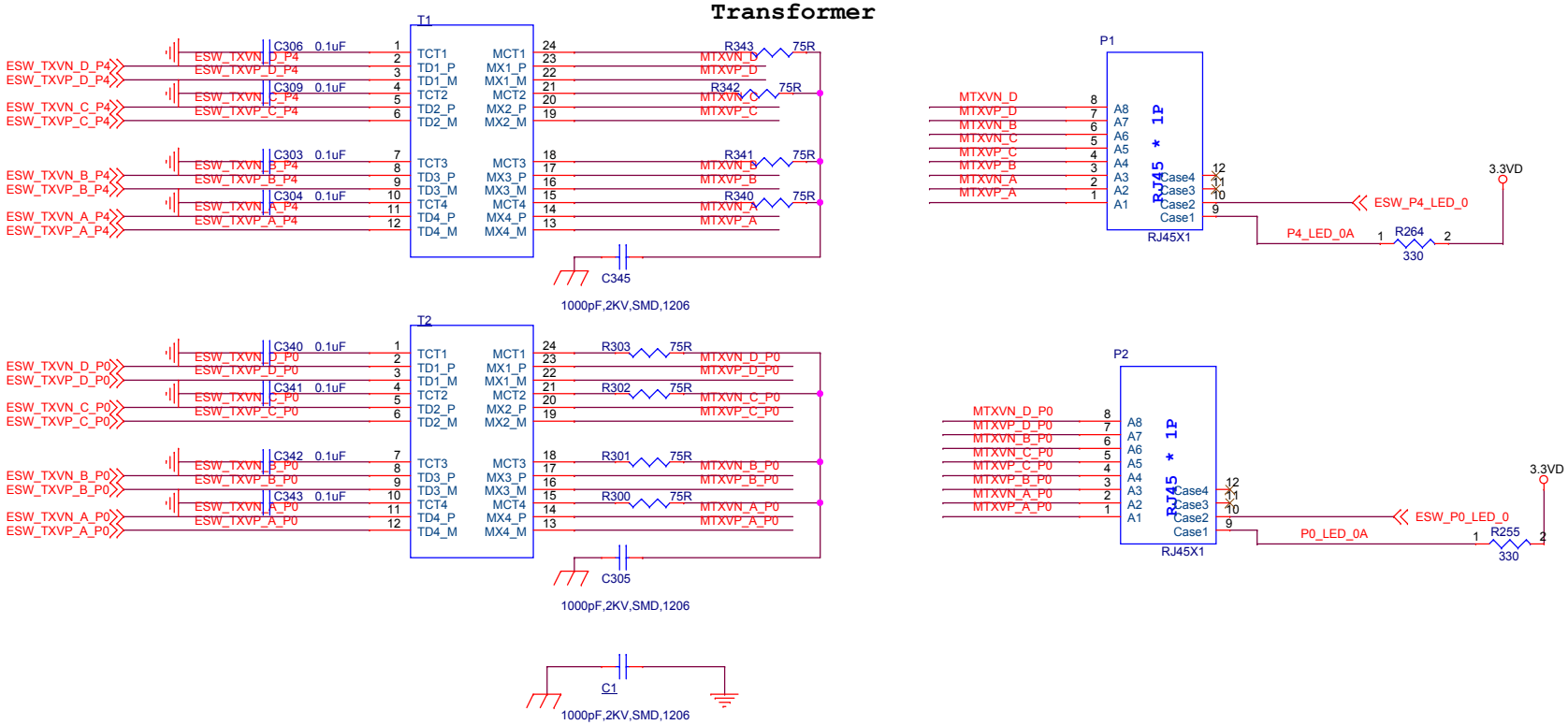
U9 ASM1061
VSSPWM
EXTL
VCC33IN
GPIO0
GPIO1
GPIO2
VCC12_1
GND1
VCC33_1
GND2
VCC12_2
VDD12S_1
VCC33P
PTXN
PTXP
GNDA3
PRXN
PRXP
VDD12P
XI
XO
PECLKN
PECLKP
VDD12S_2
PREXT
GND
+1.2V_10048
STAT_GPIO22_RST
3.3VD
PTXN_10048
PTXP_10048
PCIE_TX2_N_ST
PCIE_TX2_P_ST
XI_10048
PCIE_CK2_N_ST
PCIE_CK2_P_ST
SRXP_B_10048
SRXN_B_10048
STXN_B_10048
STXP_B_10048
SREXT
STXN_A_10048
STXP_A_10048
SRXN_A_10048
SRXP_A_10048

X1 20MHz
XO_10048
MLCC 15PF/50V (0603) NPO 5%
XTAL-CAP-NPO type
C7 15PF/50V
C4176 15PF/50V/NI
C4177 15PF/50V/NI
XI_10048
XI & XO follow differential layout rule for Min. jitter

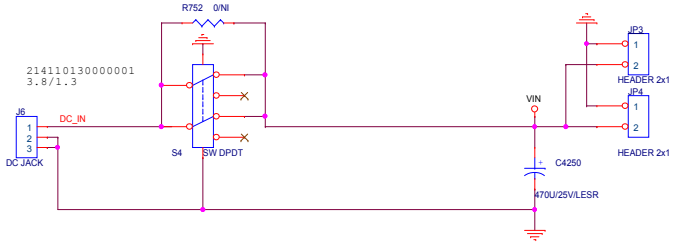
+1.2V_10048
3.3VD
C46 0.1UF/10V
+1.2V_10048
C48 0.1UF/10V
C49 0.1UF/10V

VIN
R1824 100K
C4291 0.1uF
GND
L738 10uH-GDR0810PU-100K
SATA5VD0
U1220 FR9888
BS
IN
SW
GND
SS
EN
COMP
FB
TP
C4287 10nF
C4289 22uF/25V
C4288 10uF/25V
C4290 NI
R1822 44.2K_1%
R1823 10K_1%
C4292 0.1uF
C4293 22uF
C4294 22uF
GND

Transformer

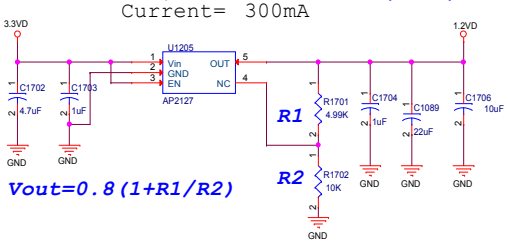


System Power

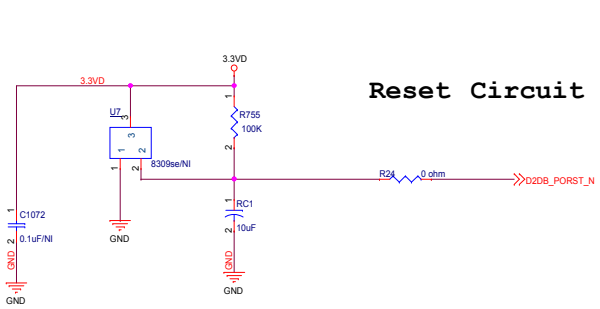


For USB/PCIe PHY Power (1.2V)

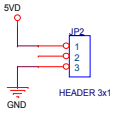
Current= 300mA



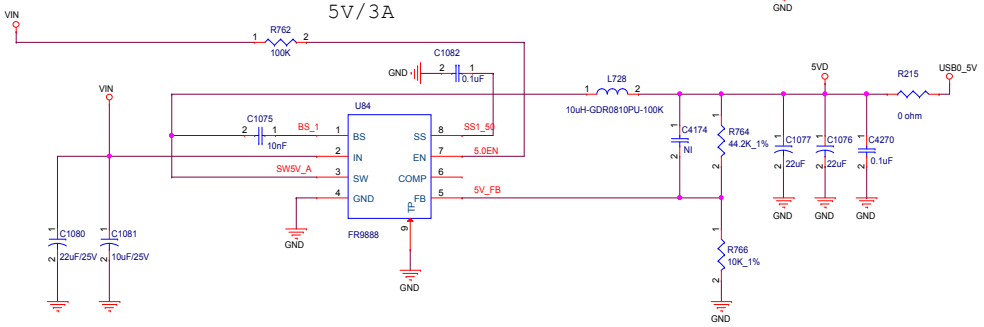
Vout=0.8(1+R1/R2)



Reset Circuit

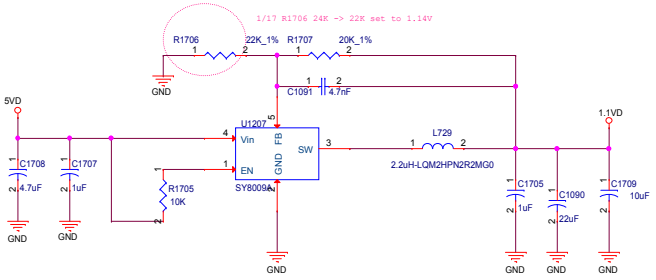


5V/3A

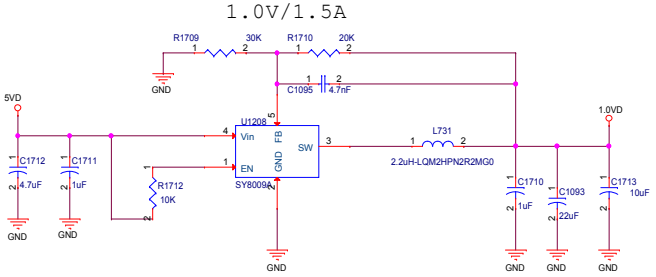


Vout=0.92(1+R255/R256)

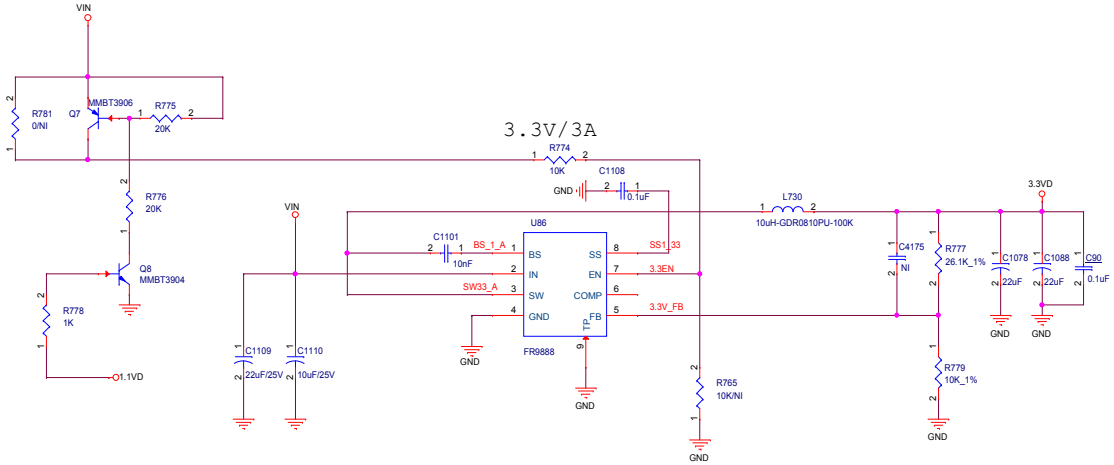
1.14V/1.5A



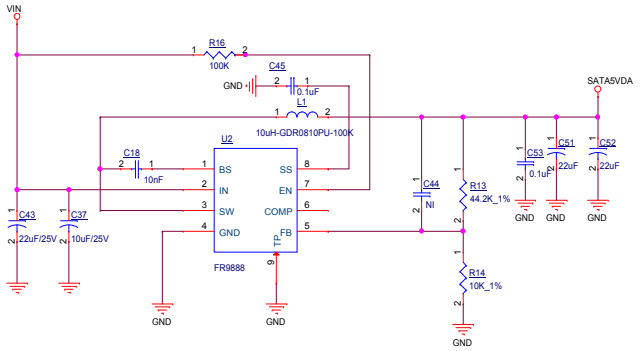
1.0V/1.5A

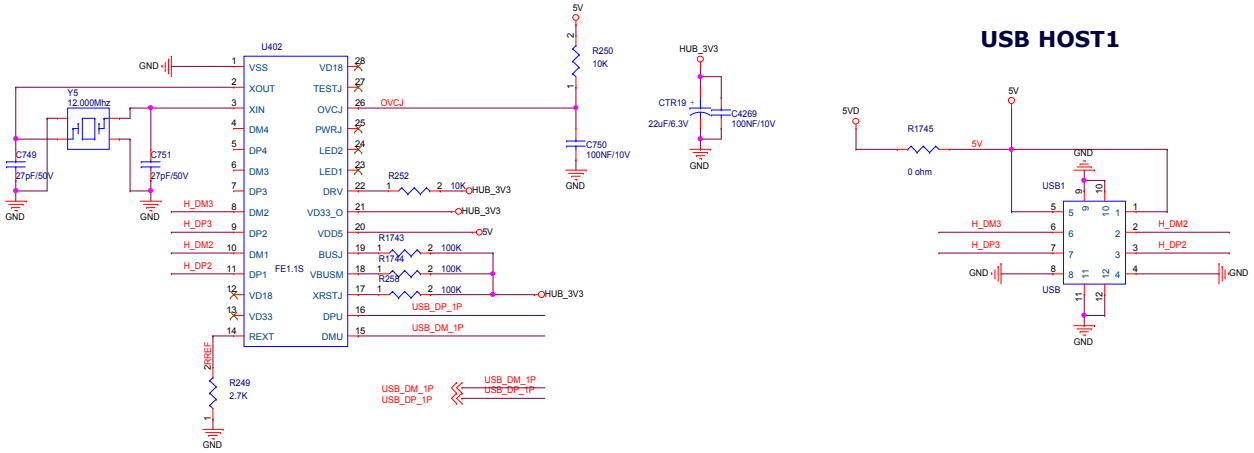


3.3V/3A



Vout=0.92(1+R251/R252)




U402
FE1.1S
VSS
XOUT
XIN
DM4
DP4
DM3
DP3
DM2
DP2
DM1
DP1
VD18
VD33
REXT
VD18
TESTJ
OVCJ
PWRJ
LED2
LED1
DRV
VD33_O
VDD5
BUSJ
VBUSM
XRSTJ
DPU
DMU
GND
Y5
12.000Mhz
C749
27pF/50V
C751
27pF/50V
H_DM3
H_DP3
H_DM2
H_DP2
R252
10K
HUB_3V3
5V
R1743
100K
R1744
100K
R258
100K
USB_DP_1P
USB_DM_1P
R249
2.7K
2KREF
R250
10K
C750
100NF/10V
OVCJ
HUB_3V3
CTR19
22uF/6.3V
C4269
100NF/10V

USB HOST1

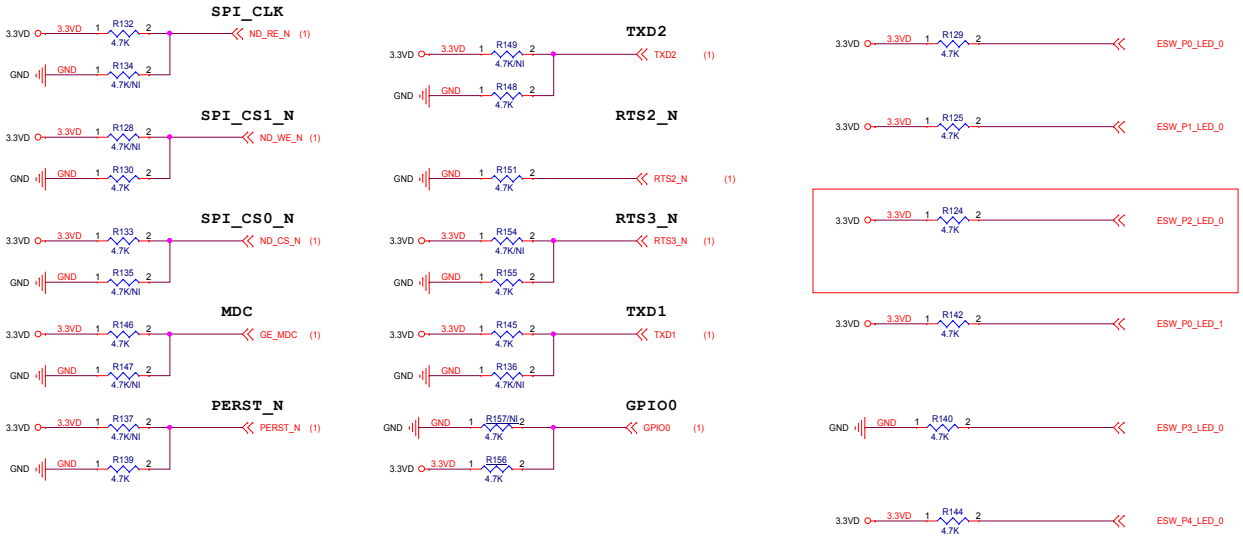
5VD
R1745
0 ohm
5V
GND
USB1
USB
H_DM3
H_DP3
H_DM2
H_DP2

Boot Strapping

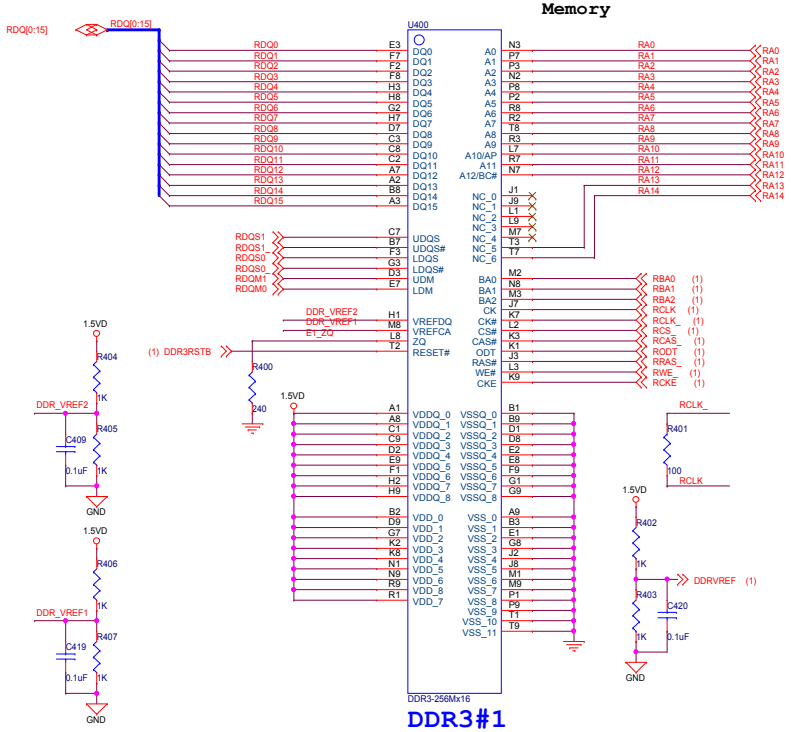
Pin Name	Description	Value	
SPI_CLK	DRAM_FROM_EE	For non scan mode: 0: DRAM/PLL configuration from EEPROM **1: DRAM configuration from Auto Detect**	For FT mode: 0: SUTIF 1: 3-wire SPI
{SPI_CS1_N, SPI_CS0_N, MDC }	XTAL_MODE	000: 20 MHz, Self Oscillation mode 001: 20 MHz, Single end input 010: 20 MHz, differential input **011: 40 MHz, Self Oscillation mode**	100: 40 MHz, Single end input 101: 40 MHz, differential input 110: 25 MHz, Self Oscillation mode 111: 25 MHz, Single end input
PERST_N	OCP_RATIO	**0: 1:3** 1: 1:4	
TXD2	DRAM_TYPE	**0: DDR3** 1: DDR2	
{RTS2_N, RTS3_N, TXD1, GPIO0}	CHIP_MODE[3:0]	0000: Normal / Boot from SPI 4-byte address and XTAL clock 0001: Normal / Boot from ROM (NAND page 2k+64 bytes) **0010: Normal / Boot from SPI 3-byte address** 0011: Normal / Boot from SPI 4-byte address 0100: iNIC RGMI / Boot from ROM 0101: iNIC MII / Boot from ROM 0110: iNIC RVMII / Boot from ROM 0111: iNIC PHY / Boot from ROM 1000: iNIC RGMII / Boot from ROM and XTAL clock 1001: Normal / Boot from internal SRAM 1010: Normal / Boot from ROM (NAND page 2k+128 bytes) 1011: Normal / Boot from ROM (NAND page 4k+128 bytes) 1100: Normal / Boot from ROM (NAND page 4k+224 bytes) 1101: Debug mode 1110: Scan mode 1111: Final Test	

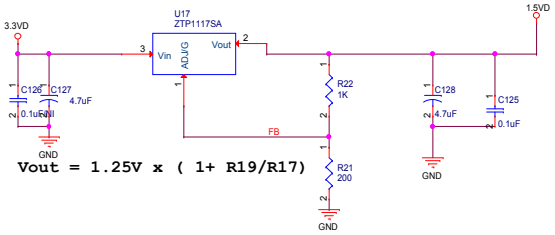
Giga Switch Hardware Trap

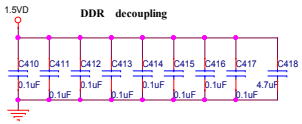
Pin Name	Trap	Fuction	Description	Default
P0_LED_0	HWTRAP[0]	HT_CHIP_MODE[0]	chip_mode[3:0] 4'b0000: IDDQ mode 4'b0001: IOTEST mode 4'b0010: NANDTREE mode 4'b0011: RING mode (both IO and std-cell) 4'b0100: MBIST 4'b0101: SCAN mode (internal) 4'b0110: SCAN-COMP mode (compression) 4'b0111: SCAN-MBIST-OLT mode 4'b1000: AFE-OLT mode 4'b1001: GPHY ATE mode 4'b1010: GPHY ADUMP mode 4'b1011: GPHY ADUMP probe mode 4'b1100: Reserved 4'b1101: Reserved 4'b1110: bootup probe mode 4'b1111: normal mode	4'b1111
P1_LED_0	HWTRAP[1]	HT_CHIP_MODE[1]		
P2_LED_0	HWTRAP[2]	HT_CHIP_MODE[2]		
P0_LED_1	HWTRAP[3]	HT_CHIP_MODE[3]		
P3_LED_0	HWTRAP[9]	HT_XTAL_FSEL[0]	External Crystal Frequency Selection xtal_freq_sel[1:0] 2'b01: 20MHz 2'b10: 40MHz 2'b11: 25MHz	2'b10
P4_LED_0	HWTRAP[10]	HT_XTAL_FSEL[1]		

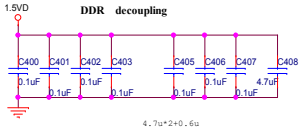


Memory

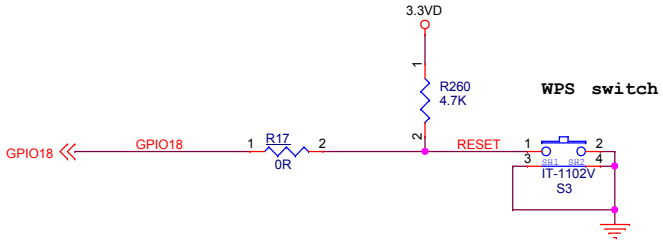

RDQ[0:15]
U400
DDR3-256Mx16
DDR3#1
1.5VD
GND
DDR_VREF2
DDR_VREF1
(1) DDR3RSTB
R400
240
R404
R405
R406
R407
C409
C419
0.1uF
1K
RCLK_
RCLK
R401
100
R402
R403
C420
DDRVREF (1)

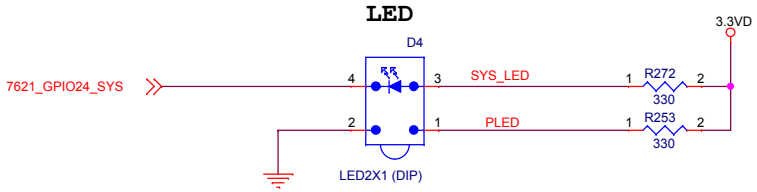

3.3VD
U17
ZTP1117SA
Vin
Vout
ADJ/G
FB
C126
C127
4.7uF
0.1uF
R22
1K
R21
200
C128
C125
1.5VD
GND
Vout = 1.25V x (1+ R19/R17)


1.5VD
DDR decoupling
C410
C411
C412
C413
C414
C415
C416
C417
C418
0.1uF
4.7uF


1.5VD
DDR decoupling
C400
C401
C402
C403
C405
C406
C407
C408
0.1uF
4.7uF
4.7u*2+0.6u

GPIO18/WPS/RESET

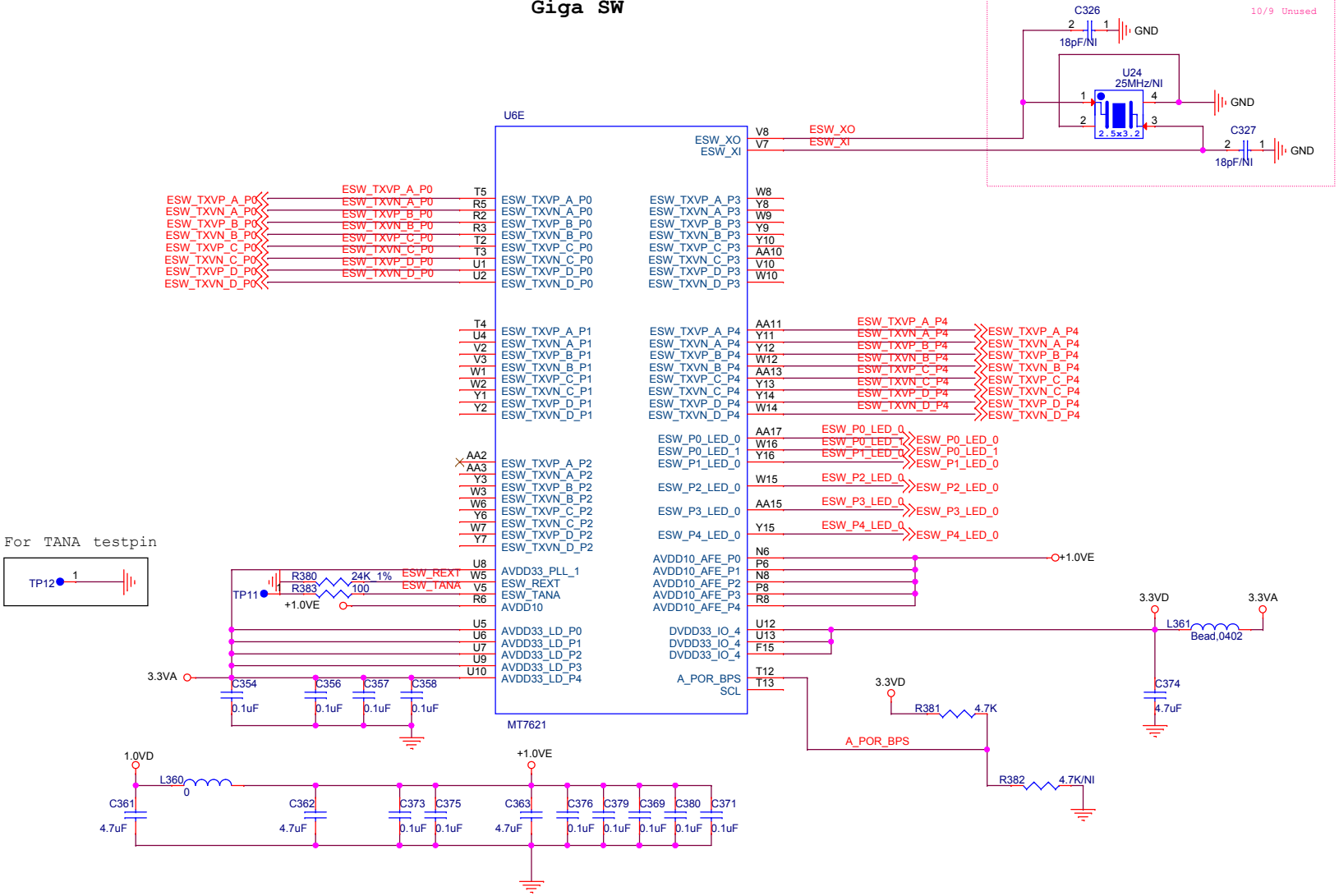




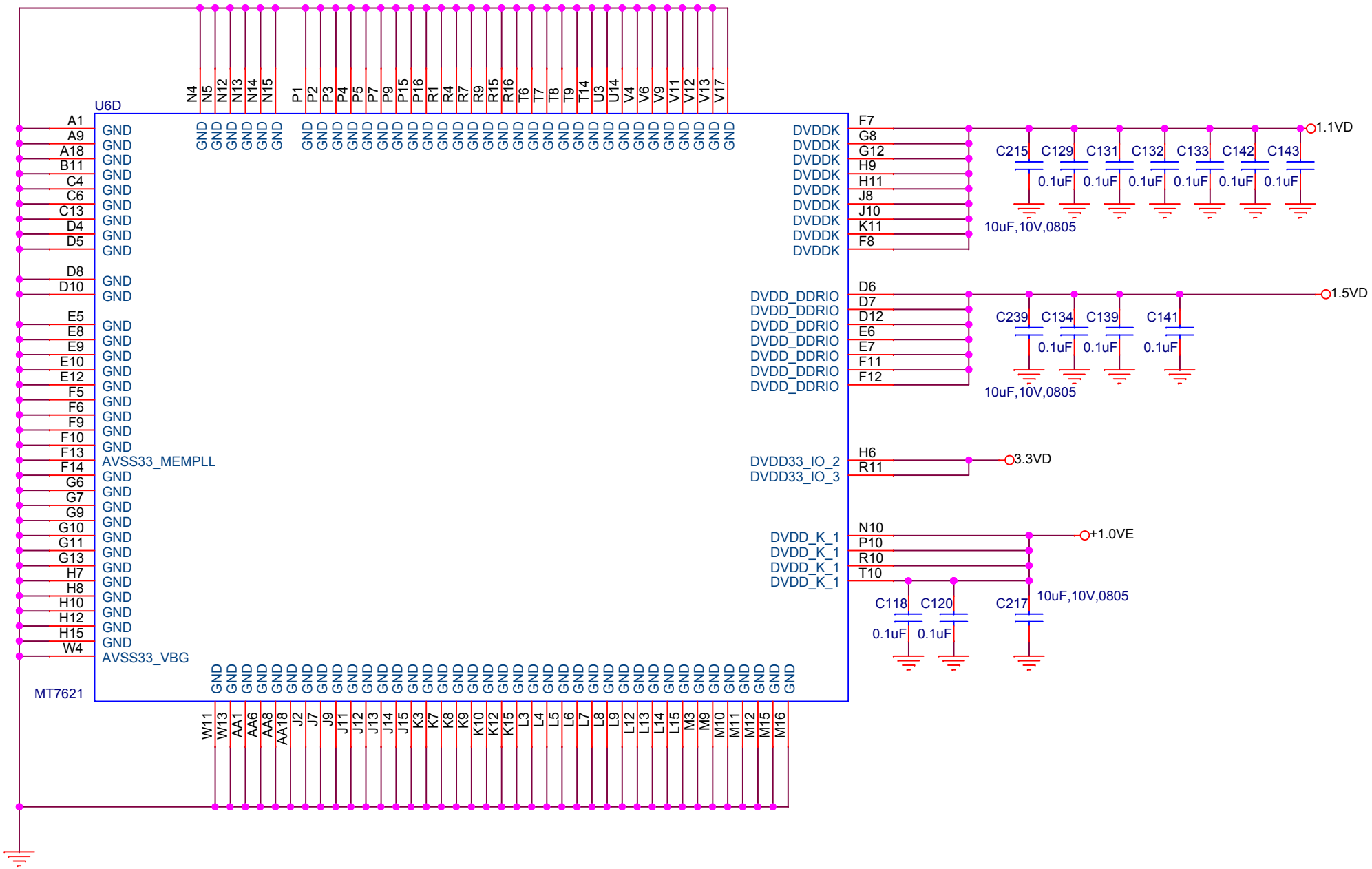
Giga SW

Please remove it in real design

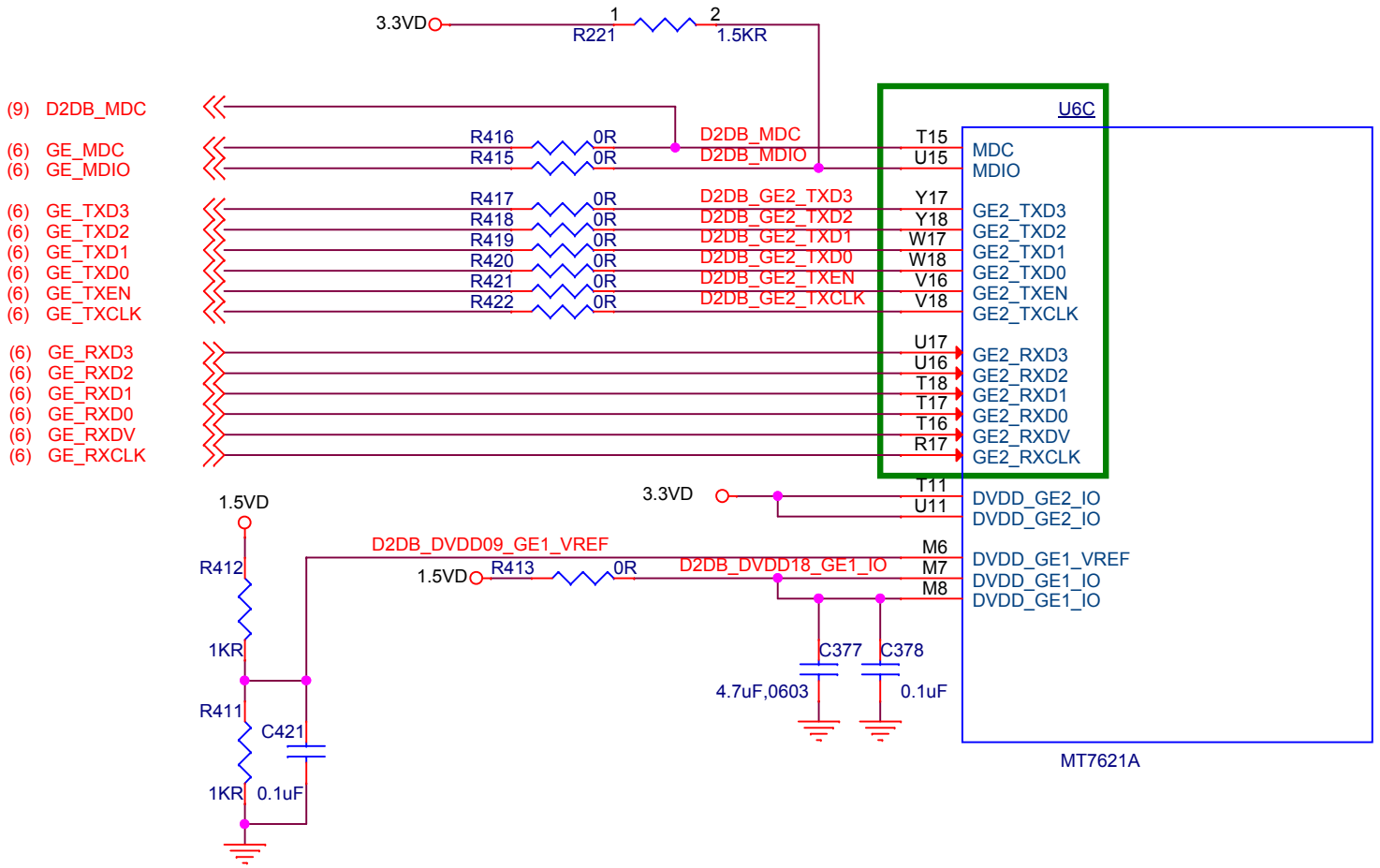
10/9 Unused



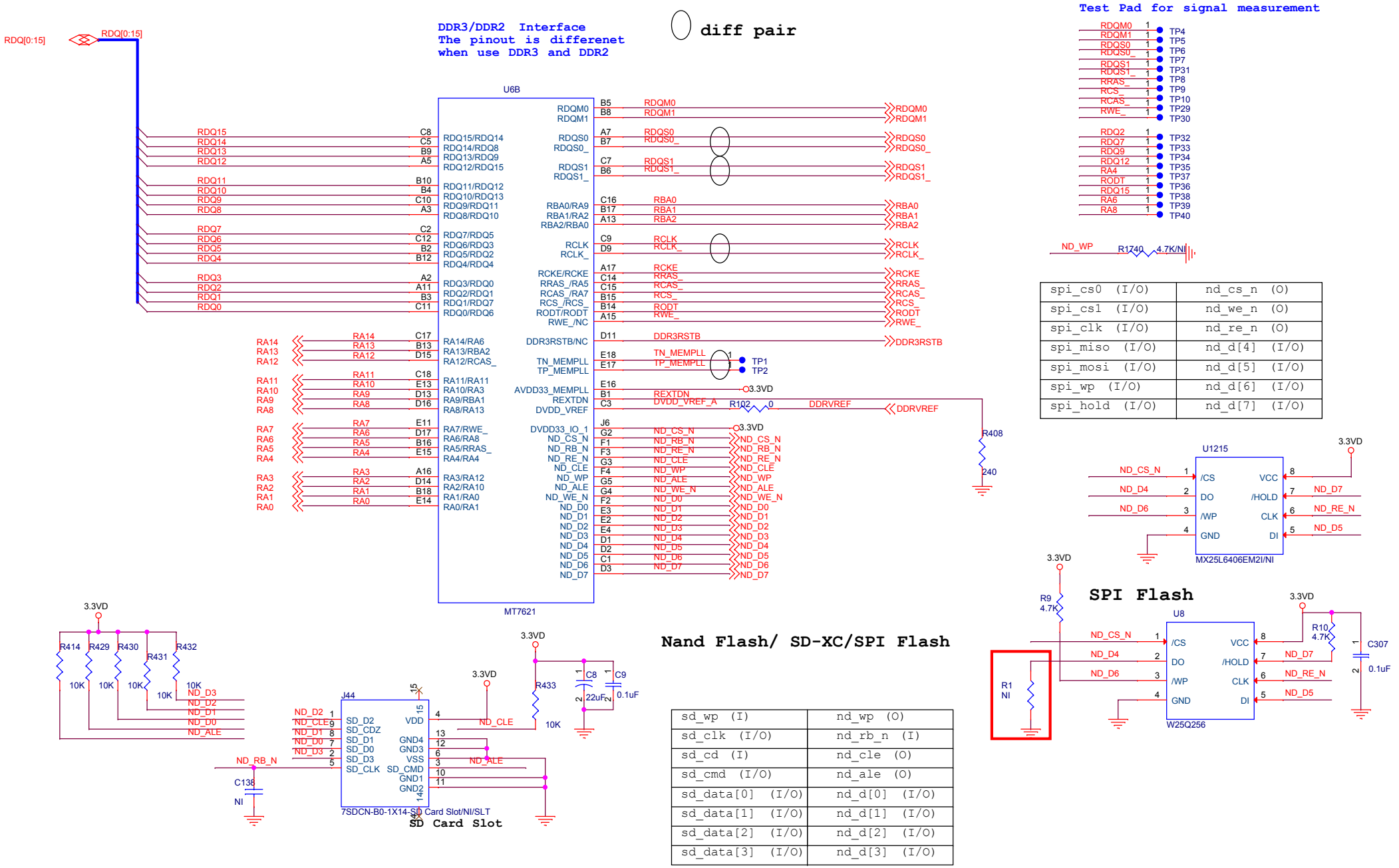
MT7621 Power



RGMII Interface

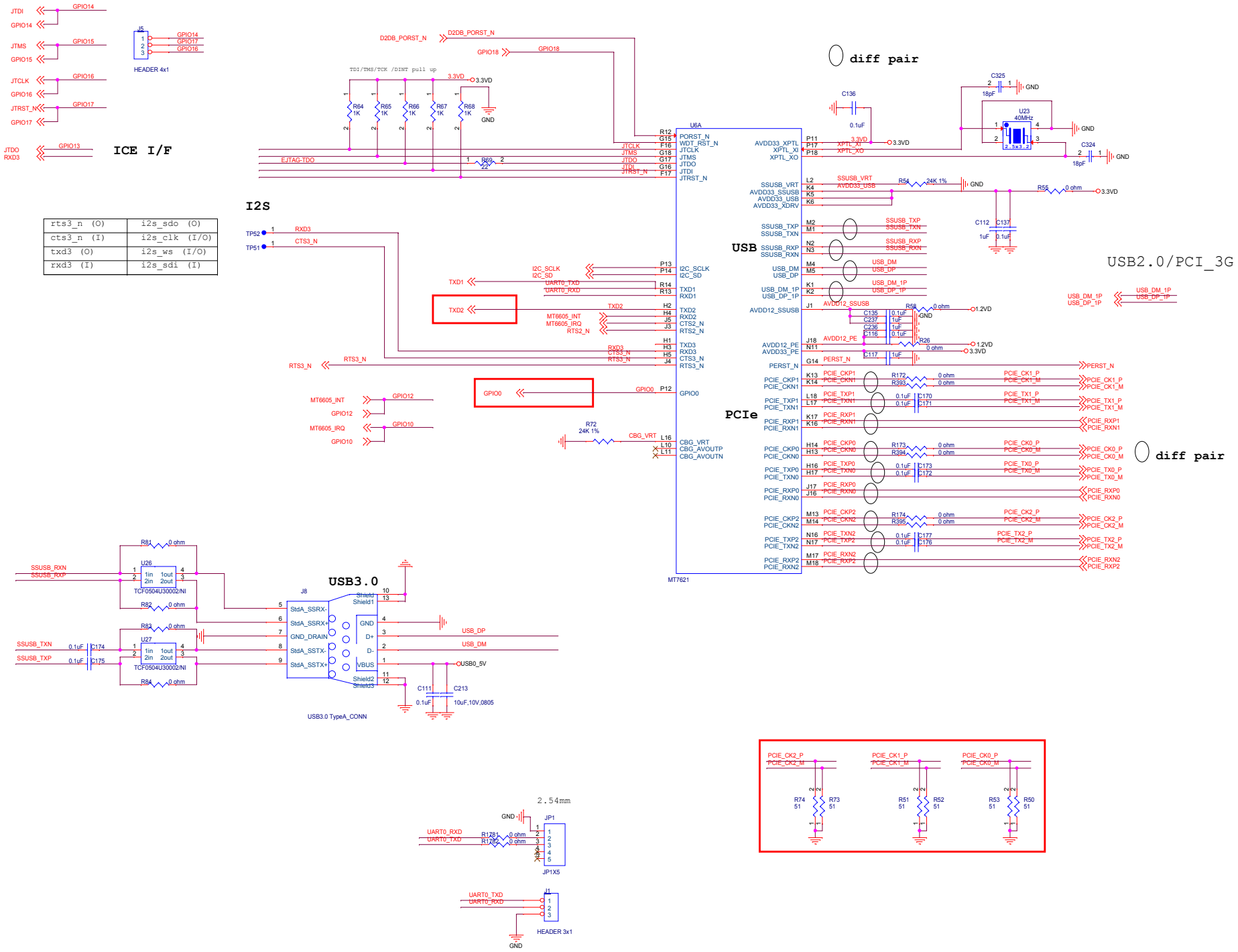


Note:
1. MT7621A/S MDC/MDIO cannot use to GPIO when needs control external/internal PHY
2. GE2 group cannot use to GPIO when WAN/LAN total bandwidth is up to 2G. Keeps the pin floating.

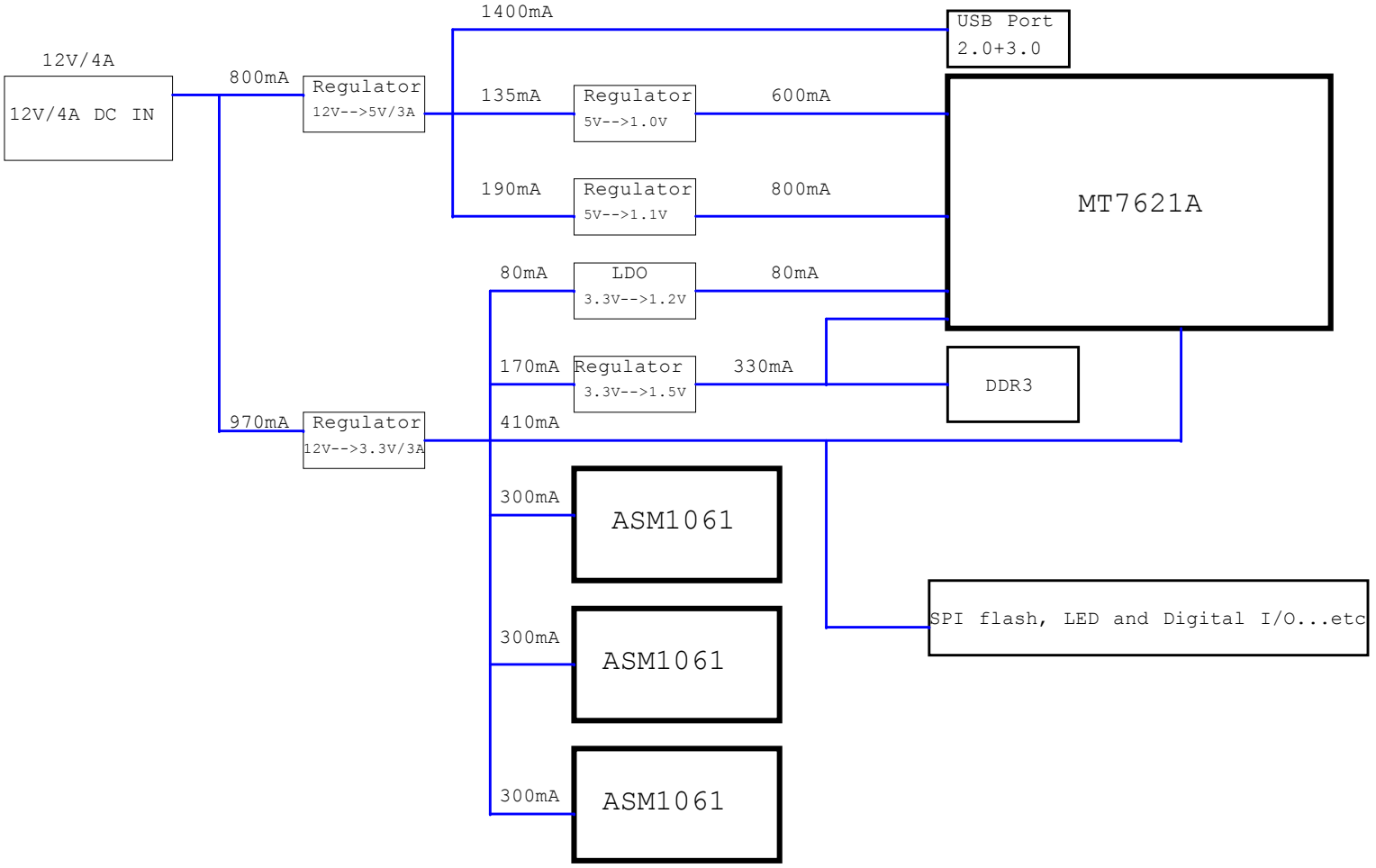


spi_cs0 (I/O)	nd_cs_n (O)
spi_cs1 (I/O)	nd_we_n (O)
spi_clk (I/O)	nd_re_n (O)
spi_miso (I/O)	nd_d[4] (I/O)
spi_mosi (I/O)	nd_d[5] (I/O)
spi_wp (I/O)	nd_d[6] (I/O)
spi_hold (I/O)	nd_d[7] (I/O)

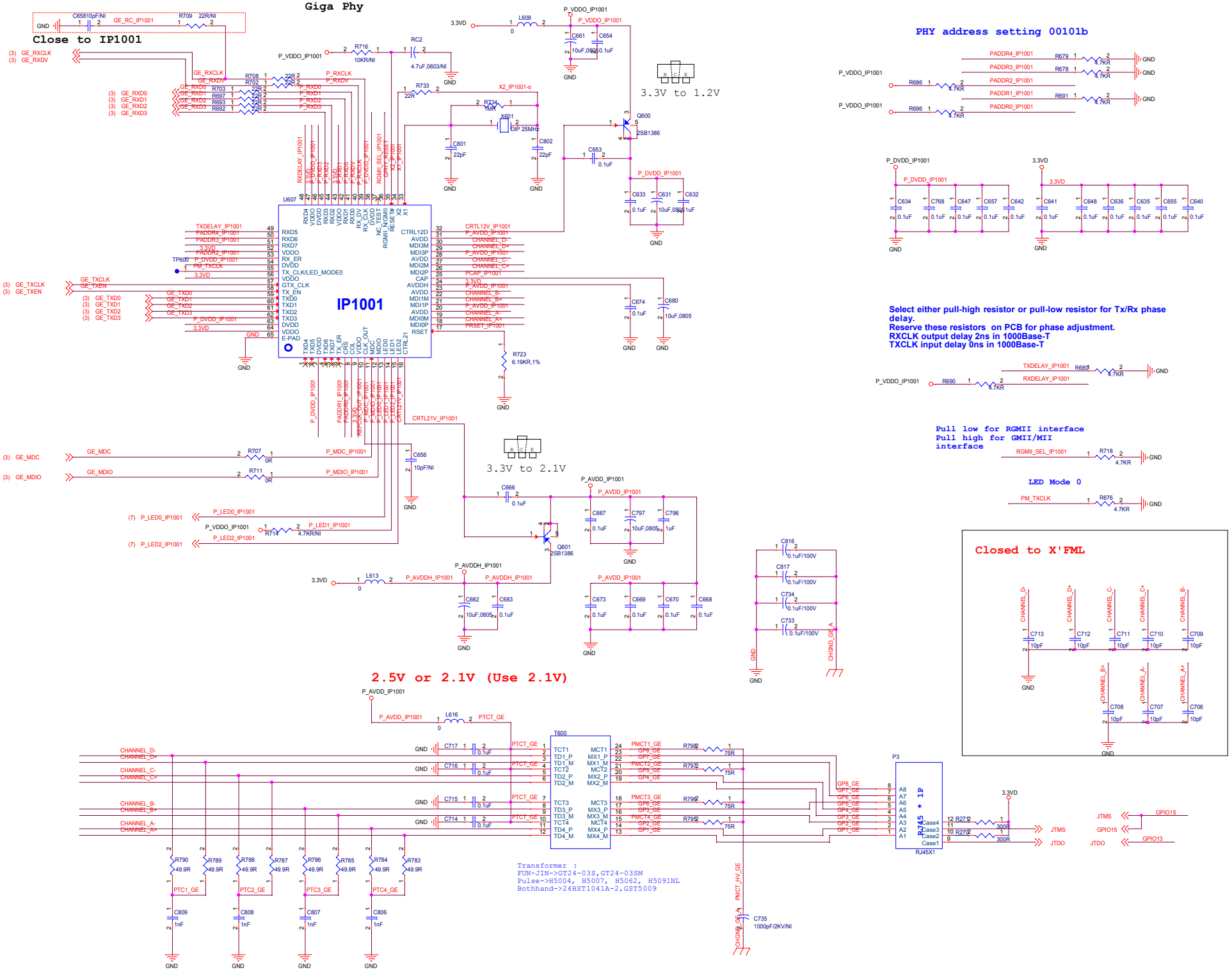
sd_wp (I)	nd_wp (O)
sd_clk (I/O)	nd_rb_n (I)
sd_cd (I)	nd_cle (O)
sd_cmd (I/O)	nd_ale (O)
sd_data[0] (I/O)	nd_d[0] (I/O)
sd_data[1] (I/O)	nd_d[1] (I/O)
sd_data[2] (I/O)	nd_d[2] (I/O)
sd_data[3] (I/O)	nd_d[3] (I/O)



rts3_n (O)	i2s_sdo (O)
cts3_n (I)	i2s_clk (I/O)
txd3 (O)	i2s_ws (I/O)
rxd3 (I)	i2s_sdi (I)


12V/4A
12V/4A DC IN
800mA
Regulator
12V-->5V/3A
1400mA
USB Port
2.0+3.0
135mA
Regulator
5V-->1.0V
600mA
190mA
Regulator
5V-->1.1V
800mA
MT7621A
80mA
LDO
3.3V-->1.2V
80mA
170mA
Regulator
3.3V-->1.5V
330mA
DDR3
970mA
Regulator
12V-->3.3V/3A
410mA
300mA
ASM1061
300mA
ASM1061
300mA
ASM1061
SPI flash, LED and Digital I/O...etc

Giga Phy


Close to IP1001
IP1001
3.3V to 1.2V
3.3V to 2.1V
PHY address setting 00101b
Select either pull-high resistor or pull-low resistor for Tx/Rx phase delay.
Reserve these resistors on PCB for phase adjustment.
RXCLK output delay 2ns in 1000Base-T
TXCLK input delay 0ns in 1000Base-T
Pull low for RGMII interface
Pull high for GMII/MII interface
LED Mode 0
Closed to X'FML
2.5V or 2.1V (Use 2.1V)
Transformer :
FUN-JIN->GT24-03S,GT24-03SM
Pulse->H5004, H5007, H5062, H5091NL
Bothhand->24HST1041A-2,GST5009