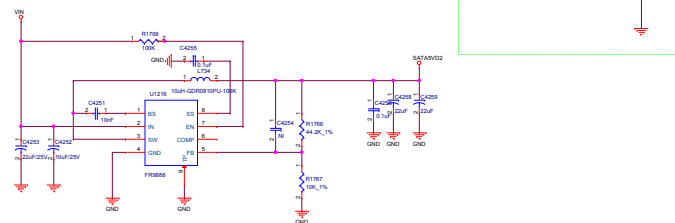
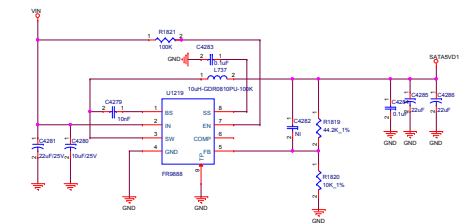
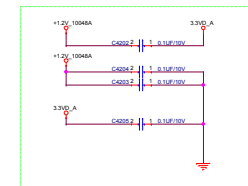
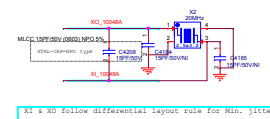
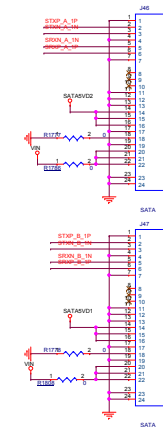
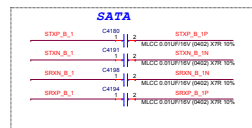
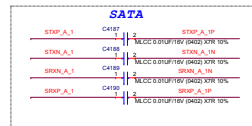
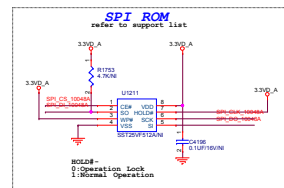
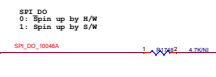


H/W Strapping

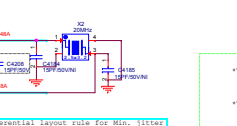
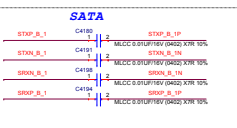
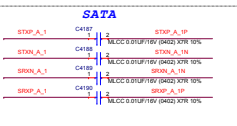
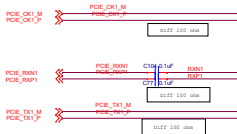
refer to datasheet:



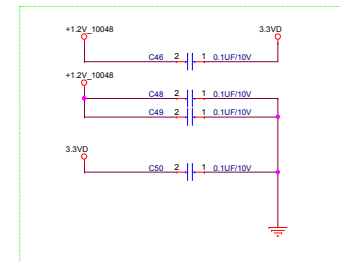
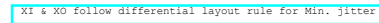
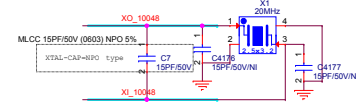
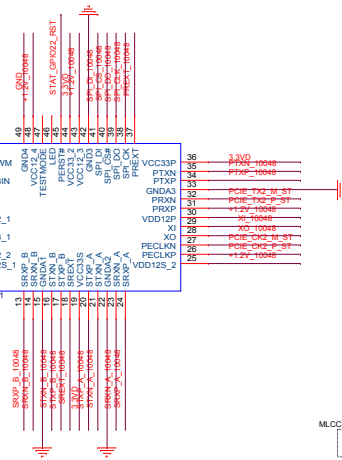
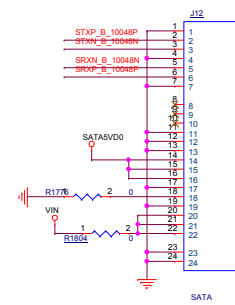
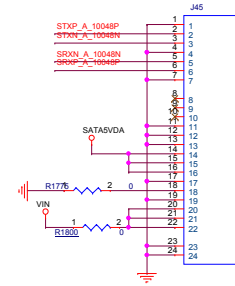
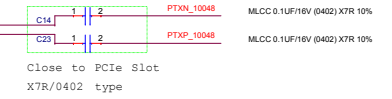
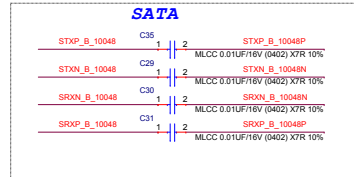
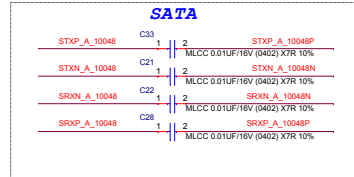
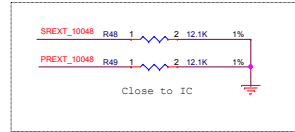
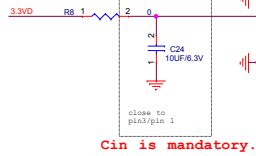
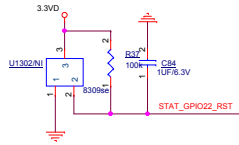
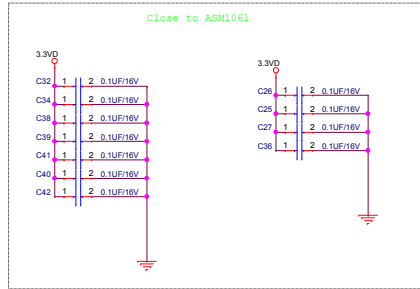
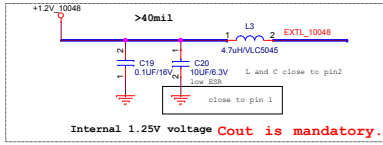
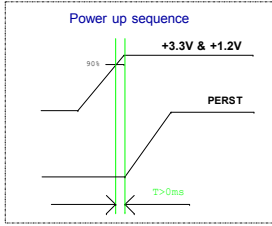
PCIe to SATA



Close to PCIe Slot

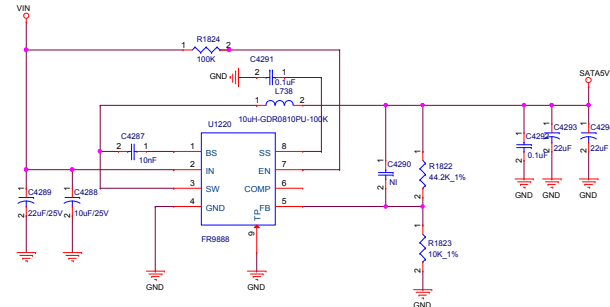
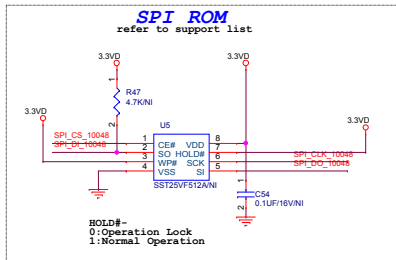
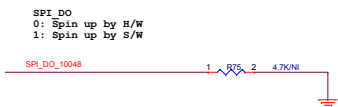


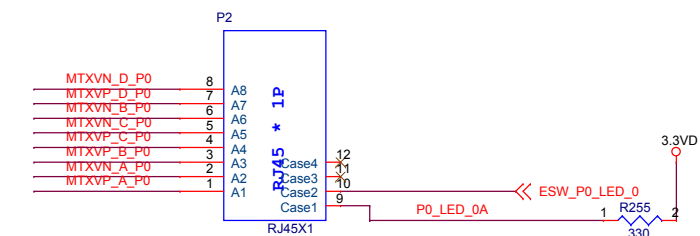
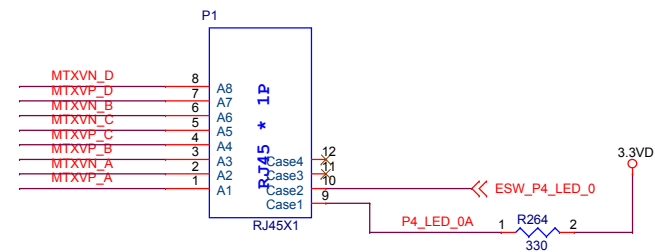
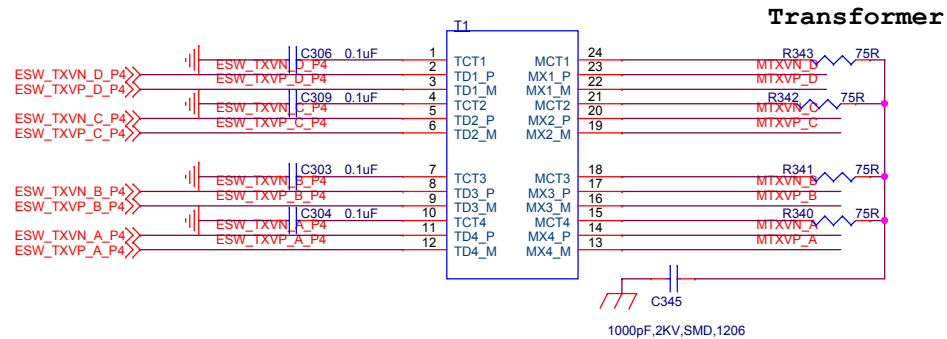
PCIe to SATA



H/W Strapping

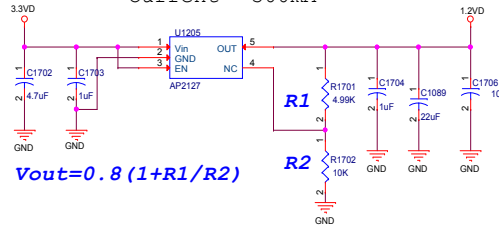
refer to datasheet:



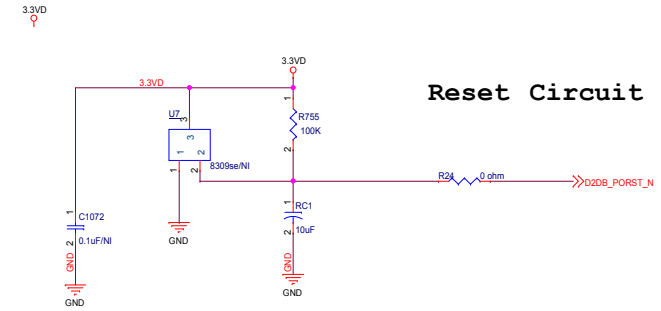


System Power

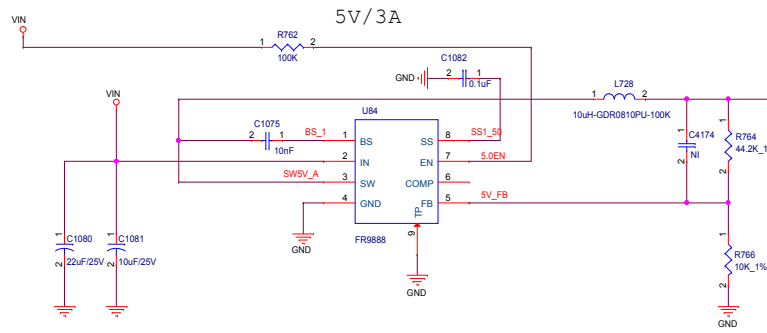
For USB/PCIe PHY Power (1.2V)
Current= 300mA



Reset Circuit

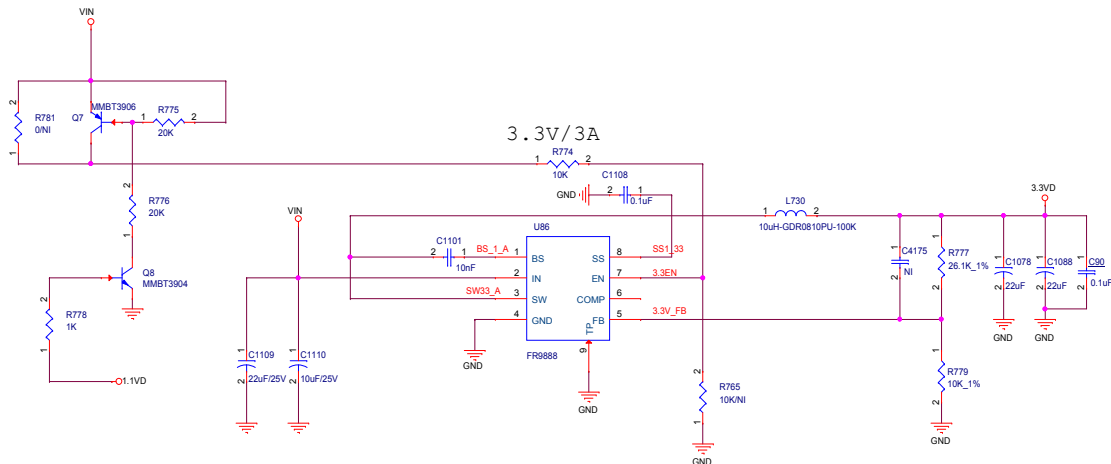


5V/3A



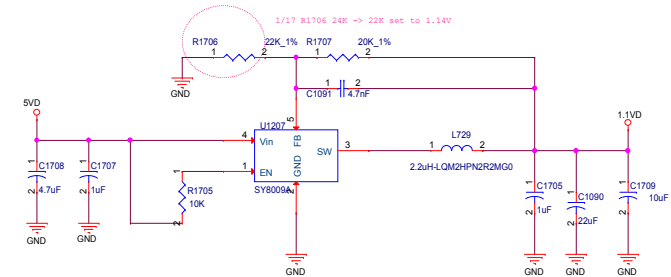
$$V_{out} = 0.92 (1 + R255/R256)$$

3.3V/3A

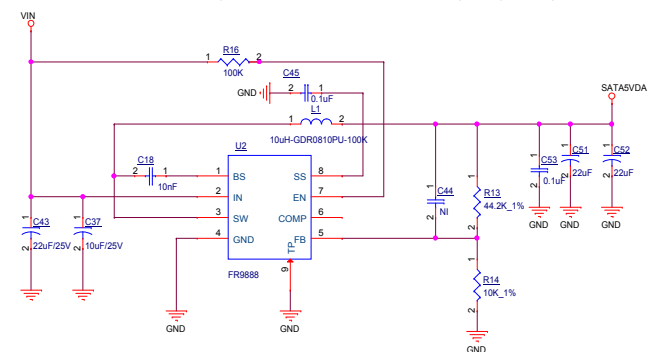
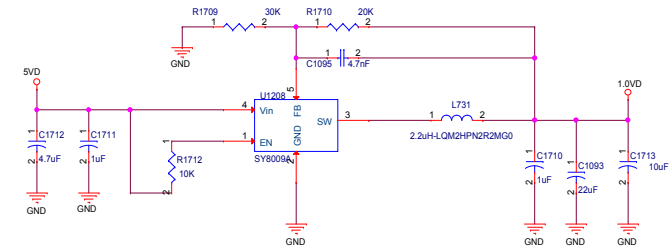


$$V_{out} = 0.92 (1 + R251/R252)$$

1.14V/1.5A

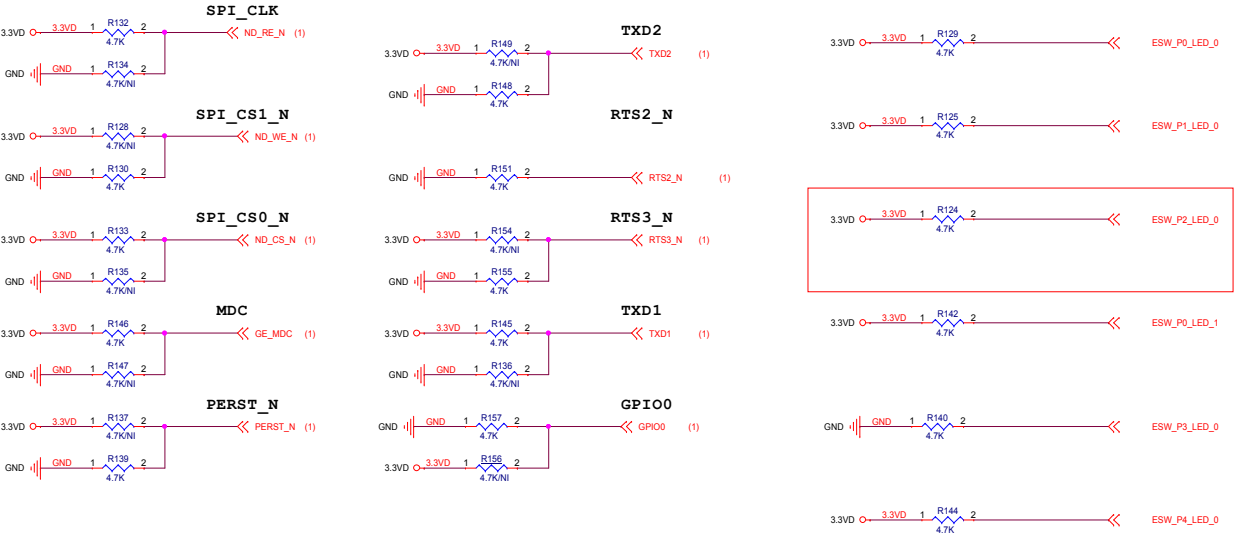


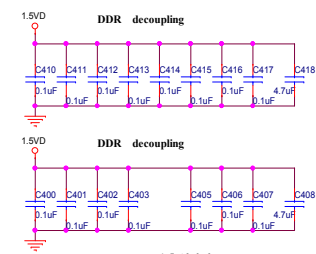
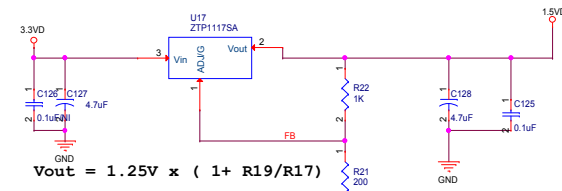
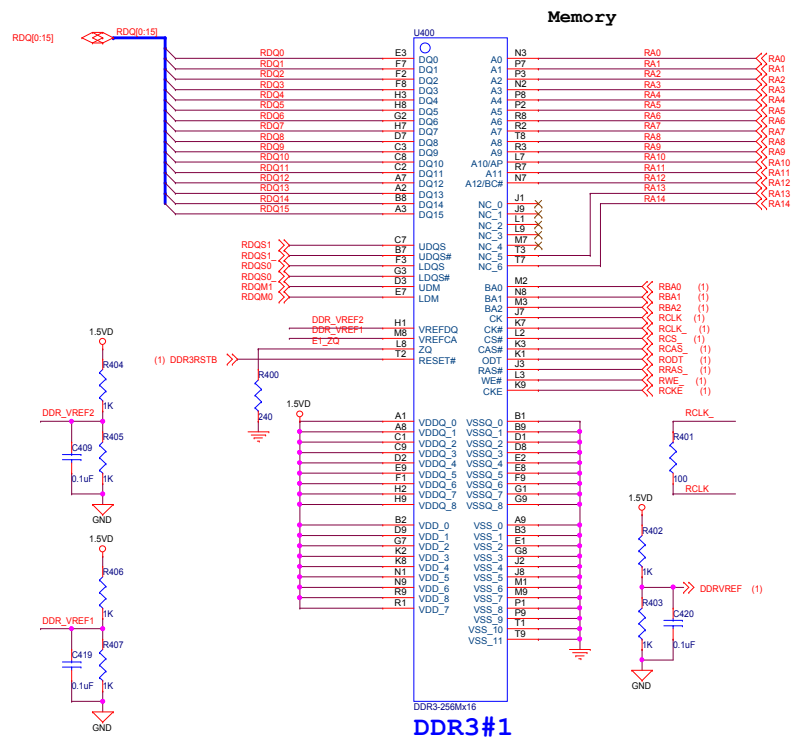
1.0V/1.5A



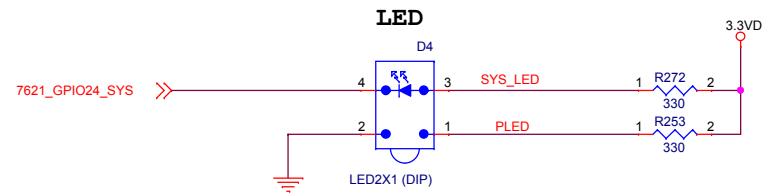
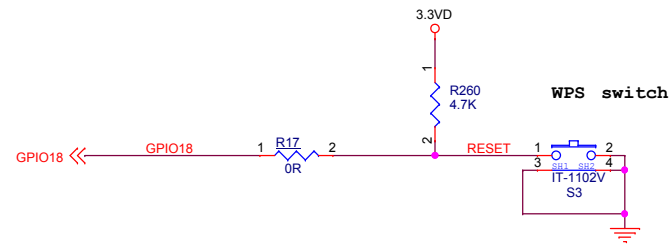
Pin Name	Description	Value	
SPI_CLK	DRAM_FROM_EE	For non scan mode: 0: DRAM/PLL configuration from EEPROM 1: DRAM configuration from Auto Detect	For FT mode: 0: SUTIF 1: 3-wire SPI
{SPI_CS1_N, SPI_CS0_N, MDC }	XTAL_MODE	000: 20 MHz, Self Oscillation mode 001: 20 MHz, Single end input 010: 20 MHz, differential input 011: 40 MHz, Self Oscillation mode	100: 40 MHz, Single end input 101: 40 MHz, differential input 110: 25 MHz, Self Oscillation mode 111: 25 MHz, Single end input
PERST_N	OCP_RATIO	0: 1:3 1: 1:4	
TXD2	DRAM_TYPE	0: DDR3 1: DDR2	
{RTS2_N, RTS3_N, TXD1, GPIO0}	CHIP_MODE[3:0]	0000: Normal / Boot from SPI 4-byte address and XTAL clock 0001: Normal / Boot from ROM (NAND page 2k+64 bytes) 0010: Normal / Boot from SPI 3-byte address 0011: Normal / Boot from SPI 4-byte address 0100: iNIC RGMI / Boot from ROM 0101: iNIC MII / Boot from ROM 0110: iNIC RVMII / Boot from ROM 0111: iNIC PHY / Boot from ROM 1000: iNIC RGMII / Boot from ROM and XTAL clock 1001: Normal / Boot from internal SRAM 1010: Normal / Boot from ROM (NAND page 2k+128 bytes) 1011: Normal / Boot from ROM (NAND page 4k+128 bytes) 1100: Normal / Boot from ROM (NAND page 4k+224 bytes) 1101: Debug mode 1110: Scan mode 1111: Final Test	

Giga Switch Hardware Trap				
Pin Name	Trap	Fuction	Description	Default
P0_LED_0	HWTRAP[0]	HT_CHIP_MODE[0]	chip_mode[3:0] 4'b0000: IDDQ mode 4'b0001: IOTEST mode 4'b0010: NANDTREE mode 4'b0011: RING mode (both IO and std-cell) 4'b0100: MBIST 4'b0101: SCAN mode (internal) 4'b0110: SCAN-COMP mode (compression) 4'b0111: SCAN-MBIST-OLT mode 4'b1000: AFE-OLI mode 4'b1001: GPHY ATE mode 4'b1010: GPHY ADUMP mode 4'b1011: GPHY ADUMP probe mode 4'b1100: Reserved 4'b1101: Reserved 4'b1110: bootup probe mode 4'b1111: normal mode	4'b1111
P1_LED_0	HWTRAP[1]	HT_CHIP_MODE[1]	External Crystal Frequency Selection xtal_freq_sel[1:0] 2'b01: 20MHz 2'b10: 40MHz 2'b11: 25MHz	2'b10
P2_LED_0	HWTRAP[2]	HT_CHIP_MODE[2]		
P0_LED_1	HWTRAP[3]	HT_CHIP_MODE[3]		
P3_LED_0	HWTRAP[9]	HT_XTAL_FSEL[0]	External Crystal Frequency Selection xtal_freq_sel[1:0] 2'b01: 20MHz 2'b10: 40MHz 2'b11: 25MHz	2'b10
P4_LED_0	HWTRAP[10]	HT_XTAL_FSEL[1]		

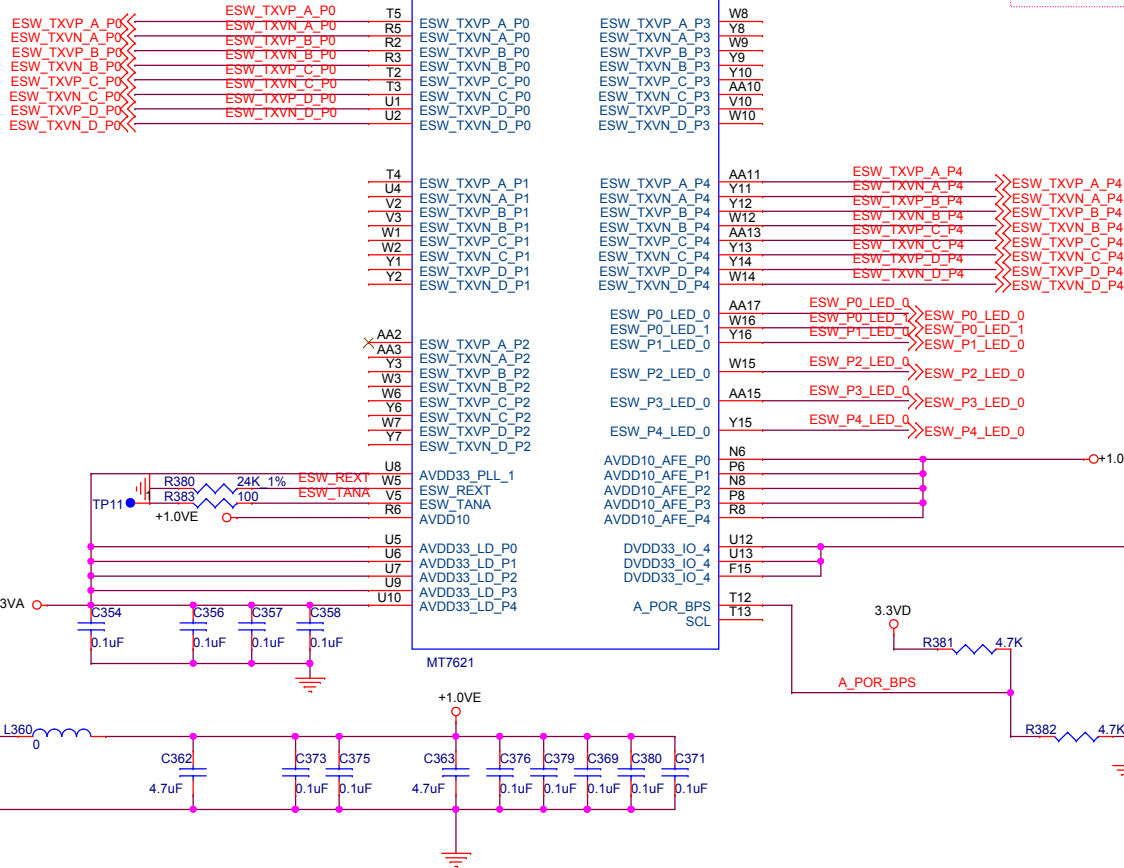
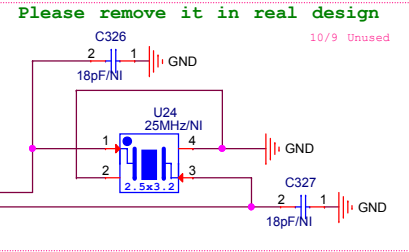




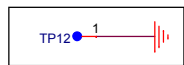
GPIO18/WPS/RESET



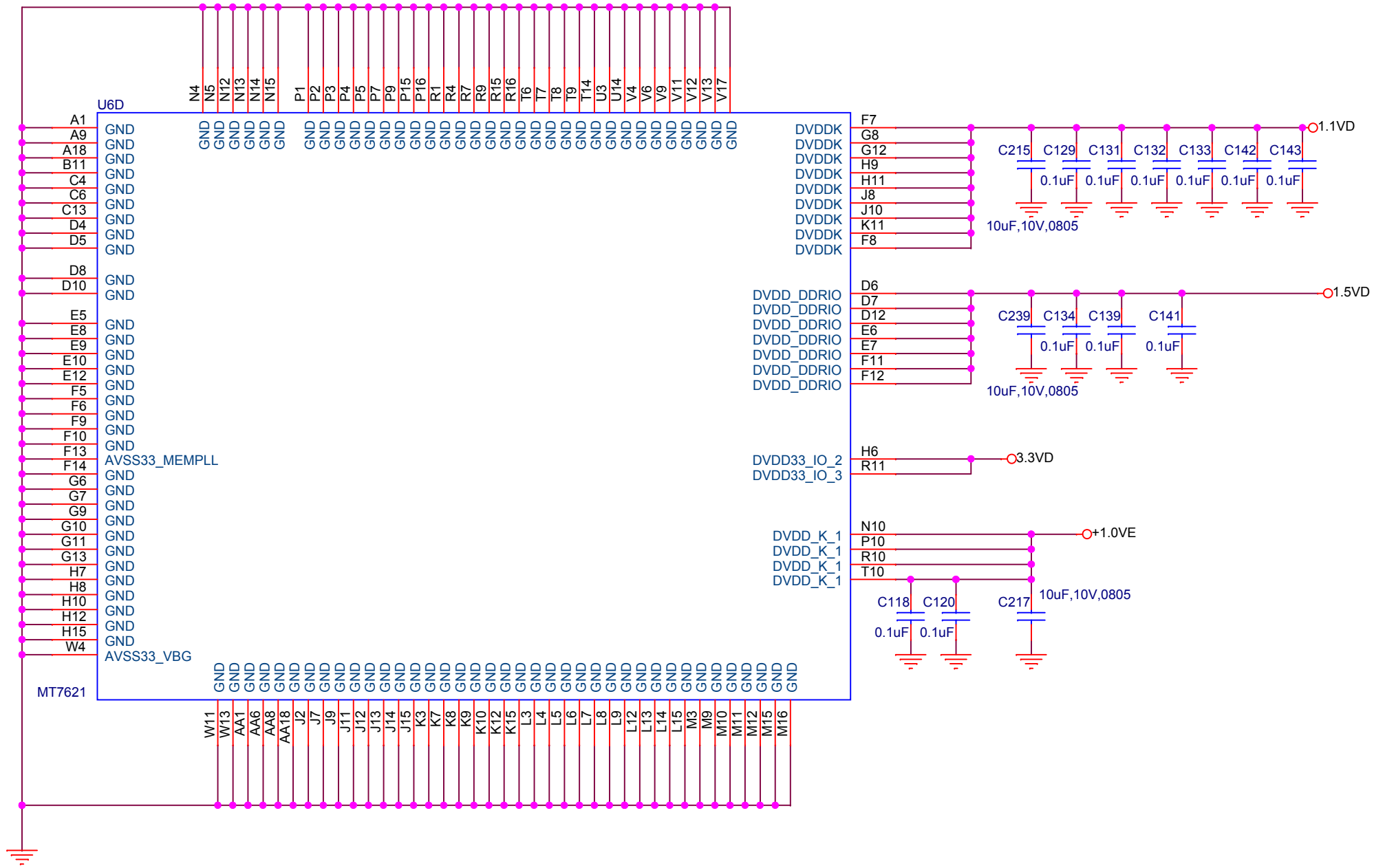
Giga SW



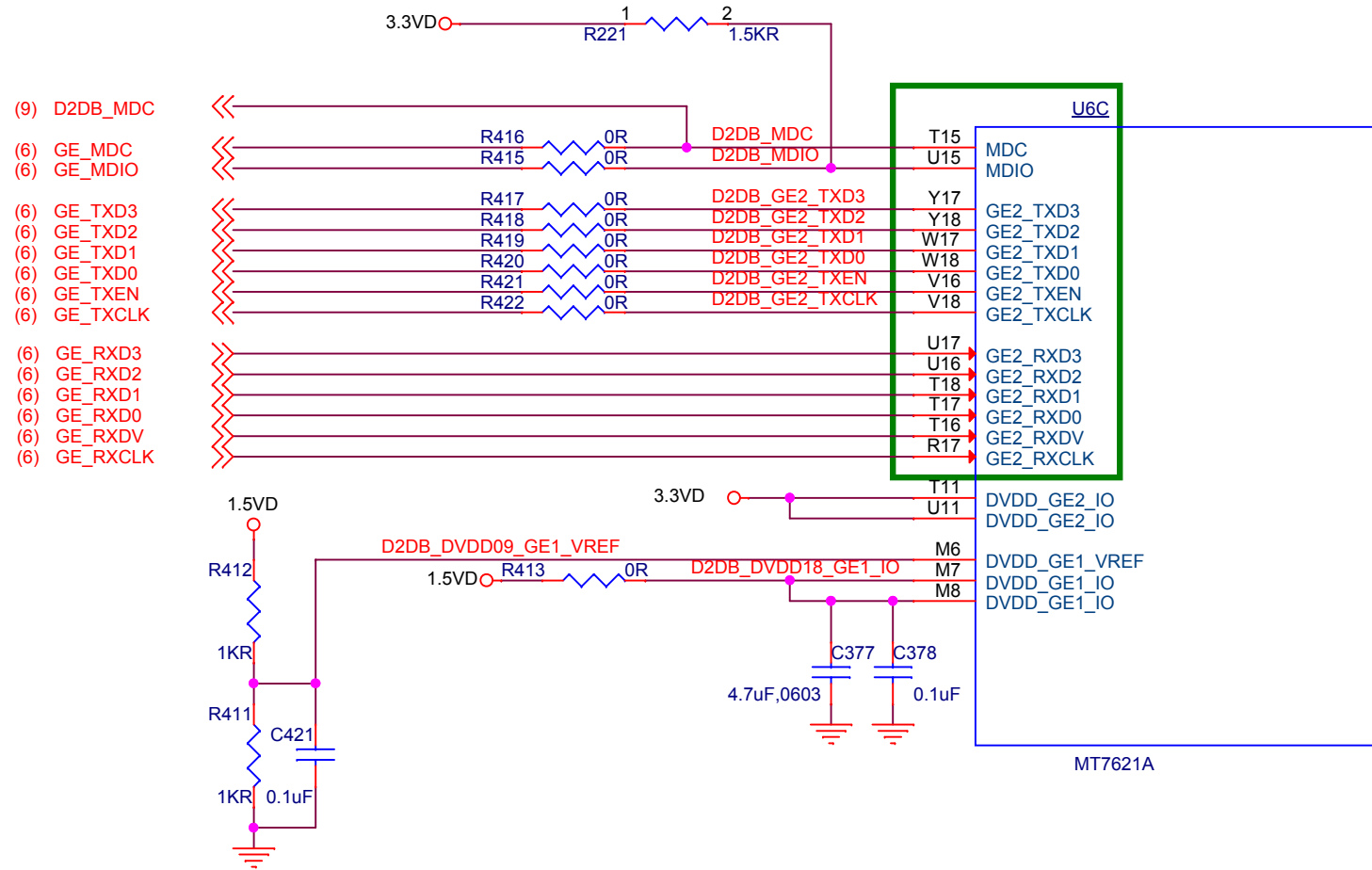
For TANA testpin



MT7621 Power



RGMII Interface



Note:

1. MT7621A/S MDC/MDIO cannot use to GPIO when needs control external/internal PHY
2. GE2 group cannot use to GPIO when WAN/LAN total bandwidth is up to 2G. Keeps the pin floating.

RDQ[0:15]

DDR3/DDR2 Interface
The pinout is different
when use DDR3 and DDR2

diff pair

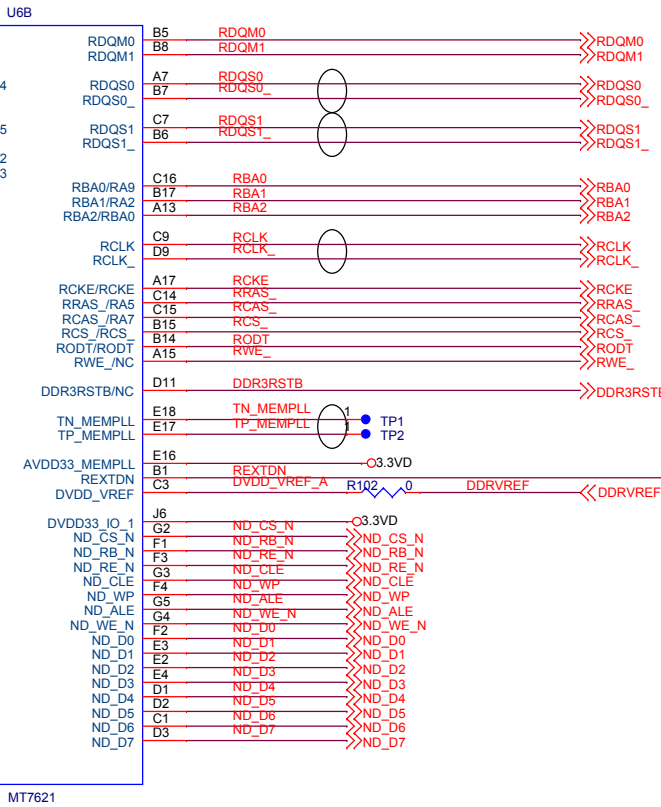
Test Pad for signal measurement

RDOM0	1	TP4
RDOM1	1	TP5
RQDS0	1	TP6
RQDS0	1	TP7
RQDS1	1	TP31
RQDS1	1	TP8
RRAS	1	TP9
RCS	1	TP10
RCAS	1	TP29
RWE	1	TP30
RDQ2	1	TP32
RDQ7	1	TP33
RDQ9	1	TP34
RDQ12	1	TP35
RA4	1	TP37
RODT	1	TP36
RDQ15	1	TP38
RA6	1	TP39
RA8	1	TP40

ND_WP R1740 4.7K/N

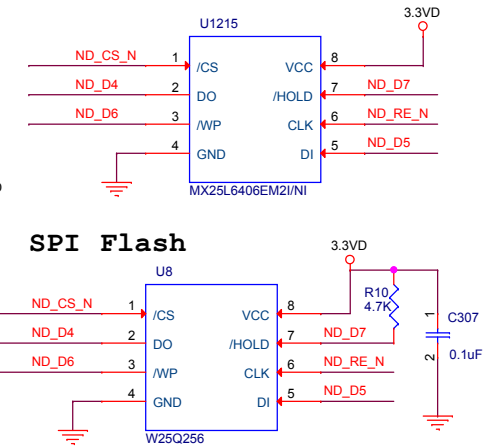
spi_cs0 (I/O)	nd_cs_n (O)
spi_cs1 (I/O)	nd_we_n (O)
spi_clk (I/O)	nd_re_n (O)
spi_miso (I/O)	nd_d[4] (I/O)
spi_mosi (I/O)	nd_d[5] (I/O)
spi_wp (I/O)	nd_d[6] (I/O)
spi_hold (I/O)	nd_d[7] (I/O)

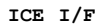
RA14	RA14	C17	RA14/RA6
RA13	RA13	B13	RA13/RBA2
RA12	RA12	D15	RA12/RCAS
RA11	RA11	C18	RA11/RA11
RA10	RA10	E13	RA10/RA3
RA9	RA9	D13	RA9/RBA1
RA8	RA8	D16	RA8/RA13
RA7	RA7	E11	RA7/RWE
RA6	RA6	D17	ND_CS_N
RA5	RA5	B16	ND_RB_N
RA4	RA4	E15	ND_RE_N
RA3	RA3	A16	ND_CLE
RA2	RA2	D14	ND_WP
RA1	RA1	B18	ND_ALE
RA0	RA0	E14	ND_WE_N



Nand Flash/ SD-XC/SPI Flash

sd_wp (I)	nd_wp (O)
sd_clk (I/O)	nd_rb_n (I)
sd_cd (I)	nd_cle (O)
sd_cmd (I/O)	nd_ale (O)
sd_data[0] (I/O)	nd_d[0] (I/O)
sd_data[1] (I/O)	nd_d[1] (I/O)
sd_data[2] (I/O)	nd_d[2] (I/O)
sd_data[3] (I/O)	nd_d[3] (I/O)





rts3_n (O)	i2s_sdo (O)
cts3_n (I)	i2s_clk (I/O)
txd3 (O)	i2s_ws (I/O)
rxid3 (I)	i2s_sdi (I)

