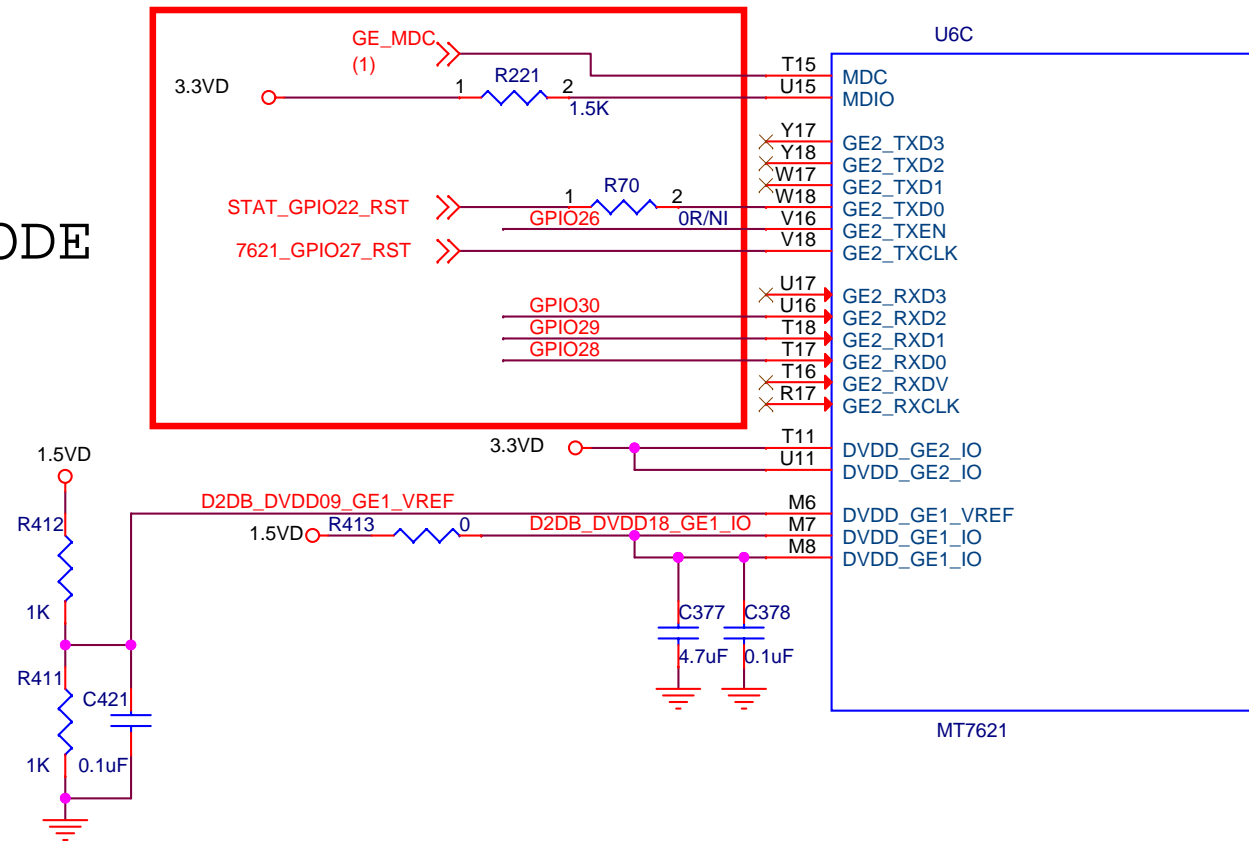
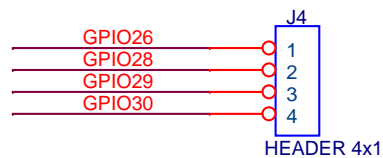


RGMII Interface

GPIO_MODE



GPIO PART



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MEDIATEK

Title

MT7621A

Size

A

Document Number

MT7621A

Drawn

Jimmy

Rev

V11

Date:

Monday, March 07, 2016

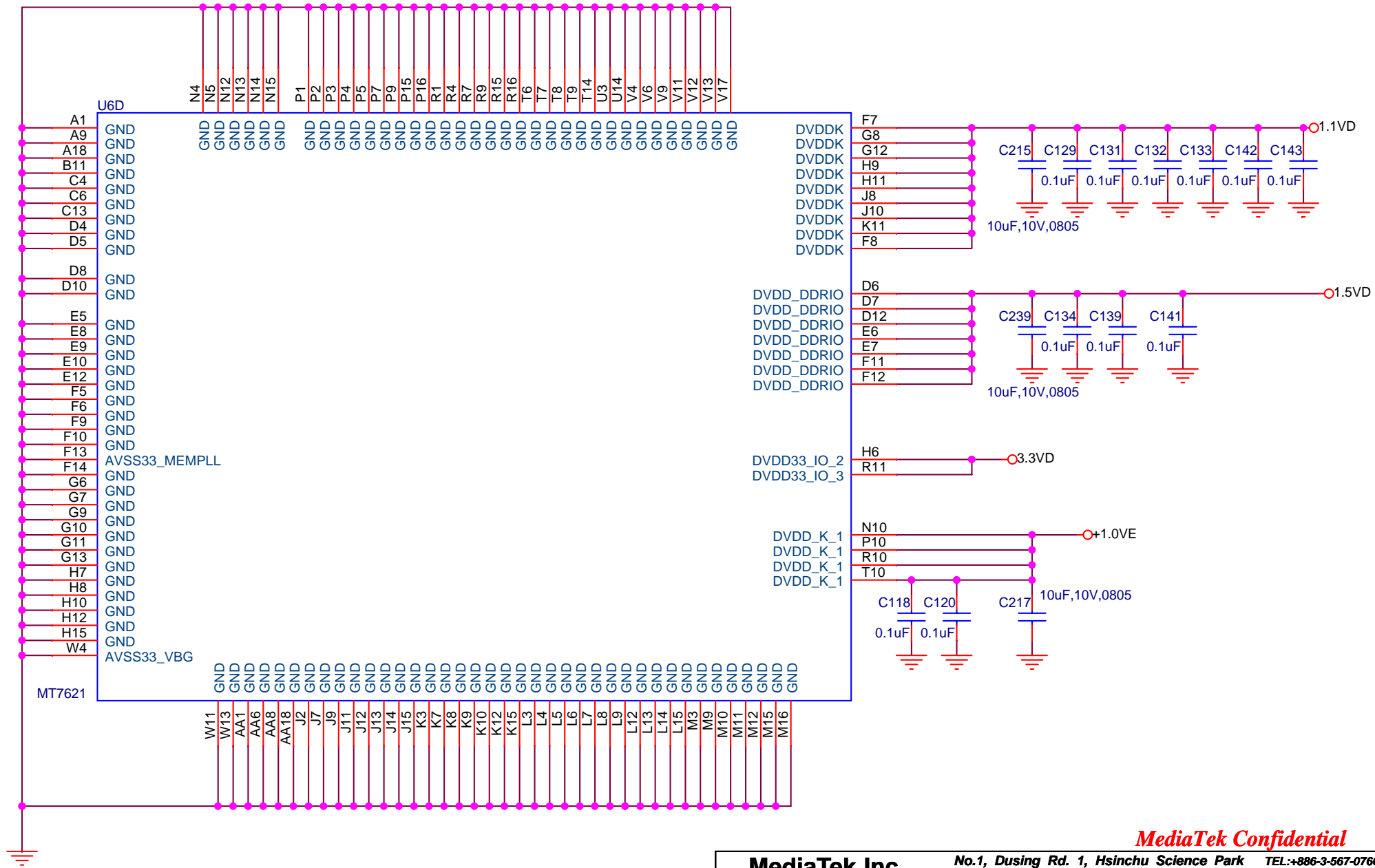
Sheet

4

of

16

MT7621 Power



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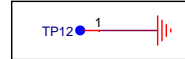
MEDIA/TEK


| | | | |
|-------------------------|----------------------------|-----------------------|------------|
| Title MT7621A | | | |
| Size A | Document Number MT7621A | Drawn Jimmy | Rev V11 |
| Date: | Monday, March 31, 2014 | Sheet 5 | of 16 |

Please remove it in real design

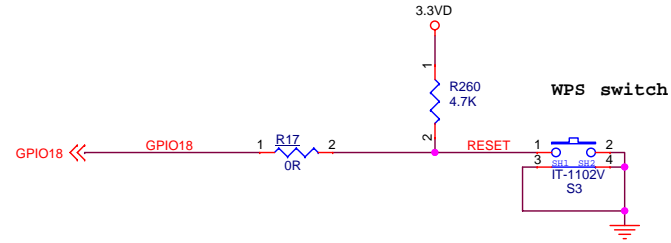
10/9 Unused

The diagram shows a 25MHz oscillator circuit. A central component, U24, is a 25MHz oscillator with a 2.5x3.2mm package. It has four pins: 1 (top left), 2 (bottom left), 3 (bottom right), and 4 (top right). Pin 1 is connected to a 18pF capacitor (C326) which is then connected to ground. Pin 2 is connected to a 18pF capacitor (C327) which is then connected to ground. Pin 3 is connected to ground. Pin 4 is connected to ground. The text 'Please remove it in real design' is written in green at the top, and '10/9 Unused' is written in red at the top right.

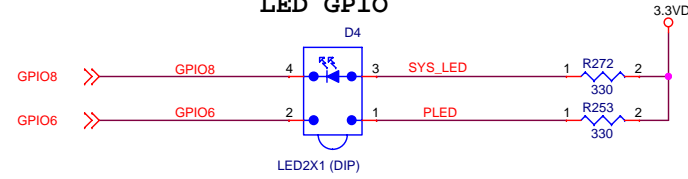


| | | | | | |
|---|---------------------------------|---|---------|--|------------|
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|  | Title MT7621A | | | | |
| | Size B | Document Number MT7621A | | Drawn Jimmy | Rev V11 |
| | Date: Friday, February 26, 2016 | | Sheet 6 | of 16 | |

GPIO18/WPS/RESET

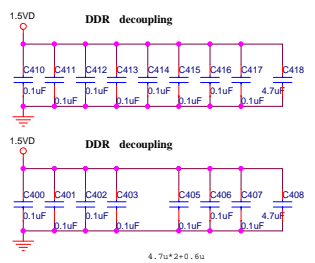
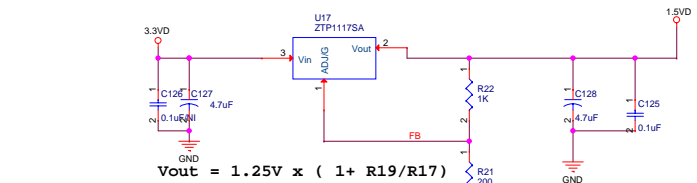


LED GPIO



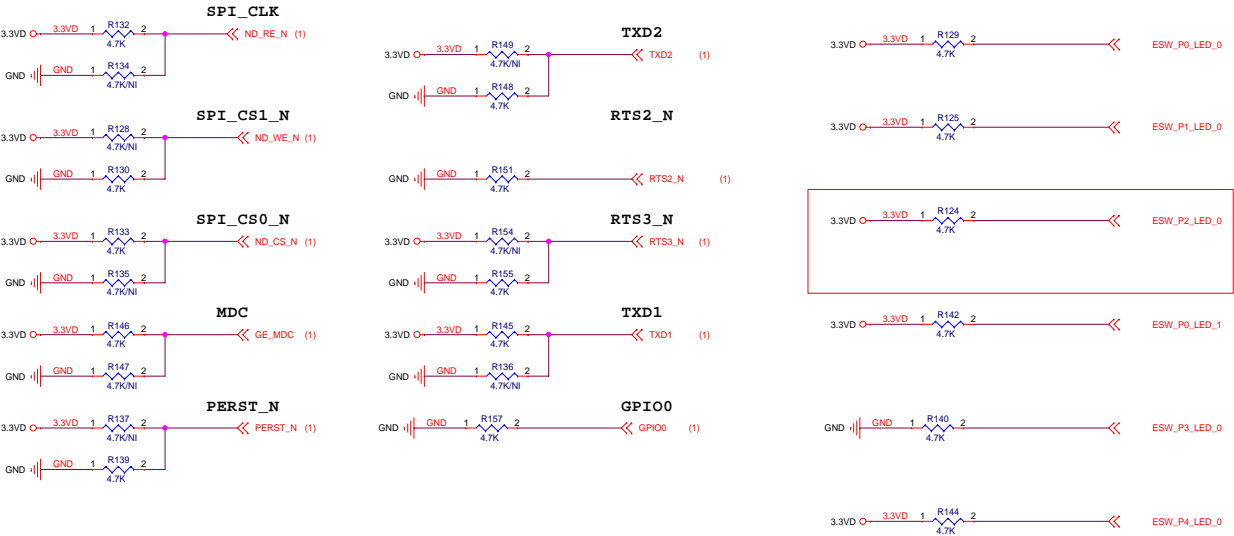
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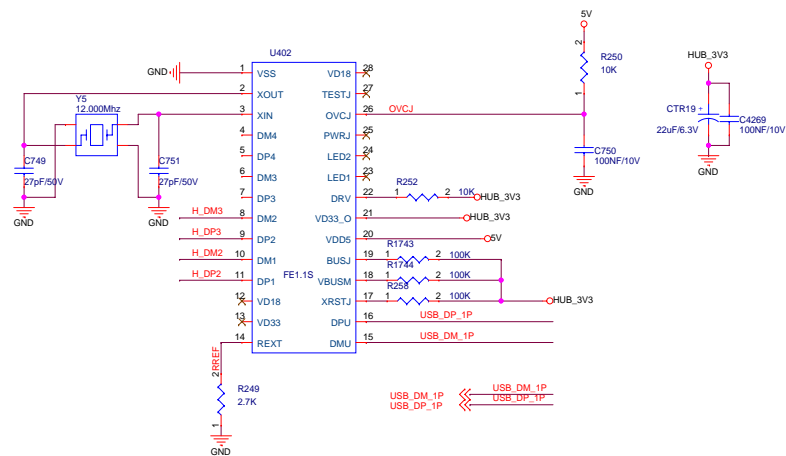
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| Title | | MT7621A | | |
| Size B | Document Number | | Drawn | Rev |
| | MT7621A | | Jimmy | V11 |
| Date: | | Monday, March 07, 2016 | Sheet | 7 of 16 |



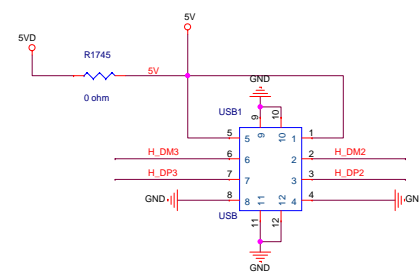
| Pin Name | Description | Value | |
|--|----------------|---|---|
| SPI_CLK | DRAM_FROM_EE | For non scan mode: 0: DRAM/PLL configuration from EEPROM 1: DRAM configuration from Auto Detect | For FT mode: 0: SUTIF 1: 3-wire SPI |
| {SPI_CS1_N, SPI_CS0_N, MDC } | XTAL_MODE | 000: 20 MHz, Self Oscillation mode 001: 20 MHz, Single end input 010: 20 MHz, differential input 011: 40 MHz, Self Oscillation mode | 100: 40 MHz, Single end input 101: 40 MHz, differential input 110: 25 MHz, Self Oscillation mode 111: 25 MHz, Single end input |
| PERST_N | OCP_RATIO | 0: 1:3 1: 1:4 | |
| TXD2 | DRAM_TYPE | 0: DDR3 1: DDR2 | |
| {RTS2_N, RTS3_N, TXD1, GPIO0} | CHIP_MODE[3:0] | 0000: Normal / Boot from SPI 4-byte address and XTAL clock 0001: Normal / Boot from ROM (NAND page 2k+64 bytes) 0010: Normal / Boot from SPI 3-byte address 0011: Normal / Boot from SPI 4-byte address 0100: iNIC RGMII / Boot from ROM 0101: iNIC MII / Boot from ROM 0110: iNIC RVMII / Boot from ROM 0111: iNIC PHY / Boot from ROM 1000: iNIC RGMII / Boot from ROM and XTAL clock 1001: Normal / Boot from internal SRAM 1010: Normal / Boot from ROM (NAND page 2k+128 bytes) 1011: Normal / Boot from ROM (NAND page 4k+128 bytes) 1100: Normal / Boot from ROM (NAND page 4k+224 bytes) 1101: Debug mode 1110: Scan mode 1111: Final Test | |

| Giga Switch Hardware Trap | | | | |
|---------------------------|------------|-----------------|--|---------|
| Pin Name | Trap | Fuction | Description | Default |
| P0_LED_0 | HWTRAP[0] | HT_CHIP_MODE[0] | chip_mode[3:0] 4'b0000: IDDQ mode 4'b0001: IOTEST mode 4'b0010: NANDTREE mode 4'b0011: RING mode (both IO and std-cell) 4'b0100: MBIST 4'b0101: SCAN mode (internal) 4'b0110: SCAN-COMP mode (compression) 4'b0111: SCAN-MBIST-OLT mode 4'b1000: AFE-OLT mode 4'b1001: GPHY ATE mode 4'b1010: GPHY ADUMP mode 4'b1011: GPHY ADUMP probe mode 4'b1100: Reserved 4'b1101: Reserved 4'b1110: bootup probe mode 4'b1111: normal mode | 4'b1111 |
| P1_LED_0 | HWTRAP[1] | HT_CHIP_MODE[1] | | |
| P2_LED_0 | HWTRAP[2] | HT_CHIP_MODE[2] | | |
| P0_LED_1 | HWTRAP[3] | HT_CHIP_MODE[3] | | |
| P3_LED_0 | HWTRAP[9] | HT_XTAL_FSEL[0] | External Crystal Frequency Selection xtal_freq_sel[1:0] 2'b01: 20MHz 2'b10: 40MHz 2'b11: 25MHz | 2'b10 |
| P4_LED_0 | HWTRAP[10] | HT_XTAL_FSEL[1] | | |



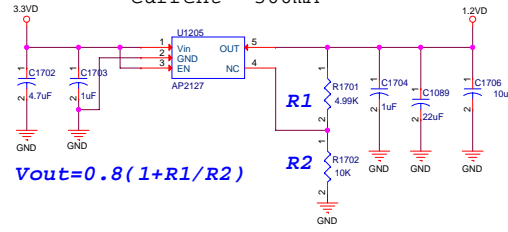


USB HOST1

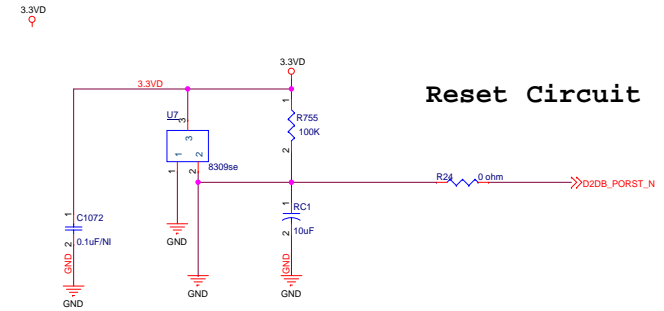


System Power

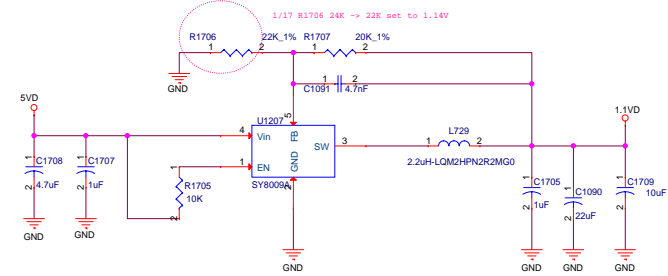
For USB/PCIE PHY Power (1.2V)
Current= 300mA



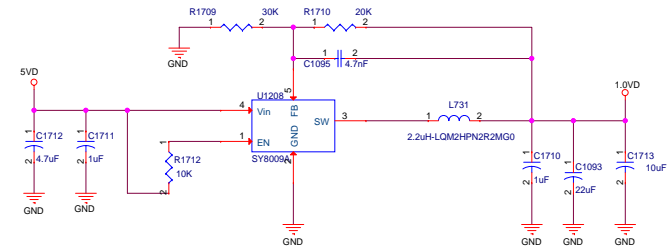
Reset Circuit



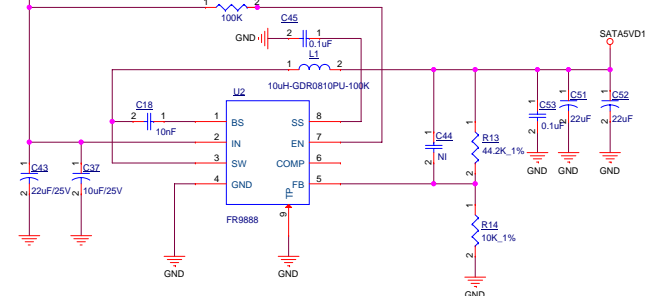
1.14V/1.5A



1.0V/1.5A



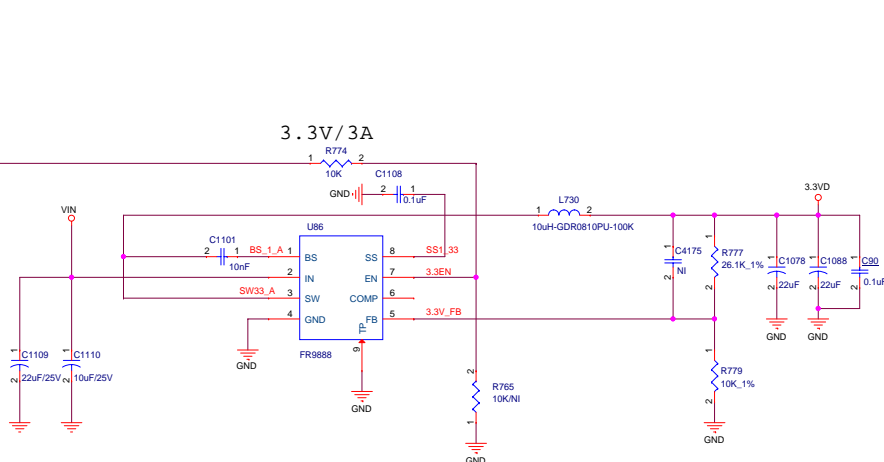
SATA POWER



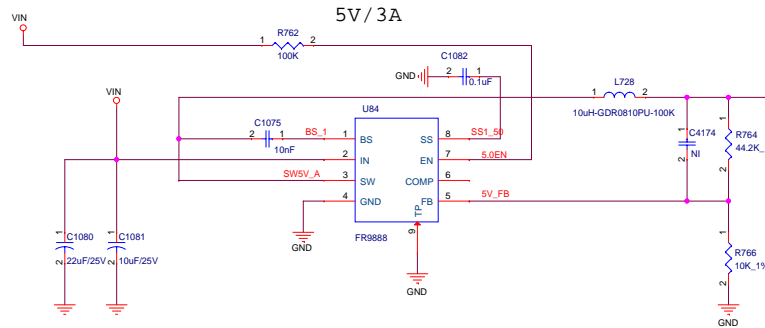
$V_{out} = 0.92(1 + R251/R252)$

$V_{out} = 0.92(1 + R255/R256)$

3.3V/3A

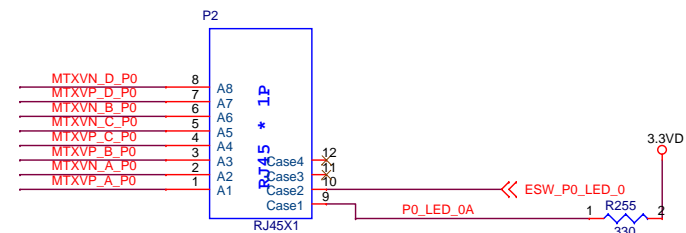
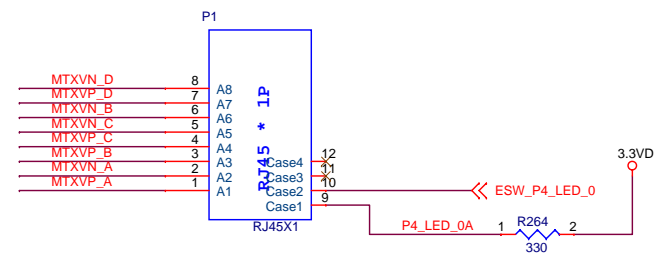
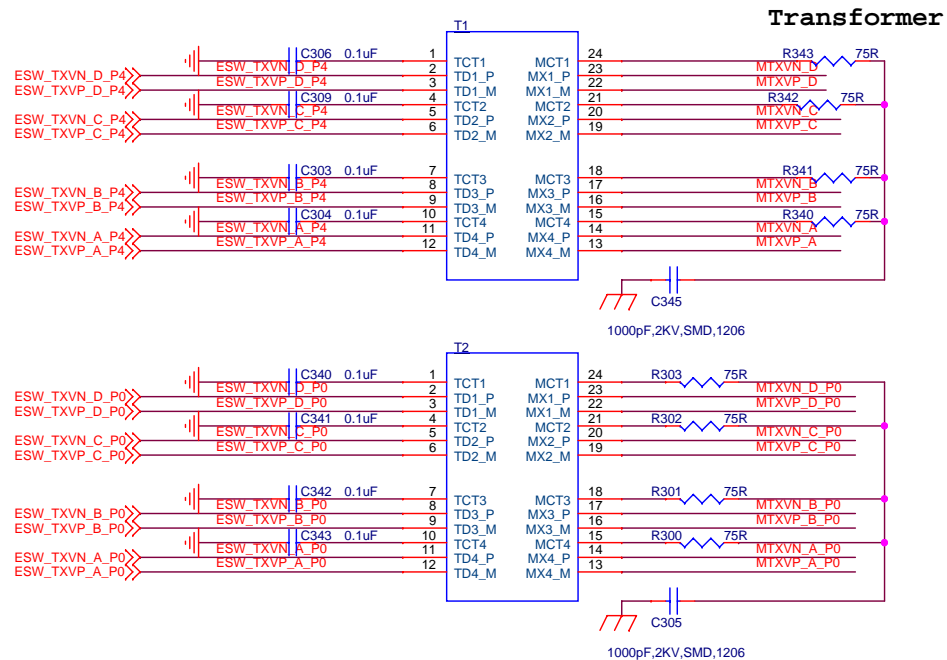


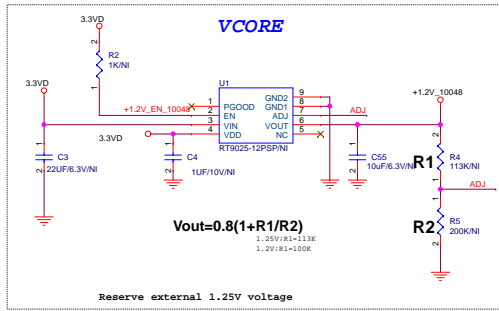
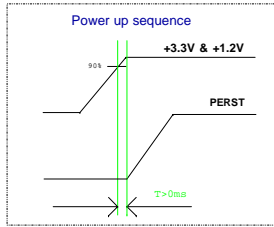
5V/3A



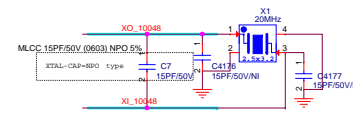
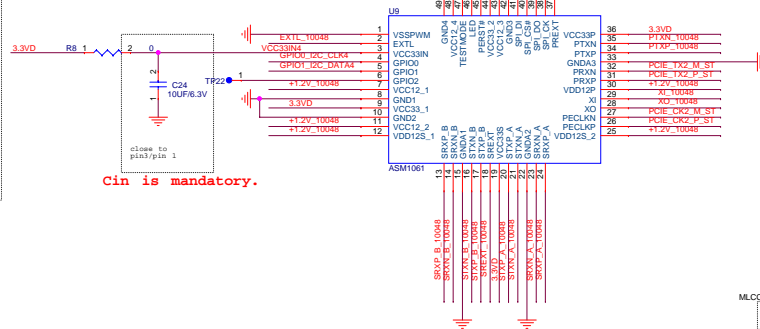
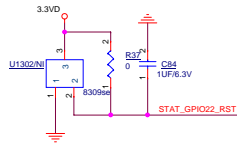
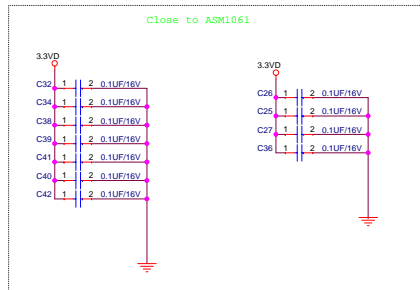
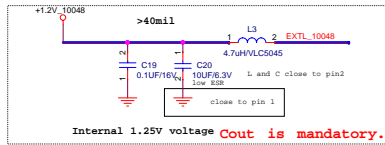
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|---------------|--|---|--|--|--|
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| File | | MT7621A | | Rev V11 | |
| Size | | Document Number | | Drawn | |
| C | | MT7621A | | Jimmy | |
| Date: | | Monday, March 07, 2016 | | Sheet 11 of 16 | |



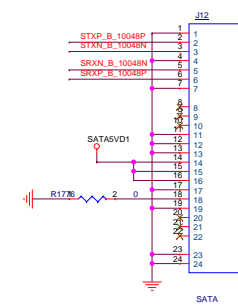
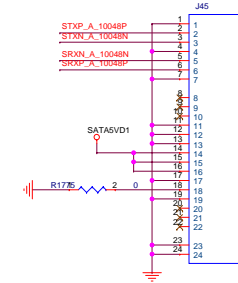
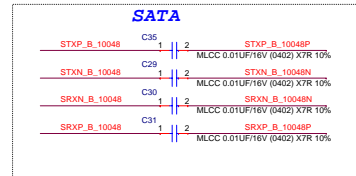
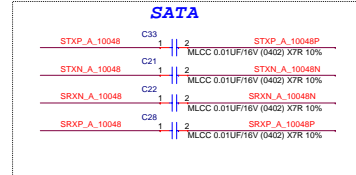
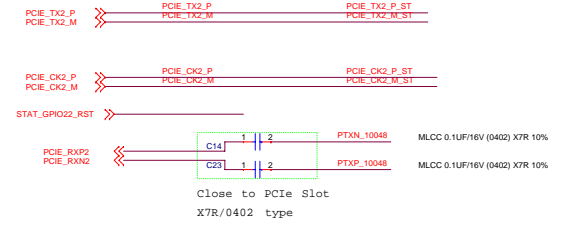


Option; refer to datasheet or contact FAE



Xi & Xo follow differential layout rule for Min. jitter

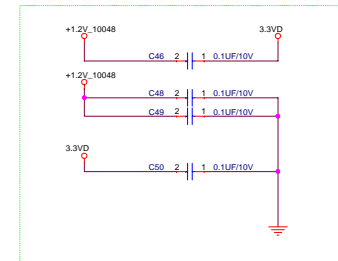
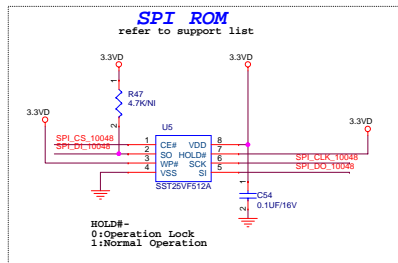
PCIe to SATA



H/W Strapping

refer to datasheet:

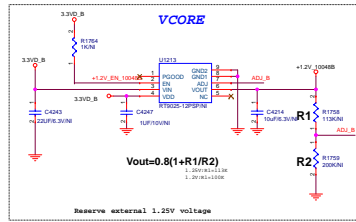
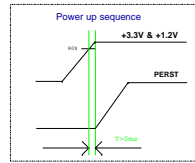
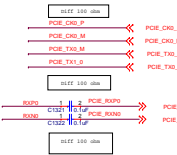
SPI_DO
0: Spin up by H/W
1: Spin up by S/W



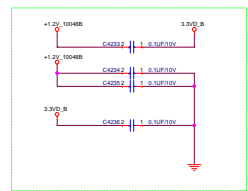
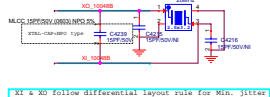
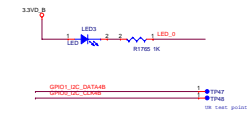
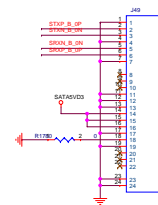
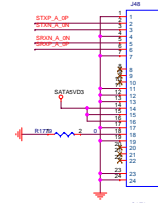
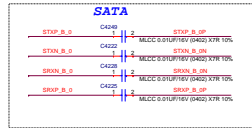
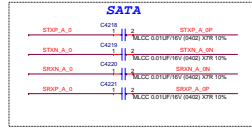
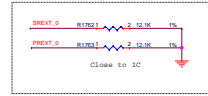
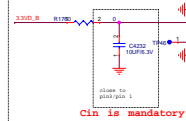
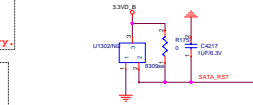
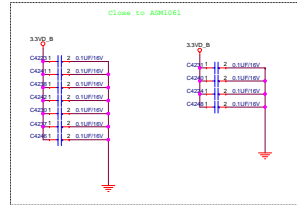
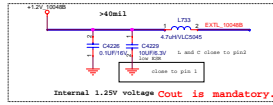
PCie to SATA



Close to PCIe Slot

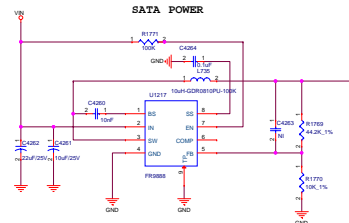
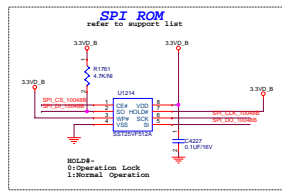
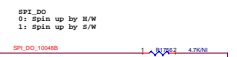


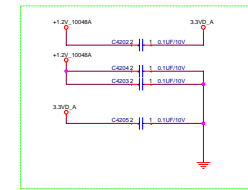
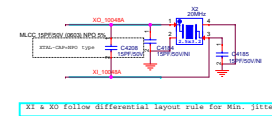
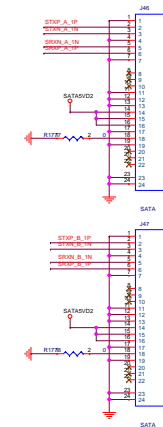
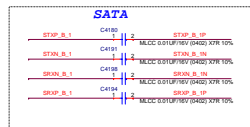
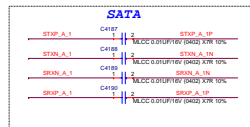
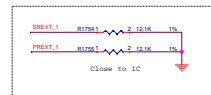
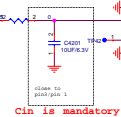
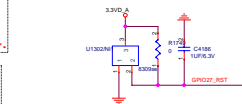
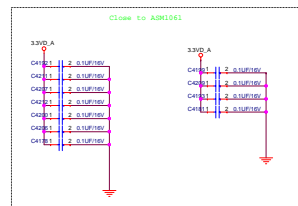
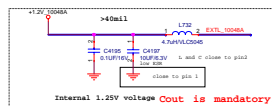
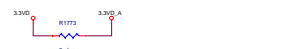
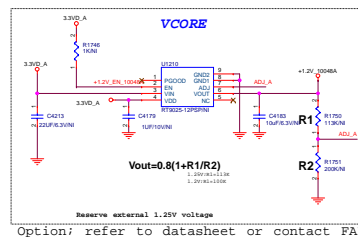
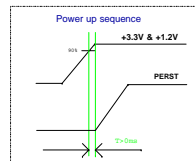
Option; refer to datasheet or contact FAE



H/W Strapping

refer to datasheet:





H/W Strapping

refer to datasheet:

