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Integration of Clock Gating and Power Gating in Digital Circuits

Agnes Shiny Rachel.N
Department of Electronics and Communication Engineering
Sri krishna college of technology
Kovaipudur, Coimbatore, India
agnesshinyrachel.n@skct.edu.in

Fahimunnisha.B
Department of Electronics and Communication Engineering
Sri krishna collegeof technology
Kovaipudur, Coimbatore, India
15tuec042@skct.edu.in

Akilandeswari.S
Department of Electronica and Communication Engineering.
Sri krishna college of technology
Kovaipudur, Coimbatore, India
15tuec011@skct.edu.in

Joyes Venula.S
Department of Electronics and Communication Engineering
Sri krishna college of technology
Kovaipudur, Coimbatore, India
15tuec061@skct.edu.in

***Abstract*— In integrated circuits, clocking system consumes a colossal portion of chip power, which includes switching activities of flip-flops, latches, clock distribution networks. Power gating and clock gating are two of the most effective techniques that is applied today for reducing dynamic and leakage power, respectively, in digital CMOS circuits. Power gating is essentially for reducing leakage power by switching off power supply to the nonoperational power domain of the chip during certain mode of operation. Header and footer switches, isolation cells and State Retention Flip Flops (SRFFs) used for implementing power gating. Clock gating is for reducing dynamic power by controlling switching activities on the clock path. Generally, Gate, Latch, or FF based clock gating cells used for implementing clock gating. The combined use of the two solutions, however , possess some challenges in terms of practical integration of the required control logics and power/timing overhead associated to it. Here we present an analysis in Cadence virtuoso tool using 90nm technology using a simple PIPO (parallel in parallel out) shift register. This project specifically targets the combined application of clock and power gating techniques.**

Keywords—dynamic power, leakage power, digital CMOS circuit, switching activities, power overhead.

I. INTRODUCTION

In the field of computer architecture, power consumption is one of the frequently occurring design constraints as per the recent advancements. This is due to both static and dynamic power consumption. Static is power consumed when the device is idle or if there is no switching activity. Moreover, dynamic is due to the frequent toggling of signals. To control this static and dynamic power consumption several clock gating and power gating techniques ca be applied together.

The clock gating techniques can be extended to provide a sleep signal for controlling switch circuits that reduce active leakage power, which is expected to achieve a fine-grained power gating technique as per this patent [1]. Grouping of gates called clustering can also be done in power gating, this cluster can be controlled by the sleep transistors [2]. While sharing the control logic by enabling them between the clock gating and power gating, clustering process have to be constrained [2]. Here clusters are nothing but the cells that is used for clock gating by using same registers. The positive effect is that the clock gating signals heave been used as control signals for sleep transistors to the best and the negative effect of using clusters is that it results in sub-optimal group of clusters for which power gating is actually done [2].

These two techniques can be coupled in a way such that the data out of clock gating can help in driving the control signal of the power gating circuit, which provides additionally more leakage power minimizations [3]. Implementing them is not easy and industrial design flow meets lot of challenges. First gated clock netlist is generated, and then partitioning of the clock gating circuits into clusters is done. For each clusters sleep transistors are introduced on a row-based granularity and achieved run time leakage reductions.

As studied from the paper [4] clock gated circuit's output signal drive the power gating circuit. Here activity driven fine-grained clock gating [FGCG] [4] and power gating [FGPG] is proposed. FGPG is that in a circuit having many power domains, placing only a portion of the circuit in a standby mode so that leakage power is reduced in which a particular block is in active mode. Initially a method named optimized -bus-specific-clock-gating [OBSCG] is introduced where by choosing applicable set of flip-flops there is a reduction in the usage of number of gated flip-flops. This is followed by another method called run-time-power-gating [RTPG] is proposed especially for power gating circuits with the stacking technique in them. The above techniques together greatly reduces dynamic as well as leakage power.

In [5] bus specific clock gating [BSCG] with a common Exor gate their signals are used to drive the power gating circuit. As a result, when temperature increases both average and leakage power is reduced. There are some application-based cases [6] where we can make use of transmission gates and latch free techniques of clock gating with low voltage complementary metal oxide semiconductor [LVCMOS]. LVCMOS is used because designers can work in several preferred different voltages such as LVCMOS 10, LVCMOS 12, LVCMOS 15, LVCMOS 18, LVCMOS 25, and LVCMOS 33. Power gating here [6] is implemented using MTCMOS (multi threshold complementary metal oxide semiconductor) to reduce leakage power dissipation.

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From the study of above reference work, we have selected simple and efficient techniques of clock gating and power gating and proposed a PIPO (parallel in parallel out) shift register design with reduced static power consumption and dynamic power consumption of an circuit.

II. BACKGROUND

Within the past few years, many designers projected several techniques for power consumption in digital CMOS circuits. In the following headings, concisely summarized the most effective techniques concerning leakage and dynamic power optimization.

A. Leakage power

About four decades ago, VLSI chips have started their evolution where even now designers are still looking for improvement in the IC performance like less area and power. One of the major challenges encountered by designers are leakage current which is due to gate induced drain leakage current, subthreshold leakage, hot electron effect, gate tunneling etc.

The total power consumption of CMOS can be summed by components like dynamic power, short circuit power and static power [8]. Here static power consumption is mainly due to leakage currents in MOSFET device

It is the result of flow of unwanted current (sub threshold current) in the channel of the transistor even when the transistor is in off state. This greatly influences the threshold voltage of the transistors in the circuits. To reduce this defect, scholars have introduced many power gating techniques. Power gating implicates turning off the power supply to a particular block or blocks when they are not working towards the output or when they are in idle stage.

Power gating can also done by transistor stacking techniques. In this method [7] when a series of transistors are connected as shown in the fig.1 the subthreshold leakage current flowing through these gets bowed off. This is well-known as “stacking effect” or “self-reverse bias”. The major disadvantage of this method is that as the transistor count is increased so the delay also increases [8].

So in this paper, have chosen LECTOR and GALEOR techniques in our power gating architecture which is more efficient [9] in leakage power as well as delay.

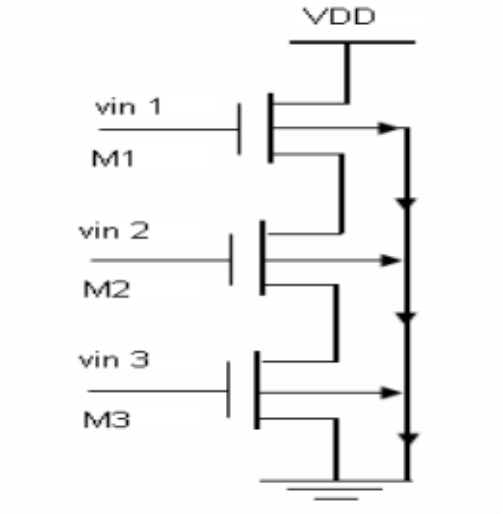

Fig 1. Example for stacking of transistors

B. Dynamic power

The power density is that in a unit area the amount of power dissipated by a chip. They are of two types static and dynamic. In a chip, each CMOS dissipates power when a switching activity takes place in the inputs and outputs. Rapidly switching transistors dissipates more power when compared to the transistors that are switching slowly. This is dynamic power dissipation and the main cause for this is the clock signal used in the circuit.

For example [10], increase in a processor’s clock speed involves switching its transistors more rapidly. Therefore, clock speed rises so does its dynamic power. Also clock consumes 40% of the total power in a circuit. Reduction of switching activity in clock pulse reduces the major power consumption of the circuit as well as the dynamic power dissipation.

For reducing, the clock switching activities various techniques developed. One of them is clock gating, which is based on the concept of powering off the clock to the flip-flops or memory elements that are not taking part in the current processing, therefore their unnecessary switching is stopped in order to save dynamic power [11].

III. PROPOSED DESIGN

In this suggested design both gated clock and gated power given to a normal PIPO shift register. Here clock gating is instigated using two techniques namely AND based clock gating and flip-flop based clock gating. Similarly, for power gating two techniques namely GALEOR and LECTOR are used. After including power gating to clock gated design decrease in dynamic and leakage power is accomplished.

A. Clock gating

Reducing dynamic power can be effectively done using clock gating techniques. In [12] AND based CG, as shown in fig 2 AND gate enables only when both the inputs are of high value. So one input of clock will be an enable signal, which will be high only when the input and output of PIPO is different [12]. The other input will be clock signal. When enable is high, the clock will be fed into the design. This efficiently reduces the active power due to changing of clock signal

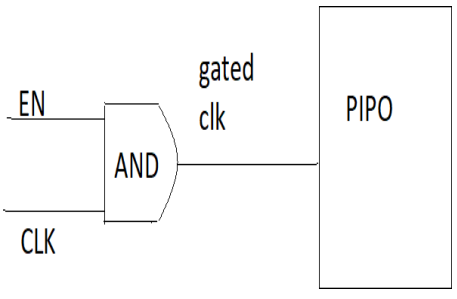

Fig 2. Clock gating using LECTOR AND gate

Flip-flop centered clock gating is a positive edge triggered flip-flop as shown in fig 3 is used for enable pin controls. This is similar to latch based clock gating [12]. Flip-flop is

controlled by the AND gate and the enable pin. While analyzing them we have encountered several drawbacks. Since flip-flops have longer sleep periods and they are affected by glitches, they require more capacitance for charging and discharging switching activity [12]. This largely affected circuit design and performance.

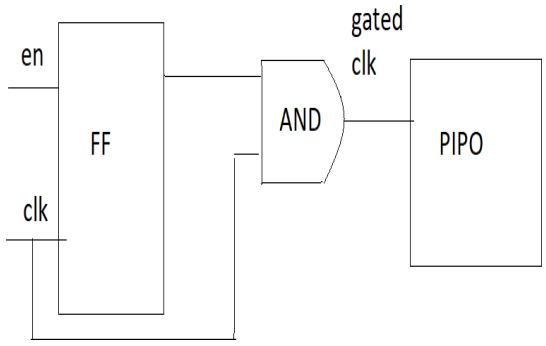

Fig 3. Clock gating using normal D flip-flop

B. *Power gating*

Here two techniques are analyzed GALEOR & LECTOR and reduction of power consumption in PIPO shift register observed. In GALEOR, introduce two CMOS transistors as shown in figure 4, PMOS and an NMOS transistor. Between the PUN (pull up network) and the output line an PMOS transistor with zero volt is fed. Similarly, an NMOS transistor is kept in between the PDN (pull down network) and the output of logic circuit with value one volt [11]. Due to the stacking of transistors leakage power is being reduced compared to a normal PIPO shift register. Though switching activities in inputs of these two transistors causes unnecessary delay in PIPO, which is a major drawback of GALEOR. In LECTOR again two transistors are introduced in a similar steps as done in GALEOR. However, input voltages not provided separately for each instead gate terminals of each transistor control the sources respectively. Here there is no delay due to the switching of inputs, so the leakage power enormously condensed here.

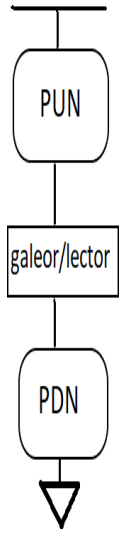

Fig 4. Power gating techniques.

IV. EXPERIMENTAL RESULTS

A. *Clock gating analysis*

The analysis of PIPO shift register using different power gating and cock gating techniques using cadence virtuoso with 90nm technology, the output power randomly varied in each techniques. Instead of using simple clock gating technique using AND gate, we proposed an LECTOR based AND gate which eventually reduced more power. On comparing LECTOR AND & a normal AND gate 3% of power is reduced in LECTOR AND.

Now this LECTOR AND gate helped in reducing nearly 15.20% of static power which is the ultimate aim of introducing clock gating in a digital circuit, the so called average power in cadence is given in below table.

TABLE I.

Technique	Total power	Leakage power	Average power
PIPO with DFF based CG	138.9417uW	34.853uW	688.1nW
PIPO with LECTOR AND based CG	126.682uW	32.997uW	597.3nW

Clock gating analysis in PIPO

B. *Power gating analysis*

Similarly, in the module of power gating PIPO using LECTOR & GALEOR techniques implemented. Moreover, leakage power reduction in LECTOR technique was comparatively high with GALEOR. As per the table given below LECTOR was able to reduce nearly 8.4 % of leakage power in PIPO

TABLE II.

Technique	Total power	Leakage power	Average power
PIPO with GALEOR	92.15739uW	214.118nW	329.6E-9W
PIPO with LECTOR	86.8604uW	197.3721nW	289.5E-9W

Power gating analysis in PIPO

C. *Combining CG and PG*

Finally when both power gating and clock gating gets combine together for PIPO shift register both static and dynamic power got reduced accordingly as per shown in the below table. Moreover, considering only the efficient LECTOR AND based clock-gating technique with the GALEOR & LECTOR power gating LECTOR again proved to be better by reducing the total power consumption of PIPO shift register to nearly 0.3 percentage. The observed

output graph of PIPO shift register is shown in figure 6 for the respective schematic in figure 5.

TABLE III.

Technique	Total power	Leakage power	Average power
PIPO+AND based CG +GALEOR PG	124.7744uW	32.9974uW	590.4nW
PIPO+AND based CG +LECTOR PG	124.2984uW	32.811uW	570nW

Clock gating and power gating analysis in PIPO

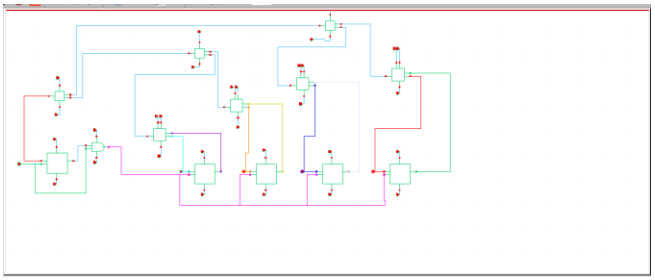

Fig 5 Schematic of combined clock gating and power gating in PIPO shift register

Fig 6 Output graph of PIPO after integration of clock gating and power gating.

V. CONCLUSION

Thus by implementing PIPO shift register in Cadence virtuoso with low power consumption by integration of both clock and power gating techniques is proved to be efficient. From the above study we conclude that when compared to flip-flop based clock gating LECTOR AND based clock gating was more efficient by reducing nearly 1.6% of static power consumption of the whole PIPO. Similarly LECTOR based power gating technique was better than GALEOR in reducing leakage power to nearly 0.5% and thus the total power about 0.3% got reduced successfully.

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