Transistor Self-Heating: The Rising Challenge for Semiconductor Testing

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***Abstract*—Quantum confinement in 3-D device structure together with the newly employed materials like silicon-germanium (SiGe) in advanced technologies (e.g., FinFET, nanowire, nanosheets, etc.) makes transistors seriously suffer from localized self-heating effects in which generated heat within the transistor's channel is trapped inside. This is mainly due to the much lower channel and surrounding material thermal conductivity and hence lower ability for heat dissipation along with the firm isolation needed for better gate control. Self-heating effects strongly accelerate transistor aging and all the underlying defect generation mechanisms leading to serious reliability problems during the early life of chips. The key challenge in transistor self-heating when it comes to semiconductor testing is the profound difficulty in measuring self-heating directly as generated heat is trapped inside the transistor. Failing in capturing self-heating phenomenon during IC testing would later lead to chips malfunctions at run-time and hence early life failures because of reliability degradations and failure mechanisms will be unexpectedly accelerated akin to excessive internal temperatures.**

In this paper, we investigate the impact of self-heating effects on n-type and p-type FinFET transistors calibrated with Intel 14 nm measurement data using mature Technology CAD (TCAD) simulations. Then, the industry standard compact model for FinFET technologies (BSIM-CMG) is carefully calibrated to accurately model and reproduce all measurements. This enables circuit's designers, for the first time, to accurately investigate how emerging self-heating effects in transistors impacts the performance and power of large circuits. This opens new doors for developing novel Design-for-Testing methods that effectively reveal self-heating effects and increase the yield of chips.

***Index Terms*—Reliability, FinFET, Transistor Self-Heating, Industry Compact Model (BSIM-CMG), Advanced Technology**

I. Introduction

The multi-gate device structures such as FinFETs, silicon nanowire (SiNW) FETs and nanosheet FET have emerged as promising CMOS logic devices due to their excellent performance in the term of high I_{ON}/I_{OFF} ratio, suppressed short channel effects, lower sub-threshold slope, power performance and increases transistor density per chip [1] [2] [3]. However, non-planar 3D-devices are expected to suffer from serious self-heating effects as nanoscale dimensions cause a high thermal resistance between the heat source and metal contacts, low thermal coupling [4], and ever-increasing effects of quantum confinement. The higher thermal resistance of silicon channel, including low thermal conductivity of SiO_2/high-κ surrounds the fins and extension length of 3-D FinFET, exacerbates the SHE [5]. The self-heating critically influences device performance, such as carrier mobility degradation, negative output conductance, threshold voltage shift, and device reliability problem, thus shortening the device lifetime [6]. The self-heating becomes more severe for 14nm FinFETs and devices with a dense array or multi-fin transistor [7].

The Key Challenge for IC Testing: Existing Design-for-Testing (DFT) methods are not yet aware or prepared to reveal if transistor self-heating has occurred in chips under test or not. Failing in capturing this critical information at the design time during IC test would later lead to chips malfunctions at run-time. Hence early life failures because of reliability degradations and failure mechanisms will be unexpectedly accelerated. Some of those failures will even have a temporal nature as they are driven by quantum mechanics and hence they will only appear once an excessive temperature has emerged within the underlying transistors. This, however, heavily depends on the activities and stress that the chip is being subject to. Hence, chips when are shipped back after exhibiting early life failures, will successfully pass the performed IC tests and again be classified "healthy" and thus the source of failures remain ambiguous and uncovered, leading to large cost overheads.

Why Self-Heating is Deceptive: First and foremost, available on-chip thermal sensors/diodes measure only the silicon die temperature and therefore they cannot detect or sense self-heating because the generated heat is inside transistors and is not able to reach the silicon substrate at which on-chip thermal sensors can measure. On the other hand, available on-chip delay sensors will also fail in detecting self-heating because despite the excessive temperature generated by self-heating, the corresponding impact on the induced delay increase in logic gates might still small and within the tolerated range caused by conventional process variation. This is because with technology scaling, operating voltage becomes very close to the voltage at which the Zero Temperature Coefficient (ZTC) occurs. In other words, delay increases induced by self-heating will be hidden and indistinguishable from delay variation normally caused by manufacturing variability, which are accepted and can be mitigated by traditional means of guardbanding. On top of that, the self-heating phenomenon itself is profoundly hard to be directly measured because generated heat is deeply trapped inside the transistor, unless very expensive testing equipment using single-photon detector within picosecond time scale is employed. Such equipment can nevertheless merely analyze a single transistor and cannot deal with complex circuits or full chips.

Note that SHE is not sensitive to process variations as thermal and electrical behavior does not change drastically in

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a good quality process. However, variations in the transistor channel doping can impact the channel thermal resistance and hence SHE. Digital PDKs generally do not model self-heating because extra test-structures and measurements (time and frequency domain) are required to correctly characterize the self-heating effect. Only after careful measurements and parameters extraction, we can get values of thermal resistance and thermal capacitance, as presented in our paper, which when put into the device modeling can predict correct electrical and thermal behavior of the transistors and the consequences on circuits. In addition, delay tests will not be able to separate out SHE from other coupled electrical effects. The best way to measure SHE is through time and frequency domain measurements, where variation in Re(Y22) or channel conductance and other quantities are measured [8]. Last but note least, SHE does not cause defects by itself directly. However, excessive heat due to SHE accelerate aging mechanisms like HCI. Existing ATPG and BIST techniques, developed to detect transistor aging, might be employed. Nevertheless, they will not be able to differentiate between the contribution of conventional transistor aging and SHE. Detailed investigation and further research on how existing ATPG and BIST techniques should be modified to account for SHE and detect SHE are indeed still required. Note that oxide trap defects activated due to SHE-stimulated quantum tunneling might cause temporal (random by nature) degradations, which makes detecting SHE-related degradations more challenging and new testing methods might be required.

In summary: Chips under test can successfully pass the performed tests because the degradations (such as delay increases) induced by self-heating might be marginal and within the accepted tolerable ranges. However, those chips later under certain conditions triggered by the end-user workload activities [9], start to failure as actual stress in the field may exaggerate self-heating leading to an unexpected acceleration of defect mechanisms and hence early life failures. It is noteworthy that at extreme feature sizes (e.g., 3nm and 5nm), the number of defects is very small. Therefore, displacing just few atoms within transistors can destroy the entire functionality. Due to the temporal nature of those failures, chips when are shipped back, after exhibiting early life failure, will again successfully pass the performed tests, leaving the source of failure unknown.

Our Novel Contribution: This paper demonstrates a comprehensive simulation framework for revealing self-heating effects (SHE) at an advanced technology node; 14nm FinFETs fully calibrated with Intel measurement data [10]. Our implementation and analysis go from the device-level modeling all the way up to SPICE model parameter extraction for the industry standard compact model of FinFET technology (BSIM-CMG). The complete simulation methodology flow chart presenting different steps used in this paper is shown in Fig. 1. The flow begins with the 3D-TCAD (Technology CAD) process and device simulations for electrical I-V calibration with 14nm FinFET experimental data from Intel [10]. The first output of the TCAD device simulation is used to extract

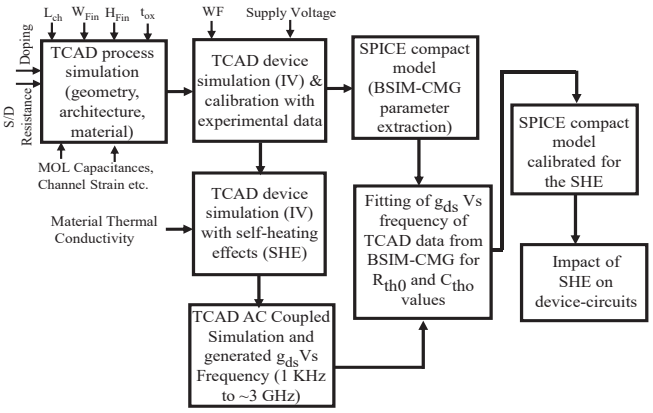

Fig. 1. Overview of our self-heating simulation methodology starting from physics and device calibration with Intel measurement data to industry standard compact model calibration which enables accurate circuit simulations.

the SPICE compact model parameters to further speed up the circuit simulations. The second output of the TCAD calibrated device simulation is used to analyze the impact of SHE on device performance parameters from the TCAD thermal simulation. In further steps, the AC coupled TCAD simulation has been performed to examine the effect of dynamic SHE with frequency and generated g_{ds} vs. frequency relation. Thereafter, we have calibrated the BSIM-CMG model for the SHE and precisely extracted the thermal resistance and thermal capacitance values. In addition, the SHE calibrated BSIM-CMG model parameters are modified to predict the SHE for multi-fin devices. The accurate SHE fin dependent exponent is extracted for both n and p FinFET to predict the SHE for multi-fin devices. In addition, we investigated the impact of dynamic self-heating with a number of fins for a wide range of frequencies. The temperature and I_{ON} dependency with switching frequency results demonstrate the impact of SHE is high until the iso-thermal frequency $\sim$ 2.78 GHz and $\sim$ 1.77 GHz for n and p FinFETs, respectively. Understanding heat dissipation in novel 3D FinFETs structures is of significant importance not only for designing energy-efficient circuits but also for preventing costly early life failures as well as ensuring circuit's reliability for the entire projected lifetime.

II. Related Work

In the previous works, there have been several discussions on the SHE characterization methods for FinFETs devices such as the small-signal AC output conductance (ACC) [11], pulse rise time [12], and changes in the DC gate resistance [13] method. In [14], the impact of self-heating on FinFETs has characterized using 2 port S-parameter data. The AC coupled method is highly accurate for the frequency in the range of a few GHz (e.g., below 5 GHz), and the S-parameter method is for higher frequency in the RF application range. The AC coupled method has been adopted in our simulation for SHE analysis since the digital circuits operate in the range of 1 to 3 GHz. Most of the SHE work in the literature has focused on nFinFETs devices, and rarely analyzed pFinFETs.

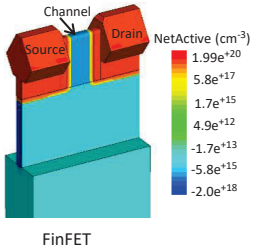

Table I: Device Parameters

Parameters	Bulk FinFET
Channel Length (nm)	20
Fin Width (nm)	8
Fin Height (nm)	42
Fin Pitch (nm)	42
EOT (nm)	~1
Source/drain Doping (cm-3)	2e20
Channel Doping (cm-3)	2e18

Fig. 2. The 3-D 14 nm FinFET device structure along with the device parameters used in the Technology CAD (TCAD) simulations.

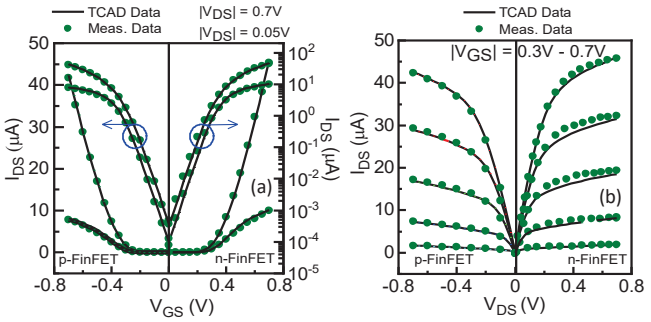

Fig. 3. (a) $I_{DS} - V_{GS}$ (b) $I_{DS} - V_{DS}$ calibration between the our TCAD modeling and measurement data from Intel 14nm FinFET [10] [16] for both n-type and p-type transistors.

However, due to *newly SiGe material adopted recently* in pFinFET, which has lower thermal conductivity compared to silicon (Si), pFinFETs become subject to severe SHE. Therefore, in this work we investigate both nFinFET and pFinFET together. [13] demonstrated that at lower technology node SiGe pFinFET have $54\ \%$ worse self-heating than relaxed germanium (rGe) channels, and $115\ \%$ compared to silicon. The thermal conductivity of alloy materials such as SiGe is strongly reduced over pure materials due to mass disorder scattering [15]. Therefore, for the accurate prediction of circuit behavior in advanced technology nodes, the impact of SHE on both n and p FinFET needs to be carefully analyzed.

III. TCAD SETUP AND CALIBRATION

The 3D self-consistent electro-thermal simulations have been performed to analyze the electrical and thermal properties of 14nm bulk FinFETs using commercial Sentaurus Technology CAD (TCAD) simulator from Synopsys.

A. Electrical I-V Simulations and Calibration

The TCAD models for nFinFETs and pFinFETs are carefully calibrated to reproduce the I-V characteristics extracted from the reported Intel 14nm FinFET measured data [10]. Fig. 2 shows the 3D device structure of 14nm FinFETs along with the device parameters given in Table. I. The device has created through TCAD sprocess simulation. The density gradient model has been used in the electrical simulation to account for the quantum confinement effects. The inversion and accumulation layer mobility model calibrated with the Lombardi model for high-κ dielectric interface and the thin layer mobility model accounts for the thickness of the Fin region. The simulations also included Fermi–Dirac statistics with a bandgap narrowing model to account for high carrier densities. Electron and hole multi-valley models are used for stress modeling. Channel strain related mobility improvement, crystal orientation effects on channel mobility, and ballistic mobility parameters to account for the quasi-ballistic carrier transport in these dimensions have been considered. The S/D doping, subfin doping, source–drain series resistance, gate metal work function, low-field mobility parameters, and high-field saturation parameters were calibrated to accurately reproduce the experimental data [10] for both p-FinFET and n-FinFET as shown in Fig. 3.

B. Thermal Simulation

The thermodynamic model is used in the thermal simulation to study the SHE in bulk FinFET. The thermal conductivity is the function of lattice temperature T, doping density N, layer thickness, and mole fraction for the alloy materials SiGe. Therefore, to account for all these effects, thermal conductivity (considering all different dependencies) and layer thickness models are also included in the physics modeling of TCAD. The thermal conductivity values of other materials such as gate material, spacer, and oxides have been obtained from [4]. The proper, equivalent boundary thermal resistance is used to characterize the thermal behavior at a source, drain, and gate contacts. Fig. 4 shows the thermal plot for the spatial temperature distribution due to SHE in a single-fin n/p-FinFET along channel and fin at a supply voltage of 0.8V. Fig. 5 (a) shows the variation of lattice temperature along the channel (corresponding to cut-lines A-A1 and B-B1 in the 2D view of Fig. 4) in both n and pFinFET. The lattice temperature peak in Fig. 5 (a) is indicated as the hotspot near the channel and drain extension. The input power increases with an increase in the supply voltage, and the device experiences a much larger temperature. The thermal plot shows the peak temperature increases up to $\sim$ 373K and $\sim$ 405K at 0.8V supply voltage for n and pFinFET, respectively. Fig. 4 shows the hot spots are distributed near the drain channel junction or, more precisely, near the channel and drain extension region. At a high lateral electric field, the carriers near the channel and drain extension get most of the energy, which leads to heat dissipation (due to phonon scattering) [17]. The impact of SHE is higher in pFinFET due to SiGe material used, which has lower thermal conductivity than Si used in nFinFET. Fig. 5 (b) shows the $I_{DS}-V_{DS}$ comparison of n and p FinFET for with and without SHE. As can be observed, SHE leads to noticeable current degradation.

IV. RESULT AND DISCUSSION

The basic TCAD setup and electrothermal simulation have been performed for n and p 14nm bulk FinFETs. However, the DC simulation is not enough to predict the correct device behavior due to SHE over a wide range of frequencies [18]. Therefore, the AC conductance method is adopted to analyze

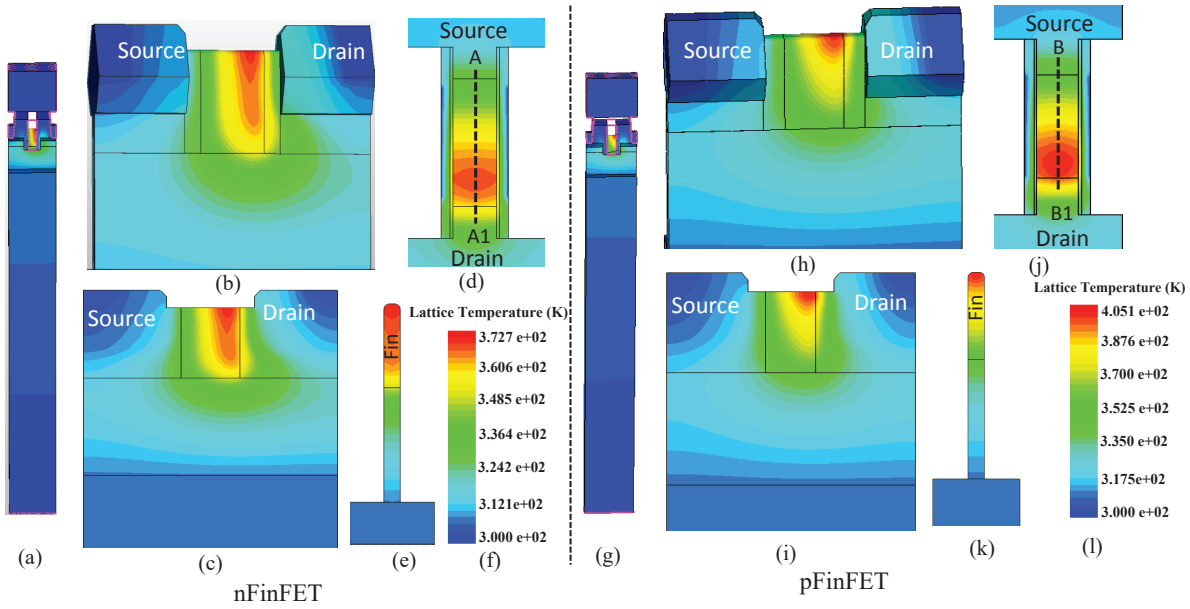

Fig. 4. The thermal plot of n/p FinFET in 3D and 2D cross-section view along the channel and fin, A-A1 and B-B1 cut-lines, show the channel's temperature distribution. Results obtained from 3D Technology CAD analysis after careful calibration with Intel 14nm FinFET measurement data.

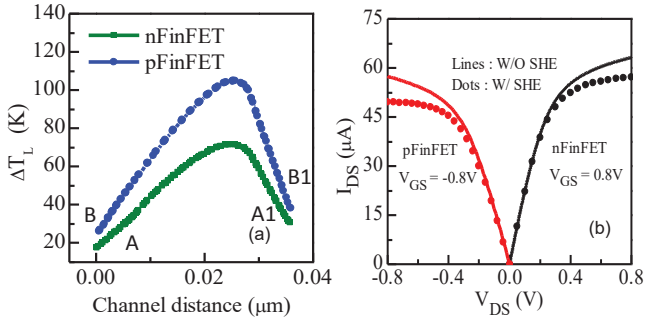

Fig. 5. (a) The temperature distribution across the fin as a cutline is A-A1 and B-B1 are indicated in Fig. 4. (b) The $I_{DS} - V_{DS}$ comparison of n and p FinFET for with and without SHE.

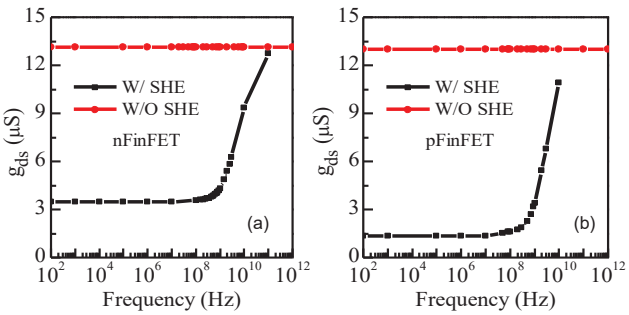

Fig. 6. (a, b) Show the g_{ds} vs frequency from the TCAD AC coupled simulation for n and p FinFET with and without SHE.

the accurate impact of self-heating with frequency [14]. Fig. 6 shows the drain conductance (g_{ds}) for a wide range of frequencies (from 100HZ to 100 GHz) from TCAD simulation with and without SHE. Fig. 6(a) shows the dynamic SHE is more pronounced up to 1 GHz frequency. After 1 GHz, the value of g_{ds} starts slightly increasing and at a higher frequency above 10 GHz, the value of g_{ds} reaches toward the without self-heating g_{ds} value. It shows the dynamic self-heating suppressed strongly at high frequency, consistent with reported data [19]. Fig. 6(b) shows the g_{ds} value is lower in pFinFET, which also underscores the higher impact of SHE in pFinFETs. In further subsection will discuss about the SHE related BSIM-CMG parameters extraction, which is needed to perform calibrated and accurate SPICE (circuit) simulations.

A. Calibration the Industry Standard Compact Model (BSIM-CMG) to account for SHE

In this subsection, the 14nm FinFET calibrated BSIM-CMG compact model is used to extract the SHE parameters since the TCAD simulation is very time consuming and not suitable to perform circuit simulations.

The g_{ds} vs. frequency methodology is adopted to extract the SHE parameters such as thermal resistance (R_{th}) and thermal capacitance (C_{th}) from BSIM-CMG model [20]. After activating the SHE mode, we have captured g_{ds} vs frequency (TCAD generated) behaviors by tuning the R_{th0} and C_{th0} of BSIM-CMG SHE related parameters. Fig. 7 shows the excellent g_{ds} vs frequency comparison between BSIM-CMG compact models with the TCAD simulation under the influence of SHE. The R_{th0} and C_{th0} are the BSIM-CMG SHE related parameters [21] used for the extraction of thermal resistance (R_{th}) and capacitance (C_{th}) as given below

$$\frac{1}{R_{th}} = \left(\frac{W_{TH0} \times NF^{BSHEXP} + FPITCH \times NFINtotal^{ASHEXP}}{R_{th0}}\right) \quad (1)$$

$$C_{th} = C_{th0}(W_{TH0} \times NF^{BSHEXP} + FPITCH \times NFINtotal^{ASHEXP}) \quad (2)$$

$$NFINtotal = NF \times NFIN \quad (3)$$

whereas, W_{TH0} is the width dependent coefficient, NF is a number of finger, NFIN is a number of the fin, and FPITCH is the fin pitch. The default value of the exponent BSHEXP and ASHEXP is 1. We found the thermal resistance R_{th0} is a more dominating parameter in matching the g_{ds} value for lower frequency range. Further, C_{th0} is used to match the g_{ds} value in the transition region above 500 MHz or the transition region. Fig. 7 shows the excellent matching of g_{ds} Vs frequency for both n and p FinFETs up to $\sim$ 5 GHz. The higher frequency (more than $\sim 5GHz$) generally use for RF applications that can be match by incorporating parasitic components such as gate parasitic network and substrate parasitic network. The extracted R_{th0} and C_{th0} are also used to compare the device DC characteristic between TCAD and BSIM-CMG model due to SHE. Fig. 8 (a, b) show the excellent matching of $I_{DS}-V_{GS}$ and $I_{DS} - V_{DS}$ characteristics between TCAD and BSIM-CMG model for both cases (i.e., with SHE and without SHE). These IVs comparison manifest itself the accuracy of extracted R_{th0} and C_{th0} values.

As AC conductance method is well enough to capture the dynamic self-heating in the range of $\sim 5GHz$. However, to validate the value of thermal time constant calculated from the AC coupled simulation, the pulse rise method is used. In this method, we applied a pulse signal on n and p FinFET devices for a wide range of input rise time from femtosecond to 100 ns. Fig. 9 (a, b) show the drain current and current degradation for both n and p FinFETs for the input pulse's different rise time values. Fig. 9 (a, b) show the dynamic self-heating is removed for both n and p FinFET for the rise time value in the range of pico to femtosecond. However, as the rise time increases, self-heating increases, resulting in $\sim$ 9 % and $\sim$ 16 % drain current degradation in n and p FinFET, respectively. Further, the thermal time constant is calculated as, the rise time when the drain current degradation is 63 % of the maximum value [12]. Table II shows thermal resistance, capacitance, a time constant, and isothermal frequency for n/p FinFETs. The isothermal frequency is the frequency up to which the SHE is dominant.

B. Impact of SHE in Multi-Fin Transistors

The calibrated BSIM-CMG model with SHE for single fin FinFET is further modified to analyze the SHE for multi-fin devices. In multi-fin FinFET, the temperature increases with an increase in fin number due to the rise in the drain current, thus increasing power dissipation. The temperature profile is non-homogeneous in the fins, middle region fins are more prone to SHE than the outer fins [22]. This is because of the low thermal coupling between the central region fins and the

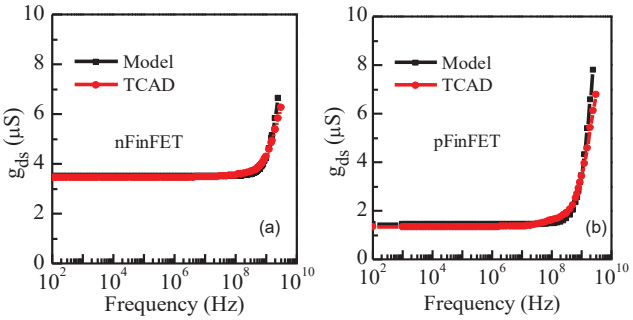

Fig. 7. (a-b) shows the g_{ds} vs frequency comparison between BSIM-CMG model and TCAD.

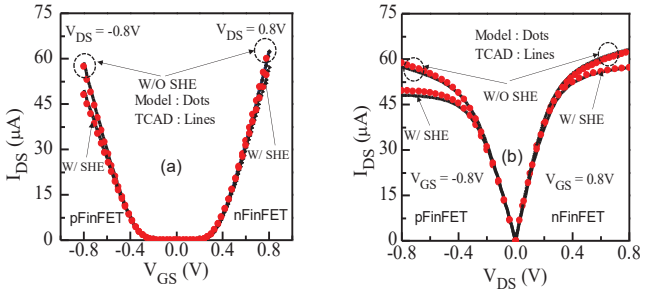

Fig. 8. (a-b) $I_{DS} - V_{GS}$ and $I_{DS} - V_{DS}$ characteristic with and without SHE. Comparisons demonstrate the excellent matching between TCAD results and SPICE simulations proving the properly calibration of the industry standard compact model (BSIM-CMG).

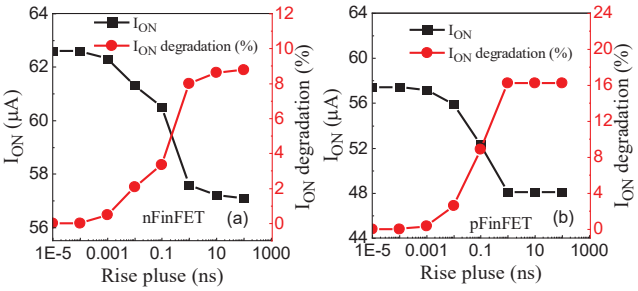

Fig. 9. (a-b) Absolute I_{ON} and I_{ON} degradation of as a function of rise time of gate input pulse for n and p FinFETs.

heat sink. Therefore, the non-linear increment of temperature in a multi-fin device is considered by the BSIM-CMG SHE ASHEXP exponent parameter. The ASHEXP is the NFINtotal exponent parameters in the R_{th} and C_{th} expression given in (1) and (2). The R_{th} decreases exponentially with the increase in fins due to the rise in the substrate area, resulting in more heat dissipation through a wider substrate.

In order to consider the effects of SHE in multi-fin FinFET device, the $ASHEXP$ parameter in the R_{th} expression is taken from the available literature [22]. Fig. 10 (a) shows the nFinFETs I_{ON} degradation and device temperature (ΔT) under the influence of SHE up to 8 fins with $ASHEXP$ values of 0.88. The I_{ON} is degraded up to $\sim$ 12 % and device

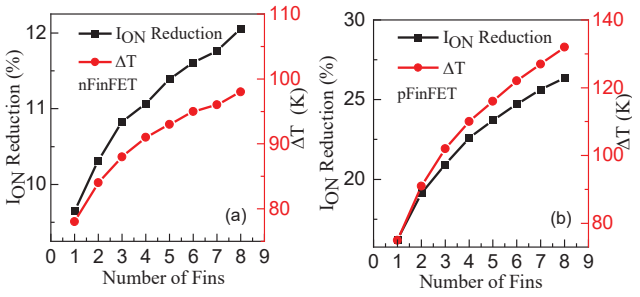

Fig. 10. (a-b) show the I_{ON} degradation and the rise of device temperature with the number of fins from 1 to 8 for n and p FinFETs.

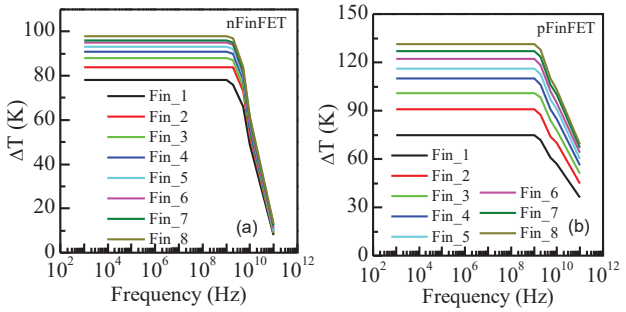

Fig. 11. (a-b) shows the impact of dynamic self-heating on n and p FinFET device temperature for wide range of frequencies.

temperature (ΔT) increases up to $\sim$ 98K for 8 fins.

The results in Fig. 10 (a) is also well consistent with the published reported data [12] [22]. This underscore and verify the accuracy of our multi-fin results. On the other hand, the impact of SHE on pFinFETs is rarely available specially with SiGe material and very few have characterized for multi-fin FinFETs. We have extracted the exponent value $ASHEXP = 0.665$ for pFinFETs from the published experimental data [15]. Fig. 10 (b) shows the I_{ON} degradation and device temperature (ΔT) for pFinFETs using BSIM-CMG model for fins 1 to 8. Its shows up to $\sim$ 26 % degradation in the I_{ON}, which is 2X more than that of nFinFET, and the device temperature (ΔT) increases up to $\sim$ 130K with increase in the number of fins up to 8. The higher degradation and higher temperature rise are due to the low thermal conductivity of SiGe material. However, these exponents are very accurate and important to predict the impacts of SHE for higher fin devices and circuits.

Table II Calibrated SHE parameters for the industry standard compact model of FinFET (BSIM-CMG)

	nFinFET	pFinFET
R_{th} (M.K/W)	1.70357	1.9406
C_{th} (f.J/K)	0.03360	0.0462
Tau (ns)	0.0572	0.08965
f_{th} (GHz)	2.78	1.775

Fig. 11 shows the impact of dynamic SHE on the multi FinFETs (from 1 to 8 fins) device temperature for the wide range of frequencies. The temperature increases with an increase in the number of fins due to high current densities. As showed, the dynamic SHE is more pronounced at a lower frequency and decreases at higher or after isothermal frequency. Further, Fig. 12 shows the impact of current degradation due to dynamic self-heating up to 8 fins for a wide frequencies range. The current degradation is higher below 2 to 3 GHz, and degradation decreases at a higher frequency. This analysis demonstrates the dynamic self-heating has a significant impact on up to $\sim$ 3 GHz and $\sim$ 5 GHz on n and p FinFET devices and becomes worse with more fins.

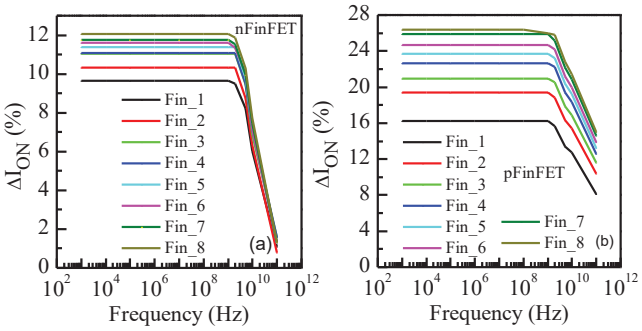

Fig. 12. (a-b) shows the impact of dynamic self-heating on n and p FinFET device I_{ON} degradation for wide range of frequencies.

V. Conclusion and Summary

In this work, we investigated the impact of self-heating effect (SHE) on the main characteristics of both 14nm n and p FinFET devices using fully calibrated 3-D process Technology CAD (TCAD) simulations. Calibrations are done with Intel 14nm FinFET measurement data. The static and dynamic (AC coupled simulation) TCAD simulations have been performed to explore SHE for a wide range of operating frequencies. Our analysis shows that the effect of self-heating on the pFinFET transistors is more severe than nFinFET transistors due to the lower thermal conductivity of newly SiGe material adopted in pFinFETs. The industry standard compact model (BSIM-CMG) has been carefully calibrated to reproduce TCAD simulation data including the Intel 14nm FinFET measurements in order to accurately account for self-heating effects in SPICE circuits. The SHE parameters such as thermal resistance and thermal capacitance values are accurately extracted and reported in this work to enable other researcher to include self-heating effect in their circuit analysis. Finally, the impact of SHE on the multi-fin transistors was also studied showing how the increase in number of fins considerably increases self-heating effect.

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