INDIAN INSTITUTE OF TECHNOLOGY TIRUPATI

Course No: **EE535L**

Name of the Lab: **Digital VLSI Design**

Academic Year/Semester: **2025/B.Tech 5^{th} Sem**

COURSE PROJECT

THE 8x8 SRAM MEMORY DESIGN

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4-Dec-2025

Design of 8×8 SRAM Memory Using 6T SRAM Cell

Objective:

To design, integrate, and simulate an 8×8 SRAM memory array using the 6T SRAM cell along with supporting circuits like the Precharge, Write Circuit, Sense Amplifier and Decoder and to verify its functionality.

Theory:

SRAM stores data using a 6T cell formed by two cross-coupled CMOS inverters and two access transistors that connect the stored nodes to the bitlines when the wordline is enabled. During a write, the bitlines force the cell to the new value, while during a read the precharged bitlines develop a small differential based on the stored data. In an 8×8 array, 64 such cells are arranged in rows and columns. A row decoder selects one wordline, and shared precharge, write driver, and sense amplifier circuits operate on the bitlines to perform read and write operations for the entire memory block.

6T SRAM Cell:

The 6T SRAM cell uses two cross-coupled CMOS inverters to hold the stored bit in a stable latch, while the two access transistors connect the internal nodes to the bitlines when the wordline is activated. During a read operation, the selected cell slightly influences the bitlines without changing its stored state, and during a write operation the bitlines drive the internal nodes to the new value.

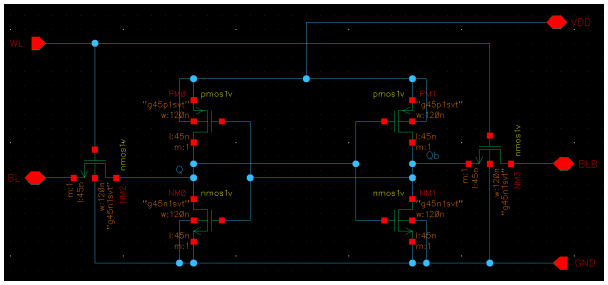

Figure 1: The 6T SRAM Cell

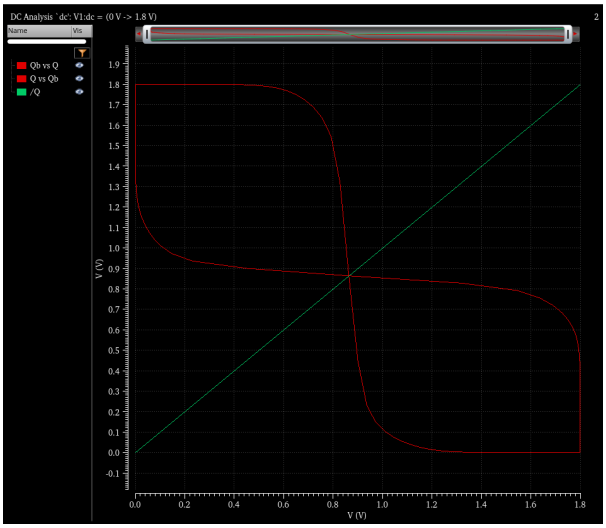

Figure 2: DC Analysis of 6T SRAM

Supporting Circuits:

Precharge Circuit

The precharge circuit pulls both BL and BLB to VDD before a read. This equalizes the bitlines so the minute differential produced during a read can be reliably detected. Correct precharge timing reduces sensing delay and helps avoid read disturb.

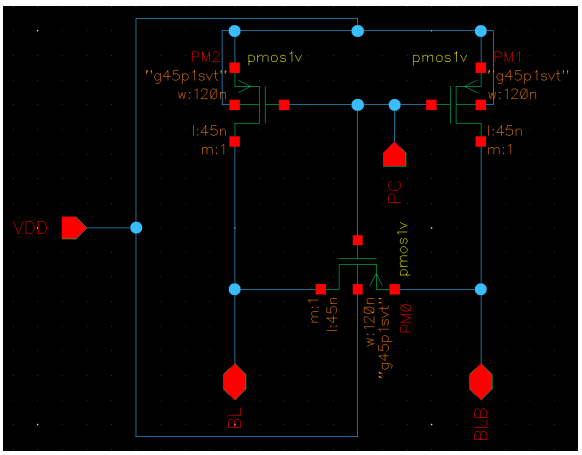

Figure 3: Precharge Circuit

Write Driver

The write driver actively drives complementary values onto BL and BLB during a write cycle. It must temporarily overcome the 6T cell's internal feedback to flip the stored state. Therfore the transistor sizing of the driver is critical for reliable writes and controlled power.

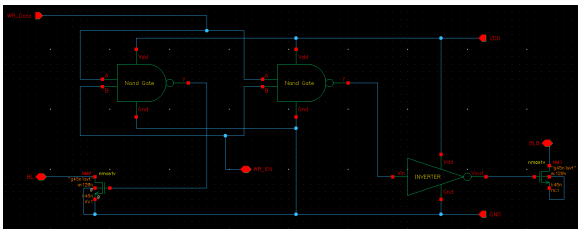

Figure 4: Write Circuit

Sense Amplifier

The latch-type differential sense amplifier senses the small voltage difference between BL and BLB after a read and amplifies it to a full swing logic output. It is enabled only after the differential has developed sufficiently, which avoids read disturb and improves reliability.

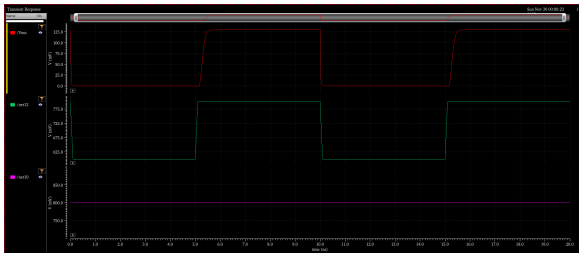

Figure 5: Sense Amplifier Working

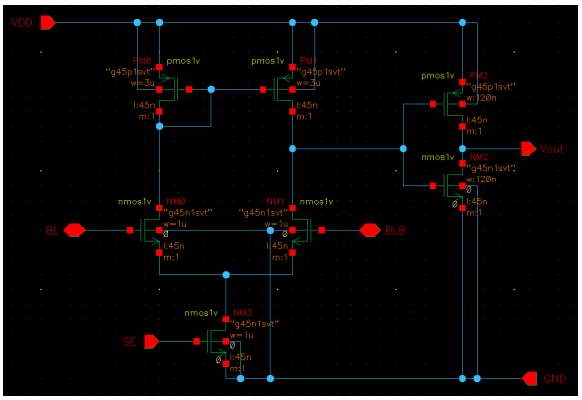

Figure 6: Sense Amplifier Schematic

1-Bit SRAM Integration:

The 1-bit module integrates the 6T storage cell, precharge circuit, write driver and sense amplifier. The control signals used are WL (wordline), PC (precharge), WR_EN (write enable), WR_Data, and SE (sense enable). During a read operation, the bitlines are first precharged, the wordline is activated, a small differential develops on BL and BLB, and the sense amplifier then resolves it. During a write operation, the bitlines are prepared if needed, the wordline is enabled, and the write driver forces the required data onto BL and BLB.

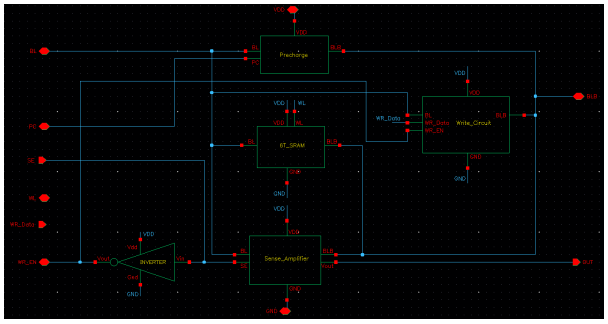

Figure 7: 1-Bit SRAM Schematic

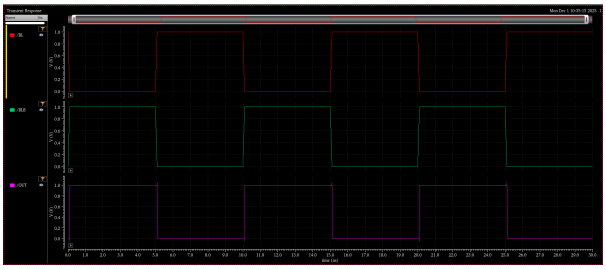

Figure 8: 1-Bit SRAM Working (Read Operation)

Decoder Hierarchy

A 3×8 decoder was implemented using two 2×4 decoder blocks with enable gating. Each 2×4 block uses simple gate level logic to generate the outputs.

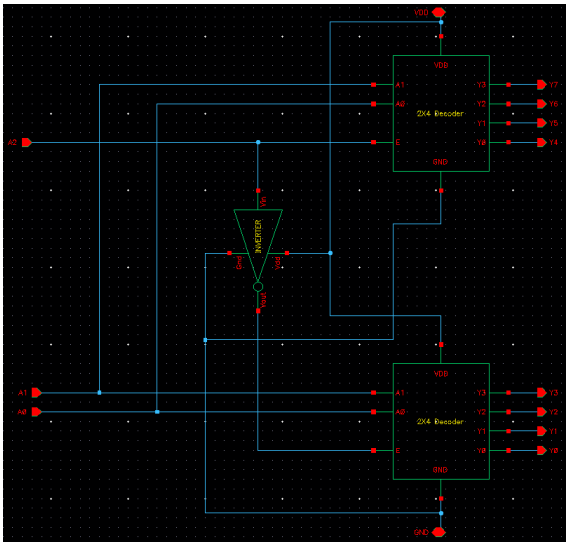

Figure 9: 3x8 Decoder Block

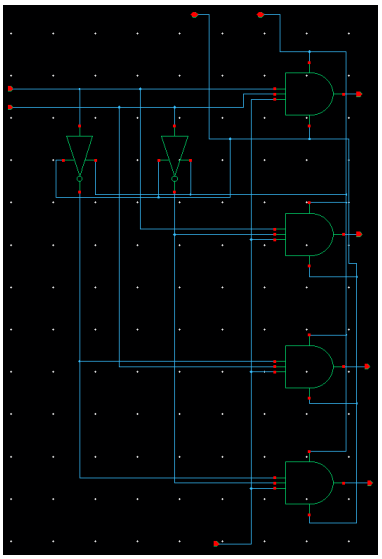

Figure 10: 2x4 Decoder Block (Used in the 3x8 Decoder)

The 8×8 SRAM Array Architecture:

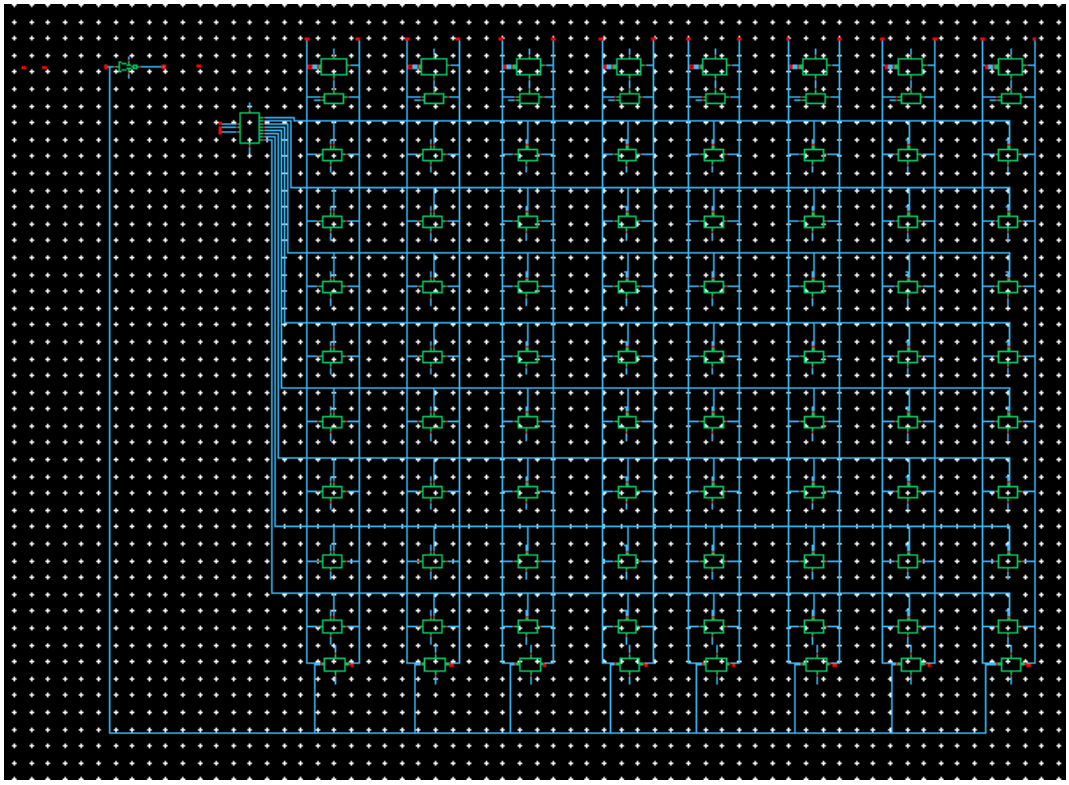

Figure 11: 8×8 SRAM Memory Array Schematic

- The 8×8 SRAM array contains 64 identical 6T cells arranged in eight rows and eight columns. Each row is enabled by a dedicated wordline, while each column has its own BL and BLB. Row selection is performed by a 3-to-8 decoder ensuring that only one wordline is activated during any read or write operation.
- Each column contains a single precharge circuit, write driver, and sense amplifier that serve all eight cells in that column. Before a read, the precharge circuit equalises BL and BLB to VDD. When a wordline is asserted, only the selected cell couples to the bitlines, producing a small voltage difference that the column's sense amplifier converts into a full-swing output.
- For write operations, the column write driver forces BL and BLB to the required logic levels while the selected wordline is active. This allows the chosen cell to switch to the new state, while all unselected cells remain disconnected and unaffected.
- This organisation of multiple cells per column with one set of support circuits per column keeps the layout structured and compact and enables reliable read and write access across the full array.

Results:

- The 6T SRAM cell exhibits stable bistable operation with a clear static noise margin, as confirmed from the DC Analysis.
- The 1-bit SRAM block, which integrates the 6T SRAM cell with its corresponding precharge, write driver and sense amplifier circuits, demonstrates correct read and write functionality.
- Column level support circuits operate correctly. Each column's precharge circuit equalises BL and BLB before a read, the write driver successfully forces new data onto the bitlines, and the sense amplifier produces a clean digital output once a difference between BL and BLB develops.
- The 3-to-8 decoder activates the correct wordline without the unintended switching of other neighbouring rows, validating proper row selection for the 8×8 array.
- The complete 8×8 array schematic combines all 64 cells with their column wise precharge, write and sensing circuits, along with the row decoder and wordline routing. The integrated structure shows that the array can correctly select rows and give reliable overall read and write functionalityl.

Inference and Learnings:

- Gained a clear understanding of the operation of the 6T SRAM cell, including how the cross-coupled inverter structure stores data and how access transistors influence read and write behaviour.
- Understood how read and write margins relate to transistor sizing and why stable operation depends on maintaining proper cell ratios.
- Learned the importance of precharge timing and correct enabling of the sense amplifier for reliable bitline sensing during read operations.
- Observed how the write driver interacts with the cell to override its stored value and how the wordline controls access to each row.
- Practised implementing a hierarchical decoder (3×8 using 2×4 blocks) and integrating it with the memory array for proper row selection.
- Gained experience in combining the cell, supporting circuits, and decoder into a complete 8×8 SRAM architecture and understanding its overall functional behaviour.