Component Choices for the MMR projet

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Contents

1 Objectives

As a general rule, the components that are more widely available are prefered to the ones that are more difficult to get so it augments the chances that they are still available in the future. It also help keep the price down. There is no fixed budget for the total price of a device but the objectif is to stay less of 200$ inluding PCB, box, and components.

1.1 Sensor

- Measure magnetic field with resolution <100 pT in the 0–500 Hz band (per axis).
- Support set/reset and offset-strap operations to null the ambient field before acquisitions.
- Tolerate Earth's field and local disturbances without saturating during setup.
- Provide a 3-axis measurement.

1.2 Digitizer (ADC)

- 24-bit delta-sigma ADC with ≥ 110 dB dynamic range at the target data rate.
- Sampling: nominal 1 kHz; synchronized across 3 axes.
- Inlcude a PGA (Programmable Gain Array) per channel.

1.3 Signal conditioning

- Provide gain that is fixed to have the best dynamic range possible in the ADC.
- Input-referred noise below sensor noise (targets: ≤ 4 nV$/\sqrt{\text{Hz}}$ above a few Hz; ≤ 30 nV$/\sqrt{\text{Hz}}$ at 1 Hz).
- Provide bias to ADC common-mode (VCM) and preserve a true-differential path.
- Analog anti-aliasing tailored to 1 kHz sampling.

1.4 Processing and communication

- On-board processing for logging, health/status, and pre-checks (set/reset and offset routine).
- USB for bulk data offload and device management.
- Bluetooth Low Energy (BLE) for configuration and status in the field.
- Data format with block-level timestamps (avoid per-sample timestamps to reduce size).

1.5 Time synchronization

- Common timebase across devices using a GPS reference.

1.6 Spatial positioning

- 6-axis IMU (Inertial Measurement Unit) (3-axis accelerometer + 3-axis gyroscope) for orientation and tilt compensation.
- Heading from fusion of IMU and magnetometer.

- Optional GPS for added positioning reference.

1.7   Power management

- Operate from a 12 V battery; generate required rails digital and analog rails.

- Limit conducted/radiated EMI into the sensor band.

- Limit power consumption.

2   Decision

2.1   Sensor

We select the **HMC1001** for the z axis and the **HMC1002** for the x–y axes for their low cost and integrated bridge design. Each sensor produces a bipolar differential output that follows:

$$\begin{align}
V_{\text{out}} &\equiv V_{out+} - V_{out-} \tag{1}\\
&= s\, V_b\, B \tag{2}\\
&= (3.2\,\text{mV}/(\text{V G}) \times 9\,\text{V})\, B \tag{3}\\
&= 28.8\,\text{mV}/\text{G} \cdot B \tag{4}
\end{align}$$

Here s is the sensitivity, V_b the bridge supply, and B the field on the axis in Gauss.

We set $V_b = 9\,\text{V}$ to keep regulator headroom with a 3S Li-ion pack (nominal 11.1 V, sagging to about 9.5 V near end of discharge). The bridge limit is 12 V; if the source stays $\geq 12\,\text{V}$, V_b may be raised (e.g., to 10 V) for extra amplitude.

Newer series (HMC1021/1022, HMC1051/1052) were considered but do not match the targeted low noise in our band; HMC1001/1002 are a better fit.

Set/reset pulses

To obtain repeatable sensitivity and minimize hysteresis, each axis must receive a *set* and a *reset* pulse before acquisition. Each axis includes its own set/reset strap; in our design the three straps are wired in series and energized together. The driver delivers 3 A to 4 A for approximately 2 µs per pulse, as illustrated in Fig. 1.

The topology of Honeywell's Fig. 4 is retained; only package-level substitutions were made, leaving the function unchanged:

- Q1 = `D882 SOT-89` (was 2N2222)

- Q3 = `D882 SOT-89` (was 2N2222)

- Q2 = `B772 SOT-89` (was 2N2907)

- X1/X2 = `DMC3028LSD` (dual complementary MOSFET)

The pulse supply is set to 18 V because the three straps are in series. The minimum total resistance is $3 \times 1.8\,\Omega = 5.4\,\Omega$, giving an initial current

$$I_0 = \frac{18\,\text{V}}{5.4\,\Omega} \approx 3.33\,\text{A}.$$

Two MCU lines (`Vset`, `Vreset`) are used to enforce non-overlap: `Vreset` turns X2 off before `Vset` drives X1 on, and X1 is turned off before X2 is enabled.
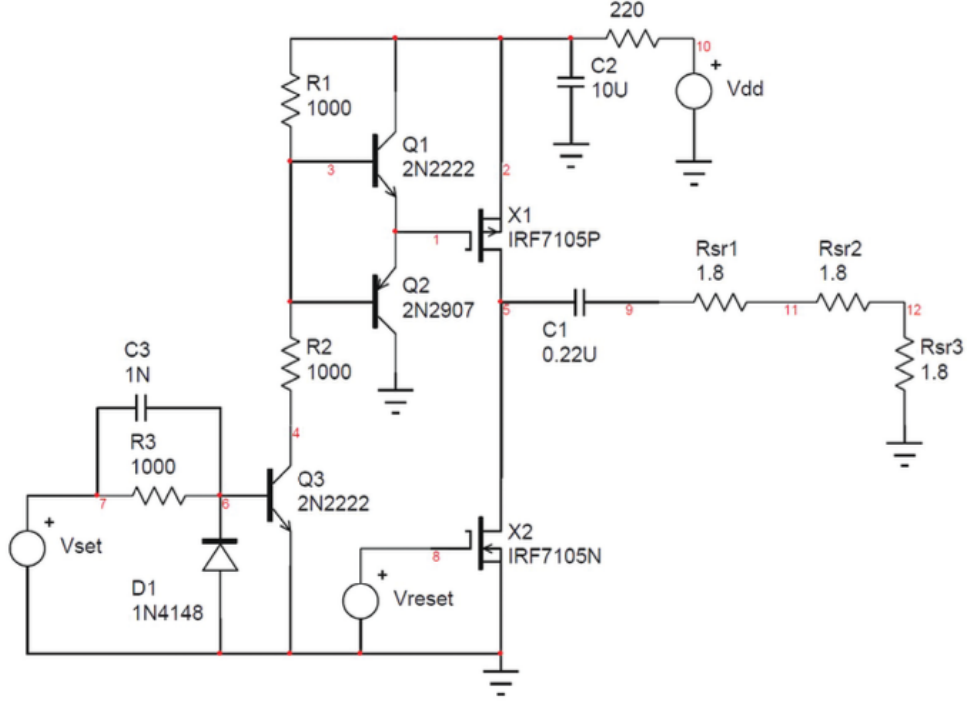

Figure 1: Set/reset pulse driver (adapted from the HMC100x/HMC102x datasheet, Fig. 4, p. 11).

Offset

Each sensor has another strap used to apply an offset on each axis. The following steps are planned to take place before each acquisition, after the set and reset activation for all three axes:

1. Reduce the gain to the smallest available value.

2. Measure the static magnetic field.

3. Use the DAC to send a current through the offset strap to compensate for it.

4. Measure the resulting static field and repeat until zero is reached.

5. Increase the gain and repeat.

It could also be done with dynamic feedback, but this would require more complex programming to ensure that the system remains stable.

To generate a signal, it is necessary to use the known value of the ambient field and to send a signal that is proportional to the offset strap current. The MCP4728 has been chosen for this signal generation. It has a 12-bit resolution and can output from 0 to $4.096\,\mathrm{V}$ in steps of $1\,\mathrm{mV}$. The circuit is shown in Figure 2. This circuit follows the equation:

$$I_{LOAD} = \frac{R_2/R_1}{R_S}(V_p - V_n) \tag{5}$$

Where

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- V_p = DAC Ch. A (command)

- V_n = DAC Ch. D (midscale reference)

- R_S = sense resistor in series with the offset strap

- The resistor values R have been chosen as $10\,\text{k}\Omega$.

With $R_1 = R_2 = R_3 = R_4 = 10\,\text{k}\Omega$ and $R_S = 20\,\Omega$, we obtain the following relation:

$$I_{\text{LOAD}} = 0.05(V_p - 2.048) \tag{6}$$

If the voltage from DAC channel A is at its maximum value of $4.096\,\text{V}$, the current through the strap will be $102.4\,\text{mA}$. Simulations in LTspice confirm that this value is accurate. The current resolution for one bit of the DAC is:

$$I_{LOAD} = 0.05(2.049 - 2.048) = 0.05\,\text{mA} \tag{7}$$

According to the sensor datasheet, the response of the offset field compensation is specified as $47.5\,\text{mA/G} = 475\,\text{mA/mT}$, so the maximum correction is:

$$\frac{102.4\,\text{mA}}{475\,\text{mA/mT}} = 0.216\,\text{mT} = 216\,\mu\text{T} \tag{8}$$

And the smallest increment is:

$$\frac{0.05\,\text{mA}}{475\,\text{mA/mT}} = 0.105\,\mu\text{T} = 105\,\text{nT} \tag{9}$$

As shown in Fig. 2, the op-amp characteristics are not strict because of the added BJT buffer stage. The op-amp chosen is the LM324DT, as it integrates four op-amp circuits into a single package and is widely available. The BJTs used for the buffer are the D882 (NPN) and B772 (PNP). They were selected because their SOT-89 package provides sufficient thermal dissipation, up to approximately $500\,\text{mW}$.

Figure 2 shows only one channel; each sensor axis has its own offset circuit, each using a dedicated channel of the DAC.

2.2   Digitizer (ADC)

The AD7779 was chosen for its 24-bit resolution, eight fully differential channels, $16\,\text{kS/s}$ acquisition rate, and integrated PGA. Within the same ADC family, the AD7771 offers up to $128\,\text{kS/s}$, making it an easy upgrade option in future designs if higher-speed sensors need to be added.

Considering the 24-bit resolution, a reference voltage of $2.5\,\text{V}$, and a PGA gain of 8, we obtain:

$$LSB = \frac{2V_{\text{REF}}/\text{PGA}_{\text{gain}}}{2^{24}} = 37.3\,\text{nV} \tag{10}$$

To estimate the noise-limited RMS signal, considering a sampling rate of $1\,\text{kHz}$, the datasheet specifies an effective resolution (ER) of 20.66. Therefore,

$$V_{\text{noise,rms}} = \frac{V_{\text{REF}}}{\text{PGA}_{\text{gain}} \cdot 2^{ER}} = 0.377\,\mu\text{V}_{\text{rms}} \tag{11}$$

Each input channel of this ADC must operate between $0.1\,\text{V}$ and $3.2\,\text{V}$, with a common-mode input voltage of $1.65\,\text{V}$.

This ADC includes an internal $2.5\,\text{V}$ reference, which can be replaced by an external precision reference if higher accuracy is required.
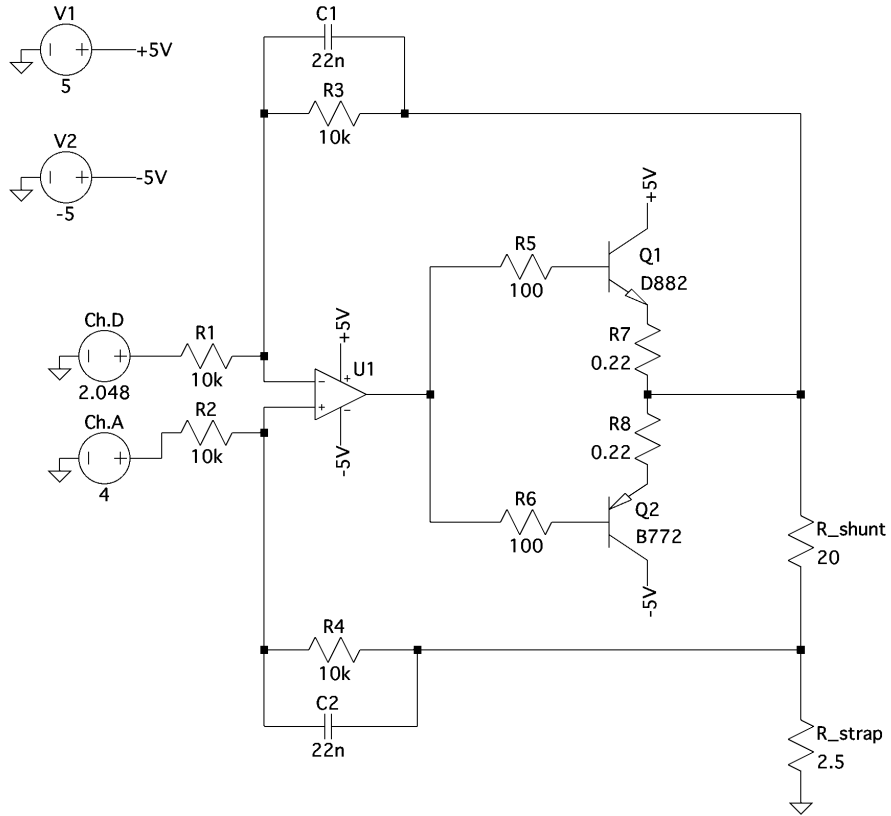
Figure 2: Circuit used to generate the offset current. This circuit was drawn in Spice and simulated to verify its accuracy. Capacitors C1 and C2 form a low-pass filter, and their values can be increased if necessary. Resistors R5, R6, R7, and R8 are used to stabilize the circuit.

2.3 Signal conditioning

Gain

The differential signal from the sensors must be amplified before reaching the ADC. According to the sensor datasheet, the minimum noise floor is $e_s = 3.8\,\text{nV}/\sqrt{\text{Hz}}$. If we integrate this noise over our bandwidth (BW):

$$v_{s,\text{rms}} = e_s\sqrt{BW} = 3.8 \times \sqrt{500} = 86\,\text{nV}_{\text{rms}} \tag{12}$$

If a pre-ADC gain of 16 is applied, the noise ratio becomes:

$$\frac{86\,\text{nV}_{\text{rms}} \times 16}{0.377\,\text{µV}_{\text{rms}}} = 3.65 \tag{13}$$

To ensure that the ADC noise can be neglected, a pre-ADC gain of 125 could be used, which yields a noise ratio of 28.5. Table 1 presents the different PGA gain values along with the corresponding maximum measurable field and expected noise levels.

Table 1: AD7779 @ 1 kSPS, fixed pre-ADC gain 124.2x adjusted to the real gain du to resistor value limitation. Very little changed.

	PGA = 1	PGA = 2	PGA = 4	PGA = 8
ER [bits]	21.84	21.69	21.28	20.66
RTI noise [µV$_{\text{rms}}$]	1.332	0.739	0.491	0.377
FS [V$_{\text{pp}}$]	5.000	2.500	1.250	0.625
LSB at ADC [nV]	298.023	149.012	74.506	37.253
Resolution [pT/LSB]	8.332	4.166	2.083	1.041
Headroom [µT$_{\text{peak}}$]	69.892	34.946	17.473	8.736

To perform the pre-ADC amplification, the INA851 was chosen for its fully differential input and output. It also allows the easy addition of the 1.65 V bias required by the ADC. This bias voltage can be sourced directly from the ADC's V_{COM} pin, although this must be tested. Otherwise, a simple rail splitter such as the TLE2426 can be used with the anaolg +3.3VA.

The gain of the INA851 is given by the following equation (see page 23 of the INA851 datasheet):

$$G = \left(1 + \frac{6\,\text{k}\Omega}{R_G}\right) \tag{14}$$

and thus,

$$R_G = \frac{6\,\text{k}\Omega}{(G-1)} \tag{15}$$

Since we require a gain of 125, the resistor value R_G must be set to 48.39 Ω. As this exact value is not readily available, the closest standard value is 48.7 Ω. This approximation yields a gain of 124.2. Table 1 shows a recalculation of Table 1 with the pre-ADC gain fixed at 124.2.

Given that the INA should never output a signal greater than 3.2 V, the supply voltage is set to +4.5V and -5V (+4.5V and not +5V to simplify design). These values could be slightly increased to ensure output stability; however, the quiescent current scales with the supply voltage, so keeping it low is preferable to minimize power consumption.
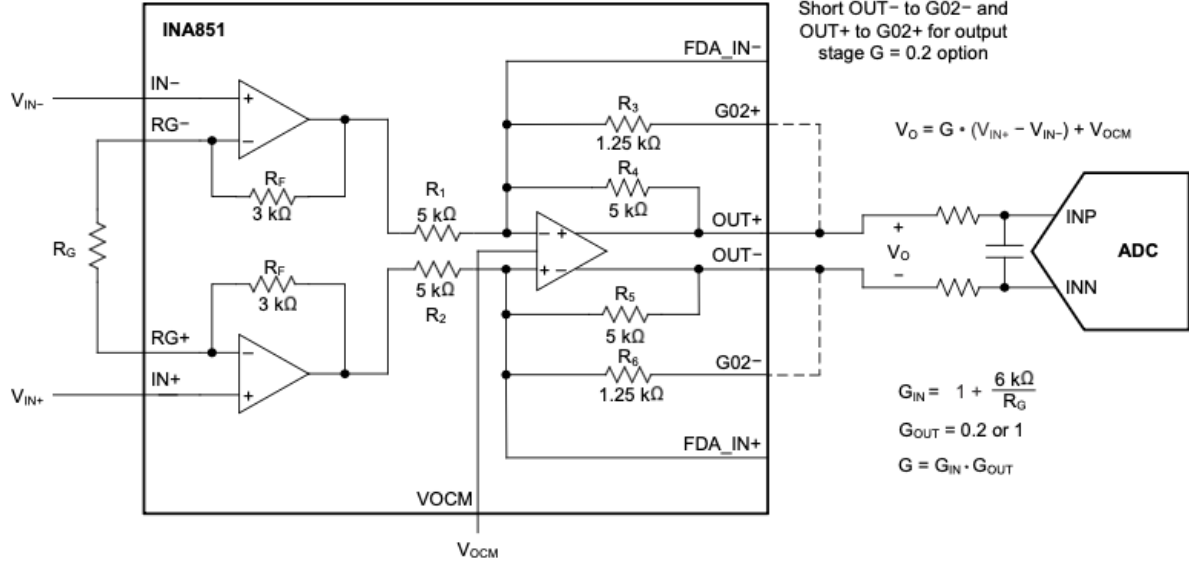
Figure 3: INA851 circuit with AAF (taken from the INA851 datasheet, Fig. 8-2, p. 23). $R_G = 48.7$ Ohm, V_{OCM} is expected to be 1.65V for the ADC bias.

Antialiasing Filter

With a sampling rate of 1 kHz, it is necessary to use an AAF with a minimum cutoff frequency of 500 Hz. However, to reduce more the higher frequencies and to use commonly available componnets the filter should have R=1 kΩ and the capacitor should have C=220 nF.

Each sensor axis has its own INA851 and corresponding AAF.

2.4 Time Synchronization and spacial reference

Time reference

To get accurate time reference, it is required to use GNSS (Global Navigation Satellite System). This signal can be capted by an module or an external antenna. For the first version of this system, the DAN-F10N module has been selected because it can also use the L5 band in addition to the L1 band. This could potentially lead to better reception in dense forest. This module include an antenna but needs a 70x70mm ground plane under the module.

Spatial positioning

The GNSS module is also able to provide coordinates. Those coordinates can be use to calculate the expected local earth magnetic field. With this value calculated, it is possible to a good estimate of the signal needed to compensate the sensors. With a measurement of magnetic field from the device it is possible to etablish the north direction.
In addition to those informations, a Inertial Measurement Unit (IMU) can be added to provide tilt so the device can put on the ground whitout great care of positioning. The IMU ISM330DHCX is chosen for its widely availability Many other IMU would work too since the requirements are not difficult.

2.5 Processing and communication

Micro-Processor

The module ESP32-S3-WROOM-1-N16R8 is chosen for the on board micro-processor. It has a PCB antenna included for Bluetooth. This module also has 16MB of Flash and 8MB of PSRAM. Is it very easy to source this module, and there is many different version with differnt combinaison of Flash and PSRAM.

Table 2 compile all the protocol and GPIO used in this projet.

Table 2: Interfaces planned on the ESP32-S3-WROOM-1-N16R8 and required GPIOs

Protocol	Used with	# GPIO
USB Device	PC link	2
I^2C	IMU	2
I^2C	DAC	2
SPI	ADC parameters	4
I^2S	ADC data out	3
SD/MMC (4-bit)	SDcard	6
UART	GNSS receiver	2
PPS line	GNSS timing pulse	1
Octal SPI	On module PSRAM	11
Quad SPI	On module Flash	6
Enable wire	EN LT3042	1
Enable wire	EN TPS61170	1
Set/Reset driver	HMC1001/2	2

2.6 Power management

During operation, the power is expected to come from a battery. The same USB port used for data transmission can be used as the main battery power input. The USB-2.0 protocol before handshake can give up to 100mA and the USB-3.0 up to 150mA at +5V. After doing a configuration with the host PC, it can go up to 500mA for USB-2.0 and 900mA for USB-3.0. Since the device needs more current than what is available before communication, a protocol is implemented using the MCU to perform the USB handshake that lets the device access more current. However, it is important to always keep the input voltage at +5V. This is only important for communication with a computer. When using the device with a USB power bank, there is no protocol needed to access the current available.

An additional board is planned to be made to take voltage from a battery and bring it down to the +5V main. This is to accommodate a passive use of the device with solar power.

Figure 4 gives a visual representation of all the regulators used in this project. The choices for all the different regulators will be explained in their respective subsections.

The table 3 is a compilation of the expected power requirement for each different voltage line.

A $150\,\mu F$ polymer capacitor is added on the battery input as a bulk decoupling capacitor to reduce line impedance and smooth load transients. To limit inrush and fault currents and to protect against incorrect input voltages or output shorts, a TPS25200 $5\,V$ eFuse is placed in series with the $5\,V$ rail.

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This device integrates a programmable current limit and an overvoltage clamp that holds the output near 5.4 V and disconnects the load if the input exceeds about 7.6 V. In addition, a low-capacitance TVS/ESD diode array (SRV05-4) is placed as close as possible to the USB/power connector to protect the input against ESD strikes and fast surge transients.
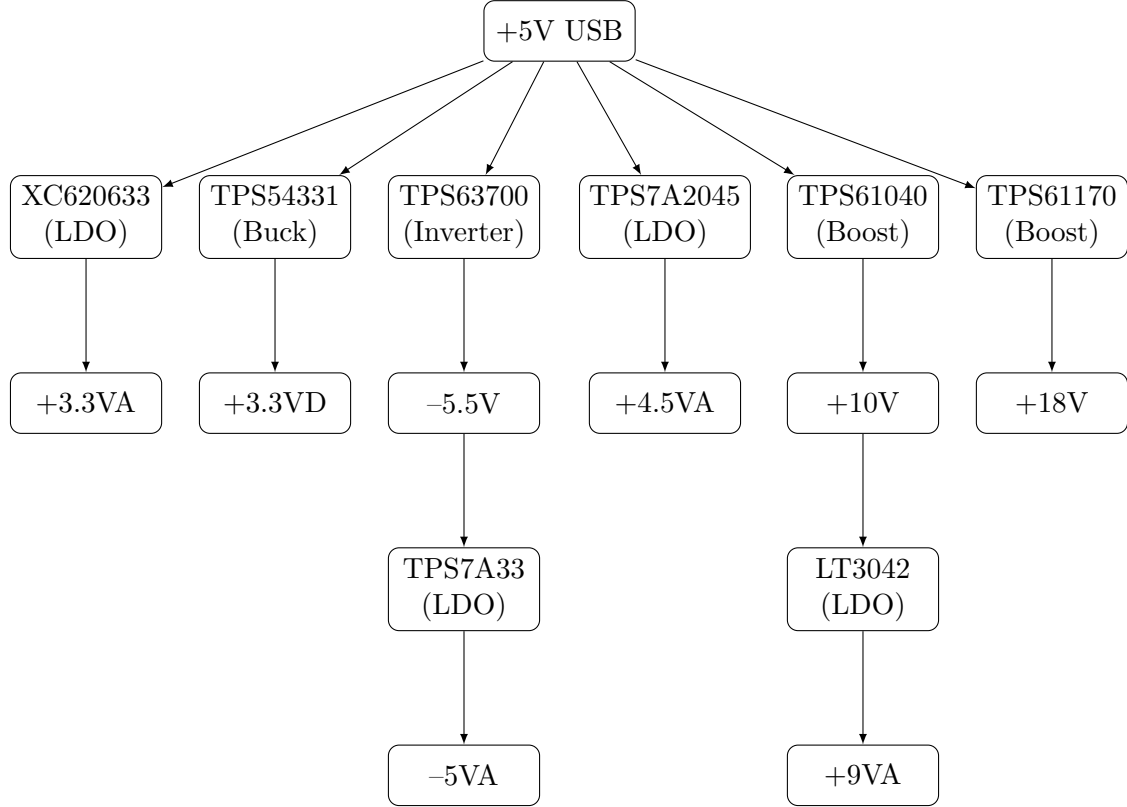
```
                              +5V USB

  XC620633    TPS54331    TPS63700    TPS7A2045   TPS61040    TPS61170
   (LDO)       (Buck)    (Inverter)     (LDO)      (Boost)     (Boost)

  +3.3VA      +3.3VD       -5.5V       +4.5VA       +10V         +18V

                         TPS7A33                  LT3042
                          (LDO)                    (LDO)

                          -5VA                     +9VA
```

Figure 4: Power tree for all the different rail used. Optimized for noise, power efficiency, EMI radiation and low BOM

+9V Sensor Bridge Voltage

To obtain the lowest noise level possible, it is required to first step up the voltage from +5V to above the target +9V, then reduce it with a specialized low-noise LDO. The target voltage before the LDO is set at +10V to minimize losses while keeping enough headroom to guarantee a high PSRR value. To do this, the TPS61040 is selected for being a promotional extended part at JLCPCB, which means low price and easy availability; besides this, there is no need for any specialized component. Then, the LT3042 is selected to bring this voltage down to the desired +9V. This LDO has the advantage of ultra-high PSRR, low spot noise, and low RMS noise.

While doing data transfer, or when not needed, this branch can be turned off using a GPIO of the MCU with the TPS61040. A pull-down resistor is added to keep this off until +3.3V is sent to the EN pin.

Considering normal operation with three bridge resistances of 850Ω giving an equivalent of 283.33Ω, this results in 32.1 mA and 292 mW in total. With an efficiency of 87%, the TPS61040 will require 73.8 mA at the +5V input.

Table 3: Estimated current and power budget by rail.

Rail	Part	Current peak (mA)	Power peak (mW)	Power average (mW)
+3.3 V	ESP32-S3-WROOM-1	100	330	70
	DAN-F10N	19	63	63
	microSD (writes)	45	150	5
	AD7779	15	49	33
	MCP4728	1	3	2
	ISM330DHCX	5	16	16
	TPS62912 (I_Q)	1	3	2
	Misc. (LEDs, logic)	5	16	3
	Subtotal	191	617	**194**
+5 V	INA851 (3 ch, $+V_s$)	10.8	54	54
	Offset strap drivers	300	1500	89 (1)
	Subtotal	310.8	1554	**143**
-5 V	INA851 (3 ch, $-V_s$)	10.8	54	54
	Offset strap drivers	300	1500	89 (1)
	Subtotal	310.8	1554	**143**
+9 V	HMC1001	15	135	97
	HMC1002	30	270	195
	Subtotal	45	405	**292**
Total				**772 mW**

Notes: (1) The average magnetic field is expected to be $50\,000\,$nT, so with an offset constant of $47.5\,$mA/G, if we average all possible field, we get $35.6\,$mA of total average offset current, then we suppose that in average the B-field would be split positive and negative.

Table 4: +9VA rail: TPS61040 pre-regulator and LT3042 LDO components. ($5\,\mathrm{V}$ in $\rightarrow$ $10\,\mathrm{V}$ $\rightarrow$ $9\,\mathrm{V}$ out)

Stage	Reference	Value	Notes
TPS61040	L1	$10\,\mathrm{\mu H}$	$\geq 0.6\,\mathrm{A}$ I sat
	D1	Schottky, $30\,\mathrm{V}$, $0.5\,\mathrm{A}$	e.g. MBR0530 or equivalent
	R_{FB1}	$715\,\mathrm{k\Omega}$	$V_{OUT} = 1.233 \cdot \left(1 + \frac{R1}{R2}\right)$
	R_{FB2}	$100\,\mathrm{k\Omega}$	$\pm 1\,\%$
	C_{FF}	$22\,\mathrm{pF}$	
	C_{IN}	$10\,\mathrm{\mu F} \geq 10\,\mathrm{V}$	
	$C_{\mathrm{IN,HF}}$	$100\,\mathrm{nF} \geq 10\,\mathrm{V}$	
	C_{OUT}	$10\,\mathrm{\mu F} \geq 25\,\mathrm{V}$	
	$C_{\mathrm{OUT,HF}}$	$100\,\mathrm{nF} \geq 25\,\mathrm{V}$	
	R_{EN2}	$100\,\mathrm{k\Omega}$	EN pull-down (MCU control)
LT3042	R_{SET}	$90.9\,\mathrm{k\Omega}$	$V_{OUT} = 100\,\mathrm{\mu A} \cdot R_{\mathrm{SET}}$
	R_{IOUT}	$2\,\mathrm{k\Omega}$	$I_{\mathrm{OUT,max}}(\mathrm{mA}) = \frac{125(\mathrm{mA}) \cdot \mathrm{k\Omega}}{R_{\mathrm{IOUT}}}$
	C_{SET}	$4.7\,\mathrm{\mu F}$	
	C_{OUT}	$4.7\,\mathrm{\mu F}$	
	C_{IN}	$10\,\mathrm{\mu F} \geq 25\,\mathrm{V}$	
	$C_{\mathrm{IN,HF}}$	$100\,\mathrm{nF} \geq 25\,\mathrm{V}$	

+3.3V Digital

For the +3.3VD, the TPS54331 is chosen for its very widely availability and being a prefered exanded part in JLCPCB. It is able to do up to 3A from 3.5V to 28V input. It also has a great efficiency at around 94%. The table 5 below give the component values for this circuit. This regulator is always on during normal operation.
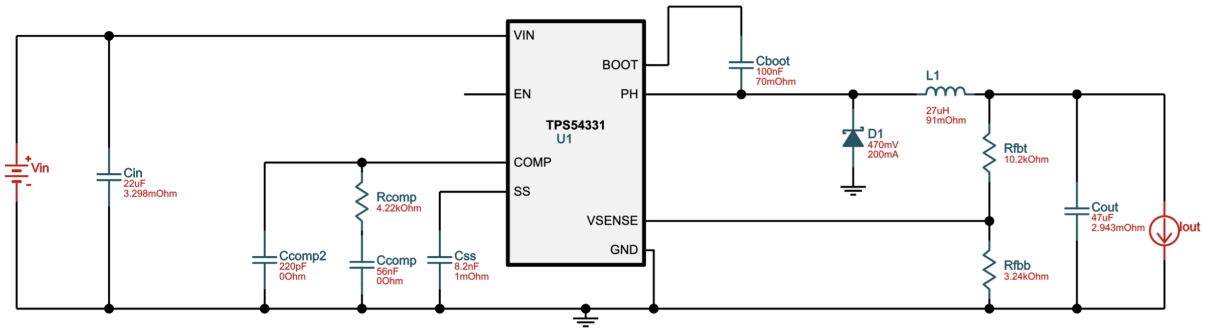

Figure 5: Circuit of TPS54331 generated with WEBENCH online tool from TI. The parts are condensend in table 5

Table 5: TPS54331 +3.3 V_D rail (5 V in $\rightarrow$ 3.3 V out, $I_{out,max} = 0.3$ A, WEBENCH values)

Ref.	Value	Notes
U1	TPS54331	Buck converter, 3 A, 570 kHz
L1	27 µH	$I_{DC} = 1.3$ A, $R_{DC} = 91$ mΩ
D1	Schottky diode	$V_{RRM} = 20$ V, $I_O = 200$ mA
Cin	22 µF, 16 V	Input bulk capacitor, derated to 16 µF
Cout	47 µF, 6.3 V	Output bulk capacitor, derated to 12 µF
Cboot	100 nF, 10 V	Bootstrap capacitor (BOOT–PH)
Css	8.2 nF, 10 V	Soft–start capacitor
Ccomp	56 nF, 50 V	Compensation capacitor (with R_{COMP})
Ccomp2	220 pF, 50 V	HF pole capacitor in compensation network
Rfbt	10.2 kΩ, 1%	Upper feedback resistor
Rfbb	3.24 kΩ, 1%	Lower feedback resistor, sets $V_{OUT} \approx 3.3$ V
Rcomp	4.22 kΩ, 1%	Error amplifier compensation resistor

+3.3V Analog

To reduce the noise level in the ADC, a separate low-noise power line is required. This line needs much lower current and lower noise than the +3.3VD. To generate this voltage, the XC620633 is chosen. It is a fixed 3.3V LDO with a decent noise level.

Table 6: XC620633 +3.3VA rail components (5 V in $\rightarrow$ 3.3 V out)

Reference	Value / Part
C_{IN1}	4.7 µF, 10 V
C_{IN2}	100 nF, 10 V
C_{OUT1}	4.7 µF, 6.3 V
C_{OUT2}	100 nF, 6.3 V
C_{BULK}	10 µF, 10 V

+4.5V Analog

To get the voltage needed for the INA851 its posisive buffer, a +4.5VA is derived from the +5V of the USB main supply. The TPS7A2045 is used, this component is a fixed 4.5V LDO witch simplify the cicruit while have good noise level. The following table 7 gives the passive capacitor values to stabilize the circuit.

Table 7: TPS7A2045 +4.5VA rail passive components (5 V in $\rightarrow$ 4.5 V out)

Ref.	Value / Part
C_{IN1}	4.7 µF, 10 V
C_{IN2}	0.1 µF, 10 V
C_{OUT1}	4.7 µF, 6.3 V
C_{OUT2}	0.1 µF, 6.3 V

-5V Analog

To supply the INA851 and the other analog stages with a negative rail, a -5VA is derived from the +5V USB main supply. First, the TPS63700 is used as an inverting DC/DC converter to generate an intermediate voltage of approximately -5.5V. This voltage is then regulated by the low-noise TPS7A33 LDO down to -5V, improving both line rejection and noise performance. The following table 8 summarizes the passive component values used in this design.

Table 8: -5VA rail: TPS63700 inverting pre-regulator and TPS7A33 LDO components. (5 V in $\rightarrow$ -5.5 V $\rightarrow$ -5 V out)

Stage	Reference	Value	Notes
TPS63700	L1	$10\,\mu H$	$\geq 0.6\,A$ I_{sat}, low DCR
	D1	Schottky, 20 V, 1 A	e.g. SS14 or equivalent
	R_{FB1}	$340\,k\Omega$	Sets $V_{OUT} \approx -5.5\,V$
	R_{FB2}	$100\,k\Omega$	$V_{OUT} = -1.25 \cdot \left(1 + \frac{R_{FB1}}{R_{FB2}}\right)$
	C_{FF}	$22\,pF$	Feed-forward for loop stability
	C_{IN}	$10\,\mu F \geq 10\,V$	Input bulk capacitor
	$C_{IN,HF}$	$100\,nF \geq 10\,V$	Input high-frequency bypass
	C_{OUT}	$10\,\mu F \geq 10\,V$	Output bulk capacitor (inverting node)
	$C_{OUT,HF}$	$100\,nF \geq 10\,V$	Output high-frequency bypass
	R_{EN}	$100\,k\Omega$	EN pull-down (MCU control on EN pin)
TPS7A33	C_{IN}	$10\,\mu F \geq 10\,V$	Close to VIN pin, low ESR
	$C_{IN,HF}$	$100\,nF \geq 10\,V$	HF bypass near VIN/GND
	C_{OUT}	$10\,\mu F \geq 10\,V$	Output capacitor for stability
	$C_{OUT,HF}$	$100\,nF \geq 10\,V$	HF bypass at VOUT/GND
	C_{NR}	$10\,nF$	Noise-reduction cap on NR pin (if used)

+18V Set/Reset

To generate the +18V rail, the TPS61288 is chosen. The requirements are not very strict, any source of +18V would be able to supply because even if the peak current is very high, about 3.33A, it is only for $2\,\mu s$ so the energy is very low. The table 9 shows the chosen values for in the schematic of figure 6.
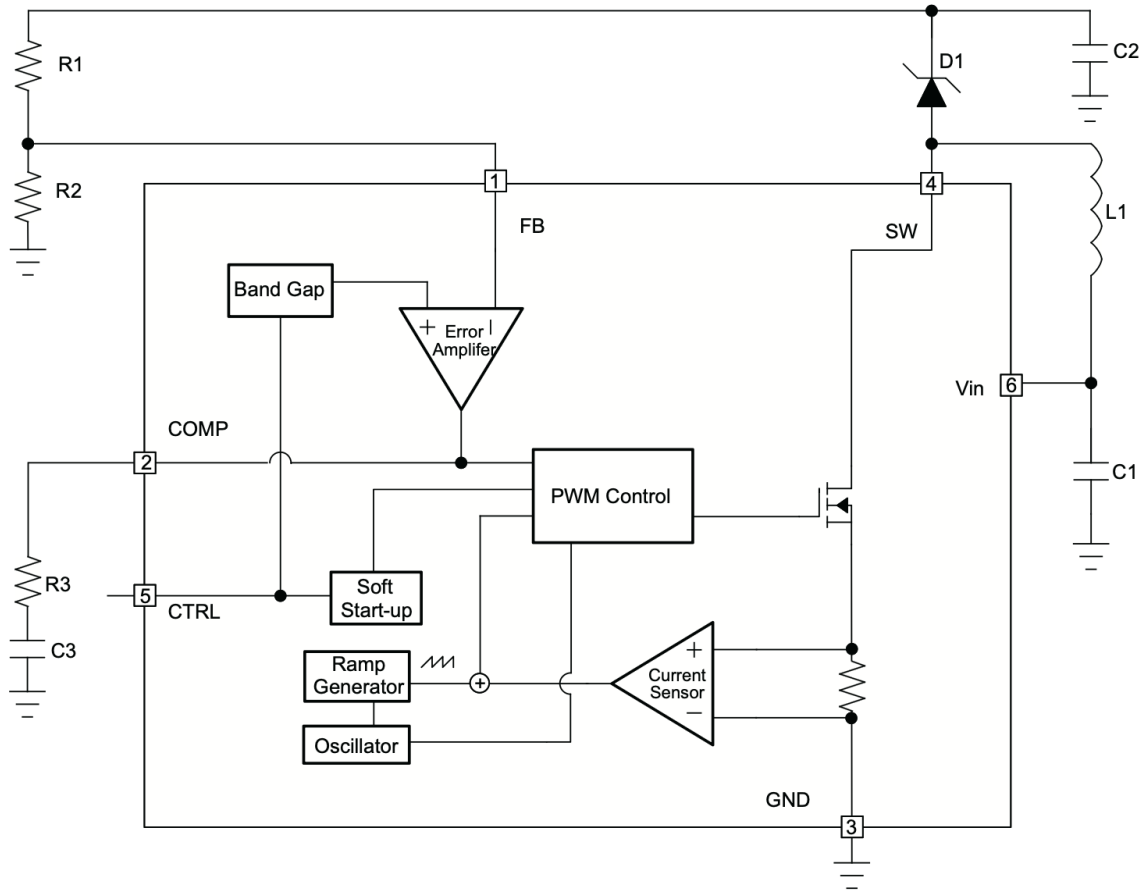
Figure 6: Circuit of TPS61170. Taken from the datasheet on p. 9. See table 9 for the componnets values.

Table 9: TPS61170 18 V Boost — Core Schematic Components

Ref	Value / Part	Notes
R1	$137\,\text{k}\Omega$	Sets $V_{\text{OUT}} \approx 18.06\,\text{V}$
R2	$10\,\text{k}\Omega$	see equation
L1	$10\,\mu\text{H}$, $I_{\text{sat}} \geq 1.2\,\text{A}$	$5{\times}5\,\text{mm}$ class inductor
D1	Schottky, $\geq 40\,\text{V}$	
C1	$4.7\,\mu\text{F}$, $\geq 25\,\text{V}$	
C2	$4.7\text{--}10\,\mu\text{F}$, $\geq 25\,\text{V}$	
R3	$10\,\text{k}\Omega$	
C3	$680\,\text{pF}$	
R_{GPIO}	$100\,\Omega\text{--}1\,\text{k}\Omega$	Series from MCU GPIO to CTRL
C_{CTRL}	$10\text{--}47\,\text{nF}$	Small RC on CTRL