Timed Model-Based Testing for openETCS

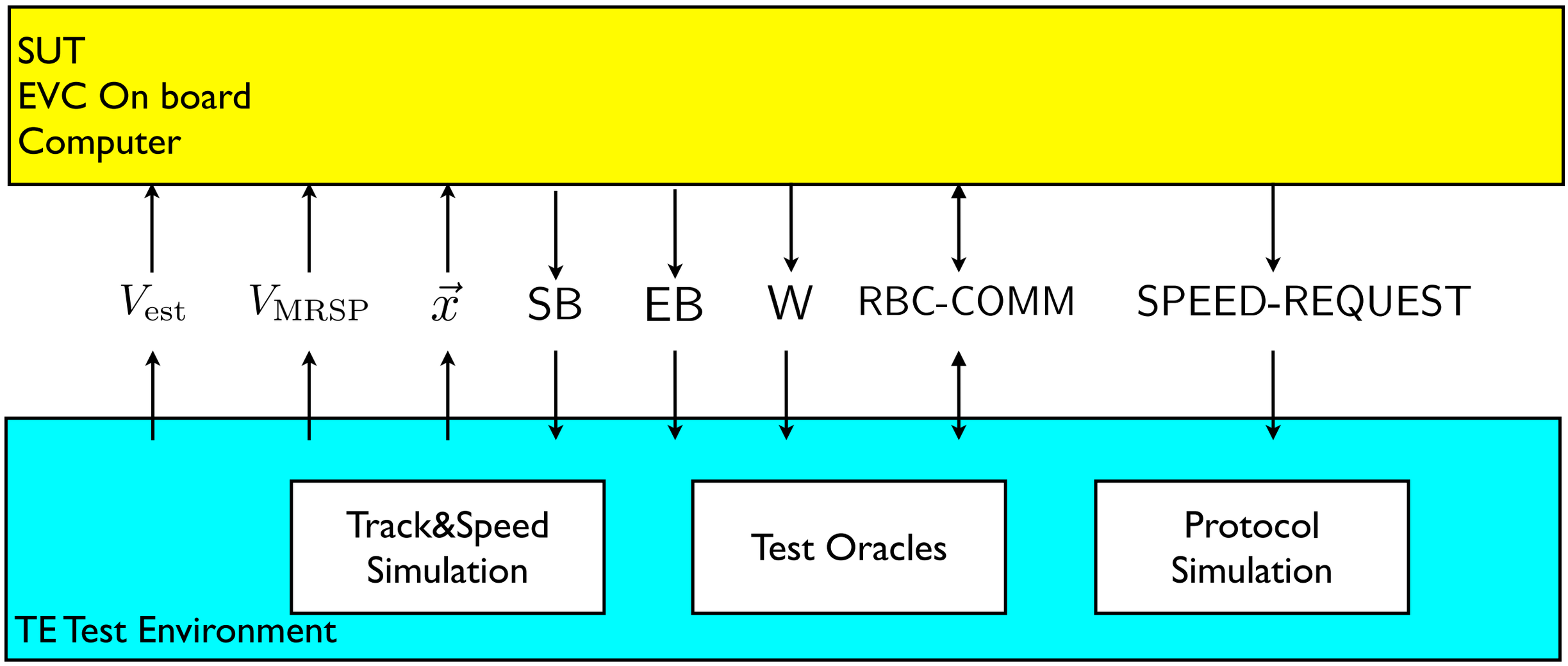
Jan Peleska
University of Bremen
2013-06-19

Objectives

openETCS system testing for the EVC on-board computer requires

- Test execution in real physical time
- Track layout with realistic speed profiles
- Simulated feed-back to EVC in response to negative (braking) and positive acceleration
- Simulated inputs from track elements and radio blocks to EVC, in order to provoke mode and level changes in the EVC
- Communication protocol handling etc.

System Test Configuration



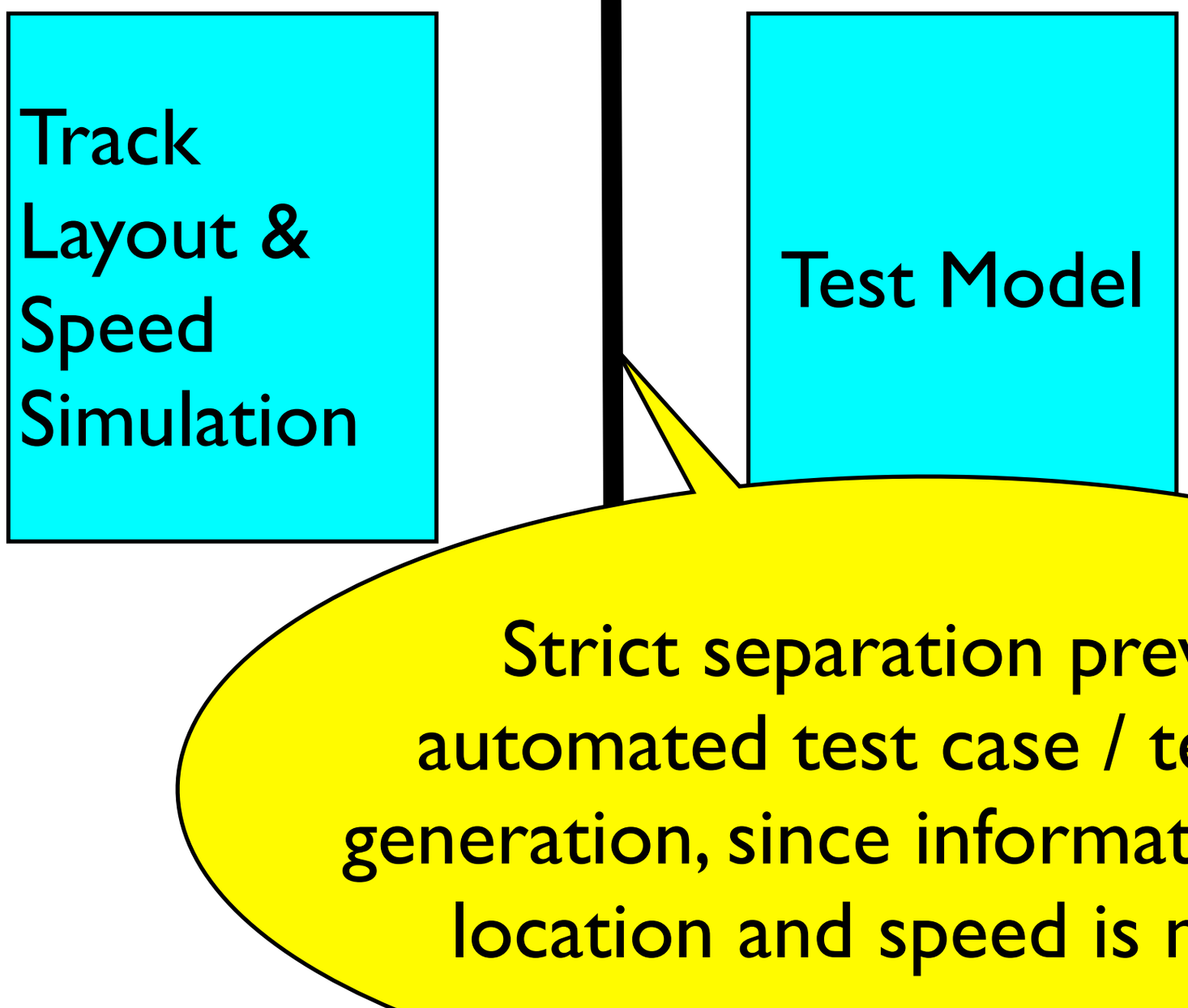
Two Variants for Track and Speed Simulation

- **Simple.** Manually programmed simulation
  - Every layout has to be configured in a manual way
- **Sophisticated.** Automated generation of "relevant" layouts and speed simulations
- Both variants will be realised for openETCS

Simple Variant – Challenge for MBT

- Track layout and speed simulation are "outside" the test model
- Relevant test cases have to be derived from incomplete test model
  - Not every detail of the track layout and speed simulation are known in the test model

Incomplete Test Model



For Test Generation: "Proxy" Provides "Basic" Simulation Information to Test Model

Track Layout & Speed Simulation

Test Model

TE-Submodel

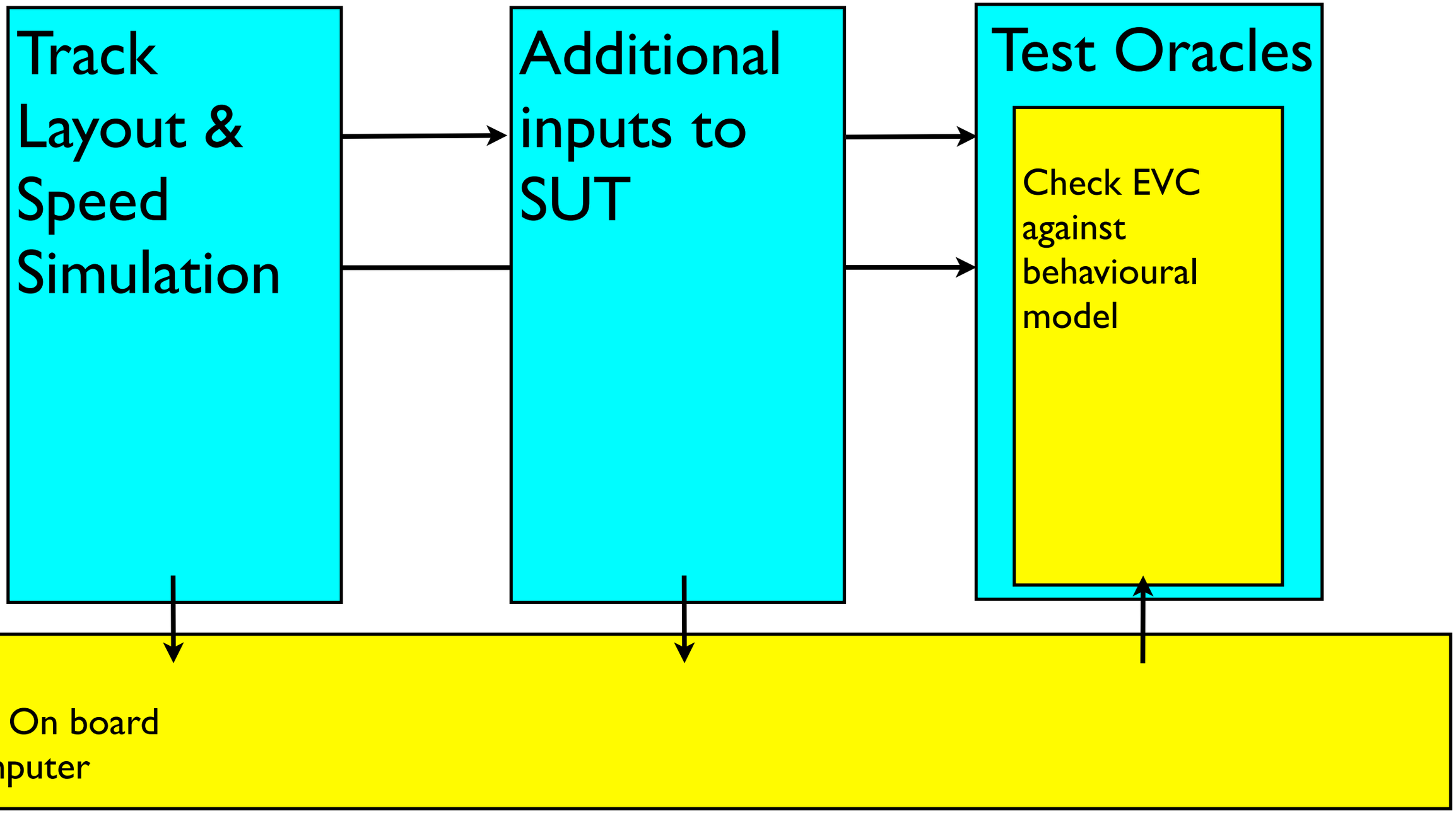
Simulation proxi providing threshold values from track layout and speed simulation

SUT-Submodel

EVC Behavioural Model

Simulation proxi sub-model provides sufficient information for test generator about relevant test cases

At Runtime: Test Oracles Observe Threshold Values from Simulation – Test Data is Sent to SUT in Sync With Track/Speed Data



Sophisticated Approach

- Test model (environment part) could contain **rules and restrictions** for
  - track layout generation
  - Speed calculation in response to braking events and speed controls by train engine driver

Sophisticated Approach – Advantages

- Test generator will **automatically create the layouts** that are relevant to cover all EVC functionality