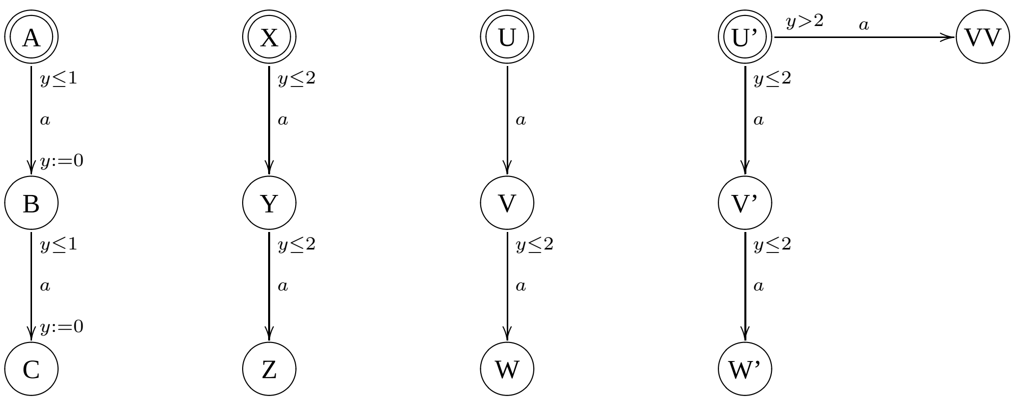
Tutorial 10

Exercise 1*

Consider the four timed automata below. Determine for each pair of initial states $(A, y = 0)$, $(X, y = 0)$, $(U, y = 0)$ and $(U', y = 0)$ whether they are timed bisimilar, untimed bisimilar or neither.



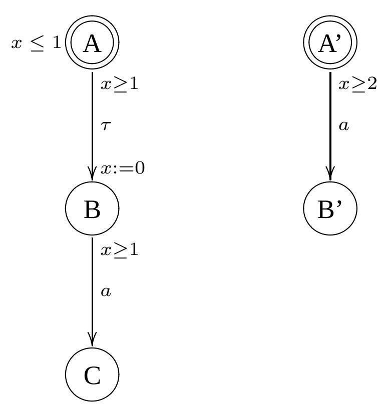
The four automata A, X, U and U'.

Exercise 2

Recall that a weak timed bisimilation is a binary relation $\mathcal{R}$ such that whenever $s\mathcal{R}t$, $a \in Act$ and $d \in \mathbb{R}^{\geq 0}$ then the following holds:

1. if $s \overset{a}{\Longrightarrow} s'$ then $t \overset{a}{\Longrightarrow} t'$ with $s'\mathcal{R}t'$ for some t',
2. if $t \overset{a}{\Longrightarrow} t'$ then $s \overset{a}{\Longrightarrow} s'$ with $s'\mathcal{R}t'$ for some s',
3. if $s \overset{d}{\Longrightarrow} s'$ then $t \overset{d}{\Longrightarrow} t'$ with $s'\mathcal{R}t'$ for some t',
4. if $t \overset{d}{\Longrightarrow} t'$ then $s \overset{d}{\Longrightarrow} s'$ with $s'\mathcal{R}t'$ for some s'.

where $s \overset{a}{\Longrightarrow} s'$ if $s \xrightarrow{\tau}^* \xrightarrow{a} \xrightarrow{\tau}^* s'$ and $s \overset{d}{\Longrightarrow} s'$ if $s \xrightarrow{\tau}^* \xrightarrow{d_1} \xrightarrow{\tau}^* \cdots \xrightarrow{\tau}^* \xrightarrow{d_n} \xrightarrow{\tau}^* s'$ with $d_1 + \cdots + d_n = d$. We say that s and t are weakly timed bisimilar if $s\mathcal{R}t$ for some weak timed bisimulation $\mathcal{R}$. Now consider the two timed automata below. Prove that $(A, x = 0)$ and $(A', x = 0)$ are weakly timed bisimilar.



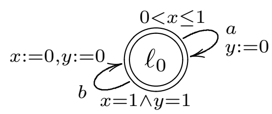
Exercise 3

Let $C = \{x, y\}$ be a set of clocks such that $c_x = 2$ and $c_y = 2$.

- Draw a picture with all regions for the clocks x and y.
- How many different regions there are on the picture?
- Select four different regions (corner point, line, two areas) and describe them via clock constraints.
- Try to find a general formula which describes a number of regions for two clocks and arbitrary maximal constants c_x and c_y.

Exercise 4*

Draw a region graph of the following timed automaton.



Using the region graph decide whether the following configurations

- (ℓ_0, v) where $v(x) = 0.7$ and $v(y) = 0.61$
- (ℓ_0, v) where $v(x) = 0.2$ and $v(y) = 0.41$

are reachable from the initial configuration.

Exercise 5

We want to model an intelligent *Interface* for a light controller. The interface has to properly translate the *press*ing and *release* of a button into actions controlling the light and light intensity based on their timing difference. In particular:

- If the time difference between the *press* and *release* is very short (no more than 0.5 sec) then nothing happens (it was too fast to be noticed).
- If the time difference is between 0.5 sec and 1.0 sec between the *press* and *release*, the light is *toggled*, i.e. the light goes from on to off or from off to on.
- At the moment 1.0 sec has elapsed from the *press* without the button having been *released* the interface issues an instruction for letting the light intensity begin to *dim*. The dimming is *stop*ped only when the botton is *release*d.

Model the above Interface as a timed automaton with two input actions (*press* and *release*) and three output actions (*toggle*, *dim* and *stop*).

Exercise 6 (Optional)

Let T be the *alarm timer* from exercise 4 in Exercise Set 9. In this exercise we will show how to make use of T. We want to model a process which offers the action a for 30 time-units after which a time-out will occur. Now we may express this behaviour directly in TCCS using the following definition:

$$A \stackrel{\text{def}}{=} a.P + \epsilon(30).\tau.Q$$

where P is a term describing the behaviour after a and Q a term describing the behaviour to be followed after the time-out. Now using the alarm timer T we may express this behaviour alternatively as:

$$B \stackrel{\text{def}}{=} \overline{set30}.(a.P + to.Q)$$

Prove that this is an equivalent definition in the sence that A and $(B \,|\, T)\backslash\{set5, set10, set30, to\}$ are weakly timed bisimilar.

Exercise 7 (Optional)

Apply the product construction and notion of symbolic bisimulation in Section 2.6 of Fahrenberg, Larsen, Thrane: *Verification, Performance Analysis and Controller Synthesis for Real-Time Systems* to prove or disprove timed bisimilarity of the timed automata U and U' of Exercise 1.