ECE 581 Final Report

Pipelined ADC Design

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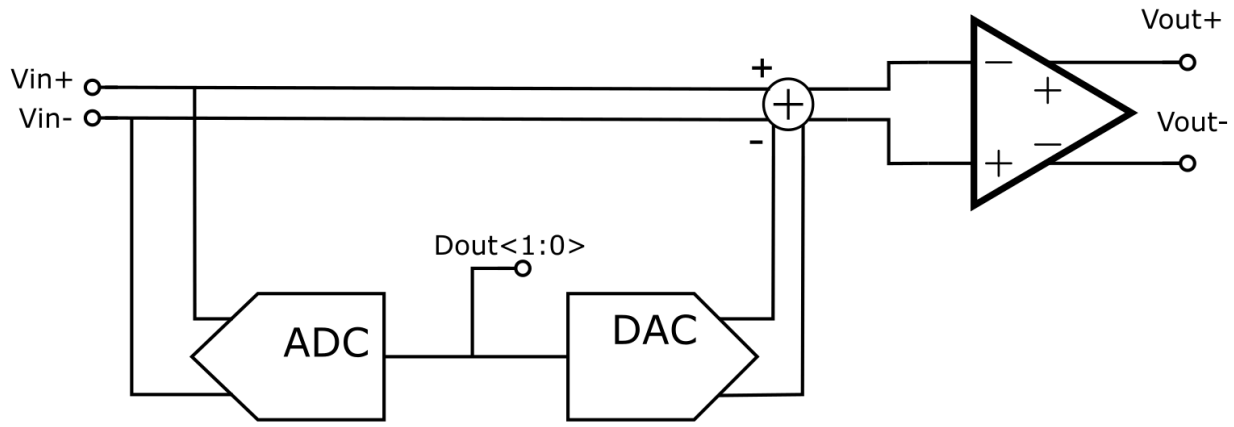
(1) Overall Design Approach:



(i) Common Mode voltage:
CM voltage was chosen at 1.1 voltage to allow NMOS current sources and cascode transistors to operate comfortable within saturation.

(ii) Reference voltage:
I selected a differential reference voltage of 1V. Due to a differential input range of +1V, -1V, splitting up the 1.5 bit adc into ranges of <-0.25, -0.25 to 0.25, and >0.25 gives a good margin of error.

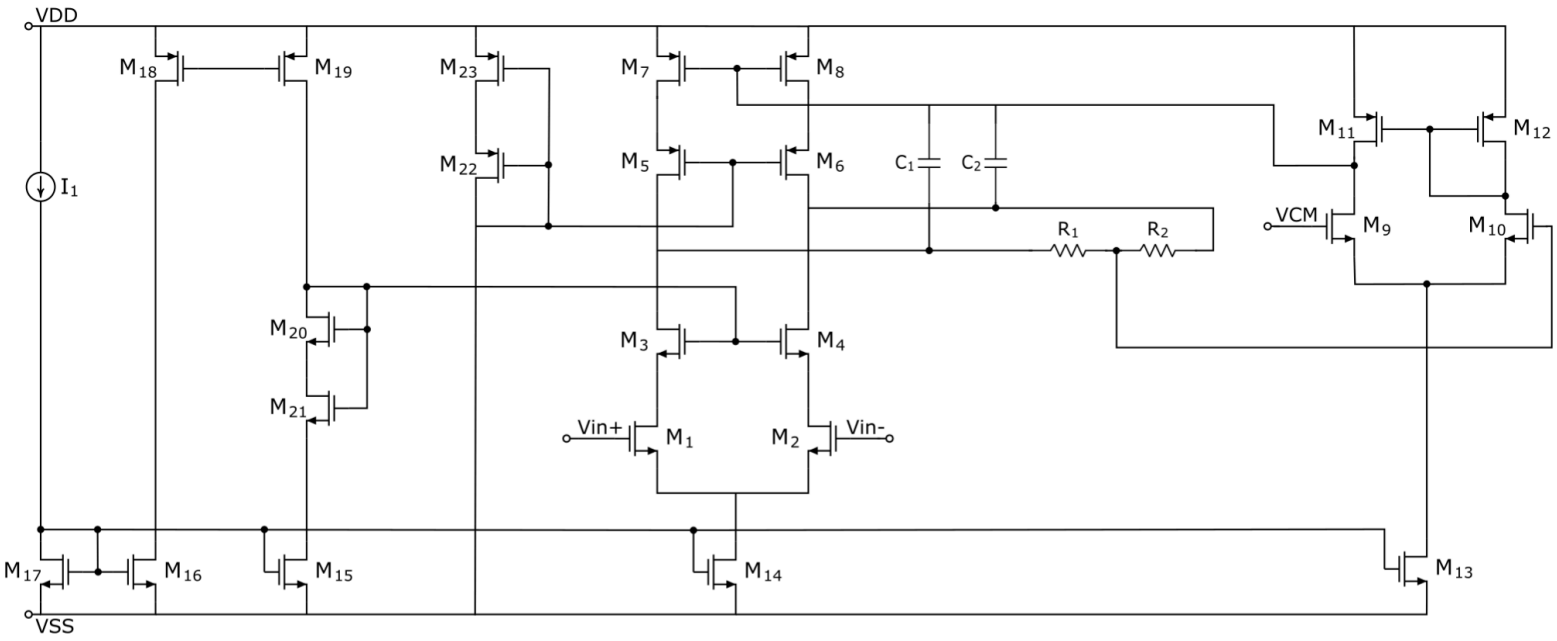
(iii) MDAC Capacitor values:
After calculating the transfer characteristics of the switched capacitor residue amplifier, I was able to arrive at a transfer equation through the following process:

$-Cs * VDAC[n] - CfVout[n] = -(Cf + Cs) * Vin(n-1)$
$Vout[n] = ((Cf + Cs) * Vin - Cs * Vdac) / Cf$

To obtain a gain of 2 for the output residue, I selected Cf = Cs = 1pF.

(iv) Other design tradeoffs
For the residue amplifier, I elected to use a single stage differential cascode amplifier with common mode feedback. This would allow me to obtain enough gain (25-30dB) to avoid considerable static error, and would also allow me to ignore any potential stability issues that would arise from a 2 stage amplifier. One disadvantage was having to carefully choose my DC operating points to ensure all transistors stayed in optimal operating conditions. The common mode feedback was stabilized through use of a miller capacitor connected to the output, trading off gain and output speed for common mode stability.

(2) Residue Amplifier Schematic:



Tabulated Parameters:

Component	W / L, Capacitance, Resistance, Current	Component	W / L, Capacitance, Resistance, Current
I1	10uA	M18	270n / 180n
M1, M2, M3, M4, M5, M6	92.16u / 180n	M19	270n / 720n
M7, M8	92.16u / 450n	M20	270n / 180n
M9, M10	19.99u / 180n	M21	270n / 720n
M11, M12	4.5u / 990n	M22	360n / 180n
M13	1.08u / 360n	M23	360n / 360n
M14	24.75u / 360n	C1, C2	200f
M15	270n / 360n	R1, R2	10kΩ
M16, M17	540 n / 360n		

(3) Amplifier Performance

Table 1: Residue Amplifier Specifications

Design parameter/variable	Simulated performance	Specification
Supply voltage	1.8V	≤ 1.8V
Closed loop gain	26.0087dB	30dB
Static settling error+	57.458mV	32.258mV
Load capacitance (CL) +	2.4736pF	2.2pF
Settling time (pos step) -1 to 1	113.329ns	150ns
Settline time (neg step)	121.8895ns	150ns
Peak SNR	114.88dB	N/A
Differential r.m.s noise voltage [μV]	1.802uV	N/A
THD (Fin = 0.5MHz)	-18.766dB	N/A
THD (Fin = 9MHz)	-25.523dB	N/A
Amplifier core power consumption [mW]	0.75168mW	minimal
Bias power consumption [mW]	0.046845mW	minimal
Total power consumption [mW]	0.798525mW	minimal
Differential DC loop gain (vod = 0) [dB]	-6.4kdB	minimal
Differential DC loop gain (vod = vod,max) [dB]	31.986dB	30dB
Differential loop-gain unity gain bandwidth [MHz]	256.597MHz	N/A
Differential loop-gain phase margin [deg]	83.7997deg	N/A
Differential loop-gain gain margin [dB]	27.087dB	N/A
Common-mode loop-gain unity gain bandwidth [MHz]	37.8167MHz	maximum
Common-mode loop-gain phase margin [deg]	44.19278 deg	45 deg

(4) Calculations for Amplifier Performance

(i) DC Gain:

DC Gain was calculated with a target of 30dB, using the input pair gm and output capacitance CL.

(ii) Static settling error:

With a gain of 30dB or 30V/V and differential peak voltage of 1V, we can calculate the settling error as 1 - 30 / (30 + 1) * 1 = 32.2mV.

(ii) Load capacitance:

Load capacitance was first measured at the transmission gate latch connected to the amplifier output, then added from the feedback capacitors in the switched cap circuit and the capacitance of the ideal ADC. Lastly, capacitance from the miller compensation in the common mode feedback circuit was added.

(iv) Power consumption:

Current usage was minimized when possible, and only increased if gain or settling time requirements needed to be met.

(v) Differential Stability:

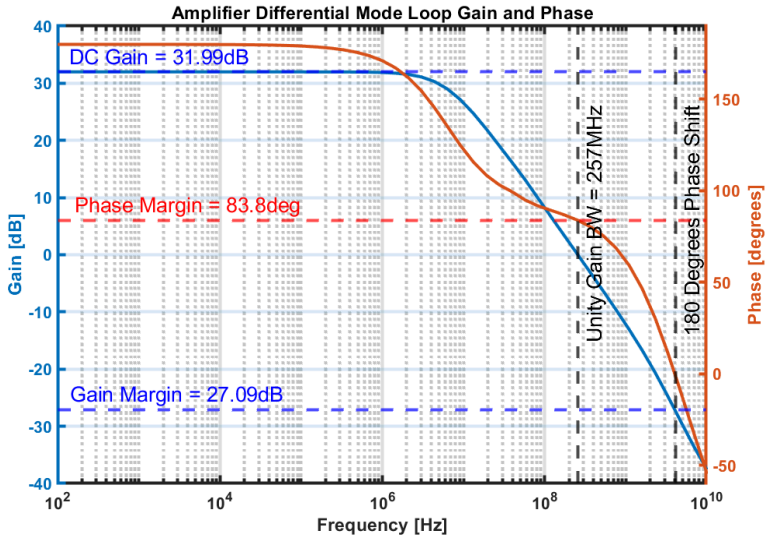
Due to selecting a single stage differential design, there were no stability concerns due to only having one pole.

(vi) Common Mode Stability:

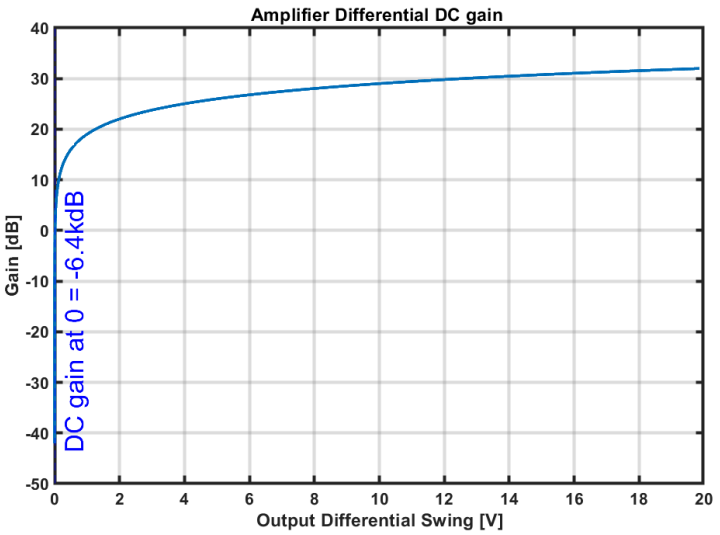
In order to avoid affecting output capacitance and differential gain by a large amount, I set the phase margin requirement for common mode loop gain to be only 45 degrees, and added only enough compensation to meet that requirement.

(5) Amplifier Simulation Results

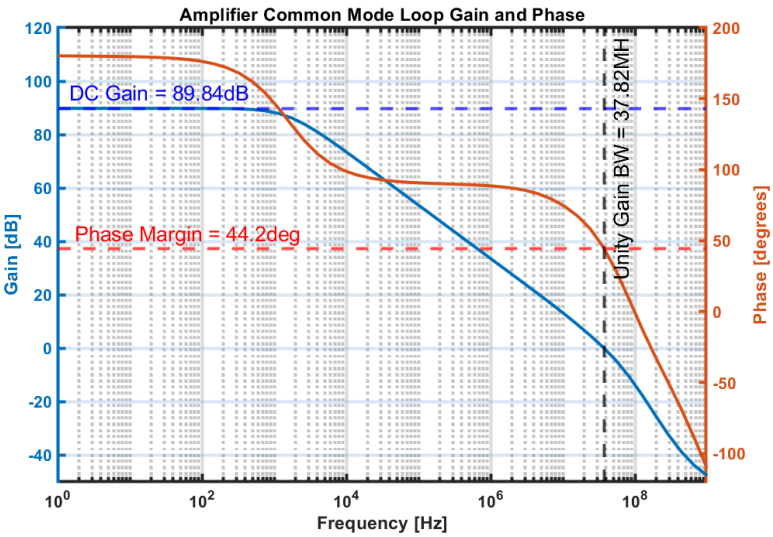
(i) Differential-mode loop-gain AC response



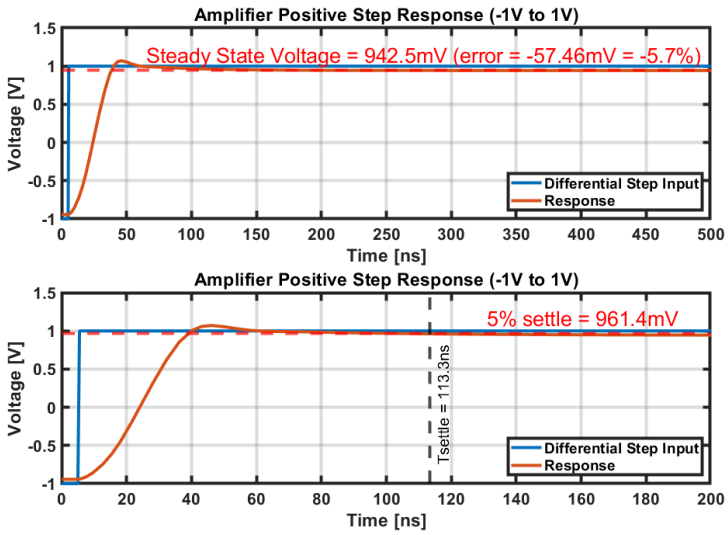
(ii) Differential-mode DC loop-gain



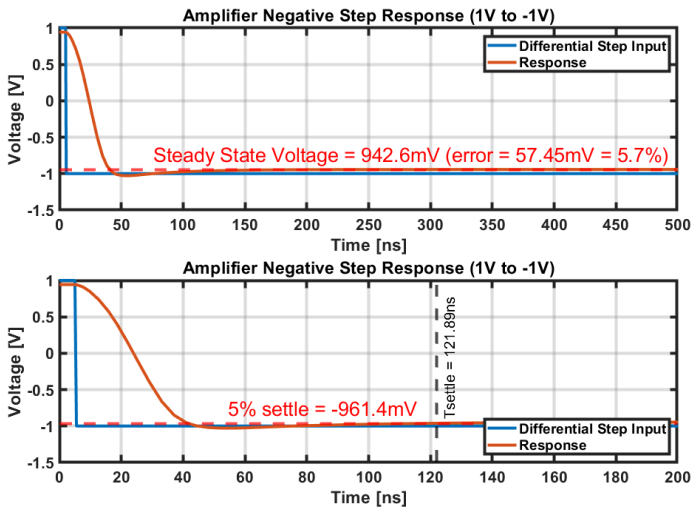
(iii) Common-mode loop-gain AC response



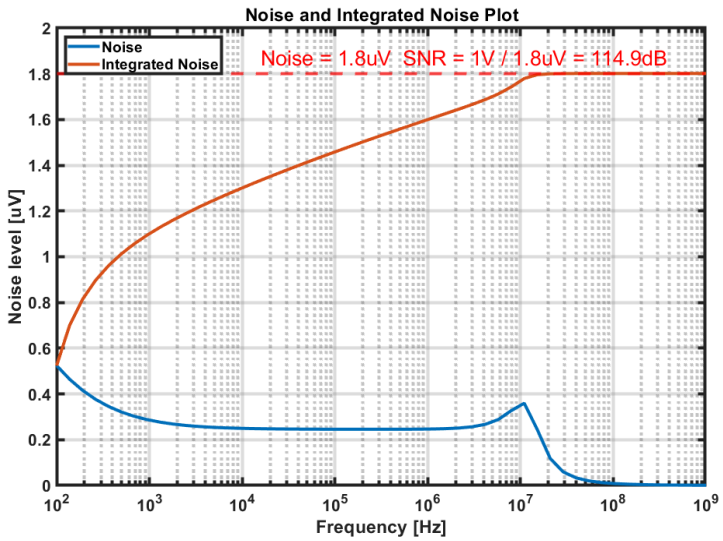
(iv) Positive step response



(v) Negative step response



(vi) Differential Noise

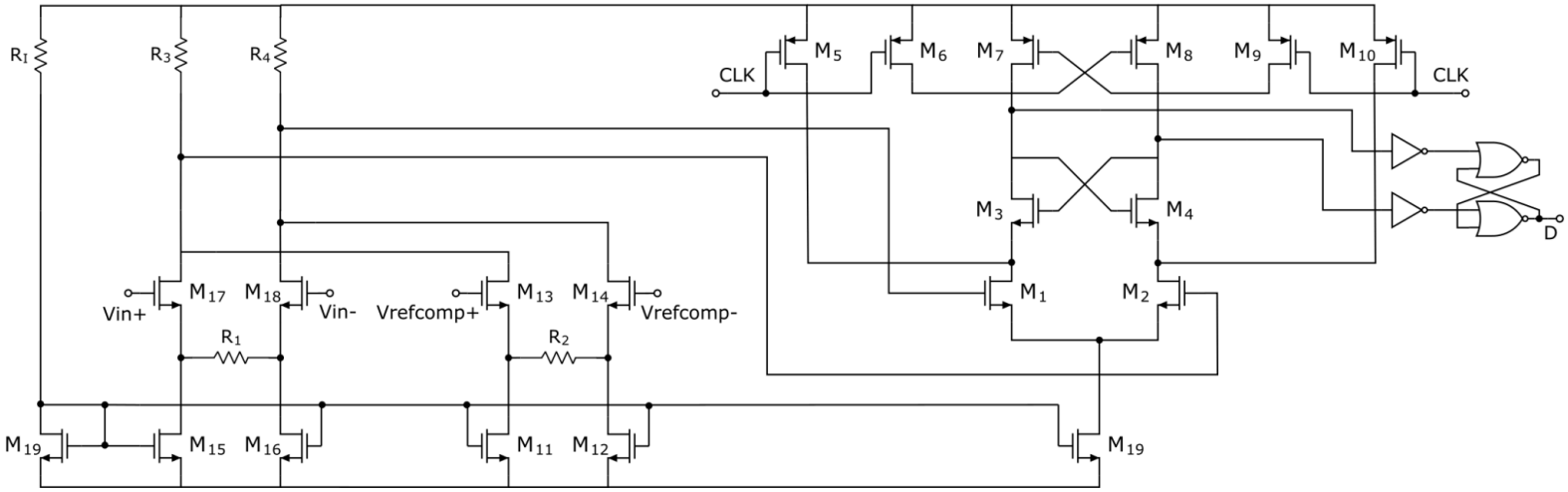


(6) 1.5 Bit Sub-ADC Design

(i) Overall Design Approach

The differential pairs for combining the input voltage and the reference voltages (initially set at Vref / 4 = 0.25) were designed first. Finding that a common mode voltage of 0.9 was too low to allow the NMOS current sources to operate properly, I raised the common mode voltage to 1.1V, utilizing a current of 5uA though M15, 16, 11, and 12 and the common mode voltage of 1.1V to calculate R1, R4 values. After creating the Strong-ARM latch, I ran transient simulations to determine the amount of noise passing through the overall 1.5 bit ADC due to rise times. I increased M19 size (bias current), M1/M2 input pair size, and the output inverter and NOR W/L size until rise/ time decreased and noise dropped to an acceptable level. Vrefcomp+ and Vrefcomp- and R1/R2 values were tuned to obtain optimal gain and place the bit transition points at +Vref / 2, - Vref / 2.

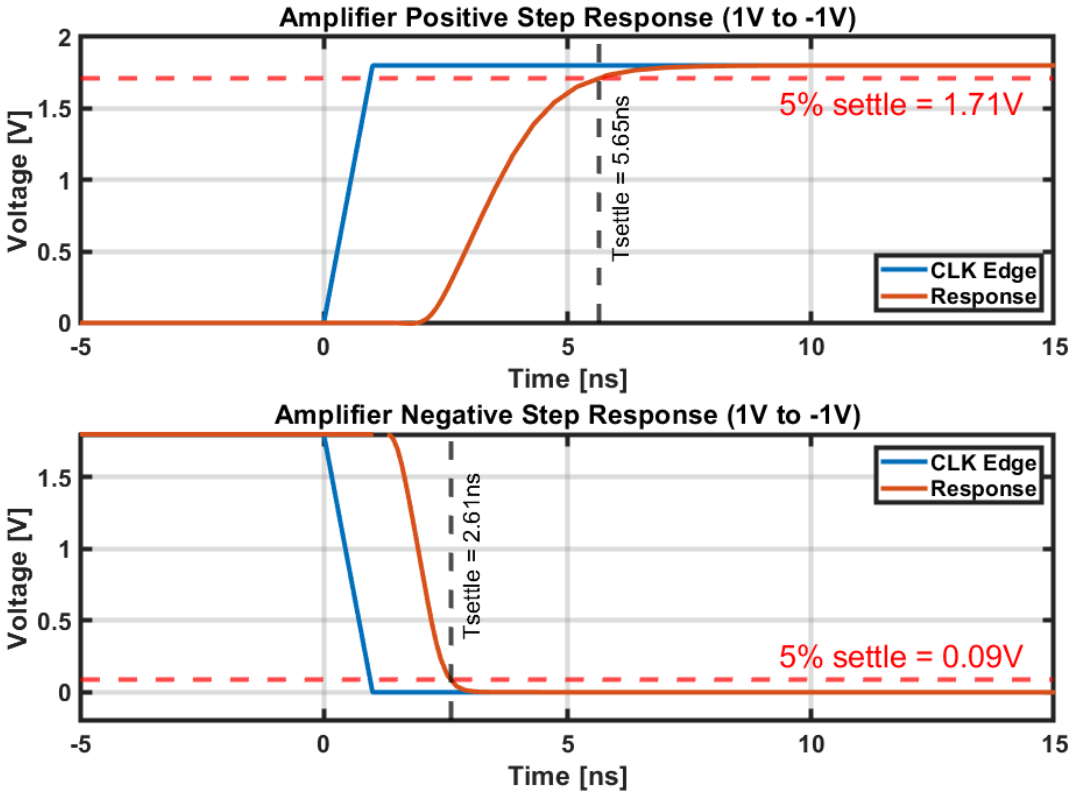
(ii) Schematic



Tabluted Parameters:

Component	W / L, Resistance	Component	W / L, Resistance
RI (5uA)	237.78kΩ	M5, M6, M7	540n / 180n
R3, R4	60kΩ	M8, M9, M19	540n / 180n
R1, R2	40kΩ	Inverter PMOS	40.004u / 180n
M11, M12, M15, M16	540n / 360n	Inverter NMOS	19.98u / 180n
M13, M14, M17, M18	10.8u / 180n	NOR PMOS	40.004u / 180n
M19, M1, M2	27u / 180n	NOR NMOS	19.98u / 180n
M3, M4	270n / 180n	Vrefcomp+, -	1.225V, 0.975V

‘(iv) Comparator transient settling waveforms



(7) MDAC Design Process

(i) Digital components

When designing the MUXes, I decided to utilize transmission gates to minimize resistance and transistor usage. By connecting the bit output from the sub-ADC to the Muxes, I was able to use two MUXes with alternated Vref/2 inputs (added to the common mode voltage) to generate the necessary differential voltage offsets for each region.

(ii) Sizing of transmission gates and inverters

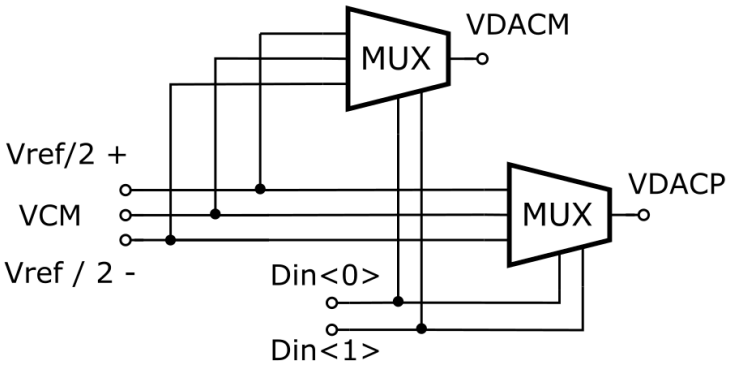
20u width with minimum 180n length was selected at first, and after simulation of transient waveforms the digital components of the DAC did not contribute noticeably to rise time. Therefore, I settled on a size of 20u / 180n for all transmission gate MOS/inverter NMOS, and 40u / 180n for all inverter PMOS.

(iii) Switched Capacitor circuit

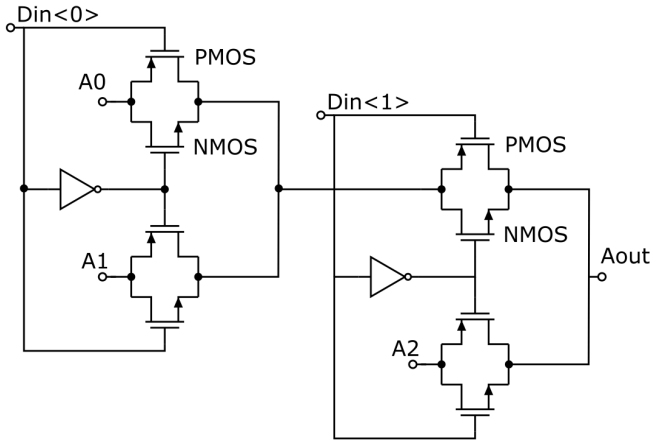
Utilizing the design shown below, all switches were modelled with the same sizes as in the MUXes. Capacitor values were chosen to be equal as calculated in Section 1 in order to achieve a gain of 2.

(8) MDAC Schematic

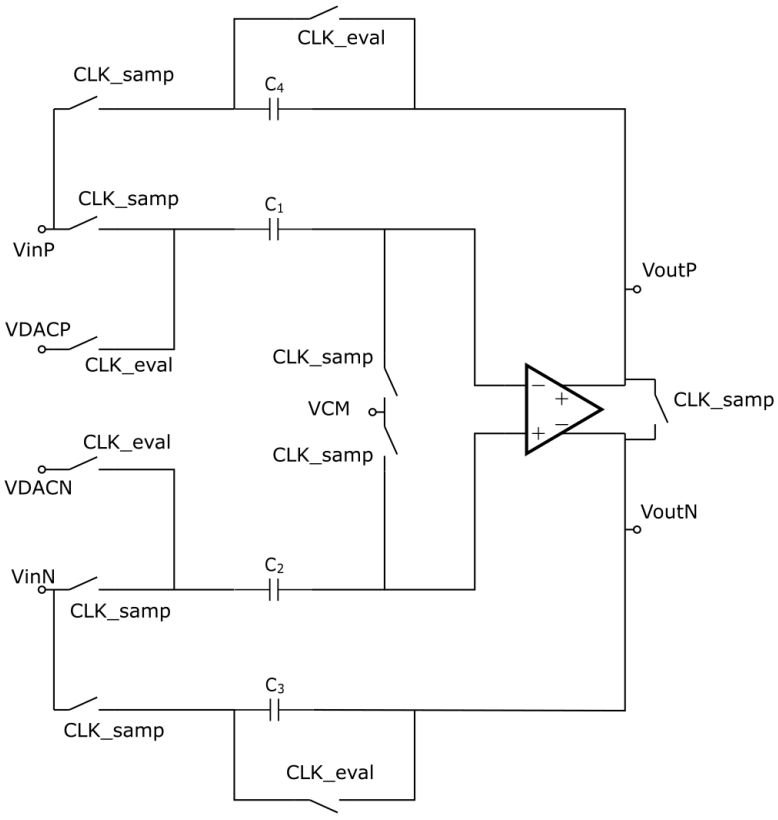
(i) Digital VDAC offset voltage selection



(ii) 3:1 MUX. All transmission gates and inverters use identical sizing.



(iii) Switched capacitor amplifier

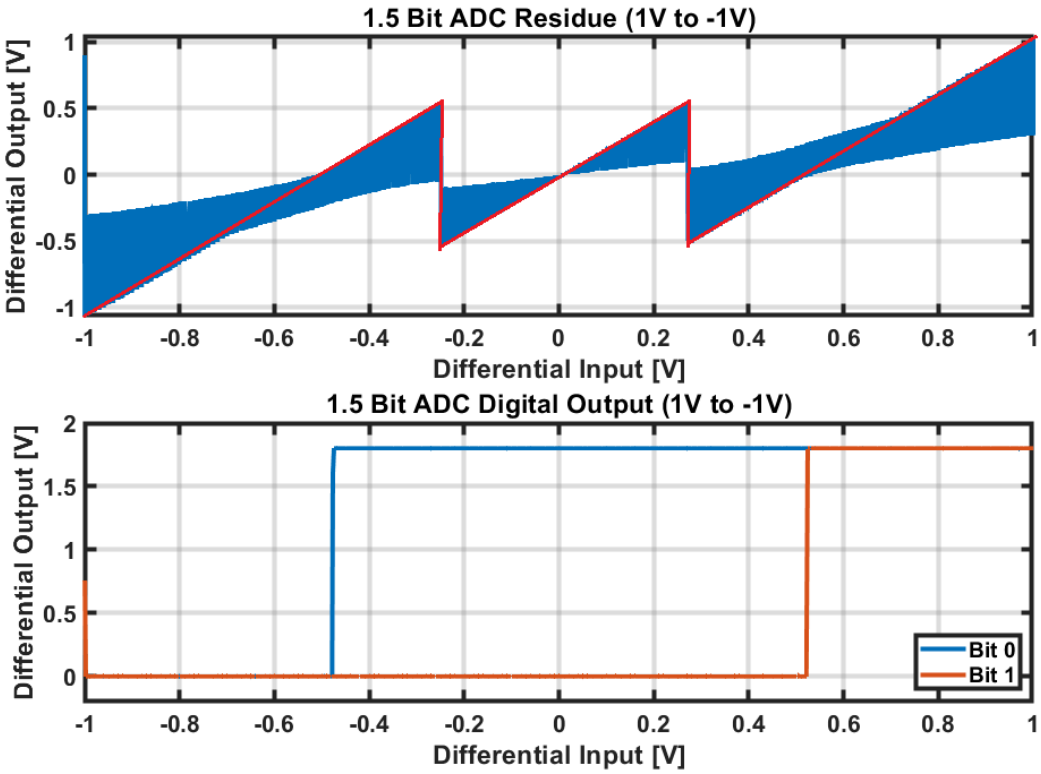


(iv) Tabulated Parameters

Component	W / L, Capacitance
Transmission Gate PMOS	19.98u / 180n
Transmission Gate NMOS	19.98u / 180n
Inverter PMOS	40.004u / 180n
Inverter NMOS	19.98u / 180n
C1, C2	1pF
C3, C4	1pF

(9) 1.5 Bit ADC Simulation Results

(i) Output Residue Voltage (ii) 2 Bit Digital Output



Noise in ADC residue noise was minimized by increasing device width at the output latch (inverter, NAND) as well as the Strong-ARM latch input pair, and increasing Strong-ARM bias current.

(iii) Total Overall Power consumption:

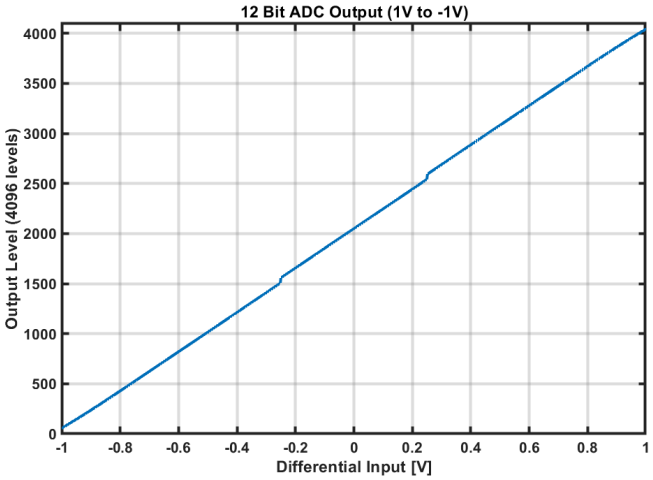
Module	Current (uA)	Power Consumption (mW)
Differential pairs	49.636	0.0893
Strong-ARM latch	66.18	0.1191

Power was found through DC simulation of operating points. Strong-ARM latch current was inferred to be (Duty Cycle * ON current). Two instances of each module were used, with inverted reference voltage inputs connected to the copy to generate B<0> and B<1>.

Bias voltages were generated via a resistor voltage divider, generating 1.6V, 1.225V, 1.1V, 0.975V, and 0.6V using resistance values of 400Ω, 750Ω, 250Ω, 250Ω, 750Ω, and 1.2k in series. This led to a current consumption of 0.5mA. This was a temporary solution, and CMOS bias generation (similar to that used on the amplifier) can be substituted for much lower current consumption

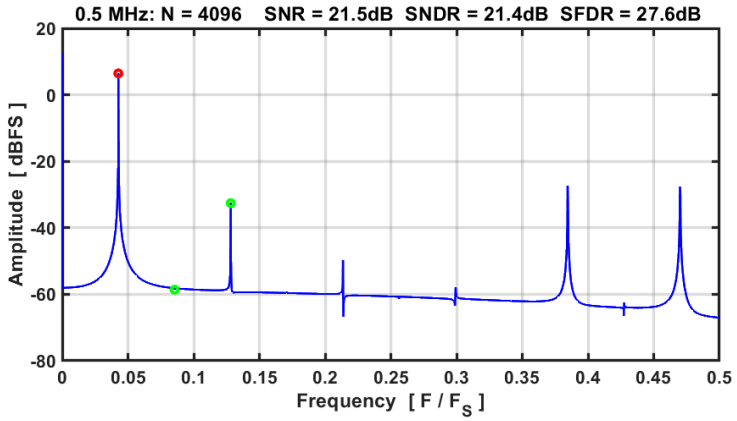
(10) Overall Simulation results: 12 Bit ADC

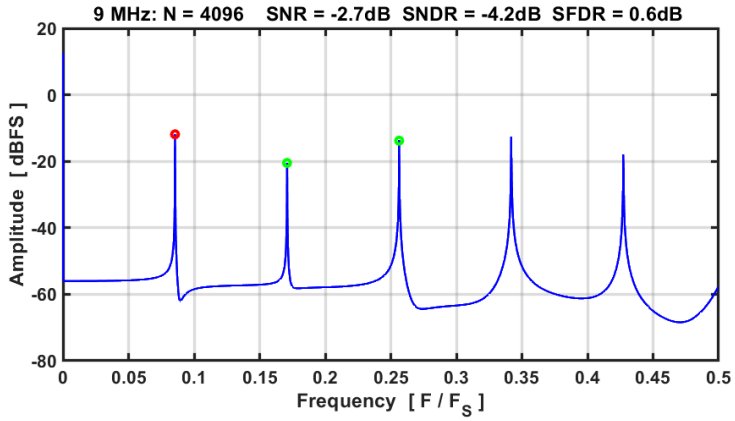
(i) Overall ADC output for ramp inpu



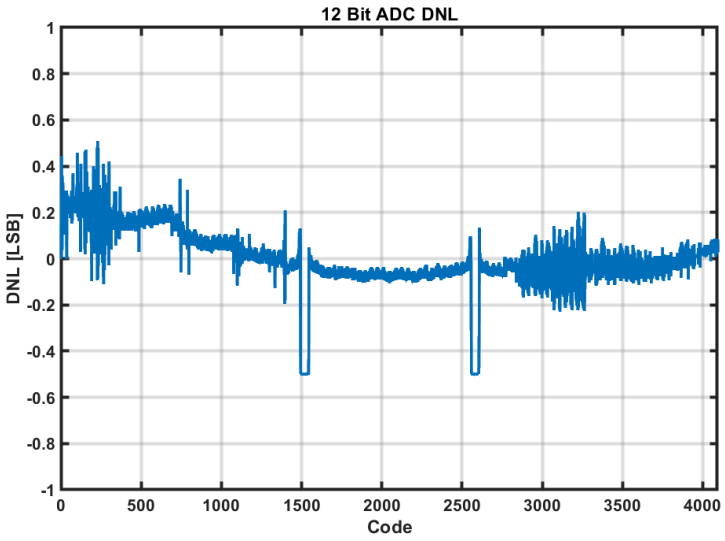
Additional Notes: I was unable to configure the FFT program correctly for the 9MHz case, meaning I was unable to acquire an accurate output spectra for it.

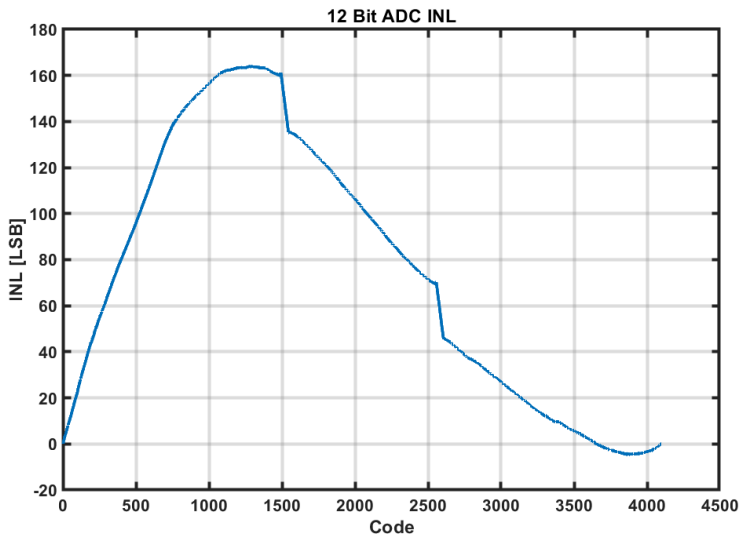
(ii) Output spectra, 0.5MHz and 9MHz





(iii) DNL and INL





(11) Other Features

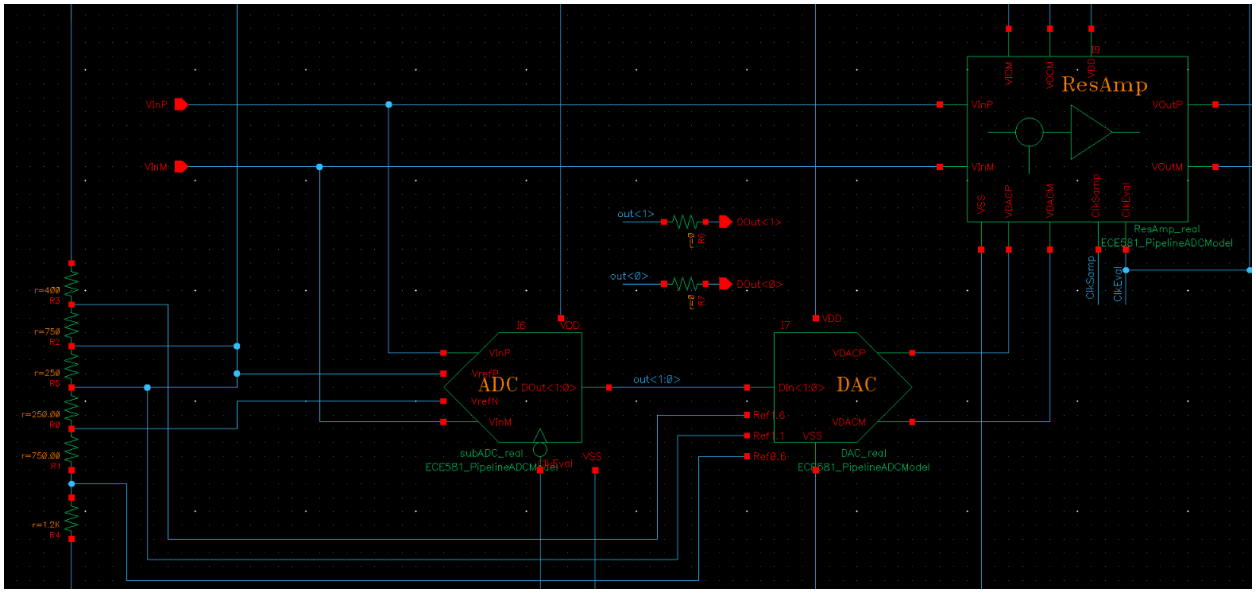
(i) Known Errors

One of the miller capacitors compensating the common mode feedback was accidentally set to 500f instead of the intended 200f and only discovered during the writing of this report. This likely lead to reduced differential gain and impacted common mode stability results, meaning transient settling times were probably altered.

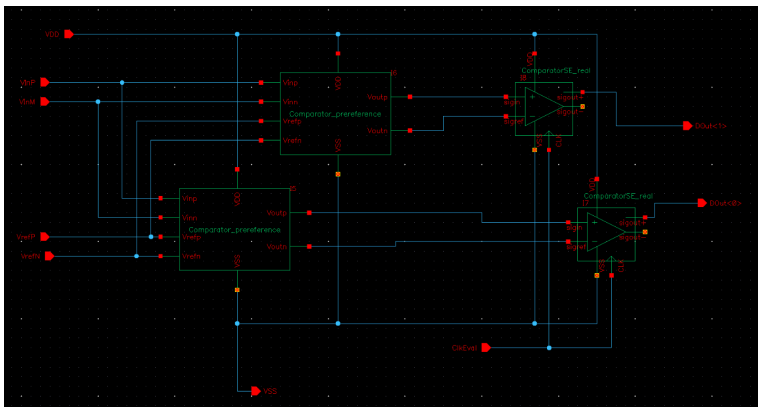
In addition, I was unable to configure the FFT program properly for the 9MHz sine wave input for the overall 12 bit ADC simulation, leading to an inaccurate result on Section 10ii.

(ii) Cadence Screenshots:

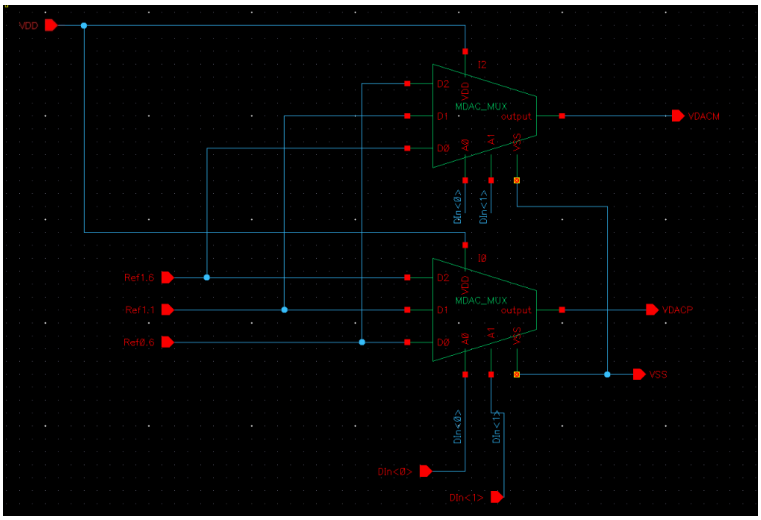
Overall 1.5-bit ADC



Sub-ADC:



DAC:



Switched Capacitor Residue Amplifier: