CSc/CPE 142 Fall 2014
Term Project Status Report

Complete this form by typing the requested information and include the completed form in your report after TOC. Gray cells will be filled by the instructor.

Name	*% Contribution*	*Grade*
Ben Smith	*50%*	
Devin Moore	*50%*	

Please do not write in the first table

Project Report/Presentation 20%	/200
Functionality of the individual components 40%	/400
Functionality of the overall design 25%	/250
Design Approach 5%	/50
Total points	/900

A: List all the instructions that were implemented correctly and verified by the assembly program on your system:

Instructions	State any issue regarding the instruction.
Signed addition	None
Signed subtraction	None
bitwise and	None
bitwise or	None
signed multiplication	None
signed division	None
Logical shift left	None
Logical shift right	None
rotate left	None
rotate right	None
load	None
store	None
branch on less than	None
branch on greater than	None
branch on equal	None
jump	None

Instructions	State any issue regarding the instruction.
Halt	None

B: Fill out the next table:

Individual Components	Does your system have this component	Does it work ?	List problems with the component, if any.
ALU	yes	yes	None
ALU control unit	yes	yes	None
Memory Unit	yes	yes	None
Register File	yes	yes	None
PC	yes	yes	None
IR	yes	yes	None
Other registers	yes	yes	None
Multiplexors	yes	yes	None
exception handler 1. Unknown opcode 2. Arith. Overflow …..	yes	yes	None, but the CPU does not transfer control to an ISR upon fault, in both cases the system halts.
Control Units 1. main 2. forwarding 3. lw hazard detection	yes	yes	None

How many stages do you have in your pipeline? Three

C: **State any issue regarding the overall operation of the datapath? Be Specific.**

CPU performs the expected instructions, including the full test program. Validations cases were generated for all instructions at the system level leaving a high degree of confidence in design functionality.