AEV: Séance 2

Benjamin Van Ryseghem

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1 Exercice 1

```
entity exo1 is
port( clk: in bit;
a: in bit_vector (4 downto 0),
s: out bit_vector (2 downto 0);
end exo1;

architecture aexo1 of exo1 is
begin
with a select
s <= "101" when "01001",
        "011" when "10010",
        "001" when others;
end aexo1;
```

2 Exercice 2

`<=` affectation de signaux
`:=` affectation direct
`=` comparaison

2.1 Question 1

a	b	s
0	0	1
0	1	0
1	0	0
1	1	1

Cela équivaut à un "not xor".

2.2 Question 2

c.f Figure 1.

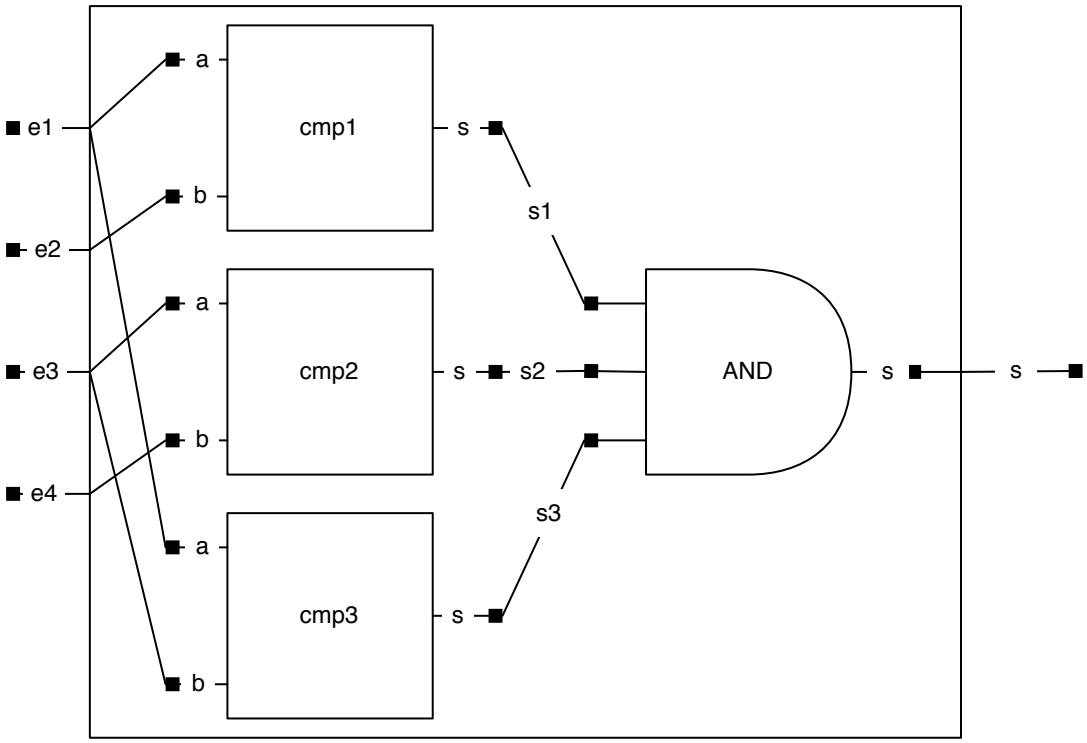

FIGURE 1 – Analyse structurelle

2.3 Question 3

Ce circuit est un *comparateur 4 bits*.

3 Exercice 3

3.1 Question 1

```
entity circuit is
       port (A, B, Cin : in std_logic;
               S, Cout : out std_logic);
end circuit;

architecture archi_circuit of circuit is
       s <= A Xor B Xor Cin;
       Cout <= (A AND B) OR (A XOR B) AND CIN;
```

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