AEV: Séance 3

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1 Exercice 1

1.1 Question A

1.2 Question B

See figure 1.

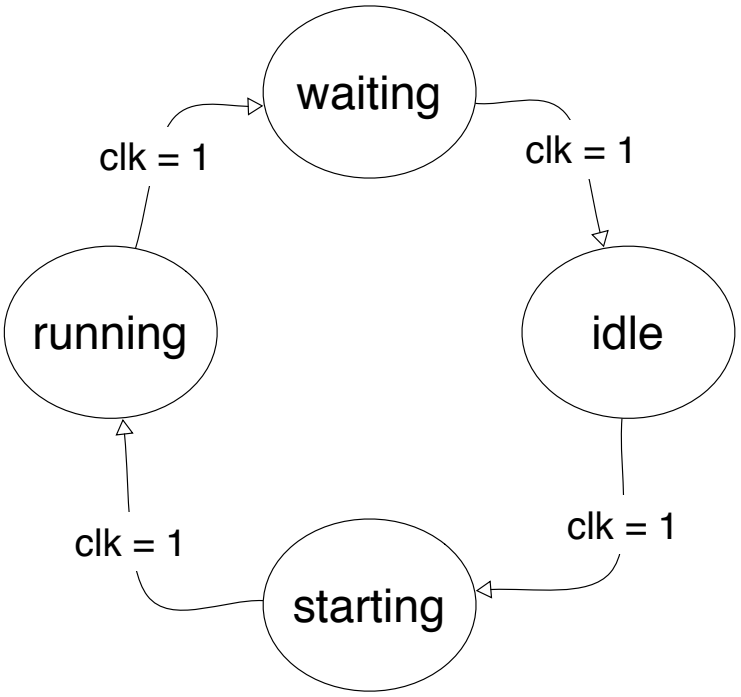

Figure 1 – State Diagram

1.3 Question C

See figure 2.

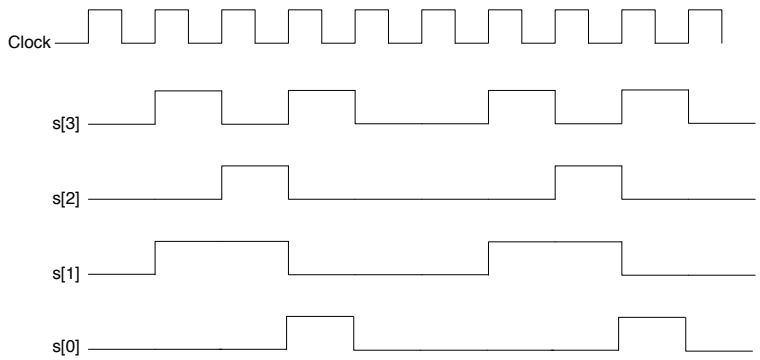

FIGURE 2 – Chronogram

2 Exercice 2

```
entity fsm2 is
    port (
        clock : n std_logic;
        S : out unsigned (3 downto 0)
        );
end    fsm2;

architecture afsm2 of fsm2 is
    type etat_type is (cours,TD,DS,TP);
    signal état : etat_type;

begin
        process
        begin
            wait until rising_edge(clock);
            case stat is
                when cours => état <= TD;
                when TD => état <= TP;
                when TP => état <= DS;
                when DS => état <= cours;
            end case;
        end process;

        with stat select
        S <= "1100" when cours,
             "0010" when TD,
             "0001" when TP,
             "1100" when DS;
end afsm2;
```

3 Exercice 3

4 Exercice 4

See figure 3.

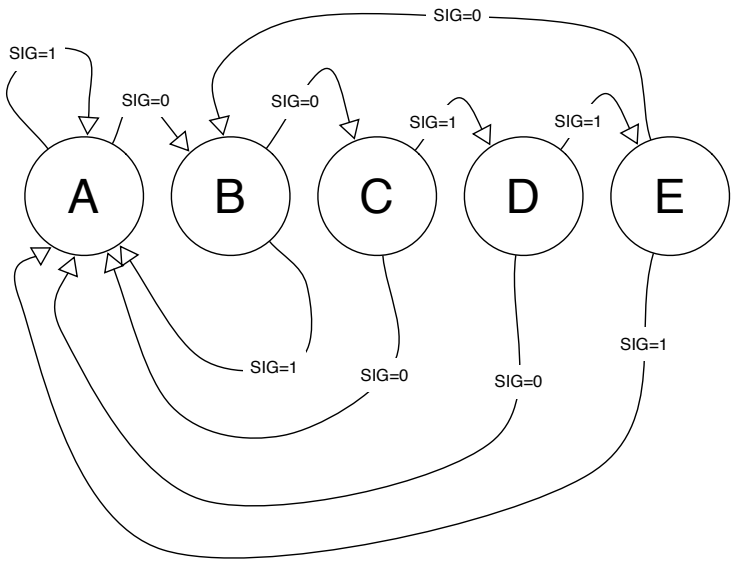

FIGURE 3 – State Diagram

```
entity FSM_6 is
port(
        CLOCK: in bit;
        SIG: in bit,
        EDG: out bit );
end FSM_6;

architecture AFSM_6 of FSM_6 is
        type etat_type is (first, second, third, fourth, nothing);
        signal etat : etat_type;
begin
        process
        begin
                wait until rising_edge (CLOCK);
                case etat is
                        when nothing    => if (SIG = 0) etat <= first else etat <= nothing;
                        when first      => if (SIG = 0) etat <= second else etat <= nothing;
                        when second     => if (SIG = 1) etat <= third else etat <= nothing;
                        when third      => if (SIG = 1) etat <= fourth else etat <= nothing;
                        when fourth     => if (SIG = 0) etat <= first else etat <= nothing;
                end case;
        end process;

        with etat select
        EDG <=  "0" when fourth,
                "1" when others;
end AFSM_6;
```

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