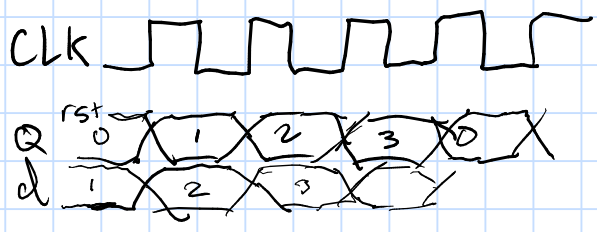
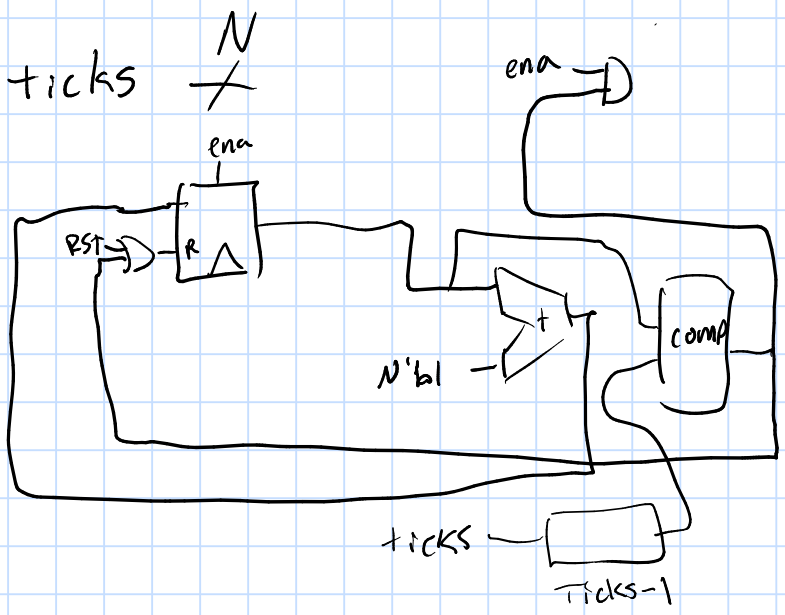
LAB 0X02

Pulse generator

@ every clock
counter ( )

out = ticks == counter





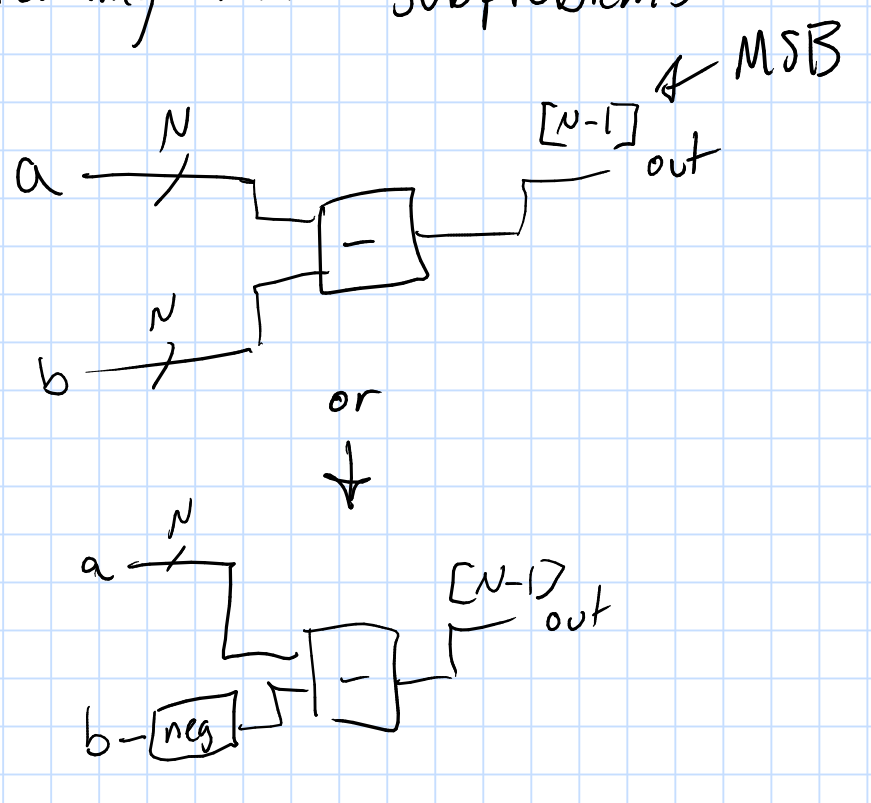
Q	d
0	1
1	2
2	3
3	0

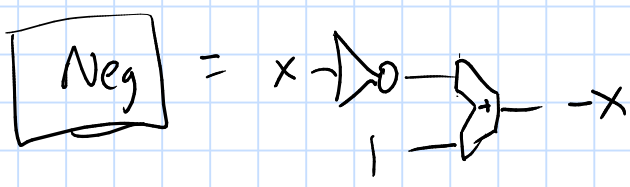
SLT (Standard less than)

a<b

if a - b is negative, than a<b

so, breaking into subproblems





How to eliminate edge cases

1 1 1 1 1 1 1 1 = 1 1 1 1 1 1 1 1 → overflow, but they are equal
- 1 1 1 1 1 1 1 1 = + 0 0 0 0 0 0 0 1 c_out

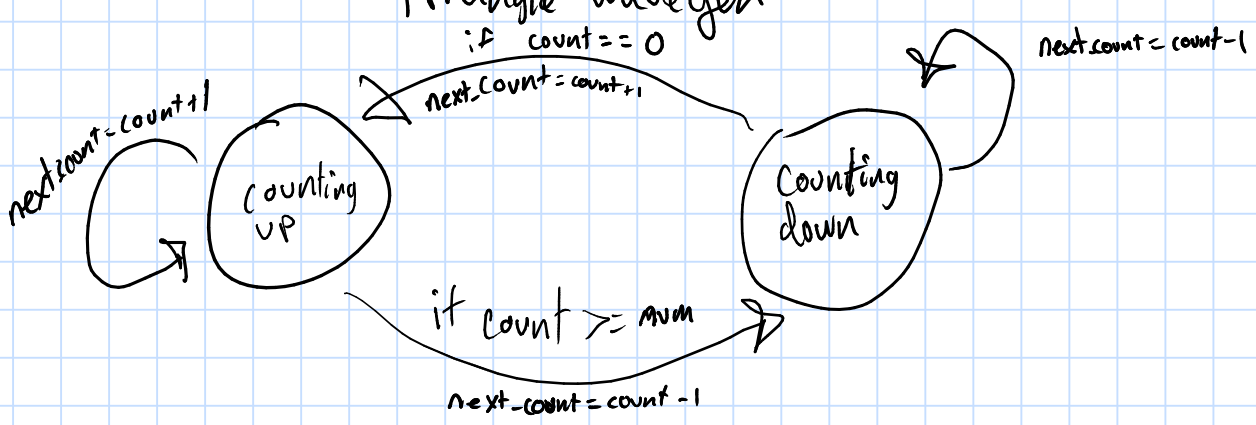
0 1 1 1 1 1 1 1 c_out
1 1 1 1 1 1 1 0

0 0 0 0 0 0
- 1 0 0 = + 1 0 0

what does c_out mean in subtraction?

c_out happens if a - b is very negative

Triangle wavegen



FSM implementation

PWM

ideally, duty on = duty / counter_size