ABI. See Application Binary Interface

(ABI)

Note: Page numbers followed by "f," "t," and "b" refer to figures, tables, and boxes, respectively; page numbers preceded by "e" refer to online material.

0, 5–6, 20. See also LOW, FALSE	Abstraction, 2–3	Advanced microarchitecture, 468-482
1, 5-6, 20. See also HIGH, TRUE	digital. See Digital abstraction	branch prediction. See Branch prediction
32-bit datapath, 394	Accumulator, 372	deep pipelines. See Deep pipelines
32-bit instructions, 332	Active low, 72–73	heterogeneous multiprocessors. See
64-bit architecture, 373	A/D conversion, 542.e37–39	Heterogeneous multiprocessors
74xx series logic, 543.e1–2	Ad hoc testing, 464	homogeneous multiprocessors. See
parts	ADCs. See Analog-to-digital converters	Homogeneous multiprocessors
2:1 mux (74157), 543.e4f	(ADCs)	micro-operations. See Microoperations
3:8 decoder (74138), 543.e4f	add instruction, 301, 444, 472–473	multiprocessors. See Multiprocessors
4:1 mux (74153), 543.e4 <i>f</i>	Adders, 237–244	multithreading. See Multithreading
AND (7408), 543.e3f	carry propagate, 238	out-of-order processor. See Out-of-
AND3 (7411), 543.e3f	carry-lookahead, 239-241	order processor
AND4 (7421), 543.e3f	full, 238	register renaming. See Register
counter (74161, 74163),	half, 238	renaming
543.e4 <i>f</i>	HDL for, 181–182, 198 <i>b</i> , 461 <i>b</i>	single instruction multiple data. See
FLOP (7474), 543.e3f	prefix, 241–243	Single instruction multiple
NAND (7400), 543.e3f	ripple-carry, 238-239	data (SIMD)
NOR (7402), 543.e3f	Addition, 12 <i>f</i> , 13 <i>b</i> , 16 <i>b</i> , 237–244, 301 <i>b</i> .	superscalar processor. See
NOT (7404), 543.e3f	See also Adders	Superscalar processor
OR (7432), 543.e3f	binary, 12-13	AHB. See Advanced High-performance
register (74377), 543.e4f	floating point, 261	Bus (AHB)
tristate buffer (74244), 543.e4f	signed binary, 13-17	AHB-Lite bus, 485
XOR (7486), 543.e3f	Address. See also Memory	Altera FPGA, 278
#define, 545.e5-6	physical, 521, 521f	ALU. See Arithmetic/logical unit (ALU)
#include, 545.e6-7. See also Standard	translation, 523-524	ALU Decoder, 408–409, 409t
libraries	virtual, 521. See also Virtual	ALUControl, 401-402, 457-458
	memory	ALUOp, 408
	Addressing modes, RISC-V, 341–342	ALUResult, 418
	base, 341	ALUSrc, 404
A	immediate, 341	AMAT. See Average memory access time
	PC-relative, 341–342	(AMAT)
	register, 341	AMBA. See Advanced Microcontroller

Advanced Micro Devices (AMD),

300

Bus Architecture (AMBA) AMD. See Advanced Micro Devices (AMD)

AMD64, 373	stored program, 343-344	ASICs. See Application-specific
Amdahl, Gene, 504	U/J-type instruction format, 338–340	integrated circuits (ASICs)
Amdahl's Law, 505	odds and ends, 355–363	Assembler, 344, 350–351
American Standard Code for	compressed instructions, 362-363	Assembler directives, 346–348
Information Interchange (ASCII),	endianness, 355–356	Assembling, 344–355
545.e8-9, 545.e27-28	exceptions, 356–360	Assembly language, RISC-V, 300–332
Analog I/O, 542.e31-39	floating-point instructions,	instructions, 301–302
A/D conversion, 542.e37–39	361–362	operands, 302–308
D/A conversion, 542.e31-34	signed and unsigned instructions,	translating high-level code to, 303–332
pulse-width modulation (PWM),	360–361	translating machine language to,
542.e34–37	programming, 308–332	342 <i>b</i> –343 <i>b</i>
Analog-to-digital converters (ADCs),	arrays, 317–320	Assembly language, x86. See x86
542.e31, 542.e37–39	branching, 311–313	Associativity
Analytical engine, 5	conditional statements, 313–315	in Boolean algebra, 60, 61t
and instruction, 309	function calls, 320–330	in caches, 505–511
AND gate, 18–19, 177 <i>b</i>	getting loopy, 315–317	Astable circuits, 117 <i>b</i>
chips (7408, 7411, 7421), 543.e3f	logical and arithmetic	Asymmetric multiprocessors. See
truth table, 18f, 20f	instructions, 308–311	Heterogeneous multiprocessors
using CMOS transistors, 31	memory, 306–308	Asynchronous circuits, 120–121
AND-OR (AO) gate, 45	pseudoinstructions, 330–332	Asynchronous resettable flip-flops
Anode, 25–26	x86 architecture, 366–374	definition, 114
Antidependence, 475	big picture, 373–374	HDL, 193 <i>b</i>
Application-specific integrated circuits	instruction encoding, 371–372	Asynchronous serial link, 542.e24. See
(ASICs), 543.e9	instructions, 369	also Universal Asynchronous
Architectural state, 344, 369	operands, 367–368	Receiver Transmitter (UART)
for RISC-V, 393–394	peculiarities, 372–373	Average memory access time (AMAT),
	registers, 366–367	503–505
Architecture, 299	0 ,	303–303
assembly language, 300-308	status flags, 369	303–303
assembly language, 300–308 instructions, 301–302	status flags, 369 Arguments, 320, 545.e24	B
assembly language, 300–308 instructions, 301–302 operands, 302–308	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22	
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading,	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22	
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic	В
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15	B -type instruction format. <i>See</i> S/B-type
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353 compilation, 348–350	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15 circuits, 237–256	B-type instruction format. <i>See</i> S/B-type instruction format
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353 compilation, 348–350 linking, 353–355	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15 circuits, 237–256 HDL operators, 183 <i>b</i>	B-type instruction format. See S/B-type instruction format Babbage, Charles, 5
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353 compilation, 348–350 linking, 353–355 loading, 355	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15 circuits, 237–256 HDL operators, 183 <i>b</i> RISC-V instructions, 309	B-type instruction format. See S/B-type instruction format Babbage, Charles, 5 Base addressing, 341
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353 compilation, 348–350 linking, 353–355 loading, 355 memory map, 344–346	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15 circuits, 237–256 HDL operators, 183 <i>b</i> RISC-V instructions, 309 Arithmetic/logical unit (ALU), 247–251	B-type instruction format. <i>See</i> S/B-type instruction format Babbage, Charles, 5 Base addressing, 341 Baud rate, 542.e24–25
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353 compilation, 348–350 linking, 353–355 loading, 355 memory map, 344–346 evolution of RISC-V architecture,	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15 circuits, 237–256 HDL operators, 183b RISC-V instructions, 309 Arithmetic/logical unit (ALU), 247–251 implementation of, 247–248	B-type instruction format. See S/B-type instruction format Babbage, Charles, 5 Base addressing, 341 Baud rate, 542.e24–25 BCD. See Binary coded decimal (BCD)
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353 compilation, 348–350 linking, 353–355 loading, 355 memory map, 344–346 evolution of RISC-V architecture, 363–366	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15 circuits, 237–256 HDL operators, 183b RISC-V instructions, 309 Arithmetic/logical unit (ALU), 247–251 implementation of, 247–248 in processor, 401–402, 409b	B-type instruction format. See S/B-type instruction format Babbage, Charles, 5 Base addressing, 341 Baud rate, 542.e24–25 BCD. See Binary coded decimal (BCD) Behavioral modeling, 188
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353 compilation, 348–350 linking, 353–355 loading, 355 memory map, 344–346 evolution of RISC-V architecture, 363–366 comparison of RISC-V and ARM	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15 circuits, 237–256 HDL operators, 183b RISC-V instructions, 309 Arithmetic/logical unit (ALU), 247–251 implementation of, 247–248 in processor, 401–402, 409b Arrays, 317–319, 545.e23–27	B-type instruction format. See S/B-type instruction format Babbage, Charles, 5 Base addressing, 341 Baud rate, 542.e24–25 BCD. See Binary coded decimal (BCD) Behavioral modeling, 188 Benchmarks, 397
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353 compilation, 348–350 linking, 353–355 loading, 355 memory map, 344–346 evolution of RISC-V architecture, 363–366 comparison of RISC-V and ARM architectures, 365–366	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15 circuits, 237–256 HDL operators, 183b RISC-V instructions, 309 Arithmetic/logical unit (ALU), 247–251 implementation of, 247–248 in processor, 401–402, 409b Arrays, 317–319, 545.e23–27 accessing, 316b, 545.e23	B-type instruction format. See S/B-type instruction format Babbage, Charles, 5 Base addressing, 341 Baud rate, 542.e24–25 BCD. See Binary coded decimal (BCD) Behavioral modeling, 188 Benchmarks, 397 beq instruction. See Branch if equal
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353 compilation, 348–350 linking, 353–355 loading, 355 memory map, 344–346 evolution of RISC-V architecture, 363–366 comparison of RISC-V and ARM architectures, 365–366 comparison of RISC-V and MIPS	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15 circuits, 237–256 HDL operators, 183b RISC-V instructions, 309 Arithmetic/logical unit (ALU), 247–251 implementation of, 247–248 in processor, 401–402, 409b Arrays, 317–319, 545.e23–27 accessing, 316b, 545.e23 bytes and characters, 317–320	B-type instruction format. See S/B-type instruction format Babbage, Charles, 5 Base addressing, 341 Baud rate, 542.e24–25 BCD. See Binary coded decimal (BCD) Behavioral modeling, 188 Benchmarks, 397 beq instruction. See Branch if equal (beq)
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353 compilation, 348–350 linking, 353–355 loading, 355 memory map, 344–346 evolution of RISC-V architecture, 363–366 comparison of RISC-V and ARM architectures, 365–366 comparison of RISC-V and MIPS architectures, 365	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15 circuits, 237–256 HDL operators, 183b RISC-V instructions, 309 Arithmetic/logical unit (ALU), 247–251 implementation of, 247–248 in processor, 401–402, 409b Arrays, 317–319, 545.e23–27 accessing, 316b, 545.e23 bytes and characters, 317–320 comparison or assignment of,	B-type instruction format. See S/B-type instruction format Babbage, Charles, 5 Base addressing, 341 Baud rate, 542.e24–25 BCD. See Binary coded decimal (BCD) Behavioral modeling, 188 Benchmarks, 397 beq instruction. See Branch if equal (beq) bge instruction. See Branch if greater
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353 compilation, 348–350 linking, 353–355 loading, 355 memory map, 344–346 evolution of RISC-V architecture, 363–366 comparison of RISC-V and ARM architectures, 365–366 comparison of RISC-V and MIPS architectures, 365 RISC-V base instruction sets and	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15 circuits, 237–256 HDL operators, 183b RISC-V instructions, 309 Arithmetic/logical unit (ALU), 247–251 implementation of, 247–248 in processor, 401–402, 409b Arrays, 317–319, 545.e23–27 accessing, 316b, 545.e23 bytes and characters, 317–320 comparison or assignment of, 545.e27–28	B-type instruction format. See S/B-type instruction format Babbage, Charles, 5 Base addressing, 341 Baud rate, 542.e24–25 BCD. See Binary coded decimal (BCD) Behavioral modeling, 188 Benchmarks, 397 beq instruction. See Branch if equal (beq) bge instruction. See Branch if greater than or equal (bge)
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353 compilation, 348–350 linking, 353–355 loading, 355 memory map, 344–346 evolution of RISC-V architecture, 363–366 comparison of RISC-V and ARM architectures, 365–366 comparison of RISC-V and MIPS architectures, 365 RISC-V base instruction sets and extensions, 364–365	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15 circuits, 237–256 HDL operators, 183b RISC-V instructions, 309 Arithmetic/logical unit (ALU), 247–251 implementation of, 247–248 in processor, 401–402, 409b Arrays, 317–319, 545.e23–27 accessing, 316b, 545.e23 bytes and characters, 317–320 comparison or assignment of, 545.e27–28 declaration, 319b, 545.e23	B-type instruction format. See S/B-type instruction format Babbage, Charles, 5 Base addressing, 341 Baud rate, 542.e24–25 BCD. See Binary coded decimal (BCD) Behavioral modeling, 188 Benchmarks, 397 beq instruction. See Branch if equal (beq) bge instruction. See Branch if greater than or equal (bge) Biased exponent, 258–259
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353 compilation, 348–350 linking, 353–355 loading, 355 memory map, 344–346 evolution of RISC-V architecture, 363–366 comparison of RISC-V and ARM architectures, 365–366 comparison of RISC-V and MIPS architectures, 365 RISC-V base instruction sets and extensions, 364–365 machine language, 332–344	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15 circuits, 237–256 HDL operators, 183b RISC-V instructions, 309 Arithmetic/logical unit (ALU), 247–251 implementation of, 247–248 in processor, 401–402, 409b Arrays, 317–319, 545.e23–27 accessing, 316b, 545.e23 bytes and characters, 317–320 comparison or assignment of, 545.e27–28 declaration, 319b, 545.e23 indexing, 317, 545.e23–27	B-type instruction format. See S/B-type instruction format Babbage, Charles, 5 Base addressing, 341 Baud rate, 542.e24–25 BCD. See Binary coded decimal (BCD) Behavioral modeling, 188 Benchmarks, 397 beq instruction. See Branch if equal (beq) bge instruction. See Branch if greater than or equal (bge) Biased exponent, 258–259 Big-endian memory, 355–356, 356f
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353 compilation, 348–350 linking, 353–355 loading, 355 memory map, 344–346 evolution of RISC-V architecture, 363–366 comparison of RISC-V and ARM architectures, 365–366 comparison of RISC-V and MIPS architectures, 365 RISC-V base instruction sets and extensions, 364–365 machine language, 332–344 addressing modes, 341–342	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15 circuits, 237–256 HDL operators, 183b RISC-V instructions, 309 Arithmetic/logical unit (ALU), 247–251 implementation of, 247–248 in processor, 401–402, 409b Arrays, 317–319, 545.e23–27 accessing, 316b, 545.e23 bytes and characters, 317–320 comparison or assignment of, 545.e27–28 declaration, 319b, 545.e23 indexing, 317, 545.e23–27 initialization, 545.e23b–e24b,	B-type instruction format. See S/B-type instruction format Babbage, Charles, 5 Base addressing, 341 Baud rate, 542.e24–25 BCD. See Binary coded decimal (BCD) Behavioral modeling, 188 Benchmarks, 397 beq instruction. See Branch if equal (beq) bge instruction. See Branch if greater than or equal (bge) Biased exponent, 258–259 Big-endian memory, 355–356, 356f Big-endian order in HDL, 176
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353 compilation, 348–350 linking, 353–355 loading, 355 memory map, 344–346 evolution of RISC-V architecture, 363–366 comparison of RISC-V and ARM architectures, 365–366 comparison of RISC-V and MIPS architectures, 365 RISC-V base instruction sets and extensions, 364–365 machine language, 332–344 addressing modes, 341–342 immediate encodings, 340–341	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15 circuits, 237–256 HDL operators, 183b RISC-V instructions, 309 Arithmetic/logical unit (ALU), 247–251 implementation of, 247–248 in processor, 401–402, 409b Arrays, 317–319, 545.e23–27 accessing, 316b, 545.e23 bytes and characters, 317–320 comparison or assignment of, 545.e27–28 declaration, 319b, 545.e23 indexing, 317, 545.e23–27 initialization, 545.e23b–e24b, 545.e24b, 545.e25	B-type instruction format. See S/B-type instruction format Babbage, Charles, 5 Base addressing, 341 Baud rate, 542.e24–25 BCD. See Binary coded decimal (BCD) Behavioral modeling, 188 Benchmarks, 397 beq instruction. See Branch if equal (beq) bge instruction. See Branch if greater than or equal (bge) Biased exponent, 258–259 Big-endian memory, 355–356, 356f Big-endian order in HDL, 176 Binary addition, 12–13. See also Adders;
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353 compilation, 348–350 linking, 353–355 loading, 355 memory map, 344–346 evolution of RISC-V architecture, 363–366 comparison of RISC-V and ARM architectures, 365–366 comparison of RISC-V and MIPS architectures, 365 RISC-V base instruction sets and extensions, 364–365 machine language, 332–344 addressing modes, 341–342 immediate encodings, 340–341 I-type instruction format, 334–336	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15 circuits, 237–256 HDL operators, 183b RISC-V instructions, 309 Arithmetic/logical unit (ALU), 247–251 implementation of, 247–248 in processor, 401–402, 409b Arrays, 317–319, 545.e23–27 accessing, 316b, 545.e23 bytes and characters, 317–320 comparison or assignment of, 545.e27–28 declaration, 319b, 545.e23 indexing, 317, 545.e23–27 initialization, 545.e23b–e24b, 545.e24b, 545.e25 as input argument, 545.e24b–25b,	B-type instruction format. See S/B-type instruction format Babbage, Charles, 5 Base addressing, 341 Baud rate, 542.e24–25 BCD. See Binary coded decimal (BCD) Behavioral modeling, 188 Benchmarks, 397 beq instruction. See Branch if equal (beq) bge instruction. See Branch if greater than or equal (bge) Biased exponent, 258–259 Big-endian memory, 355–356, 356f Big-endian order in HDL, 176 Binary addition, 12–13. See also Adders; Addition
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353 compilation, 348–350 linking, 353–355 loading, 355 memory map, 344–346 evolution of RISC-V architecture, 363–366 comparison of RISC-V and ARM architectures, 365–366 comparison of RISC-V and MIPS architectures, 365 RISC-V base instruction sets and extensions, 364–365 machine language, 332–344 addressing modes, 341–342 immediate encodings, 340–341 I-type instruction format, 334–336 interpreting, 342–343	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15 circuits, 237–256 HDL operators, 183b RISC-V instructions, 309 Arithmetic/logical unit (ALU), 247–251 implementation of, 247–248 in processor, 401–402, 409b Arrays, 317–319, 545.e23–27 accessing, 316b, 545.e23 bytes and characters, 317–320 comparison or assignment of, 545.e27–28 declaration, 319b, 545.e23 indexing, 317, 545.e23–27 initialization, 545.e23b–e24b, 545.e24b, 545.e25 as input argument, 545.e24b–25b, 545.e24	B-type instruction format. See S/B-type instruction format Babbage, Charles, 5 Base addressing, 341 Baud rate, 542.e24–25 BCD. See Binary coded decimal (BCD) Behavioral modeling, 188 Benchmarks, 397 beq instruction. See Branch if equal (beq) bge instruction. See Branch if greater than or equal (bge) Biased exponent, 258–259 Big-endian memory, 355–356, 356f Big-endian order in HDL, 176 Binary addition, 12–13. See also Adders; Addition Binary coded decimal (BCD), 260b
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353 compilation, 348–350 linking, 353–355 loading, 355 memory map, 344–346 evolution of RISC-V architecture, 363–366 comparison of RISC-V and ARM architectures, 365–366 comparison of RISC-V and MIPS architectures, 365 RISC-V base instruction sets and extensions, 364–365 machine language, 332–344 addressing modes, 341–342 immediate encodings, 340–341 I-type instruction format, 334–336 interpreting, 342–343 R-type instruction format, 332–334	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15 circuits, 237–256 HDL operators, 183b RISC-V instructions, 309 Arithmetic/logical unit (ALU), 247–251 implementation of, 247–248 in processor, 401–402, 409b Arrays, 317–319, 545.e23–27 accessing, 316b, 545.e23 bytes and characters, 317–320 comparison or assignment of, 545.e27–28 declaration, 319b, 545.e23 indexing, 317, 545.e23–27 initialization, 545.e23b–e24b, 545.e24b, 545.e25 as input argument, 545.e24b–25b, 545.e24 multi-dimensional, 545.e25–26	B-type instruction format. See S/B-type instruction format Babbage, Charles, 5 Base addressing, 341 Baud rate, 542.e24–25 BCD. See Binary coded decimal (BCD) Behavioral modeling, 188 Benchmarks, 397 beq instruction. See Branch if equal (beq) bge instruction. See Branch if greater than or equal (bge) Biased exponent, 258–259 Big-endian memory, 355–356, 356f Big-endian order in HDL, 176 Binary addition, 12–13. See also Adders; Addition Binary coded decimal (BCD), 260b Binary encoding, 127–128
assembly language, 300–308 instructions, 301–302 operands, 302–308 compiling, assembling, and loading, 344–355 assembling, 350–353 compilation, 348–350 linking, 353–355 loading, 355 memory map, 344–346 evolution of RISC-V architecture, 363–366 comparison of RISC-V and ARM architectures, 365–366 comparison of RISC-V and MIPS architectures, 365 RISC-V base instruction sets and extensions, 364–365 machine language, 332–344 addressing modes, 341–342 immediate encodings, 340–341 I-type instruction format, 334–336 interpreting, 342–343	status flags, 369 Arguments, 320, 545.e24 pass by reference, 545.e22 pass by value, 545.e22 Arithmetic C operators, 545.e11–15 circuits, 237–256 HDL operators, 183b RISC-V instructions, 309 Arithmetic/logical unit (ALU), 247–251 implementation of, 247–248 in processor, 401–402, 409b Arrays, 317–319, 545.e23–27 accessing, 316b, 545.e23 bytes and characters, 317–320 comparison or assignment of, 545.e27–28 declaration, 319b, 545.e23 indexing, 317, 545.e23–27 initialization, 545.e23b–e24b, 545.e24b, 545.e25 as input argument, 545.e24b–25b, 545.e24	B-type instruction format. See S/B-type instruction format Babbage, Charles, 5 Base addressing, 341 Baud rate, 542.e24–25 BCD. See Binary coded decimal (BCD) Behavioral modeling, 188 Benchmarks, 397 beq instruction. See Branch if equal (beq) bge instruction. See Branch if greater than or equal (bge) Biased exponent, 258–259 Big-endian memory, 355–356, 356f Big-endian order in HDL, 176 Binary addition, 12–13. See also Adders; Addition Binary coded decimal (BCD), 260b

Binary numbers	commutativity, 60	conditional statements. See
signed, 13–17	complements, 60	Conditional statements
unsigned, 7–9	consensus, 60	control-flow statements. See Control
Binary to decimal conversion, 8b, 9f	covering, 60	flow statements
Binary to hexadecimal conversion, $10b$	De Morgan's, 61	data types. See Data types
Bipolar junction transistors, 24	distributivity, 60	executing a program, 545.e3
Bipolar motor drive, 542.e61f	idempotency, 60	function calls. See Function calls
Bipolar signaling, 542.e25	identity, 59	loops. See Loops
Bipolar stepper motor, 542.e59f,	involution, 60	operators. See Operators
542.e60–63	null element, 59–60	simple program, 545.e3
AIRPAX LB82773-M1, 542.e62f	Branch if equal (beq), 311	standard libraries. See Standard
direct drive current, 542.e62f	Branch if greater than or equal (bge),	libraries
Bistable element, 107–108	311, 316 <i>b</i>	variables. See Variables in C
Bit, 6	Branch if less than (blt), 360	Caches, 505–520
dirty, 519	Branch if not equal (bne), 311–312	address fields
least significant, 11, 12f	Branch instructions, 311	block offset, 513
most significant, 11, 12f	Branch misprediction penalty, 451, 470	byte offset, 508
sign, 13–14	Branch prediction, 470–472	set bits, 508
use, 515–516	Branch target address (BTA), 337,	tag, 508
valid, 509	430–431, 432 <i>f</i>	advanced design, 516-520
Bit cells, 267	Branch target buffer, 470–471	multiple level, 516–518
DRAM, 268–269	Branching, 311–313	organizations, 515–516
ROM, 268	conditional, 311–312	direct mapped, 507–511
SRAM, 269	unconditional, see Jump	fully associative, 512
Bit swizzling, 186	Breadboards, 543.e20	multi-way set associative,
Bitline, 267	BTA. See Branch target address (BTA)	511–512
Bitwise operators, 175–176	Bubble, 18, 61–62	parameters
Block, 505	pushing, 61–62, 67–68	block size (<i>b</i>), 513–514
Block offset, 513–514	Bubble, in pipeline, 448	capacity (C), 505
Block size (b), 505–506	Buffers, 18	degree of associativity (N), 505
Blocking and nonblocking assignments,	lack of, 115	number of blocks (B) , 505,
197, 203–207	tristate, 72, 73 Bugs, 173–174	512–514
blt instruction. See Branch if less than (blt)	in C code, 545.e44–48	number of sets (S) , 505
BlueSMiRF silver module, 542.e53–54	Bus, 54	performance of
Bluetooth wireless communication,	tristate, 73f	capacity, 518
542.e53–54	Bypassing, 446. See also Forwarding	compulsory, 518
BlueSMiRF silver module, 542.e53–54	Byte, 11–12, 317–320. <i>See also</i>	conflict, 512, 518
classes, 542.e53t	Characters	hit, 502
bne instruction. See Branch if not equal	least significant, 11	hit rate, 503–505
(bne)	most significant, 11	miss, 502, 518
Boole, George, 6	Byte offset, 508	miss rate, 503–505
Boolean algebra, 58–64	Byte-addressable memory, 306–307	miss rate <i>vs.</i> cache parameters, 518–519
axioms, 59 equation simplification, 63–64	big-endian, 355	
theorems, 59–62	little-endian, 355	penalty, 513 reducing, 518–519
Boolean equations, 56–58	nene chami, ooo	replacement policy, 527–529
product-of-sums (POS) form, 58		status bits
sum-of-products (SOP) form, 56–58	C	dirty bit (D), 528
Boolean logic, 6. See also Boolean		use bit (U), 528–529
algebra; Logic gates		valid bit (V), 525
Boolean theorems, 59–62	C programming, 545.e1–48	write policy, 519–520
associativity, 60	common mistakes. See Common	write-back, 519, 519 <i>b</i>
combining, 60	mistakes in C	write-through, 519, 519b
combining, oo	iniotaico iii O	write through, 317, 3170

CAD. See Computer-aided design (CAD)	CISC. See Complex instruction set	Complements theorem, 60
Callee, 320	computer	Complex instruction set computer
Callee save rule, 326	CLA. See Carry-lookahead adder (CLA)	(CISC) architectures, 302, 366,
Callee-saved registers, 325	CLBs. See Configurable logic blocks	469–470
Caller save rule, 326	(CLBs)	Complexity management, 2-5
Caller-saved registers, 325	Clock cycles per instruction (CPI). See	abstraction, 2–3
Canonical form. See Sum-of-products	Cycles per instruction (CPI)	discipline, 3–4
(SOP) form; Product-of-sums	Clock period, 140, 398	hierarchy, 4
(POS) form	Clock skew, 146–149, 468–469	modularity, 4
Capacitors, 26	Clustered multiprocessors, 481–482	regularity, 4
Capacity, of cache, 505	CMOS. See Complementary Metal-	Compressed instructions, 362–363
Capacity miss, 518	Oxide-Semiconductor gates	Compulsory miss, 518
Carry propagate adder (CPA). See	(CMOS)	Computer-aided design (CAD), 127,
Carry-lookahead adder (CLA);	Combinational composition, 54–55	171, 246
Prefix adders; Ripple-carry adder	Combinational logic, 172b	Concurrent signal assignment statement
Carry-lookahead adder (CLA), 239–241,	design, 53–56	177, 182
240 <i>f</i>	Boolean algebra, 58–64	Condition flags, 369
case statement, in HDL, 199–200. See	Boolean equations, 56–58	Condition mnemonics, 332
also Switch/case statement	building blocks, 81–86	Conditional assignment, 179–180
casez, case?, in HDL, $203b$	delays, 86–90	Conditional branches, 311, 312 <i>b</i>
Cathode, 25–26	don't cares, 79–80	Conditional operator, 179
Cathode ray tube (CRT), 542.e47–48.	Karnaugh maps (K-maps), 73–81	Conditional signal assignments, 179
See also VGA (Video Graphics	multilevel, 67–71	Conditional statements, 313–315
Array) monitor	precedence, 56	in RISC-V assembly
horizontal blanking interval,	timing, 86–93	if, 313
542.e47–48	two-level, 67–68	if/else, 313-314
vertical blanking interval, 542.e47–48	X (contention). See Contention	switch/case, 314-315
Character LCDs, 542.e44–47	(X)	in C, 545.e17–19
Characters (char), 317–319, 542.e44–47	X (don't cares). See Don't care	if, 545.e17
arrays. See also Strings	(X)	if/else, 545.e1 7
C type, 545.e27	Z (floating). See Floating (Z)	switch/case, 545.e18
Chips, 26	HDLs. See Hardware description	in HDL, 199–200
multiprocessors, 479–482	languages (HDLs)	case, 199–200
Chopper constant current drive, 542.e62	Combining theorem, 60	casez, case?, 203
Circuits	Command line arguments, 545.e44	if, if/else, 200–203
74xx series. See 74xx series logic	Comments	Configurable logic blocks (CLBs), 167,
application-specific integrated	in RISC-V assembly, 302	278. See also Logic elements (LEs
(ASICs), 543.e9	**	Conflict miss, 518
astable, 117 <i>b</i>	in C, 302, 545.e5	Consensus theorem, 60, 62 <i>b</i>
The state of the s	in SystemVerilog, 178	
asynchronous, 120–121	in VHDL, 178	Constants
combinational. See Combinational	Common mistakes in C, 545.e44–48	in RISC-V assembly, 302–308. See also Immediates
logic	Comparators, 245–246	
definition of, 53–54	Comparison	in C, 545.e5–6
delay, 86–90	in hardware. See Arithmetic/logical	Contamination delay, 86–90. See also
glitches in, 90–93	unit (ALU); Comparators	Short path
multiple-output, 66b	processor performance, 397–398	Contention (x), 67b, 71–72
priority, 66	using ALU, 249	Context switching, 478
sequential. See Sequential logic	Compiler, in C, 348–350, 545.e4,	Continuous assignment statements, 177,
synchronous, 120–121	545.e43	191
synchronous sequential, 121	Complementary Metal-Oxide-	Control signals, 81, 399, 406f, 407, 410
synthesized, 174 <i>f</i> , 176 <i>f</i> , 177 <i>f</i>	Semiconductor gates (CMOS),	Control signals, 81, 399, 406 <i>f</i> , 407–410
111111111111111111111111111111111111111	/. I= 1/.	+/./ + 11

Control unit, 394. See also ALU	Datapath	Digital circuits. See Logic
Decoder; Main Decoder; Instr	multicycle processor, 416–438	Digital signal processors (DSPs), 254, 257b
Decoder	I-type ALU instructions, 433–434	Digital system implementation,
of multicycle RISC-V processor,	jal instruction, 433–434	543.e1–37
422–432	w instruction, 417–419	74xx series logic. See 74xx series logic
of pipelined RISC-V processor,	R-type instructions, 421	application-specific integrated
439–456	sw instruction, 420–421	circuits (ASICs), 543.e9
of single-cycle RISC-V processor,	pipelined processor, 441–443	assembly of, 543.e19–23
398–415	single-cycle processor, 399–407	breadboards, 543.e20
Control-flow statements	I-type ALU instructions, 410–411	datasheets, 543.e9–13
conditional statements. See	jal instruction, 411–412	economics, 543.e35–37
Conditional statements	w instruction, 400–402	logic families, 543.e15–16
loops. See Loops	R-type instructions, 404–405	packaging, 543.e19–23
CoreMark, 397	sw instruction, 403–404	printed circuit boards, 543.e20–23
Counters, 261–263	Datasheets, 543.e9–13	programmable logic, 543.e2-9
divide-by-3, 129 <i>t</i>	DC motors, 542.e55–59	Digital-to-analog converters (DACs),
Covering theorem, 60	H-bridge, 542.e55–58, 542.e56 <i>t</i>	542.e31–34
CPA. See Carry propagate adder (CPA)	shaft encoder, 542.e58 <i>f</i> , 542.e54–55,	DIMM. See Dual inline memory module
CPI. See Cycles per instruction (CPI)	542.e58–59	(DIMM)
Critical path, 87–88, 412–414, 414 <i>f</i>	DC transfer characteristics, 22, 23f,	Diodes, 25–26
Cross-coupled inverters, 108, 269	45f. See also Direct current (DC)	p-n junction, 26f
bistable operation of, 108f	transfer characteristics; Noise	DIPs. See Dual-inline packages (DIPs)
Cycle time. See Clock period	margins (DDD)	Direct current (DC) transfer
Cycles per instruction (CPI), 398, 413,	DDR. See Double-data rate memory (DDR)	characteristics, 22
437, 454, 468	De Morgan, Augustus, 61b	Direct mapped cache, 506–511
Cyclic paths, 118	De Morgan's theorem, 61	Direct voltage drive, 542.e63
Cyclone IV FPGA, 278–283	DE-9 cable, 542.e26 <i>f</i>	Dirty bit (D), 519, 528
	Decimal numbers, 7	Discipline
	Decimal to binary conversion, 9b	dynamic, 140. See also Timing
D	Decimal to hexadecimal conversion, 11b	analysis
	Decode stage, 439	static, 140. See also Noise margins
	Decoders definition of, 84–86	Discrete-valued variables, 5
D flip flore See Flip flore	HDL for	Distributivity theorem, 60
D flip-flops. <i>See</i> Flip-flops D latch. <i>See</i> Latches	behavioral, 200 <i>b</i>	Divide-by-3 counter
D/A conversion, 542.e31–34	parameterized, 217 <i>b</i>	design of, 127, 128 <i>f</i> , 128 <i>t</i> , 129 <i>f</i> HDL for, 208 <i>b</i>
DACs. See Digital-to-analog converters	logic using, 85–86	Divider, 255–256
(DACs)	seven-segment. See Seven-segment	Division
Data hazard, 446–450	display decoder	circuits, 254–256
Data memory, 395, 467 <i>b</i>	Deep pipelines, 468–469	Do/while loops, in C, 545.e19
Data segment, 345–346	Delay, logic gates. See also Propagation	Don't care (X), 66–67, 79–80, 203
Data types, 545.e21–35	delay, Contamination Delay	Dopant atoms, 25
arrays. See Arrays	in HDL (simulation only), 186–187	Double, C type, 545.e8t
characters. See Characters (char)	DeleteUser function, 545.e33	Double-precision formats, 259–260
dynamic memory allocation. See	Dennard, Robert, 268b	DRAM. See Dynamic random access
Dynamic memory allocation	Destination register (rd), 333	memory (DRAM)
(malloc, free)	Device driver, 542.e3, 542.e10–14	Dual-inline packages (DIPs), 26b, 543.e1
linked list. See Linked list	Device under test (DUT), 218	DUT. See Device under test (DUT)
pointers. See Pointers	Dhrystone, 397	Dynamic branch predictors, 470–471
strings. See Strings	Dice, 26	Dynamic data segment, 346
structures. See Structures (struct)	Dielectric, 27	Dynamic discipline, 140. See also Timing
typedef, 545.e31	Digital abstraction, 5-7, 20-24	analysis

Ethernet, 73, 542.e15

Exceptions, 356–360 back-to-back, 111, 143-146, 195. Dynamic memory allocation (malloc, free), 545.e40 exception-related instructions, 358 See also Synchronizers Dynamic power, 32 execution modes and privilege levels, comparison with latches, 116–117 Dynamic random access memory 356-357 enabled, 113-114 (DRAM), 266, 268–269, 268f handler, 357-358 HDL for, 451. See also Registers Execution time, 397 metastable state of. See Metastability exit, 545.e41 register, 112–113 Extended instruction pointer (EIP), 367 resettable, 114 Е scannable, 265 shift register, 169 transistor count, 112b F transistor-level, 114-116 Economics, 543.e35-37 Float, C type, 545.e6 Edge-triggered flip-flop. See Flip-flops print formats of, 545.e36t EEPROM. See Electrically erasable factorial function call, 327-329 programmable read only memory Floating (Z), 72-73stack during, 329 Floating output node, 115 (EEPROM) EFLAGS register, 369 Factoring state machines, 132–135 Floating-gate transistor, 272. See also False, 6, 18, 56–58, 58f, 109–114 Flash memory EIP. See Extended instruction pointer (EIP) Fast Fourier Transform (FFT), 257b Floating-point division (FDIV) Electrically erasable programmable read FDIV. See Floating-point division bug, 174, 261b only memory (EEPROM), 272 Embedded I/O (input/output) systems, (FDIV) Floating-point instructions, 361–362 FE310-G002 system-on-chip, 542.e5 Floating-point numbers, 257–261 542.e1-43 A/D conversion, 542.e37-39 FFT. See Fast Fourier Transform (FFT) addition, 261 Field programmable gate arrays formats, single-and double-precision, analog I/O, 542.e31-39 (FPGAs), 542.e23f, 542.e49f, quad-precision, 259-260 D/A conversion, 542.e31-34 276, 543.e7-9 digital I/O, 542.e5-10 in programming. See Double, C type; general-purpose I/O (GPIO), driving VGA cable, 542.e49f Float, C type in SPI interface, 542.e19, 542.e19-20 rounding, 260-261 542.e5-10 File manipulation, in C, 545.e38–39 interrupts, 542.e39-43 special cases Finite state machines (FSMs), 121-139, infinity, 259 LCDs. See Liquid Crystal Displays 207-209, 423 NaN, 259 (LCDs) microcontroller peripherals, complete multicycle control, 434f Floating-point unit (FPU), 261b 542,e43 deriving from circuit, 135*b*–138*b* For loops, 315–316, 545.e20 divide-by-3 FSM, 127b-128b, 208b Format conversion (atoi, atol, atof), motors. See Motors serial I/O, 542.e14-29 factoring, 132–135 545.e41 in HDL, 207-209 Forwarding, 446-448. See also timers, 542.e29-31 LE configuration for, 280*b*–281*b* Hazards VGA monitor. See VGA (Video Mealy FSM, 130–132 FPGAs. See Field programmable gate Graphics Array) monitor Enabled flip-flops, 113-114 Moore FSM, 130–132 arrays (FPGAs) snail/pattern recognizer FSM, FPU. See Floating-point unit (FPU) Enabled registers, 194. See also 130*b*–131*b*, 210*b* Frequency shift keying (FSK), 542. Flip-flops e53-54 state encodings, 127-128. See also Endianness, 355–356 Binary encoding; One-cold and GFSK waveforms, 542.e53f EPROM. See Erasable programmable encoding; One-hot encoding Front porch, 542.e48 read only memory (EPROM) Equality comparator, 245 state transition diagram, 122f, 123f FSK. See Frequency shift keying (FSK) traffic light FSM, 121-127 FSMs. See Finite state machines (FSMs) Equation minimization Fixed-point numbers, 256–257 Full adder, 54, 180–181, 182b, 198b, using Boolean algebra, 63b using Karnaugh maps. See Karnaugh Flags, 248 238 Flash memory, 272. See also Solid state using always/process statement, 238 maps (K-maps) drive (SSD) Fully associative cache, 512 Erasable programmable read only memory (EPROM), 543.e2 Flip-flops, 112, 112–113, 113–114, 114, funct3 field, 333b, 334 114-116, 191. See also Registers funct7 field, 332b, 333

E		II
Function calls, 320–330, 545.e15–16 additional arguments and local	Н	Hazard unit, 446–448 Hazards. <i>See also</i> Hazard unit
variables, 330		control hazards, 446, 450–452
arguments, 330		data hazards, 446–448
leaf, 326	Half adder, 238	pipelined processor, 443–454
multiple registers, loading and	Hard disk, 502-504. See also Hard drive	read after write (RAW), 444, 475
storing, 365–366	Hard drive, 502, 520. See also Hard	solving
naming conventions, 545.e16	disk; Solid state drive (SSD);	control hazards, 450–452
with no inputs or outputs, 320–321,	Virtual memory	forwarding, 446–448
545.e15	Hardware description languages	stalls, 448–450
nonleaf, 326–327	(HDLs), 171–223. See also	write after read (WAR), 475
preserved registers, 324–326	SystemVerilog; VHDL (VHSIC	write after write (WAW), 476
prototypes, 545.e16	Hardware Description Language)	H-bridge control, 542.e56f
recursive, 327–329	2:1 multiplexer, 463 <i>b</i>	HDL. See Hardware description
return, 320–321, 545.e15	adder, 461 <i>b</i>	languages (HDLs); SystemVerilog;
stack, use of, 322-324. See also	combinational logic, 172 <i>b</i> , 175–188	VHDL
Stack	bitwise operators, 175–176 blocking and nonblocking	Heap, 346
Fuse-programmable ROM, 271	assignments, 203–207	Heterogeneous multiprocessors,
	case statements, 199–200	480–481
	conditional assignment, 179–180	Hexadecimal numbers, 9-11
0	delays, 186–187	Hexadecimal to binary and decimal
G	data memory, 467 <i>b</i>	conversion, $9b$
	data types, 211–215	Hierarchy, 4
	flip-flop, 191–192, 192 <i>b</i>	HIGH, 6
Gates	history of, 172–173	High-level programming languages, 308,
AND, 18–19, 31 <i>f</i>	If statements, 200–203	545.e5
buffer, 18	internal variables, 180-182	compiling, assembling, and loading,
multiple-input, 19–20	numbers, 183	344–355
NAND, 18, 29–30, 30 <i>f</i>	operators and precedence,	translating into assembly, 304b
NOR, 19, 30 <i>f</i> , 109–110	182–183, 183 <i>b</i>	High-performance microprocessors,
NOT, 18, 29 <i>f</i>	reduction operators, 178	468
OR, 19	immediate extension, 430–431	Hit, 502
transistor-level. See Transistors	instruction memory, 466 <i>b</i> –467 <i>b</i>	Hit rate, 503–505
XNOR, 19 <i>b</i>	modules, 171–172	Hold time constraint, 142–143
XOR, 19 General-purpose I/O (GPIO), 542.e5–10	parameterized modules, 215–218	with clock skew, 146–149 Hold time violations, 143, 143–144,
switches and LEDs example, 542.	processor building blocks, 461–464	145 <i>b</i> –146 <i>b</i> , 148 <i>b</i> –149 <i>b</i>
e13 <i>b</i> –14 <i>b</i>	register file, 461b	Homogeneous multiprocessors, 479–480
Generate signal, 239–241	resettable flip-flop, 192–194, 193 <i>b</i> , 194 <i>f</i> , 462 <i>b</i>	Hopper, Grace, 346b
GenWaves function, 542.e33–34	resettable flip-flop with enable,	Tropper, Grace, 5 100
Glitches, 90–93	194–195, 194 <i>b</i> , 195 <i>f</i> , 463 <i>b</i>	
Global data segment, 345	sequential logic, 191–196, 207	1
GND. See Ground (GND)	simulation and synthesis, 173–175	
GPIO. See General-purpose I/O (GPIO)	single-cycle RISC-V processor,	
GPUs. See Graphics processing units	456–467	I-type instruction format, 334–336
(GPUs)	structural modeling, 188–190	I/O. See Input/output (I/O) systems
Graphics accelerators, 480–481	testbench, 218–222, 464–468	IA-32 architecture. See x86
Graphics processing units (GPUs), 472	top-level module, 466b	IA-64, 370 <i>t</i>
Gray, Frank, 74b	Hardware handshaking, 542.e25	ICs. See Integrated circuits (ICs)
Gray codes, 74b	Hardware multithreaded processor, 479	Idempotency theorem, 60
Ground (GND), 20	Hardware reduction, 68-69. See also	Identity theorem, 59
symbol for, 29	Equation minimization	Idioms, 175

IEEE. See Institute of Electrical and Electronics Engineers (IEEE) If statements in C, 545.e17 in HDL, 200–203 in RISC-V assembly, 313, 313b If/else statements, 308 in C, 545.e17 in HDL, 200–203 in RISC-V assembly, 314b ILP. See Instruction level parallelism (ILP) IM. See Instruction memory Immediate addressing, 341 Immediate encodings, 340–341	Instruction register (IR), 416–417, 423–424 Instruction set, 299. See also Architecture Instructions, RISC-V, 299 branch instructions, 311 branching, 311–313 logical, 309 multiply instructions, 310–311 shift instructions, 309–310 Instructions, x86, 366–374 Instructions per cycle (IPC), 398, 472 Integrated circuits (ICs), 543.e19 Intel. See x86	with "don't cares", 79–80 logic minimization using, 73–81 prime implicants, 75–79 seven-segment display decoder, 77b–79b KB. See Kilobyte (KB) Kib. See Kibibit (Kib/Kibit) KiB. See Kibibyte (KiB) Kibibit (Kib/Kibit), 12 Kibibyte (KiB), 12 Kilobit (Kb/Kbit), 12 Kilobyte (KB), 12 Kilobyte (KB), 12
Immediate extension, 406 <i>b</i> , 412 <i>b</i> Immediate field (imm), 334–336 Immediate instructions (I-type instructions), <i>see</i> I-type	Intel processors, 366 Intel x86. See x86 Interrupts, 356, 542.e39–43 Invalid logic level, 184	L
instruction format Immediates, 304–306, 365–366. See also Constants Implicit leading one, 258 Information, amount of, 6	Inverters, 18, 117, 176b. See also NOT gate cross-coupled, 107–108, 108f in HDL, 176b, 196–197 Investigation of the Laws of Thought,	LAB. See Logic array block (LAB) Language. See Instructions assembly, 300–308 machine, 332–344 mnemonic, 301
Initializing arrays in C, 545.e23 <i>b</i> , 545.e24 <i>b</i> , 545.e24 <i>b</i> variables in C, 545.e11	An (Boole), 6 Involution theorem, 60 IOEs. See Input/output elements (IOEs) IPC. See Instructions per cycle (IPC)	Last-in-first-out (LIFO) queue, 322. See also Stack Latches, 109–111 comparison with flip-flops, 107–108,
Input/Output (I/O) systems, 542.e1–43 device driver, 542.e3, 542.e10–14 embedded I/O systems. <i>See</i> Embedded I/O (input/output)	IR. See Instruction register (IR) IRWrite, 416–417, 423–424	116–117 D, 111–112 SR, 109–111 transistor-level, 114–116
systems I/O registers, 542.e3 memory-mapped I/O, 542.e1–3	J	Latency, 155, 439, 448 Lattice, silicon, 25f, 31 LCDs. See Liquid crystal displays (LCDs)
personal computer I/O systems. See Personal computer (PC) I/O systems Input/output elements (IOEs), 278 Institute of Electrical and Electronics Engineers (IEEE), 173–174, 258 Instr Decoder, 423	j instruction, 312, 313 <i>b</i> J-type instruction format. <i>See</i> U/J-type instruction format jal instruction, 320–321 jalr instruction, 321 Java, 308. <i>See also</i> Language	Leaf function, 326 Leakage current, 33–34 Least recently used (LRU) replacement, 515 two-way associative cache with, 515–516, 515f Least significant bit (lsb), 11, 12f Least significant byte (LSB), 11, 12f,
Instruction Decoder. <i>See</i> Instr Decoder Instruction encoding, x86, 369, 370 <i>t</i> Instruction formats, RISC-V, 332–340 I-type, 334–336	jr instruction, 320–321 Jump instruction. See j instruction	306–307 LEDs. See Light-emitting diodes (LEDs) LEs. See Logic elements (LEs) Level-sensitive latch. See Latches
R-type, 332–334 S/B-type, 336–338 U/J-type, 338–340 Instruction formats, x86, 369	K	LIFO. See Last-in-first-out (LIFO) queue Light-emitting diodes (LEDs), 542.e7, 543.e18–19 Line options, compiler and command,
Instruction level parallelism (ILP), 476 Instruction memory, 395, 440–441, 466 <i>b</i> –467 <i>b</i>	K-maps. See Karnaugh maps (K-maps) Karnaugh, Maurice, 73–74 Karnaugh maps (K-maps), 73–81, 92	348–350, 545.e43–44 Linked list, 545.e33 Linker, 344, 353

Linking, 344	Logic synthesis, 174–175	Max-delay constraint. See Setup time
Linux, 545.e4	Logical instructions, 309	constraint
Liquid crystal displays (LCDs), 542.	Logical shifter, 252	Maxterms, 56
e43–44	Lookup tables (LUTs), 82–83, 273	Mb. See Megabit (Mb/Mbit), Mebibit
Literal, 56, 94	Loops, 315–317, 545.e19–20	(Mib/Mibit)
loading, 344–355	in C	Mbit. See Megabit (Mb/Mbit), Mebibit
Little-endian bus order in HDL, 176	for, 545.e20	(Mib/Mibit)
Little-endian memory addressing, 356	do/while, 545.e19	MCUs. See Microcontroller units (MCUs)
Load word (Tw), 417–419	while, 545.e19	Mealy machines, 121, 121 <i>f</i> , 130–132
Loading literals, 345	in RISC-V assembly	state transition and output table, 132 <i>t</i>
Loads. See Load word (\lambda w)	for, 315–316	state transition diagrams, 131 <i>f</i>
Local variables, 330	while, 315	timing diagrams for, 133 <i>f</i>
Locality, 500	Lovelace, Ada, 343 <i>b</i>	Mean time between failure (MTBF), 151
The state of the s		Mebibit (Mib/Mibit), 12
Logic	LOW, 6	* **
bubble pushing, 69–71	Low Voltage CMOS Logic (LVCMOS),	Medium-scale integration (MSI) chips,
combinational. See Combinational	23	543.e2
logic	Low Voltage TTL Logic (LVTTL), 23	Megabit (Mb/Mbit), 12. See also
families, 23, 543.e10, 543.e15–16	lsb. See Least significant bit (lsb)	Mebibit (Mib/Mibit)
gates. See Gates	LSB. See Least significant byte (LSB)	Memory, 317. See also Memory arrays
hardware reduction, 68-69	LUTs. See Lookup tables (LUTs)	access time, 503–505
multilevel. See Multilevel	LVCMOS. See Low Voltage CMOS	addressing modes, 306–308, 368 <i>t</i>
combinational logic	Logic (LVCMOS)	area and delay, 269-270
programmable, 543.e2-9	LVTTL. See Low Voltage TTL Logic	big-endian, 355
sequential. See Sequential logic	(LVTTL)	byte-addressable, 306-307, 307 <i>b</i> , 355
transistor-level. See Transistors	w instruction, 417–419	bytes and characters, 317-320
two-level, 67–68		HDL for, 313b, 317f, 466b–467b
Logic array block (LAB), 279		hierarchy, 502f
Logic array block (LAB), 279 Logic arrays, 275–284. <i>See also</i> Field		hierarchy, 502 <i>f</i> little-endian, 356
Logic arrays, 275–284. <i>See also</i> Field programmable gate arrays (FPGAs)	M	
Logic arrays, 275-284. See also Field	M	little-endian, 356
Logic arrays, 275–284. <i>See also</i> Field programmable gate arrays (FPGAs)	M	little-endian, 356 logic using, 272–273
Logic arrays, 275–284. <i>See also</i> Field programmable gate arrays (FPGAs) transistor-level implementation,	MAC. See Multiply-accumulate (MAC)	little-endian, 356 logic using, 272–273 main, 502
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284		little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284 Logic elements (LEs), 278	MAC. See Multiply-accumulate (MAC)	little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311 physical, 521
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284 Logic elements (LEs), 278 of Cyclone IV, 278f, 279 functions built using, 280b–281b	MAC. See Multiply-accumulate (MAC) Machine code. See Machine language Machine language, 332–344	little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311 physical, 521 ports, 267
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284 Logic elements (LEs), 278 of Cyclone IV, 278f, 279	MAC. See Multiply-accumulate (MAC) Machine code. See Machine language	little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311 physical, 521 ports, 267 protection, 527. See also Virtual memory
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284 Logic elements (LEs), 278 of Cyclone IV, 278f, 279 functions built using, 280b–281b Logic families, 23, 543.e10, 543.e15–16 compatibility of, 24t	MAC. See Multiply-accumulate (MAC) Machine code. See Machine language Machine language, 332–344 addressing modes, 341–342 interpreting, 342–343	little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311 physical, 521 ports, 267 protection, 527. See also Virtual memory types, 267–268
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284 Logic elements (LEs), 278 of Cyclone IV, 278f, 279 functions built using, 280b–281b Logic families, 23, 543.e10, 543.e15–16 compatibility of, 24t logic levels of, 23	MAC. See Multiply-accumulate (MAC) Machine code. See Machine language Machine language, 332–344 addressing modes, 341–342 interpreting, 342–343 I-type instructions, 334–336	little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311 physical, 521 ports, 267 protection, 527. See also Virtual memory types, 267–268 DDR, 269–270 DRAM, 269–270
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284 Logic elements (LEs), 278 of Cyclone IV, 278f, 279 functions built using, 280b–281b Logic families, 23, 543.e10, 543.e15–16 compatibility of, 24t logic levels of, 23 specifications, 543.e17t	MAC. See Multiply-accumulate (MAC) Machine code. See Machine language Machine language, 332–344 addressing modes, 341–342 interpreting, 342–343 I-type instructions, 334–336 R-type instructions, 332–334	little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311 physical, 521 ports, 267 protection, 527. See also Virtual memory types, 267–268 DDR, 269–270 DRAM, 269–270 flash, 272
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284 Logic elements (LEs), 278 of Cyclone IV, 278f, 279 functions built using, 280b–281b Logic families, 23, 543.e10, 543.e15–16 compatibility of, 24t logic levels of, 23 specifications, 543.e17t Logic gates, 17–20, 543.e1	MAC. See Multiply-accumulate (MAC) Machine code. See Machine language Machine language, 332–344 addressing modes, 341–342 interpreting, 342–343 I-type instructions, 334–336 R-type instructions, 332–334 S/B-type instructions, 336–338	little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311 physical, 521 ports, 267 protection, 527. See also Virtual memory types, 267–268 DDR, 269–270 DRAM, 269–270 flash, 272 register file, 270–271
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284 Logic elements (LEs), 278 of Cyclone IV, 278f, 279 functions built using, 280b–281b Logic families, 23, 543.e10, 543.e15–16 compatibility of, 24t logic levels of, 23 specifications, 543.e17t Logic gates, 17–20, 543.e1 AND. See AND gate	MAC. See Multiply-accumulate (MAC) Machine code. See Machine language Machine language, 332–344 addressing modes, 341–342 interpreting, 342–343 I-type instructions, 334–336 R-type instructions, 332–334 S/B-type instructions, 336–338 stored program, 343–344, 343f	little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311 physical, 521 ports, 267 protection, 527. See also Virtual memory types, 267–268 DDR, 269–270 DRAM, 269–270 flash, 272 register file, 270–271 ROM, 271–272
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284 Logic elements (LEs), 278 of Cyclone IV, 278f, 279 functions built using, 280b–281b Logic families, 23, 543.e10, 543.e15–16 compatibility of, 24t logic levels of, 23 specifications, 543.e17t Logic gates, 17–20, 543.e1 AND. See AND gate AND-OR (AO) gate, 45	MAC. See Multiply-accumulate (MAC) Machine code. See Machine language Machine language, 332–344 addressing modes, 341–342 interpreting, 342–343 I-type instructions, 334–336 R-type instructions, 332–334 S/B-type instructions, 336–338	little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311 physical, 521 ports, 267 protection, 527. See also Virtual memory types, 267–268 DDR, 269–270 DRAM, 269–270 flash, 272 register file, 270–271 ROM, 271–272 SRAM, 269–270
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284 Logic elements (LEs), 278 of Cyclone IV, 278f, 279 functions built using, 280b–281b Logic families, 23, 543.e10, 543.e15–16 compatibility of, 24t logic levels of, 23 specifications, 543.e17t Logic gates, 17–20, 543.e1 AND. See AND gate AND-OR (AO) gate, 45 with delays in HDL, 187b	MAC. See Multiply-accumulate (MAC) Machine code. See Machine language Machine language, 332–344 addressing modes, 341–342 interpreting, 342–343 I-type instructions, 334–336 R-type instructions, 332–334 S/B-type instructions, 336–338 stored program, 343–344, 343f translating to assembly language, 342b–343b	little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311 physical, 521 ports, 267 protection, 527. See also Virtual memory types, 267–268 DDR, 269–270 DRAM, 269–270 flash, 272 register file, 270–271 ROM, 271–272 SRAM, 269–270 virtual, 503. See also Virtual memory
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284 Logic elements (LEs), 278 of Cyclone IV, 278f, 279 functions built using, 280b–281b Logic families, 23, 543.e10, 543.e15–16 compatibility of, 24t logic levels of, 23 specifications, 543.e17t Logic gates, 17–20, 543.e1 AND. See AND gate AND-OR (AO) gate, 45 with delays in HDL, 187b multiple-input gates, 19–20	MAC. See Multiply-accumulate (MAC) Machine code. See Machine language Machine language, 332–344 addressing modes, 341–342 interpreting, 342–343 I-type instructions, 334–336 R-type instructions, 332–334 S/B-type instructions, 336–338 stored program, 343–344, 343f translating to assembly language, 342b–343b U/J-type instructions, 338–340	little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311 physical, 521 ports, 267 protection, 527. See also Virtual memory types, 267–268 DDR, 269–270 DRAM, 269–270 flash, 272 register file, 270–271 ROM, 271–272 SRAM, 269–270 virtual, 503. See also Virtual memory Memory address computation, 307–308,
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284 Logic elements (LEs), 278 of Cyclone IV, 278f, 279 functions built using, 280b–281b Logic families, 23, 543.e10, 543.e15–16 compatibility of, 24t logic levels of, 23 specifications, 543.e17t Logic gates, 17–20, 543.e1 AND. See AND gate AND-OR (AO) gate, 45 with delays in HDL, 187b multiple-input gates, 19–20 NAND. See NAND gate	MAC. See Multiply-accumulate (MAC) Machine code. See Machine language Machine language, 332–344 addressing modes, 341–342 interpreting, 342–343 I-type instructions, 334–336 R-type instructions, 332–334 S/B-type instructions, 336–338 stored program, 343–344, 343f translating to assembly language, 342b–343b U/J-type instructions, 338–340 Magnitude comparator, 245	little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311 physical, 521 ports, 267 protection, 527. See also Virtual memory types, 267–268 DDR, 269–270 DRAM, 269–270 flash, 272 register file, 270–271 ROM, 271–272 SRAM, 269–270 virtual, 503. See also Virtual memory Memory address computation, 307–308, 401–402, 425f
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284 Logic elements (LEs), 278 of Cyclone IV, 278f, 279 functions built using, 280b–281b Logic families, 23, 543.e10, 543.e15–16 compatibility of, 24t logic levels of, 23 specifications, 543.e17t Logic gates, 17–20, 543.e1 AND. See AND gate AND-OR (AO) gate, 45 with delays in HDL, 187b multiple-input gates, 19–20 NAND. See NAND gate NOR. See NOR gate	MAC. See Multiply-accumulate (MAC) Machine code. See Machine language Machine language, 332–344 addressing modes, 341–342 interpreting, 342–343 I-type instructions, 334–336 R-type instructions, 332–334 S/B-type instructions, 336–338 stored program, 343–344, 343f translating to assembly language, 342b–343b U/J-type instructions, 338–340 Magnitude comparator, 245 Main Decoder, 408, 411t	little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311 physical, 521 ports, 267 protection, 527. See also Virtual memory types, 267–268 DDR, 269–270 DRAM, 269–270 flash, 272 register file, 270–271 ROM, 271–272 SRAM, 269–270 virtual, 503. See also Virtual memory Memory address computation, 307–308, 401–402, 425f data flow during, 402f, 425f
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284 Logic elements (LEs), 278 of Cyclone IV, 278f, 279 functions built using, 280b–281b Logic families, 23, 543.e10, 543.e15–16 compatibility of, 24t logic levels of, 23 specifications, 543.e17t Logic gates, 17–20, 543.e1 AND. See AND gate AND-OR (AO) gate, 45 with delays in HDL, 187b multiple-input gates, 19–20 NAND. See NAND gate NOR. See NOR gate NOT. See NOT gate	MAC. See Multiply-accumulate (MAC) Machine code. See Machine language Machine language, 332–344 addressing modes, 341–342 interpreting, 342–343 I-type instructions, 334–336 R-type instructions, 332–334 S/B-type instructions, 336–338 stored program, 343–344, 343f translating to assembly language, 342b–343b U/J-type instructions, 338–340 Magnitude comparator, 245 Main Decoder, 408, 411t Main FSM, 422–432, 436f	little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311 physical, 521 ports, 267 protection, 527. See also Virtual memory types, 267–268 DDR, 269–270 DRAM, 269–270 flash, 272 register file, 270–271 ROM, 271–272 SRAM, 269–270 virtual, 503. See also Virtual memory Memory address computation, 307–308, 401–402, 425f data flow during, 402f, 425f Memory arrays, 265–275. See also
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284 Logic elements (LEs), 278 of Cyclone IV, 278f, 279 functions built using, 280b–281b Logic families, 23, 543.e10, 543.e15–16 compatibility of, 24t logic levels of, 23 specifications, 543.e17t Logic gates, 17–20, 543.e1 AND. See AND gate AND-OR (AO) gate, 45 with delays in HDL, 187b multiple-input gates, 19–20 NAND. See NAND gate NOR. See NOR gate NOT. See NOR gate OR. See OR gate	MAC. See Multiply-accumulate (MAC) Machine code. See Machine language Machine language, 332–344 addressing modes, 341–342 interpreting, 342–343 I-type instructions, 334–336 R-type instructions, 332–334 S/B-type instructions, 336–338 stored program, 343–344, 343f translating to assembly language, 342b–343b U/J-type instructions, 338–340 Magnitude comparator, 245 Main Decoder, 408, 411t Main FSM, 422–432, 436f main function in C, 545.e3	little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311 physical, 521 ports, 267 protection, 527. See also Virtual memory types, 267–268 DDR, 269–270 DRAM, 269–270 flash, 272 register file, 270–271 ROM, 271–272 SRAM, 269–270 virtual, 503. See also Virtual memory Memory address computation, 307–308, 401–402, 425f data flow during, 402f, 425f Memory arrays, 265–275. See also Memory
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284 Logic elements (LEs), 278 of Cyclone IV, 278f, 279 functions built using, 280b–281b Logic families, 23, 543.e10, 543.e15–16 compatibility of, 24t logic levels of, 23 specifications, 543.e17t Logic gates, 17–20, 543.e1 AND. See AND gate AND-OR (AO) gate, 45 with delays in HDL, 187b multiple-input gates, 19–20 NAND. See NAND gate NOR. See NOR gate NOR. See NOR gate OR. See OR gate OR. See OR gate OR-AND-INVERT (OAI) gate, 45	MAC. See Multiply-accumulate (MAC) Machine code. See Machine language Machine language, 332–344 addressing modes, 341–342 interpreting, 342–343 I-type instructions, 334–336 R-type instructions, 336–338 stored program, 343–344, 343f translating to assembly language, 342b–343b U/J-type instructions, 338–340 Magnitude comparator, 245 Main Decoder, 408, 411t Main FSM, 422–432, 436f main function in C, 545.e3 Main memory, 501–503	little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311 physical, 521 ports, 267 protection, 527. See also Virtual memory types, 267–268 DDR, 269–270 DRAM, 269–270 flash, 272 register file, 270–271 ROM, 271–272 SRAM, 269–270 virtual, 503. See also Virtual memory Memory address computation, 307–308, 401–402, 425f data flow during, 402f, 425f Memory arrays, 265–275. See also Memory bit cell, 267
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284 Logic elements (LEs), 278 of Cyclone IV, 278f, 279 functions built using, 280b–281b Logic families, 23, 543.e10, 543.e15–16 compatibility of, 24t logic levels of, 23 specifications, 543.e17t Logic gates, 17–20, 543.e1 AND. See AND gate AND-OR (AO) gate, 45 with delays in HDL, 187b multiple-input gates, 19–20 NAND. See NAND gate NOR. See NOR gate NOT. See NOT gate OR. See OR gate OR-AND-INVERT (OAI) gate, 45 XNOR. See XNOR gate	MAC. See Multiply-accumulate (MAC) Machine code. See Machine language Machine language, 332–344 addressing modes, 341–342 interpreting, 342–343 I-type instructions, 334–336 R-type instructions, 336–338 stored program, 343–344, 343f translating to assembly language, 342b–343b U/J-type instructions, 338–340 Magnitude comparator, 245 Main Decoder, 408, 411t Main FSM, 422–432, 436f main function in C, 545.e3 Main memory, 501–503 malloc function, 545.e40	little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311 physical, 521 ports, 267 protection, 527. See also Virtual memory types, 267–268 DDR, 269–270 DRAM, 269–270 flash, 272 register file, 270–271 ROM, 271–272 SRAM, 269–270 virtual, 503. See also Virtual memory Memory address computation, 307–308, 401–402, 425f data flow during, 402f, 425f Memory arrays, 265–275. See also Memory bit cell, 267 HDL for, 273b, 274b, 275f,
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284 Logic elements (LEs), 278 of Cyclone IV, 278f, 279 functions built using, 280b–281b Logic families, 23, 543.e10, 543.e15–16 compatibility of, 24t logic levels of, 23 specifications, 543.e17t Logic gates, 17–20, 543.e1 AND. See AND gate AND-OR (AO) gate, 45 with delays in HDL, 187b multiple-input gates, 19–20 NAND. See NAND gate NOR. See NOR gate NOT. See NOT gate OR. See OR gate OR-AND-INVERT (OAI) gate, 45 XNOR. See XNOR gate	MAC. See Multiply-accumulate (MAC) Machine code. See Machine language Machine language, 332–344 addressing modes, 341–342 interpreting, 342–343 I-type instructions, 334–336 R-type instructions, 336–338 stored program, 343–344, 343f translating to assembly language, 342b–343b U/J-type instructions, 338–340 Magnitude comparator, 245 Main Decoder, 408, 411t Main FSM, 422–432, 436f main function in C, 545.e3 Main memory, 501–503 malloc function, 545.e40 Mantissa, 258	little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311 physical, 521 ports, 267 protection, 527. See also Virtual memory types, 267–268
Logic arrays, 275–284. See also Field programmable gate arrays (FPGAs) transistor-level implementation, 283–284 Logic elements (LEs), 278 of Cyclone IV, 278f, 279 functions built using, 280b–281b Logic families, 23, 543.e10, 543.e15–16 compatibility of, 24t logic levels of, 23 specifications, 543.e17t Logic gates, 17–20, 543.e1 AND. See AND gate AND-OR (AO) gate, 45 with delays in HDL, 187b multiple-input gates, 19–20 NAND. See NAND gate NOR. See NOR gate NOT. See NOT gate OR. See OR gate OR-AND-INVERT (OAI) gate, 45 XNOR. See XNOR gate	MAC. See Multiply-accumulate (MAC) Machine code. See Machine language Machine language, 332–344 addressing modes, 341–342 interpreting, 342–343 I-type instructions, 334–336 R-type instructions, 336–338 stored program, 343–344, 343f translating to assembly language, 342b–343b U/J-type instructions, 338–340 Magnitude comparator, 245 Main Decoder, 408, 411t Main FSM, 422–432, 436f main function in C, 545.e3 Main memory, 501–503 malloc function, 545.e40	little-endian, 356 logic using, 272–273 main, 502 operands in, 306, 310–311 physical, 521 ports, 267 protection, 527. See also Virtual memory types, 267–268 DDR, 269–270 DRAM, 269–270 flash, 272 register file, 270–271 ROM, 271–272 SRAM, 269–270 virtual, 503. See also Virtual memory Memory address computation, 307–308, 401–402, 425f data flow during, 402f, 425f Memory arrays, 265–275. See also Memory bit cell, 267 HDL for, 273b, 274b, 275f,

Memory hierarchy, 503	Microcontroller peripherals, 542.e43	MOSFETs. See Metal-oxide-
Memory instructions, 306–308,	Bluetooth wireless communication,	semiconductor field effect
317–320, 334–336, 400–402	542.e53–54	transistors (MOSFETs)
encodings, 334–335	character LCD, 542.e44-47	Most significant bit (msb), 11, 12f
Memory interface, 499	control, 542.e47 <i>b</i>	Most significant byte (MSB), 11, 12f,
Memory map, RISC-V, 344–346,	parallel interface, 542.e44,	306–307
542.e2 <i>f</i>	542.e45 <i>f</i>	Motors
Memory performance. See Average	motor control, 542.e54–64	DC, 542.e54–59
Memory Access Time (AMAT)	VGA monitor, 542.e45–52	H-bridge, 542.e55-58
Memory protection, 527	Microcontroller units (MCUs), 542.e3	servo, 542.e54, 542.e58–60
Memory systems, 499	Micro-operations, 469–470	stepper, 542.e54, 542.e60–64
performance analysis, 503–505	designers, 468	msb. See Most significant bit (msb)
Memory-mapped I/O, 542.e1–3,	high-performance, 468	MSB. See Most significant byte (MSB)
542.e7	Microprocessors, 1, 11 <i>b</i> , 299, 393	MSI chips. See Medium-scale integration
address decoder, 542.e1–3, 542.e2	architectural state of, 395	(MSI) chips
communicating with I/O devices,	Millions of instructions per second,	MTBF. See Mean time between failure
542.e2 <i>b</i> –3 <i>b</i>	439	(MTBF)
hardware, 542.e2 <i>f</i> , 542.e3	Min-delay constraint. See Hold time	Multicycle processor, 415–438
Mem Write, 403, 404f	constraint	control, 422–432, 436 <i>f</i>
Metal-oxide-semiconductor field effect	Minterms, 56	datapath, 416–422
transistors (MOSFETs), 24	Miss, 502–505, 518	beg instruction, 421–422
switch models of, 28f	capacity, 518	I-type ALU instructions,
Metastability, 149–150	compulsory, 518	w instruction, 417–419
metastable state, 108, 149	conflict, 511	R-type instructions, 421–422
resolution time, 149–150, 152–155	Miss penalty, 513	sw instruction, 420–421
synchronizers, 150–152	Miss rate, 503–505	instructions, 410–412
Mib. See Mebibit (Mib/Mibit)	and access times, 504t	performance, 435–438
Mibit. See Mebibit (Mib/Mibit)	Misses	
	cache, 502	Multicycle microarchitectures, 396
Micro-operations (micro-ops), 469–470	cache, 302	Multilevel combinational logic, 67–71.
Microarchitecture, 300, 393, 396. See also Architecture	1	See also Logic
advanced. See Advanced	compulsory, 518	Multiple output singuit (Ch
	conflict, 518	Multiple-output circuit, 66b
microarchitecture	page fault, 521–522	Multiplexers, 81–84
architectural state. See Architectural	Mnemonics, 301, 301 <i>b</i>	definition of, 81
state	ModR/M byte, 371–372	HDL for
description of, 393–394	Modularity, 4	behavioral model of, 179 <i>b</i>
design process, 394–396	Modules, in HDL	parameterized N-bit, 216b
evolution of RISC-V, 482–485	behavioral and structural, 171–172	structural model of, 188b
HDL representation, 456–468	parameterized modules, 215–218	logic using, 82–84
generic building blocks, 461–464	Moore, Gordon, 28b	symbol and truth table, 81f
single-cycle processor, 457	Moore machines, 121–132	Multiplicand, 253
testbench, 464–468	state transition and output table,	Multiplication. See Multiplier
multicycle processor. See Multicycle	131 <i>t</i>	Multiplier, 253
RISC-V processor	state transition diagrams, 131f	HDL for, 254
performance analysis, 397–398. See	timing diagrams for, 133f	Multiply instructions, 310–311
also Performance analysis	Moore's law, 28b	Multiprocessors, 479–482
pipelined processor. See Pipelined	MOS transistors. See Metal-oxide-	chip, 479
RISC-V processor	semiconductor field effect	heterogeneous, 479
real-world perspective, 482–485	transistors (MOSFETs)	homogeneous, 479
single-cycle processor. See Single-	MOSFET. See Metal-oxide-	Multithreaded processor, 479
cycle RISC-V processor	semiconductor field effect	Multithreading, 478–479
Microcontroller, 542.e3, 542.e31	transistors (MOSFETs)	Mux. See Multiplexers

N	0	Page offset, 523
		Page table, 522–523
		Pages, 521–522
21.21.6.21	0.11	Paging, 528
NaN. See Not a number (NaN)	Odds and ends, 355–363	Parallel I/O, 542.e14–15
NAND (7400), 543.e3 <i>f</i>	endianness, 355–356	Parallelism, 155–158
NAND gate, 19	exceptions, 356–360	Parity gate. See XOR gate
CMOS, 29–30	nop, 331–332	Partial products, 253
Nested if/else statement, 314–315,	OFF, 24, 28	Pass by reference, 545.e22
545.e18	Offset, 307, 400–401, 418	
Nibbles, 11–12	ON, 24, 28	Pass by value, 545.e22
nMOS transistors, 26–29, 27b	One-bit dynamic branch predictor, 471	Pass gate. See Transmission gates
Noise margins, 21–22, 21 <i>f</i>	One-cold encoding, 128	PC. See Program counter (PC)
calculating, 21b-22b	One-hot encoding, 127–128	PC Logic, 415
Nonarchitectural state, 393–394, 396, 416	One-time programmable (OTP), 543.e2	PC-relative addressing, 341–342
Nonblocking and blocking assignments,	op field, 333	PCBs. See Printed circuit boards (PCBs)
197, 203–207	Opcode. See op field	PCI. See Peripheral Component
Nonleaf function calls, 326-327	Operands	Interconnect (PCI)
Nonpreserved registers, 324, 327–329	RISC-V, 302	PCSrc, 406–407, 409, 411
nop, 331–332, 444–445	constants/immediates, 304–306	PCWrite, 419
NOR gate, 19–20, 61, 543.e3f	memory, 306–308	Perfect induction, proving theorems
chip (7402), 543.e3 <i>f</i>	register set, 304	using, 62b
CMOS, 30b	registers, 303–304	Performance analysis, 397–398. See also
pseudo-nMOS logic, 31	x86, 367–369	Average Memory Access Time
truth table, 20 <i>f</i>	Operation code. See op field	(AMAT)
Not a number (NaN), 259	Operators	multicycle processor, 436-437
NOT gate, 18	in C, 316	pipelined processor, 439–456
chip (7404), 543.e3 <i>f</i>	in HDL, 176 <i>b</i>	processor comparison, 438b
CMOS, 29	bitwise, 175–176	single-cycle processor, 412–414
Noyce, Robert, 24 <i>b</i>	precedence, 183 <i>b</i>	Peripherals, 542
Null element theorem, 59–60	reduction, 178	Peripherals devices. See Input/output
Number conversion	table of, 183 <i>b</i>	(I/O) systems
binary to decimal, 8b	ternary, 179 <i>b</i>	Phase locked loop (PLL), 542.e50-53
binary to hexadecimal, 9–11	OR gate, 19	Physical memory, 503
decimal to binary, 9b, 11b	OR-AND-INVERT (OAI) gate, 194	Physical page number (PPN), 523
decimal to hexadecimal, 11b	or instruction, 309	Physical pages, 522
hexadecimal to binary and decimal,	OTP. See One-time programmable (OTP)	Pipelined processor, 439–456
9 <i>b</i> , 10 <i>b</i>	Out-of-order execution, 477 <i>f</i>	abstract view of, 441f
taking the two's complement, 14–16	Out-of-order processor, 473–476	control unit, 443, 453
Number systems, 7–17	Output dependence, 476	datapath, 441–443
binary, 7–17	Overflow	description, 439–456
comparison of, 16–17, 17 <i>t</i>	with addition, 13	hazards, 443–453
estimating powers of two, $12b$	detection, 248–249	performance analysis, 454–456
fixed-point, 256–257, 256 <i>f</i>	Oxide, 26–27	throughput, 439–440
floating-point, 257–261	, ·	Pipelined microarchitecture. See
addition, 260f, 261		Pipelined processor
special cases, 259		Pipelining, 156–157. See also Pipelined
hexadecimal, 9–11, 10 <i>t</i>	P	processor
negative and positive, 13–14		PLAs. See Programmable logic arrays
sign/magnitude, 13–14		(PLAs)
signed, 13–17	Packages, chips, 543.e19–20	Plastic leaded chip carriers (PLCCs),
two's complement, 14–16	Page fault, 521–522	543.e19–20
unsigned, 7–13	Page number, 523	Platters, 520–521
unsigneu, /-13	1 age mulliber, 323	1 1411018, 320-321

PLCCs. See Plastic leaded chip carriers RISC-V register descriptions, 303 PROMs. See Programmable read only (PLCCs) memories (PROMs) schematic, 270-271 PLDs. See Programmable logic devices Propagate signal, 239 Register renaming, 476–478 (PLDs) Propagation delay, 86-90. See also Register set, 304. See also Register file (RF) PLL. See Phase locked loop (PLL) R-type (register-type) instruction, Critical path pMOS transistors, 26-29, 27f Pseudo-nMOS logic, 31–32, 31f 332-334 Pointers, 542.e9, 545.e21-22, 545.e33 Registers. See RISC-V registers; Flip-NOR gate, 31f POS. See Product-of-sums (POS) form ROMs and PLAs, 283-284 flops; x86 registers Pseudoinstructions, 330-332, 358b preserved and nonpreserved, 324-326 Positive edge-triggered flip-flop, 112 Power consumption, 32-34 Pulse-Width Modulation (PWM), 542 Regularity, 4 RegWrite, 402 PPN. See Physical page number (PPN) analog output with, 542.e31 Prefix adders, 241–243 duty cycle, 542.e35 Replacement policies, 527–529 Prefix tree, 243 signal, 542.e35f Resettable flip-flops, 114 Preserved registers, 324–326, 325t PWM. See Pulse-Width Modulation Resettable registers, 192–193 (PWM) Resolution time, 149-150. See also Prime implicants, 63-81 Printed circuit boards (PCBs), 543.e20-23 Metastability derivation of, 152-155 printf, 545.e36-37 Return value, 320 Priority Q circuit, 66-67 RF. See Register file (RF) Ring oscillator, 313b, 335f encoder, 100-101, 103 Ripple-carry adder, 238–239, 241*b* Procedure calls. See Function calls Processor performance comparison, Quiescent supply current, 33-34 RISC architecture. See Reduced 438*b*, 455*b* instruction set computer (RISC) architecture multicycle processor, 436–437 pipelined processor, 454-456 RISC-V architecture, evolution of, R single-cycle processor, 415b363-366 comparison of RISC-V and ARM Processor-memory gap, 502 Product-of-sums (POS) form, 58 architectures, 365-366 comparison of RISC-V and MIPS Program counter (PC), 308, 343-344, R-type instruction, 35–37 Race conditions, 117b-118b, 118f architectures, 365 Programmable logic arrays (PLAs), RAM. See Random access memory (RAM) RISC-V Base Instruction Sets and rand, 545.e40-41 Extensions, 364–365 275-276, 543.e2, 543.e6-7 transistor-level implementation, Random access memory (RAM), RISC-V instructions, 299 267-269, 272-273 addressing modes, 341-342 283-284 RAW hazard. See Read after write Programmable logic devices (PLDs), branch instructions, 311–313 (RAW) hazard immediate encodings, 340-341 543.e6-7 Programmable read only memories rd field. See Destination register (rd) interpreting, 342–343 (PROMs), 271, 543.e2-6 Read after write (RAW) hazard, 444, logical instructions, 309 Programming 475. See also Hazards multiply instructions, 310-311 Read only memory (ROM), 267, shift instructions, 309-310 arrays. See Arrays 269-271 formats branching. See Branching transistor-level implementation, 284 in C. See C programming I-type instructions, 334–336 conditional statements, 313-315 Read/write head, 520-521 R-type instructions, 332–334 constants. See Constants; Immediates ReadData bus, 402, 403f S/B-type instructions, 336–338 function calls. See Function calls Receiver gate, 20-21 U/J-type instructions, 338–340 Recursive function calls, 327-329 instruction set, 302 getting loopy. See Loops Reduced instruction set computer (RISC) memory instructions, 306-308 logical and arithmetic instructions, architecture, 302, 469-470 miscellaneous instructions, 355-356 309 loops. See Loops Reduction operators, 178 pseudoinstructions, 330-332 Register file (RF) stored program, 343-344 memory, 317-320 in RISC-V, 308 HDL for, 461-464 RISC-V microprocessor, 393–467 in pipelined RISC-V processor (write data memory, 395 shift instructions, 309–310, 333–335, on falling edge), 441-442 instruction memory, 395 335f

multicycle, 396, 415-438	Semiconductors, 25	Sign/magnitude numbers, 13–14,
pipelined, 396, 439–456	industry, sales, 1	256–257
program counter, 394	Sequencing overhead, 141–142,	Signed binary numbers, 13–17
register file, 395	147–149, 157–158, 455–456	Signed instructions, 360–361
single-cycle, 396, 398-415	Sequential building blocks. See	Signed multiplier, 215
state elements of, 393-394	Sequential logic	Silicon dioxide (SiO ₂), 26–27
RISC-V processors. See RISC-V	Sequential logic, 107, 261–265	Silicon lattice, 25
microprocessors	counters, 261–263	SIMD. See Single instruction multiple
RISC-V registers, 303–304	finite state machines. See Finite state	data (SIMD)
program counter, 341, 343–344, 394	machines (FSMs)	simple function, 320-321
register file, 394–395	flip-flops, 112-113. See also	Simple programmable logic devices
register set, 304–305	Registers	(SPLDs), 277
RISC-V single-cycle HDL, 456–467	latches, 107-117	Simulation waveforms, 174
building blocks, 461-463	D, 111–112	with delays, 187f
controller, 458b-460b	SR, 109–111	Single instruction multiple data (SIMD),
datapath, 460 <i>b</i> –461 <i>b</i>	registers. See Registers	473
testbench, 464–468	shift registers, 263–265	Single-cycle processor, 398–415, 457
Rising edge, 86	timing of. See Timing analysis	control, 407–410
ROM. See Read only memory (ROM)	Serial Clock (SCK), 542.e15	controller, 458b
Rotations per minute (RPM), 542.e55	Serial communication, with PC,	datapath, 399–407
Rotators, 251–253	542e27	addi instruction, 410–411
Rounding modes, 260–261	Serial Data In (SDI), 542.e15	beq instruction, 421–422
RPM. See Rotations per minute (RPM)	Serial Data Out (SDO), 542.e15	jal instruction, 411–412
rs1 field. See Source register 1 (rs1)	Serial I/O, 542.e14–29	w instruction, 400–402
rs2 field. See Source register 2 (rs2)	SPI. See Serial peripheral interface	R-type instructions, 404–405
RS-232, 542.e25	(SPI)	sw instruction, 403–404
RV32IMAC instruction set, 484–486	UART. See Universal Asynchronous	decoders, 459b
	Receiver Transmitter (UART)	HDL for, 457–467
	Serial Peripheral Interface (SPI), 542.e4,	instructions, 410–412
S	542.e15–22	performance, 412–415
3	connection between FE310 controller	Single-cycle microarchitecture. See
	and FPGA, 542.e19-20	Single-cycle processor
	ports	Single-pole double-throw switches
S-type instruction format. See S/B-type	Serial Clock (SCK), 542.e15	(SPDT switches), 543.e17–18
instruction format	Serial Data In (SDI), 542.e15	Single-pole single-throw switches (SPST
S/B-type instruction format, 336–338	Serial Data Out (SDO), 542.e15	switches), 543.e17–18
Sampling, 139	waveforms, 542.e15	Single-precision formats, 259–260. See
Sampling rate, 542.e31	Servo motor, 542.e60 <i>b</i> , 542.e54,	also Floating-point numbers
SATA. See Serial ATA (SATA)	542.e58–60	SiO ₂ . See Silicon dioxide (SiO ₂)
Scalar processor, 472–473	Set bits, 508	Skew. See Clock skew
Scan chains, 265 scanf, 545.e37	Setup time constraint, 141–142 with clock skew, 146–149	Slash notation, 54f
	Seven-segment display decoder, 77b–79b	Small-scale integration (SSI) chips, 543.e1
Scannable flip-flop, 265 Schematics, rules of drawing, 29, 65		SMP. See Symmetric multiprocessing (SMP)
SCK. See Serial Clock (SCK)	with don't cares, 80 <i>b</i> HDL for, 199 <i>b</i>	Solid state drive (SSD), 502. See also
SDI. See Serial Data In (SDI)	Shaft encoder, 542.e58 <i>f</i> , 542.e54,	Flash memory; Hard drive
SDO. See Serial Data III (SDI) SDO. See Serial Data Out (SDO)	542.e58–59	SOP. See Sum-of-products (SOP) form
SDRAM. See Synchronous dynamic	Shift instructions, 309–310, 310 <i>f</i>	Source register 1 (rs1), 332f, 333
random access memory (SDRAM)	Shift registers, 263–265	Source register 2 (rs2), 332f, 333
Segment descriptor, 372	Shifters, 251–253	sp. See Stack pointer (sp)
Segmentation, 373	Short path, 87–90	SparkFun's RED-V RedBoard, 542
Selected signal assignment statements,	Sign bit, 13–14	Spatial locality, 500, 514 <i>b</i>
180b	Sign extension, 16	Spatial parallelism, 155–156
1000	organ extension, 10	opanai paranenom, 100 100

CDDT : 1 C C: 1 1 1 11	545 40 6 1	11 1: 1 11 1:
SPDT switches. See Single-pole double-	stdlib.h, C library, 545.e40. See also	blocking and nonblocking
throw switches (SPDT switches)	Standard libraries	assignment, 197, 203–207
SPEC, 397	Stepper motors, 542.e54, 542.e60–64	case statements, 199–200, 203 <i>b</i>
SPECINT2000, 438	bipolar stepper motor, 542.e60–64,	combinational logic using, 175–188,
SPI. See Serial Peripheral Interface (SPI)	half-step drive, 542.e60–61	196–207, 215–218
SPLDs. See Simple programmable logic	two-phase-on drive, 542.e60–61	comments, 178
devices (SPLDs)	wave drive, 542.e62-63	conditional assignment, 179–180
SPST switches. See Single-pole single-	Store/branch instructions (S/B-type	data types, 211–215
throw switches (SPST switches)	instructions). See S/B-type	decoders, 200 <i>b</i> , 217
Squashing, 476	instruction format	delays (in simulation only), $187b$
SR latches, 109–111, 110 <i>f</i>	Stored program, 343–344	divide-by-3 FSM, 208 <i>b</i>
SRAM. See Static random access	string.h, C library, 545.e42-43	finite state machines (FSMs), 207–209
memory (SRAM)	Strings, 319, 545.e27-28. See also	Mealy FSM, 211 <i>b</i>
srand, 545.e40-41	Characters (char)	Moore FSM, 208–210
SSD. See Solid state drive (SSD)	struct. See Structures (struct)	full adder, 182b
SSI chips. See Small-scale integration	Structural modeling, 171–172, 188–190	history of, 173b
(SSI) chips	Structures (struct), 545.e29–30	if statements, 200–203
Stack, 322-324. See also Function calls	sub instruction, 301	internal signals, 180-182
preserved registers, 324–326	Substrate, 26–27	inverters, 176 <i>b</i> , 197 <i>b</i>
during recursive function call,	Subtraction, 15, 244–245	latches, 196
327–329	Subtractor, 244–245	logic gates, 175–188
stack frame, 324–325	Sum-of-products (SOP) form, 56–58	multiplexers, 179 <i>b</i> , 188 <i>b</i> , 216 <i>b</i>
stack pointer (SP), 329	Superscalar processor, 472–473	multiplier, 215
storing additional arguments on, 330	Supply voltage, 56–58. See also VDD	numbers, 183
storing local variables on, 330	sw instruction, 307–308	operators, 182–183
Stalls, 448–450. See also Hazards	Swap space, 528	parameterized modules, 215–218
Standard libraries, 545.e35–43	Switch/case statements	N-bit multiplexers, 216b
file manipulation, 545.e38–39	in C, 545.e18	N-input AND gate, 218b
printf, 545.e36–37	in HDL. See case statement, in HDL	$N:2^N$ decoder, 217 b
scanf, 545.e37		priority circuit, 202 <i>b</i>
The state of the s	in RISC-V assembly, 314–315	
math, 545.e42	Switches, 543.e17–18	using don't cares, 203b
stdio, 545.e35–40	Symbol table, 351–353	reduction operators, 178
stdlib, 545.e40–42	Symmetric multiprocessing (SMP),	registers, 191
exit, 545.e41	479–480. See also Homogeneous	enabled, 194
format conversion (atoi, atol,	multiprocessors	resettable, 192–193
atof), 545.e41	Synchronizers, 150–152	sequential logic using, 191–196,
rand, srand, 545.e40-41	Synchronous circuits, 120–121	207–209
string, 545.e42–43	Synchronous dynamic random access	seven-segment display decoder,
State encodings, FSM, 127–128,	memory (SDRAM), 269–270	77 <i>b</i> –79 <i>b</i>
132–135. See also Binary	DDR, 269–270	simulation and synthesis,
encoding; One-cold encoding;	Synchronous logic, design, 117–121	173–175
One-hot encoding	Synchronous resettable flip-flops, 114	structural models, 188–190
State machine circuit. See Finite state	Synchronous sequential circuits,	synchronizer, 195 <i>b</i>
machines (FSMs)	118-120, 120b. See also Finite	testbench, 218–222
State variables, 107	state machines (FSMs)	self-checking, 220b
Static branch prediction, 470–472	timing specification. See Timing analysis	simple, 219b
Static discipline, 22–24	SystemVerilog, 171-223. See also	with test vector file, 221 <i>b</i> –222 <i>b</i>
Static power, 32	Hardware description languages	tristate buffer, 185 <i>b</i>
Static random access memory (SRAM),	(HDLs)	truth tables with undefined and
268–269	accessing parts of busses, 186b, 190b	floating inputs, 185b, 186t
Status flags, 369. See also Condition flags	bad synchronizer with blocking	using always/process, 198b
stdio.h, C library, 545.e35. See also	assignments, 207b	using nonblocking assignments, 206
Standard libraries	bit swizzling, 186	z's and x's, 184-186, 203b

T	Transistor-Transistor Logic (TTL), 23,	Two-level logic, 67–68
	543.e15	Two's complement numbers, 14–16
	Transistors, 24–32	typedef, 459b, 545.e31
Tag, 508	bipolar, 24 CMOS, 24–32	
Taking the two's complement, 15	gates made from, 29, 29–31, 30,	m.
Temporal locality, 500, 505, 509	30, 31	U
Temporal parallelism, 155–156	latches and flip-flops, 114–115	
Temporary registers, 303b	MOSFETs, 24	
Ternary operators, 179b, 545.e13	nMOS, 26–29	U. See Use bit (U)
Testbench, 464–468	pMOS, 26–29	U-type instruction format. See U/J-type
Testbenches, HDLs, 218	pseudo-nMOS, 31–32	instruction format
self-checking, 219	ROMs and PLAs, 283	U/J-type instruction format, 338–340
simple, 219	transmission gate, 31	UART. See Universal Asynchronous
with testvectors, 221 <i>b</i> –222 <i>b</i>	Translating and starting a program, 344f	Receiver Transmitter (UART)
Text Segment, 345, 355	Translation lookaside buffer (TLB),	Unconditional branches, 311
Thin small outline package (TSOP), 543.e19–20	525-526, 526-527	Undefined instruction exception, 356
Thread level parallelism (TLP), 478	Transmission gates, 31	Unicode, 317b
Threshold voltage, 27–28	Transmission lines, 543.e23–35	Unit under test (UUT), 218b
Throughput, 155, 396, 439, 479	characteristic impedance (Z_0),	Unity gain points, 22
Timers, 542.e29–31	543.e24, 543.e33	Universal Asynchronous Receiver
Timing	derivation of, 543.e33-34	Transmitter (UART), 542.e23–29
of combinational logic,	matched termination, 543.e24-26	hardware handshaking, 542.e25 Universal Serial Bus (USB), 275,
86–87	mismatched termination, 543.e27–29	542.e15, 542.e24
delay. See Contamination delay	open termination, 543.e26	Unsigned instructions, 360–361
glitches. See Glitches	reflection coefficient (k_r) , 543.e33–34	Unsigned multiplier, 215 <i>b</i> , 360
of sequential logic, 139-155	derivation of, 543.e33–34	Unsigned numbers, 16
analysis. See Timing analysis	series and parallel terminations,	Upper immediate/jump instructions
clock skew. See Clock skew	543.e30–32	(U/J-Type instructions), 338–340
dynamic discipline, 139	short termination, 543.e27	USB. See Universal Serial Bus (USB)
metastability. See Metastability	when to use, 543.e30 Transparent latch. <i>See</i> Latches: D	Use bit (<i>U</i>), 515–516
resolution time. See Resolution	Traps, 356	UUT. See Unit under test (UUT)
time system timing. <i>See</i> Timing	Tristate buffer, 72, 185 <i>b</i>	
analysis	HDL for, 184	W
Timing analysis, 143 <i>b</i> –145 <i>b</i>	multiplexer built using, 82, 89 <i>b</i> –90 <i>b</i>	V
calculating cycle time. See Setup time	True, 6, 18, 56, 68, 72, 109–110, 114,	
constraint	127–128, 178, 180, 203	
with clock skew. See Clock skew	Truth tables, 17–18	V. See Valid bit (V)
hold time constraint. See Hold time	ALU decoder, 408–409, 412 <i>t</i>	Valid bit (<i>V</i>), 509
constraint	with don't cares, 66-67, 79-80, 203	Variables in C, 545.e7–11
max-delay constraint. See Setup time	multiplexer, 81–84	global and local, 545.e9–10
constraint	seven-segment display decoder,	initializing, 545.e11
min-delay constraint. See Hold time	77 <i>b</i> –79 <i>b</i>	primitive data types, 545.e8–9
constraint	SR latch, 132–135	V_{CC} , 21b. See also Supply voltage; VDD
multicycle processor, 437b	with undefined and floating inputs,	V_{DD} , 20–21, 30b. See also Supply
pipelined processor, 452	185b	voltage
setup time constraint. See Setup time	TSOP. See Thin small outline package	Vector processor, 472 <i>b</i> –473 <i>b</i> Verilog. <i>See</i> SystemVerilog
constraint single-cycle processor, 415 <i>b</i>	(TSOP) TTL. See Transistor-Transistor Logic	Very High Speed Integrated Circuits
TLB. See Translation lookaside buffer	(TTL)	(VHSIC), 173b. See also VHDL
(TLB)	Two-bit dynamic branch predictor, 471	(VHSIC Hardware Description
TLP. See Thread level parallelism (TLP)	Two-cycle latency of LDR, 448	Language)

VGA (Video Graphics Array) monitor, 542.e47–53	sequential logic using, 191–196, 207	WAR hazard. See Write after read (WAR) hazard
connector pinout, 542.e49 <i>f</i>	seven-segment display decoder,	WAW hazard. See Write after write
driver for, 542.e50 <i>b</i> –53 <i>b</i>	222	(WAW) hazard
VHDL, 171–223	simulation and synthesis, 173-175	Weak pull-up, 31
accessing parts of busses, 190b	structural models, 188–190	Weird number, 16
bad synchronizer with blocking	synchronizer, 195	While loops, 315, 545.e19
assignments, 207b	testbench, 218–222	White space, 178
bit swizzling, 186b	self-checking, 220b	Whitmore, Georgiana, 5b
blocking and nonblocking	simple, 219	Wire, 65
assignment, 197, 203–207	with test vector file, 221 <i>b</i> –222 <i>b</i>	Wireless communication, Bluetooth,
case statements , 199–200, 217	tristate buffer, 185b	542.e53-54
combinational logic using, 175,	truth tables with undefined and	Wordline, 267
196–207, 220–222	floating inputs, 185b, 203	Write after read (WAR) hazard, 475. See
comments, 178	z's and x's, 184-186	also Hazards
conditional assignment, 179-180	VHSIC. See VHDL	Write after write (WAW) hazard, 476
data types, 211–215	VHSIC Hardware Description	Write policy, 519–520
decoders, 200	Language. See VHDL	write-back, 519
delays (in simulation), 186-187	Video Graphics Array (VGA). See VGA	write-through, 519
divide-by-3 FSM, 208b	(Video Graphics Array) monitor	
finite state machines (FSMs), 393	Virtual address, 521	
Mealy FSM, 211b	space, 527	**
Moore FSM, 209, 210 <i>b</i>	Virtual memory, 503, 520–530	X
full adder, 182 <i>b</i>	address translation, 521-522	
using always/process, 198b	cache terms comparison, 522	
using nonblocking assignments,	memory protection, 527	X. See Contention (x); Don't care (X)
208	multilevel page tables, 529–530	x86
history of, 173b	page fault, 521–522	architecture, 366-374
if statements, 200–203	page number, 523	big picture, 373–374
internal signals, 182b	page offset, 523	branch conditions, 371t
inverters, 176, 196-197	page table, 524–525	instruction encoding, 371–372
latches, 196	pages, 521–522	instructions, 369
logic gates, 177b	replacement policies, 529–530	memory addressing modes, 368t
multiplexer, 179b, 188-189, 216b	translation lookaside buffer (TLB),	operands, 367–368
multiplier, 215b	525–526	peculiarities, 372–373
N-bit multiplexers, 216b	write policy, 519–520	registers, 366–367
N-input AND gate, 218b	Virtual page number (VPN), 524	status flags, 369
$N:2^{\bar{N}}$ decoder, 217	Virtual pages, 521–522	Xilinx FPGA, 278
numbers, 183	VPN. See Virtual page number (VPN)	XNOR gate, 19b
operators, 182–183	V_{SS} , 21 b	XOR gate, 19
parameterized modules, 215		
priority circuit, 203b		
reduction operators, 178	W	
using don't cares, 203b	••	Z
reduction operators, 178		_
registers, 191	TTT (
enabled, 194	Wafers, 26	7 (Pl : (7)
resettable, 192–193	Wall, Larry, 18b	Z. See Floating (Z)