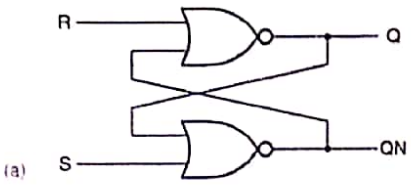
Set- Reset Latch



S	R	Q	QN
0	0	last Q	last QN
0	1	0	1
1	0	1	0
1	1	0	0

(b)

Figure 7-5
S-R latch: (a) circuit design using NOR gates; (b) function table.

Figure 7-6 Typical operation of an S-R latch: (a) "normal" inputs; (b) S and R asserted simultaneously.

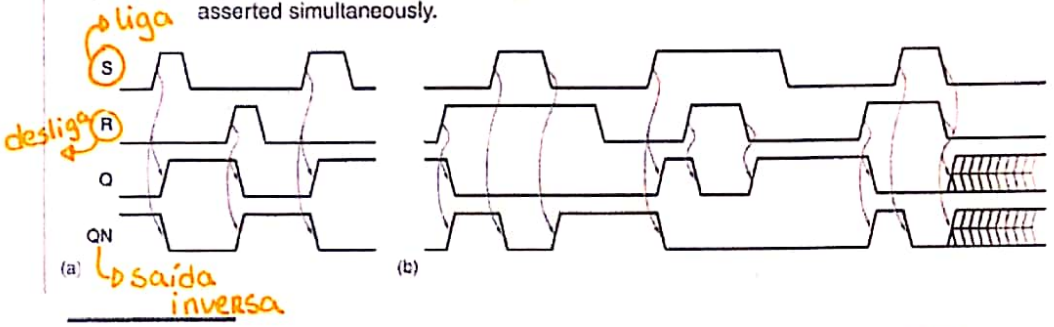
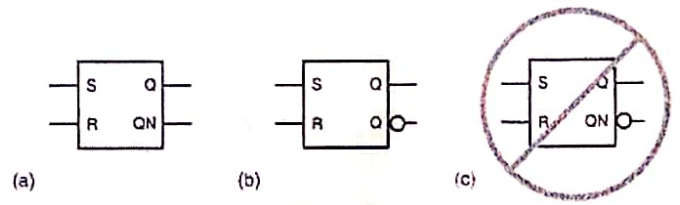
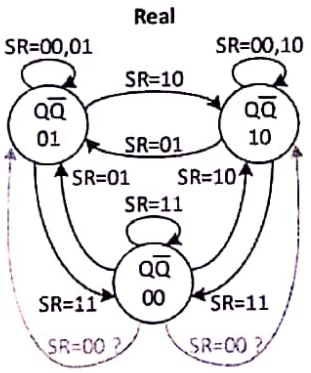


Figure 7-7
Symbols for an S-R latch:
(a) without bubble;
(b) preferred for bubble-to-bubble design;
(c) incorrect because of double negation.

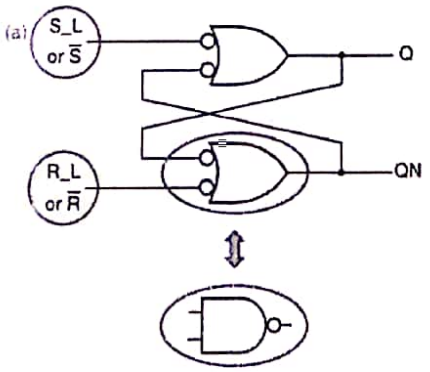




Q \ SR	00	01	11	10
0	0	0	X	1
1	1	0	X	1

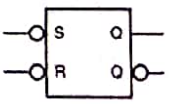
$Q^+ = S + \overline{Q}.R$

Figure 7-9 S-R̄ latch: (a) circuit design using NAND gates; (b) function table; (c) logic symbol.



(b)

S_L	R_L	Q	QN
0	0	1	1
0	1	1	0
1	0	0	1
1	1	last Q	last QN



Máquinas Moore
↳ no estado 11 independentemente do enable a saída será sempre 0

Máquinas de Mealy
↳ estado 11
- EN-0 → saída sempre 0
- EN-1 → saída reflete valor do enable

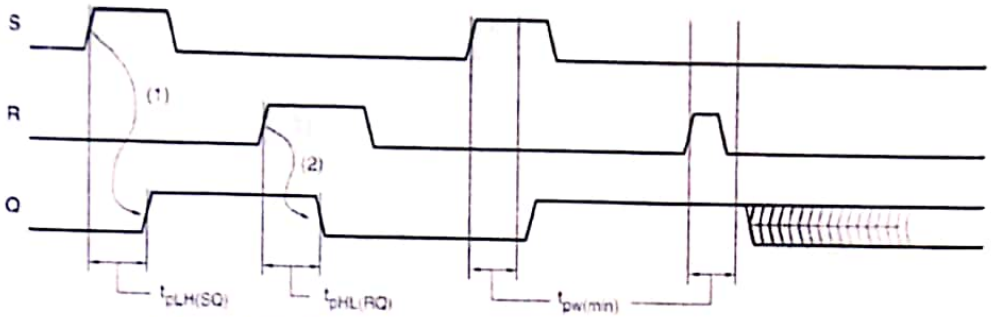


Figure 7-8 Timing parameters for an S-R latch.

D LATCH

- as entradas nunca são iguais
- transparente quando o relógio está ativo

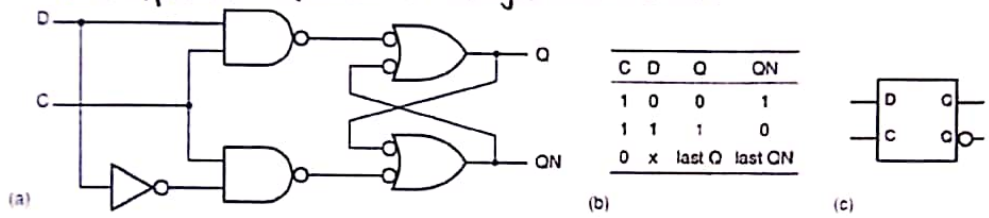


Figure 7-12 D latch: (a) circuit design using NAND gates; (b) function table; (c) logic symbol.

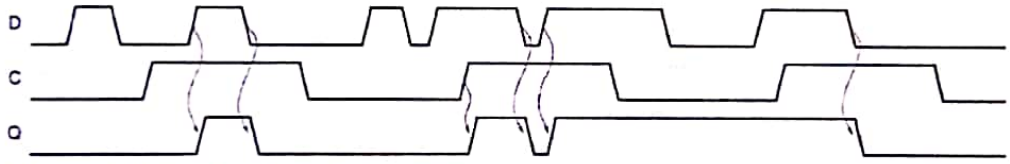
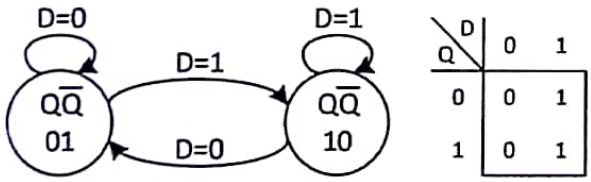


Figure 7-13 Functional behavior of a D latch for various inputs.

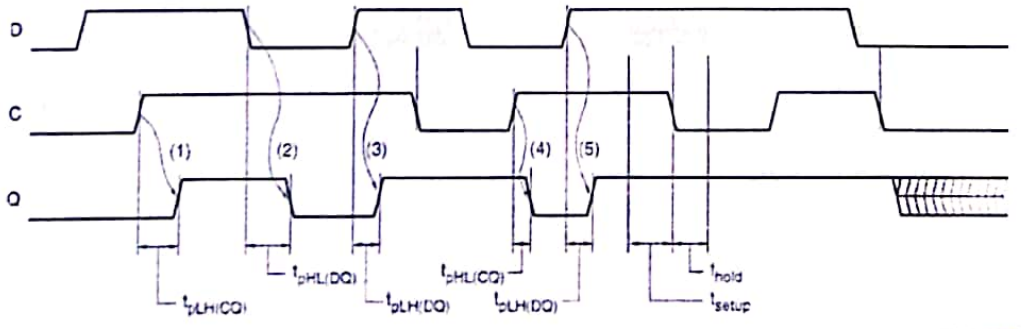


Q \ D	0	1
0	0	1
1	0	1

$Q^+ = D$

- mantém o estado quando o relógio não está ativo

Figure 7-14 Timing parameters for a D latch.



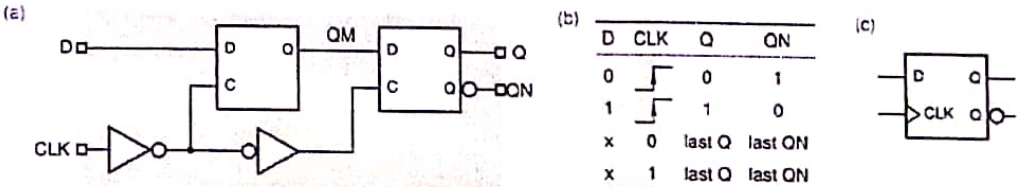
Device Type	Characteristic Equation
S-R latch	$Q^* = S + R' \cdot Q$
D latch	$Q^* = D$
Edge-triggered D flip-flop	$Q^* = D$
D flip-flop with enable	$Q^* = EN \cdot D + EN' \cdot Q$

Table 7-1 Latch and flip-flop characteristic equations.

DECIMAL	BINÁRIO	OCTAL	HEXADECIMAL	COMP.1	COMP.2	BCD-AIKEN	BCD
0	0000	0	0	0	0	0000	0000
1	0001	1	1	1	1	0001	0001
2	0010	2	2	2	2	0010	0010
3	0011	3	3	3	3	0011	0011
4	0100	4	4	4	4	0100	0100
5	0101	5	5	5	5	1011	0101
6	0110	6	6	6	6	1100	0110
7	0111	7	7	7	7	1101	0111
8	1000	10	8	-7	-8	1110	1000
9	1001	11	9	-6	-7	1111	1001
10	1010	12	A	-5	-6		
11	1011	13	B	-4	-5		
12	1100	14	C	-3	-4		
13	1101	15	D	-2	-3		
14	1110	16	E	-1	-2		
15	1111	17	F	-0	-1		

Flip-Flop D

Figure 7-15 Positive-edge-triggered D flip-flop: (a) circuit design using D latches; (b) function table; (c) logic symbol.



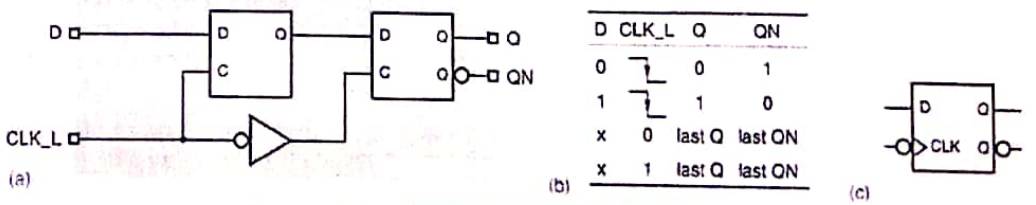
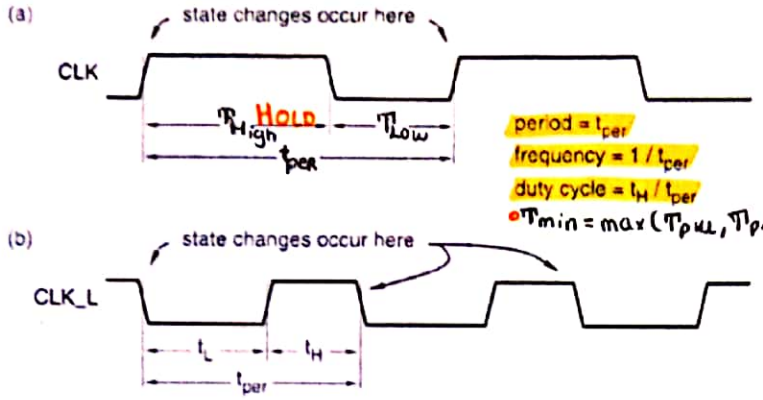


Figure 7-18 Negative-edge triggered D flip-flop: (a) circuit design using D latches; (b) function table; (c) logic symbol.



period = t_{per}
frequency = $1 / t_{per}$
duty cycle = t_H / t_{per}
• $T_{min} = max(T_{pHL}, T_{pLH}) + T_{setup}$ (+ T_{gate})

Figure 7-1
Clock signals:
(a) active high;
(b) active low.

FLIP-FLOPS

- T ➡ comuta apenas quando recebe o impulso do relógio
  ➡ $Q^{(n+1)} = T \cdot \bar{Q}^n + \bar{T} Q^n$ T XOR Q^n
- SR ➡ $Q^{(n+1)} = S + \bar{R} \cdot Q^n$

Mealy => dependem diretamente das entradas externas, enable e do estado atual

Moore => dependem apenas da saída da unidade de memória (estado atual)

Leis

$$\overline{x \cdot y} = \bar{x} + \bar{y}$$

$$\overline{\prod_{i=0}^{n-1} x_i} = \sum_{i=0}^{n-1} \bar{x}_i$$

Mux 2:1

F = (I0·S')+(I1·S)

Morgan

$$\overline{x + y} = \bar{x} \cdot \bar{y}$$

$$\overline{\sum_{i=0}^{n-1} x_i} = \prod_{i=0}^{n-1} \bar{x}_i$$

1ª forma canónica: soma de produtos
$$f(x_0, x_1, \ldots, x_{n-1}) = \sum_{i=0}^{2^n-1} m_i \cdot f_i$$ AND-OR

2ª forma canónica: produto de somas
$$f(x_0, x_1, \ldots, x_{n-1}) = \prod_{i=0}^{2^n-1} (f_i + M_i)$$ OR-AND

3ª forma canónica: produto de produtos
$$f(x_0, x_1, \ldots, x_{n-1}) = \overline{\prod_{i=0}^{2^n-1} \overline{f_i \cdot m_i}}$$ NAND-NAND

4ª forma canónica: soma de somas
$$f(x_0, x_1, \ldots, x_{n-1}) = \overline{\sum_{i=0}^{2^n-1} \overline{f_i + M_i}}$$ NOR-NOR