Multiplxer VHDL descriptions

Tuesday, March 16, 2021 3:34 PM

Alternative VHDL descriptions for 2:1 Multiplexer

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.all;
entity Mux2_1 is
  port(sel    : in  std_logic;
       input0 : in  std_logic;
       input1 : in  std_logic;
       muxOut : out std_logic);
end Mux2_1;
architecture Mux_Proc of Mux2_1 is
begin
  process(sel, input0, input1)
  begin
    if (sel = '0') then
      muxOut <= input0;
    else
      muxOut <= input1;
    end if;
  end process;
end Mux_Proc;
architecture Mux_Proc_case of Mux2_1 is
begin
  process(sel, input0, input1)
  begin
    case sel is
          when '0' => muxOut <= input0;
          when '1' => muxOut <= input1;
          when others => muxOut <= 'X'; -- Important, why?
    end case;
  end process;
end Mux_Proc_case;

-- Concurrent selection
architecture Mux_with_select of Mux2_1 is
begin
  with sel select
          muxOut <= input0 when '0',
                    input1 when '1',
                       'X' when others;   -- Important, why?

end Mux_with_select;
architecture Mux_when of Mux2_1 is
begin
          muxOut <= input0 when sel = '0' else
                    input1 when sel = '1' else
                   'X';
end Mux_when;
```

Alternative VHDL descriptions for 4:1 Multiplexer

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.all;
entity Mux4_1 is
  port(sel    : in  std_logic_vector(1 downto 0) ;
       inputs : in  std_logic_vector(3 downto 0);
       muxOut : out std_logic);
end Mux4_1;
architecture Mux_Proc_case of Mux4_1 is
begin
  process(sel, inputs)
  begin
    case sel is
          when "00" => muxOut <= inputs(0);
          when "01" => muxOut <= inputs(1);
          when "10" => muxOut <= inputs(2);
          when "11" => muxOut <= inputs(3);
          when others => muxOut <= 'X';
      end case;
  end process;
end Mux_Proc_case;
architecture Mux_Proc of Mux4_1 is
begin
  process(sel, inputs)
  begin
    if      (sel = "00") then muxOut <= inputs(0);
      elsif (sel = "01") then muxOut <= inputs(1);
      elsif (sel = "10") then muxOut <= inputs(2);
      elsif (sel = "11") then muxOut <= inputs(3);
    else
      muxOut <= 'X';
    end if;
  end process;
end Mux_Proc;
```

Example simulation