Register with WE

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```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
entity RegN is
      generic(n : natural := 8);
      port (clk : in std_logic;
            WEN : in std_logic;
                  din : in std_logic_vector(n-1 downto 0);
                  dout : out std_logic_vector(n-1 downto 0));
end RegN;
architecture Behavioral of RegN is
begin
      process(clk,WEN)
      begin
            if rising_edge(clk) then
                  if (WEN = '1') then
                        dout <= din;
                  end if;
            end if;
      end process;
end Behavioral;
```