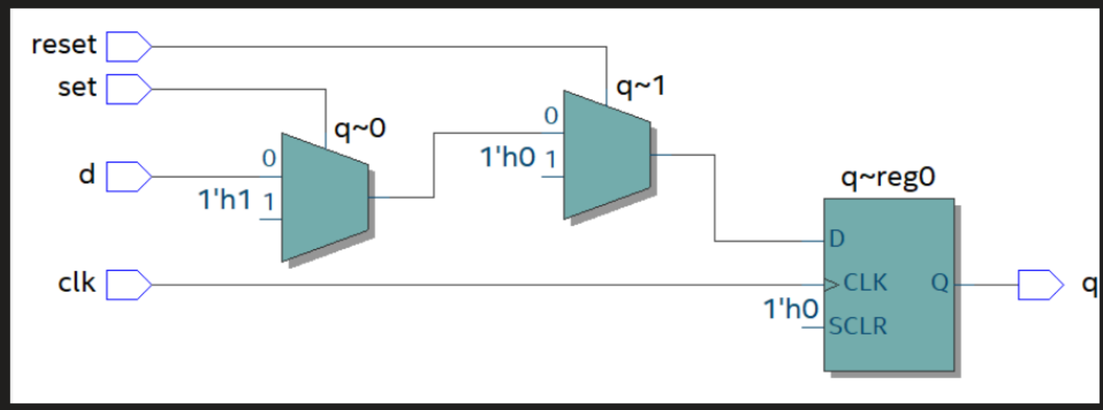
Flip-Flop D

Tuesday, April 13, 2021 3:11 PM

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
entity FlipFlopD is
      port(clk : in std_logic;
             d : in std_logic;
                 reset : in std_logic;
                 set : in std_logic;
             q : out std_logic);
end FlipFlopD;
--architecture Behavioral of FlipFlopD is
--begin
--    process( clk )
--    begin
--          if( rising_edge(clk) ) then
--                if (reset = '1') then q <= '0'; -- sync reset
--                elsif (set = '1') then q <= '1'; -- sync set
--                else q <= d;
--                end if;
--          end if;
--    end process;
--end Behavioral;
```

Synchronous Reset/Set. Reset has priority



Asynchronous Reset/Set. Reset has priority

```
architecture ASyncBehavioral of FlipFlopD is
begin
      process( reset, set, clk )
      begin
            if (reset = '1') then q <= '0'; -- Async reset
            elsif (set = '1') then q <= '1'; -- Async set
            elsif( rising_edge(clk) ) then q <= d;
            end if;
      end process;
end ASyncBehavioral;
```