Priority Encoders

Tuesday, March 16, 2021 4:44 PM

Example VHDL description for 4:2 Priority Encoder

```
library IEEE;
use IEEE.STD_LOGIC_1164.ALL;

entity PENC4_2 is
   port (decodeIn  : in std_logic_vector(3 downto 0);
         encodeOut : out std_logic_vector(1 downto 0);
         validOut : out std_logic);
end entity PENC4_2;

architecture Behavioral of PENC4_2 is
begin
   process(decodeIn)
     begin
          if    decodeIn(3) = '1' then encodeOut <= "11";
          elsif decodeIn(2) = '1' then encodeOut <= "10";
elsif decodeIn(1) = '1' then encodeOut <= "01";
else  encodeOut <= "00";
end if;
     end process;
          validOut <= '0' when decodeIn = "0000" else '1';

end architecture Behavioral;
```

Example simulation