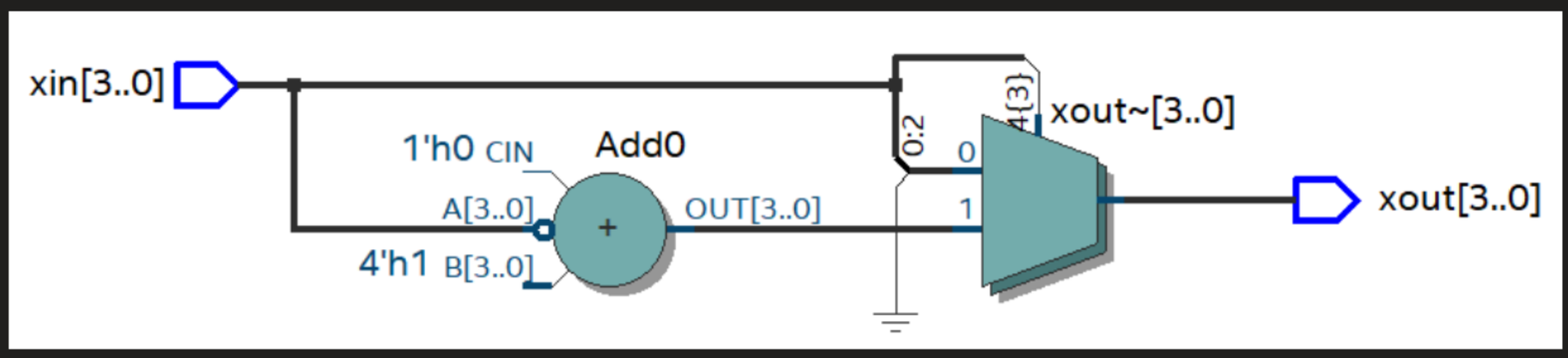
4 bit Absolute Value module

Tuesday, March 23, 2021 7:30 PM

```
library IEEE;
use IEEE.STD_LOGIC_1164.all;
use IEEE.NUMERIC_STD.all;
entity AbsValue is
      port (xin : in  std_logic_vector(3 downto 0);
            xout: out std_logic_vector(3 downto 0));
end AbsValue;
architecture Behav of AbsValue is
begin
      xout <= std_logic_vector(unsigned(not xin)+1) when xin(3) = '1' else
              xin;
end;
```



Example Simulation