Decoder Exercices

Tuesday, March 16, 2021 2:47 PM

1. Analyze the logic diagram and fullfil the truth table
2. Write a VHDL model to describe the 74138, 3:8 decoder.
3. Simulate the block.
4. Use a structural approach to write a VHDL model for a 4:16 decoder with enable and active-low outputs based on the previous module.

74138 Truth Table

G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7