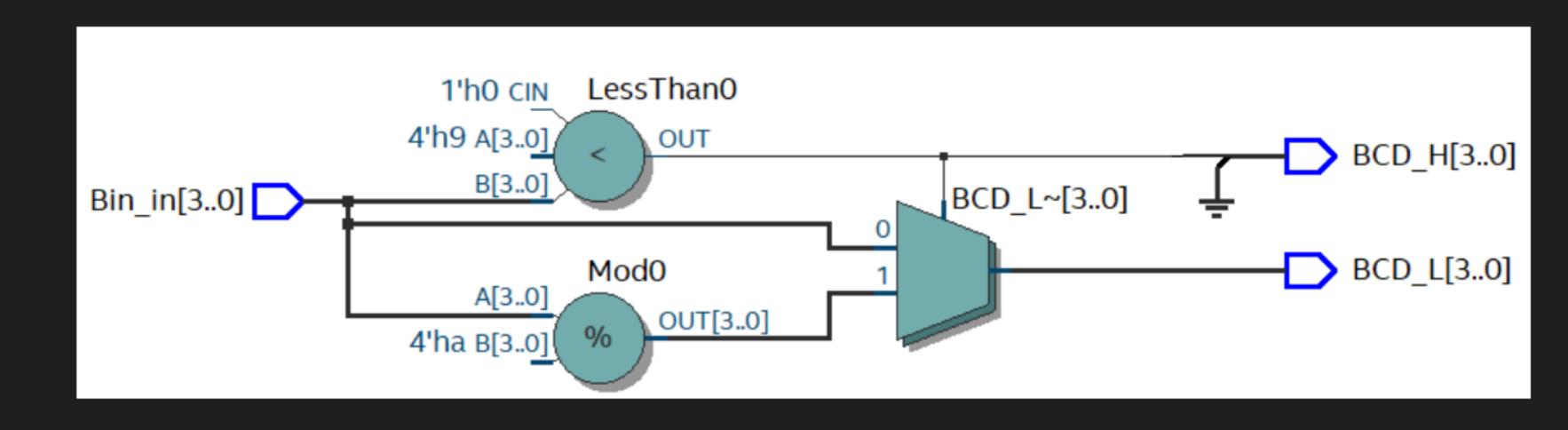
4 bit binary 2 bcd converter

```
Tuesday, March 23, 2021 7:21 PM
library IEEE;
use IEEE.STD LOGIC 1164.all;
use IEEE.NUMERIC STD.all;
entity bin2BCD is
   BCD L : out std logic vector(3 downto 0);
        BCD H : out std logic vector(3 downto 0));
end bin2BCD;
architecture Behavioral of bin2BCD is
begin
 process(Bin in)
 begin
   if unsigned(Bin in) > 9 then
     BCD H <= "0001";
     BCD L <= std logic vector(unsigned(Bin in) rem 10);
   else
     BCD H <= "0000";
     BCD L <= Bin in;
   end if;
  end process;
end Behavioral;
```



Example Simulation

Master Time Bar: 0 ps			Pointer:					Interval:			Start:		
	Nama	Value at	0 ps	80.0 ns	160 _: 0 ns	240 _: 0 ns	320 _: 0 ns	400 _i 0 ns	480 _i 0 ns	560 _i 0 ns	640 _: 0 ns	720 <mark>,</mark> 0 ns	800 _; 0 ns
	Name	0 ps	0 ps										
>	Bin_in	B 0000	0000	0001 🗶 0	010 X 0011 X	0100 \(\) 0101	X 0110 X	0111 1000	X 1001 X	1010 1011	X 1100 X 1101	1110	1111 🔾 00
₩ >	BCD_H	B 0000				0000			X		0001		
₩ >	BCD_L	B 0000	0000	0001 🗶 0	010 X 0011 X	0100 × 0101	X 0110 X	0111 1000	X 1001 X	0000 0001	X 0010 X 0011	0100	0101 🔾 00
	·												