Decoder Exercises

23 de março de 2021 12:11

Exercise 1

74138 TRUTH TABLE

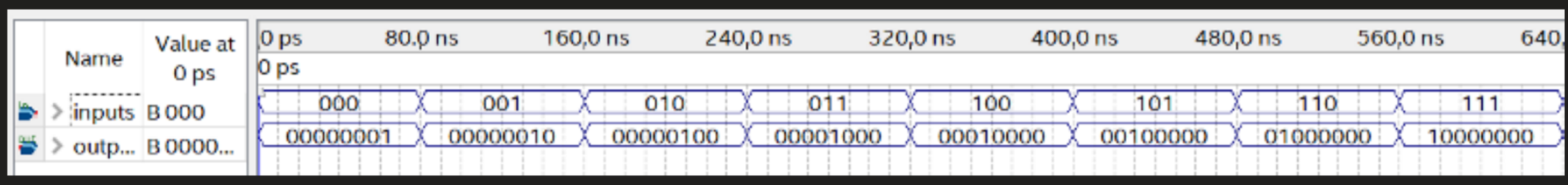
G1	G2A	G2B	C	B	A	Y0	Y1	Y2	Y3	Y4	Y5	Y6	Y7
1	X	X	X	X	X	1	1	1	1	1	1	1	1
X	1	X	X	X	X	1	1	1	1	1	1	1	1
X	X	0	X	X	X	1	1	1	1	1	1	1	1
0	0	1	0	0	0	0	1	1	1	1	1	1	1
0	0	1	1	0	0	1	0	1	1	1	1	1	1
0	0	1	0	1	0	1	1	0	1	1	1	1	1
0	0	1	1	1	0	1	1	1	0	1	1	1	1
0	0	1	0	0	1	1	1	1	1	0	1	1	1
0	0	1	1	0	1	1	1	1	1	1	0	1	1
0	0	1	0	1	1	1	1	1	1	1	1	0	1
0	0	1	1	1	1	1	1	1	1	1	1	1	0

1 - High
0 - Low
X - Don't Care

Exercise 2

```vhdl
library IEEE;
use IEEE.STD_LOGIC_1164.all;
entity Dec3_8 is
    port(inputs  : in  std_logic_vector(2 downto 0);
         outputs : out std_logic_vector(7 downto 0));
end Dec3_8;
architecture Boolean_Expression of Dec3_8 is
begin
    outputs(0) <= ( not inputs(2))  and (not inputs(1))  and (not inputs(0));
    outputs(1) <= ( not inputs(2))  and (not inputs(1)) and (    inputs(0));
    outputs(2) <= ( not inputs(2))  and (    inputs(1)) and (not inputs(0));
    outputs(3) <= ( not inputs(2))  and (    inputs(1)) and (    inputs(0));
    outputs(4) <= (     inputs(2))  and (not inputs(1)) and (not inputs(0));
    outputs(5) <= (     inputs(2))  and (not inputs(1)) and (    inputs(0));
    outputs(6) <= (     inputs(2))  and (    inputs(1)) and (not inputs(0));
    outputs(7) <= (     inputs(2))  and (    inputs(1)) and (    inputs(0));
end Boolean_Expression;
```

Exercise 3



Exercise 4