Digital Logic Gate Simulation
Assignment 1
ELEE 2640

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Date Performed: January 13, 2024
Instructor: Professor Paulik

1 Objective

First Objective

Become familiar with Logic gates.

Second Objective

Be able to simulate Combinational Logic Functions using Multisim.

2 Standard Logic Gates Used

2-INPUT AND	74LS08D
2-INPUT OR	74LS32D
2-INPUT NOT	74LS04D
2-INPUT NAND	74LS00D
2-INPUT NOR	74LS02D

3 Requirements

One-Chip Logic Circuits

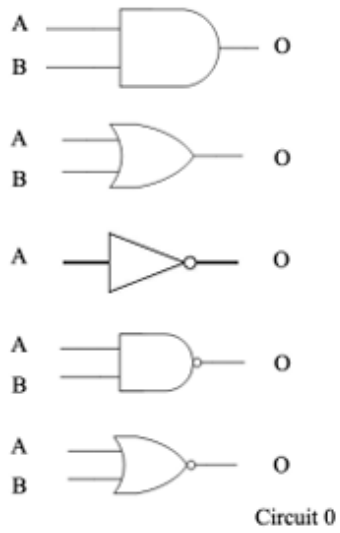

Figure 1: Circuit 0

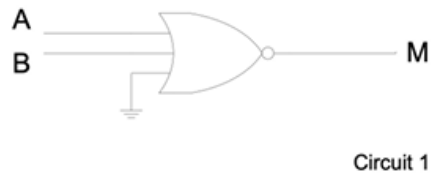

Figure 2: Circuit 1

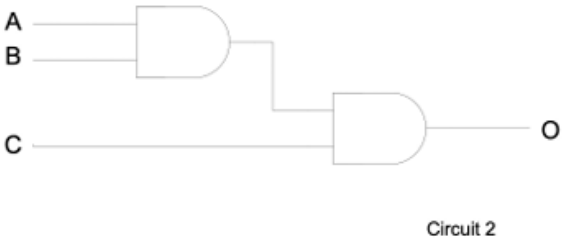

Figure 3: Circuit 2

Two-Chip Logic Circuits

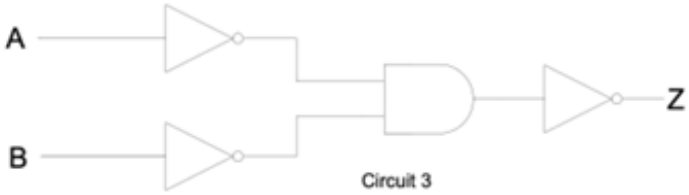

Figure 4: Circuit 3

Three-Chip Logic Circuits

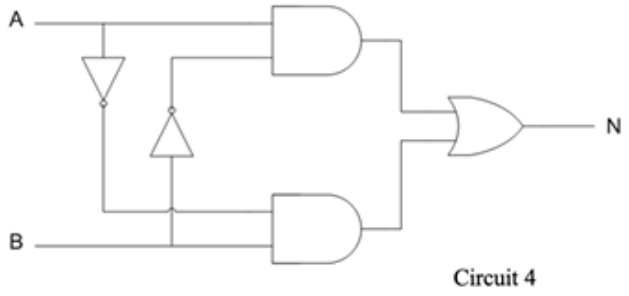

Figure 5: Circuit 4

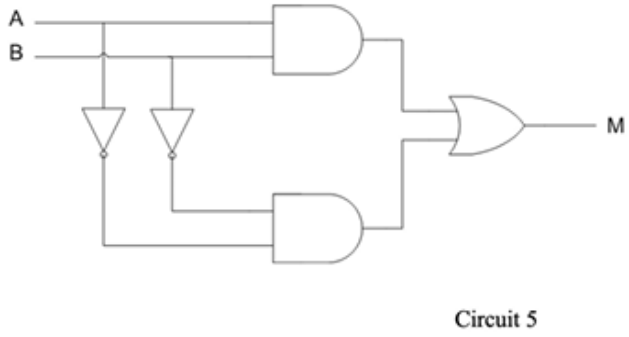

Figure 6: Circuit 5

Additional Circuits

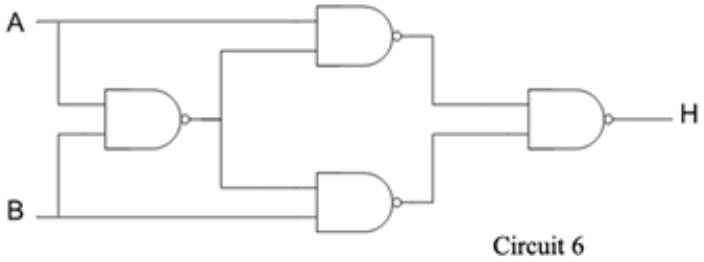

Figure 7: Circuit 6

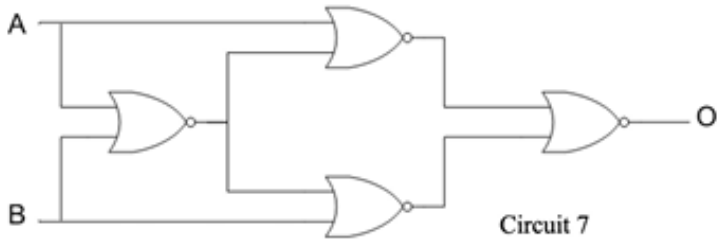

Figure 8: Circuit 7

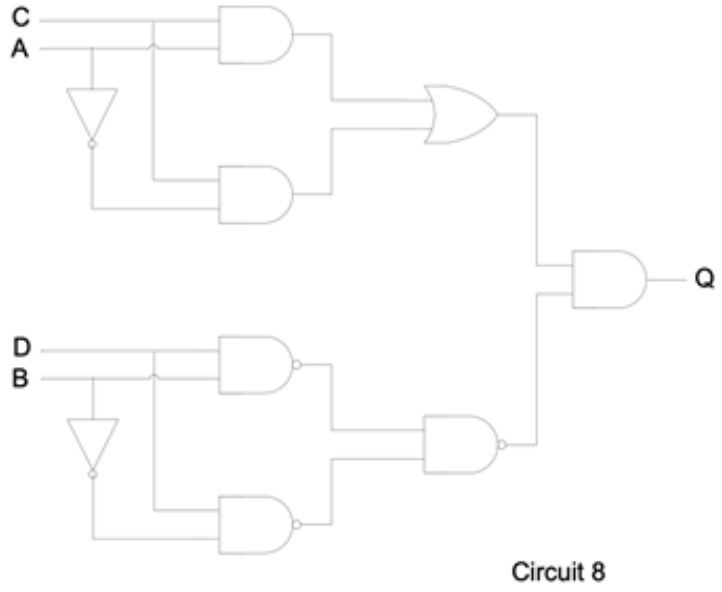

Figure 9: Circuit 8

4 Experiment

One-Chip Logic Circuits

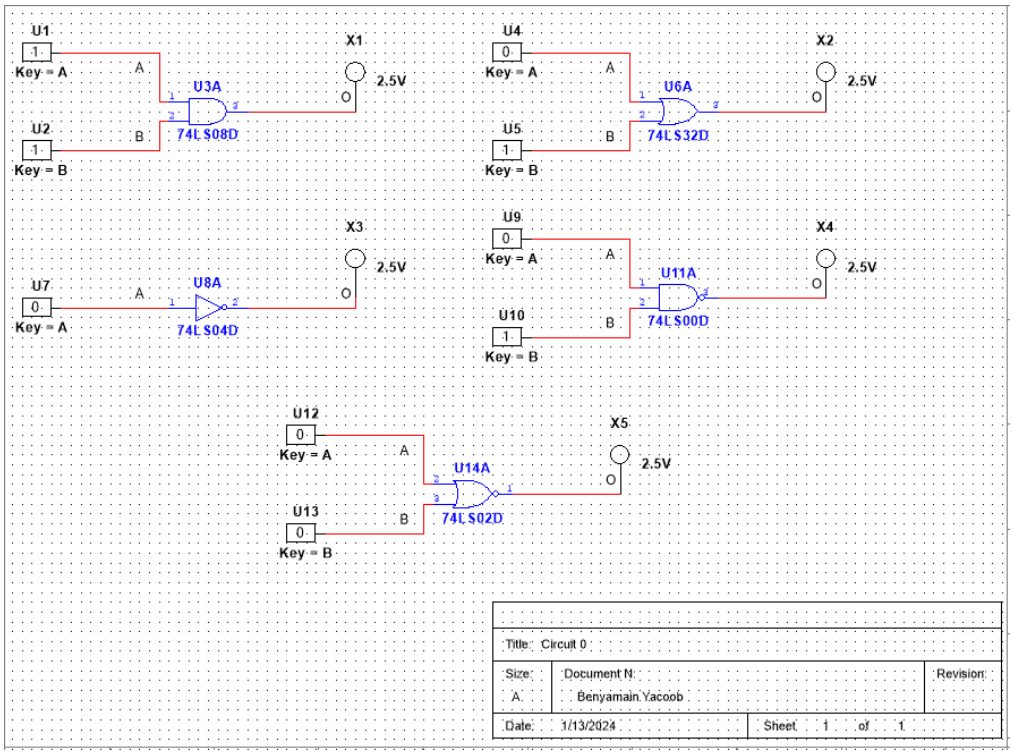

Figure 10: Circuit 0

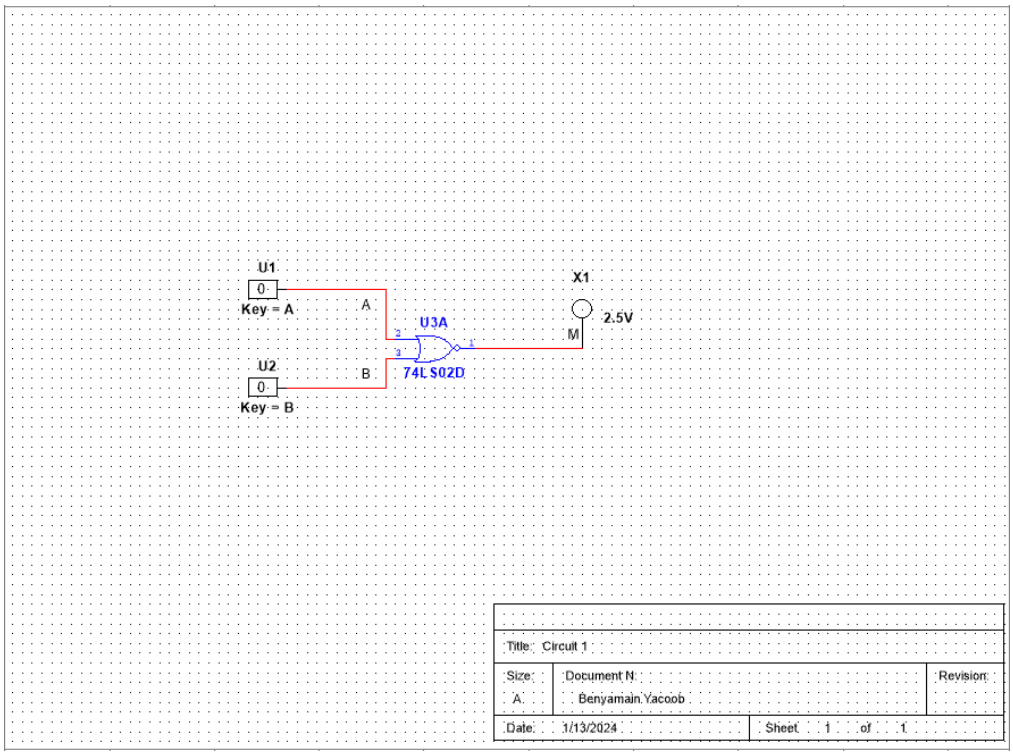

Figure 11: Circuit 1

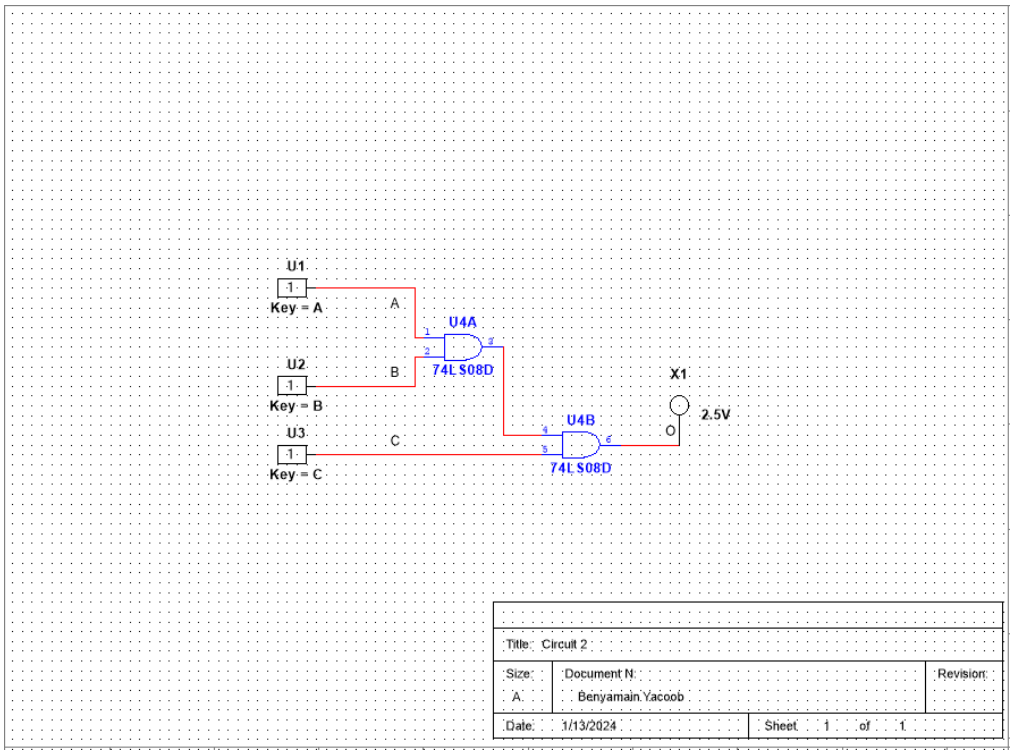

Figure 12: Circuit 2

Two-Chip Logic Circuits

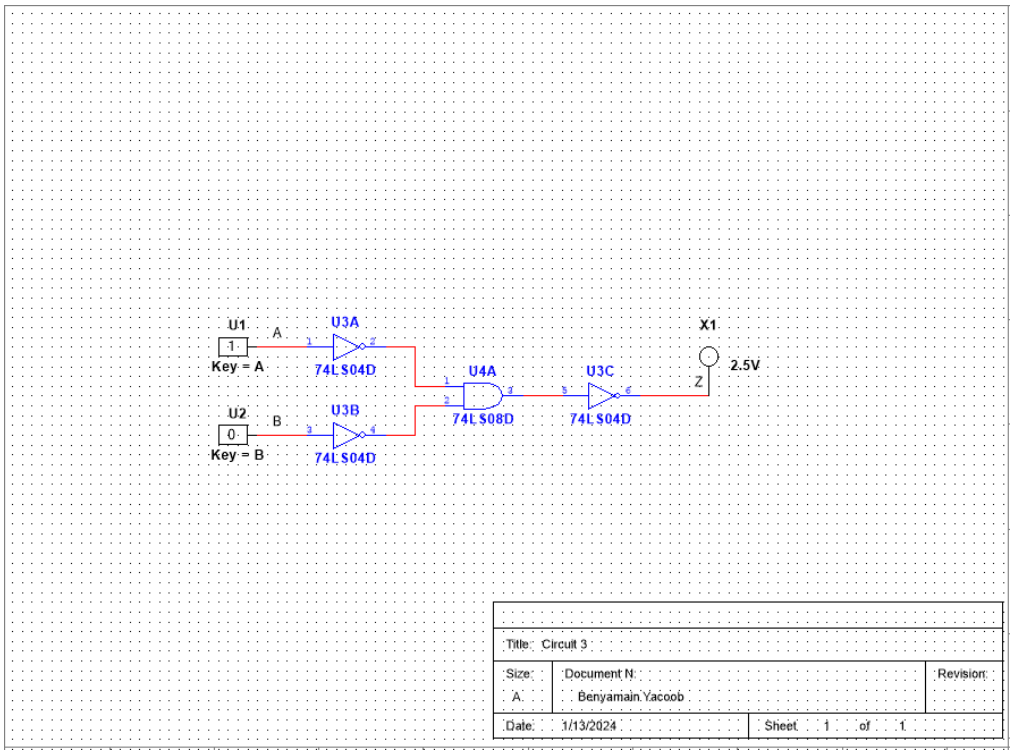

Figure 13: Circuit 3

Three-Chip Logic Circuits

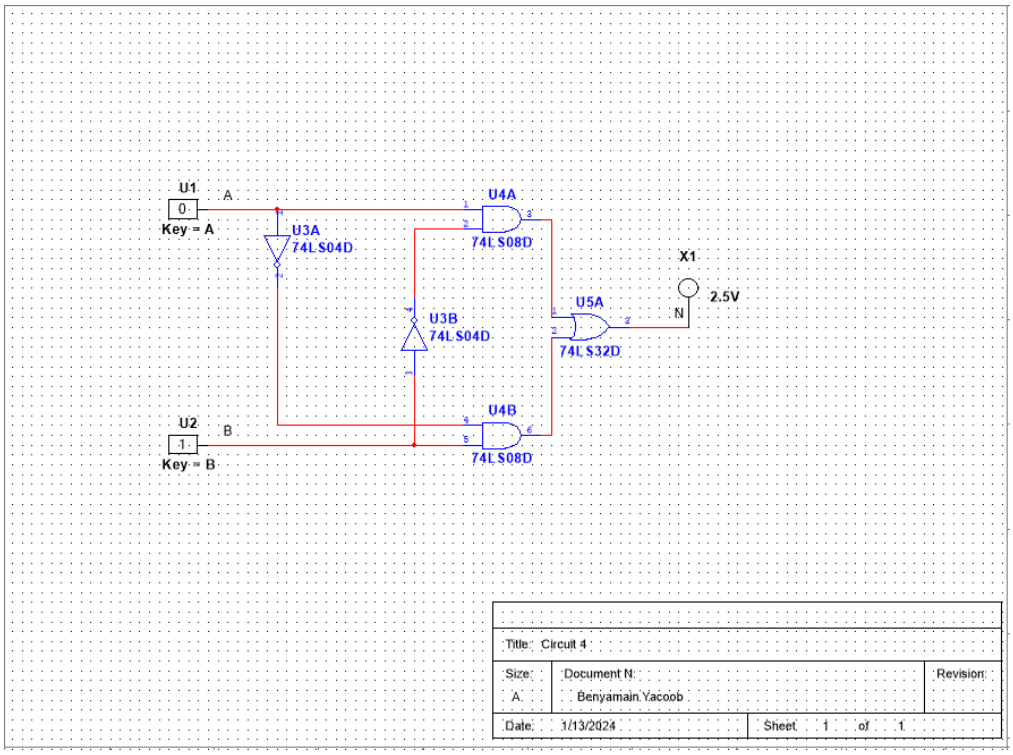

Figure 14: Circuit 4

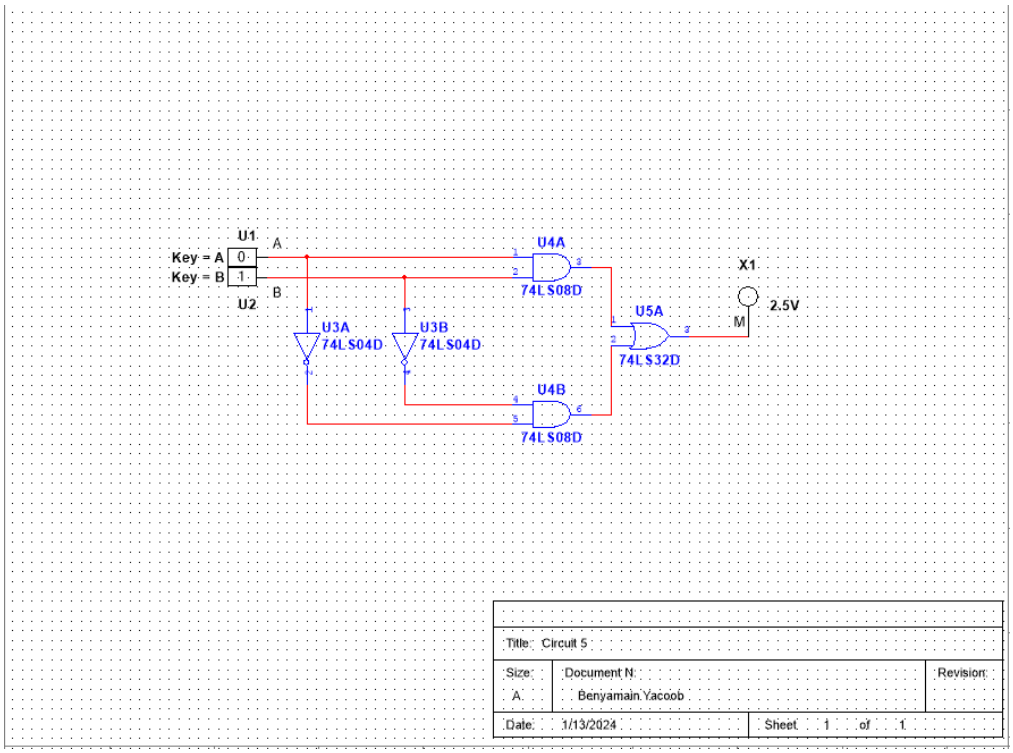

Figure 15: Circuit 5

Additional Circuits

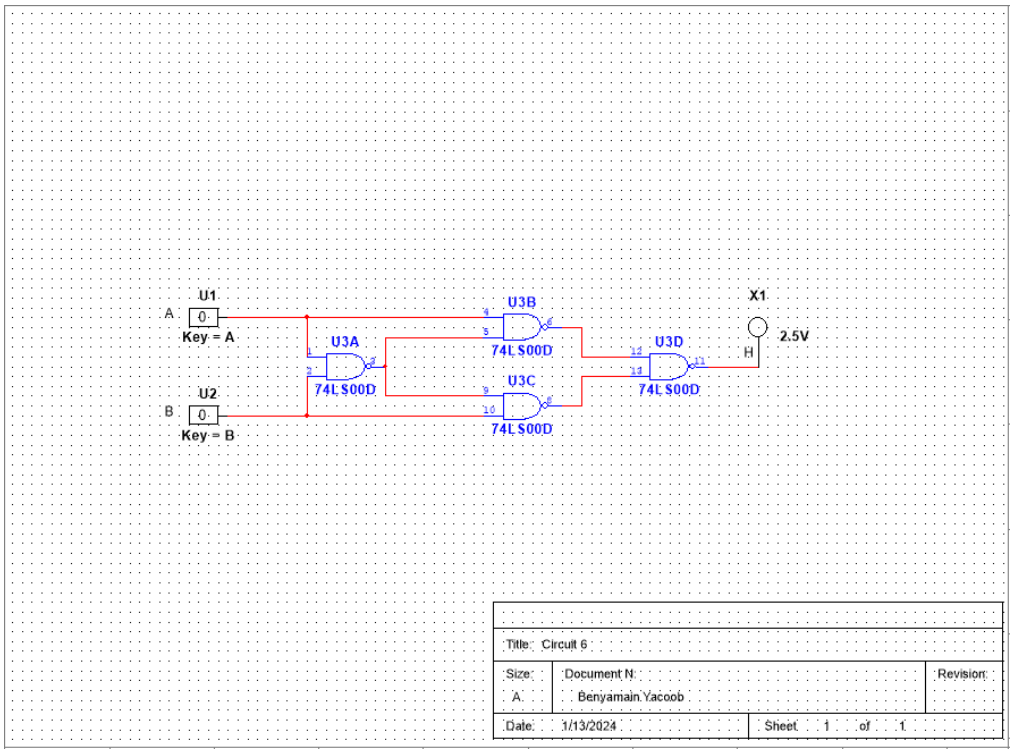

Figure 16: Circuit 6

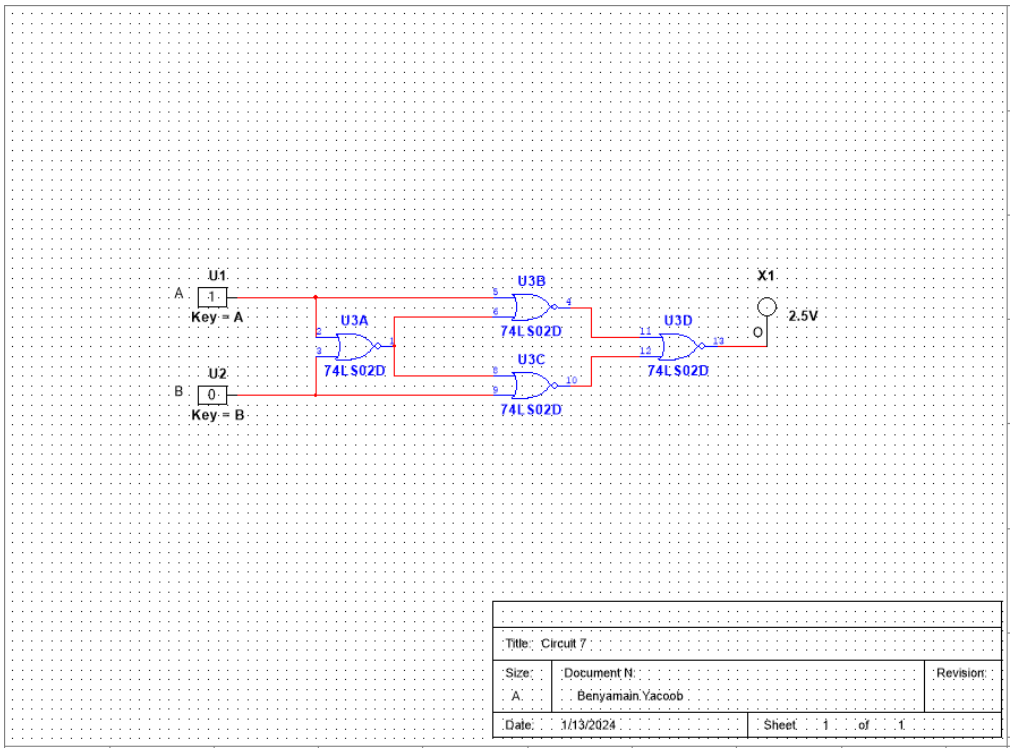

Figure 17: Circuit 7

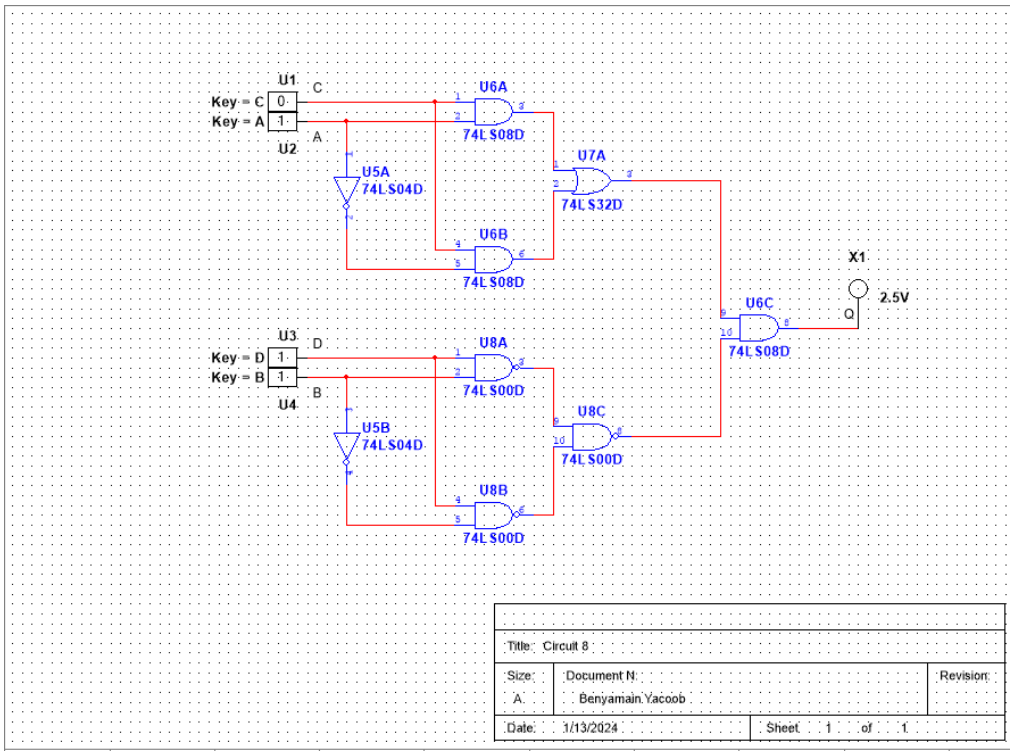

Figure 18: Circuit 8

5 Results and Conclusions

This section discusses the results of the digital logic gate simulation experiments. The discussion provides in-depth explanations of the results and reconciling any discrepancies between the results and theoretical expectations. It also explores potential sources of error and discusses the accuracy of the tests, the debugging process, and what was learned from these experiences.

Started with the first logic circuit, found through Multisim's component database, some interactive input/output, and an indicator. Respective to each one that was mentioned before, an "Interactive Digital Constant" and "Red Probe" were used. The input keys on the interactor were remapped to be different from each other to indicate independence. For each input, a corresponding text label was created and their label names remained consistent with the assignment's labels. The output was also given a text label as well. Lastly, navigated through Multisim to find a property to globally enable package pin names to visually show them and added a title block to name the logic circuit. Next, searched for the name of the chip that the assignment instructed and connected the components altogether. To be efficient, the first logic circuit was copied and pasted multiple times, and each gate

was substituted with the one provided in the assignment. After watching some tutorials, a “Logic Converter” was used to see consistencies between the red probe lighting up and the computed truth table(s). Each input was mapped to the first eight connectors and the output to the last connector.

Errors like mislabeling of the individual circuits were addressed by using the Multisim toolkit that allows the user to go into advanced RefDes configurations and renumber each component appropriately. The source of the problem was caused by copying circuits multiple times through the keyboard shortcut the software provides. Utilizing the “Logic Converter” feature was also not functioning the way it was intended to. It turned out to be a fault of the user, with their attempts to connect the converter to the circuit when interactive input(s) and indicators were still connected themselves. The problem was solved after removing said components and the input and output gates were mapped correctly on the converter device. The key lessons learned were new users are almost always going to run into errors, but it is their responsibility to either find external documentation or experiment with Multisim in hopes of solving their issue(s).

One-Chip Logic Circuits

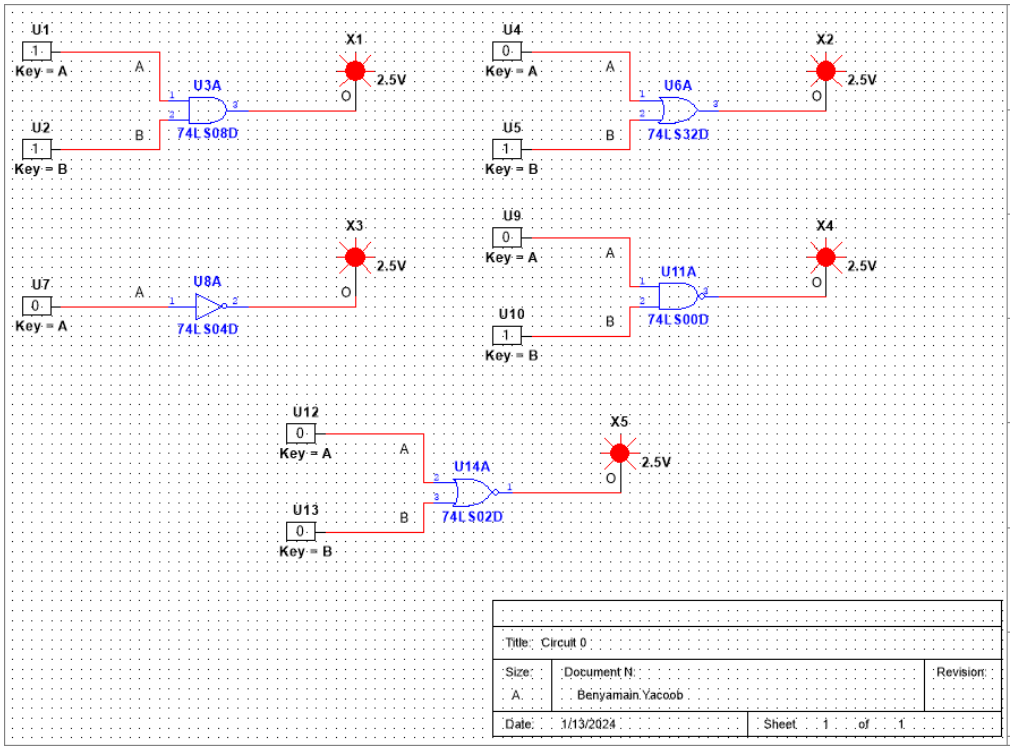

Figure 19: Circuit 0

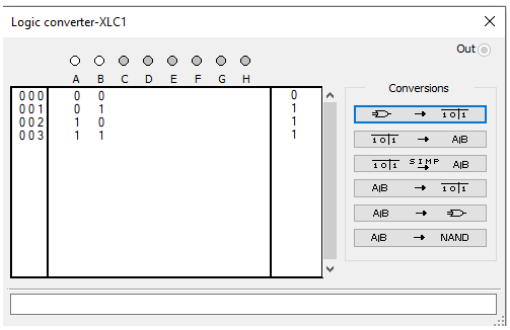

Figure 20: Truth Table for Circuit 0

$$A'B + AB' + AB = O \tag{1}$$

$$A + B = O \tag{2}$$

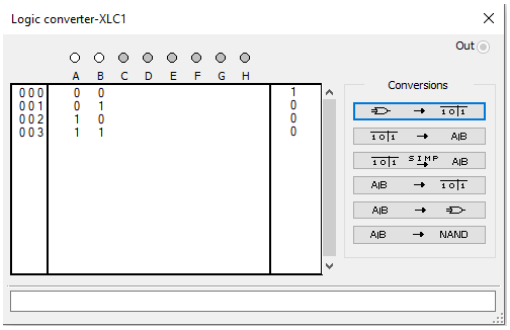

Figure 21: Truth Table for Circuit 0

$$A'B' = O \tag{3}$$

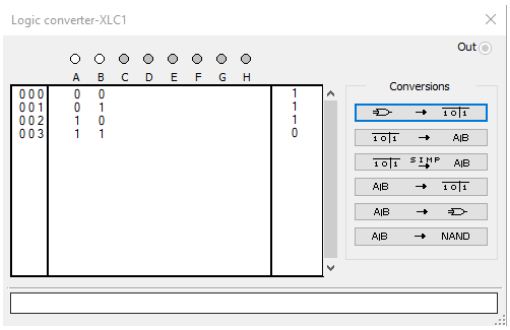

Figure 22: Truth Table for Circuit 0

$$A'B' + A'B + AB' = O \tag{4}$$

$$A' + B' = O \tag{5}$$

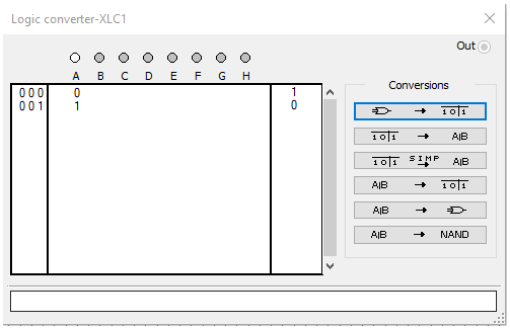

Figure 23: Truth Table for Circuit 0

$$A' = O \tag{6}$$

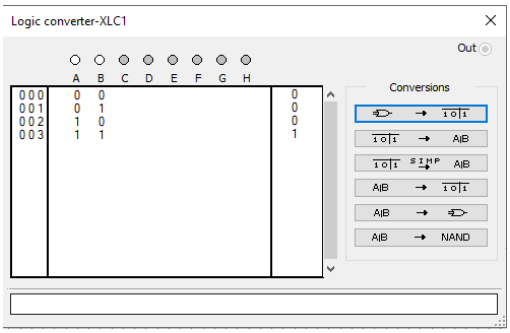

Figure 24: Truth Table for Circuit 0

$$AB = O \tag{7}$$

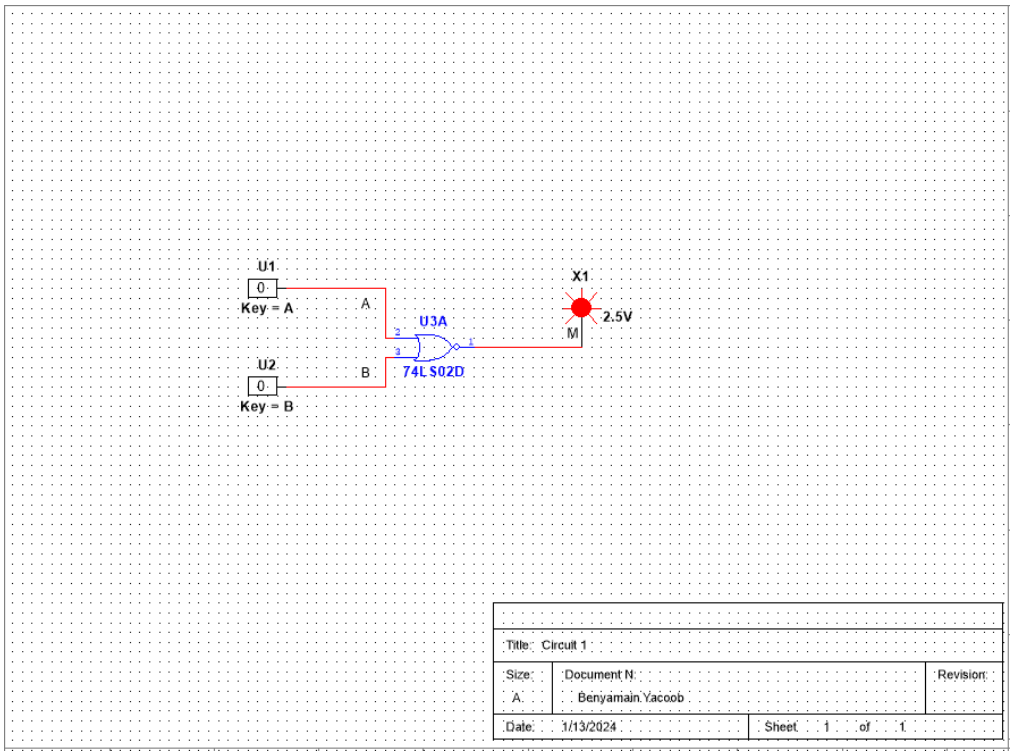

Figure 25: Circuit 1

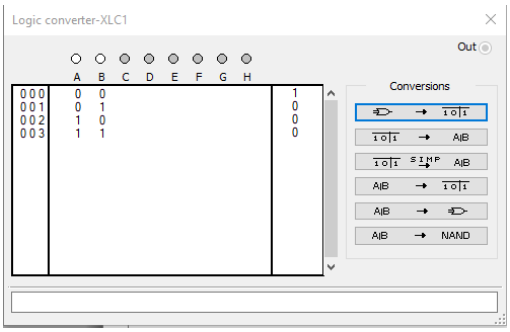

Figure 26: Truth Table for Circuit 1

$$A'B' + A'B + AB' = M \tag{8}$$

$$A' + B' = M \tag{9}$$

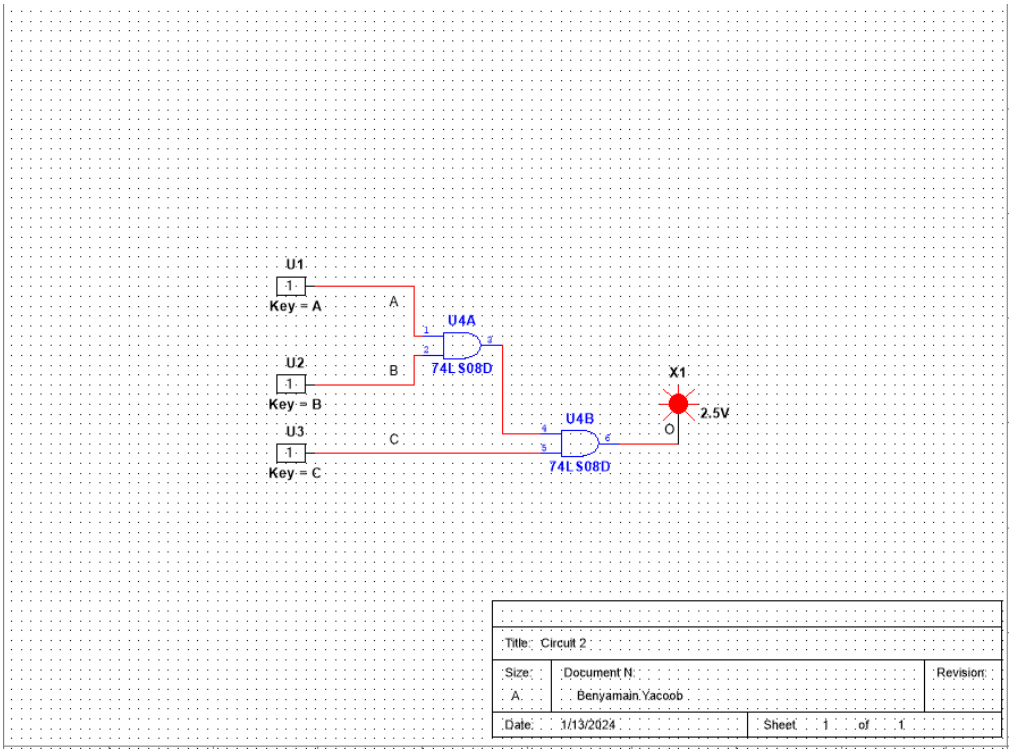

Figure 27: Circuit 2

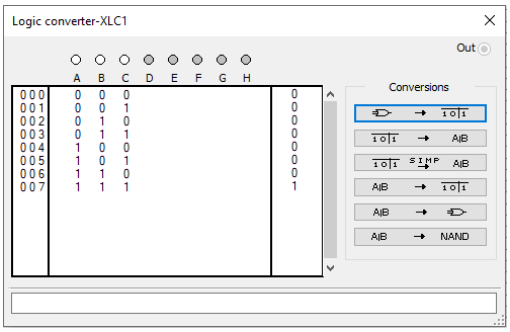

Figure 28: Truth Table for Circuit 2

$$ABC = O \tag{10}$$

The functionality of the logic circuits[19, 25, 27] were designed to outline the basic gates used for one-chip logic circuits. The simulations confirmed that the indicator received "HIGH" voltage when the probe was lit red. Discrepancies between expected[1, 2, 3] and actual[10, 11, 12] results were addressed by referring to the assignment from time to time to validate the circuit was being produced correctly to account for variations from theoretical expectations. In this case, the design process was easy, but there was a minor discrepancy. It was determining the purpose of a partial arrow drawing[2] that was part of the design. Because there was an inconsistency in that circuit design, which was not found in the others, it was conclusively ignored. Assessing the accuracy of the circuits involved waiting for the probe to be lit red as simulations were running, and computing truth tables[20, 21, 22, 23, 24, 26, 28] to further validate the logic circuit experiments. The derived logic function(s) were also reported.[2, 3, 5, 6, 7, 9, 10]

Two-Chip Logic Circuits

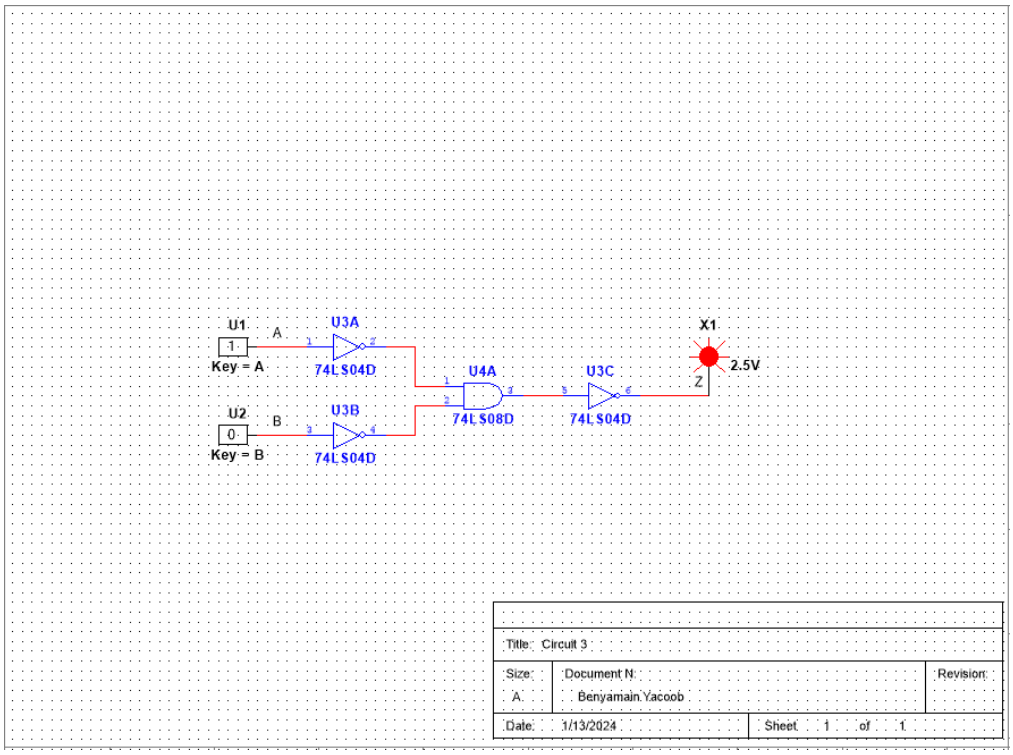

Figure 29: Circuit 3

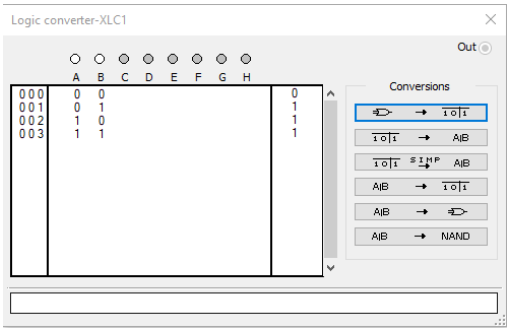

Figure 30: Truth Table for Circuit 3

$$A'B + AB' + AB = Z \tag{11}$$

$$A + B = Z \tag{12}$$

The functionality of the logic circuit[29] is designed to outline the basic gates used for two-chip logic circuits. The simulation confirmed that the indicator received “HIGH” voltage when the probe was lit red. Discrepancies between expected[4] and actual[13] results were addressed by referring to the assignment from time to time to validate the circuit was being produced correctly to account for variations from theoretical expectations. In this instance, the design process was relatively easy, so no discrepancies were found. Assessing the accuracy of the circuit involved waiting for the probe to be lit red as the simulation was running, and computing a truth table[30] to further validate the logic circuit experiment. The derived logic function(s) were also reported.[12]

Three-Chip Logic Circuits

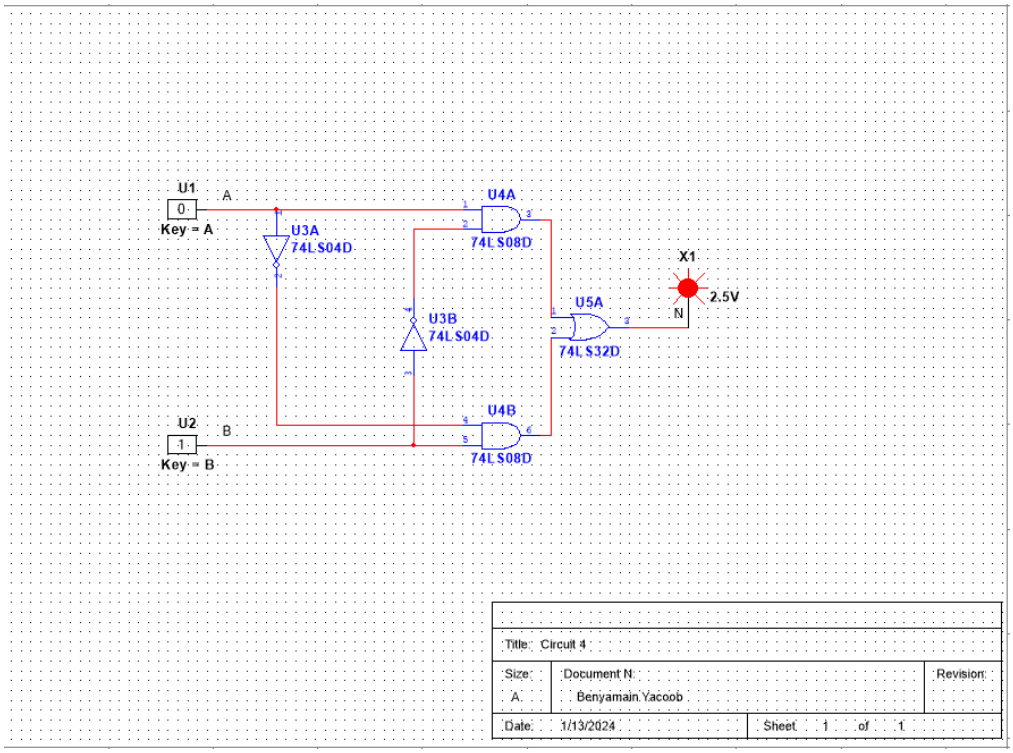

Figure 31: Circuit 4

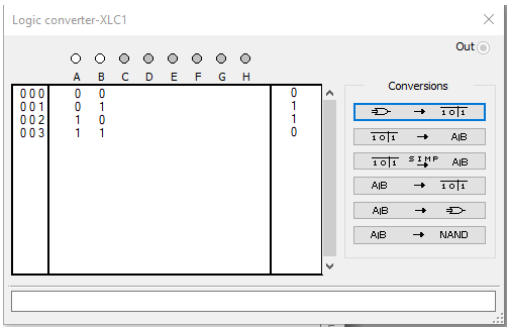

Figure 32: Truth Table for Circuit 4

$$A'B + AB' = N \tag{13}$$

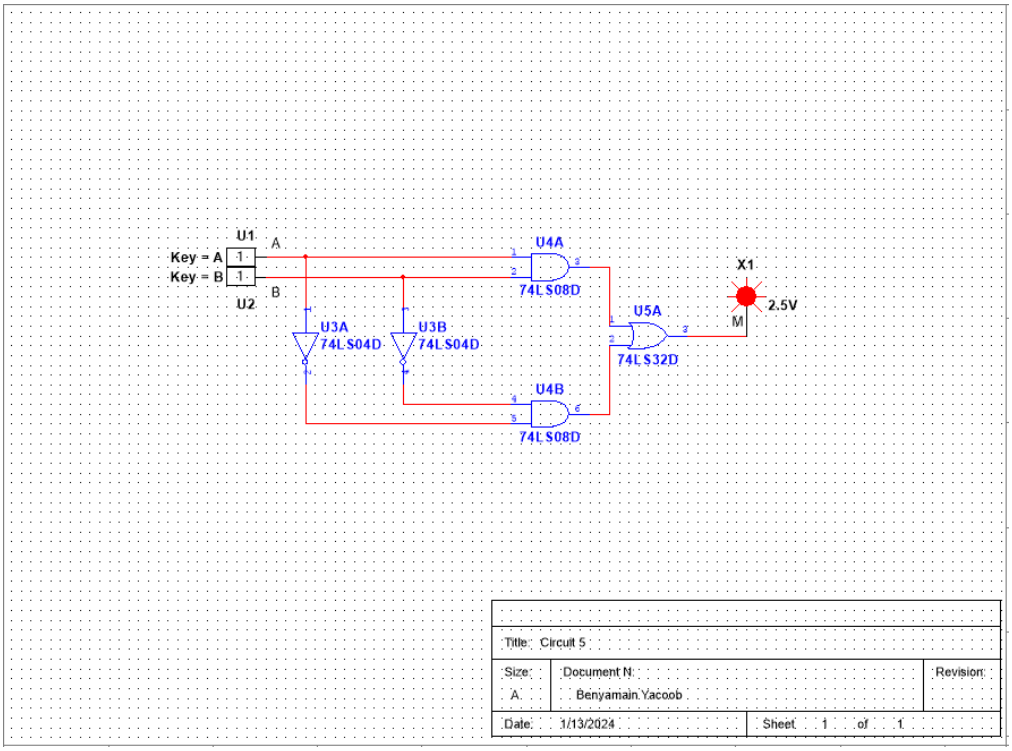

Figure 33: Circuit 5

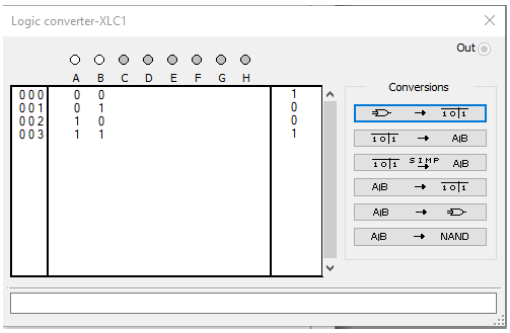

Figure 34: Truth Table for Circuit 5

$$A'B' + AB = M \tag{14}$$

The functionality of the logic circuits[31, 33] were designed to outline the basic gates used for three-chip logic circuits. The simulations confirmed that the indicator received "HIGH" voltage when the probe was lit red. Discrepancies between expected[5, 6] and actual[14, 15] results were addressed by referring to the assignment from time to time to validate the circuit was being produced correctly to account for variations from theoretical expectations. In these instances, the design process was manageable, so no discrepancies were found. Assessing the accuracy of the circuits involved waiting for the probe to be lit red as simulations were running, and computing truth tables[32, 34] to further validate the logic circuit experiments. The derived logic function(s) were also reported.[13, 14]

Additional Circuits

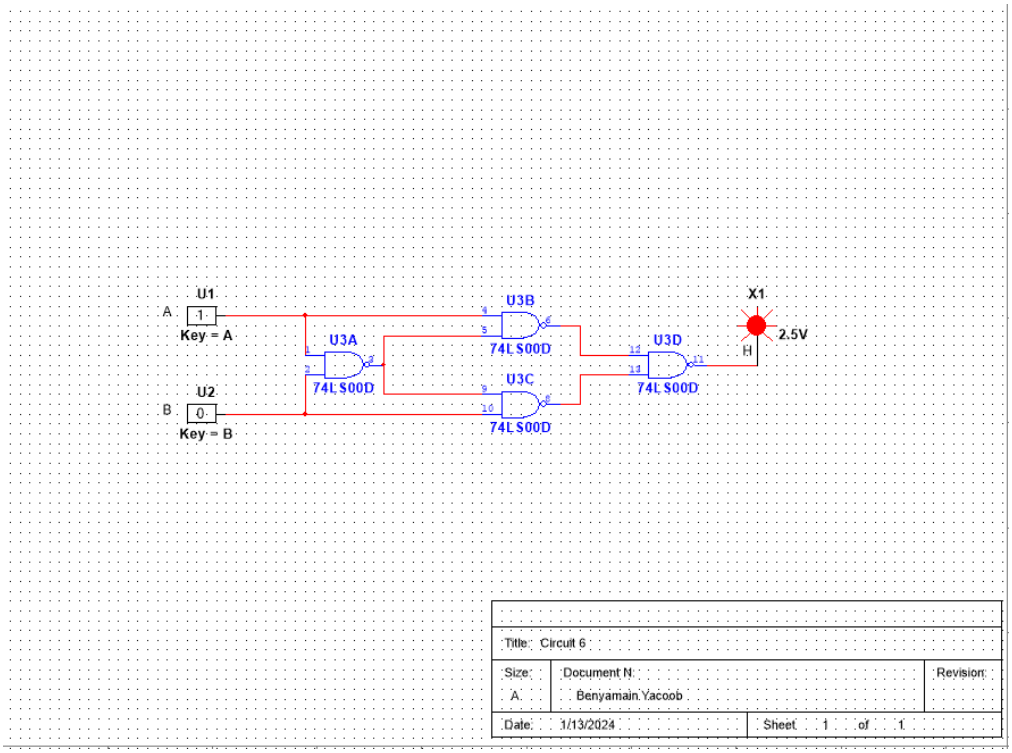

Figure 35: Circuit 6

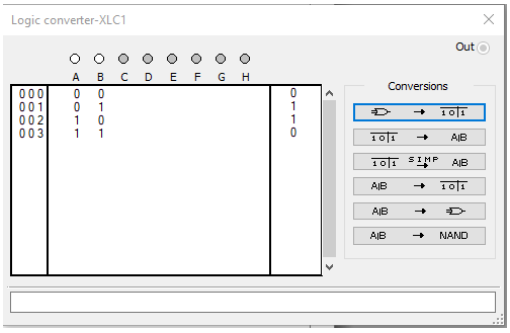

Figure 36: Truth Table for Circuit 6

$$A'B + AB' = H \tag{15}$$

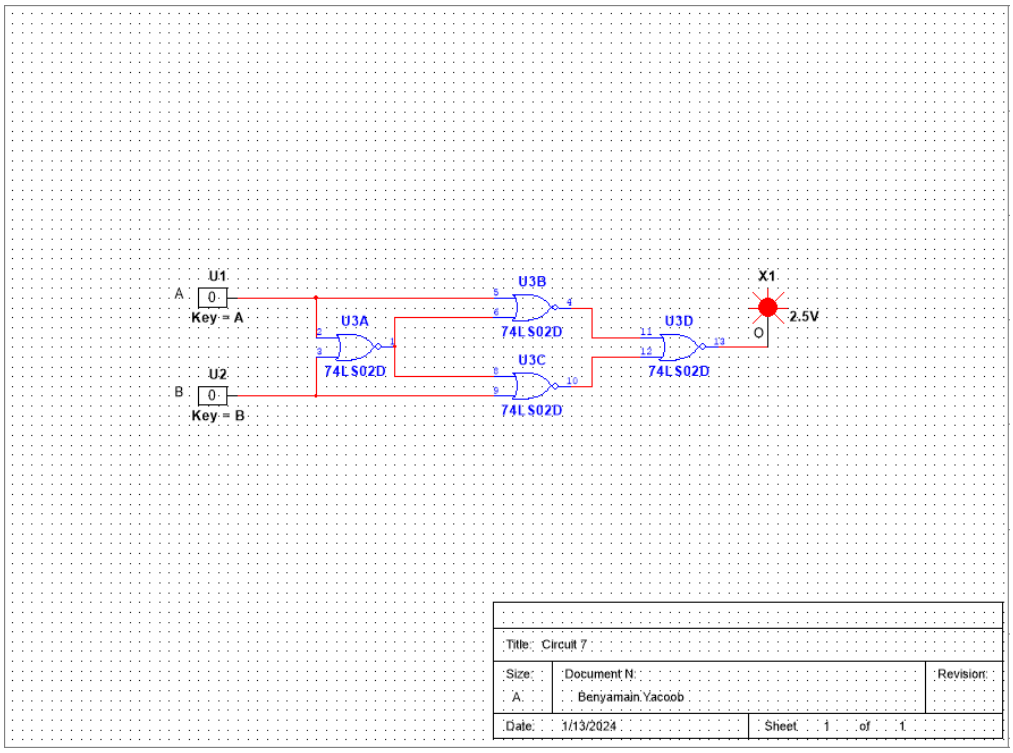

Figure 37: Circuit 7

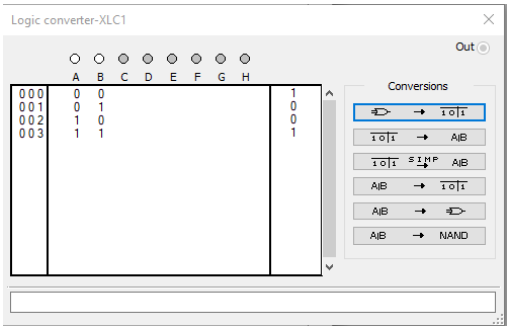

Figure 38: Truth Table for Circuit 7

$$A'B' + AB = O \tag{16}$$

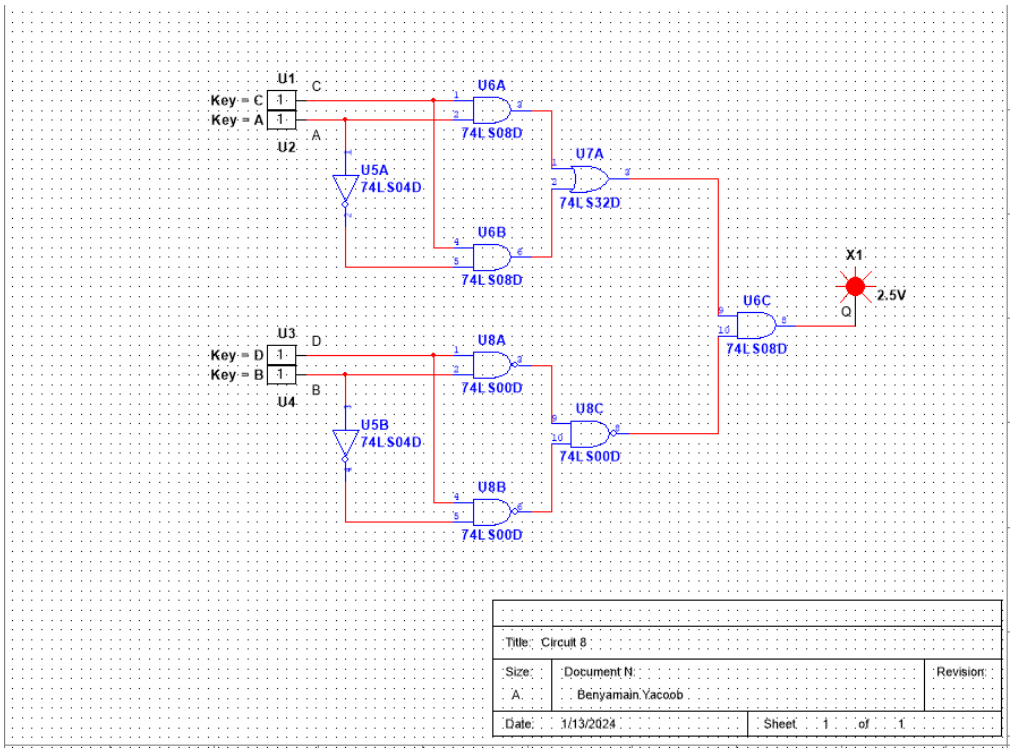

Figure 39: Circuit 8

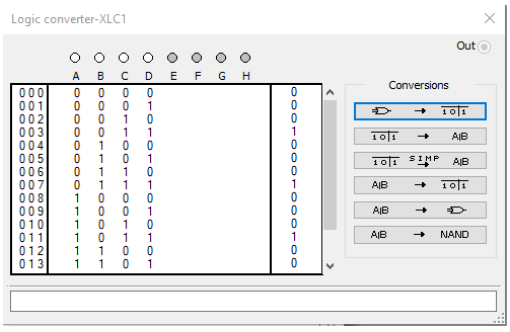

Figure 40: Truth Table for Circuit 8

$$A'B'CD + A'BCD + AB'CD + ABCD = Q \tag{17}$$

$$CD = Q \tag{18}$$

The functionality of the logic circuits[35, 37, 39] were designed to outline the basic gates used for the additional circuits. The simulations confirmed that the indicator received “HIGH” voltage when the probe was lit red. Discrepancies between expected[7, 8, 9] and actual[16, 17, 18] results were addressed by referring to the assignment from time to time to validate the circuit was being produced correctly to account for variations from theoretical expectations. In these instances, the design process was manageable, so no discrepancies were found. Assessing the accuracy of the circuits involved waiting for the probe to be lit red as simulations were running, and computing truth tables[36, 38, 40] to further validate the logic circuit experiments. The derived logic function(s) were also reported.[15, 16, 18]