Digital Logic Gate Simulation Exercise 3
Combinational Logic Seven-Segment Displays
ELEE 2640

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Date Performed:	January 30, 2024
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Contents

1 Objectives

First Objective

Design and simulate advanced combinational circuits using MultiSIM with medium-scale integration (MSI) 7400 series chips.

Second Objective

Investigate the operation of a seven-segment decoder.

Third Objective

Integrate 4-bit full adder with display circuits.

2 Problem Statement

The goal of this simulation assignment is to design and simulate a Digital Decoder IC, specifically focusing on the Binary Coded Decimal (BCD) to seven-segment display. The seven-segment display, whether LED or LCD, is a widely used output device for displaying numerical and alphanumeric characters. In this context, the simulation involves creating a simulation model for a BCD to seven-segment decoder using the 74LS47 Decoder IC.

3 Materials

2-INPUT AND	74LS08N/7408N
2-INPUT OR	74LS32N
2-INPUT XOR	74LS386N/7486N
4-BIT FULL ADDER	74283N
BCD TO SEVEN-SEGMENT DISPLAY	74LS47D

4 Requirements

4-Bit Full Adder

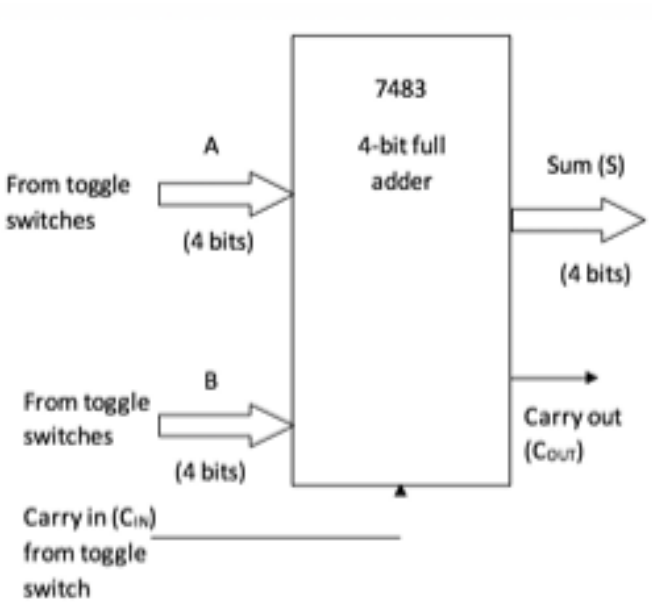

Figure 1: 4-Bit Full Adder Data Flow Diagram

BCD to Seven-Segment Decoder

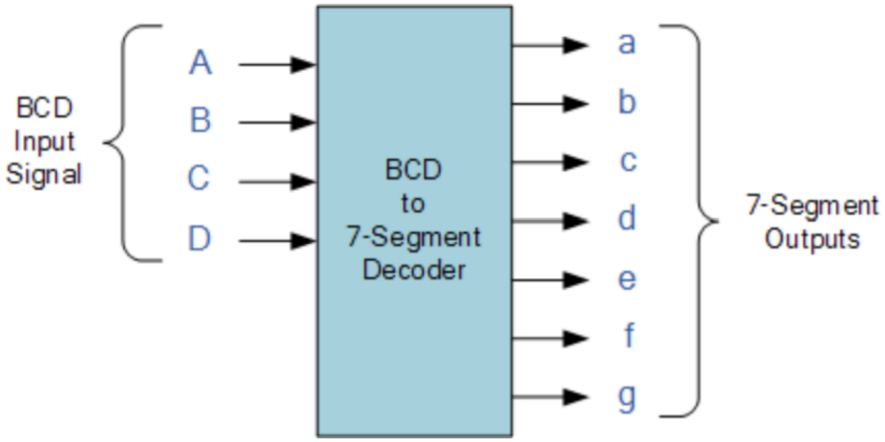

Figure 2: BCD to Seven-Segment Decoder

Seven-Segment Display Format

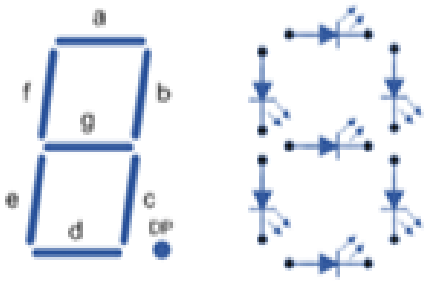

Figure 3: Seven-Segment Display Segments and Diodes

5 Seven-Segment Display

5.1 Seven-Segment Display Truth Table

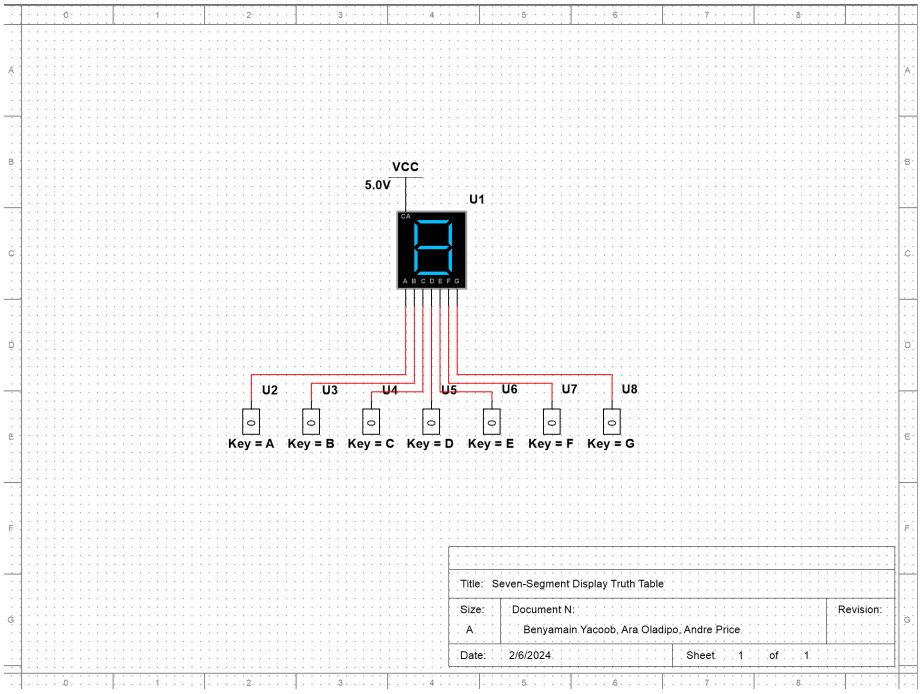

Figure 4: Seven-Segment With Common Anode Display

S_4	S_3	S_2	S_1	Decimal	a	b	c	d	e	f	g
0	0	0	0	0	0	0	0	0	0	0	1
0	0	0	1	1	1	0	0	1	1	1	1
0	0	1	0	2	0	0	1	0	0	1	0
0	0	1	1	3	0	0	0	0	1	1	0
0	1	0	0	4	1	0	0	1	1	0	0
0	1	0	1	5	0	1	0	0	1	0	0
0	1	1	0	6	1	1	0	0	0	0	0
0	1	1	1	7	0	0	0	1	1	1	1
1	0	0	0	8	0	0	0	0	0	0	0
1	0	0	1	9	0	0	0	1	1	0	0
1	0	1	0	A	1	1	1	0	0	1	0
1	0	1	1	B	1	1	0	0	1	1	0
1	1	0	0	C	1	0	1	1	1	0	0
1	1	0	1	D	0	1	1	0	1	1	0
1	1	1	0	E	1	1	1	0	0	0	0
1	1	1	1	F	1	1	1	1	1	1	1

Figure 5: Seven-Segment Display Truth Table

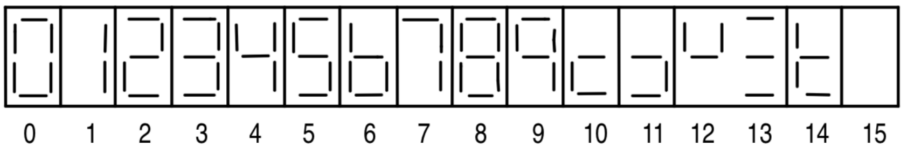

Figure 6: Numerical Designations and Resultant Displays

5.1.1 Results and Analysis Discussion

Using our knowledge of truth tables and what was given to us by the assignment, we were able to create a truth table using the given figures. Since we are going

to be building a seven-segment display, specifically a 74LS47 decoder and a seven-segment display, which has an active-low output, we were able to implement the patterns given, which can be seen below. We will verify this truth table later in the report.

The process of creating seven truth tables for each segment of the seven-segment display turned out to be very tedious, but we were able to complete it with minimal issues. We originally did not understand the goal of this, but we were later able to understand that if we were able to get the simplified Boolean expression for the truth table for the seven segments, we could put them all together into one big circuit and replicate the MultiSIM 74LS47 Decoder IC. The image of our segments, as well as their simplified Boolean expressions and truth tables, is shown below.

5.2 Segment A

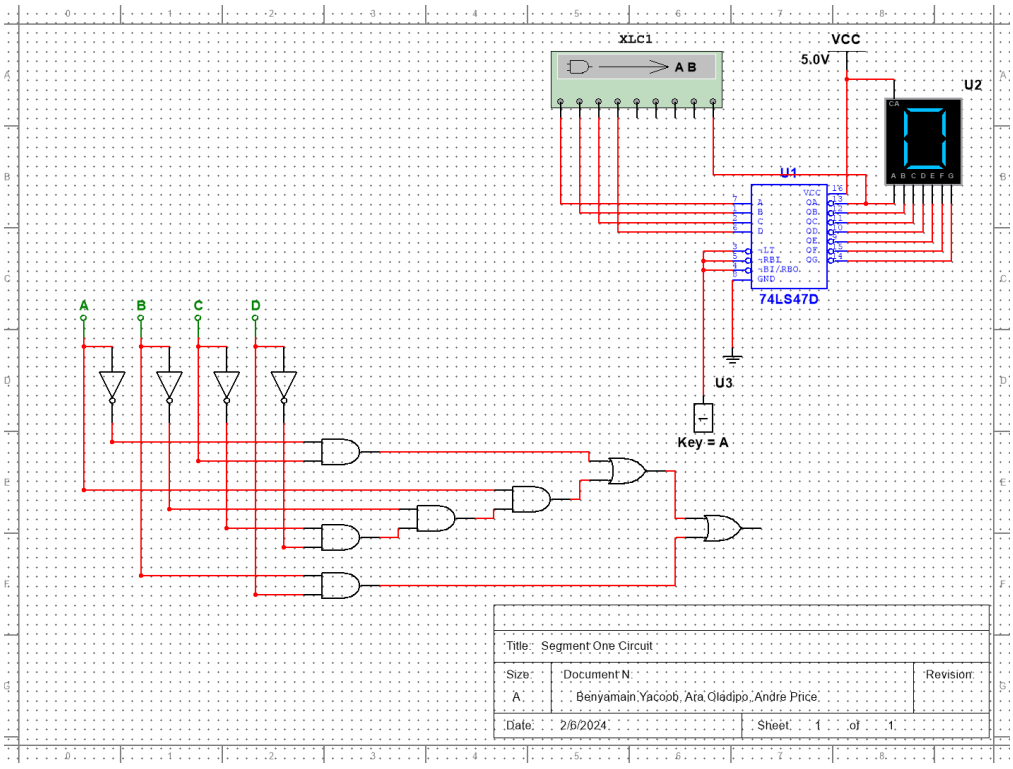

Figure 7: Segment A Logic Converter With Generated Circuit

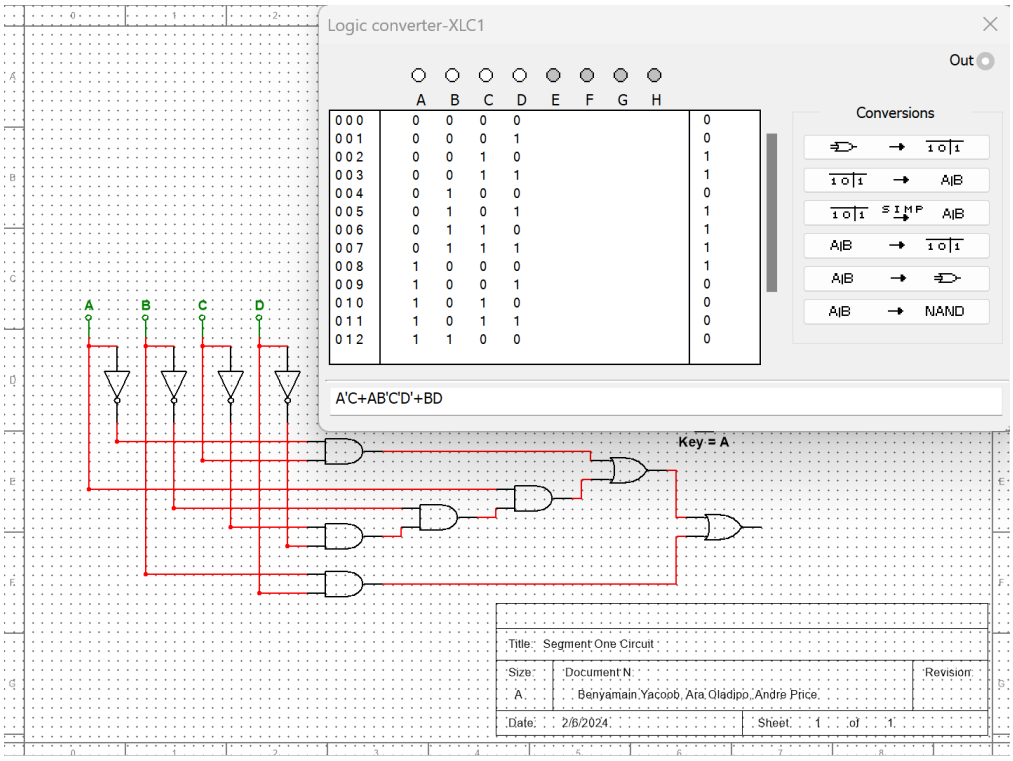

Figure 8: Segment A Circuit Truth Table

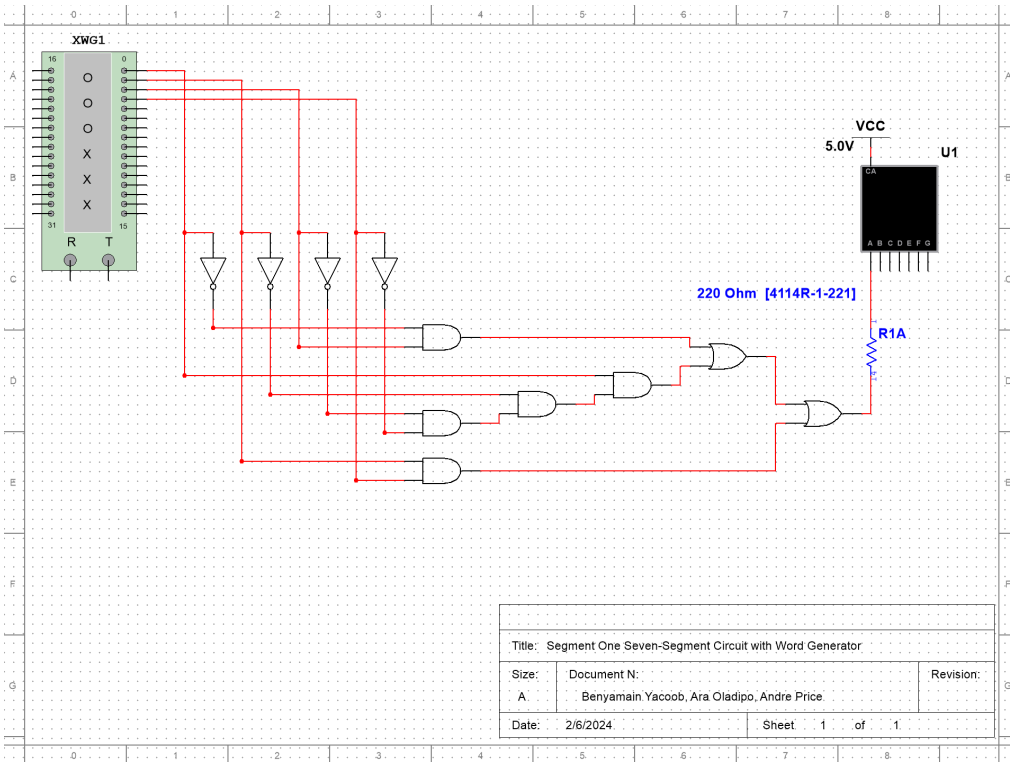

Figure 9: Complete Segment A

$$Y = A'C + AB'C'D' + BD \tag{1}$$

5.3 Segment B

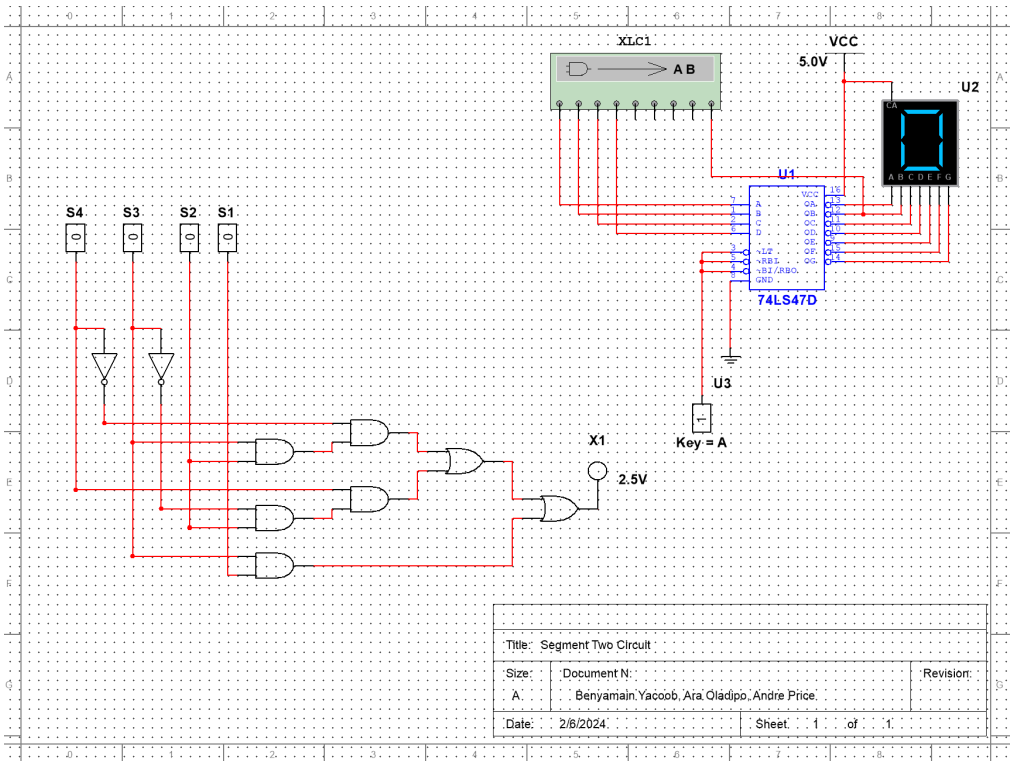

Figure 10: Segment B Logic Converter With Generated Circuit

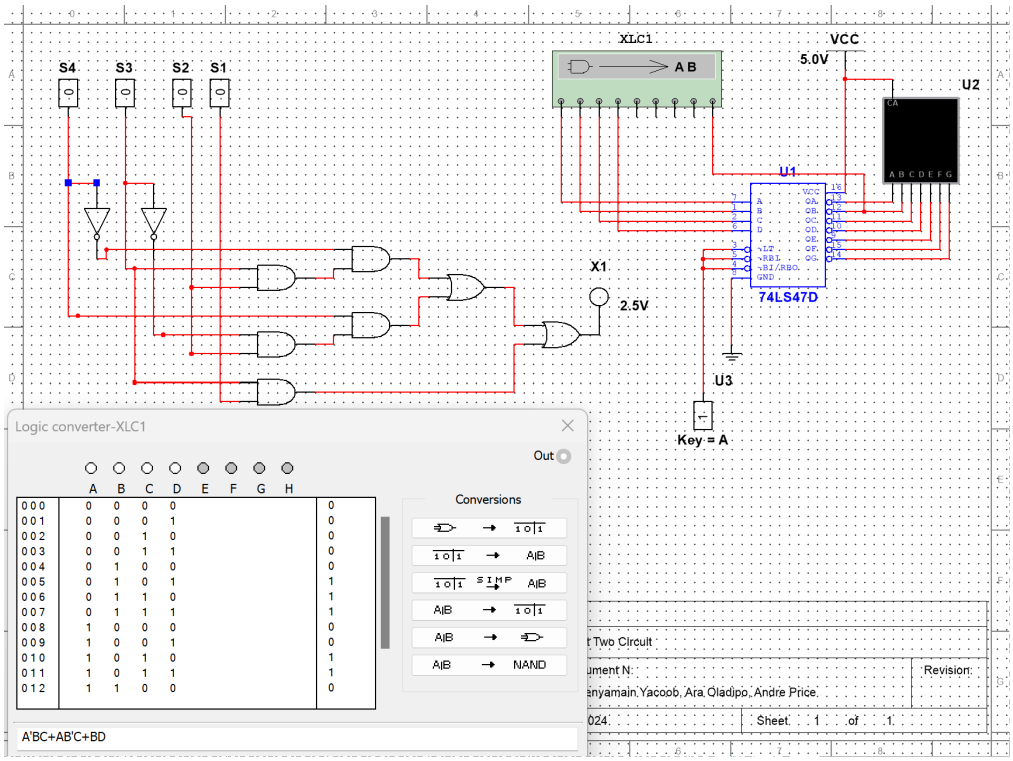

Figure 11: Segment B Circuit Truth Table

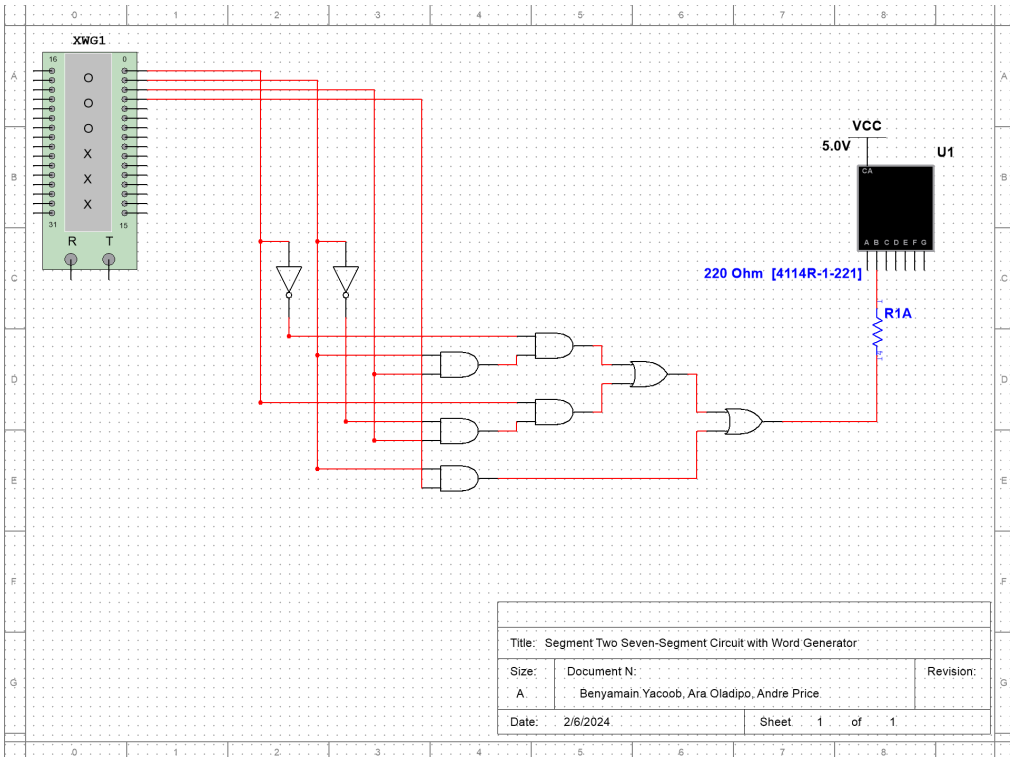

Figure 12: Complete Segment B

$$Y = A'BC + AB'C + BD \tag{2}$$

5.4 Segment C

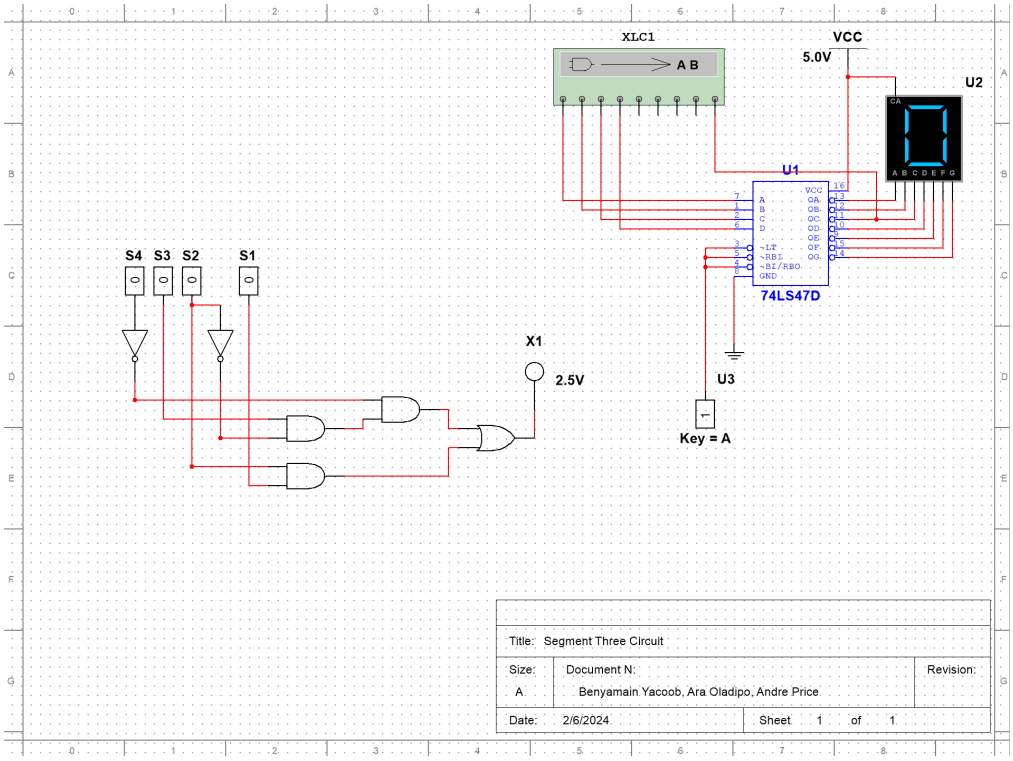

Figure 13: Segment C Logic Converter With Generated Circuit

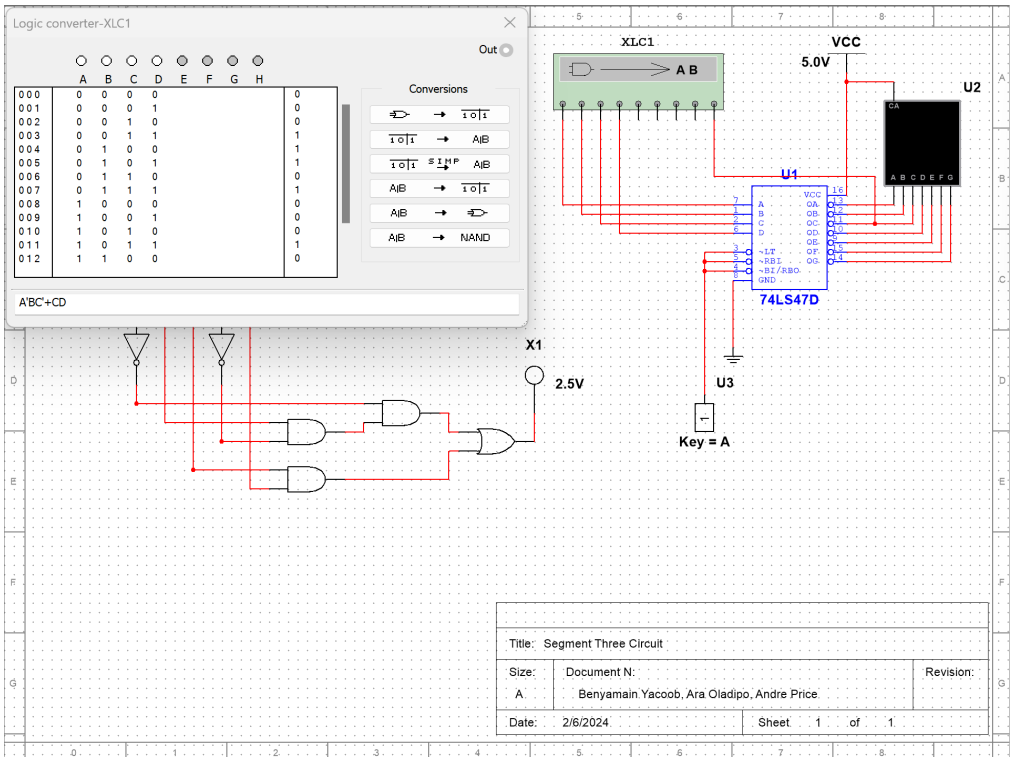

Figure 14: Segment C Circuit Truth Table

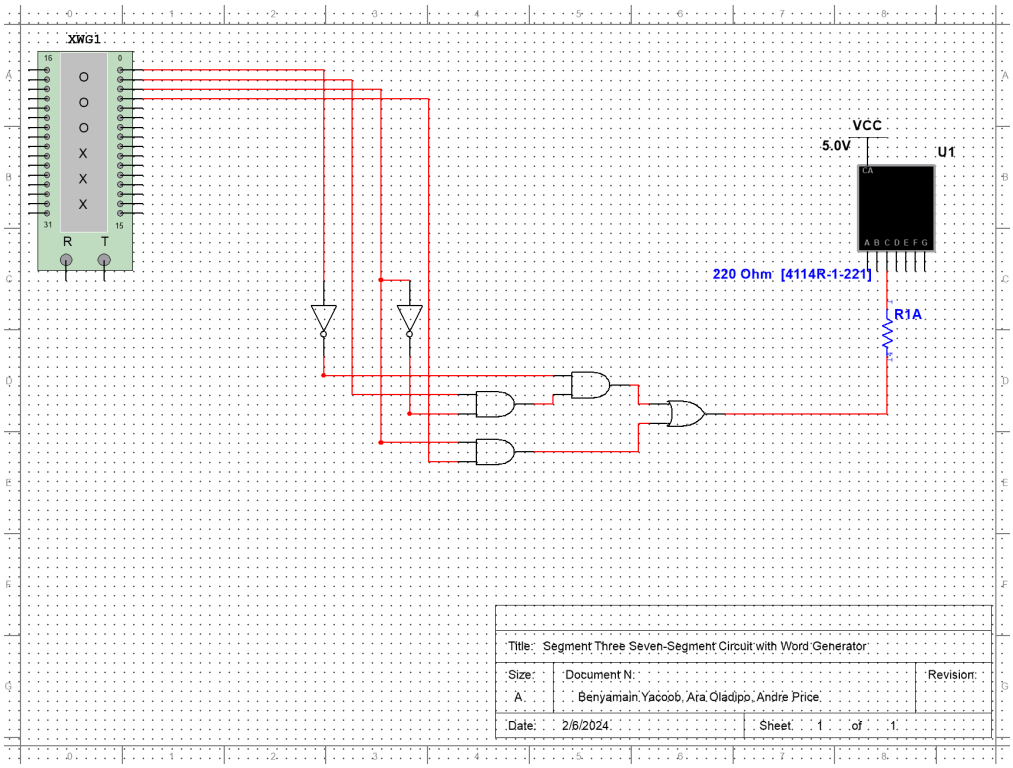

Figure 15: Complete Segment C

$$Y = A'BC' + CD \tag{3}$$

5.5 Segment D

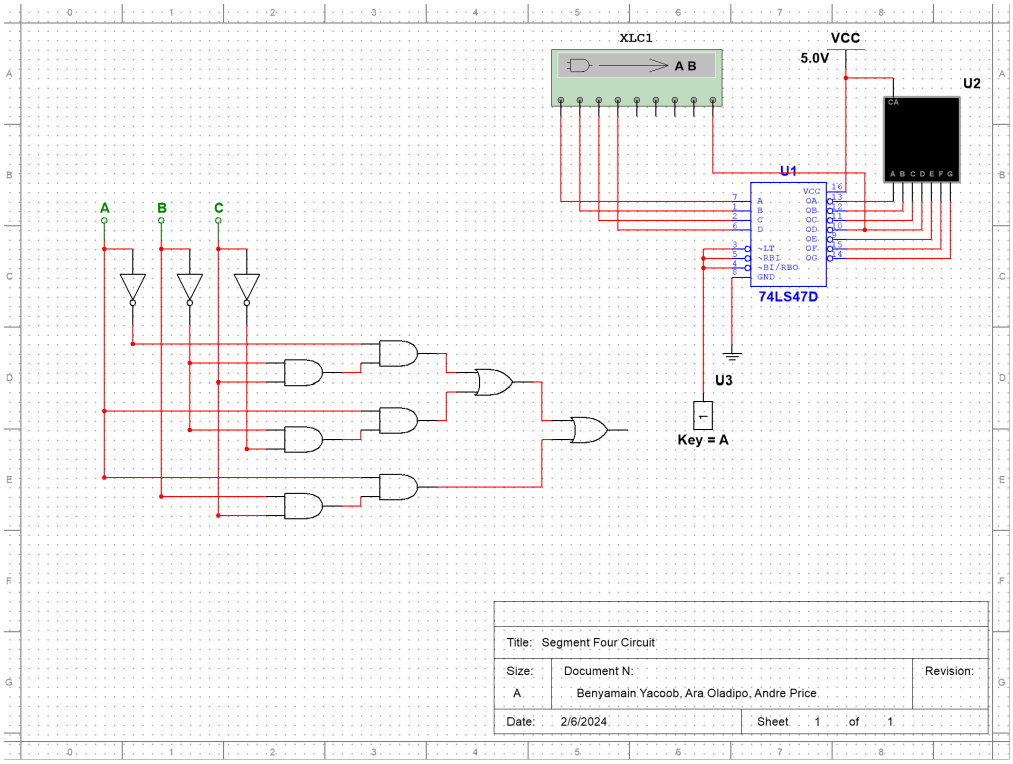

Figure 16: Segment D Logic Converter With Generated Circuit

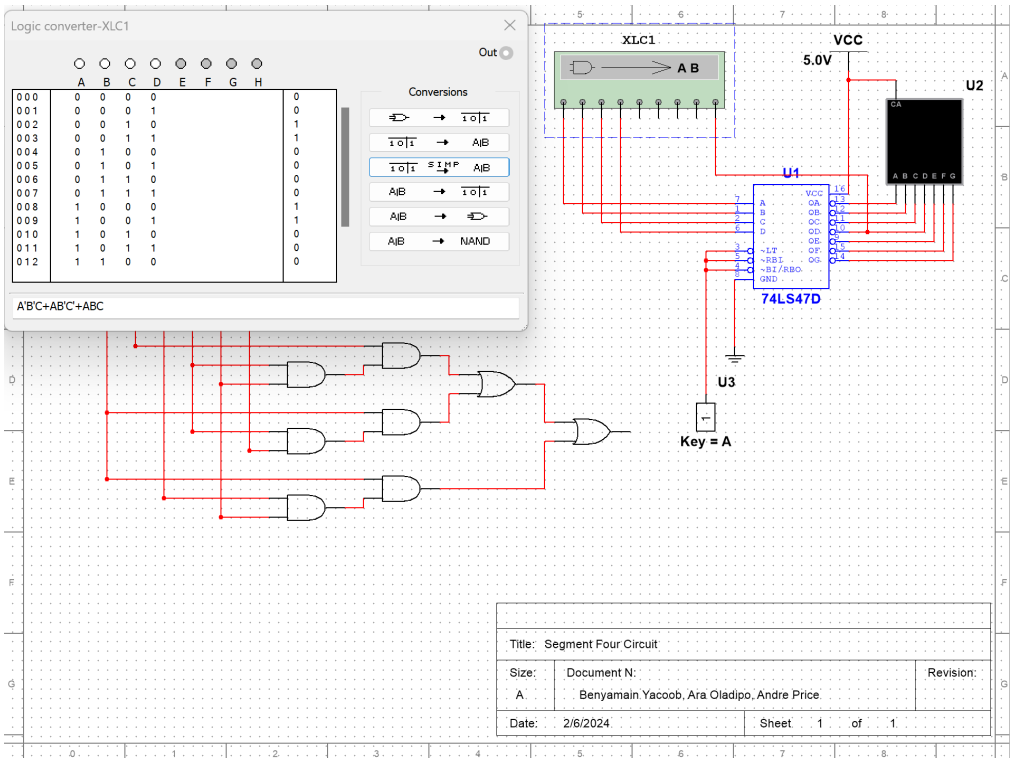

Figure 17: Segment D Circuit Truth Table

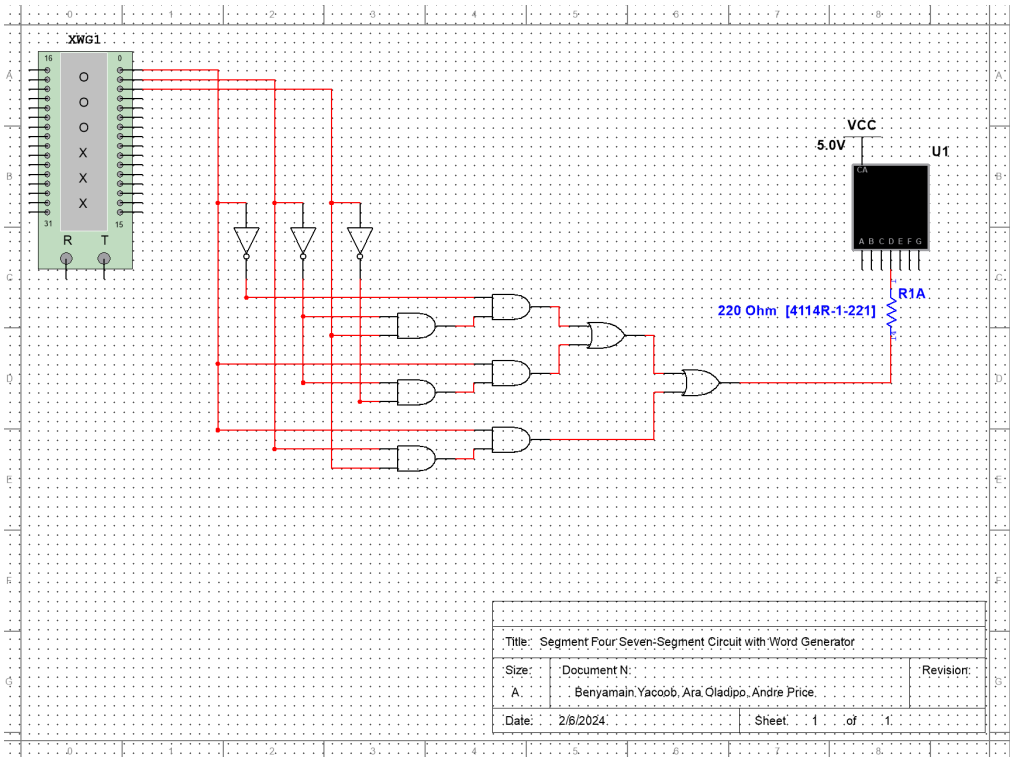

Figure 18: Complete Segment D

$$Y = A'B'C + AB'C' + ABC \tag{4}$$

5.6 Segment E

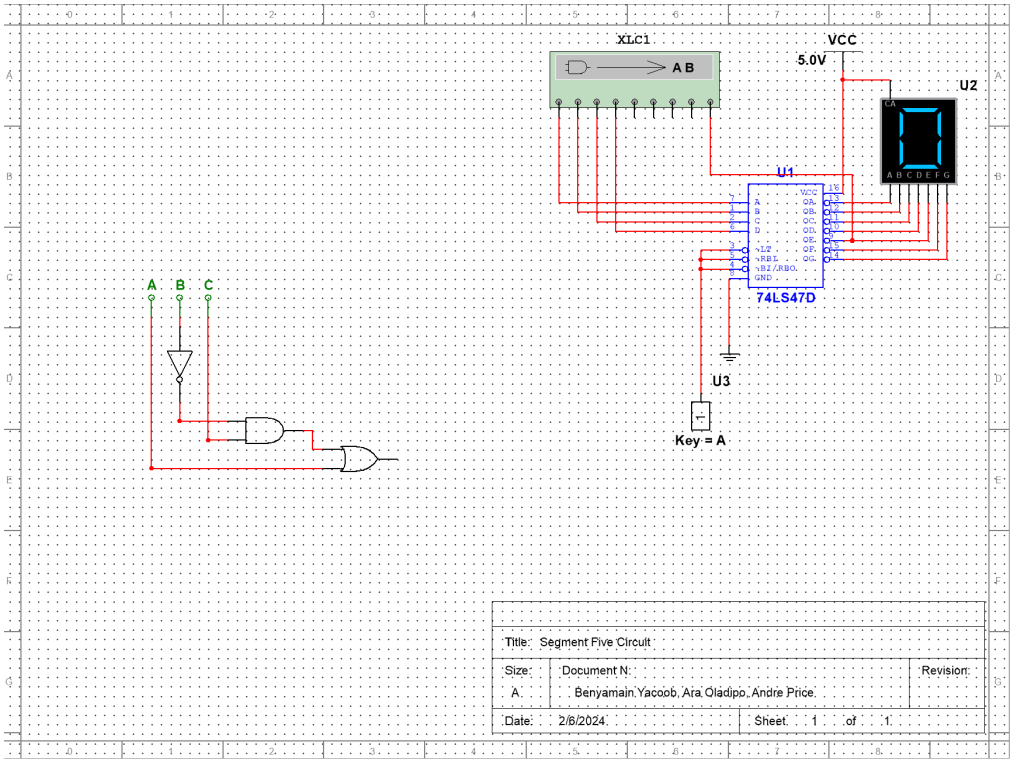

Figure 19: Segment E Logic Converter With Generated Circuit

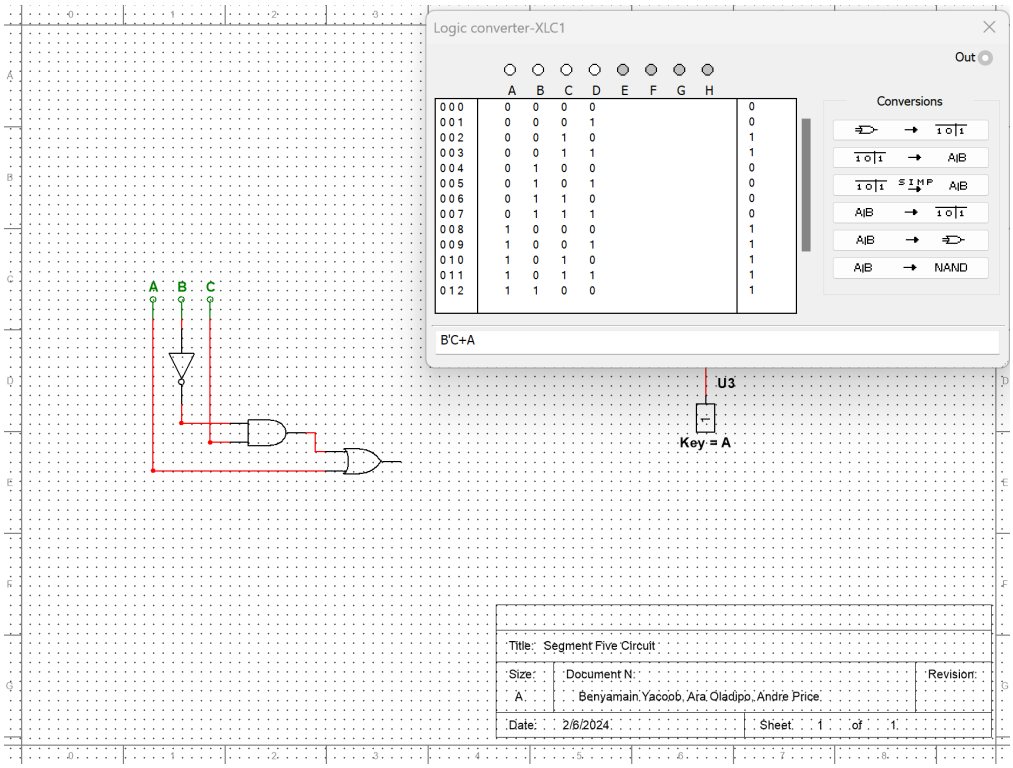

Figure 20: Segment E Circuit Truth Table

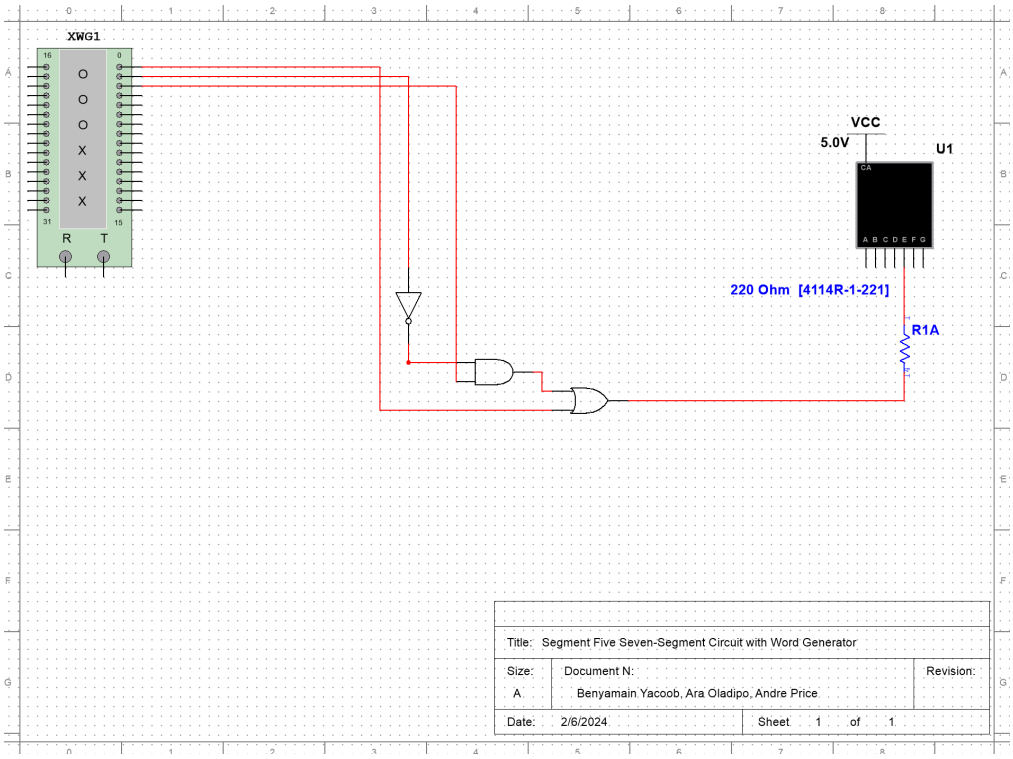

Figure 21: Complete Segment E

$$Y = B'C + A \tag{5}$$

5.7 Segment F

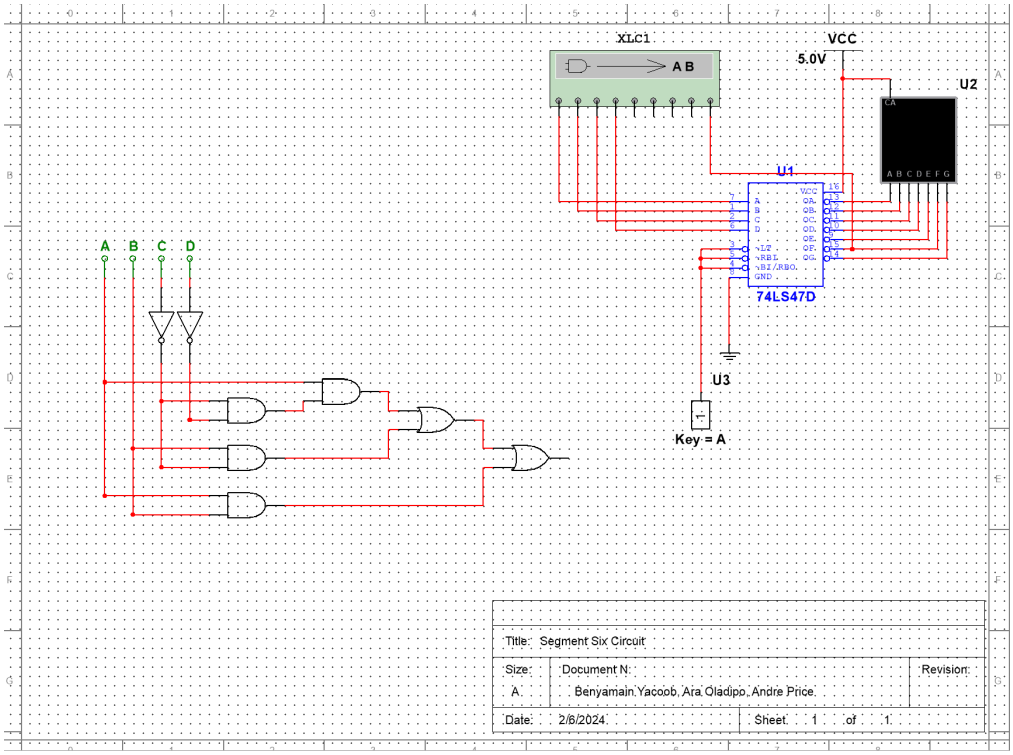

Figure 22: Segment F Logic Converter With Generated Circuit

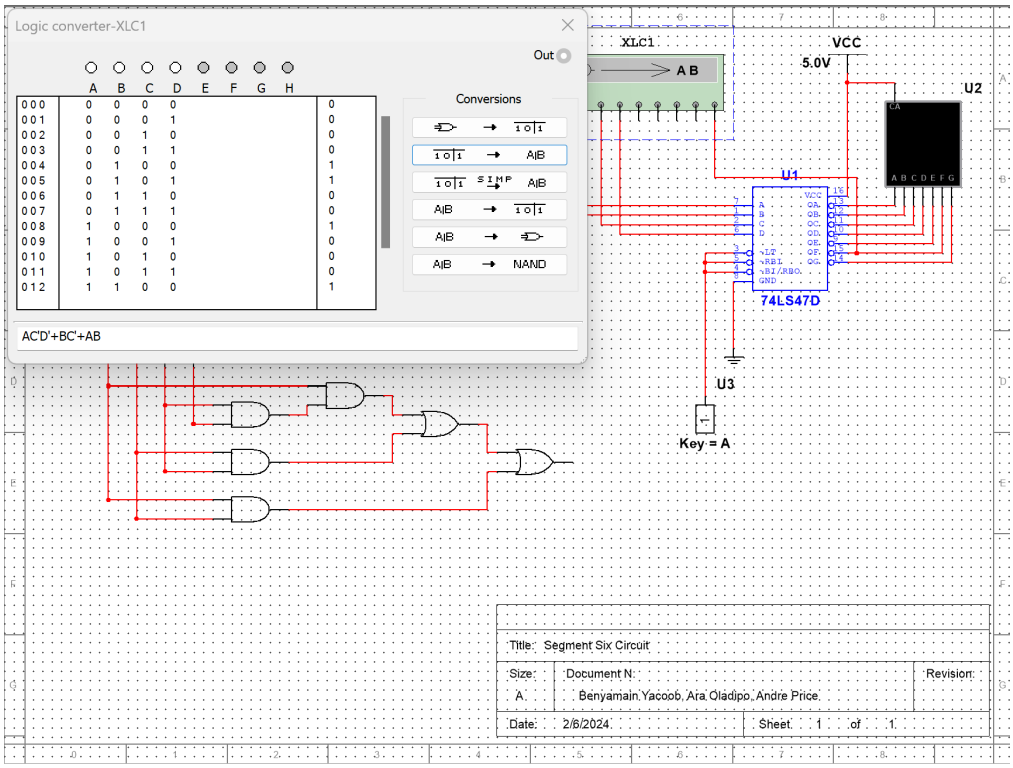

Figure 23: Segment F Circuit Truth Table

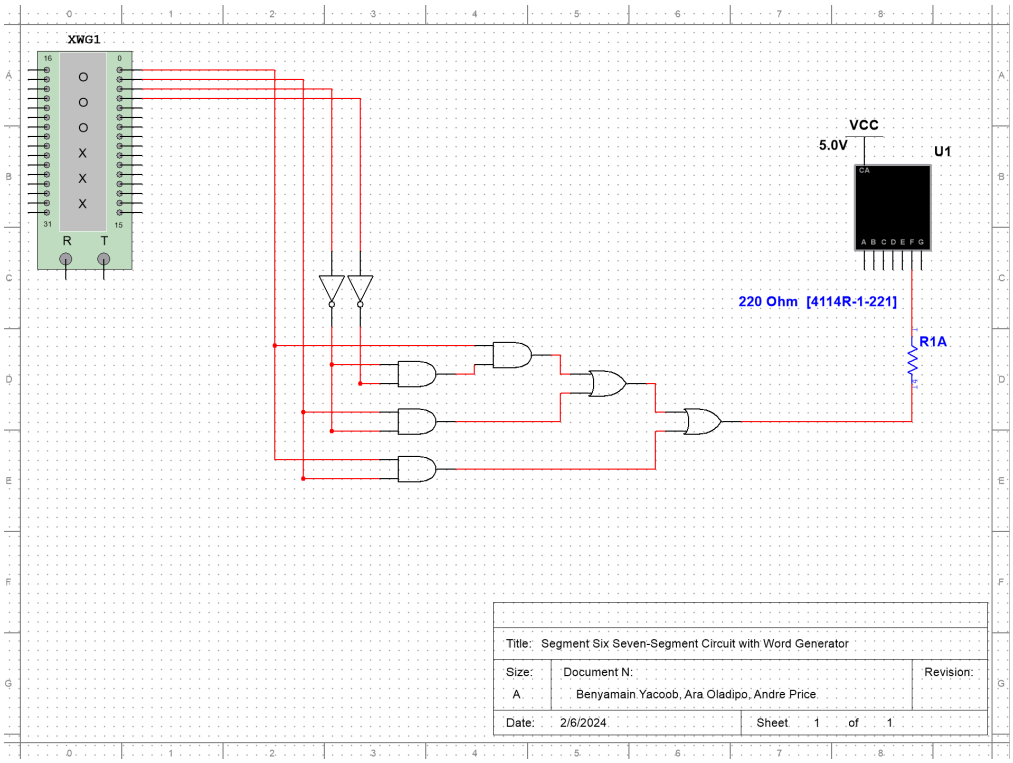

Figure 24: Complete Segment F

$$Y = AC'D' + BC' + AB \tag{6}$$

5.8 Segment G

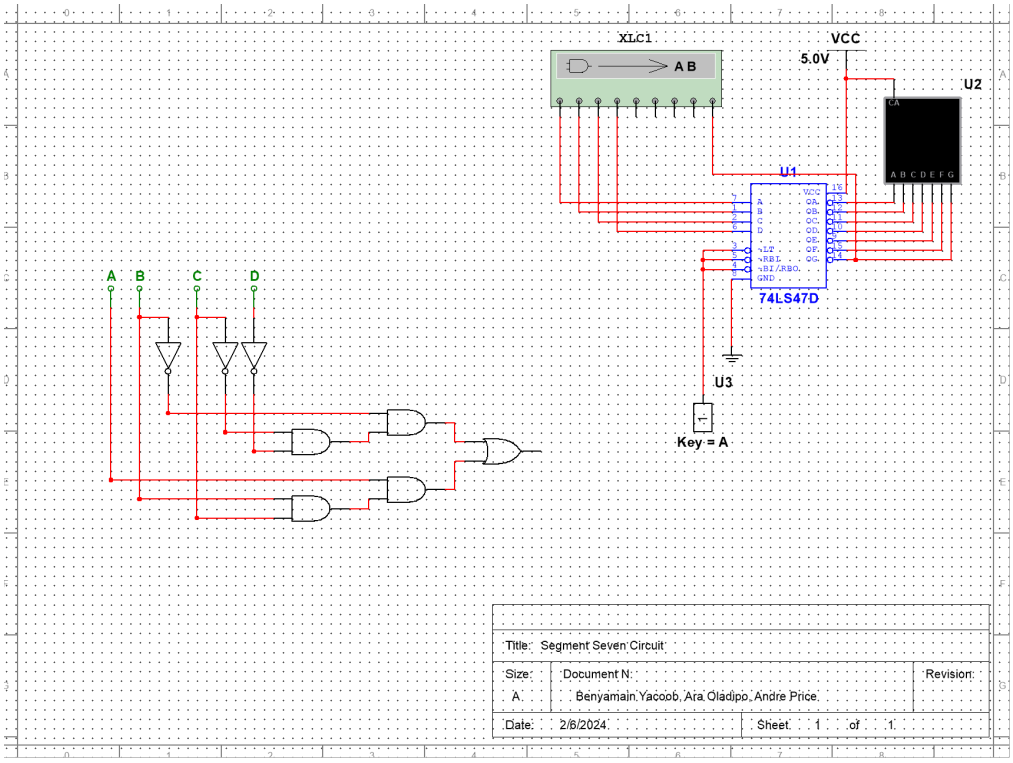

Figure 25: Segment G Logic Converter With Generated Circuit

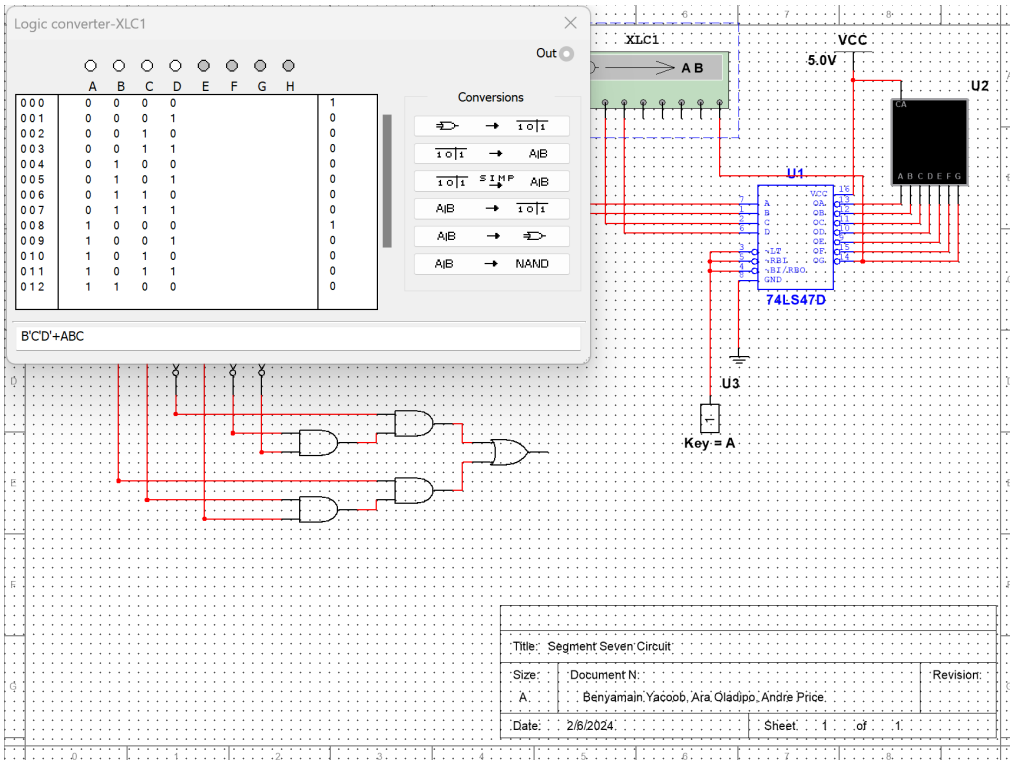

Figure 26: Segment G Circuit Truth Table

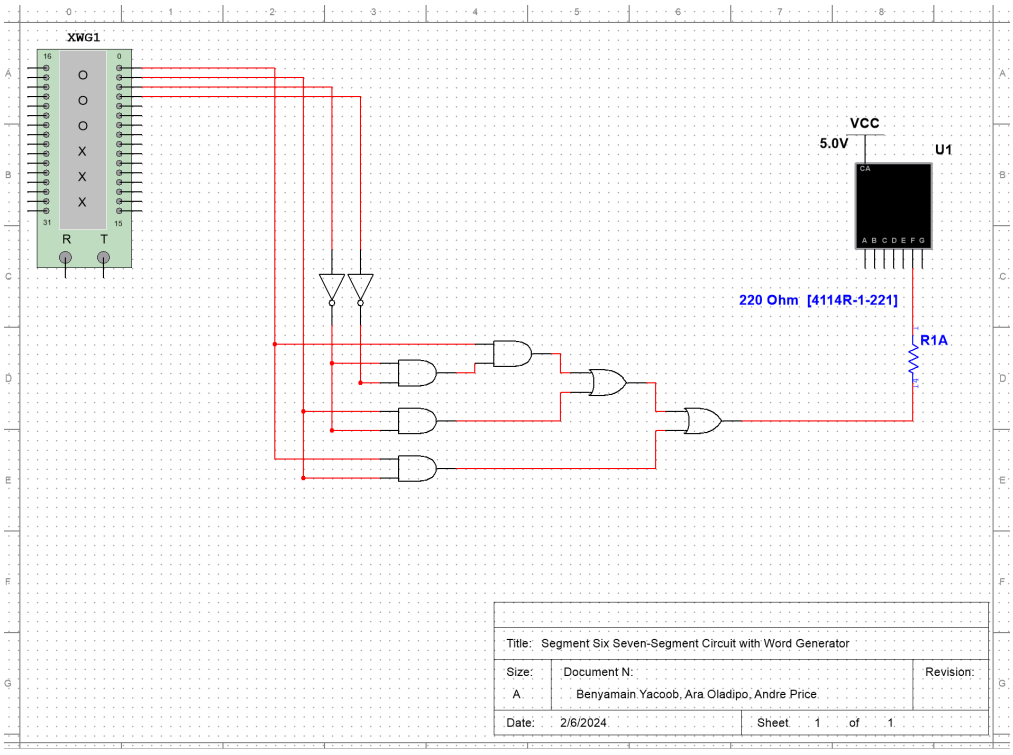

Figure 27: Complete Segment G

$$Y = B'C'D' + ABC \tag{7}$$

5.9 Results and Analysis Discussion

For each of the segments, we were able to verify the accuracy of our circuits with the common anode display and the word generator. We first generated the Boolean equations for each segment (A-G) by connecting the 74LS47 Decoder IC to the Logic Converter. By doing this, we were able to get the simplified boolean equation from each segment. The process of generating a circuit based on these equations was straightforward. We realize that we limited ourselves to 2-input AND gates, rather than sometimes using 3-input or 4-input gates, but the results were ultimately the same. To verify our circuits, we connected them to a common anode display, along with a word generator, to make it easy to see the output as the input changes.

5.10 Complete Circuit Design

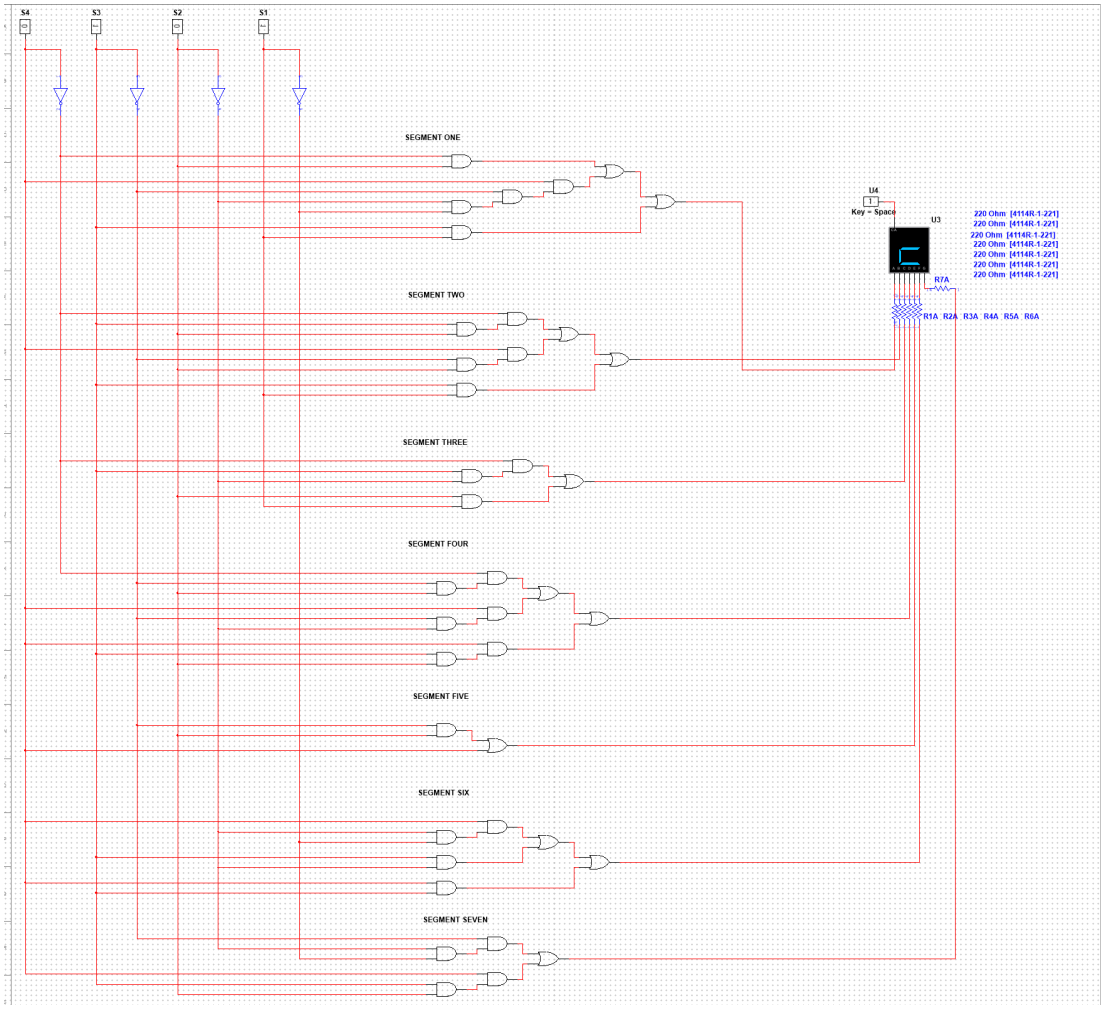

Figure 28: Complete Circuit Design Integrating Seven Segment Circuits

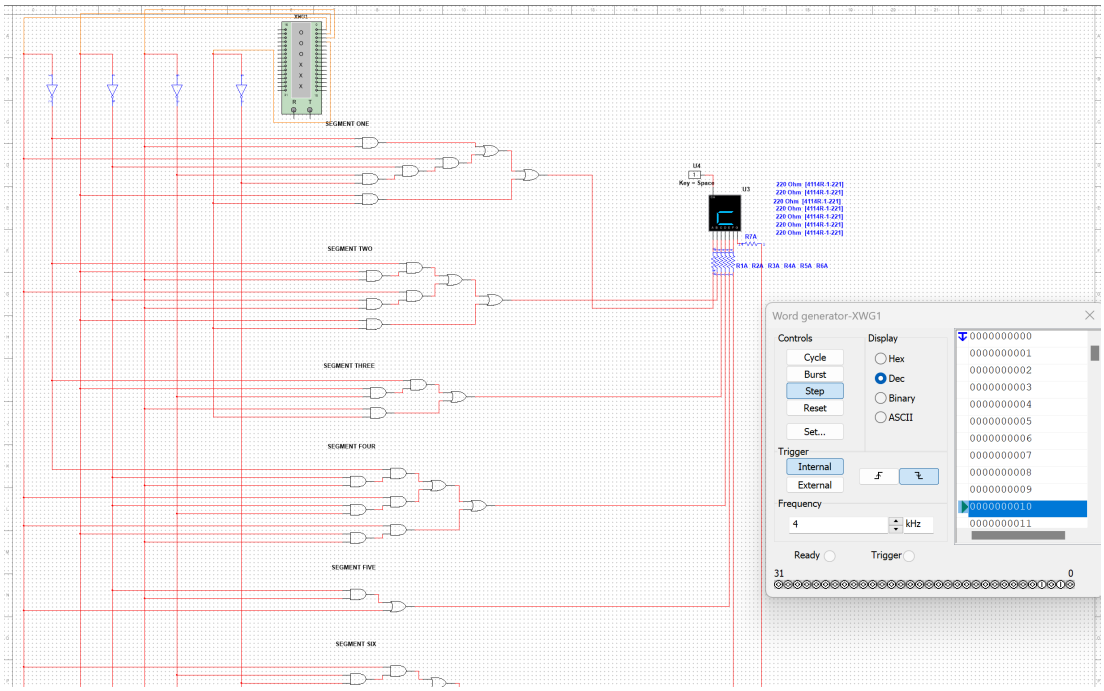

Figure 29: Seven-Segment Decoder With Word Generator

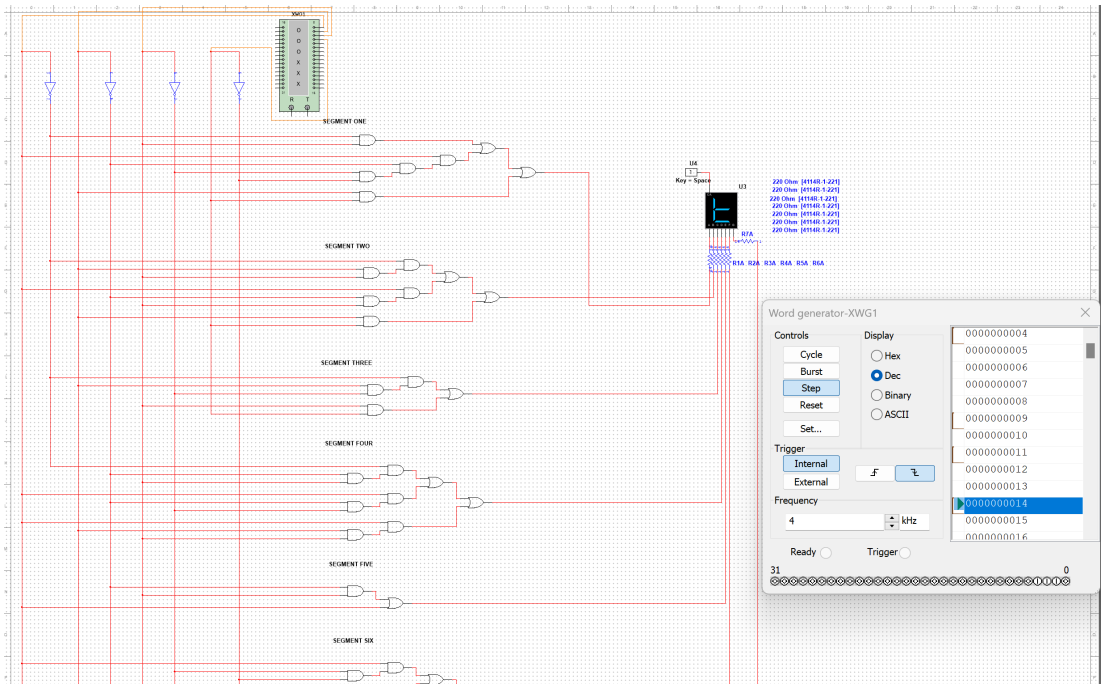

Figure 30: Seven-Segment Decoder With Word Generator

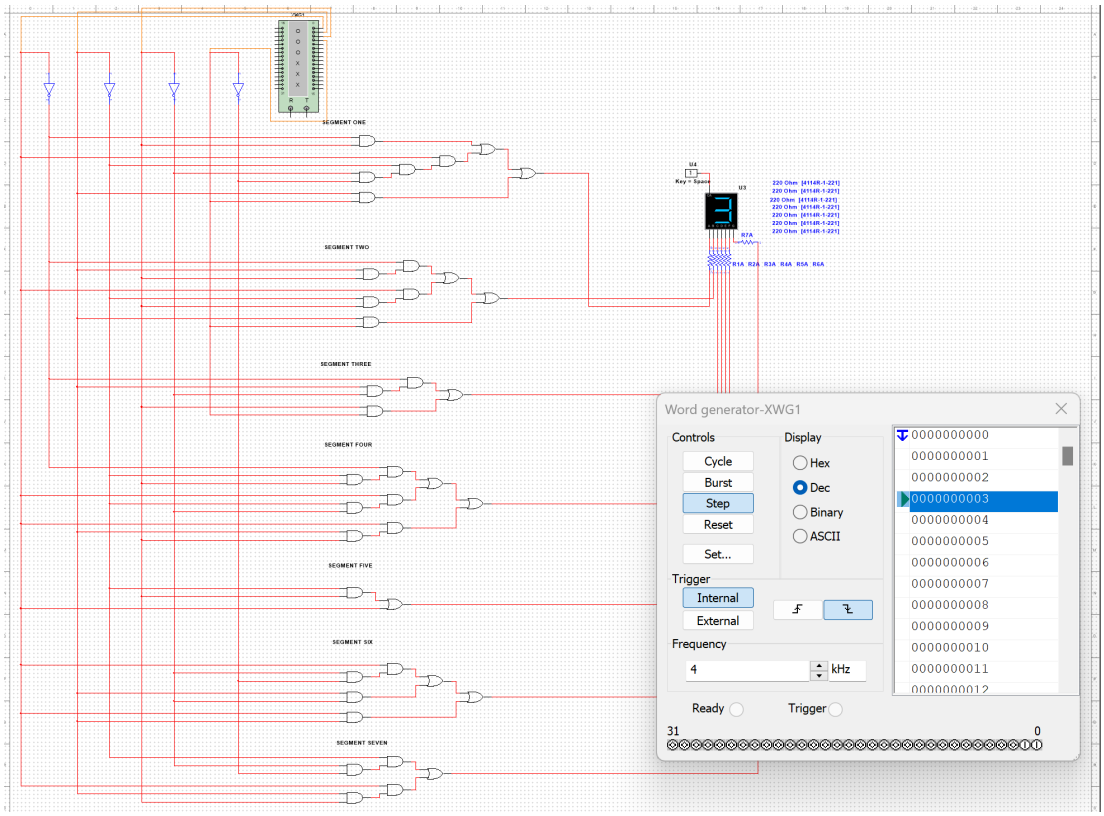

Figure 31: Seven-Segment Decoder With Word Generator

5.10.1 Results and Analysis Discussion

The circuit-building process was slow and tedious, requiring the simultaneous work of our team to reduce the potential for error. We also experienced some difficulties when setting up the word generator. The biggest issue we faced was having to redo the final circuit because we realized that we did not need to connect every segment to a unique input. Ultimately, we were able to gain a comprehensive understanding of the circuit's functionality and purpose. The simple solution was to connect each corresponding A, B, C, etc. input of some circuit to the same wire(s). We added resistors to each segment to prevent an overflow of current on the display!

6 74LS47 Decoder IC

6.1 74LS47 Decoder IC Comparison

S_4	S_3	S_2	S_1	Decimal	a	b	c	d	e	f	g	Correct ✓
0	0	0	0	0	0	0	0	0	0	0	1	✓
0	0	0	1	1	1	0	0	1	1	1	1	✓
0	0	1	0	2	0	0	1	0	0	1	0	✓
0	0	1	1	3	0	0	0	0	1	1	0	✓
0	1	0	0	4	1	0	0	1	1	0	0	✓
0	1	0	1	5	0	1	0	0	1	0	0	✓
0	1	1	0	6	1	1	0	0	0	0	0	✓
0	1	1	1	7	0	0	0	1	1	1	1	✓
1	0	0	0	8	0	0	0	0	0	0	0	✓
1	0	0	1	9	0	0	0	1	1	0	0	✓
1	0	1	0	A	1	1	1	0	0	1	0	✓
1	0	1	1	B	1	1	0	0	1	1	0	✓
1	1	0	0	C	1	0	1	1	1	0	0	✓
1	1	0	1	D	0	1	1	0	1	1	0	✓
1	1	1	0	E	1	1	1	0	0	0	0	✓
1	1	1	1	F	1	1	1	1	1	1	1	✓

Figure 32: Seven-Segment Decoder Truth Table

6.1.1 Results and Analysis Discussion

After using the common anode display and testing all the combinations to verify the accuracy of our circuits, we were able to verify that our truth table from the beginning was correct. This verification process allowed us to fully exercise our circuit by comparing each segment output for each input combination.

6.2 74LS47 Decoder IC, 4-Bit Adder, and Display Integration

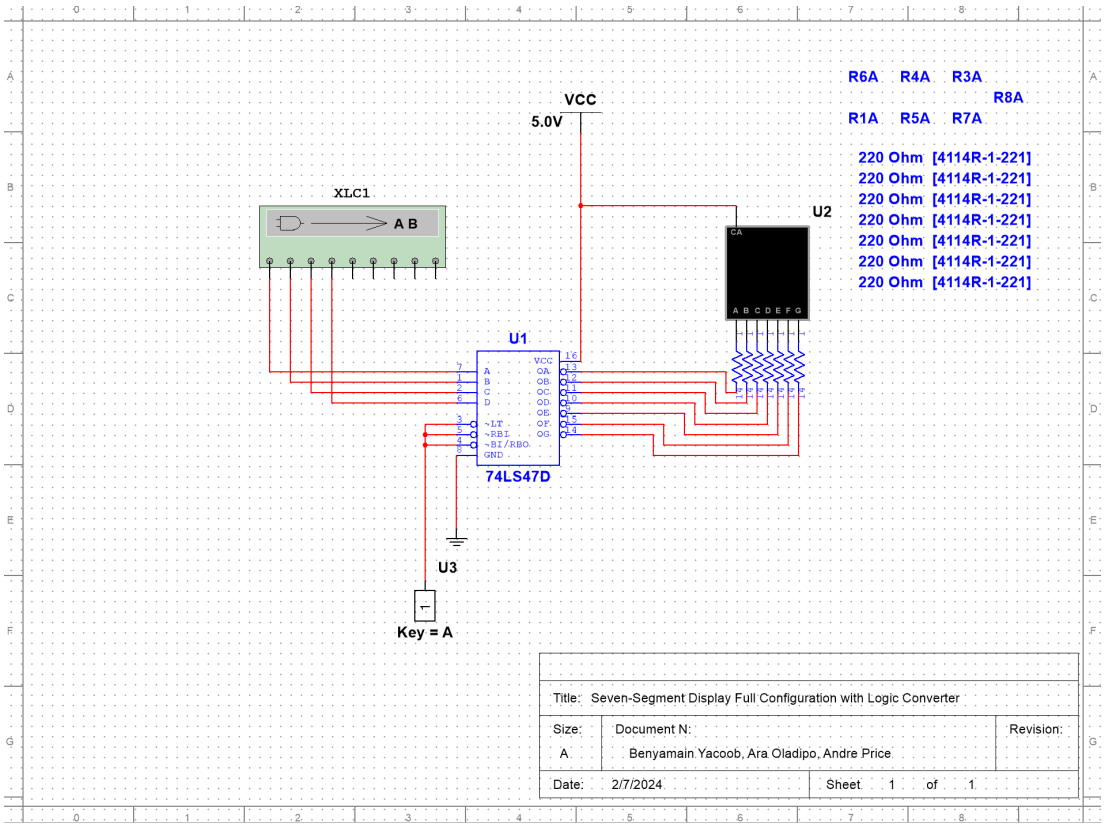

Figure 33: Seven-Segment Decoder Truth Table

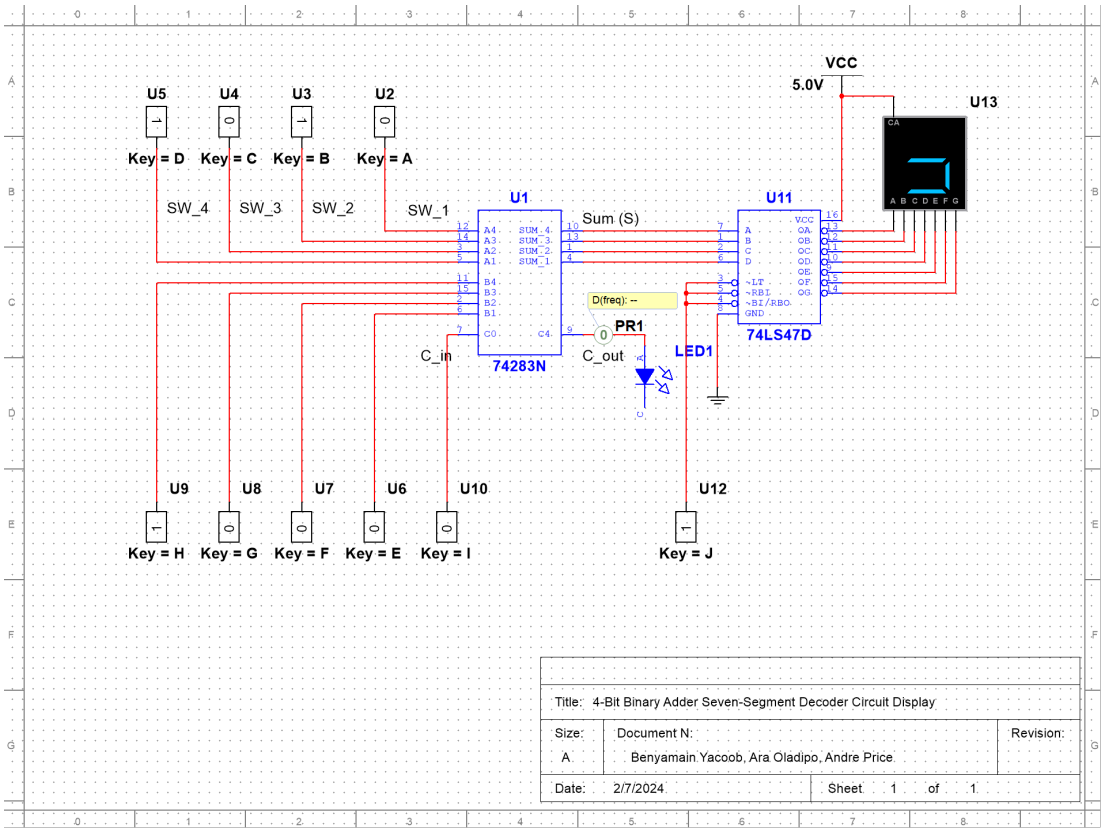

Figure 34: Seven-Segment Decoder Truth Table

6.3 74LS47 Decoder IC, 4-Bit Adder, and Word Generator

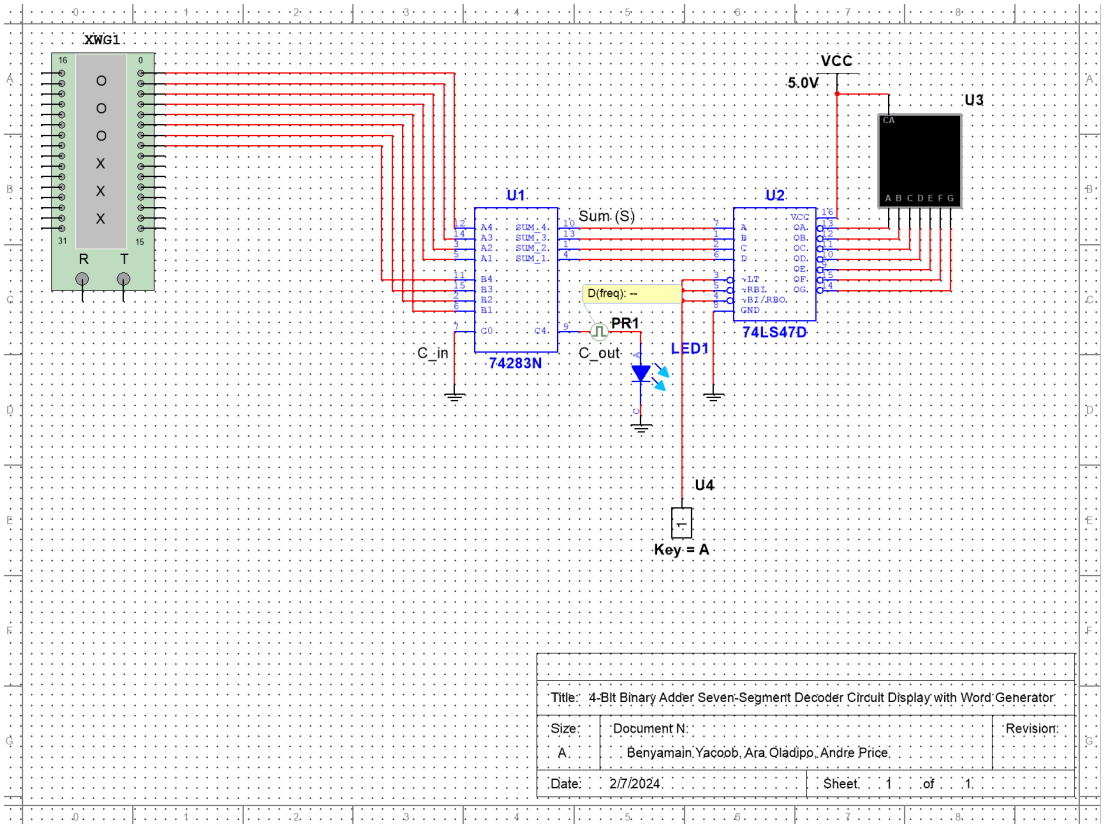

Figure 35: Seven-Segment Decoder IC With 4-Bit Adder and Word Generator

INPUTS									EXPECTED OUT		ACTUAL OUT		Check if Correct
A_4	A_3	A_2	A_1		B_4	B_3	B_2	B_1	C_{out}	S_{out}	C_{out}	S_{out}	✓
0	1	0	1		0	1	0	1	0	A	0	A	✓
0	1	1	1		0	1	0	1	0	C	0	C	✓
1	0	0	1		0	1	0	1	0	E	0	E	✓
1	0	1	1		0	1	0	1	1	0	1	0	✓

Figure 36: Truth Table for 4-bit Adder: HEX Outputs

6.4 Results and Analysis Discussion

We were under the impression that the assignment required us to integrate the 4-bit binary subtractor on top of the 74LS47 Decoder IC and the seven-segment HEX display. However, after getting clarification from the teacher assistants, as well as direct confirmation from the professor, we did not change our integration of the decoder with the display and as shown in the figure, a 4-bit binary adder was integrated. Connecting the inputs from the word generator to the 74283N and grounding the carry was not difficult to implement in the circuitry, but the inner workings of the decoder required us to refer to the Internet for documentation on those last three connectors at the bottom left of the component. We were experimenting with a switch on top of the interactive digital constant when referring to making those three connectors work because the seven-segment display was not outputting anything. By connecting the three connectors to the same wire, our problem was resolved.

7 Results and Conclusion

This section discusses the results of the digital logic gate simulation experiments. The discussion provides in-depth explanations of the results and any discrepancies between the results and theoretical expectations. It also explores potential sources of error and discusses the accuracy of the tests, the debugging process, and what was learned from these experiences.

This being our third simulation assignment, we as a group have successfully managed to comprehend the basic foundation of what it means to utilize many of the different capabilities with MultiSIM; however, this being our third simulation assignment also means that it is accompanied by newer forms of complexities not seen in any of the previous simulation assignments. This form takes shape as it pertains to the BCD to Seven-Segment Display and corresponding Decoder IC. One of the major difficulties was understanding how to display them correctly. We tried to map the inputs to the corresponding segments of the displays in a way that minimizes the overall complexity of the diagrams while ensuring that the work we were turning in was complete and accurate. Although it took a while for us to complete this respective section of the assignment, hard work and office hours played a large part in getting our questions answered and finishing up the assignment.

Another problem experienced from this simulation assignment came from the assignment itself. When comparing the sizes of the circuits from assignment to assignment, it can be observed that the circuits are ever-growing in both size and depth. This makes it harder to account for the increasing amount of components As a group, we wanted to ensure that we were creating well-made schematics while also following the requirements of the assignment; but, it must be mentioned that finding that balance was a challenge that was experienced throughout this process and will likely continue across the assignments after this one as the circuits continue to grow in number and intricacy; consequently, the sophistication of the assignments will grow our skill with MultiSIM and allow us to take of further advantage of the

different tools at our disposal.

One last problem came from our own understanding of the assignment. As observed in previous simulation assignments and noted in this one, our misreading of the instructions led to a negation of the intended outcome. Multiple times throughout this simulation assignment, we concluded that our interpretation of the instructions surrounding many of the circuits was correct until we tried making the circuits and struggled with understanding the logic. Misreading effectively obstructed our flow with the assignment, and we had to take multiple steps back and think before being able to finish each individual circuit.

Overall, this simulation assignment was challenging and rewarding but allowed us the opportunity to grasp new concepts and ideas not previously introduced beyond a theoretical point of view.

8 Group Contributions

The work for this simulation assignment was spread among three individuals, with Benyamain Yacoob covering 75% of the circuit design and labeling. Ara Oladipo finished the remaining portion of the circuits. He and Andre Price composed most of the report, gathering screenshots, wrote the discussions and analysis, and Benyamain proofread the report before submitting it. Any questions that arose during any part of this report process were answered through team collaboration and research.