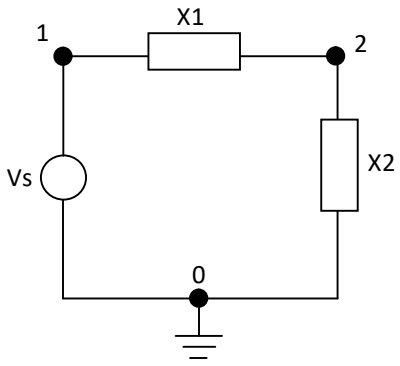
EE735_2023_Assignment8_Solution [Total Marks: 12]

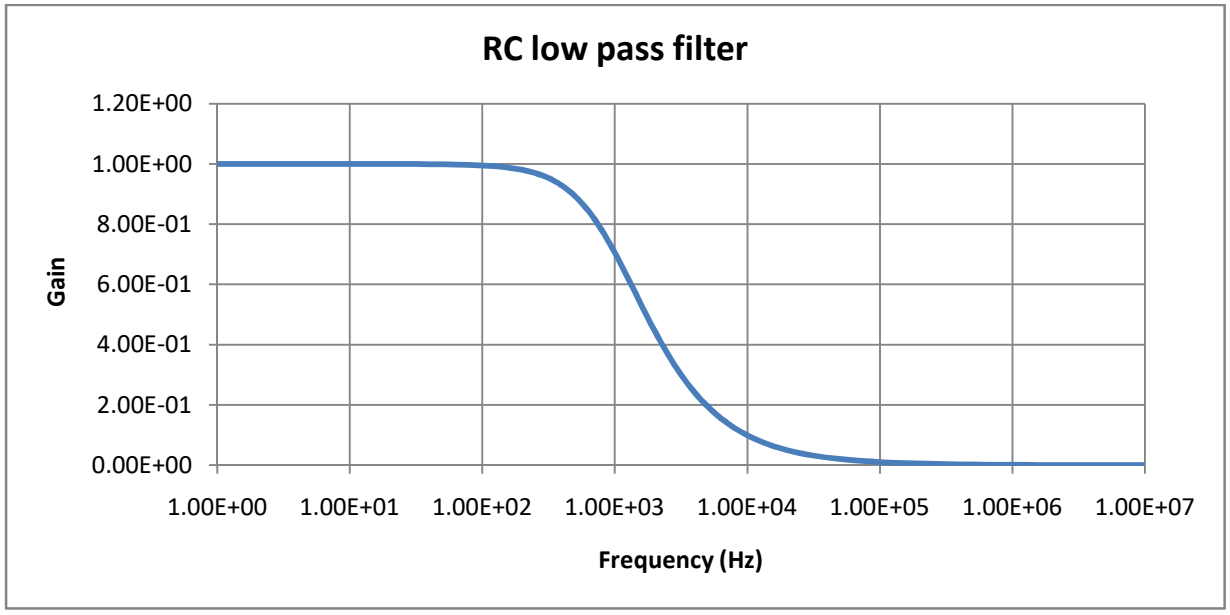
Q1.

3 marks (1 mark for circuit diagram; 1 mark for R and C values; 1 mark for the graph showing frequency response).

The circuit for RC low pass filter is shown below. X1 is the model for resistor whereas X2 is that for capacitor. Vs is the voltage source.



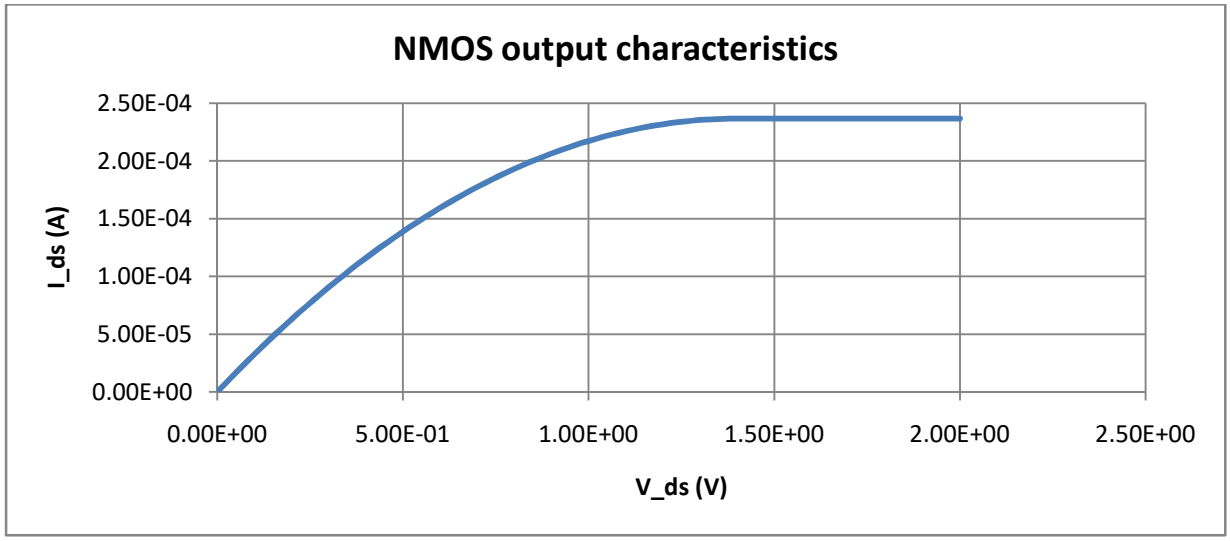
The gain vs frequency curve is given below. R=1600 ohms, C=1e-7 F have been used for 3db bandwidth of ~ 1 KHz.



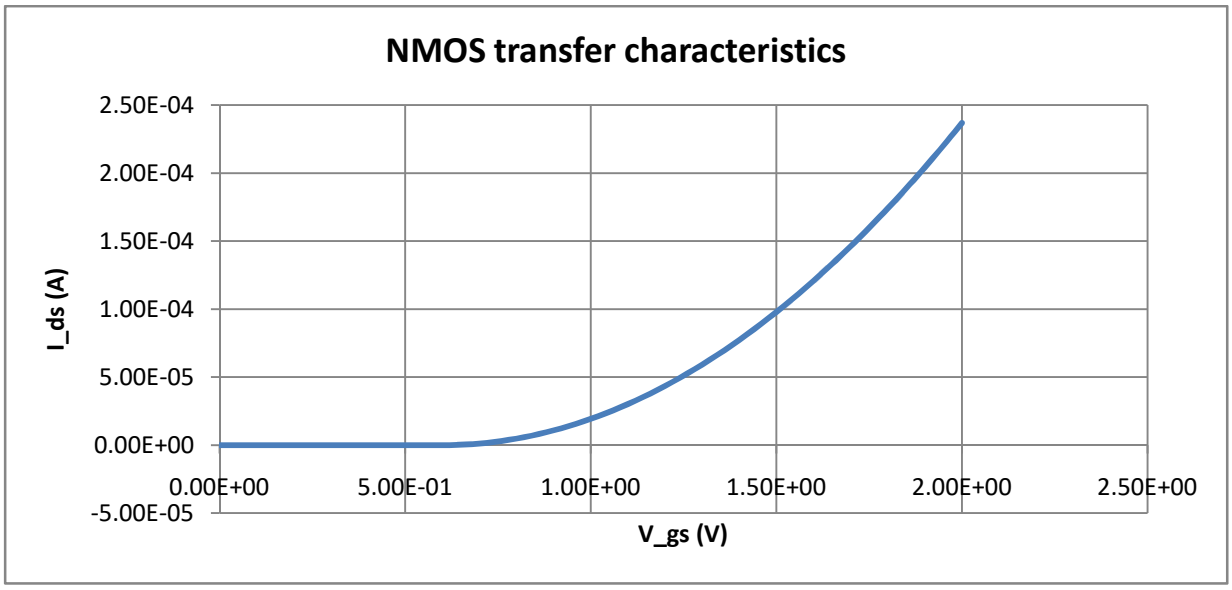
Q2 (a).

3 marks (1 mark for Verilog-A implementation of current equations in linear and saturation regions; 1 mark for I_ds vs V_ds graph; 1 mark for I_ds vs V_gs graph).

It is given that Vth=0.6V for the NMOS. The output characteristic has been asked to plot at Vgs=2V. The transistor enters into saturation mode at Vds > (Vgs-Vth=1.4V). Before that it operates in the linear region.



The transfer characteristic has been asked to plot at Vds=2V. The NMOS transistor switches ON for Vgs > Vth i.e. Vgs > 0.6 V. It remains in the saturation region because Vgs-Vth < Vds for the given bias range.



Q2 (b).

1 mark for the voltage transfer characteristic.

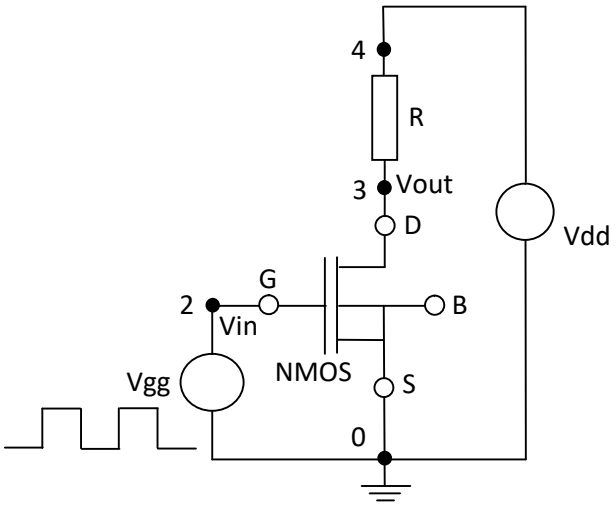
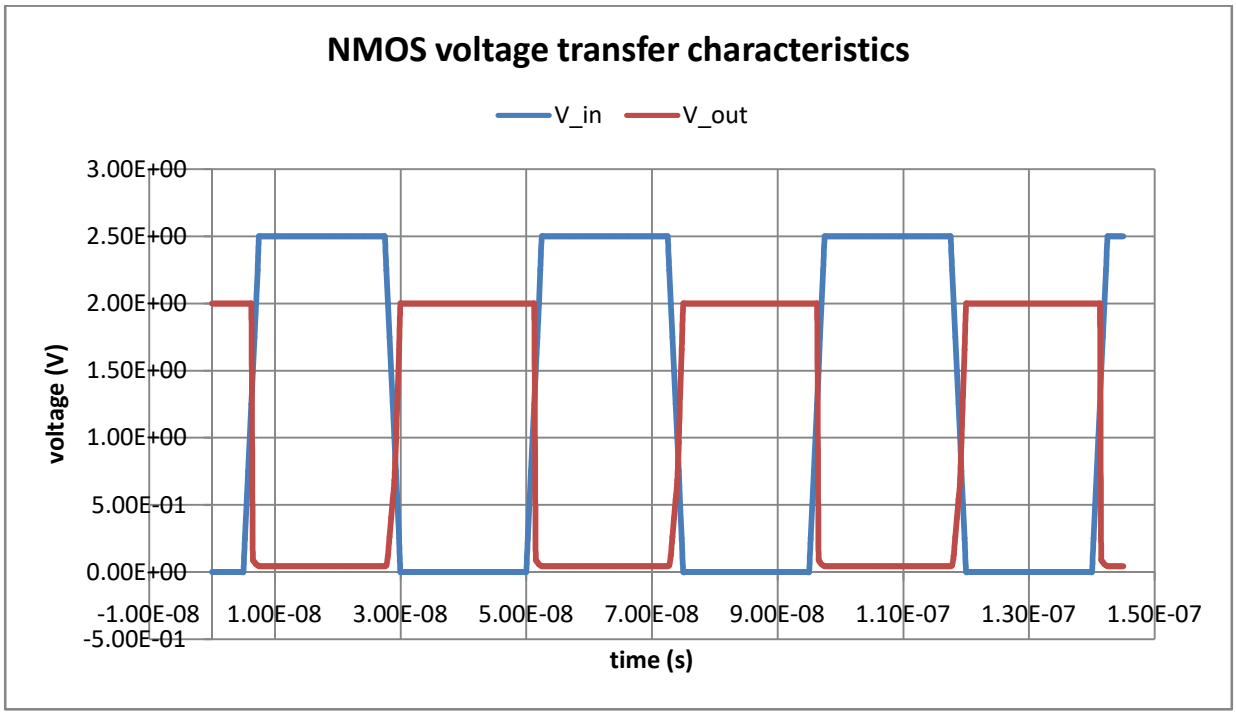


Figure: NMOS Inverter

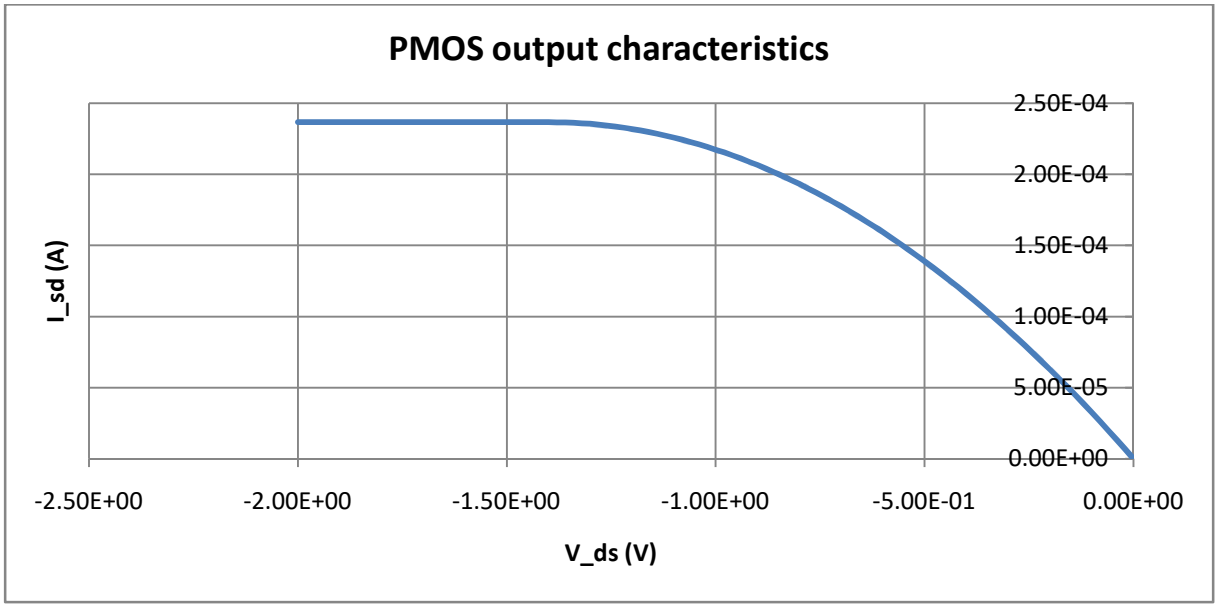
The voltage transfer characteristic (VTC) of NMOS inverter shows input voltage at the gate terminal switching between 0 to Vgg (Vgg is 2.5 V) and the output voltage at the drain terminal switching between (Vdd-Ids*R) to Vdd (Vdd is 2 V).



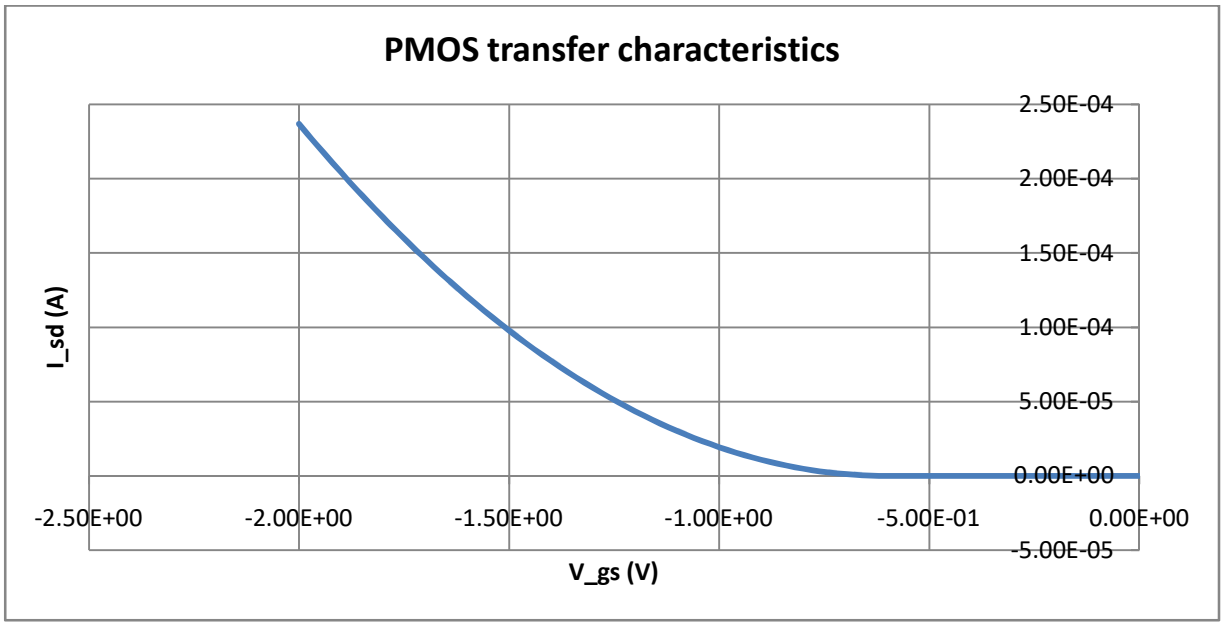
Q3.

3 marks (1 mark for Verilog-A implementation of current equations in linear and saturation regions; 1 mark for I_sd vs V_ds graph; 1 mark for I_sd vs V_gs graph).

For the PMOS, Vth=-0.6V. The output characteristic is plotted at Vgs=-2V. The transistor remains in the linear mode for Vds >= (Vgs-Vth) i.e. Vds >= -1.4V, and enters into saturation mode when Vds falls below -1.4V.



The transfer characteristic is plotted at Vds=-2V. The transistor becomes ON when Vgs < Vth i.e Vgs < -0.6V. For the given bias range, Vds remains below Vgs-Vth so that the transistor always operates in the saturation region.



Q4.

2 marks (1 mark for circuit implementation in Hspice; 1 mark for voltage transfer characteristic)

The voltage at the input (gate) and output (drain) terminals switches between 0 and 2 V, and are out of phase confirming the inverter operation of CMOS (see the VTC curve below). The C_load is small enough (smaller RC delay) to charge to Vdd and discharge to 0V within the given time frames.

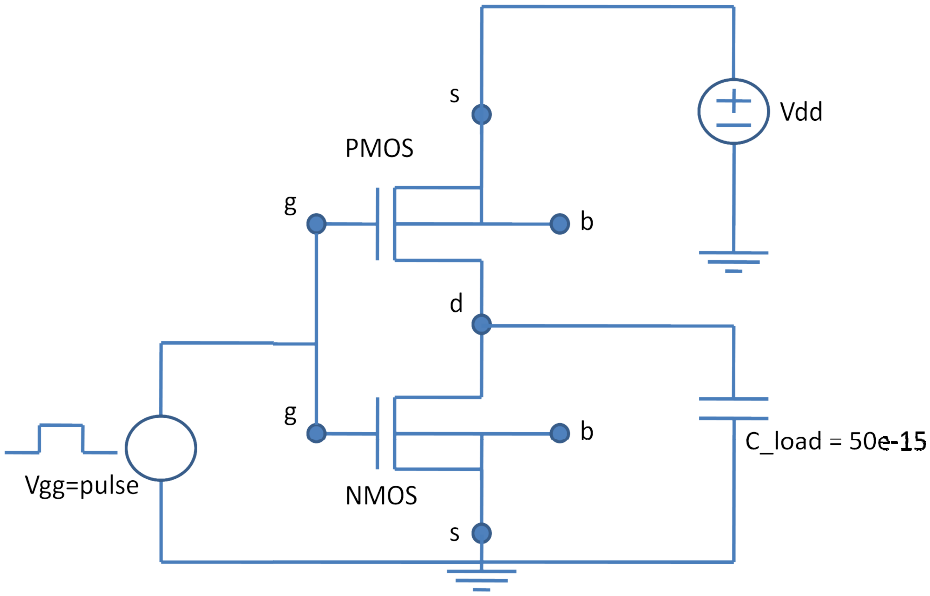


Fig. A: CMOS Inverter circuit