EE 735 Assignment 8

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Q1. Use your customized models for resistor and capacitor to design RC-Low Pass Filter with 3-dB Bandwidth of 1KHz. Perform AC analysis to verify the result. Overwrite appropriate values in place of default values for Resistor and Capacitor. Draw the circuit showing Vs, X1, X2, and node labels.

Verilog-A Model for a Simple Resistor-

```
`include "disciplines.vams"
module simple_resistor(p,n) ;
inout p,n;
parameter real resistance = 1000.0 from (0.0:inf) ;
electrical p, n ;
analog
begin
I(p,n) <+ V(p,n)/resistance ;
end
endmodule
```

H-spice file for a Simple Resistor

```
* Basic Resistor
*********************************
* Include Files (* means comment)
*********************************
```

```
.OPTION POST=2 INGOLD=2 $ (text after $ is comment)
.hdl “Resistor.va“ $ calling the verilog-a file
.model res simple_resistor $ creating a model instance
*******************************
* Netlist
*******************************
X1 1 0 res resistance=100 $ instantiating the instance as sub-circuit
Vs 1 0 DC 0.8
*******************************
.dc Vs 0 4 0.2
.print V(1)
.print I(Vs)
.end
```

Verilog-A model of a Capacitor

```
`include "disciplines.vams"
module simple_capacitor(p,n);
inout p,n;
electrical p,n;
parameter real C=1e-6 from [0.0:inf); //default value
real q;
analog begin
q=C*V(p,n);
I(p,n)<+ ddt(q);
end
```

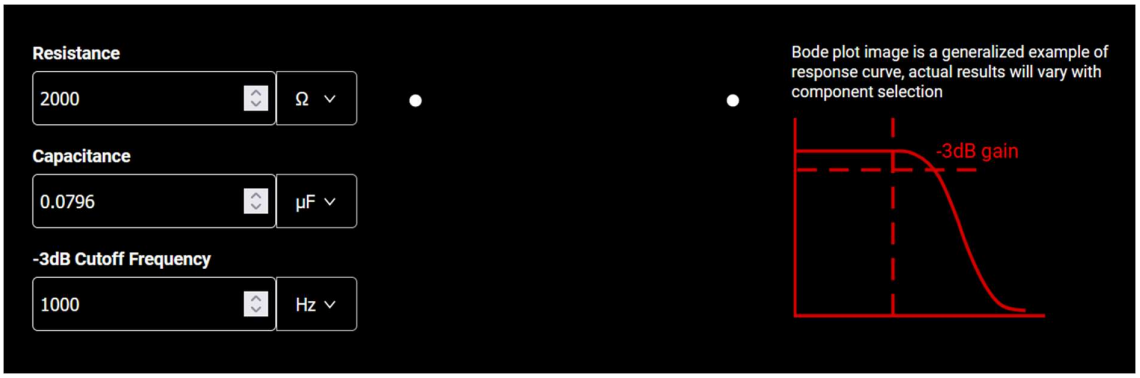
endmodule

H-spice file for a RC

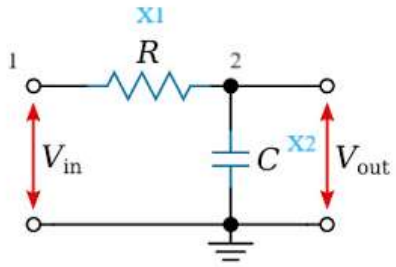
```
*RC-Check
********Include Files*******
.OPTION POST=2
.hdl “Resistor.va"
.hdl “Capacitor.va"
.model cap simple_capacitor
.model res simple_resistor
******* Netlist ************

X1 1 2 res resistance=2000
X2 2 0 cap C= 0.0796e-6
Vs 1 0 AC 1V
*************************
.AC DEC 10 1 1MEG
.print V(2) V(1)
.end
```

RC Low-Pass Filter:

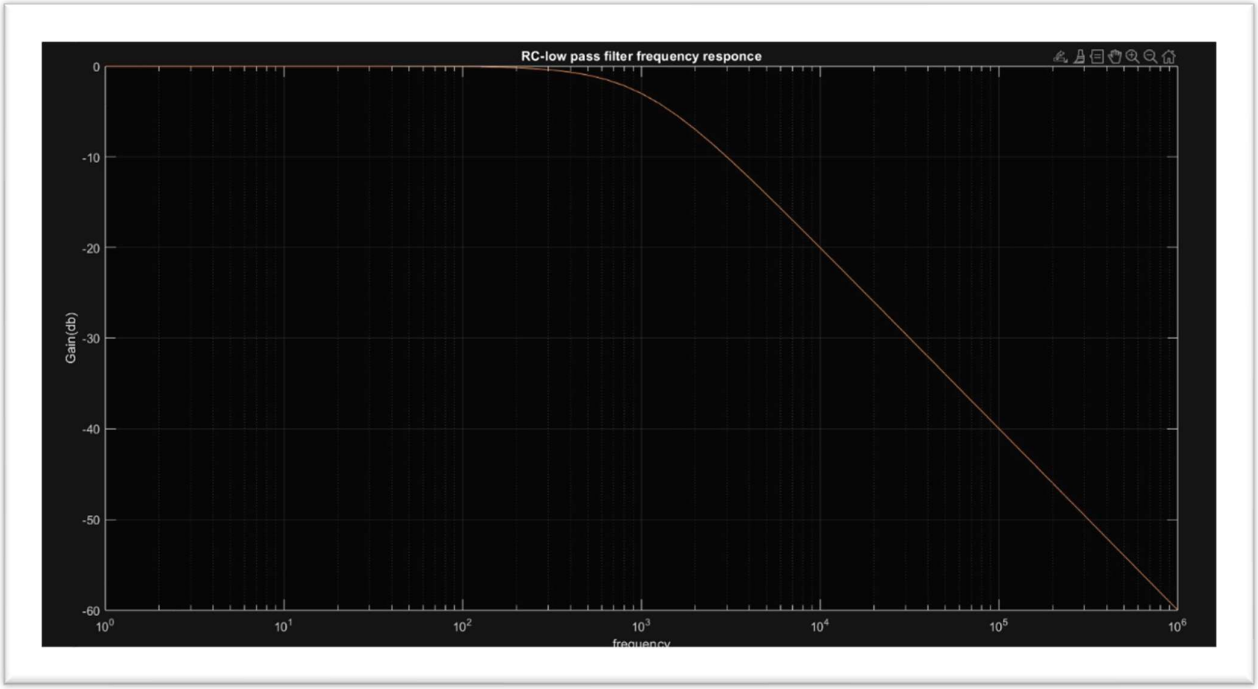
The cutoff frequency (f_c) of an RC low-pass filter is given by fc=1/2*pi*RC. The values of resistance and capacitance was calculated online as shown in figure below.



The calculated fc value comes out to be 999.99964Hz.This value is very close to the desired 1 kHz cutoff frequency



The plot of Vout vs Vin was calculated after using excel to copy values from RC.lis file and then plotted in MATLAB. The plot comes out to be as shown below



Observations:

1)At 1 kHz, a drop of -3 dB in the output voltage is observed.
2)The frequency response should confirm that the circuit acts as a low-pass filter with a cutoff frequency close to 1 kHz.

Q2(a). Make a Verilog-A model for a simple n-channel MOSFET (NMOS) by defining current equations in linear and saturation regions. Verify by plotting input and output characteristics in HSPICE. Consider Vth=0.6V.

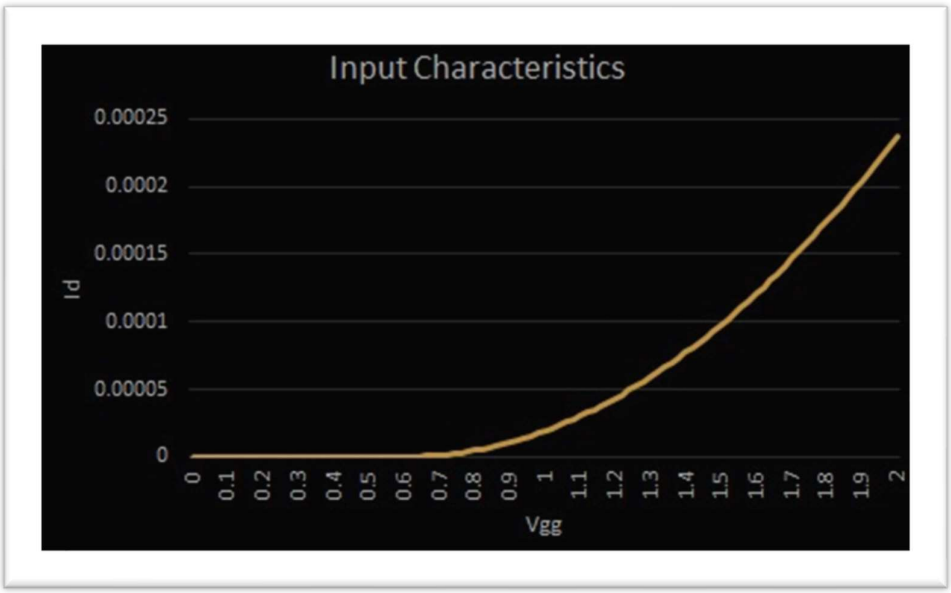
Verilog-A Model file for a NMOS

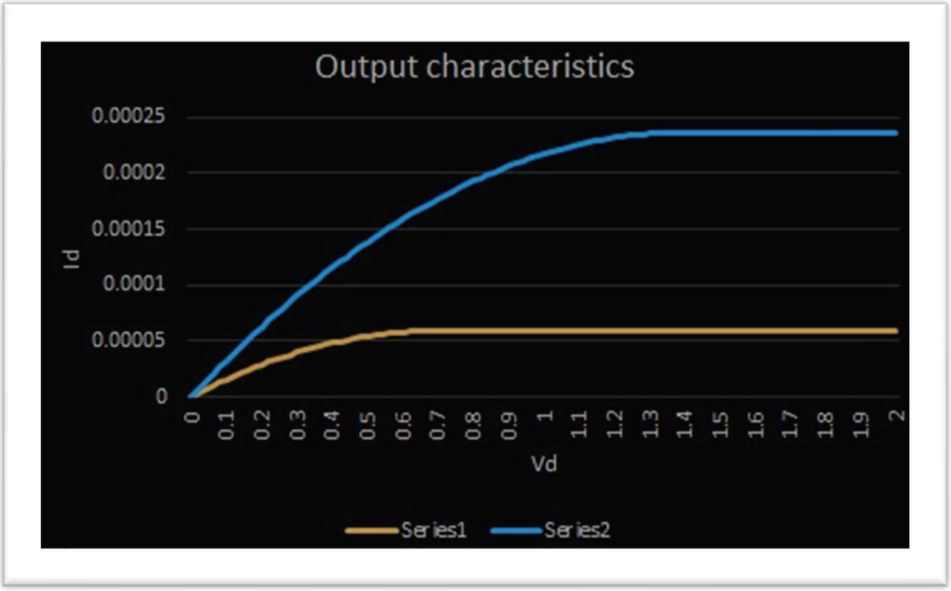
```
`include "disciplines.vams"
`include "constants.vams"
module simple_NMOS(d,g,s,b);
inout d,g,s,b; // inout TERMINALS
electrical d ,g ,s ,b ; //input-output nodes
parameter real W=1e-5 from [0:inf]; // width of MOSFET
parameter real L=1e-5 from [0:inf]; // Length of MOSFET
parameter real Vth=0.6 from [0:inf]; // Threshold voltage
parameter real mu=1400 from [0:inf];
parameter real NA=1e17 from [1e13:1e22]; // Doping

parameter real TOX=20e-7; // Oxide Thickness
parameter real VSB=0.0; //Body-Bias
parameter real P_EPSOX=3.9*8.85e-14;
parameter real P_EPSSI=11.7*8.85e-14;
parameter real COX=P_EPSOX/TOX from [0:inf];
real PHI,GAMMA,PHI_F,VT;
real Id, Vgs, Vds;
real Ni=1e10;
real q=1.6e-19;
analog
begin
if (V(g,s) > Vth)
begin
        if(V(d,s) >= V(g,s)-Vth)
                I(d,s) <+ (mu*W*COX/(2*L))*(V(g,s)-Vth)**2;

        else
                I(d,s) <+ (mu*W*COX/L)*(((V(g,s)-Vth)*V(d,s))-
(V(d,s)*V(d,s)/2));
        end
end
endmodule
```

H-spice file for a NMOS

```
* Basic mos_test
******** Include Files
.OPTION POST=2 INGOLD=2
.hdl "NMOS.va" $ change the names according to your file_names
.model mos simple_nmos $ change module name accordingly
****NETLIST
X1 3 2 0 0 mos
Vdum 4 3 DC 0
Vdd 4 0 DC 2
*Reference Hspice code for NMOS
Vgg 2 0 DC 2
*****Analysis $ LV HV td tr tf PW PER
.dc Vdd 0 2 0.02 vgg 0.6 2 0.35 $ to plot Output Characteristics
*.dc Vgg 0 2 0.02 vdd 0 2 0.5 $ to plot Input Characteristics
*For Ip char uncomment line 14 and for Op char uncomment line 13
.print I(Vdum)
```

The plots were obtained using values taken from the .lis files. The input and output characteristics look as the figure below.





Observations:

1) The input characteristics of an NMOS transistor describe its behavior with respect to the gate-source voltage (Vgs) and the drain current (Id). The threshold voltage (Vth) is the gate-source voltage at which the NMOS transistor starts conducting. Below Vth, the transistor is in the off state, and there is negligible current flow from the drain to the source. When Vgs exceeds Vth, the transistor enters the saturation region. In this region, the NMOS transistor operates as a voltage-controlled current source. The drain current (Id) is relatively insensitive to further increases in Vgs, and it remains relatively constant. As Vgs increases further, the transistor can enter the linear region, where the drain current increases in a more linear manner. In this region, the transistor behaves as a voltage-controlled resistor, and the drain current is directly proportional to Vgs – Vth.

2)The output characteristics of an NMOS transistor describe its behavior in terms of drain current (Id) and drain-source voltage (Vds). In the saturation region, the output characteristics show that the drain current remains relatively constant as Vds increases. This indicates that the NMOS transistor operates in a constant-current mode in this region, offering a relatively low output resistance. If Vds continues to increase beyond the saturation region, the transistor enters the triode or linear region. In this region, the drain current decreases as Vds increases, and the transistor behaves as a variable resistor.The resulting plot shows the drain current (Ids) versus the gate-source voltage (Vgs) for various drain-source voltages.

Q2(b). Design a basic INVERTER using the NMOS and verify by applying a square pulse at Gate.

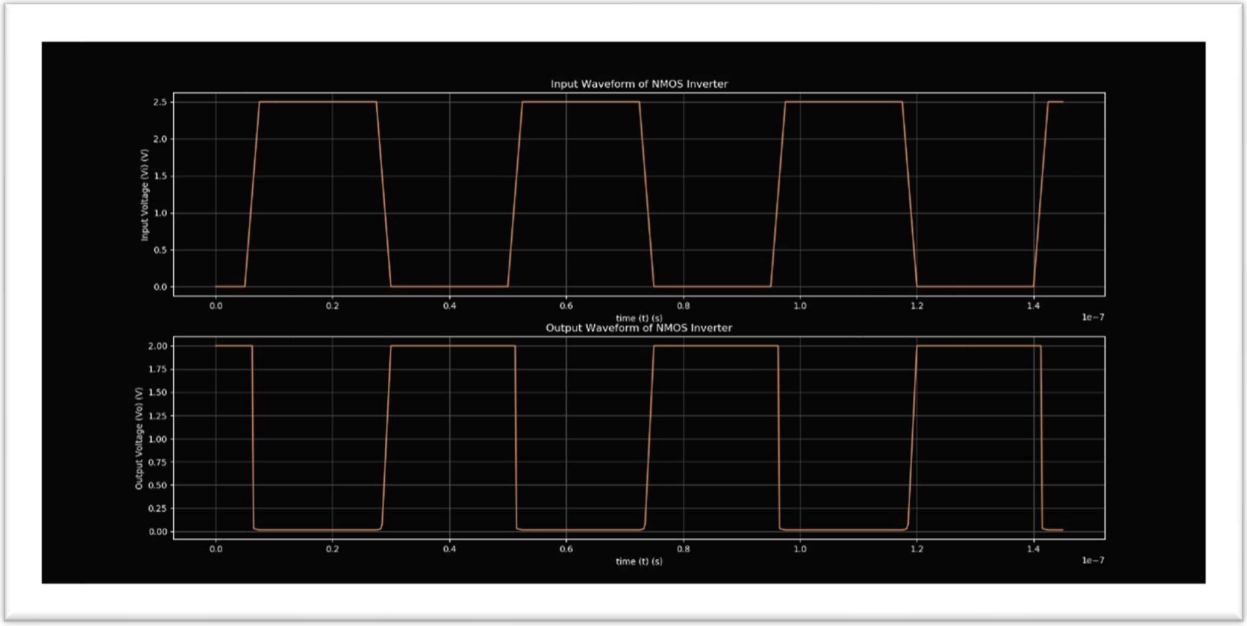
Verilog-A Model file for a NMOS

```
`include "disciplines.vams"
`include "constants.vams"
module simple_NMOS(d,g,s,b);
inout d,g,s,b; // inout TERMINALS
electrical d ,g ,s ,b ; //input-output nodes
parameter real W=1e-5 from [0:inf]; // width of MOSFET
parameter real L=1e-5 from [0:inf]; // Length of MOSFET
parameter real Vth=0.6 from [0:inf]; // Threshold voltage
parameter real mu=1400 from [0:inf];
parameter real NA=1e17 from [1e13:1e22]; // Doping

parameter real TOX=20e-7; // Oxide Thickness
parameter real VSB=0.0; //Body-Bias
parameter real P_EPSOX=3.9*8.85e-14;
parameter real P_EPSSI=11.7*8.85e-14;
parameter real COX=P_EPSOX/TOX from [0:inf];
real PHI,GAMMA,PHI_F,VT;
real Id, Vgs, Vds;
real Ni=1e10;
real q=1.6e-19;
analog
begin
if (V(g,s) > Vth)
begin
        if(V(d,s) >= V(g,s)-Vth)
                I(d,s) <+ (mu*COX/(2*L))*(V(g,s)-Vth)**2;

        else
                I(d,s) <+ (mu*COX/L)*(((V(g,s)-Vth)*V(d,s))-(V(d,s)*V(d,s)/2));
        end
end
endmodule
```

H-spice file for a NMOS

```
* Basic mos_test
******** Include Files
.OPTION POST=2 INGOLD=2
.hdl "NMOS.va" $ change the names according to your file_names
.model mos simple_nmos $ change module name accordingly
****NETLIST
X1 3 2 0 0 mos
R 4 3 100K
Vdd 4 0 DC 2

Vgg 2 0 PULSE(0 2.5 5n 2.5n 2.5n 20n 45n)


*****Analysis $ LV HV td tr tf PW PER

.tran 250p 145n

.print V(3) V(2)
```

Plot for input and output waveforms are shown below.



Observations:

The simulation results shows the expected inverter behavior where the input and output values are inverse of each other confirming the inversion of the input signal at the output due to the NMOS switching action.The NMOS switches ON when input goes high thus pulling the output waveform to zero and vice versa.

Q3. Repeat Q2(a) for a PMOS transistor. Plot magnitude of current versus Vds
(Vdd=0 to -2V) at Vgg=-2V, and magnitude of current versus Vgs (Vgg=0 to -2V) at
Vdd=-2V. Consider Vth=-0.6V.
Note the following differences compared to NMOS: PMOS is ON when Vgs < Vth, is
in linear region when Vds >= (Vgs-Vth), and is in saturation when Vds < (Vgs-Vth).

Verilog-A Model for a PMOS

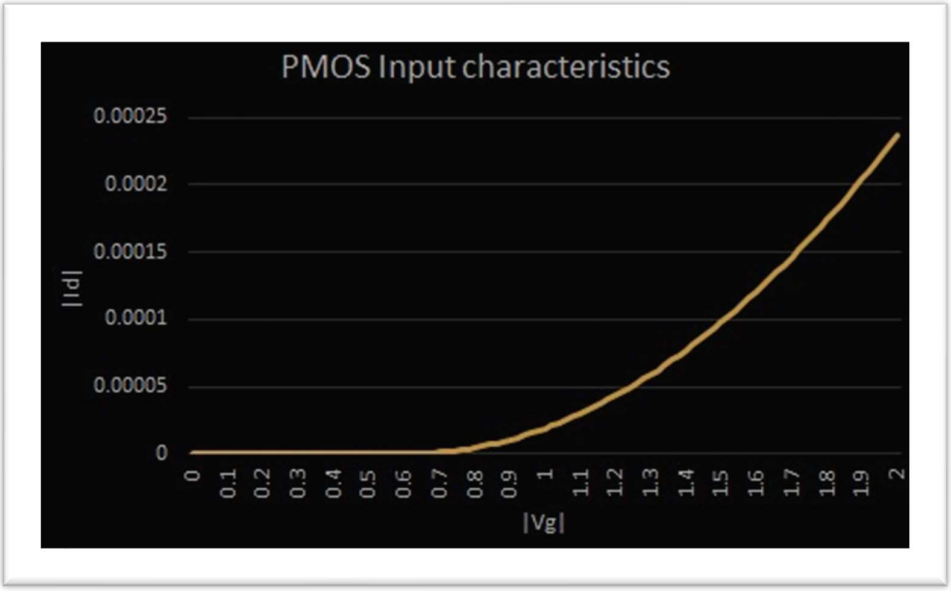
```
`include "disciplines.vams"
`include "constants.vams"
module simple_PMOS(d,g,s,b);
inout d,g,s,b; // inout TERMINALS
electrical d ,g ,s ,b ; //input-output nodes
parameter real W=1e-5 from [0:inf]; // width of MOSFET
parameter real L=1e-5 from [0:inf]; // Length of MOSFET
parameter real Vth=-0.6 from [-inf:inf]; // Threshold voltage
parameter real mu=400 from [0:inf];
parameter real Nd=1e17 from [1e13:1e22]; // Doping

parameter real TOX=20e-7; // Oxide Thickness
parameter real VSB=0.0; //Body-Bias
parameter real P_EPSOX=3.9*8.85e-14;
parameter real P_EPSSI=11.7*8.85e-14;
parameter real COX=P_EPSOX/TOX from [0:inf];
real PHI,GAMMA,PHI_F,VT;
real Id, Vgs, Vds;
real Ni=1e10;
real q=1.6e-19;
```

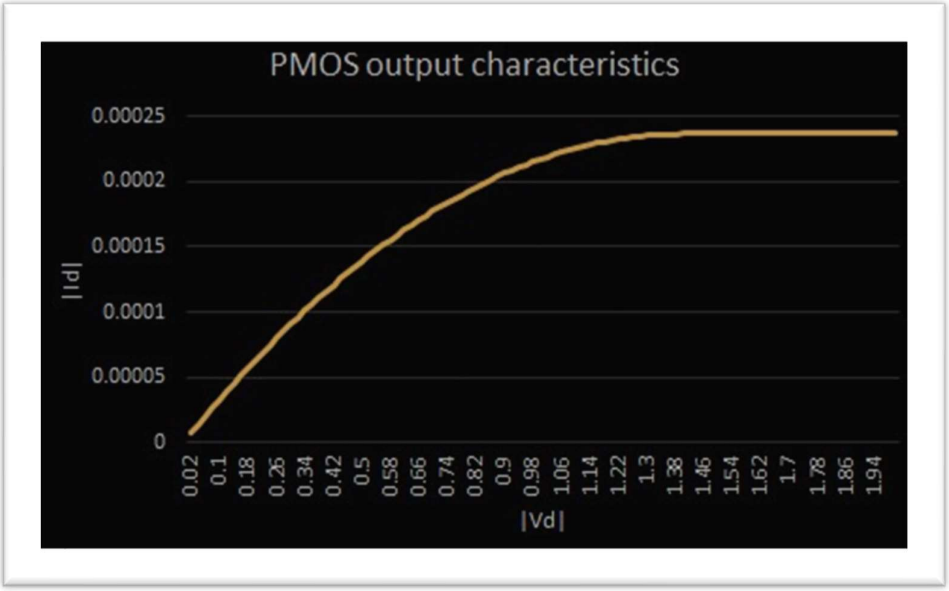
```
analog
begin
if (V(g,s) < Vth)
begin
        if(V(d,s) >= V(g,s)-Vth)
                I(s,d) <+ (mu*COX/L)*(((V(g,s)-Vth)*V(d,s))-(V(d,s)*V(d,s)/2));


        else
                I(s,d) <+ (mu*COX/(2*L))*(V(g,s)-Vth)**2;
        end
end
endmodule
```

H-spice file for a PMOS

```
* Basic mos_test
******** Include Files
.OPTION POST=2 INGOLD=2
.hdl "PMOS.va" $ change the names according to your file_names
.model mos simple_pmos $ change module name accordingly
****NETLIST
X1 3 2 0 0 mos
Vdum 4 3 DC 0
Vdd 4 0 DC -2
*Reference Hspice code for NMOS
Vgg 2 0 DC -2
*****Analysis $ LV HV td tr tf PW PER
*.dc Vdd 0 -2 0.02 vgg -0.5 -2 0.5  $ to plot Output Characteristics
.dc Vgg 0 -2 0.02 vdd -0.5 -2 0.5 $ to plot Input Characteristics
*For Ip char uncomment line 14 and for Op char uncomment line 13
.print I(Vdum)
```

Plot


PMOS Input characteristics
0.00025
0.0002
0.00015
0.0001
0.00005
0
|Id|
0 0.1 0.2 0.3 0.4 0.5 0.6 0.7 0.8 0.9 1 1.1 1.2 1.3 1.4 1.5 1.6 1.7 1.8 1.9 2
|Vg|


PMOS output characteristics
0.00025
0.0002
0.00015
0.0001
0.00005
0
|Id|
0.02 0.1 0.18 0.26 0.34 0.42 0.5 0.58 0.66 0.74 0.82 0.9 0.98 1.06 1.14 1.22 1.3 1.38 1.46 1.54 1.62 1.7 1.78 1.86 1.94
|Vd|

Observations:

1) The input characteristics of a PMOS transistor describe its behavior with respect to the gate-source voltage (Vgs) and the drain current (Id). The threshold voltage (Vth) for a PMOS transistor is the gate-source voltage at which the transistor starts conducting. Above Vth, the transistor is in the off state, and there is negligible drain current (Id). When Vgs is less negative than Vth (i.e., Vgs < Vth), the PMOS transistor operates in the saturation region. In this region, the drain current (Id) is relatively insensitive to further decreases in Vgs, and it remains relatively constant, following a similar quadratic relationship to NMOS transistors.

2) The output characteristics of a PMOS transistor describe its behavior with respect to drain current (Id) and drain-source voltage (Vds). In the saturation region, the output characteristics show that the drain current remains relatively constant as Vds increases, similar to the NMOS transistor. The transistor operates in a constant-current mode in this region, offering a relatively high output resistance compared to NMOS.If Vds continues to increase beyond the saturation region, the PMOS transistor enters the triode or linear region. In this region, the drain current decreases as Vds increases, and the transistor behaves as a variable resistor.

Q4. Design a CMOS inverter using NMOS (from Q2) and PMOS (from Q3) and verify by applying the same input square pulse as in Q2(b), however the pulse oscillates between 0V and 2V in this case. The circuit for CMOS is shown in Fig. A.

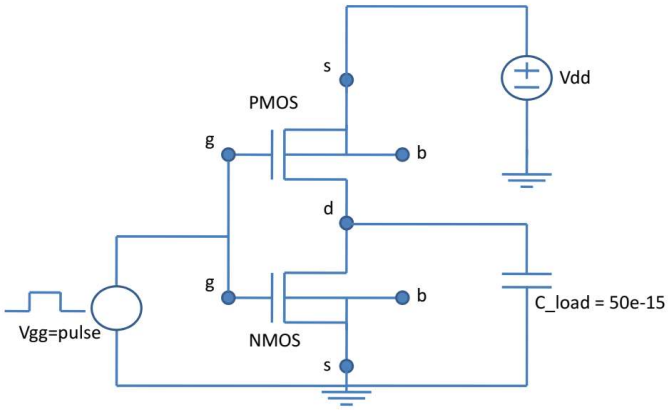


Fig. A: CMOS Inverter circuit

Verilog-A Model for a NMOS

```
`include "disciplines.vams"
`include "constants.vams"
module simple_NMOS(d,g,s,b);
inout d,g,s,b; // inout TERMINALS
electrical d ,g ,s ,b ; //input-output nodes
parameter real W=1e-5 from [0:inf]; // width of MOSFET
parameter real L=1e-5 from [0:inf]; // Length of MOSFET
parameter real Vth=0.6 from [0:inf]; // Threshold voltage
parameter real mu=1400 from [0:inf];
parameter real NA=1e17 from [1e13:1e22]; // Doping

parameter real TOX=20e-7; // Oxide Thickness
parameter real VSB=0.0; //Body-Bias
```

```
parameter real P_EPSOX=3.9*8.85e-14;
parameter real P_EPSSI=11.7*8.85e-14;
parameter real COX=P_EPSOX/TOX from [0:inf];
real PHI,GAMMA,PHI_F,VT;
real Id, Vgs, Vds;
real Ni=1e10;
real q=1.6e-19;
analog
begin
if (V(g,s) > Vth)
begin
        if(V(d,s) >= V(g,s)-Vth)
                I(d,s) <+ (mu*COX/(2*L))*(V(g,s)-Vth)**2;

        else
                I(d,s) <+ (mu*COX/L)*(((V(g,s)-Vth)*V(d,s))-(V(d,s)*V(d,s)/2));
        end
end
endmodule
```

Verilog-A Model for a PMOS

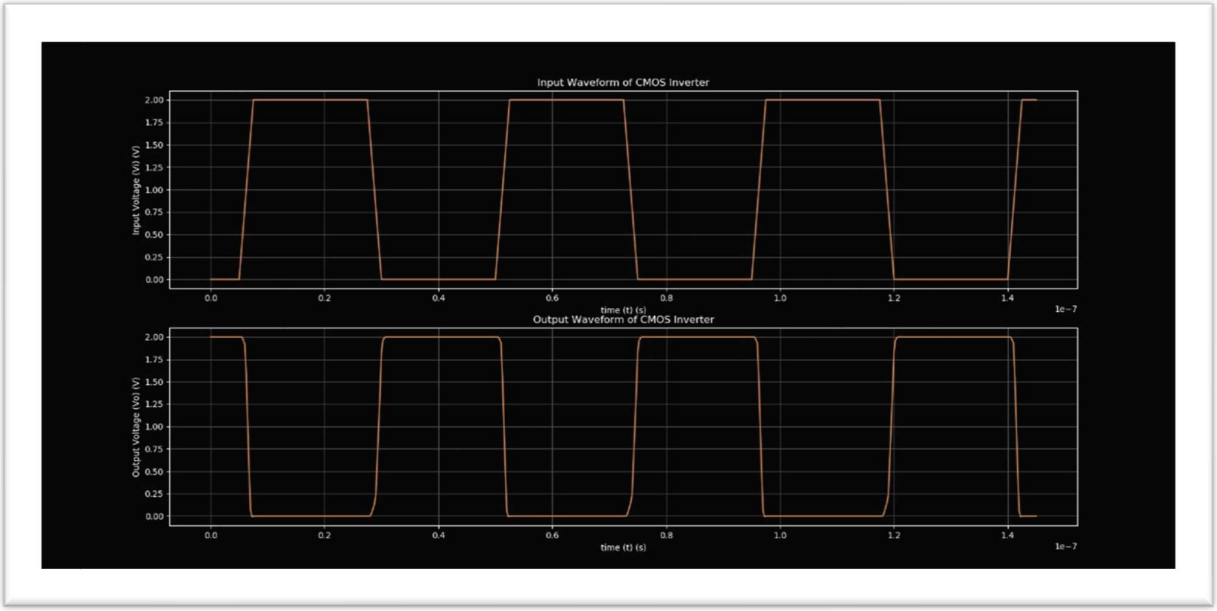
```
`include "disciplines.vams"
`include "constants.vams"
module simple_PMOS(d,g,s,b);
inout d,g,s,b; // inout TERMINALS
electrical d ,g ,s ,b ; //input-output nodes
parameter real W=1e-5 from [0:inf]; // width of MOSFET
parameter real L=1e-5 from [0:inf]; // Length of MOSFET
parameter real Vth=-0.6 from [-inf:inf]; // Threshold voltage
parameter real mu=400 from [0:inf];
parameter real Nd=1e17 from [1e13:1e22]; // Doping

parameter real TOX=20e-7; // Oxide Thickness
parameter real VSB=0.0; //Body-Bias
parameter real P_EPSOX=3.9*8.85e-14;
parameter real P_EPSSI=11.7*8.85e-14;
parameter real COX=P_EPSOX/TOX from [0:inf];
real PHI,GAMMA,PHI_F,VT;
real Id, Vgs, Vds;
```

```
real Ni=1e10;
real q=1.6e-19;
analog
begin
if (V(g,s) < Vth)
begin
        if(V(d,s) >= V(g,s)-Vth)
                I(s,d) <+ (mu*COX/L)*(((V(g,s)-Vth)*V(d,s))-(V(d,s)*V(d,s)/2));


        else
                I(s,d) <+ (mu*COX/(2*L))*(V(g,s)-Vth)**2;
        end
end
endmodule
```

H-spice file for a CMOS

```
* Basic mos_test
******** Include Files
.OPTION POST=2 INGOLD=2
.hdl "NMOS.va" $ change the names according to your file_names
.model nmos simple_nmos $ change module name accordingly
.hdl "PMOS.va" $ change the names according to your file_names
.model pmos simple_pmos $ change module name accordingly
**************netlist
X1 1 2 3 3 pmos
X2 1 2 0 0 nmos
vdd 3 0 DC 2
c 1 0 0.00050pF
Vgg 2 0 PULSE(0 2 5n 2.5n 2.5n 20n 45n)

.tran 250p 145n
.print V(2) V(1)
```

Plot for input and output waveforms are shown below.



Observations:

The output should display an inverted signal concerning the input square wave, as the NMOS and PMOS act complementary to each other. When the NMOS is ON, the PMOS is OFF, and vice versa.

The CMOS inverter uses both NMOS and PMOS transistors, enabling it to efficiently invert the input signal. When the input square wave oscillates between 0V and 2V, the output should oscillate between 2V and 0V, displaying the expected inverting action characteristic of a CMOS inverter.