MARMARA UNIVERSITY

FACULTY OF ENGINEERING

ELECTRICAL AND ELECTRONICS ENGINEERING

ELECTRONICS 1

Simulation Project: Cockcroft-Walton Generator

Berat Asrın CAFEROĞLU – 150718056

1- Introduction to Cockcroft-Walton Generator

What Is the Cockcroft-Walton Generator?

- **Cockcroft-Walton Generator** is a simple **voltage multiplier** circuit that is designed by John Cockcroft and Ernest Walton. This generator bring them a Nobel Prize. Main idea behind this circuit is that circuit multiplies the input several times and give it to the output.
- This generator has a very special property, the input and the output are not in the same waveform. Because of the circuit characteristics the input in the form of **Alternative Current (AC)** occurs in the output as **Direct Current (DC)**.

Which Areas Do We Use This Generator?

- Cockcroft-Walton Generator is invented by scientists to be used as **accelerator for atomic particles**, and its smaller versions provided high voltages in the cathode ray tube televisions in the past. Of course the generators that creates high-voltage output needs a greater companents instead of the ones that we use in everyday electronics.
- In today's world this type of generator is used in the devices which need high voltages to operate such as X-ray, microwave ovens etc.
- Before getting to the technical or schemetic part of this circuit let us see the picture of this generator.

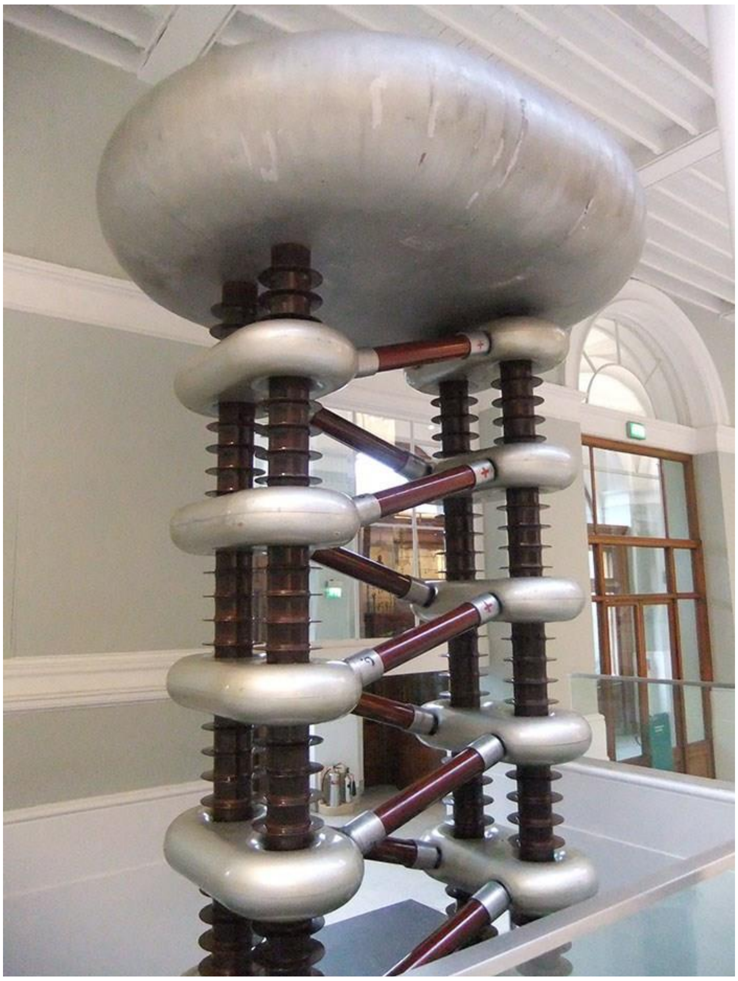

Figure 1: The Cockcroft-Walton Generator

2- CIRCUIT DESCRIPTION

Building Block of the Cockcroft-Walton Generator: Voltage Doubler

- In fact, Cockcroft-Walton generator is based on the **voltage doubler** circuit. If we get many of them together in as special way we can obtain Cockcroft-Walton generator. So that, let us get familiar with the voltage doubler circuit.
- Voltage doubler is the voltage multiplier which scales the V_{peak} of the **AC** input by **2** and gives the output in the **DC**. Basicly we can say that $\mathbf{V_{out} = 2V_{peak}}$. The circuit scheme of this multiplier is given below.

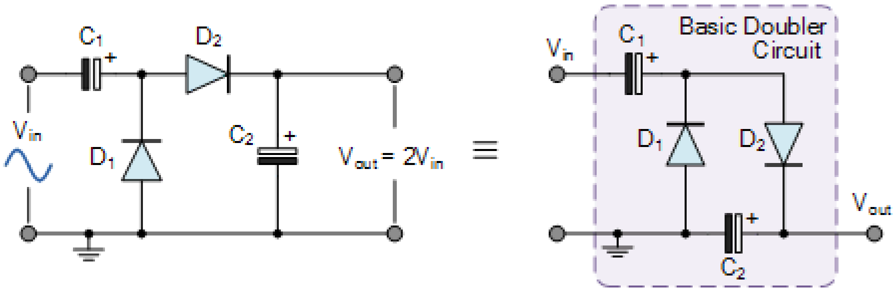

Figure 2: Circuit Scheme For Voltage Doubler

- We have AC input, so that to give a direction to the current the diodes are sufficient to use. Let us simulate the circuit step by step. In order to make the explaination simple the **diodes are assumed as ideal**, means that there is no loss on the diodes. And initially all the **capacitors are uncharged**.
  1. Assume that $\mathbf{V_{in}}$ is at the **negative peak**.
  2. In such case the $\mathbf{D_1}$ diode is **forward biased** because the P side has greater voltage than N side, that is, this diode is conducting.
  3. This case allows to charge the $\mathbf{C_1}$ capacitor up to $\mathbf{V_{in}}$.
  4. Meanwhile the $\mathbf{D_2}$ diode is also **forward biased** just for one time in this half wave, and the reason will be explained in following steps.
  5. The capacitor $\mathbf{C_2}$ is charged up to $\mathbf{V_{in}}$.
  6. Then, assume that $\mathbf{V_{in}}$ is at the **positive peak**.
  7. In such case the $\mathbf{D_1}$ diode is **reversed biased** because the P side has lower voltage than N side, that is, this diode is not conducting.
  8. Remember that the $\mathbf{C_1}$ was charged up to $\mathbf{V_{in}}$ now it supports the source and the node at the plus side of $\mathbf{C_1}$ has $\mathbf{V_{in} + V_{in} = 2V_{in}}$.
  9. So that, the $\mathbf{D_2}$ is **forward biased**, and it conducts the current. The node at the N side of diode has the voltage of $\mathbf{2V_{in}}$ because there is no loss on the diode due to diodes are ideal.
  10. In the step 3 we said that $\mathbf{C_1}$ is charged up to $\mathbf{V_{in}}$ just for one time because now it will be charged up to $\mathbf{2V_{in}}$, and now the input voltage is doubled at the output as you can see. Notice that while charging the $\mathbf{C_2}$ the $\mathbf{C_1}$ will be discharging.
- Let us repeat the same procedure but this time we continue from the step 10 where the capacitors are charged. $\mathbf{C_1 < V_{in}}$ because it charged the other capacitor, $\mathbf{C_2 = 2V_{in}}$. Again assume that the **diodes are ideal**.
  11. We have $\mathbf{V_{in}}$ that is at the **negative peak** again.
  12. The P side of $\mathbf{D_1}$ diode has $\mathbf{V_{in}}$ again, and remember that $\mathbf{C_1 < V_{in}}$, that is, the N side has a voltage less than $\mathbf{V_{in}}$. Thus, the diode $\mathbf{D_1}$ is **forward biased**.
  13. $\mathbf{C_1}$ is being charged now up to $\mathbf{V_{in}}$.
  14. Unlike **step 4**, the $\mathbf{D_2}$ diode **reversed biased** now. So that, the current coming from the **plus side** of the voltage source cannot return to the **minus side** of the voltage source.
  15. In such condition if we connect a load resistor to the $\mathbf{V_{out}}$. The $\mathbf{C_2}$ will be source to this load. And at the and of the **negative half-wave** the voltage stored in the $\mathbf{C_2}$ will be less than $\mathbf{2V_{in}}$. So that, $\mathbf{C_2 < 2V_{in}}$.
  16. Now let us assume that the $\mathbf{V_{in}}$ is at the **positive peak** again.

17. Now capacitor C_1 supports the voltage source and the plus side of the capacitor will be **$2V_{in}$**.
18. In this case, the D_1 is **reversed biased**, and it does not conduct the electricity because the N side has greater voltage value than P side.
19. And the D_2 diode is **forward biased**, because the P side has greater voltage.
20. At the end of the **negative half-wave** we said that **$C_2 < 2V_{in}$**, and the **D_2** conducts the electricity. So that, the capacitor **C_2** is charged up to **$2V_{in}$** again.

- Let us simulate the voltage doubler and see the input output relationship.

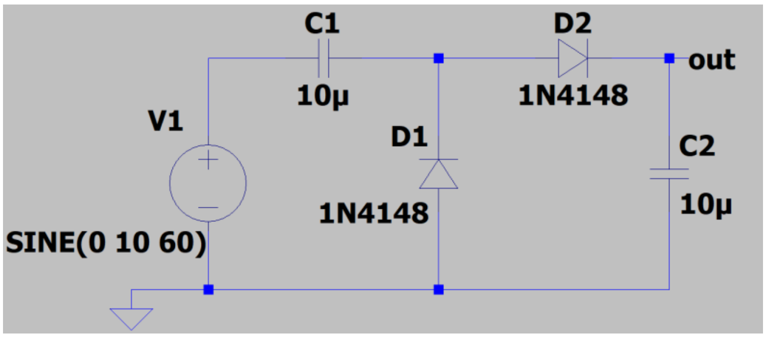

Figure 3: Voltage Doubler Circuit

- The source **V_1** has peak value of **10 volts**, frequency of **60 Hz**, and the phase of **0 radians**. Theoretically we expect the output to be **$V_{out} = 2V_1 = 20$ volts**. The output of the simulation is given below.

Figure 4: Output Voltage According To Time

- Here we see that **V_{out} = 19.310003 volts**. Actually the results can be considered as great because we do not have any ideal diodes in the real life, and note that the **1N4148** has the **forward voltage around 0.65 volts**. The improvement ideas to decrease the error percentage will be given in the following parts after the Cockcroft-Walton generator.
  - $Percentage\ Error = \frac{20-19.310003}{20} \times 100\% = 3.449985\%$
  - This error mostly occurs because of the drop on the D_2 diode.
- This type of voltage multipliers are called as **half-wave voltage multiplier** because only one half of the input source charges the **C_2**. Now we will discuss how to design a **full-wave voltage multiplier** shortly.

- In order to have **full-wave voltage multiplier** just connect two voltage doubler to the same ground. The important point here is that because of we connect the plus side of $\mathbf{V_2}$ to the ground there is $\boldsymbol{\pi}$ **radians** phase angle between them. In other words, the **full-wave voltage multiplier** can be created by using 2 **half-wave voltage multipliers** with **different polarities**. Notice that capacitor $\mathbf{C_2}$ is being charged in the both half-waves.

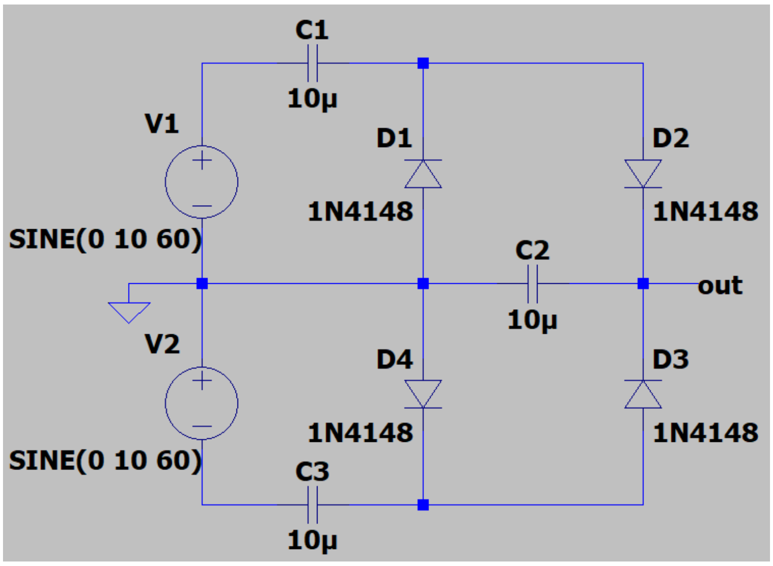

Figure 5: Full-Wave Voltage Doubler Circuit

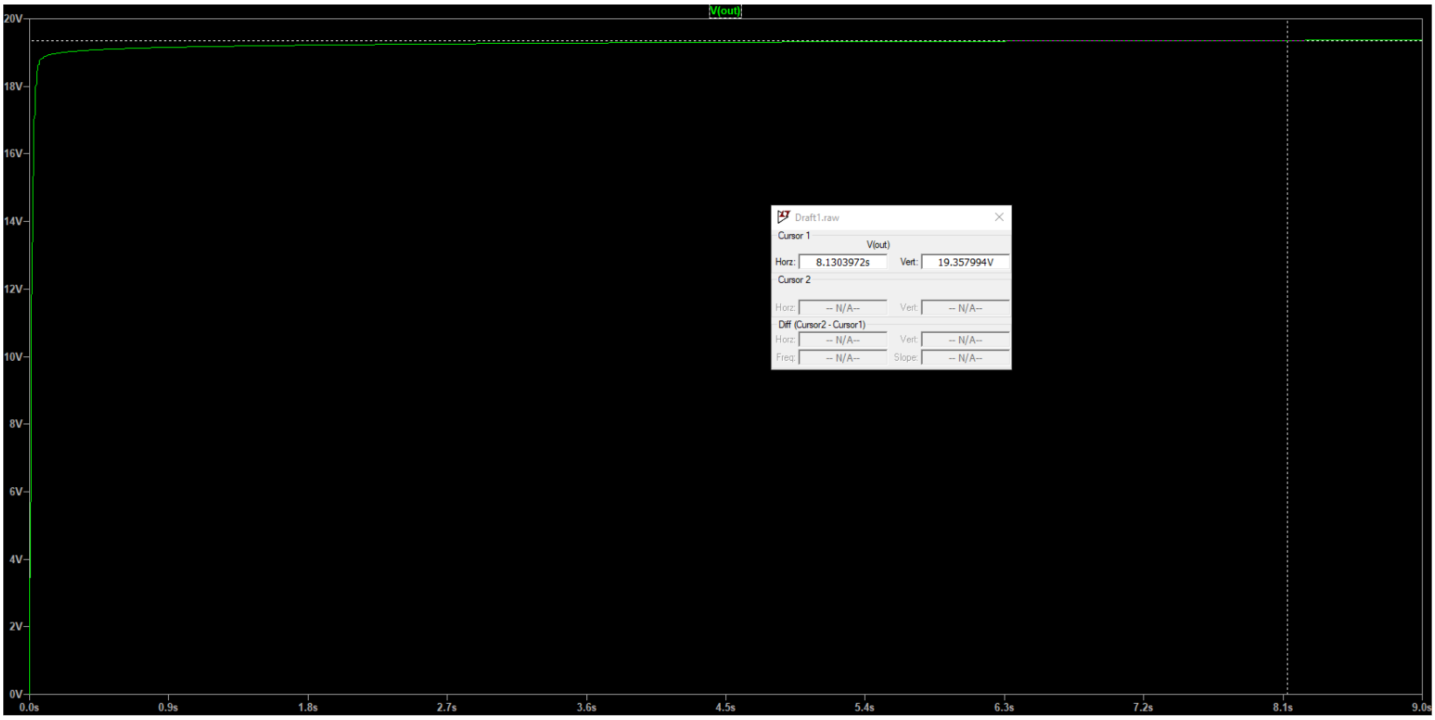

Figure 6: Output of the Full-Wave Voltage Doubler

- The output of the **full-wave voltage doubler** is given above at the same instant with **half-wave voltage doubler**.
  - $Percentage\ Error = \frac{20-19.357994}{20} \times 100\% = 3.21003\%$
  - The error is decreased because we design full-wave voltage multipliers to have **less ripples** in the output. So, because of the ripples have been decreased the average output have been increased, that is, the DC value have been increased too.
  - If the peak value of the input source were more greater value the percentage error in the half-wave voltage doubler would be also greater.

- The main **advantage of the voltage multiplier circuits** is that these circuits allow to have high voltages using the low input voltages without using expensive transformer or OP-AMP. In other words, they are cost efficient.
- The main **disadvantage of the voltage multiplier circuits** is that to get a stable DC output the capacitance values of the capacitor should be arranged properly. Otherwise, the **ripples may be occur** in the output, and the form becomes other than DC. To prevent these **ripples** the **full-wave voltage multiplier** is recommended to use.

Cockcroft-Walton Generator Circuit

- In the previous part we studied the voltage doubler, and the Cockcroft-Walton generator is just the circuit consists of **cascaded voltage doublers**.
- The reference model that I searched uses a **half-wave voltage multiplier** type of the generator. In this part, we will analyze the reference circuit, and then my improvements on the circuit will be given in the coming parts.

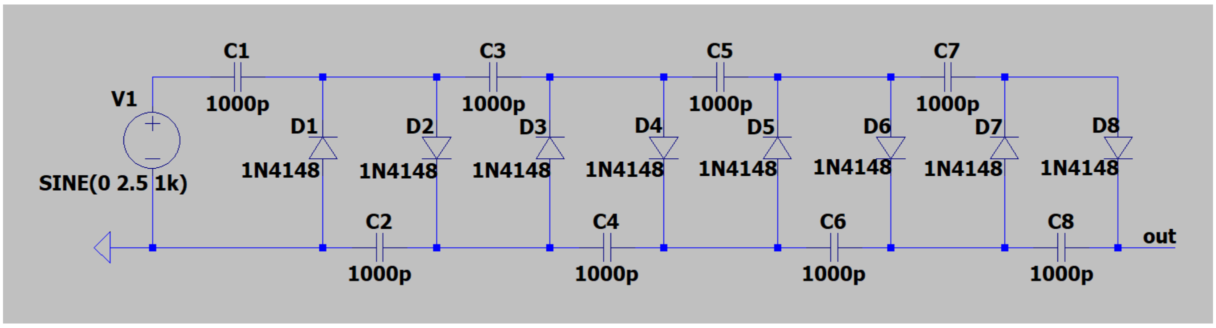

Figure 7: A Four-Stage Half-Wave Cockcroft-Walton Generator Circuit

- Here every one **voltage doubler** is called **stage** and **number of stages** is represented by **N**. Remember that the voltage doubler consists of **two capacitors** and **two diodes**. Therefore, the number of stages can be calculated easily by the formula:
  - $N = \frac{Number\ of\ Diodes}{2}$
  - For example, in figure 7 we have 8 diodes, let us divide it 2. Then, we have **four stages**.
- Assuming the diodes in the design are ideal and there is no voltage loss on them. In that case, we can say that:
  - $V_{out} = 2NV_{peak} = NV_{peak-to-peak}$
  - The V_{peak} represent that the peak point of the source called V_1.
  - The $V_{peak-to-peak}$ represent that the peak-to-peak voltage difference of the source called V_1.
- Of course there will be less output voltage than expected in real life because,
  - **We do not have any ideal diodes** in real life. So that, there is always a voltage loss on them.
  - The capacitance values of the capacitors affect the amount of **ripples**. So, this value should be arranged wisely according to the needed output.
  - No need to mention but as we make the system more closer to the expected output the cost of the circuit will be more expensive due to the component selections.
- Now let us simulate the reference design without connecting any load to the output and any improvments on the reference circuit. The components are as follows:
  - 1000pF Capacitors
  - AC Signal Source (5 V Peak-To-Peak, 1kHz Frequency, 0 Radian Phase)
  - 1N4148 Diodes

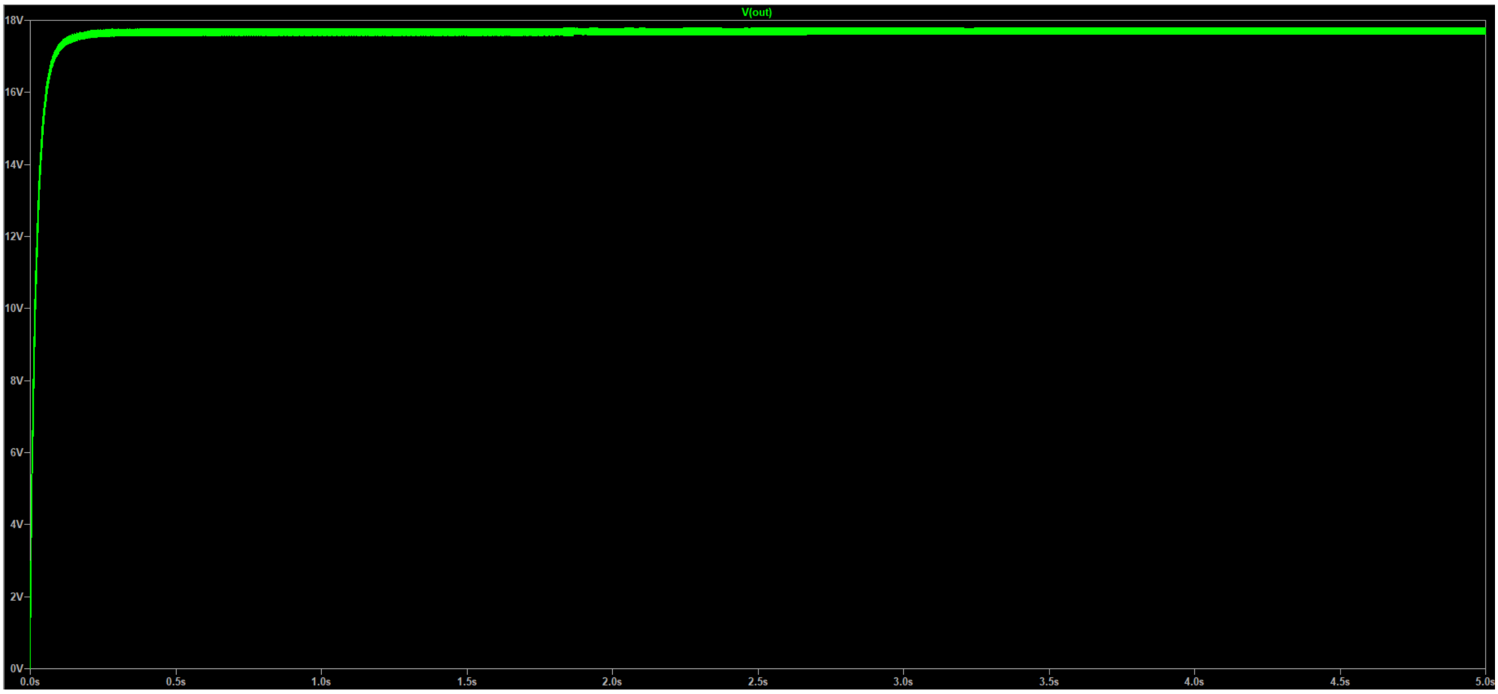

Figure 8: Output of Reference Design Without Load

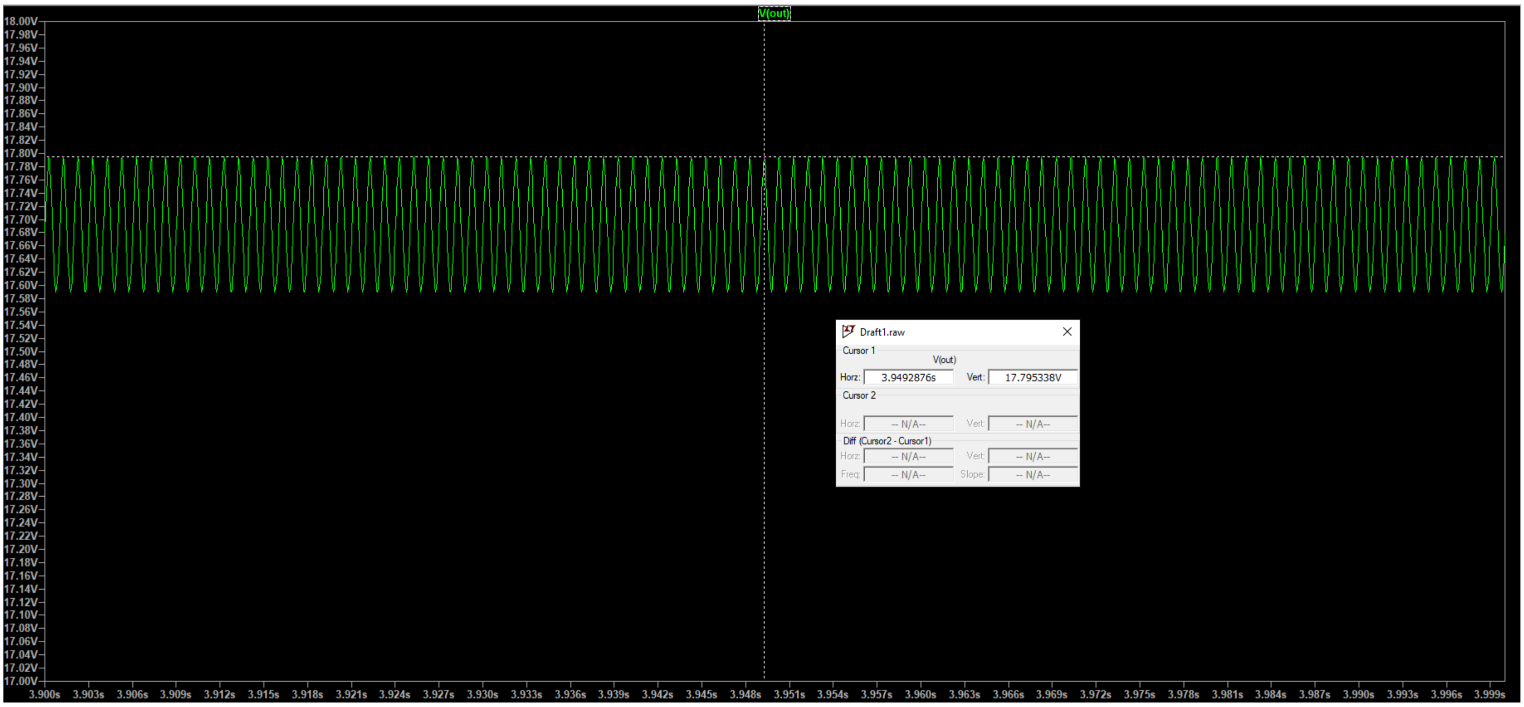

Figure 9: Zoomed Output of Reference Design Without Load

- As you can see from the figure 8 the output of the generator is **V_{out} = 17.795338 volts**. If we check percentage error and efficiency of the circuit without load:
  - $Number\ of\ Stages\ (N) = 4,\ V_{peak-to-peak} = 5\ volts$
  - $Expected\ Output = NV_{peak-to-peak} = 4 \times 5 = 20\ volts$
  - $Percentage\ Error = \frac{20-17.795338}{20} \times 100\% = 11.02331\%$
  - $Efficiency = \frac{17.795338}{20} \times 100\% = 88.97669\%$

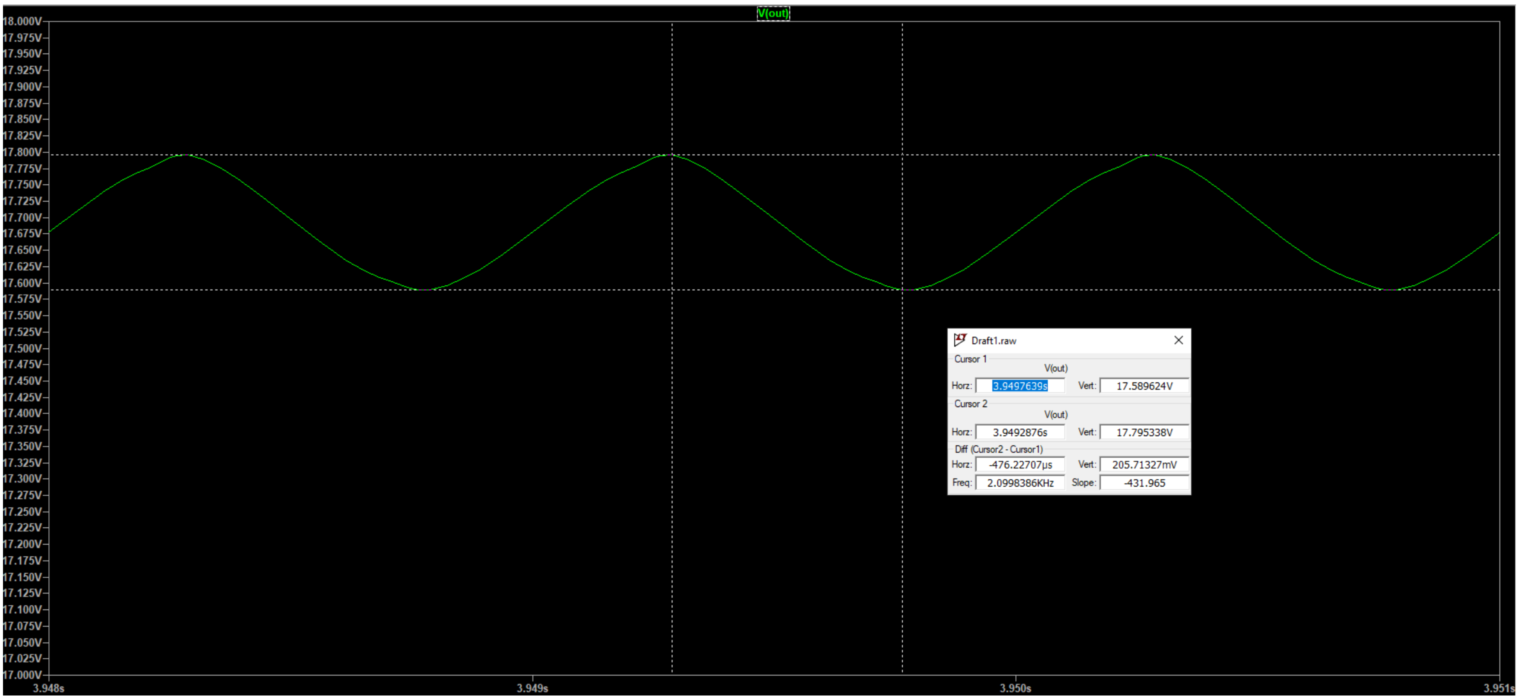

Figure 10: Ripple In the Reference Design

- Even though we said the output is DC with these capacitor values and diodes there is a lot ripple. Which can be found using peak-to-peak difference at the output. It is seen that LTSpice calculates the difference between cursors and the result is:
  - $Amount\ of\ Ripple = V_r = 17.795338 - 17.589624 = 205.71327\ mV$
- Without load at the output everything is fine because the only deal of the circuit is to charge capacitors but if we connect a load, the current will also pass through the load resistor. So, let us check what happens in the output if we connect an 100 kΩ load.

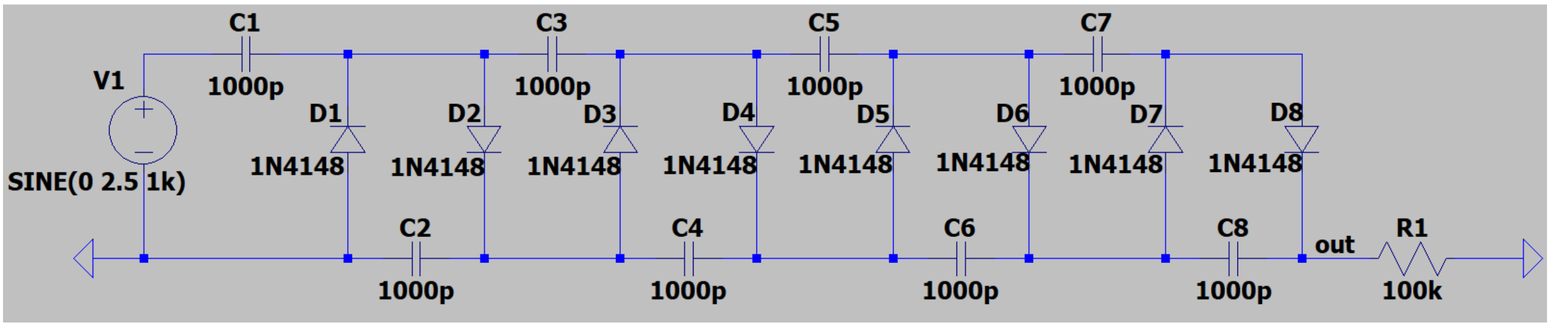

Figure 11: Reference Design With Load Resistor

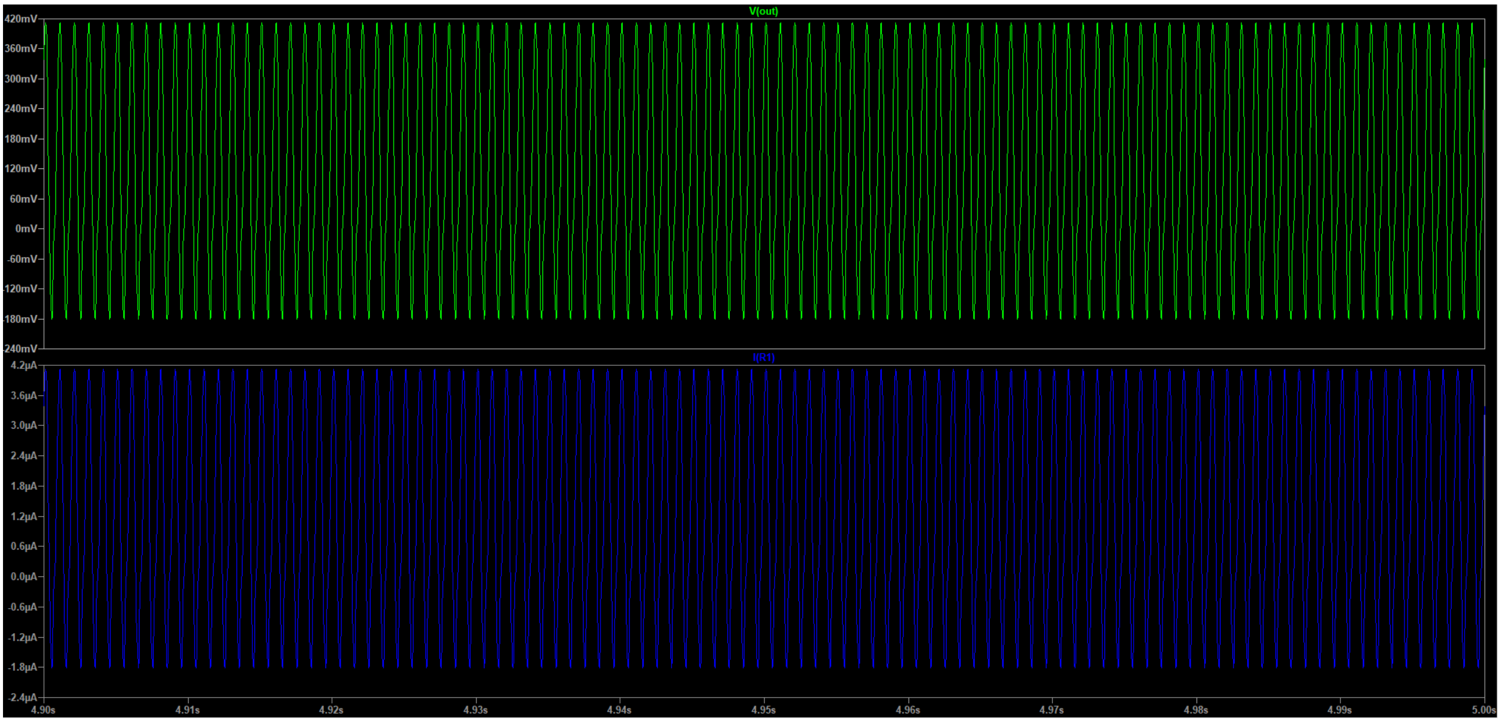

Figure 12: Output of Reference Design With Load

- As you can see from the figure 12 the output with load resistor is far away from what we expected and which is a big problem. Even if we connect a big resistor like 100 kΩ the output is not satisfying. So that, the reference design and the values of components must be rearranged.

3- Circuit Improvements

- In this part we will discuss how the circuit can be more stable and how to output converge to the DC with existence of load resistor. At the end of the this part the comparison between reference circuit and improved circuit will be discussed. Shortly, this part contains my improvement ideas about reference design.

Step 1: Use Full-Wave Voltage Multiplier Instead Of Half-Wave

- As it is mentioned before there is several ways to eliminate the ripples and get DC output. The first of them is connecting the voltage multiplier stages in **full-wave order**.
- To design full-wave voltage multiplier two voltage multiplier circuits must be connected with opposite polarities.

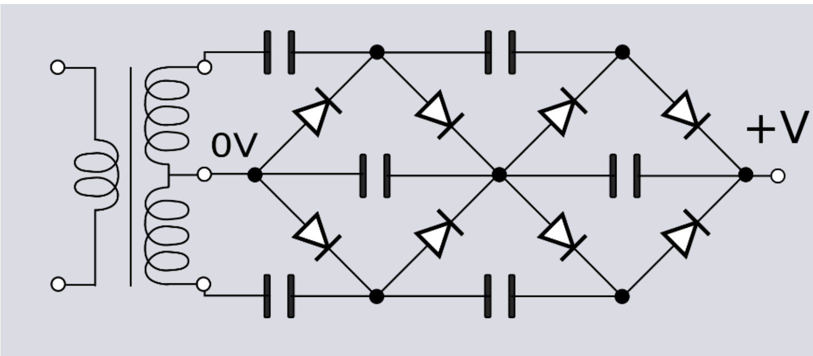

Figure 13: Two-Stage Full-Wave Cockcroft–Walton Generator

- In the figure 13 the transformer is used to explain the design of the full-wave voltage multiplier. In my improvement the transformer will not be exist to decrease the cost of the circuit. Instead of transformer two AC voltage sources with opposite polarities, in other words sharing the same ground, will be used.

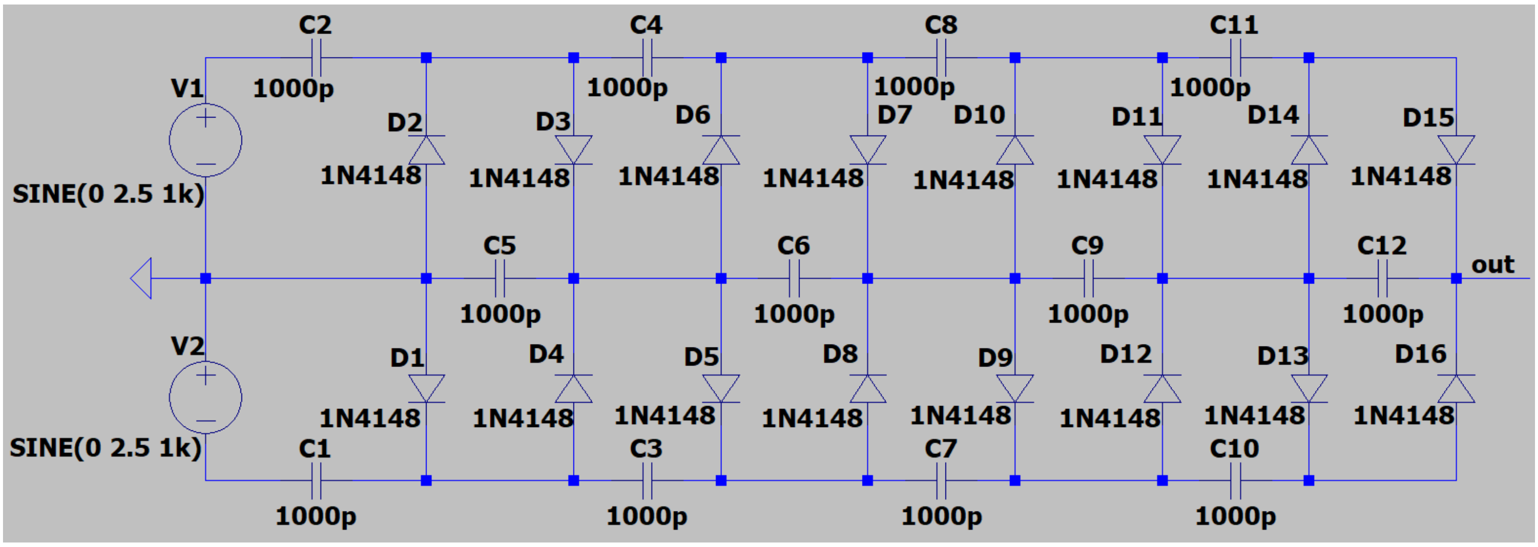

Figure 14: Four-Stage Full-Wave Cockcroft–Walton Generator

- Let us see the output without connecting the load.

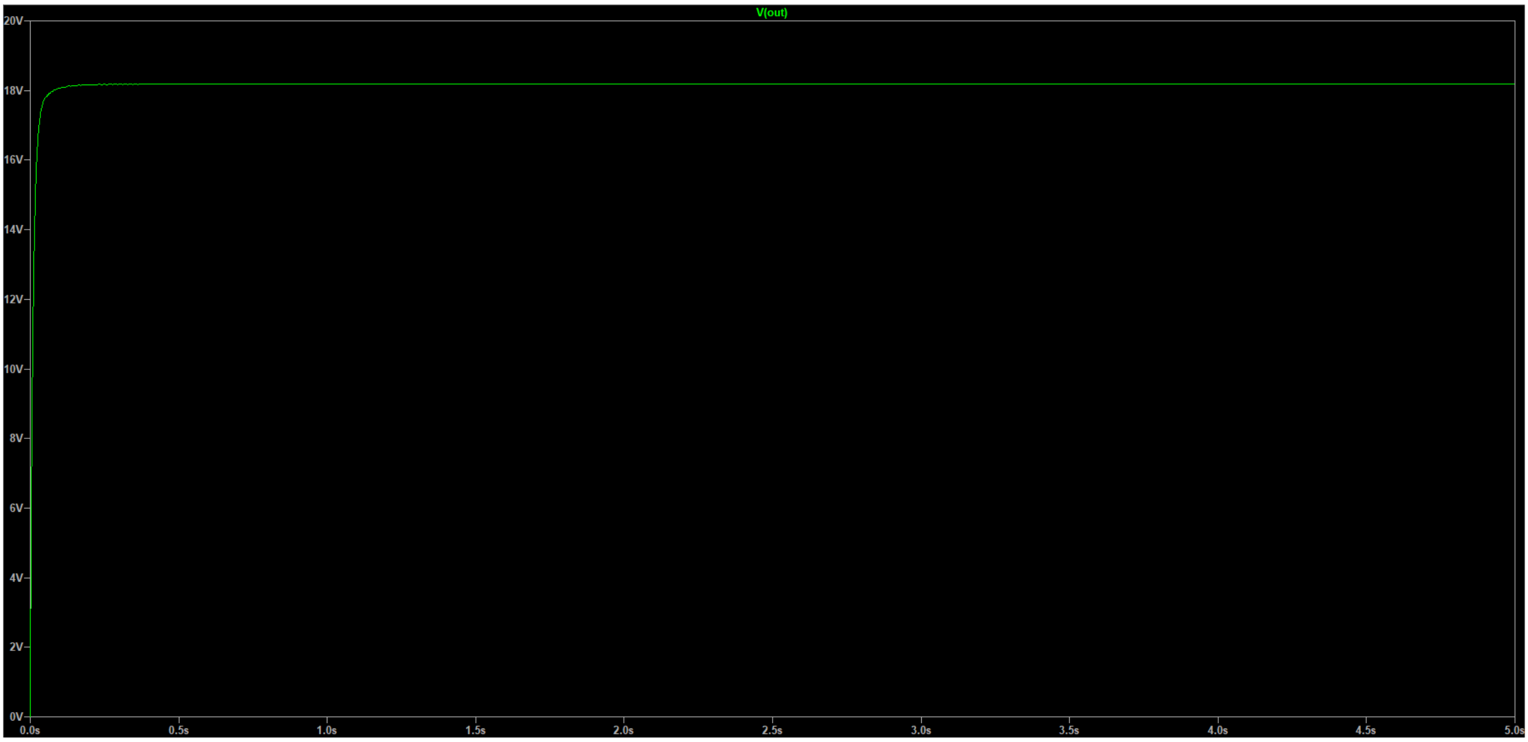

Figure 15: Output of the Four-Stage Full-Wave Cockcroft-Walton Generator

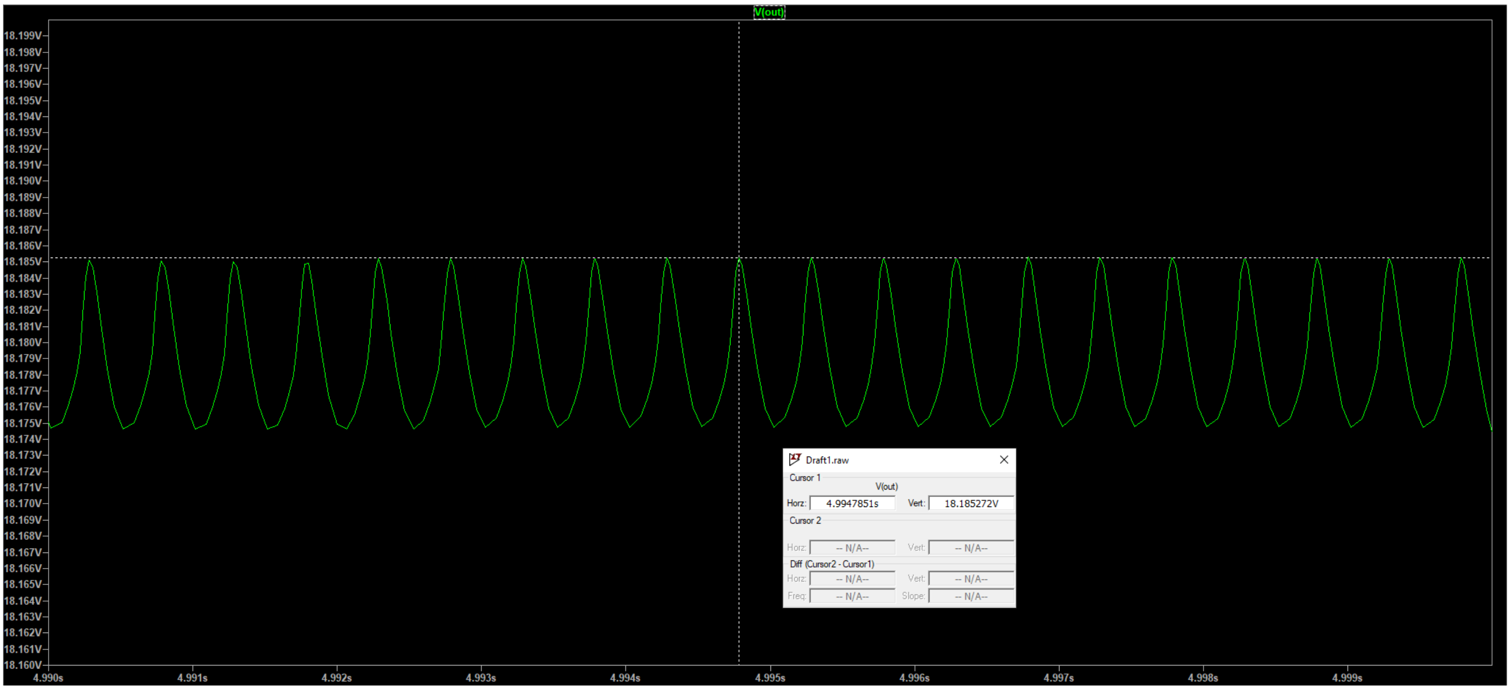

Figure 16: Zoomed Output of the Four-Stage Full-Wave Cockcroft-Walton Generator

- Let us check the output efficiency and percentage error.
  - $Number\ of\ Stages\ (N) = 4, V_{peak-to-peak} = 5\ volts$
  - $Expected\ Output = NV_{peak-to-peak} = 4 \times 5 = 20\ volts$
  - $Percentage\ Error = \frac{20-18.185272}{20} \times 100\% = 9.07364\%$
  - $Efficiency = \frac{18.185272}{20} \times 100\% = 90.92636\%$

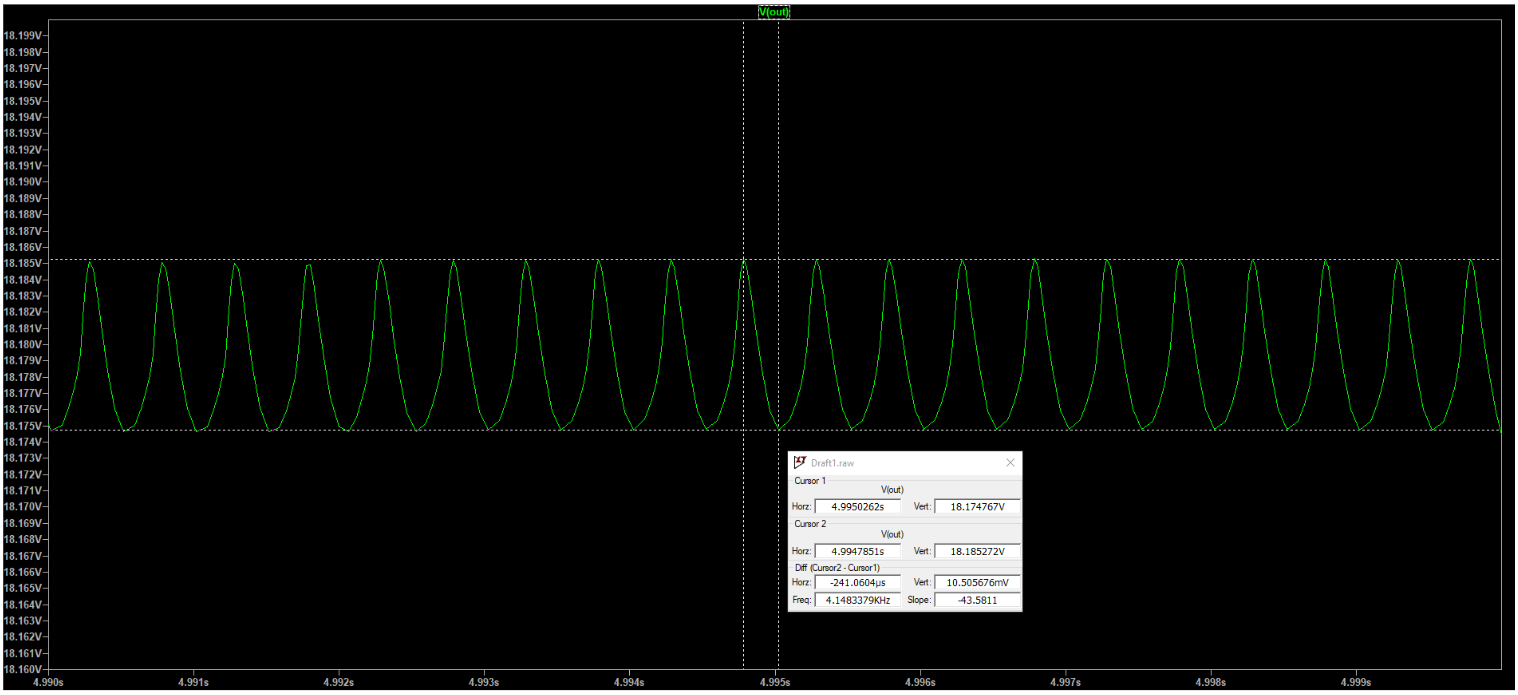

Figure 17: Ripple In the Improved Design

- Let us calculate the amount of ripple at the output without load resistor by looking the difference between peak points from LTSpice.
  - $Amount\ of\ Ripple = V_r = 18.185272 - 18.174767 = 10.505676\ mV$

- Now the 100-kΩ load resistor is connected to the output of the generator. The circuit diagram is given below.

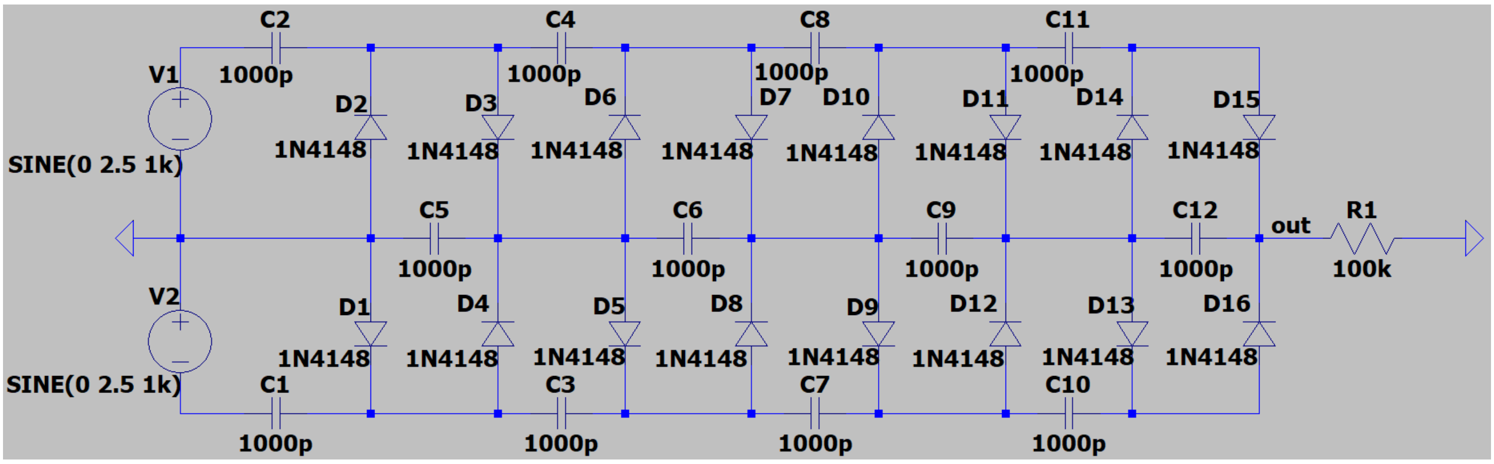

Figure 18: A Four-Stage Full-Wave Cockcroft–Walton Generator With Load

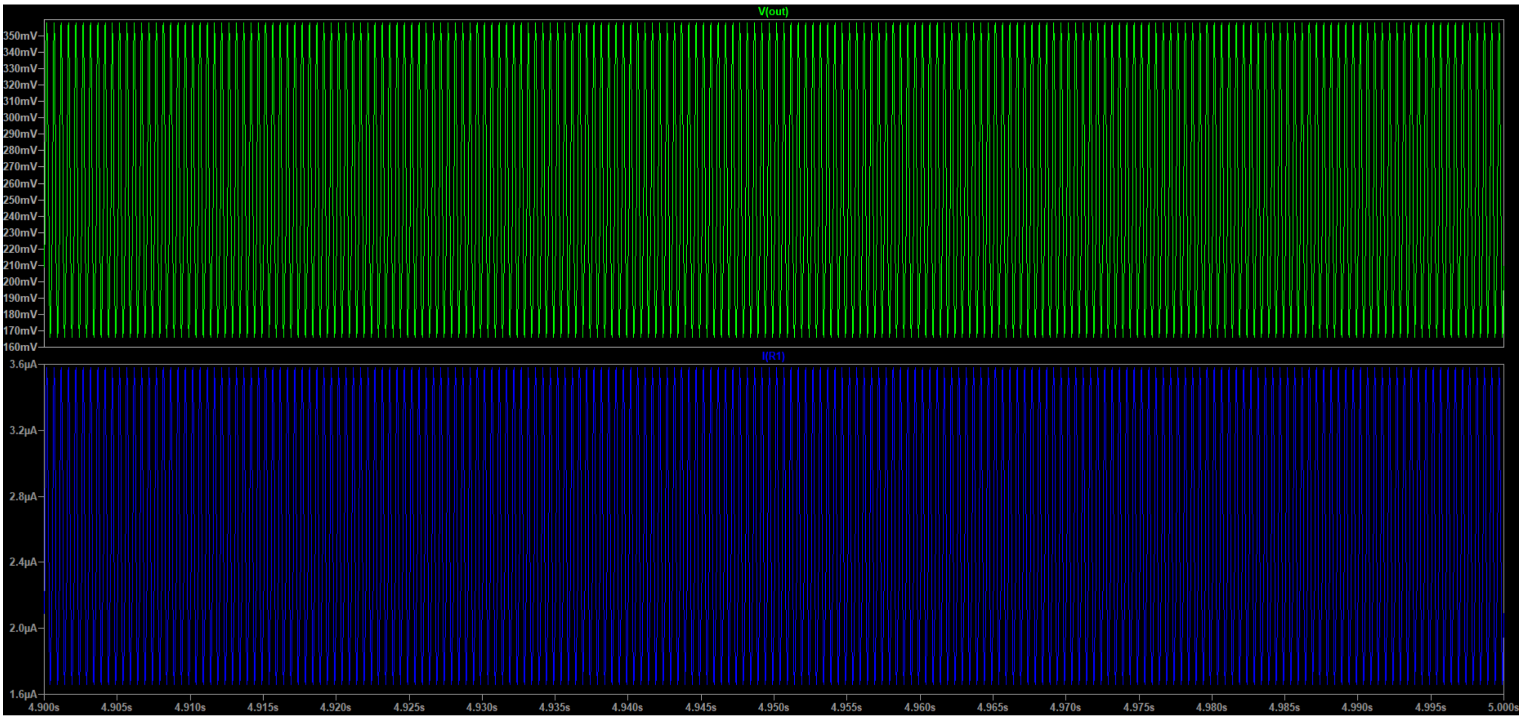

Figure 19: Output of Step 1 With Load

- The figure 19 shows the output with load. Changing half-wave to full-wave makes the ripples at the output less without load but as you can see from the figure it is not enough to stabilize the output when the load resistor exists. In that case the uncharging time of capacitors should be extended. The next step of the improvements includes this because we would like to have an stable output with load too.

Step 2: Adjust Values of Capacitors

- We know that the charging and uncharging times depends on the **time constant** (τ)**.**
  - $\tau = R \times C$
  - Here R is equivalent resistor, and the C is equivalent capacitance of circuit.
- In that case the **time constant** should have **greater value** because as the time constant becomes bigger, also the uncharging time of the capacitors extends.
- To make longer this time there is two choice:
  - We can increase the value of load resistor. But it will also make the output current less, and of course in the other day we may want to connect another device with another load resistor value. So that, changing the load resistor is not a good idea for now.
  - The second way is to **increase the capacitance value of the capacitors**.
- Now as a addition to the step 1, we will make the capacitance values greater than before.
  - Remember that we want the output to be in **DC form** and as close as possible to **20 volts**.
    - ➢ No need to mention but peak value of the source was 2.5 volts or peak-to-peak voltage was 5 volts and the number of stages was 4. From here we say the thoretically the output should be 20 volts using the given formula $V_{out} = NV_{peak-to-peak} = 5 \times 4 = 20\ volts$
- Most important part here is that if we do not want to connect a load, smaller capacitance values would be better because already system's energy consumption is very low to uncharge the capacitors fully. But in that case if we connect load the output is not satifying. On the other hand, if we are going to connect a load we need to adjust the values of capacitor, but in that case the charging and uncharging times will be extended. The extended charging time will occur a problem which is lower output without load (In the coming parts this problem will be solved by improvements). But the advantage of the increasing capacitances is that the output value will be in DC, and stable with load resistor.
- Capacitance values are adjusted to 100 μF decrease the ripple at the output when the load is connected.

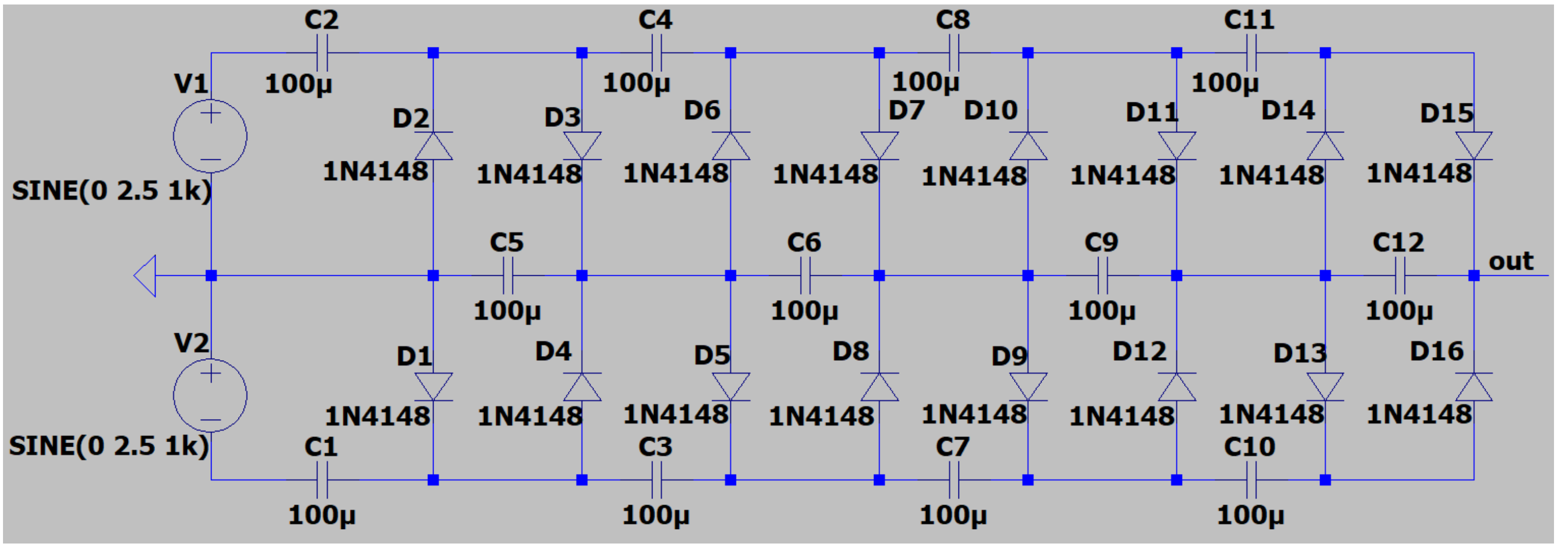

Figure 20: Capacitance Values Changed

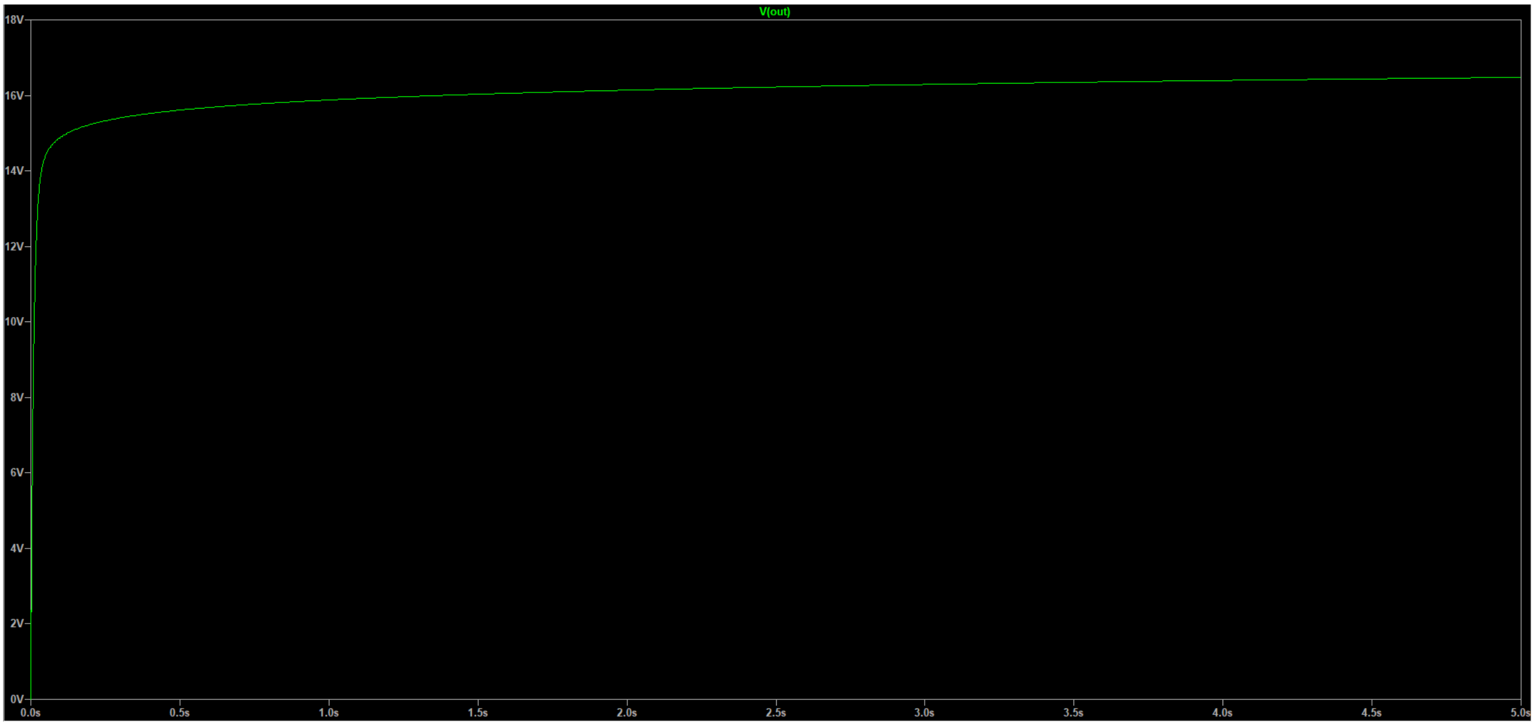

Figure 21: Output Without Load

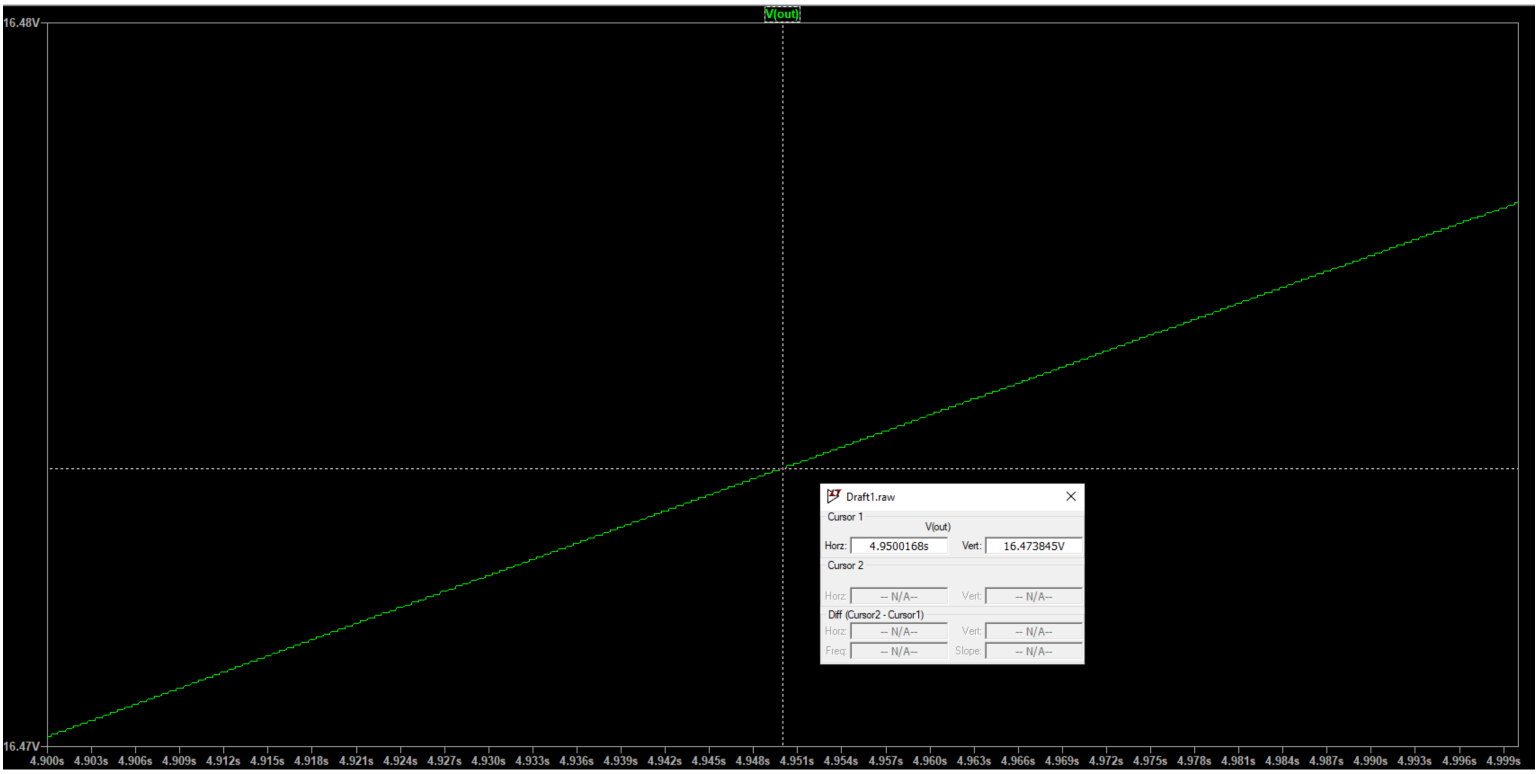

Figure 22: Zoomed Output Without Load

- As you can see from the figures numbered 21 and 22 because of the capacitance values of capacitors has been increased the charging time is extended and at the time interval we chose the capacitors are still charging.
- Already this improvement has been made to obtain DC output in case of load resistor existance. Before getting that point let us see what the output will be if we wait enough.

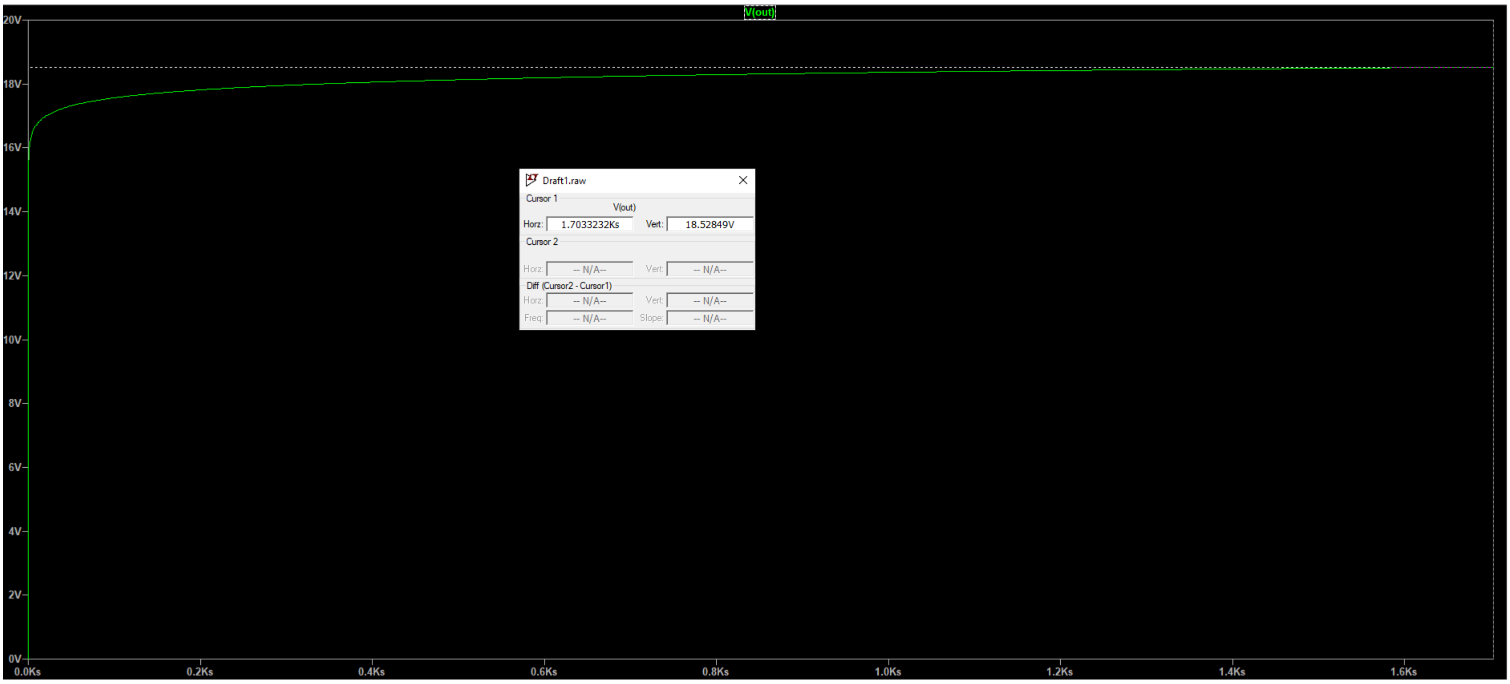

Figure 23: More Waited For Output

- As the figure 23 shows us more we wait, more voltage at the output occurs (Pay attention to the time scale). In other words, as the time converges to the infinity, the voltage at the output converges to the 20 volts (But do not forget the loss on the diodes).
- Now the load resistor with 100 kΩ will be connected to the output.

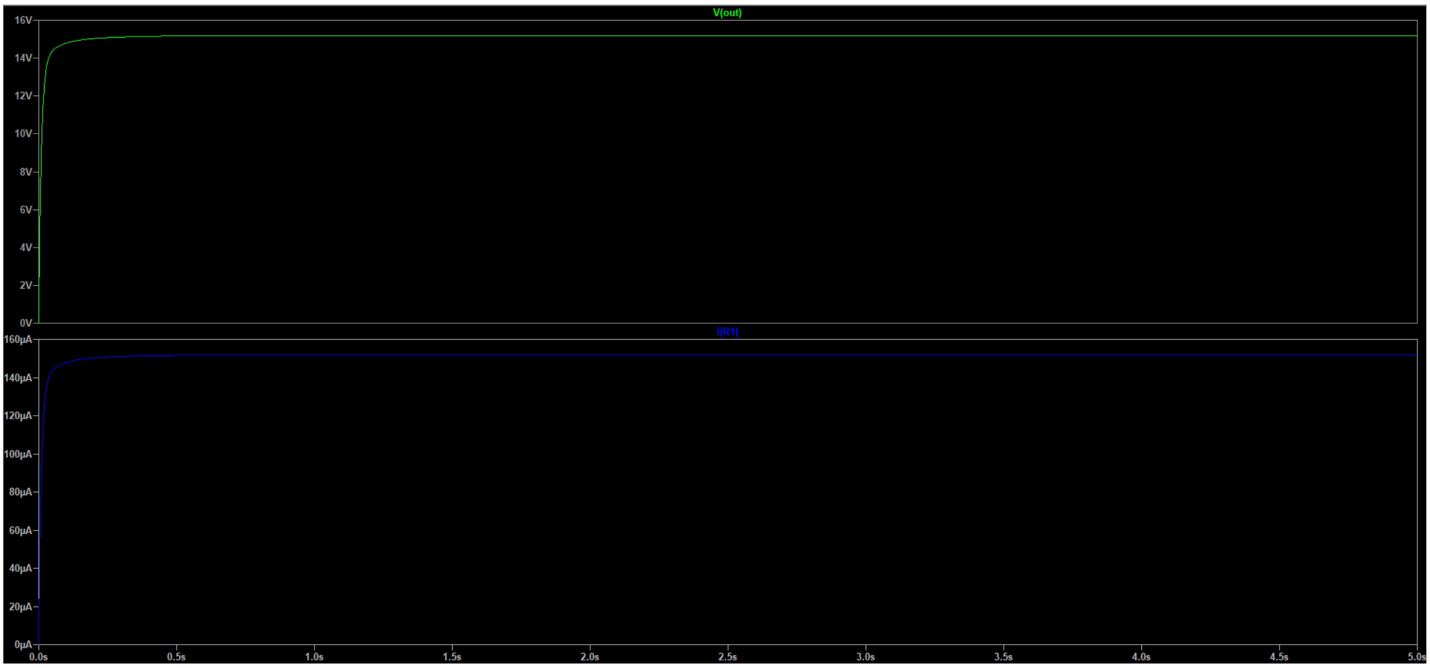

Figure 24: Output With Load Resistor

- The figure 24 shows us the output voltage and the current passing through the 100-kΩ resistor. Please notice that it clearly DC output and there is no noticeable ripple, thanks to the higher capacitance values. If we wait long enough there will be a loss on the diodes but the output will converge to the 20 volts.
- The only penalty of this improvement is obvious which is we need to wait so long to get higher output voltages. In the next step of improvements this problem will be solved.

Step 3: Change Diodes With Schottky Diode

- One reason the problem occurred in step 2 is the high-frequency AC signal source we use. Remember that the source has the f**requency of 1 kHz**, and the diode used in the design with the name **1N4148** needs around **0.65 volts** to be **forward biased**. This is a huge value for high frequencies. Therefore, the model of the diodes needs to be changed with another type of diode with faster respond level. At that moment diode type called Schottky diode is the best choice.
- Schottky diodes are the fastest diodes in switching process and respond levels. Usually **0.15 volts – 0.45 volts** is needed to be **forward biased**. So that, usage of Schottky diode in the circuit will increase the output level because the capacitors will be start to charge themselves at the lower voltage levels instead of 0.65 volts.
- Let us change all the diodes with the **BAT54 Schottky diode**. The datasheets of the components will be given at the end of the document.

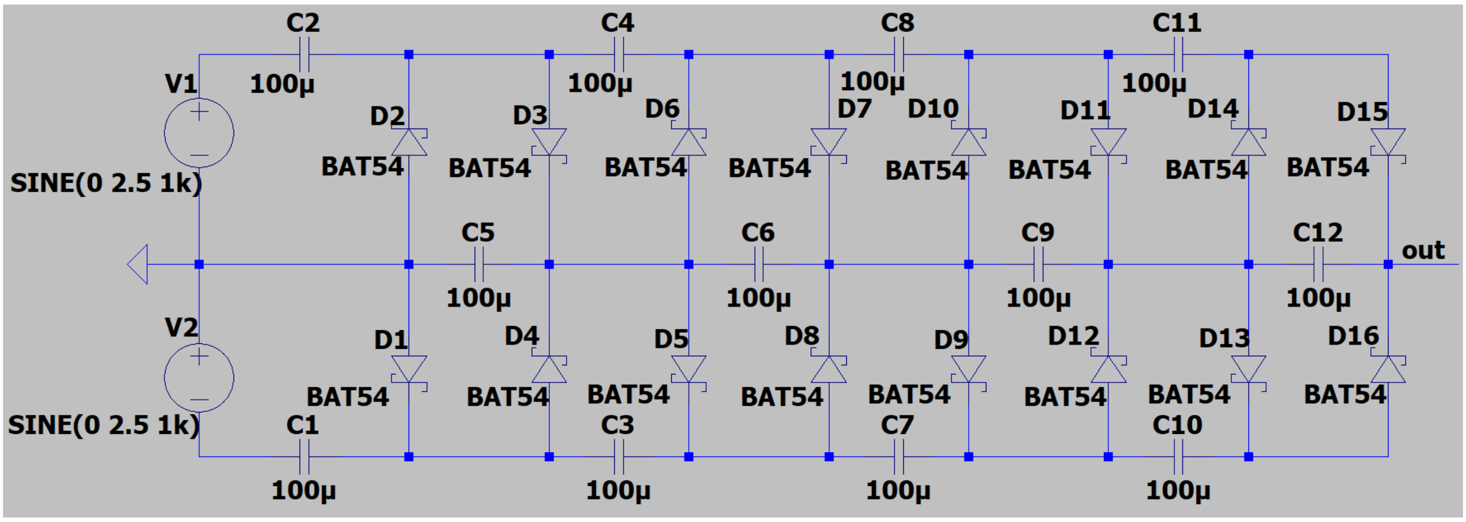

Figure 25: Circuit Scheme After Step 2

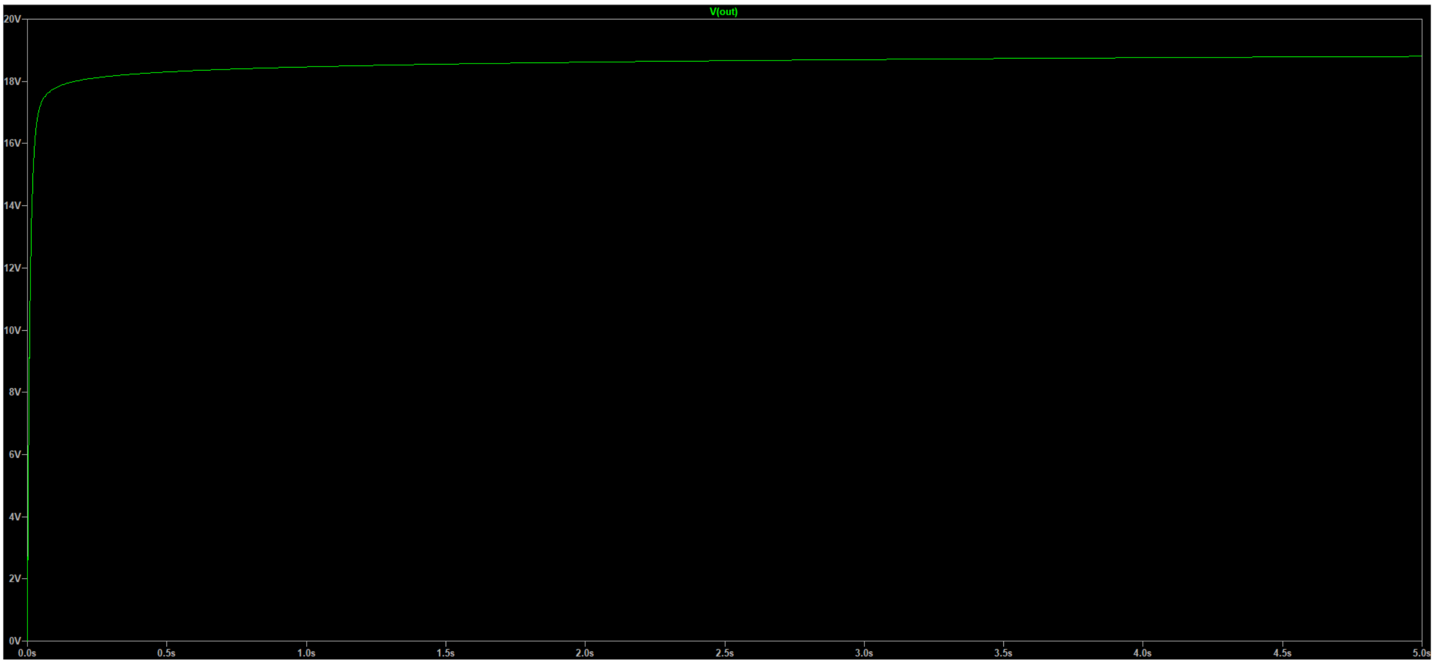

Figure 26: Output Without Load

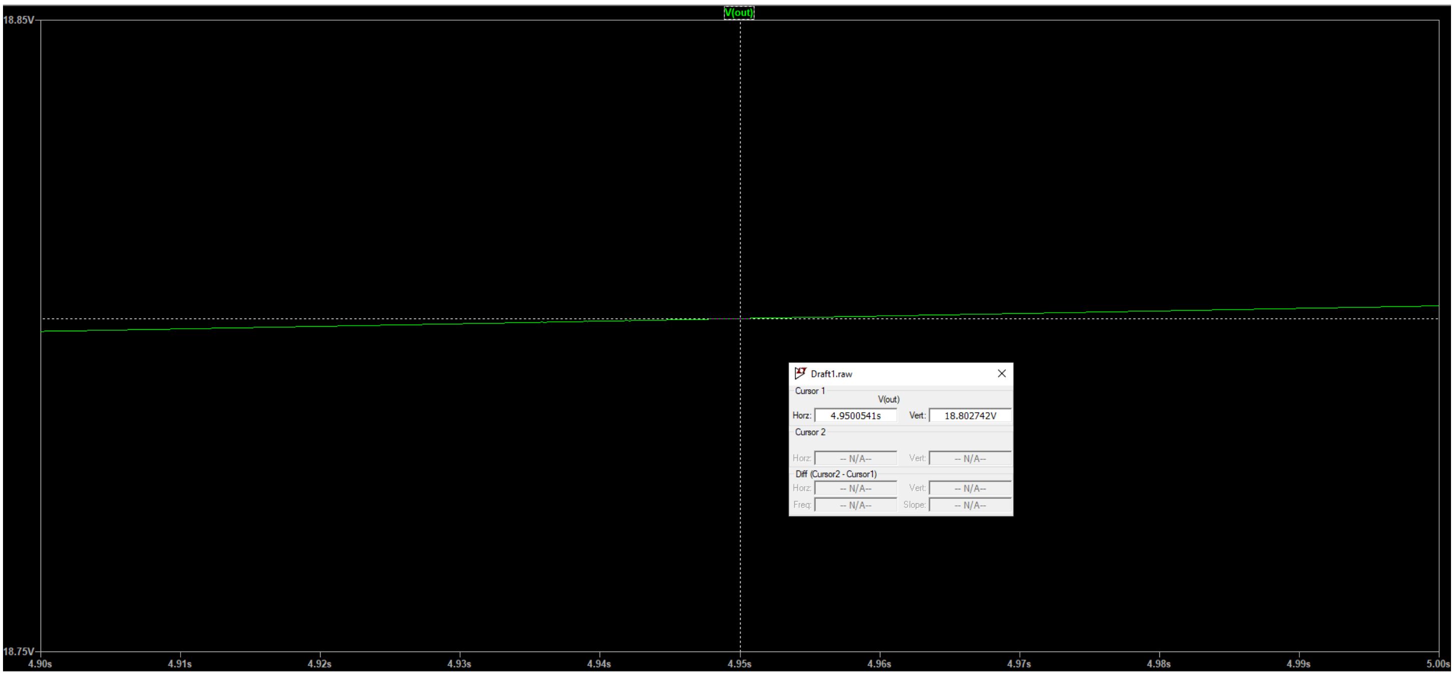

Figure 27: Zoomed Output Without Load

- Notice that, the capacitors are still charging at the moment we test in the figure 27 but let us compare the effect of improvement with before.
  - The figure 22 shows the result at the output before this improvement. In that figure, at the time 4.95 s we have output of **16.473845 volts.**
  - Now take a look to the figure 27 which shows the output after the improvement. In the figure, at the time 4.95 s we have output of **18.802742 volts**.
- So, it is seen that the diode selection has a huge role on the result. The diodes with fast-respond levels are better in this design.
- Now let us connect a load of 100 kΩ resistor to the output.

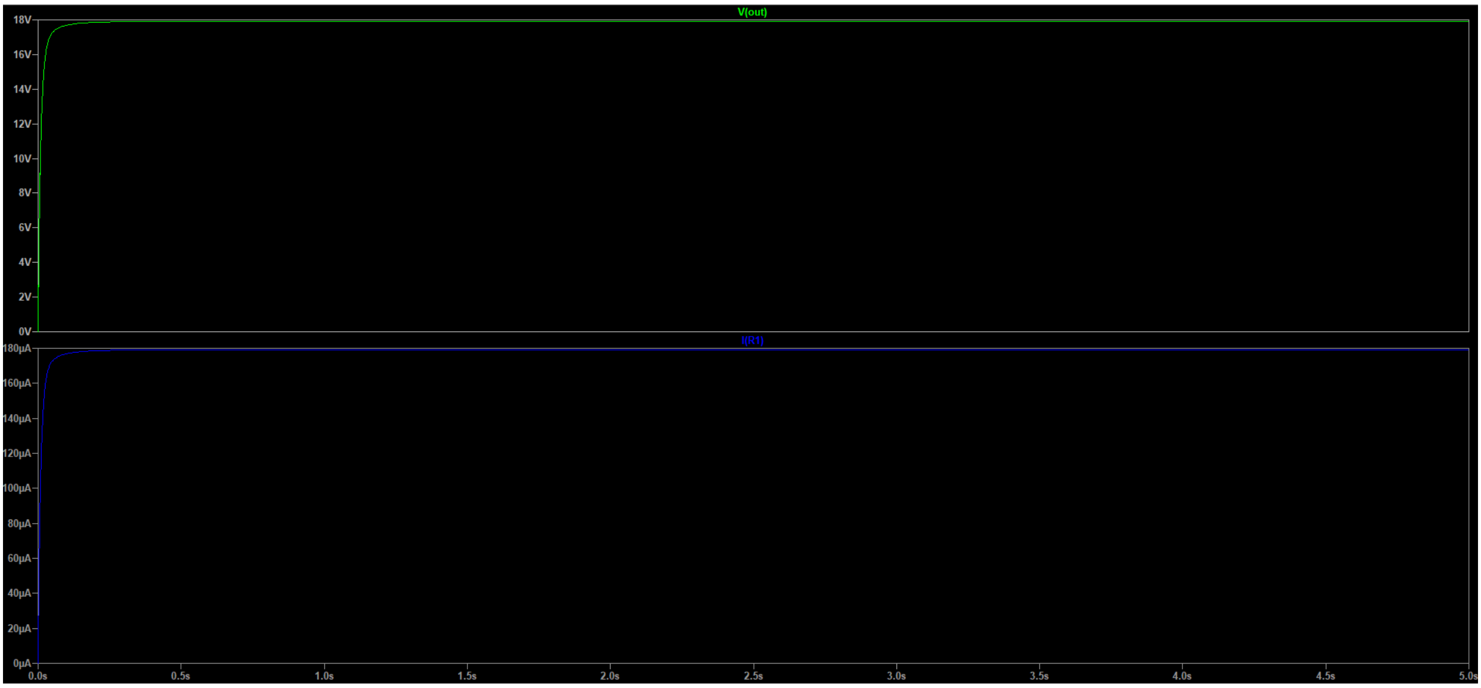

Figure 28: Output With Load

- The figure numbered 28 shows the output of the generator with 100-kΩ load resistor. The best side of this improvement is that even if we connect a resistor to the output the voltage at the node called **out** remains almost the same. But before this improvement we saw that the voltage at **out** node is less in case of load existance.
    - To compare the results please look at the figures numbered 24 and 28.

4- Comparison Between Reference Circuit and Improved Circuit

- In this part the circuit will be tested under different conditions and the results will be interpreted. Shortly, this part includes the comparison between reference design and my improved design.

Circuit Scheme Design Differences

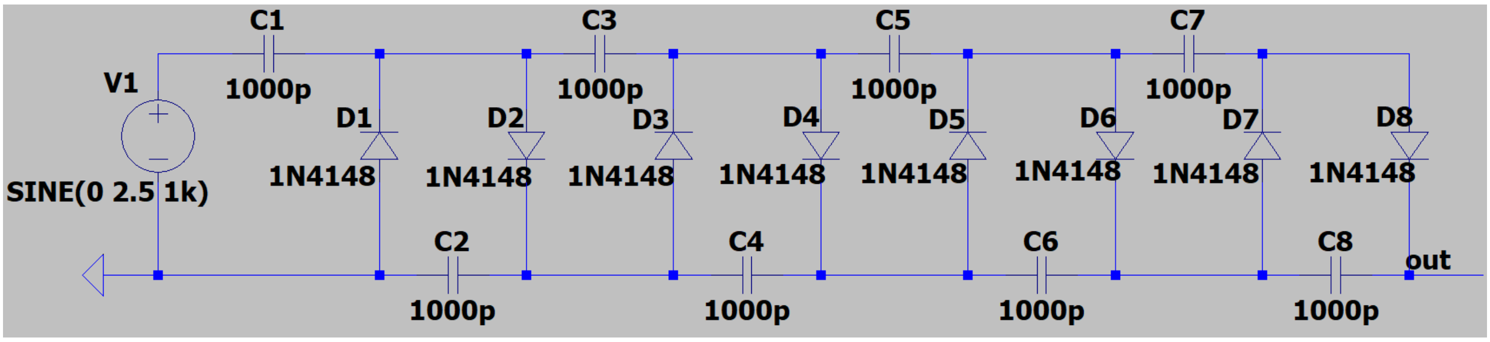

Figure 29: Reference Circuit Design

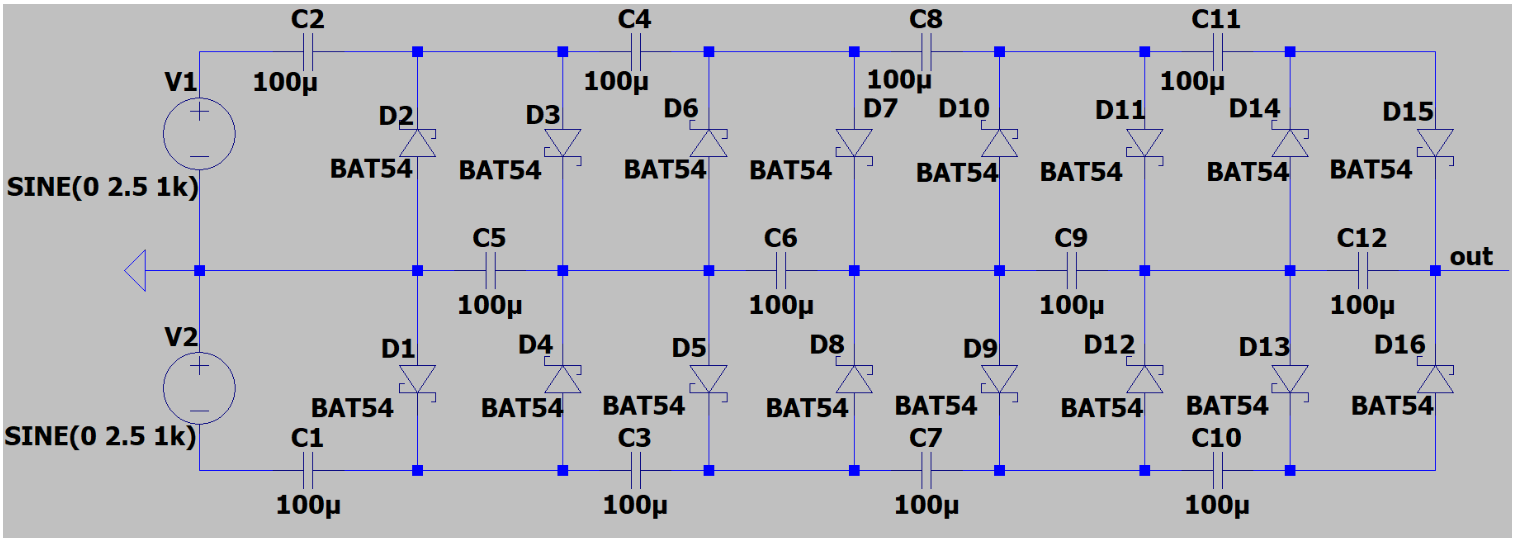

Figure 30: Improved Circuit Design

Improvement Area	*Reference Design*	*Improved Design*
Charging	Half-Wave Voltage Multipler	Full-Wave Voltage Multipler
Capacitor	1000 pF	100 μF
Diode	Normal Diode: 1N4148	Schottky Diode: BAT54

Table 1: Main Changes

Test 1: Test the Circuit Without Any Load Resistor

- In this section the circuits will be remain the same, that is, there is **no load resistor** at the node called **out**. The results will be compared using percentages at the end of the LTSpice results. Note that capacitors are still charging but we will consider the two designs **at the same time intervals** without waiting the capacitors charge themselves fully.

Figure 31: Output of Reference Design Without Load

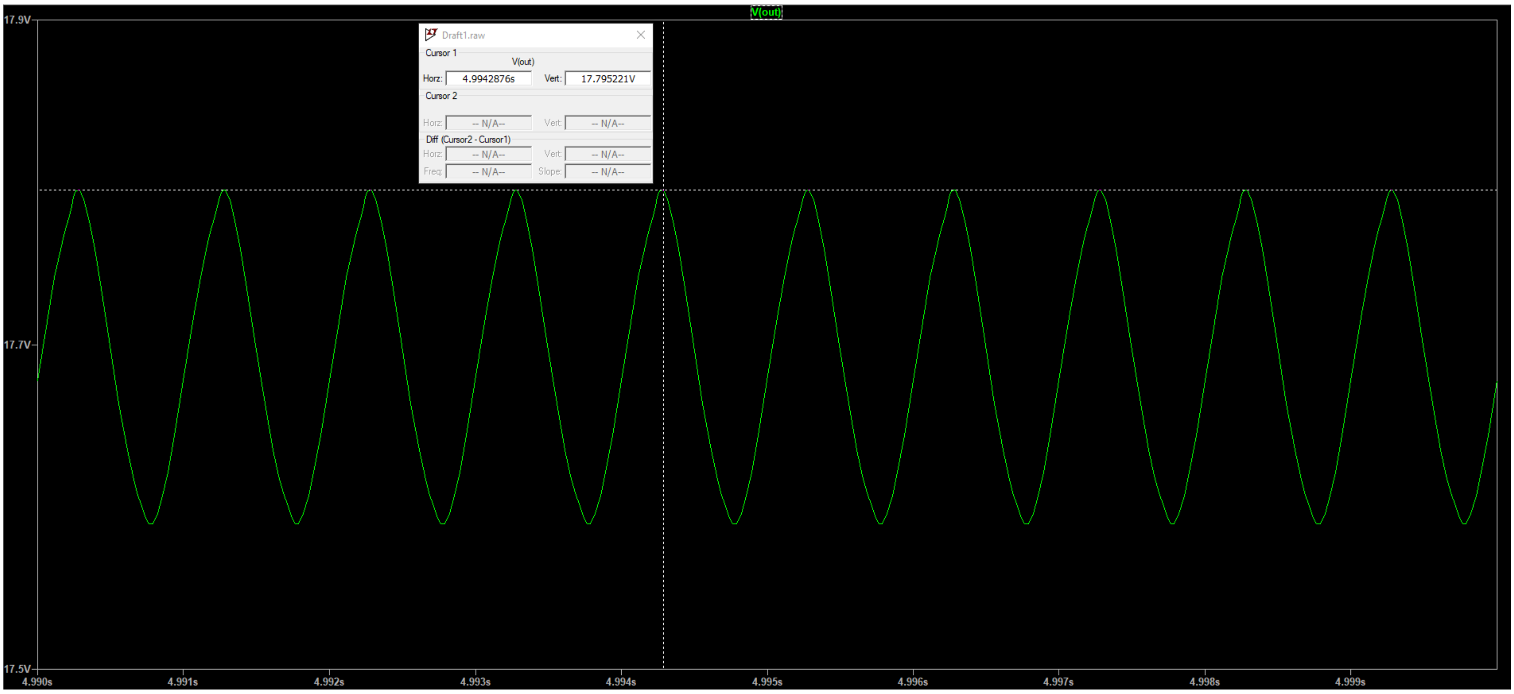

Figure 32: Zoomed Output of Reference Design Without Load

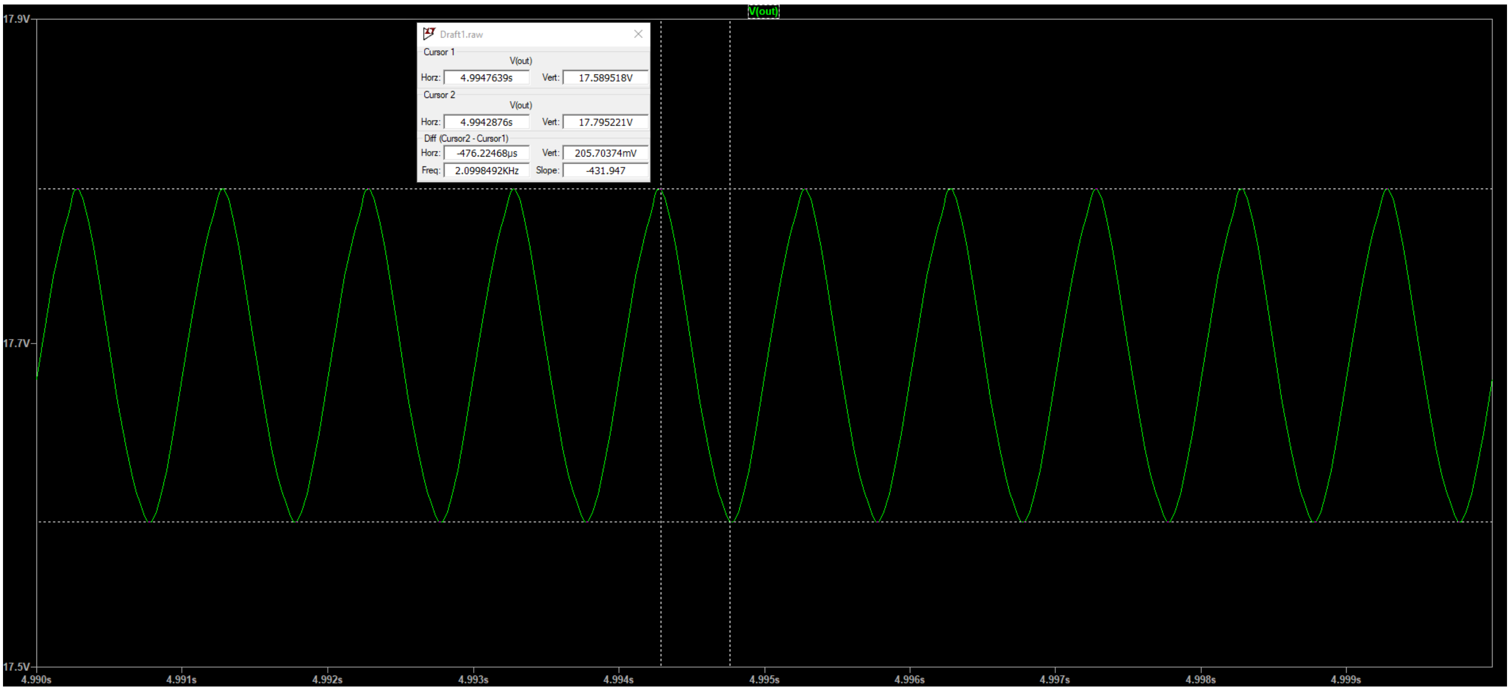

Figure 33: Ripple Calculation of Reference Design Without Load

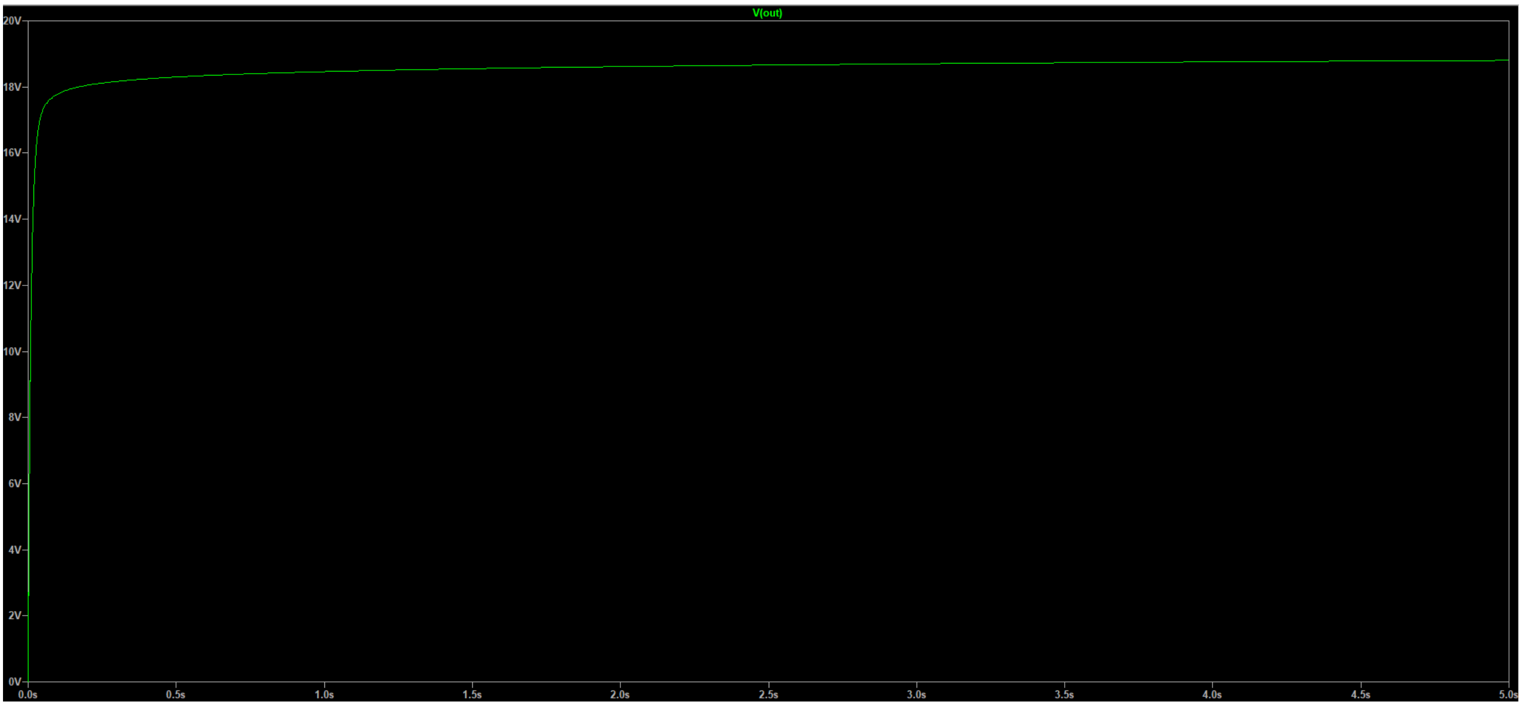

Figure 34: Output of the Improved Design Without Load

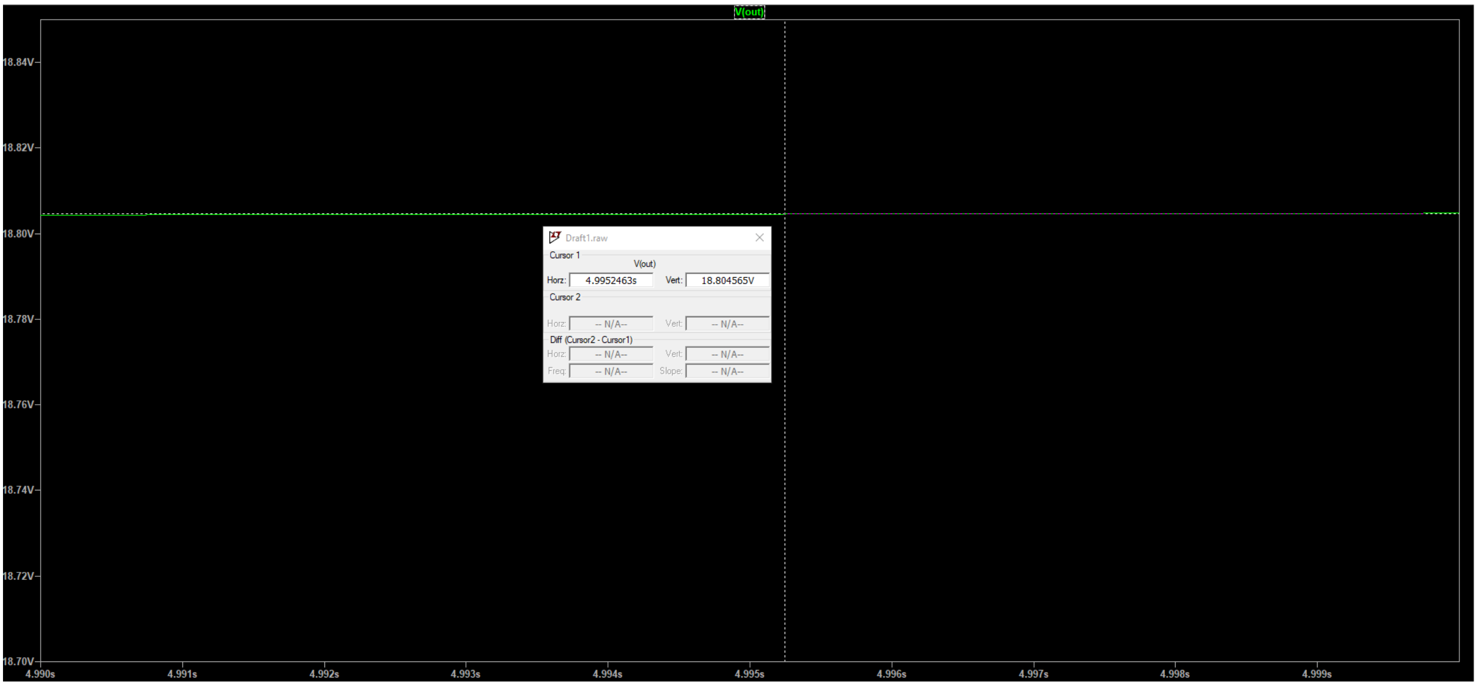

Figure 35: Zoomed Output of the Improved Design Without Load

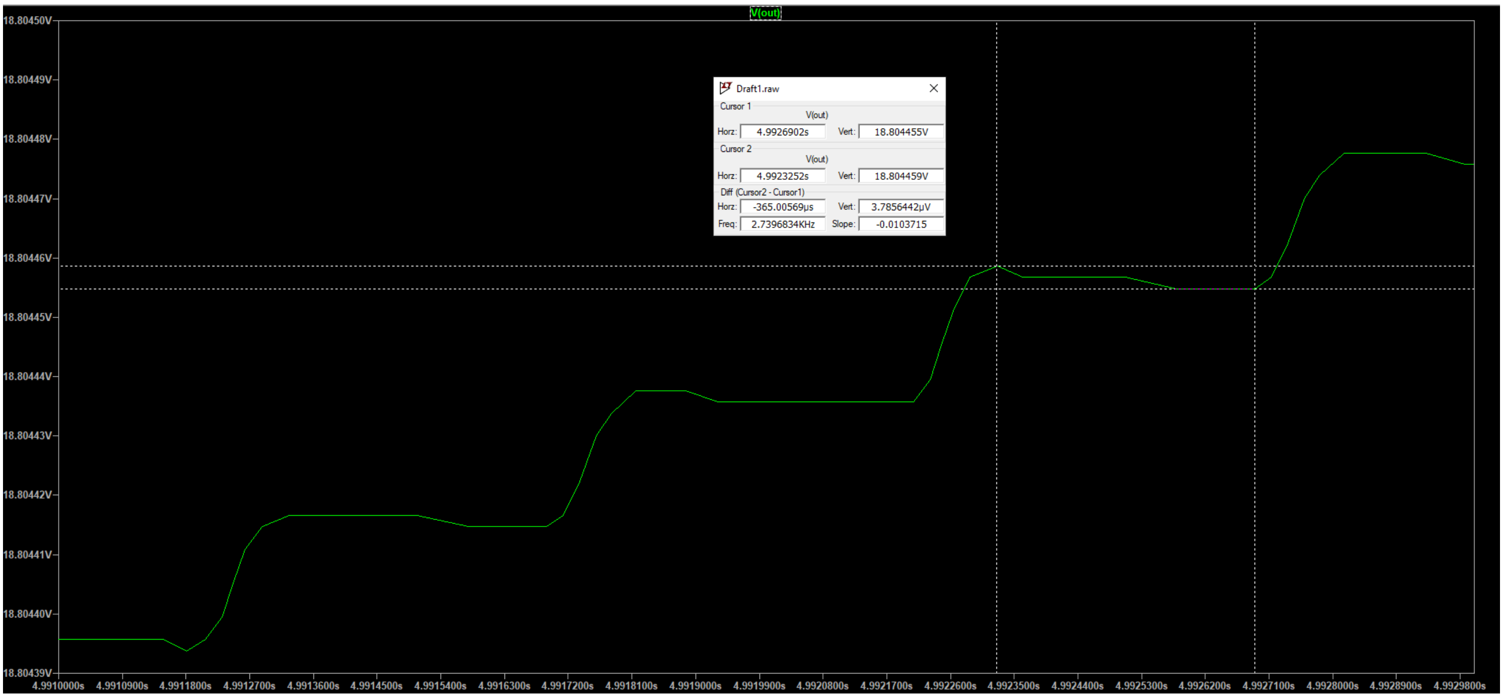

Figure 36: Ripple Calculation of Improved Design Without Load

- Note that voltage goes upward in the figure 36 which is related to the improved design because the capacitors are still charging.

- The data in the table given below are related to the same time interval which is between t = 4.99s and t = 5s.

	Reference Design	Improved Design	Related Figures
Output Form	Close to DC	DC	31 and 34
Output Voltage	17.795221 Volts (max) and 17.589518 Volts (min)	18.804565 Volts	33 and 35
Percentage Error According to the Expected Output (20 Volts)	11.023895% (Calculated using max value)	5.977175%	-
Ripple Amount (V_r) (Calculated by LTSpice Based On Maximum and Minimum Data)	205.70374 mV	3.7856442 μV	33 and 36

Table 2: Results of Test 1

- It is clearly seen that improvements which is made on the circuit affect the output in a positive way, and the output get closer to the voltage level we desire.

Test 2: Test the Output With Higher Input Voltage and Without Load

- In this test section we will consider the circuit with higher input voltage levels and without load resistor to see how the error rates changes with the input voltage. Shortly, we desire to observe the relationship between percentage error and input voltage.
- The input voltage has **peak value** of **100 volts** or **peak-to-peak value** of **200 volts**. The **frequency** is again **1 kHz**, and the **phase angle** of **0 radians**. There is no load resistor.The number of stages is **N = 4**.
- Using the formula mentioned before the output is expected to be **800 volts**.
    - $V_{expected} = NV_{peak-to-peak} = 4 \times 200 = 800\ volts$

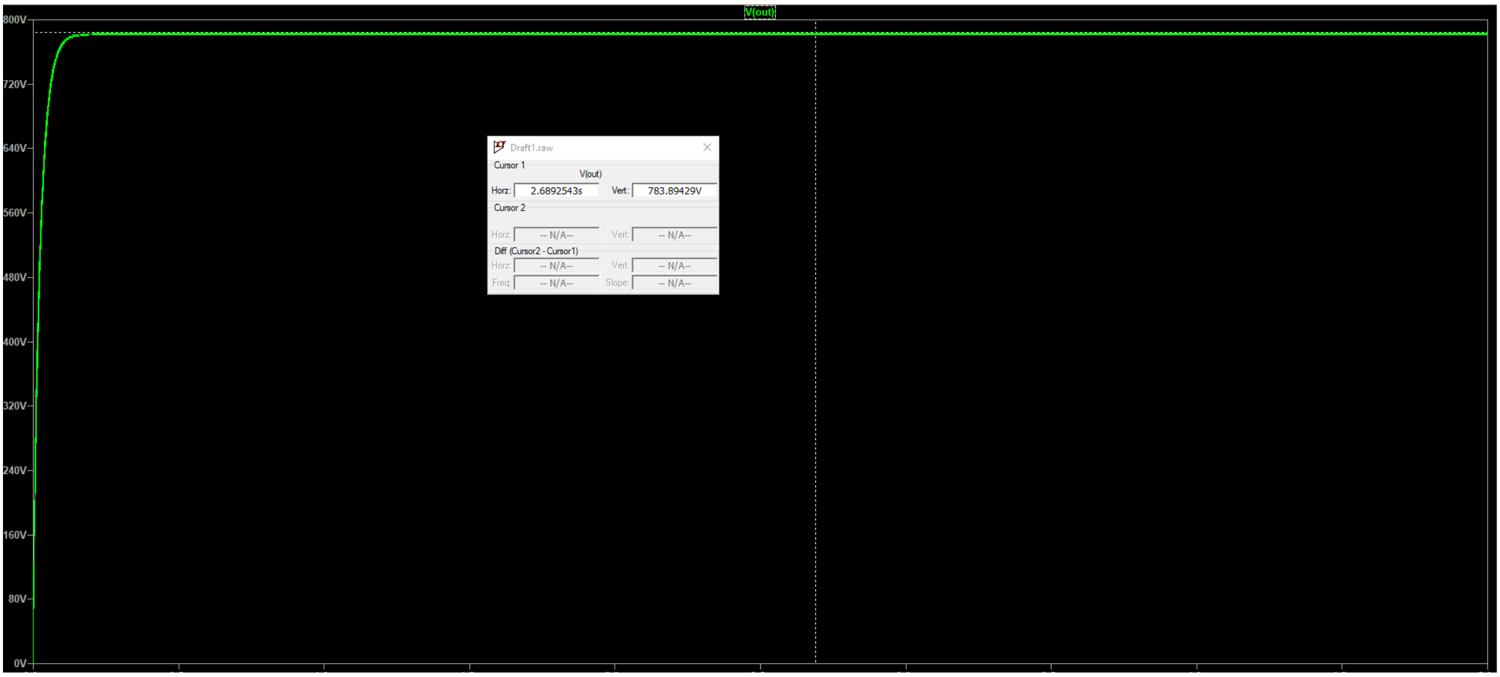

Figure 37: Output of Reference Design

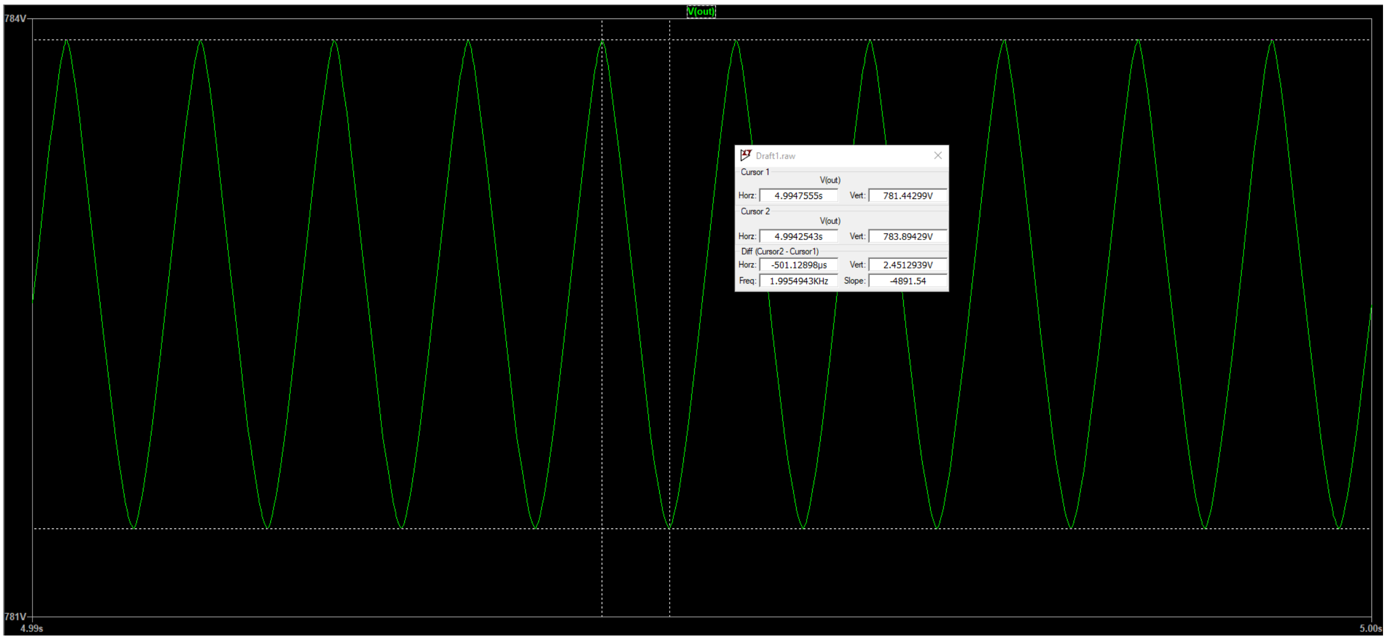

Figure 38: Zoomed Output of Reference Design

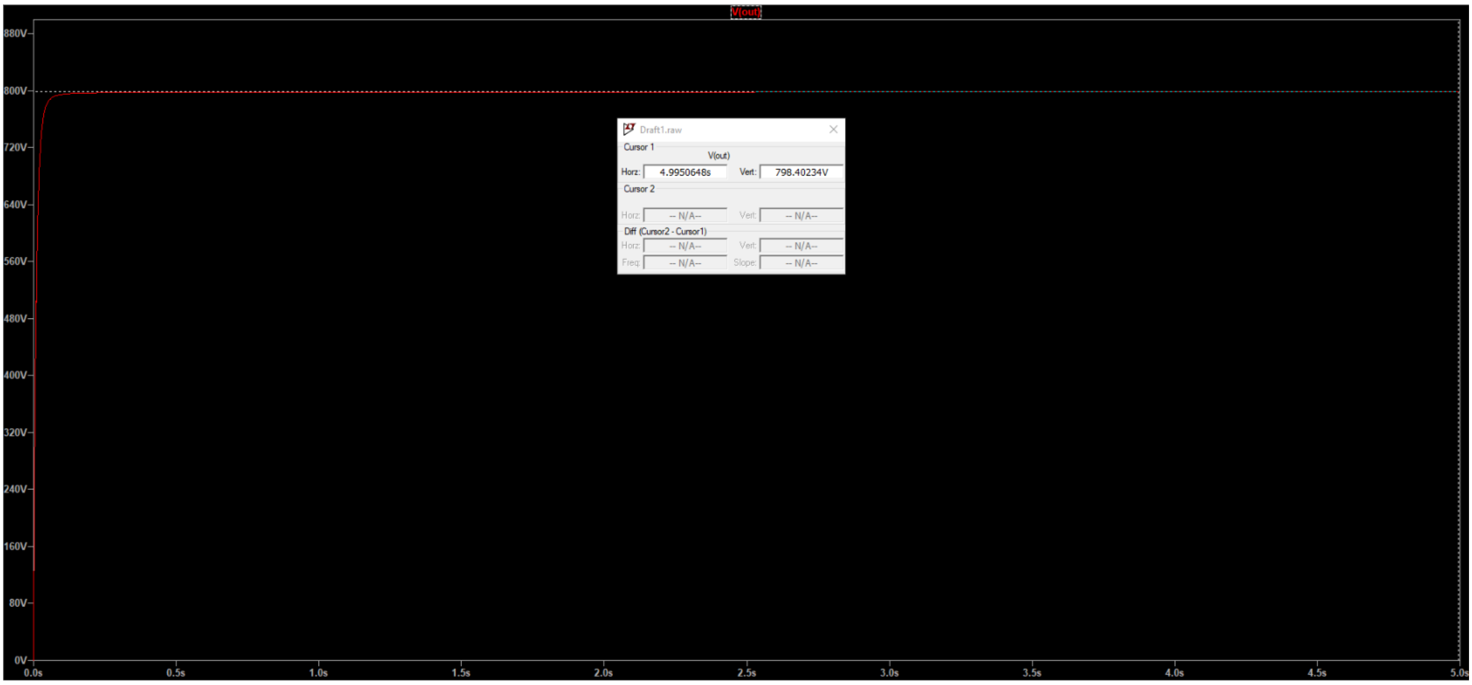

Figure 39: Output of Improved Design

- Samples are taken from the interval t = 4.99 s and t = 5 s.
- As you can see at the output of the reference design there is a ripple with the value of **2.45 volts** which cannot be negligible, and this ripple causes error in the end. But in the improved design as you can see from the figure numbered 39 the output is in the DC form.

	Reference Design	Improved Design	Related Figures
Output Form	Close to DC But With Ripples	DC	37 and 39
Output Voltage	783.89429 Volts (max) and 781.44299 Volts (min)	798.40234 Volts	38 and 39
Percentage Error According to the Expected Output (800 Volts)	2.01321375% (Calculated using max value.)	0.1997075%	-

Table 3: Results of Test 2

- This test shows us as we increase the input voltage, we get less percentage error in the output. With the input given in the test procedure the error of the improved design is very close to the zero.

Test 3: Test the Output With Low-Valued Load Resistor

- In this test the designs will be compared with the existence of high current consumption at the output due to low-valued resistor.
- The **load resistor** which is connected to the output node called **out** has the value of **10kΩ**. The input has **peak value of 2.5 volts** and **peak-to-peak value of 5 volts** again with **1 kHz frequency** and **0 radians phase angle**.
- Samples are taken from the interval t = 4.99 s and t = 5 s.

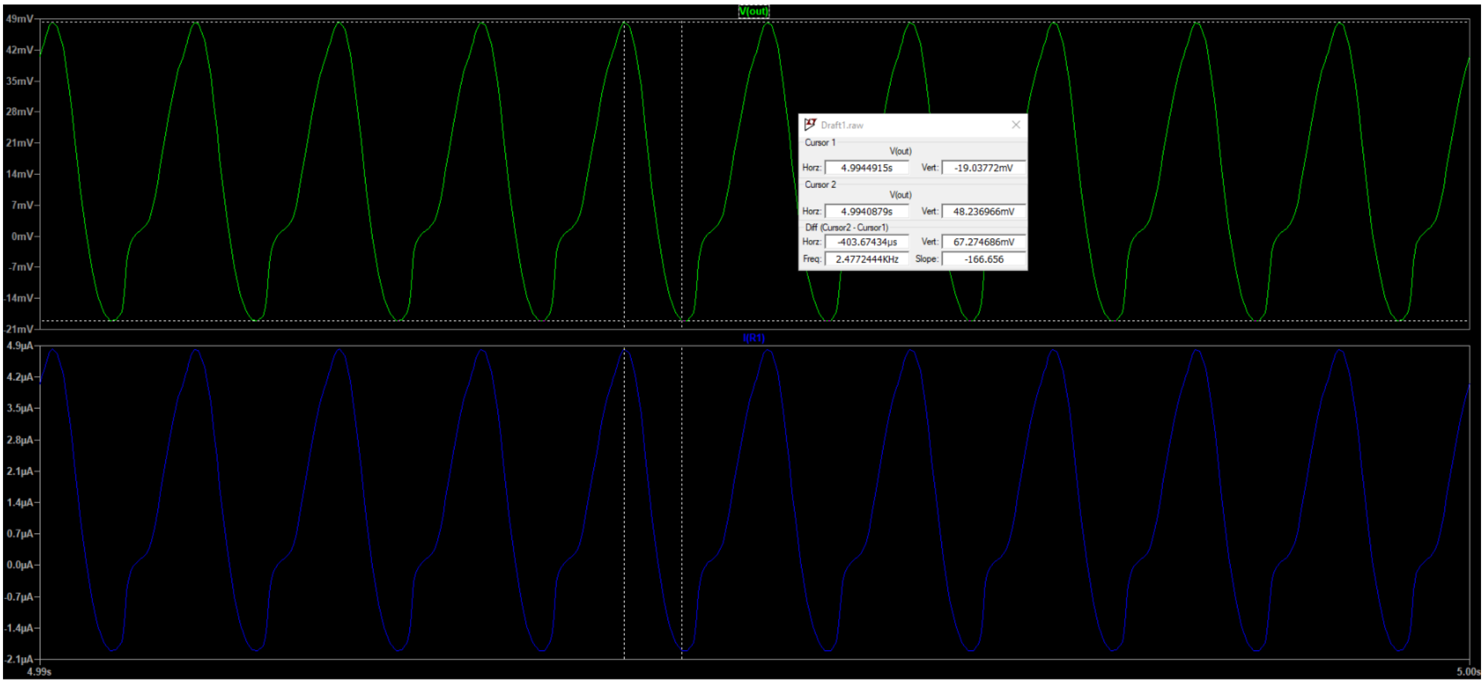

Figure 40: Output of Reference With Load

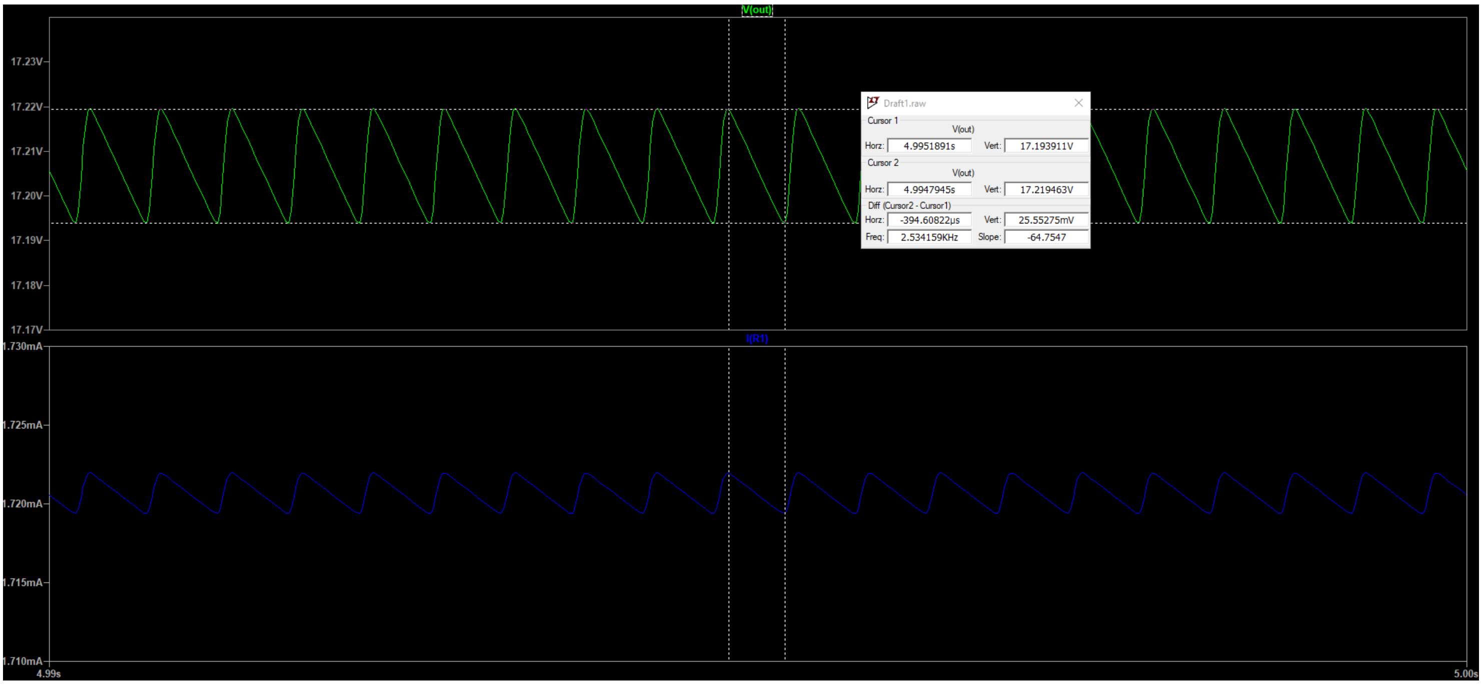

Figure 41: Output of Improved Design With Load

	Reference Design	Improved Design	Related Figures
Output Form	Not Even Closer to DC	DC With Very Small Ripples	40 and 41
Output Voltage	48.236966 mVolts (max) and -19.03772 mVolts (min)	17.219463 Volts (max) and 17.193911 Volts (min)	40 and 41
Percentage Error According to the Expected Output (20 Volts)	99.75881517% (Calculated using max value)	13.902685%(Calculated using max value)	-
Ripple Amount (V_r) (Calculated by LTSpice Based On Maximum and Minimum Data)	67.274686 mVolts	25.55275 mVolts	40 and 41

Table 4: Results of Test 3

- As you can see from the data included in the table there is a huge difference between the reference design and improved design.
- The reference design is too sensitive to the load resistor connections but the design I improved can still work efficiently and effectively with load resistor. With 10-kΩ load resistor efficiency percentages are as follows:
  - Reference Design ➔ 0.24118483%
  - Improved Design ➔ 86.097315%

Test 4: Test the Output With Higher Input Voltage and With Low-Valued Resistor

- In this test procedure:
  - Voltage Sources have **200 volts peak-to-peak voltage**, **1 kHz frequency**, **0 radian phase angle**.
  - Load resistor with the value of **10-kΩ**.
  - Samples are taken from the interval t = 4.99 s and t = 5 s.
  - Remember that Number of stages is **N = 4**. ➔ $V_{expected} = 800\ volts$

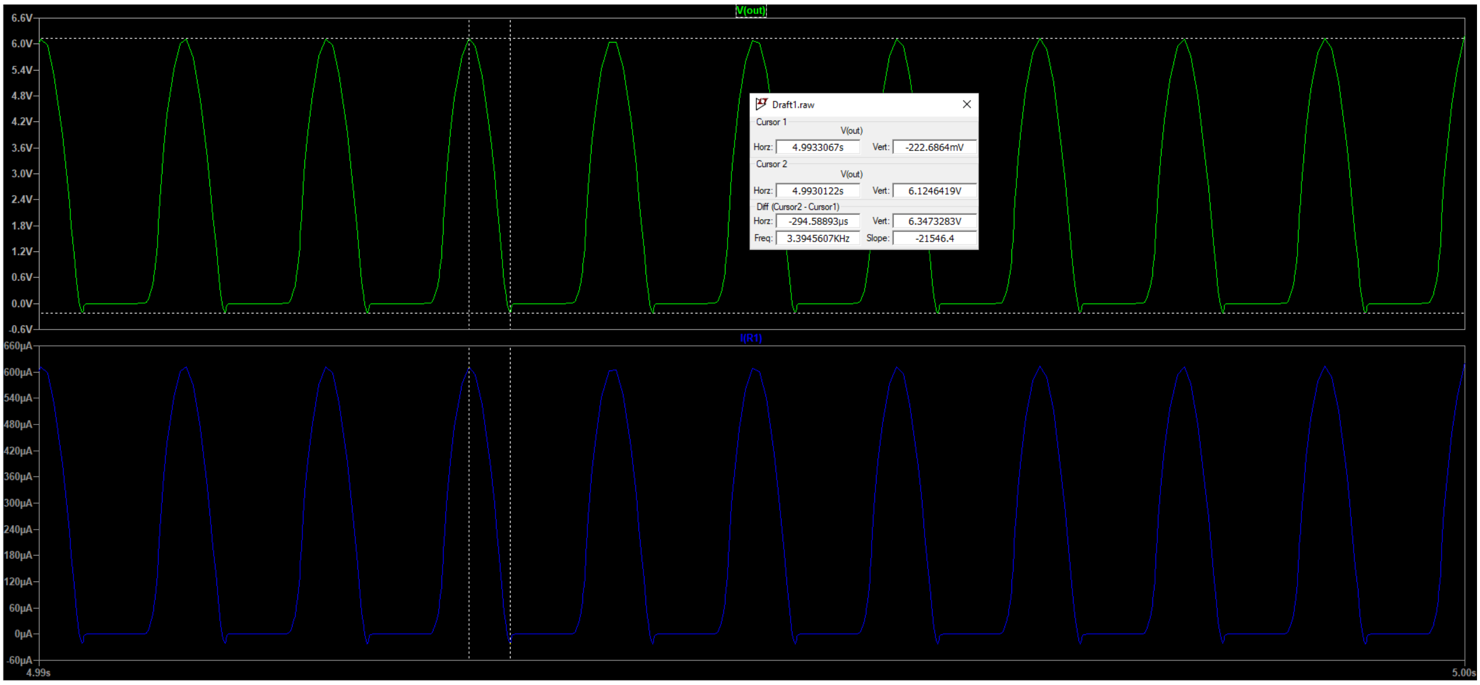

Figure 42: Output of Reference Design

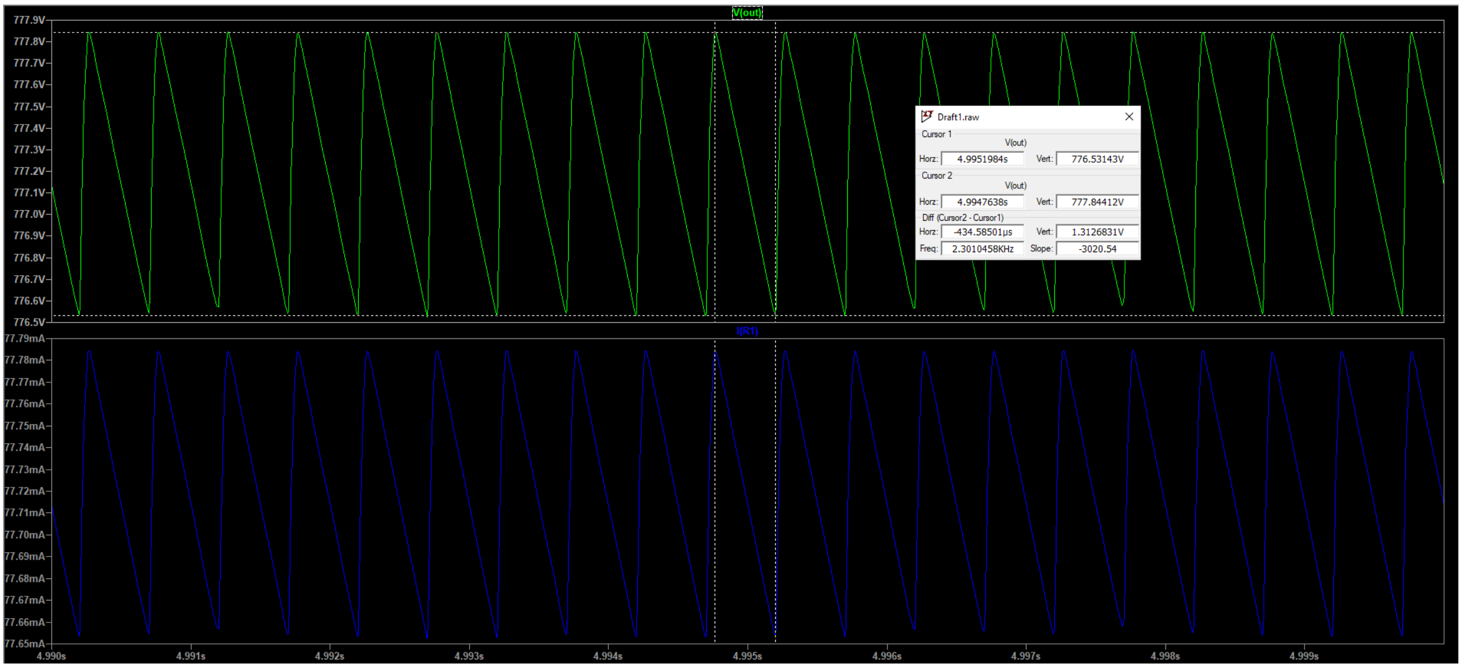

Figure 43: Output of Reference Design

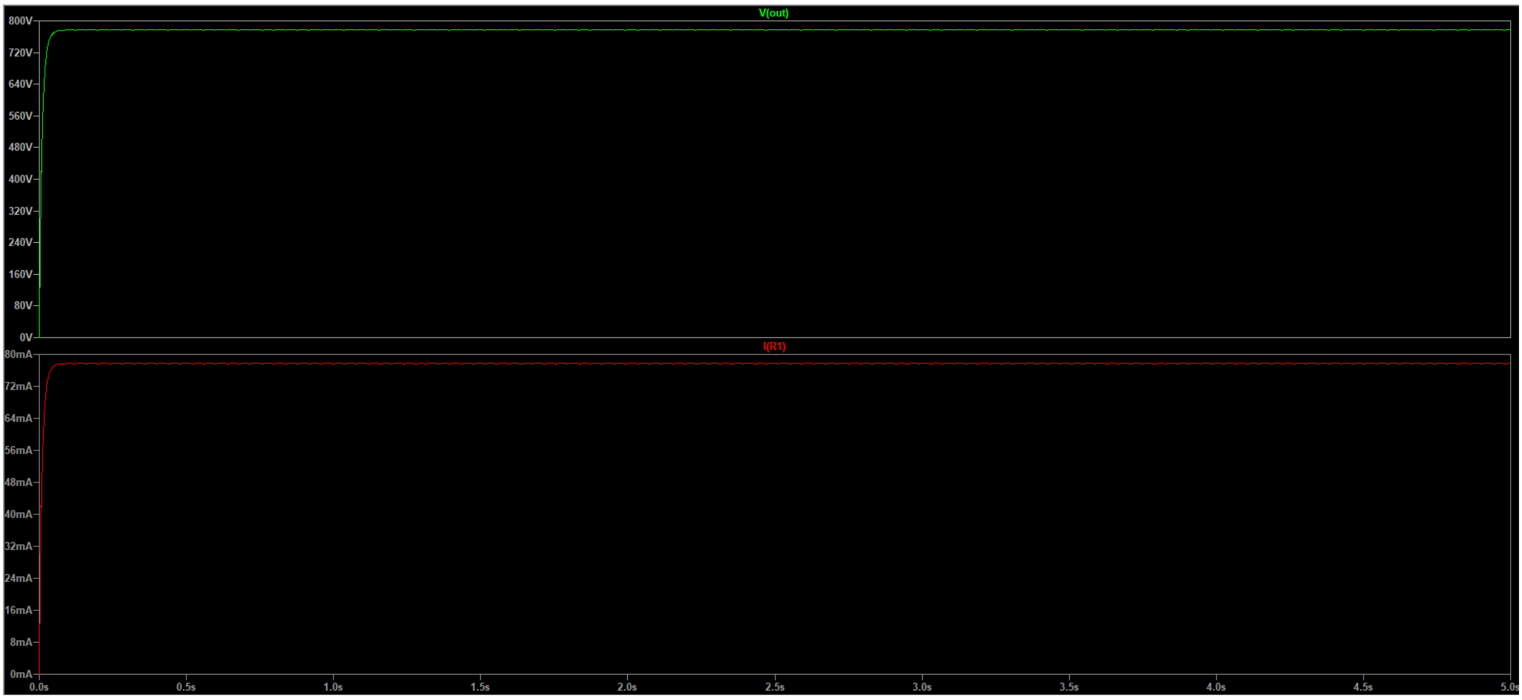

Figure 44: Output of Improved Design

	Reference Design	Improved Design	Related Figures
Output Form	Not Even Closer to DC	DC With Very Small Ripples	42 and 44
Output Voltage	6.1246419 Volts (max) and -222.6864 mVolts (min)	777.84412 Volts (max) and 776.53143 Volts (min)	42 and 43
Percentage Error According to the Expected Output (800 Volts)	99.23441976% (Calculated using max value)	2.769485%(Calculated using max value)	-
Ripple Amount (V_r) (Calculated by LTSpice Based On Maximum and Minimum Data)	6.3473283 Volts	1.3126831 Volts	42 and 43

Table 5: Results of Test 4

- Efficiency of the designs are as follows:
  - Reference Design ➔ 0.76558024%
  - Improved Design ➔ 97.230515%

5- Conclusion and Comments

Last Reminders and Remarks

- At the beginning we explained that the **Cockcroft-Walton Generator** consists of cascaded **voltage doublers**, and remember that every single voltage doubler part was called a **stage**. Then, we should notice that at the end of the every stage the gain of voltage multiplier changes. Let us take a look.

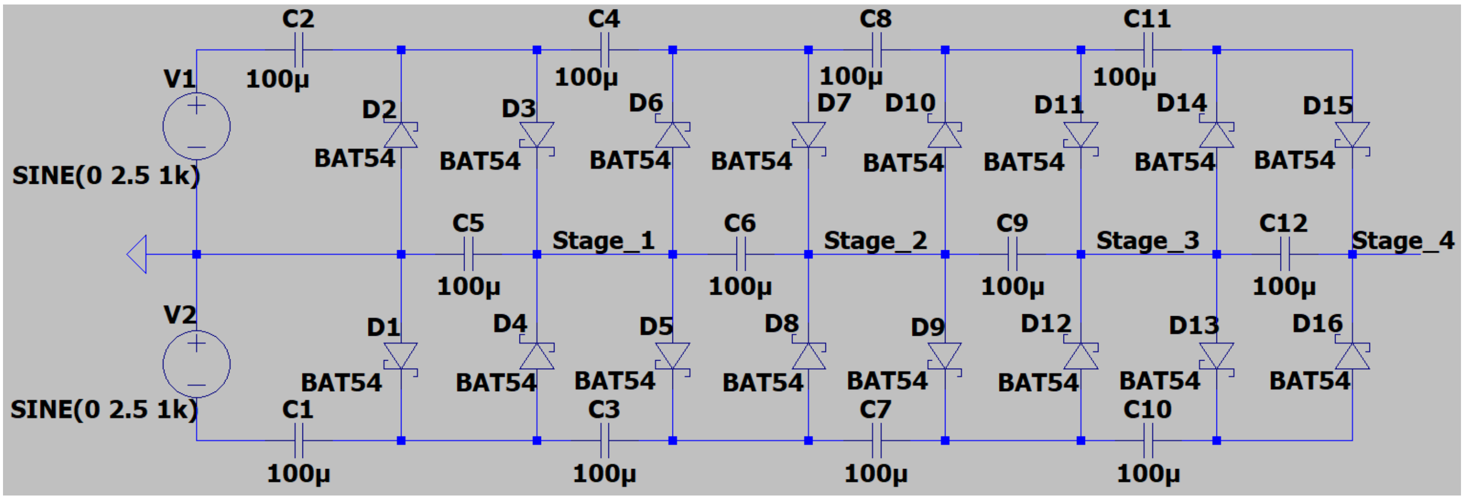

Figure 45: Improved Design With Stages

- As you can see from the figure 45 the output of the every voltage doubler is named with the related stage number.
  - If the stage is numbered with 1 which means that at that node **N = 1**.
  - The overall output is located at the Stage_4. So that, the output value of the generator is calculated using **N = 4**.

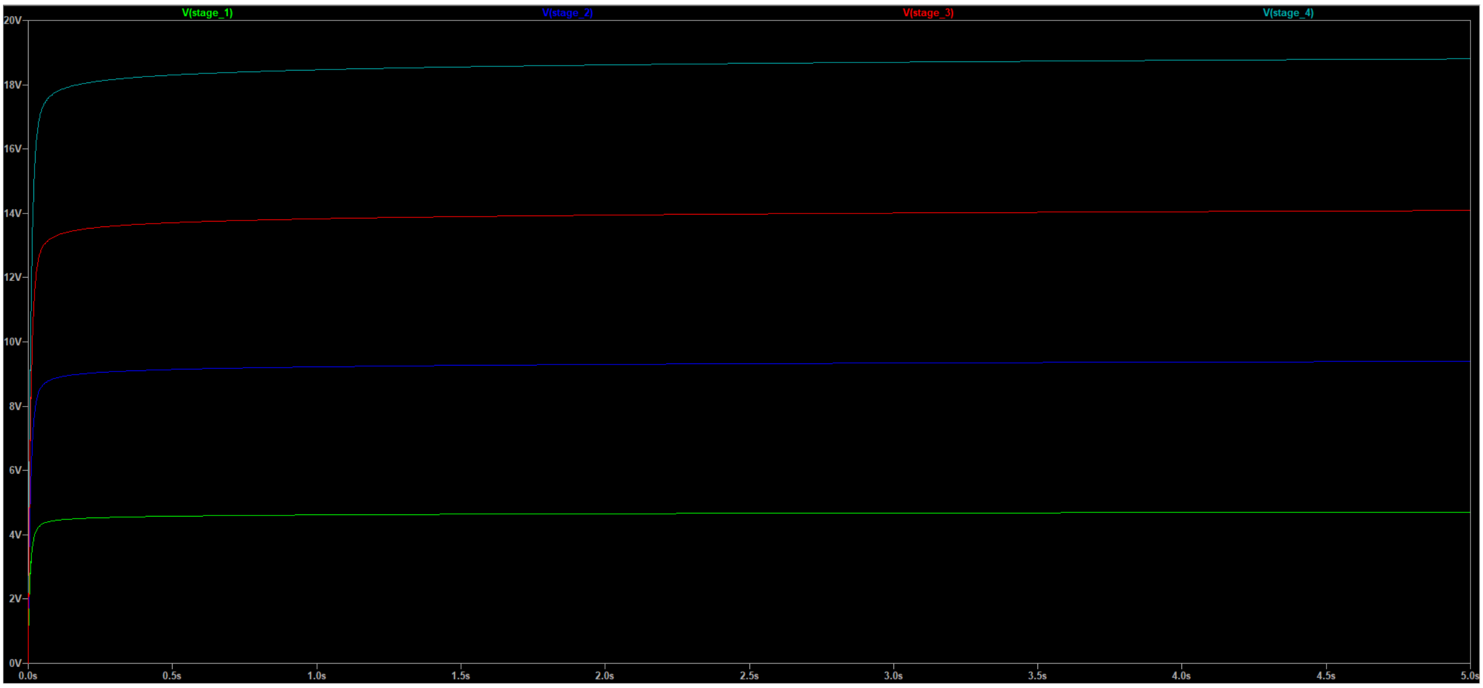

Figure 46: Outputs of Stages

- The reference Cockcroft-Walton Generator is very handy circuit design to obtain high voltages using low voltages. In my opinion, if the only goal is to increase the voltage the reference design can be used because without load resistor the ripple amounts are acceptable and the output is close to the DC. But the weakest point of this design occurs when you connect a load resistor to the output. It can work properly with high resistor values but even in that situation the result is not satisfying. Thus, the reference design needs to be redesigned. The reference design that I used is given below.

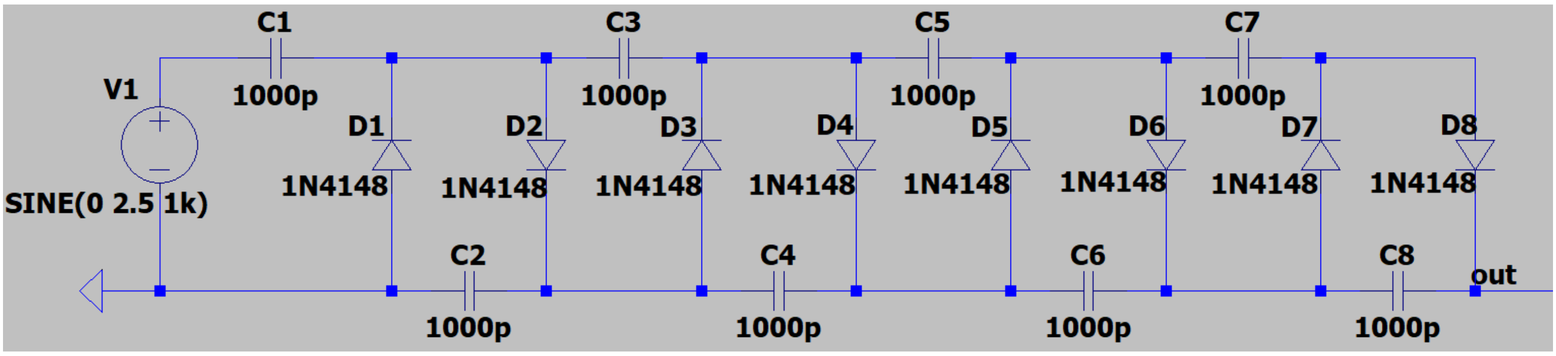

Figure 47: Reference Design

- I investigated the weak points and rearranged the values and changed the components used in the original (reference) design, and the circuit I designed has become as given below.

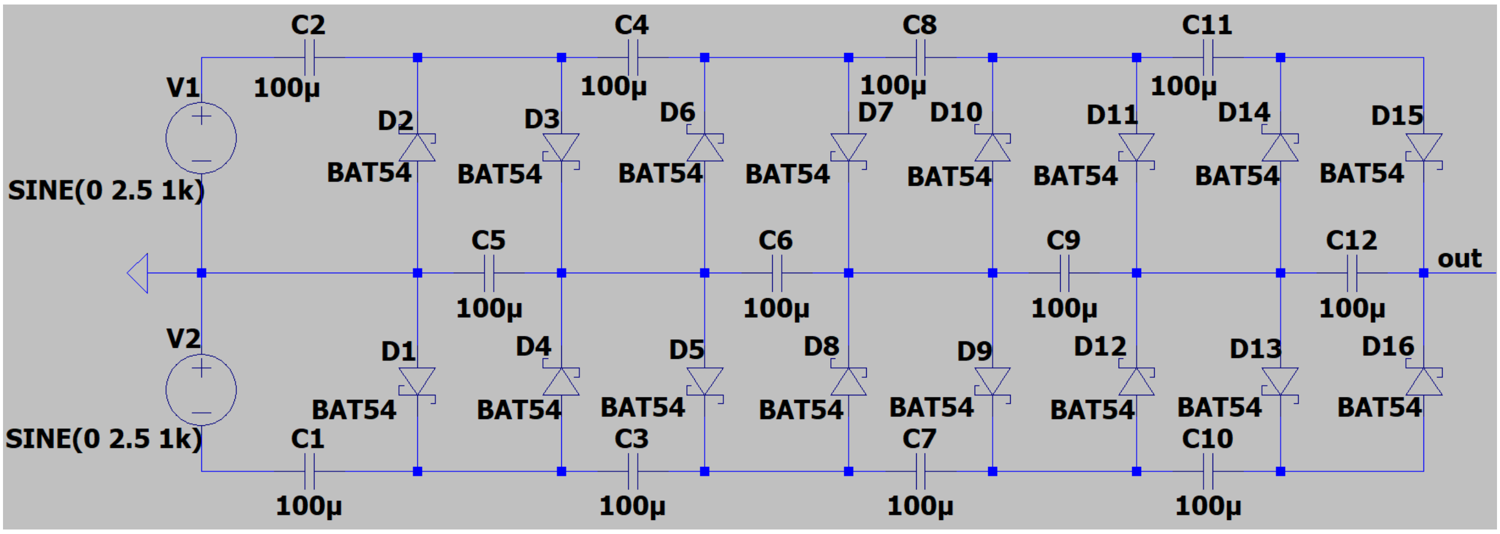

Figure 48: My Design

- In my design the output is stable even if you connect a load resistor to the output, and according to my test the efficiency of the circuit is always higher than 85%. This generator circuit can be used to produce high voltages using low voltage inputs in the devices that requires high voltage values to work properly. Another reason to use this design is cost efficiency because by using this circuit you do not need transformer which is very expensive component. So that, the design is suitable for television sets, home appliances etc.

REFERENCES

1. Reference Design of Cockcroft-Walton Generator: https://www.allaboutcircuits.com/textbook/semiconductors/chpt-3/voltage-multipliers/
2. History and Short Description of Cockcroft-Walton Generator: https://www.nms.ac.uk/explore-our-collections/stories/science-and-technology/cockcroft-walton-generator/
3. Voltage Multiplier Basics: https://www.electronics-tutorials.ws/blog/voltage-multiplier-circuit.html
4. Voltage Multiplier and Cockcroft-Walton Generator: https://en.wikipedia.org/wiki/Voltage_multiplier
5. Cockcroft-Walton Generator: https://en.wikipedia.org/wiki/Cockcroft%E2%80%93Walton_generator
6. Basics of RC Circuits: https://www.electronics-tutorials.ws/rc/rc_1.html
7. Datasheet of 1N4148: https://www.vishay.com/docs/81857/1n4148.pdf
8. Datasheet of BAT54: https://www.vishay.com/docs/85508/bat54.pdf