GEBZE TECHNICAL UNIVERSITY
ENGINEERING FACULTY
ELECTRONICS ENGINEERING DEPARTMENT

ELEC-336
Electronics II
Project

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Numarası	**210102002061** **210102002033**

1)Circuit schematic and explanations of design choices

1) Introduction

Differential amplifiers are fundamental building blocks in analog circuit design, widely used due to their high gain, low noise, and superior common-mode rejection capabilities. These circuits play a vital role in various applications such as signal amplification, noise reduction, and data transmission.

In this project, a differential amplifier with an active load is designed and analyzed. The use of an active load provides higher differential gain and improves the common-mode rejection ratio (CMRR) compared to resistive loads. Additionally, the design is optimized for low power consumption, which is critical for modern integrated circuits, especially in portable and battery-operated devices.

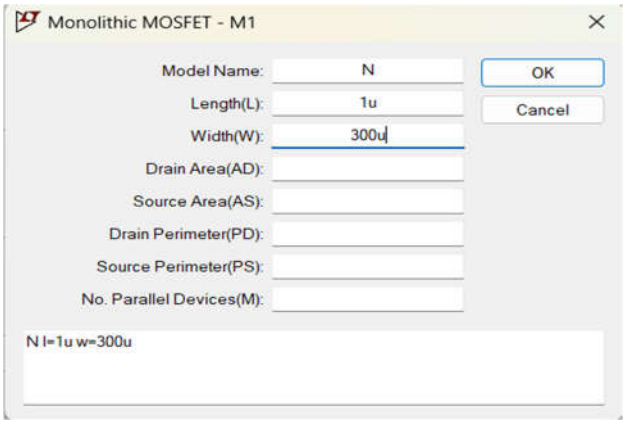
The design is implemented using 180nm CMOS technology and simulated in LTSpice. With a supply voltage of 1.8V and a tail current of 1mA, the circuit achieves efficient operation while maintaining performance metrics such as high gain and CMRR.

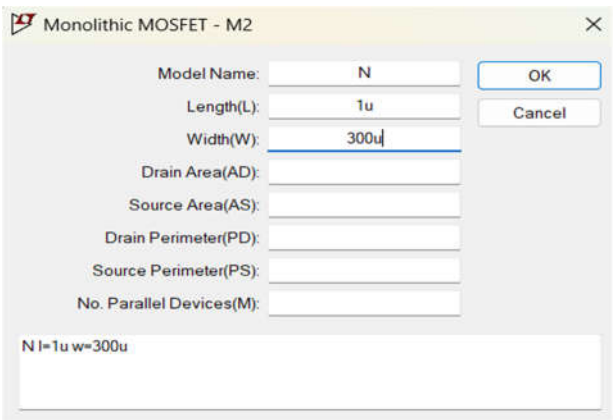
The goal of this project is to design a differential amplifier and evaluate its performance metrics, including gain, input/output impedance, CMRR, and power consumption. The design process, operating principles, and simulation results are thoroughly documented to ensure a comprehensive understanding of the circuit's operation and optimization.

2) Design and Component Selection

a. **Input Differential Pair (M1 and M2):**

- **Transistors M1 and M2:** These are NMOS transistors forming the core of the differential amplifier W/L ratio is 300u/1u.

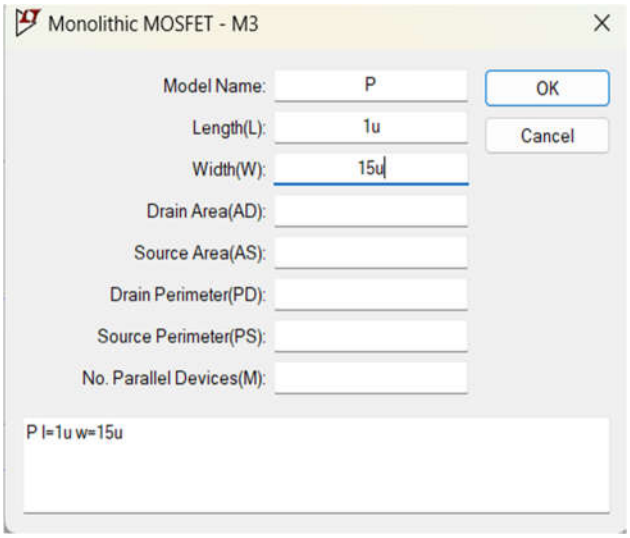


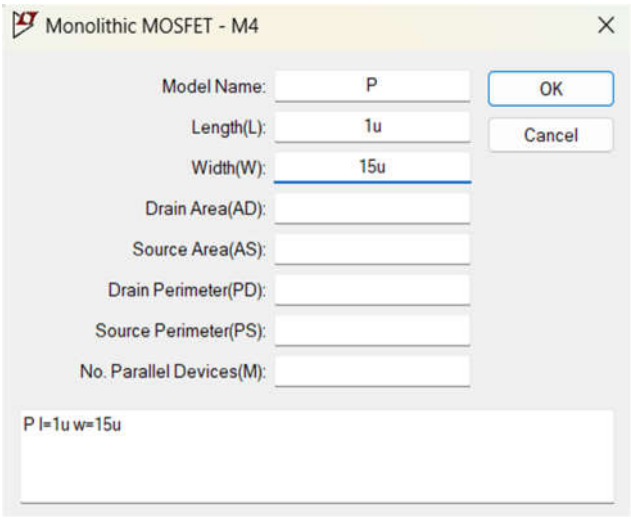


- **Functionality:**
  - Amplify the difference between the input signals applied at the gates of M1 and M2.
  - Operate in the saturation region to achieve maximum amplification.
  - Properly biased using the tail current source (I1) to ensure stable operation.

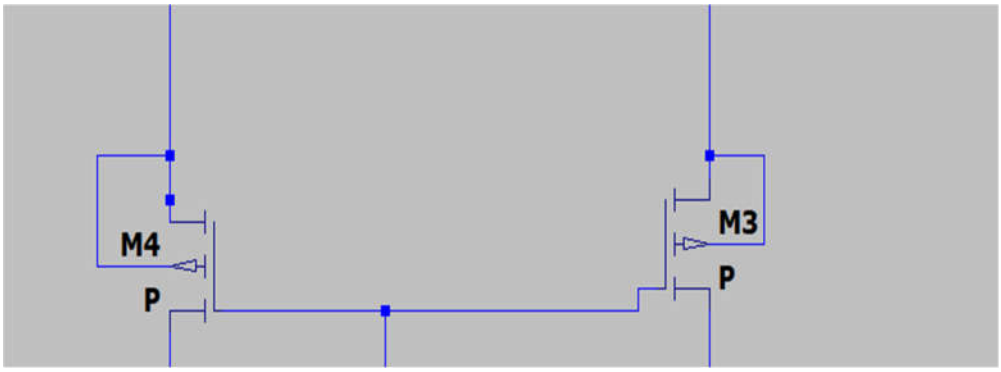
b. **Active Load (M3 and M4):**

- **Transistors M3 and M4:** These are PMOS transistors configured as a current mirror W/L ratio is 15u/1u .





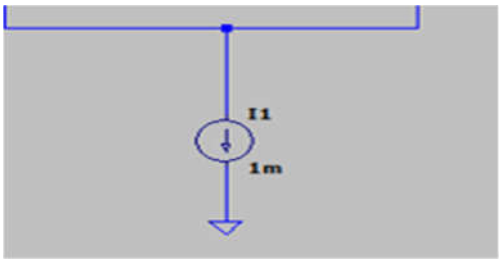
- **Functionality:**
  - Act as an active load for the differential amplifier, enhancing the voltage gain.
  - Provide high output resistance, which is essential for achieving a high differential gain.



c. **Tail Current Source (I1):**

- **Current Source (I1):** Sets the bias current for the differential pair.

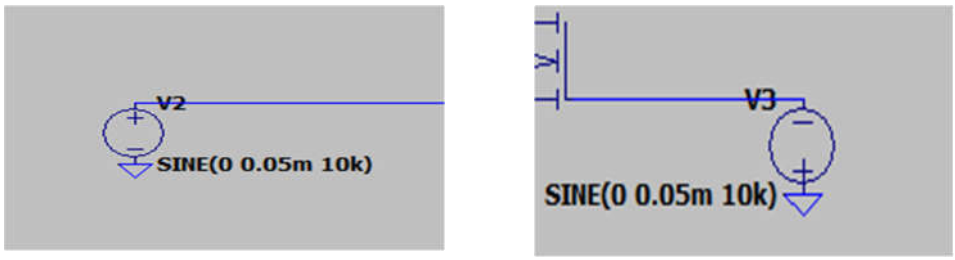
- **Functionality:**
  - Ensures balanced operation of the differential amplifier.
  - Improves common-mode rejection by providing constant current regardless of input conditions.



d. **Input Sources (V2 and V3):**

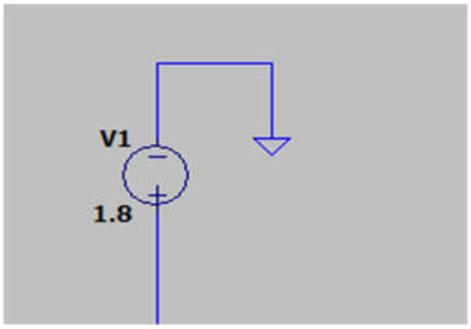
- Differential sinusoidal signals are applied to the gates of M1 and M2.

- Amplitude: 0.05mV.
- Frequency: 10kHz.
- These signals represent the differential input that the amplifier is designed to process.



e. **Power Supply (V1):**

- A 1.8V DC voltage source powers the circuit.
- Chosen to align with the CMOS technology node, ensuring proper transistor operation.

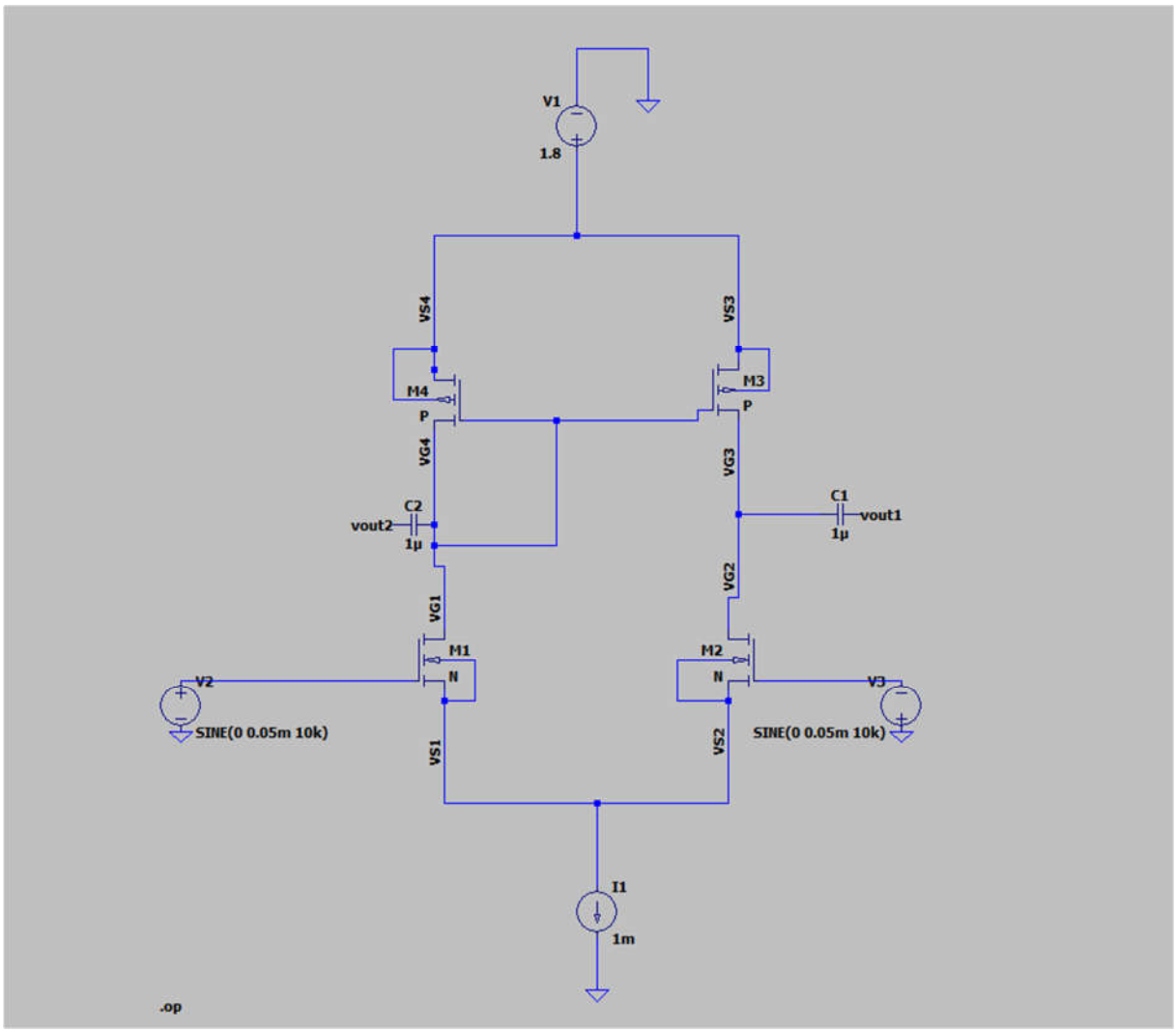


f. **Capacitors (C1 and C2):**

- Serve as coupling capacitors for the output nodes (Vout1 and Vout2).
- Block any DC component while allowing the AC signal to pass.

3) Circuit Design

The differential amplifier employs a current mirror as an active load, consisting of PMOS transistors M3 and M4, to achieve high performance. The active load enhances the circuit's output resistance, significantly boosting the differential gain (Ad), which is the ratio of the amplified differential output voltage to the differential input voltage. The NMOS transistors M1 and M2 form the input differential pair, amplifying the difference between the input signals, while the tail current source (I1) ensures symmetric operation and rejects common-mode signals. This symmetry minimizes the common-mode gain (Acm), resulting in a high common-mode rejection ratio (CMRR), defined as 20log(Ad/Acm). The high CMRR ensures effective noise and interference rejection, making the design suitable for precise signal amplification. Overall, the active load and current source are key to optimizing gain, reducing common-mode effects, and achieving the design goals of high Ad, low Acm, and robust CMRR.



2) Simulation results (DC, AC, and transient waveforms) and Calculation

A) DC Analysis And Simulation results

The DC analysis was performed to evaluate the operating point of the differential amplifier. The simulation results confirm that the transistors operate in the correct regions and that the circuit functions symmetrically. Below, the findings are validated with theoretical principles:

1. **Saturation Region Operation of NMOS Transistors:** NMOS transistors must satisfy the following conditions to operate in the saturation region:

$$Vds > Vgs - Vth$$

Here, Vth (threshold voltage) is approximately 0.4 V. From the simulation results, the drain current of M1 and M2 is Id=0.5 mA, and the Vgs values ensure that the saturation condition is met.

2. **Saturation Region Operation of PMOS Transistors:** PMOS transistors (M3 and M4), which form the current mirror, must satisfy the following conditions:

$$|Vds| > |Vgs - Vth||$$

The simulation confirms that M3 and M4 source a current of Is=0.5 mA, indicating proper operation of the current mirror. This configuration provides high output resistance, enhancing the differential gain.

3. **Symmetry of Differential Output Voltages:** For balanced operation, the tail current (I1) should be evenly distributed between M1 and M2:

$$I1 = Id(M1) + Id(M2)$$

According to the simulation, the tail current I1=1 mA is equally divided, with 0.5 mA, flowing through each NMOS transistor. Additionally, the output voltages (Vout1 and Vout2) are symmetric, confirming proper differential operation.

Here, gm=Id/Vov, where Vov=Vgs−Vth. The simulation results demonstrate that the high output resistance of the PMOS active load significantly increases the gain.

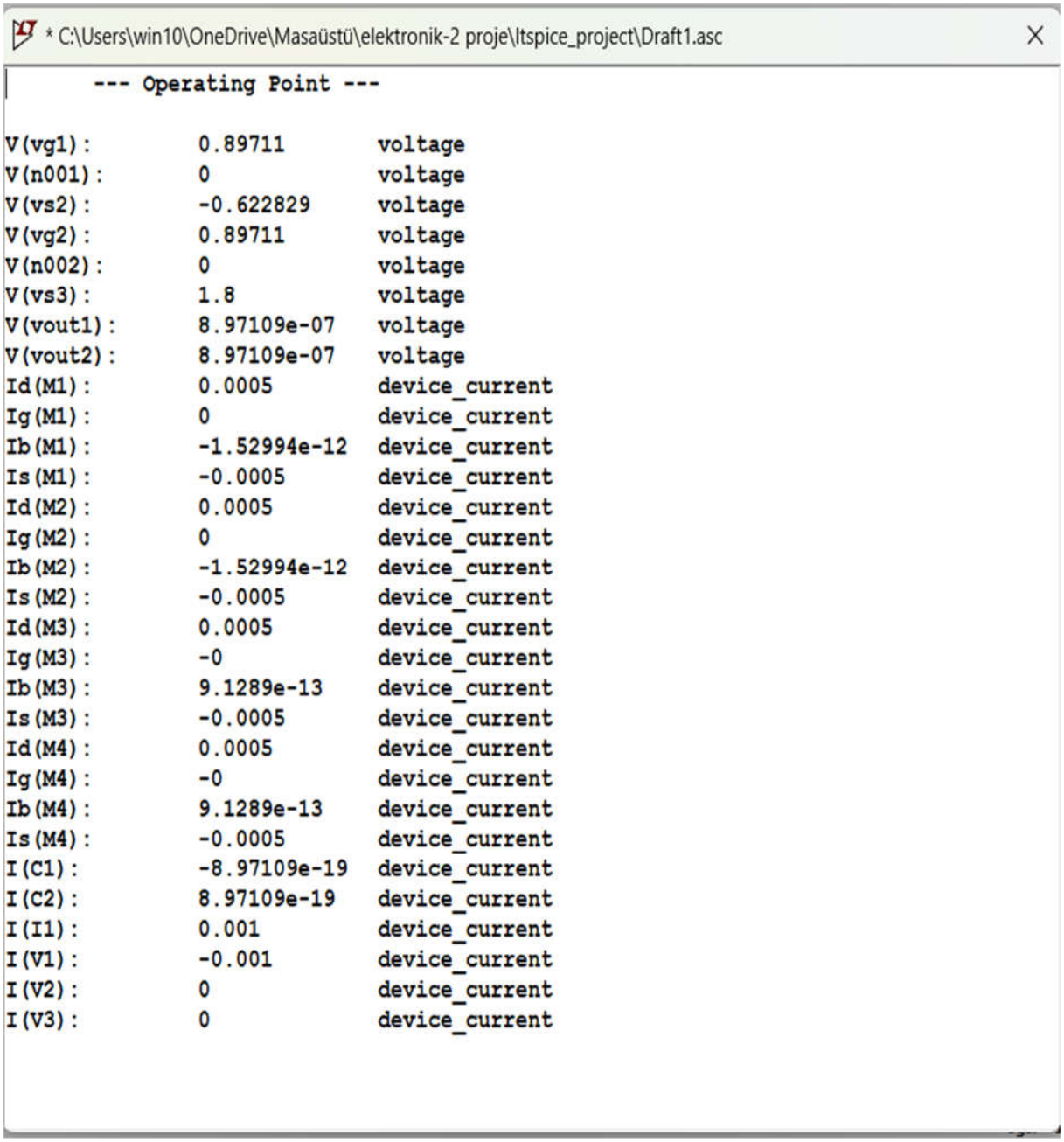
4. **Current Balance:** The current balance across the circuit is validated by the following equality:

$$Is(M3) = Is(M4) = Id(M1) = Id(M2)$$

In the simulation, all these currents are 0.5 mA, confirming balanced operation of the differential pair and the current mirror.

- The DC analysis confirms that all transistors in the circuit operate in the saturation region, the differential pair achieves symmetrical current distribution, and the output voltages exhibit the expected symmetry. Furthermore, the active load (current mirror) enhances the gain and output resistance, significantly improving circuit performance. These findings validate that the differential amplifier is correctly designed and that the simulation results align with theoretical expectations.

DC Simulation results:



B) AC Analysis And Simulation Results and Calculation (Ad – Acm – BW(3Db and unity-gain) - Rin – Rout – CMRR)

1. Differential Gain (Ad)

The differential gain (Ad) represents the ability of the amplifier to amplify the voltage difference between two input signals. It is calculated as the ratio of the differential output voltage (Vout1−Vout2) to the differential input voltage (Vin1−Vin2):

$$Ad=((Vout1-Vout2)/(Vin1-Vin2))$$

In the simulation, opposite-phase input signals (Vin1=−Vin2) with an amplitude of 0.2 mV were applied. The output differential voltage was measured as 17.45mV. Substituting these values into the formula:

$$Ad=((17.45/(0.2))=87.25\ V/V$$

In decibels (dB), the differential gain is expressed as:

$$Ad(dB)=20\cdot\log(Ad)$$

Substituting the calculated gain:

$$Ad(dB)=20\cdot\log10(87.25)\approx 38.81dB$$

The achieved high differential gain (Ad=87.25 V/V) demonstrates the effective amplification of differential input signals. The symmetry observed in the output waveforms further confirms the correct operation of the differential pair and the active load, contributing to the high gain.

Observation Regarding Vout2:

The voltage at Vout2 is observed to be close to 0 V. The following factors can explain this behavior:

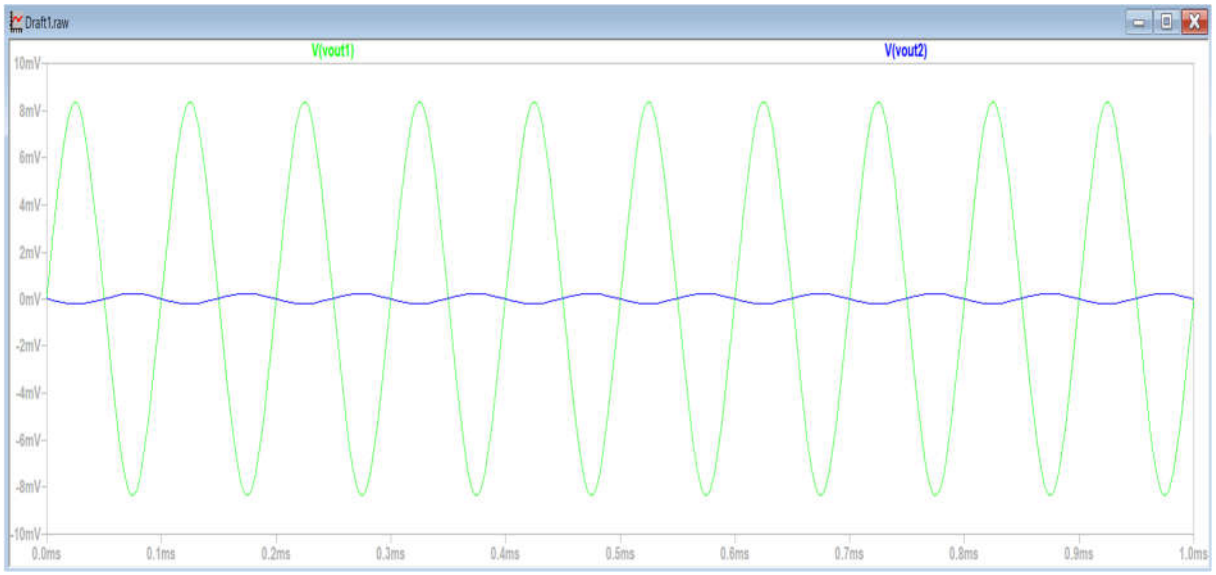
a. Differential Design:
   The circuit prioritizes amplifying the difference between Vout1 and Vout2 rather than individual outputs. As a result, one output (e.g., Vout2) may approach 0 V due to the complementary nature of the differential design.

b. Symmetric Operation:
   In a perfectly balanced differential amplifier, when Vout1 increases, Vout2 decreases proportionally. This ensures that the difference (Vout1−Vout2) is maximized, while individual outputs may appear reduced or close to 0 V.

c. Active Load Impact:
   The current mirror (active load) enhances the output impedance and ensures symmetry. However, it also restricts the single-ended output voltage swing, making one of the outputs (e.g., Vout2) appear lower in magnitude.

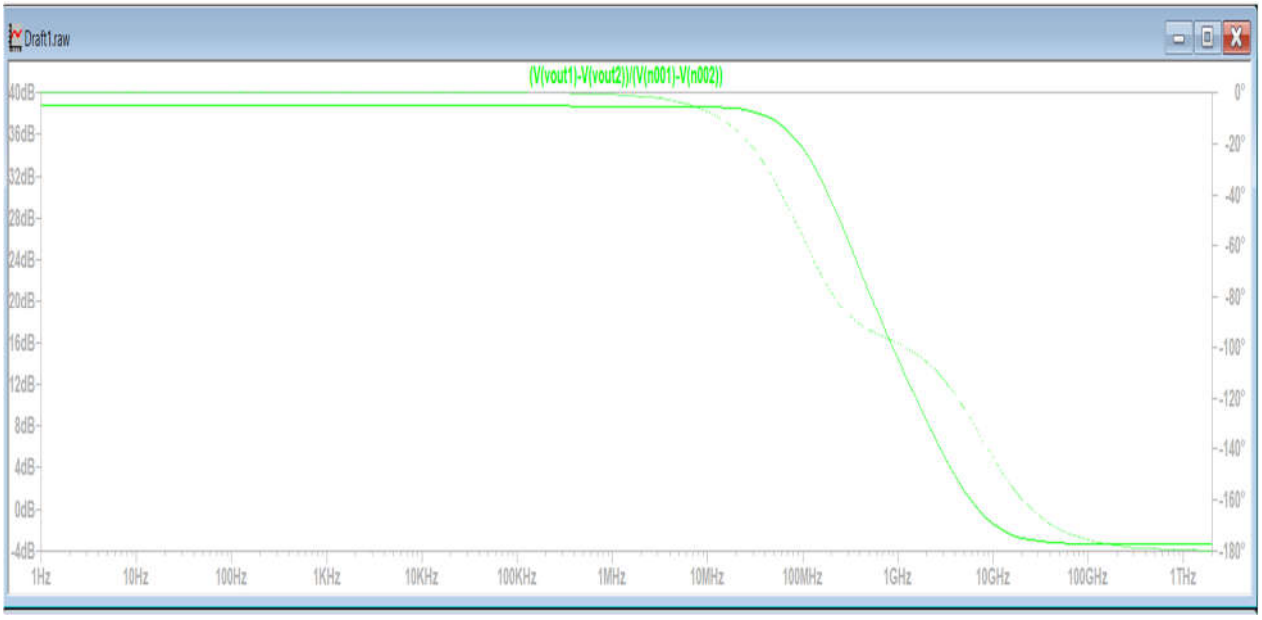
The calculated differential gain (Ad=87.25 V/V) satisfies the design goal Ad>80 V/V) The voltage at Vout2 being close to 0V is a direct result of the circuit's differential design, which ensures symmetric operation and maximized differential output (Vout1−Vout2). This behavior confirms the proper functionality of the amplifier and emphasizes the importance of using differential outputs for optimal performance.

Differential gain simulation result



dx = 80.529509µs(12.417808KHz) dy = 17.45mV (slope = 216.733V/s)

Differential gain (dB) simulation result



2) Common-Mode Gain (Acm)

The common-mode gain (Acm) evaluates the ability of the amplifier to suppress common-mode signals, which are identical signals applied to both inputs. It is calculated as the ratio of the differential output voltage (Vout1−Vout2) to the sum of the input voltages (Vin1+Vin2):

$$Acm=(Vout1−Vout2)/(Vin1+Vin2)$$

In this analysis, identical input signals (Vin1=Vin2=0.1 mVpp} were applied. The resulting differential output voltage was measured as 1.554 nV. Substituting these values into the formula:

$$Acm=1.554\ nV/0.2\ mV=7.77×10−6\ V/V$$

This extremely small gain indicates that the circuit effectively suppresses common-mode signals.

To express the common-mode gain in decibels (dB), the following formula is used:

$$Acm(dB)=20·log(Acm)$$

Substituting the calculated gain:

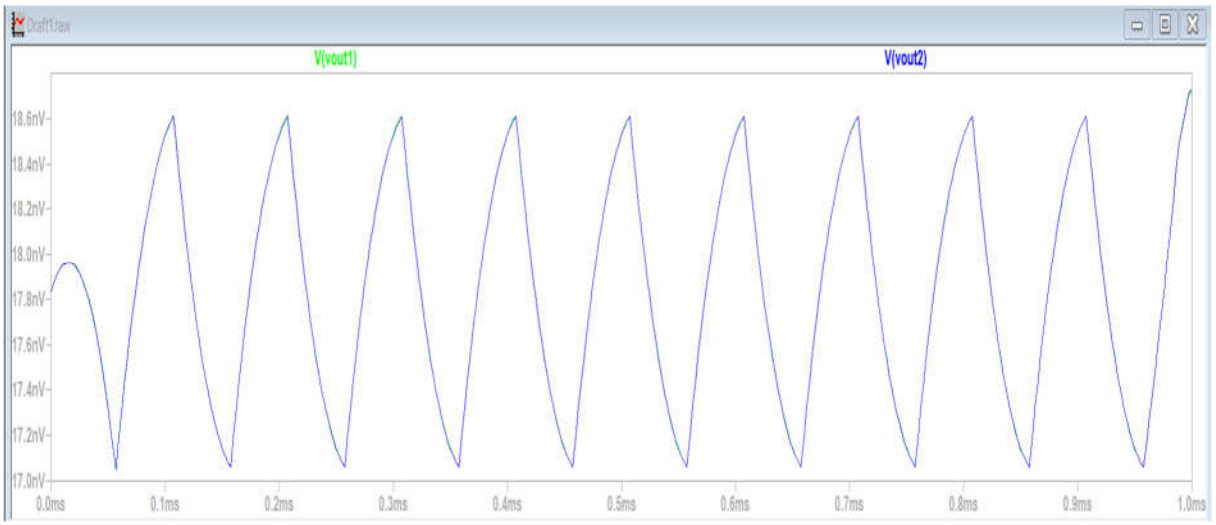
$$Acm(dB)=20·log(7.77×10−6) ≈ −102.2\ dB$$

Interpretation of Results

1. **Negative dB Value:** A negative dB value (−102.2 dB) for the common-mode gain signifies that the gain is significantly less than 1. This means the amplifier strongly suppresses the common-mode signal, allowing almost no amplification of identical input signals.
2. **Low Common-Mode Gain:** The calculated Acm=7.77×10−6 V/V confirms that the amplifier is highly efficient in rejecting common-mode signals. This ensures that the circuit is effectively isolating the differential signal from unwanted noise or interference, which is a key requirement in differential amplifier designs.

The common-mode gain (Acm) is extremely low, as expected, with a value of −102.2 dB . This indicates excellent common-mode rejection, confirming that the circuit is optimized for differential signal amplification while effectively suppressing identical signals applied to both inputs. The results align with the design goals and validate the amplifier's functionality.

Common-Mode gain simulation result

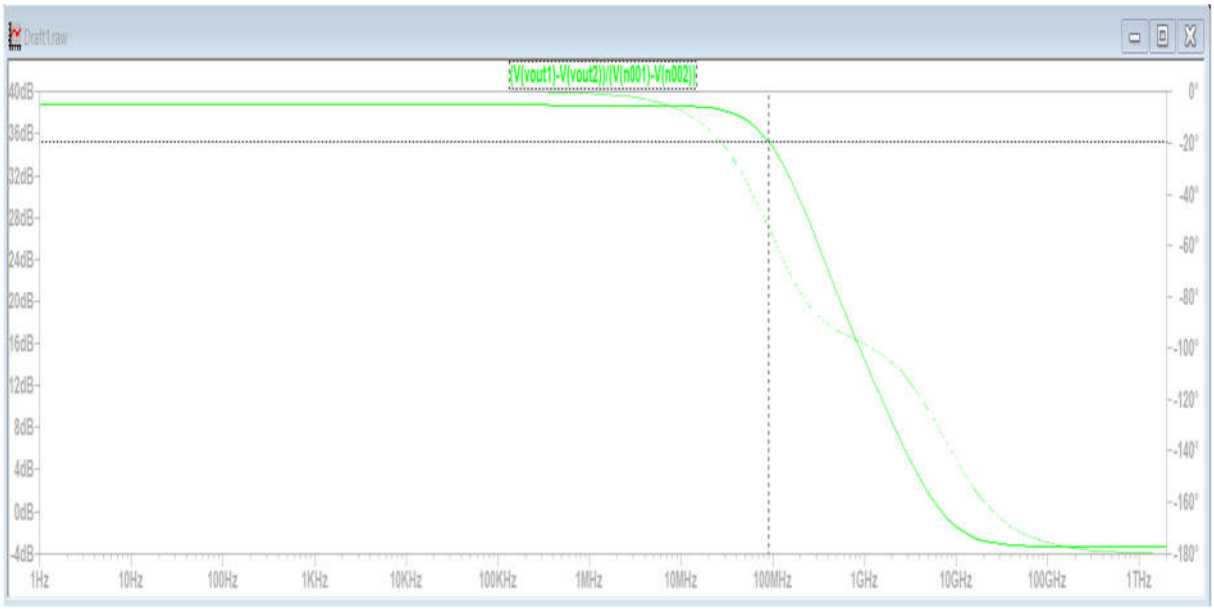


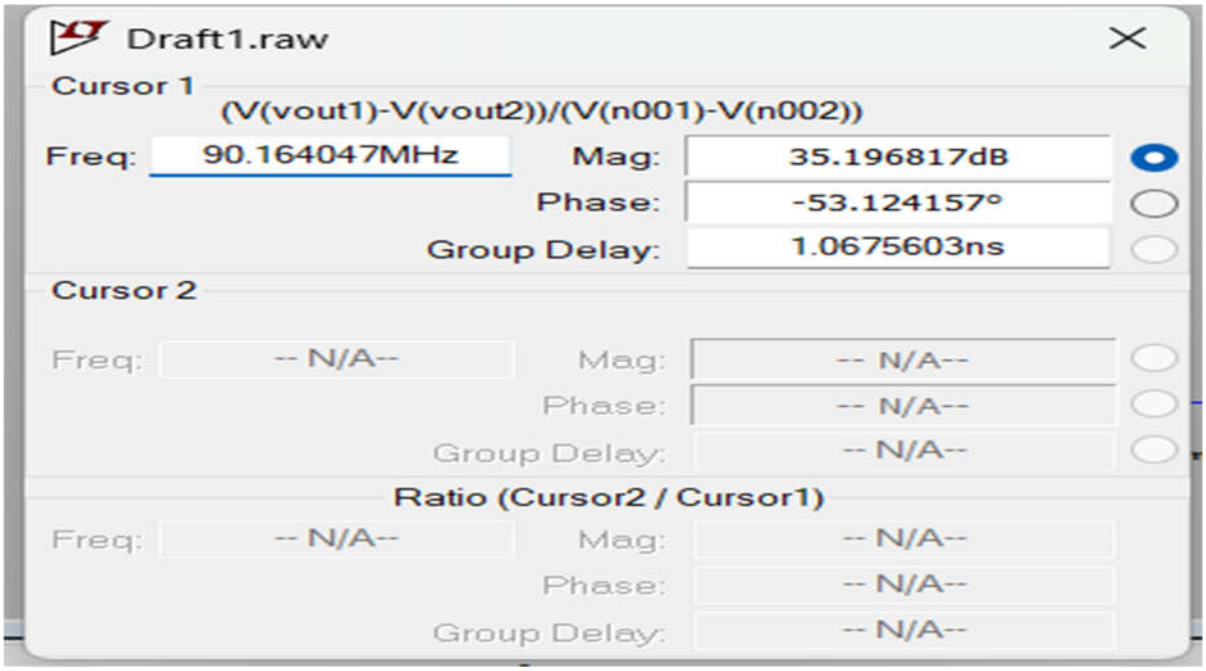
dx = 121.61415µs(8.2227273KHz) dy = 1.554nV (slope = 1.27784e-05V/s)

3) Bandwidth 3Db and unity-gain

During the AC analysis, the frequency-dependent gain variation of the differential amplifier was examined, and the frequency at which the gain drops by 3 dB was determined to be approximately 90 MHz. In this analysis, the frequency at which the gain decreases by 3 dB from its maximum value was identified. The calculation involved locating the point on the Bode plot where the gain is 3 dB lower than the maximum value (e.g., if the maximum gain is 38.81 dB, the frequency corresponding to 35.81 dB was marked). This value defines the amplifier's bandwidth and represents the maximum speed at which the system can accurately process high-frequency signals. The 3 dB frequency is a critical parameter in defining the performance limits of a system, and this study demonstrates that the design is suitable for high-speed applications .

Bandwidth 3Db simulation result

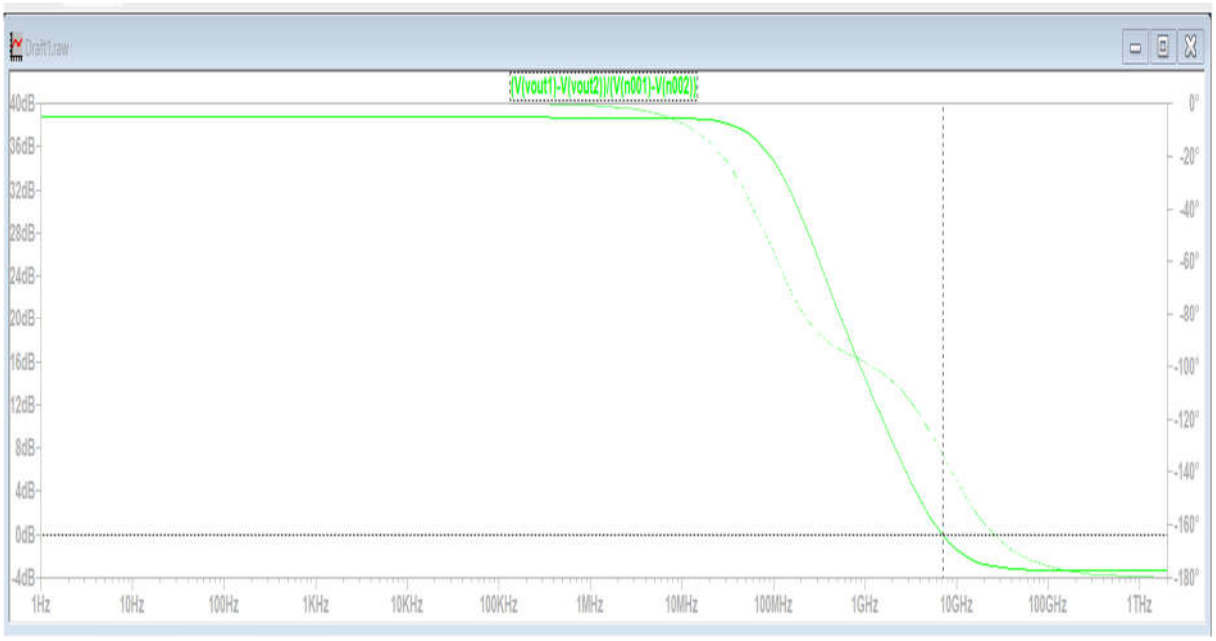


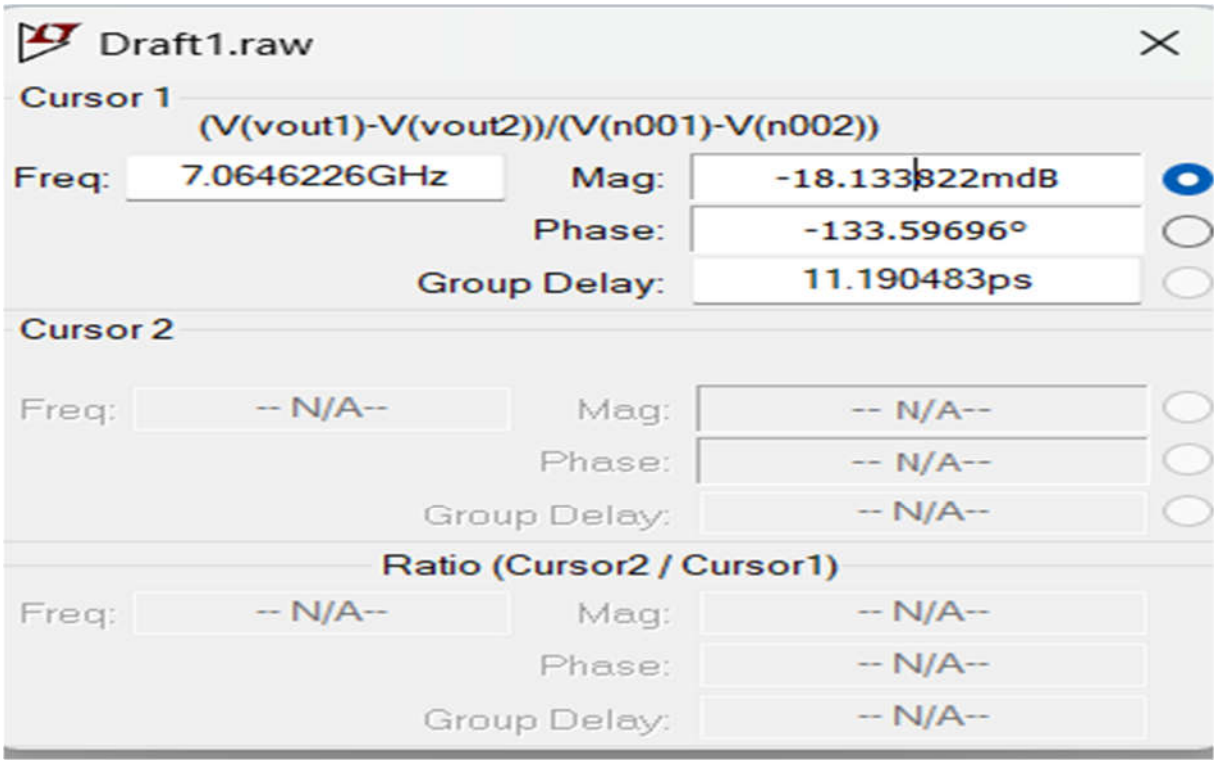


Unity gain refers to the condition where the amplifier's gain is 0 dB, meaning the ratio between the input and output signals is one-to-one. According to the simulation results, the unity gain frequency was determined to be approximately 7 GHz. At this frequency, the amplifier transmits the signal without providing any gain. On the Bode plot, the unity gain frequency corresponds to the point where the gain curve intersects

the 0 dB line. The unity gain frequency is crucial for evaluating the amplifier's ability to operate and remain stable at high frequencies

Unity-Gain simulation result





4) Rin

In differential amplifiers, the input impedance (Rin) is generally expected to be high, as this minimizes the loading on the signal source and prevents signal loss. In this design, the input impedance was calculated based on the simulation results, which showed a small voltage variation (Vin) of 0.1 mV applied at the input and the resulting input current (Iin) of 9.5 pA. Using the formula:

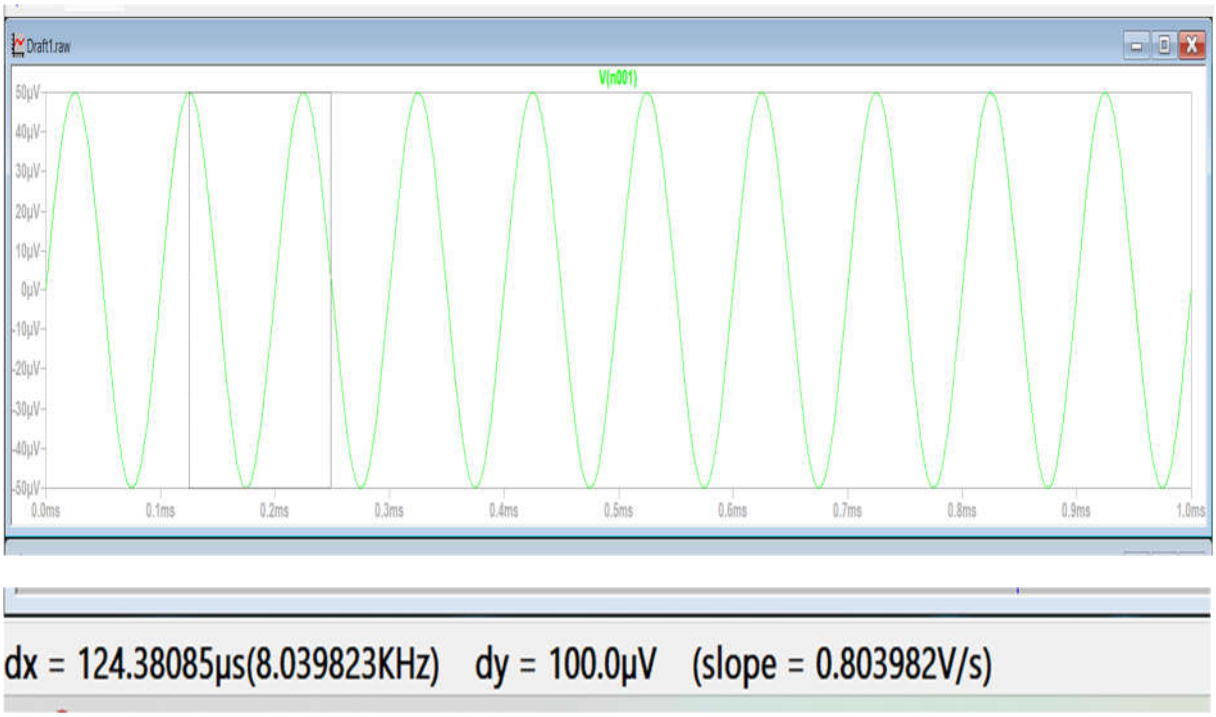
$$Rin=(Vin/Iin)$$

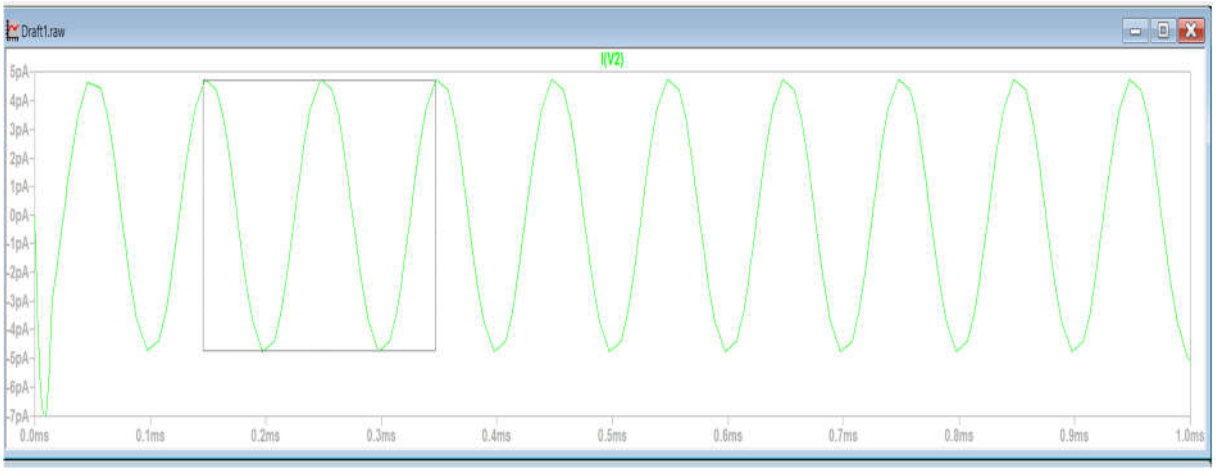
The calculated value is:

$$Rin=0.1mV/9.5pA=10.53M\Omega$$

This result aligns well with the theoretical expectation of a high input impedance for differential amplifiers with active loads. The high Rin confirms that the circuit is effectively designed to handle input signals without significant loading, ensuring efficient signal processing.

Rin simulation result





dx = 200.43812µs(4.989071KHz) dy = 9.47pA (slope = 4.72257e-08A/s)

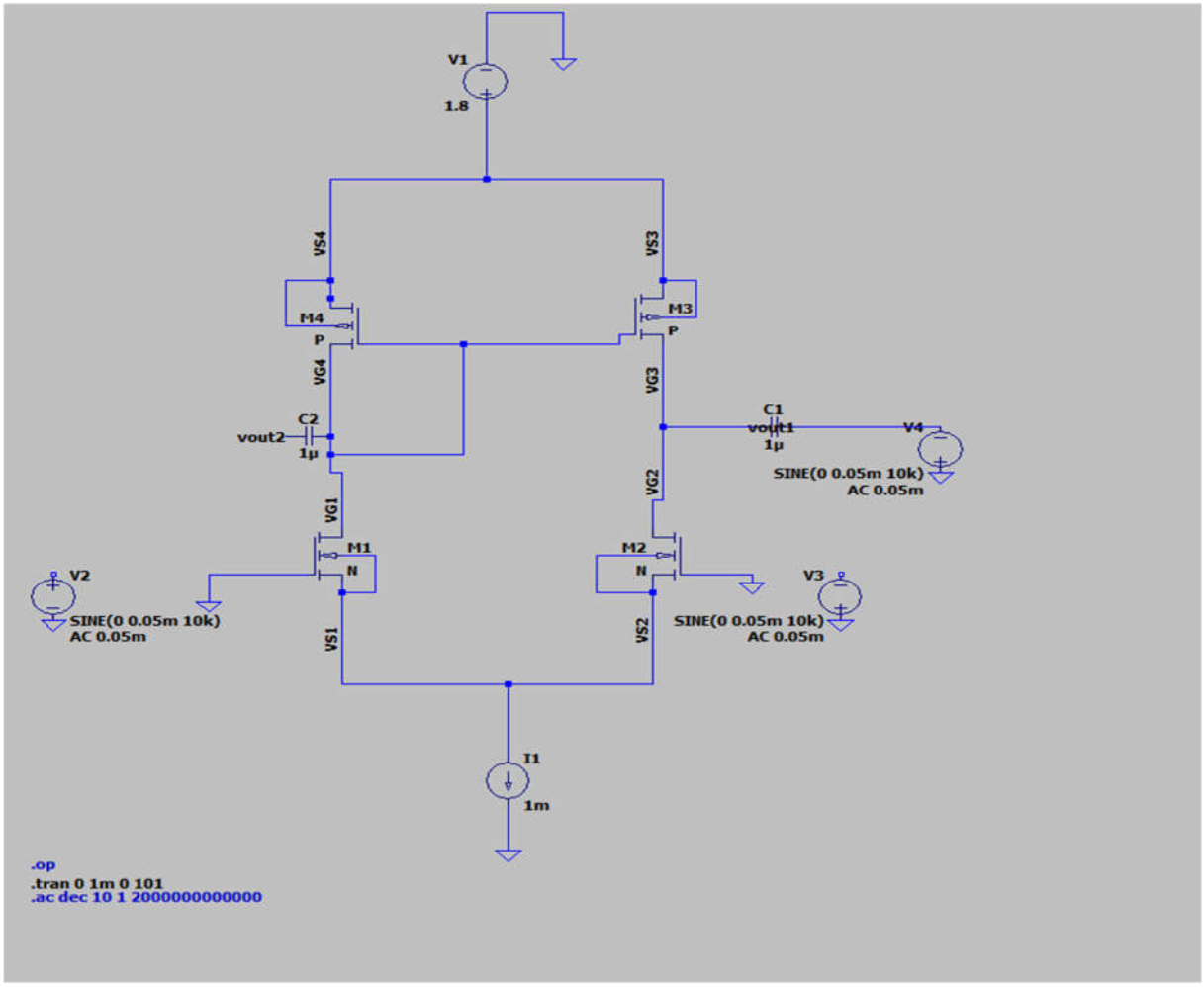
5) Rout

In differential amplifiers with active loads, the output impedance (Rout) is a critical parameter that affects the circuit's gain and overall performance. In this design, Rout was measured by grounding the input sources (V2 and V3) to eliminate their influence on the output. A small test voltage (Vtest=0.1mV) was applied to the output terminal (Vout), and the resulting output current (Itest=8.5 nA) was measured in the simulation. The output impedance was then calculated using the formula:

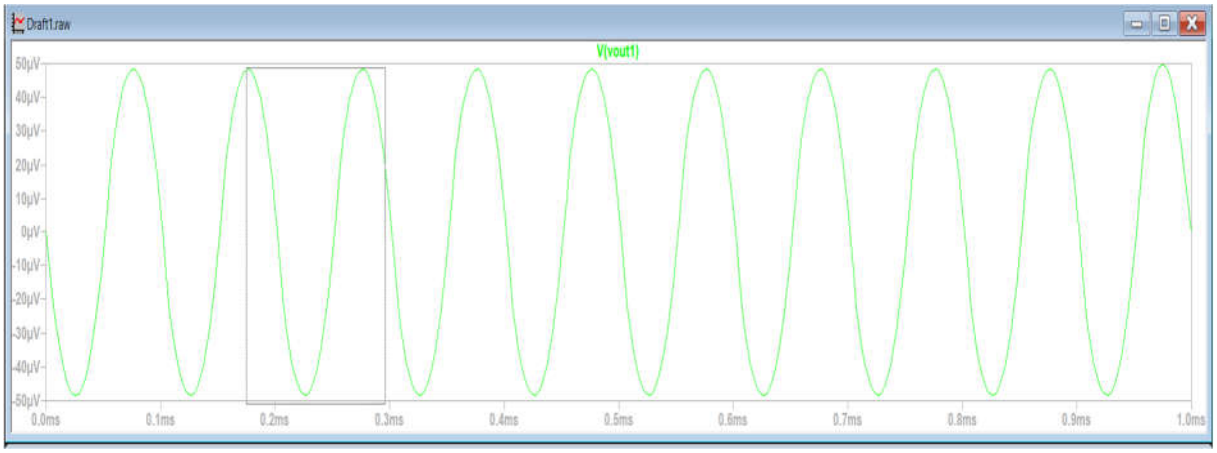
$$R_{out} = \left(\frac{V_{test}}{I_{test}}\right) = \frac{0.1\ mV}{8.5\ nA} \approx 11.76\ k\Omega$$

This result reflects a moderate output impedance, which is consistent with the expected behavior for an active-load differential amplifier, confirming the proper functionality and balance of the design.

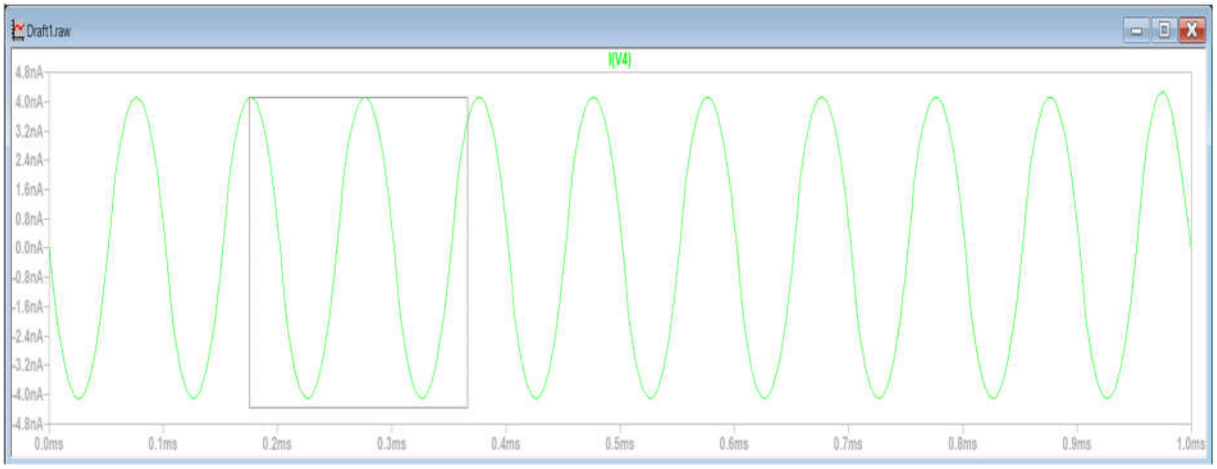
Circuit Design for Output Impedance (Rout) Measurement



Rout simulation result



dx = 214.63952µs(4.6589744KHz) dy = 100.0µV (slope = 0.465897V/s)



dx = 191.5011µs(5.221902KHz) dy = 8.5nA (slope = 4.437e-05A/s)

6) CMRR (Common Mode Rejection Ratio)

The Common-Mode Rejection Ratio (CMRR) is a critical parameter that quantifies a differential amplifier's ability to suppress common-mode signals while amplifying differential signals. CMRR is expressed as the logarithmic ratio of differential gain (Ad) to common-mode gain (Acm) using the formula:

$$CMRR=20\cdot\log(Acm/Ad)$$

In this design, simulation results provided Ad=87.25 V/V and Acm=7.77×10−6V/V. Using these values, CMRR was calculated as follows:

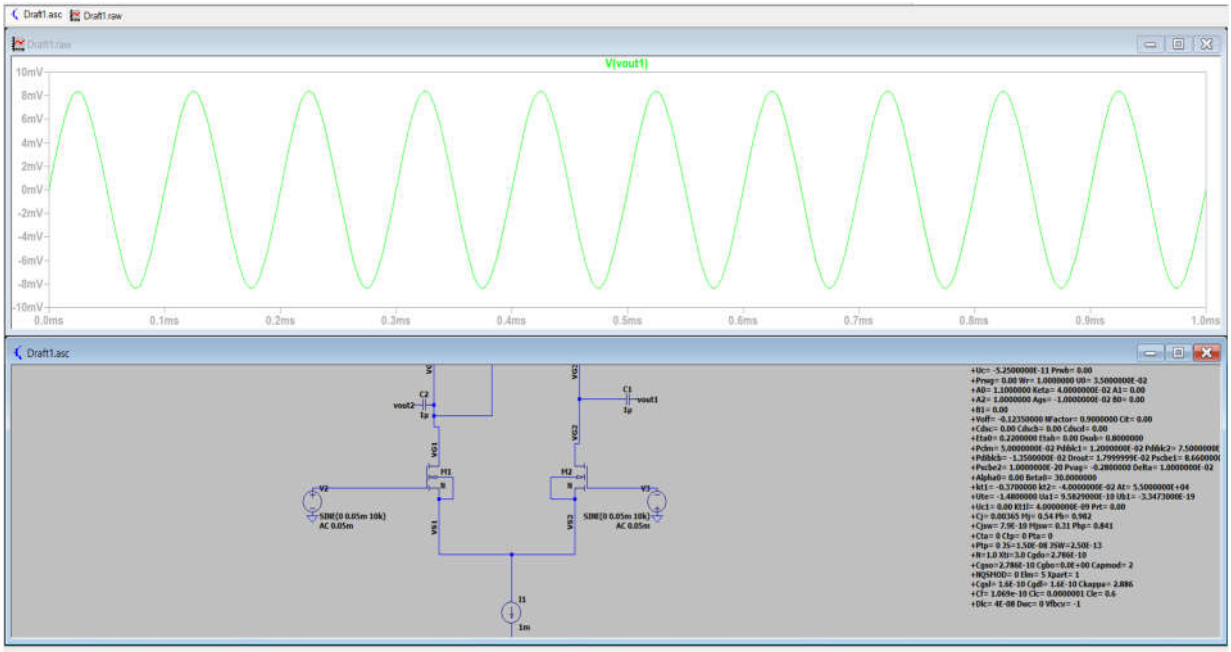
$$CMRR=20\cdot\log(87.25/7.77\times10-6) = 141.0\ dB$$

The calculated CMRR=141.0 dB demonstrates the amplifier's high sensitivity to differential signals and its effective suppression of common-mode signals. This high value confirms the design's success in achieving excellent noise immunity and precise signal amplification.

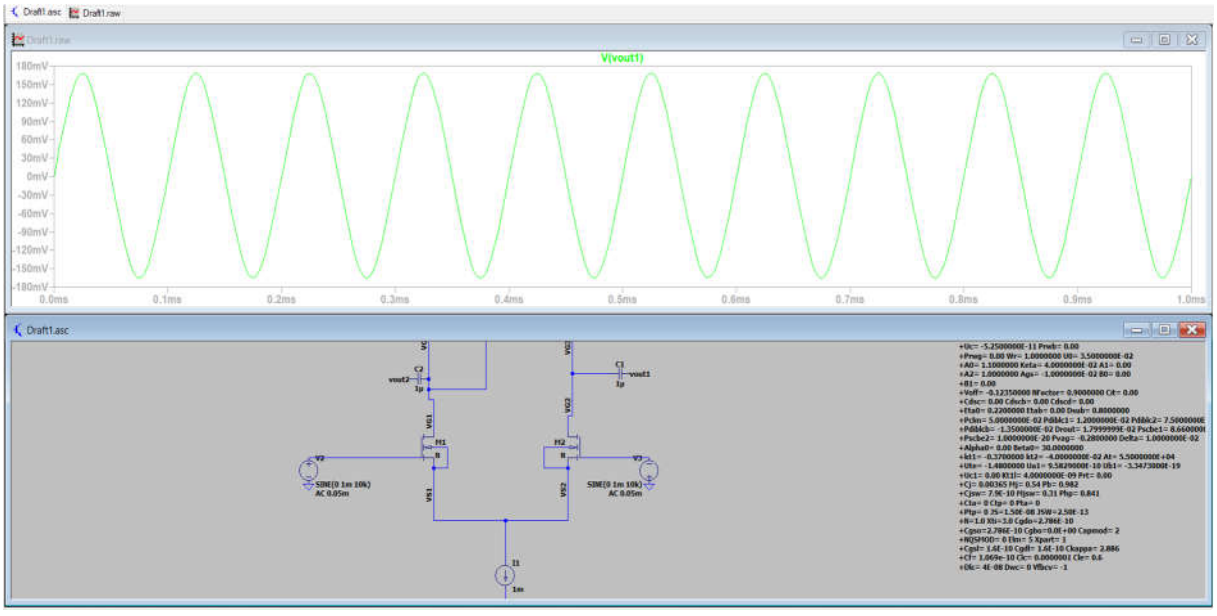
C) Transient Analysis

By increasing the voltage value of the input signal step by step, the value of the output signal was observed.

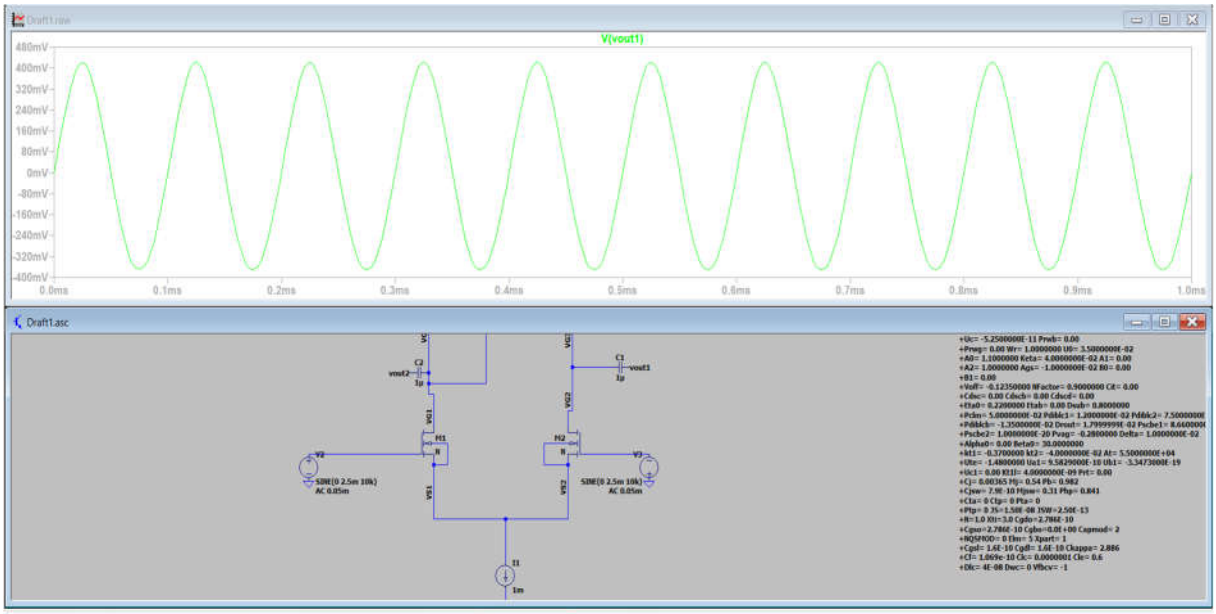
simulation result Vin=0.05 mV



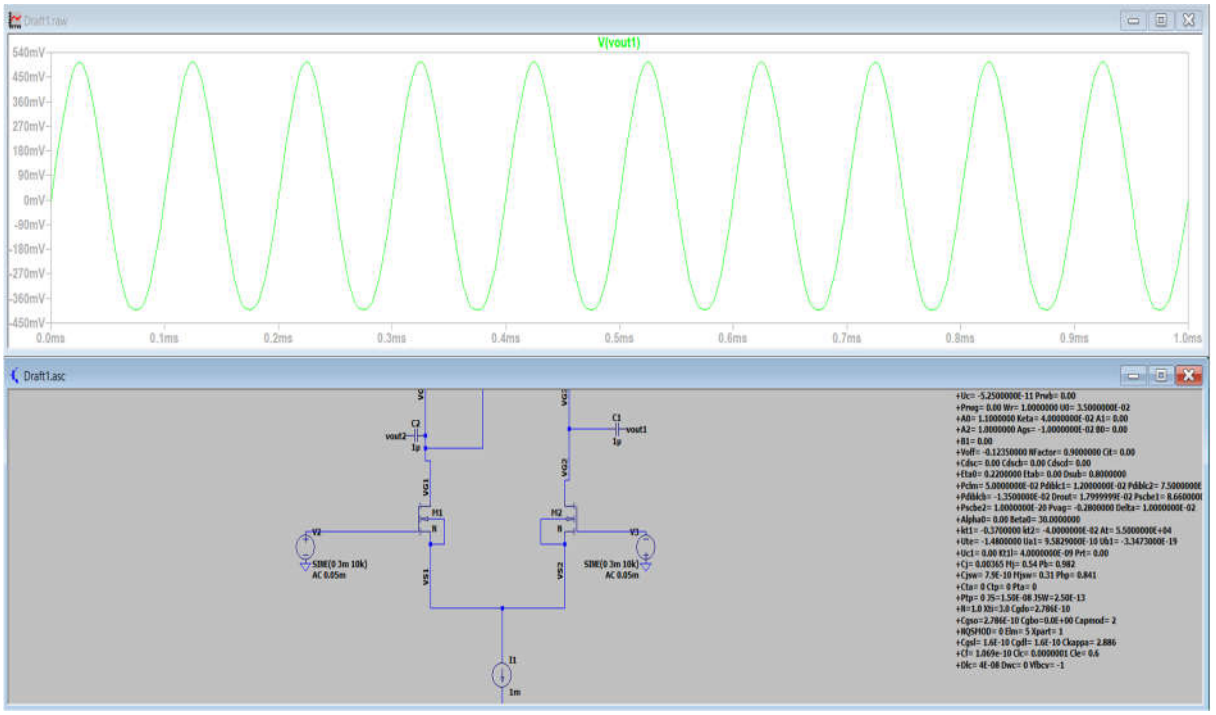
simulation result Vin=1 mV



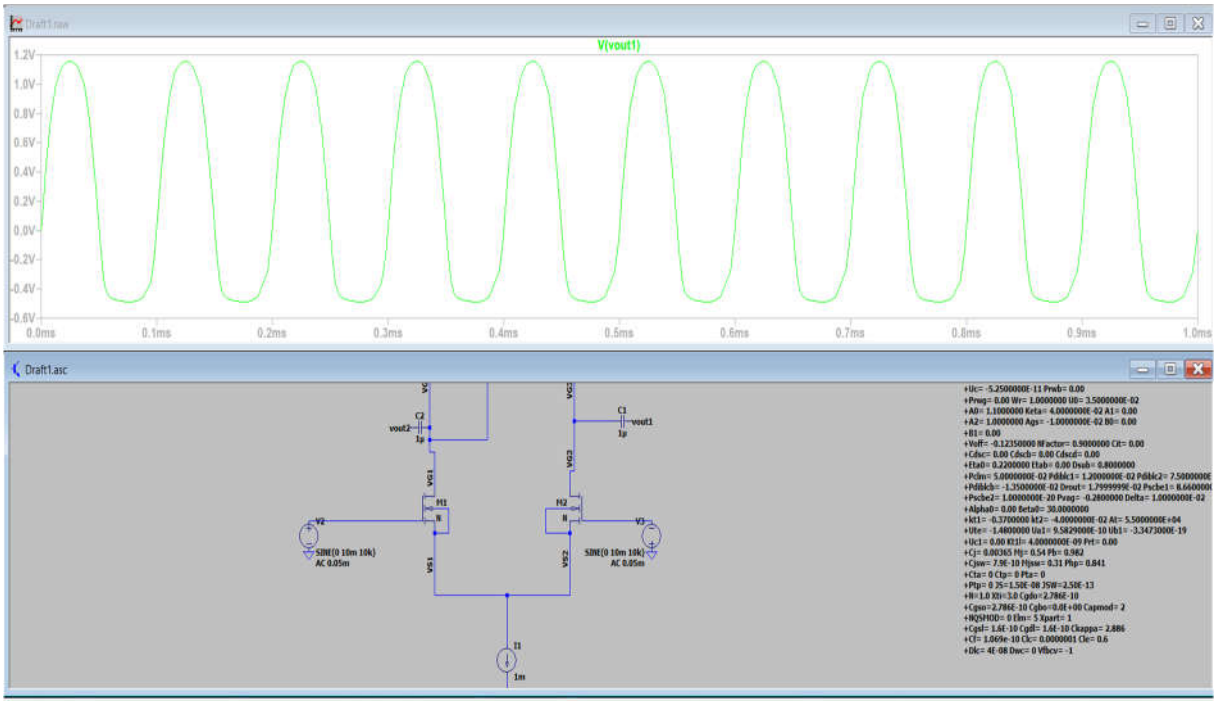
simulation result Vin=2 mV



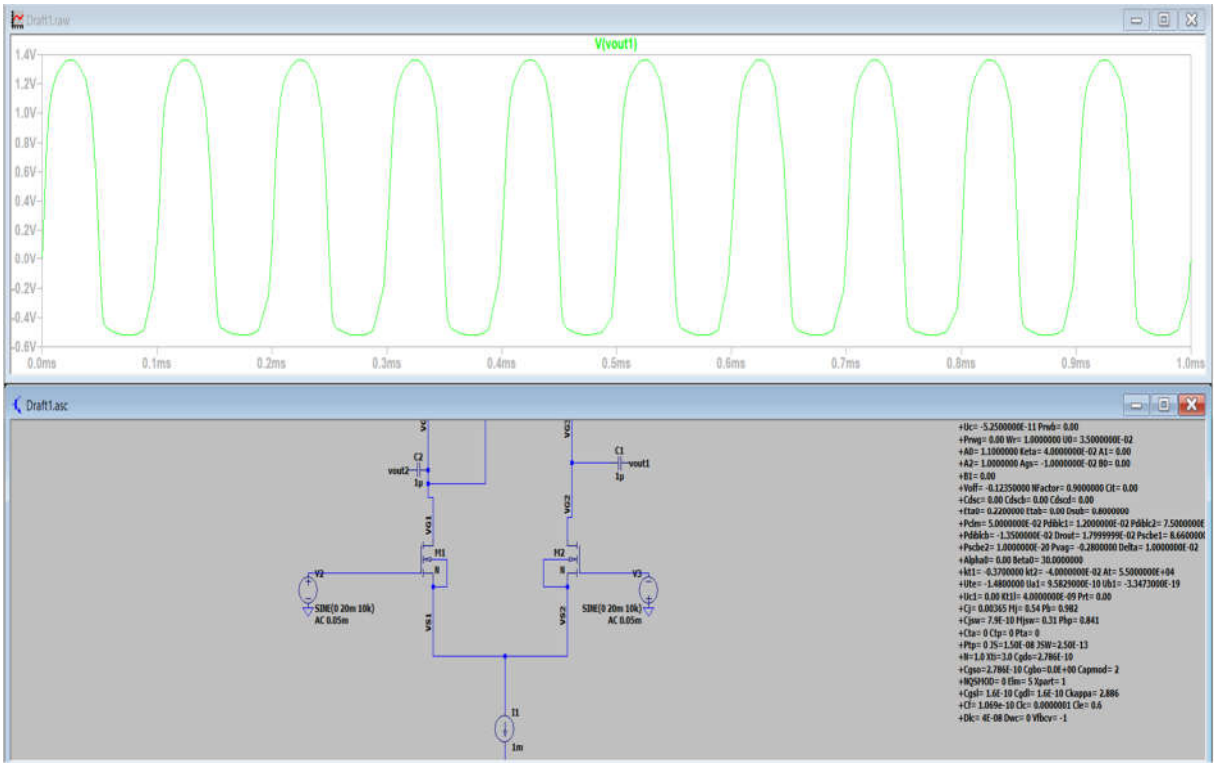
simulation result Vin=3 mV



simulation result Vin=10 mV



simulation result Vin=20 mV



In the simulations, the response of the differential amplifier's output signal to the input signal was analyzed. When the input signal was at 1mV (Vin=1mV), the output signal (Vout1) was observed to be a clean and symmetric sine wave. As the input signal increased up to 2.5mV (Vin=2.5mV), the output signal continued to increase symmetrically. However, when the input signal exceeded 2.5mV, the symmetric nature of the output signal began to deteriorate, and imbalances between the positive and negative amplitudes were observed. Specifically, at an input signal level of 10mV (Vin=10mV), the positive amplitude of the output increased further, while the negative amplitude became limited. When the input signal reached 20mV (Vin=20mV), the output signal clipped in both the positive and negative directions, constrained by the supply voltage (VDD) and ground limits, and the sine wave transformed into a square wave. Furthermore, when the input signal exceeded 20mV, no further increase in the output signal was observed. These observations are attributed to the operating points of the transistors and the input signal amplitude exceeding the supply voltage limits. To achieve a wider linear operating range, the design parameters and transistor sizing should be revisited and appropriately adjusted.

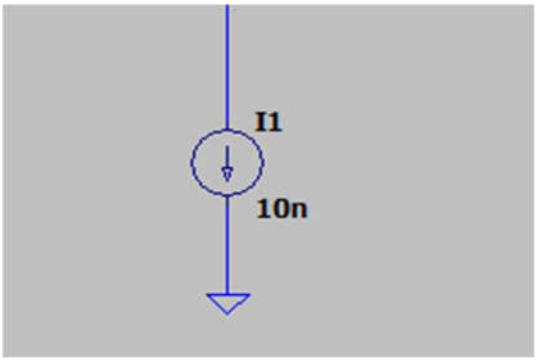
D) Optimization

In order to reduce the circuit's power consumption and improve its energy efficiency, several key design parameters were adjusted. The tail current (I1) was decreased to reduce the overall current consumption of the circuit, while the supply voltage (VDD) was lowered to minimize power dissipation. Additionally, the W/L ratios of the NMOS and PMOS transistors were optimized to balance power efficiency and maintain sufficient transistor performance. These adjustments were necessary to achieve a design suitable for low-power applications, ensuring the circuit operates effectively with reduced energy requirements while maintaining functionality.

1)Optimized Circuit Components

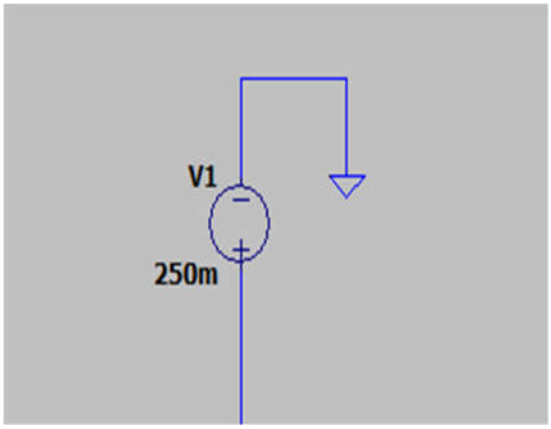
- Tail Current (I1):

Reduced from 1mA to 10nA to significantly lower the overall current consumption and power dissipation of the circuit.



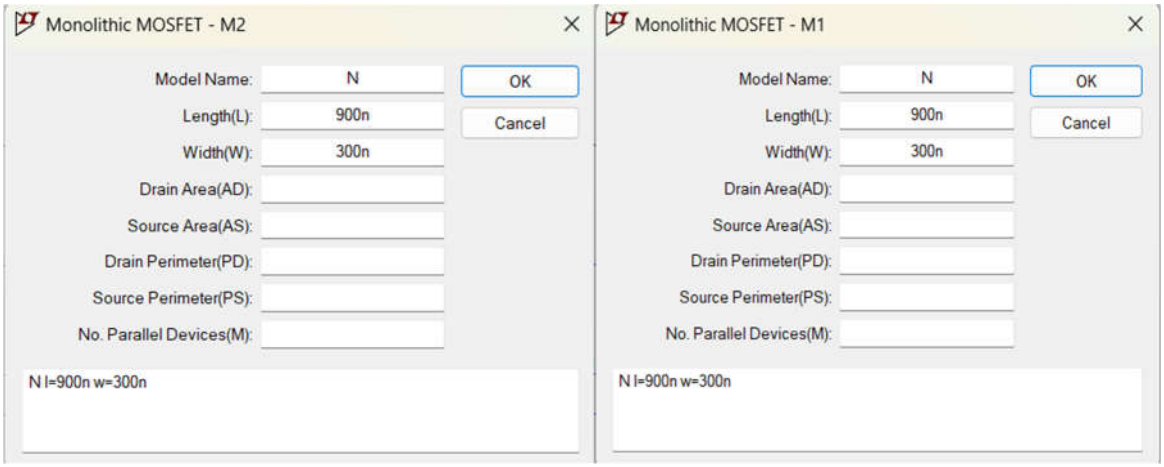
- Supply Voltage (VDD):

Reduced from 1.8V to 0.25V to minimize the power consumed by the circuit while maintaining functionality.



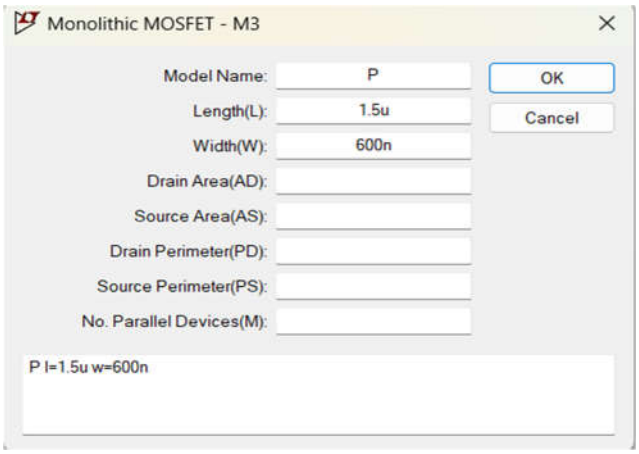
- NMOS Transistors (W/L):

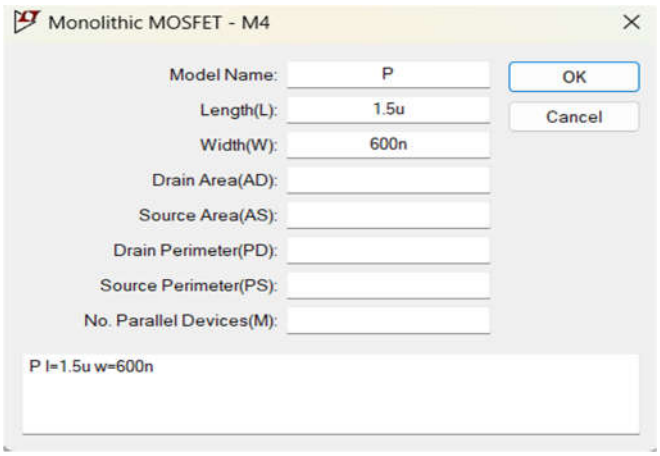
Adjusted from 300u/1u to 900n/300n to optimize transistor performance for lower power consumption.



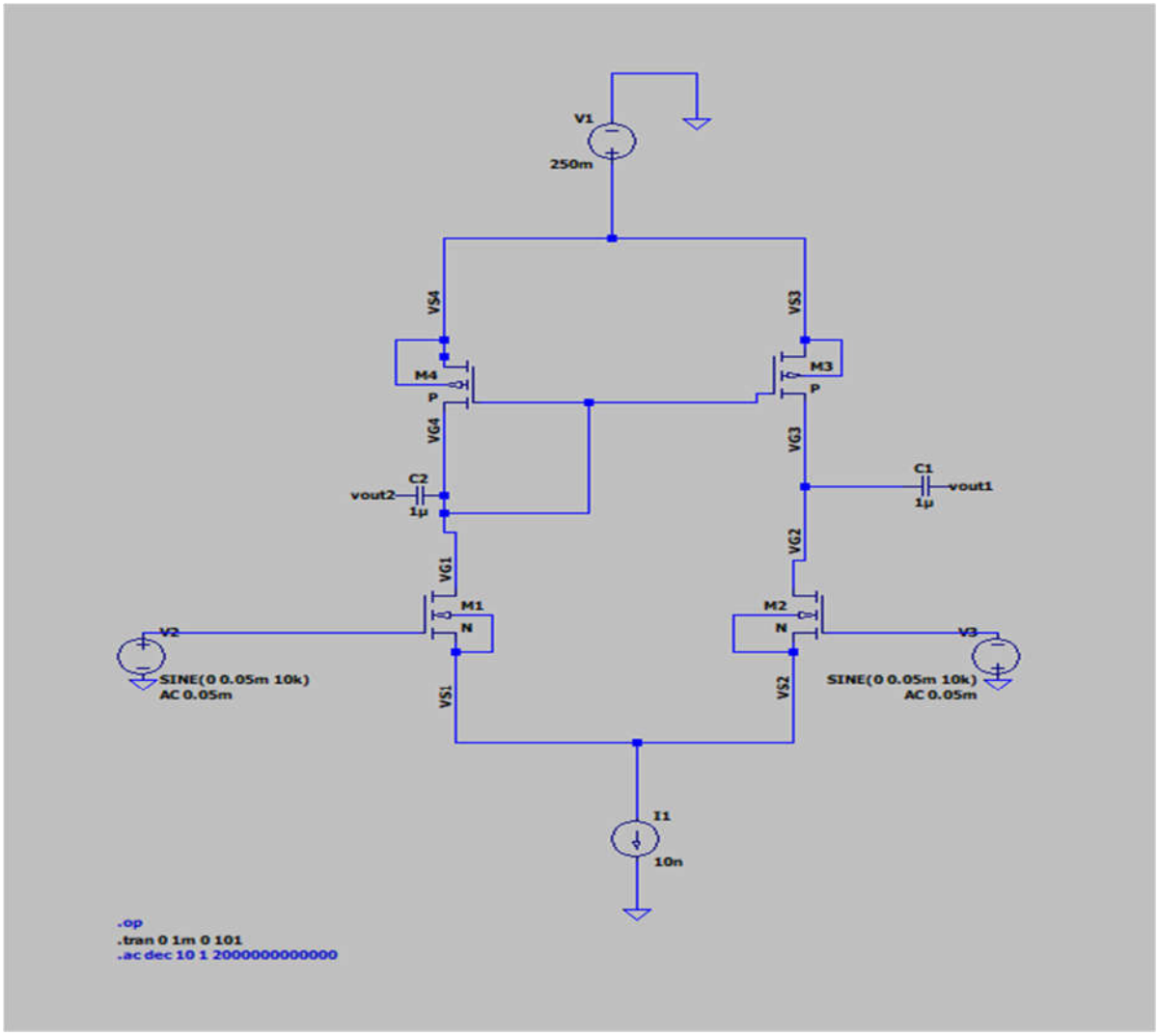
- PMOS Transistors (W/L):

Adjusted from 15u/1u to 1.5u/600n to balance power efficiency with sufficient transistor functionality.





Optimized Circuit Design



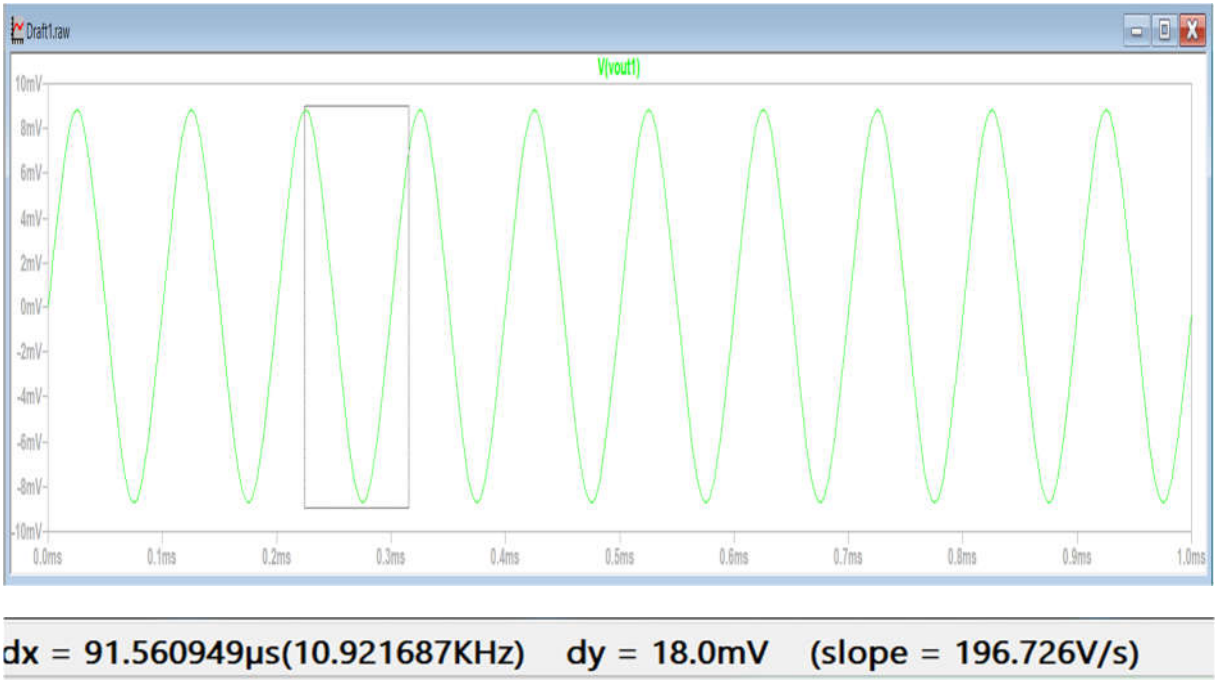
2)Optimized Differential Gain (Ad)

The differential gain (Ad) in the optimized circuit is calculated as 90 V/V. Compared to the initial circuit gain (Ad=87.25V/V), the differential gain shows only a slight increase. This indicates that while power consumption was significantly reduced during the optimization process, the circuit's gain performance remained largely consistent, with minimal changes observed.

$$Ad=((Vout1-Vout2)/(Vin1-Vin2))$$

$$Ad=(18.0mV/0.2mV)=90\ V/V$$

Optimized Differential Gain simulation result



3)Optimized Common-Mode Gain (Acm)

In the optimized circuit, Acm has significantly decreased compared to the initial circuit. In the initial circuit, Acm=7.77×10−6 V/V, while in the optimized circuit, Acm=5.235×10−6 V/V. This reduction indicates that the common-mode signals have less influence on the circuit's output.

The optimizations applied, such as changes in transistor W/L ratios, a reduced VD value, and a decrease in tail current, have lowered the common-mode gain. This makes the circuit less sensitive to common-mode signals and enhances its ability to suppress them. Consequently, the circuit has improved its focus on differential signal processing, which is a critical aspect of its design.

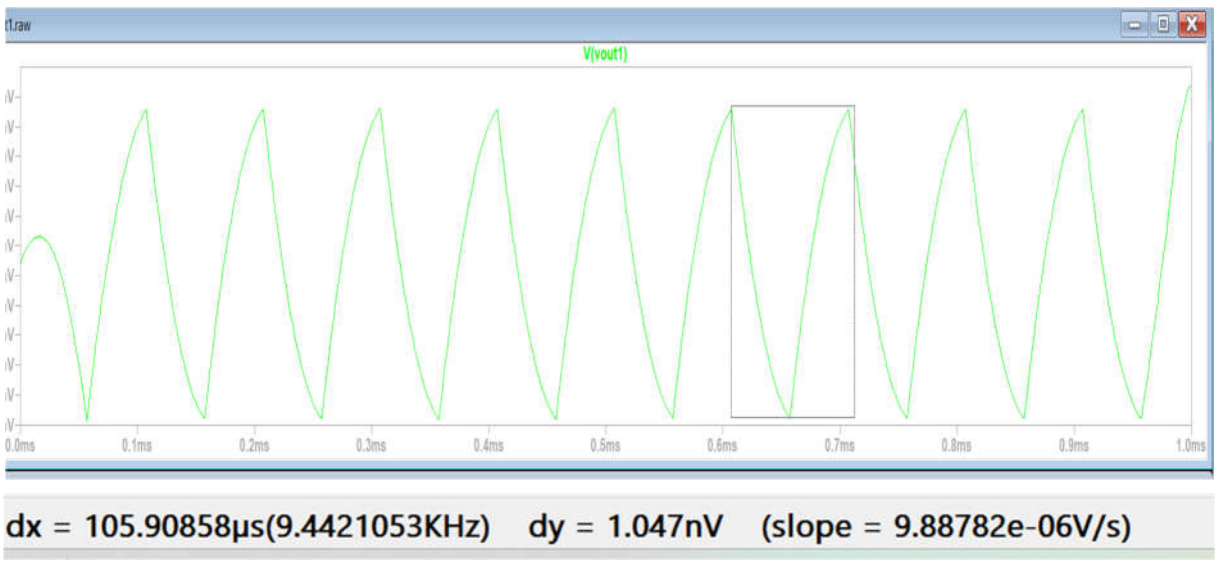
The reduction in Acm demonstrates an important advantage of the optimized circuit: it is less affected by undesired common-mode signals, resulting in better performance in differential amplification.

$$Acm=(Vout1-Vout2)/(Vin1+Vin2)$$

$$(Vout1-Vout2)=1.047nV \text{ and } (Vin1+Vin2)=0.2mV=200\mu V$$

$$Acm=1.047nV/200\mu V=5.235\times10-6\ V/V$$

Optimized Common-Mode Gain simulation result



4)**Optimized CMRR(Common Mode Rejection Ratio) and Bandwidth**

In the optimized circuit, the CMRR value increased from 141 dB to 144.7dB, indicating an improvement in the circuit's ability to suppress common-mode signals. This improvement is associated with a reduction in the common-mode gain (Acm) from 7.77×10−6 V/V to 5.235×10−6 V/V and an increase in the differential gain (Ad) from 87.25 V/V to 90 V/V. The decrease in common-mode gain is a result of better balancing of the transistor W/L ratios, reduced tail current, and improved design symmetry. As a result, the circuit has become more resistant to common-mode signals and improved its differential signal processing capability.

CMRR=20·log(Ad/Acm)

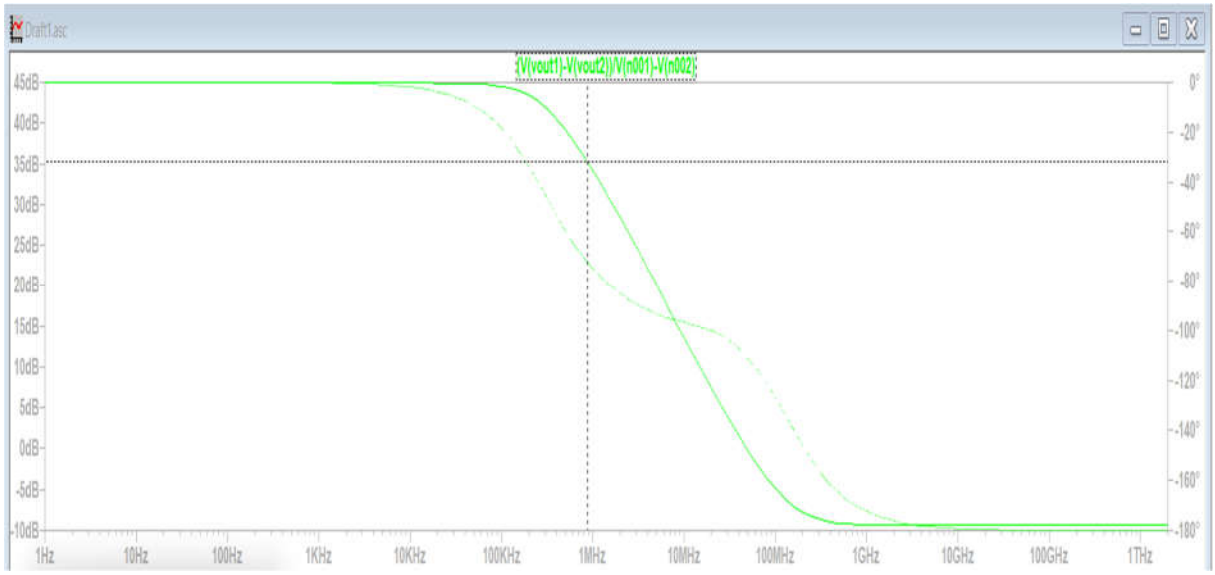
CMRR=20·log(90/5.235×10^−6)=144.7dB

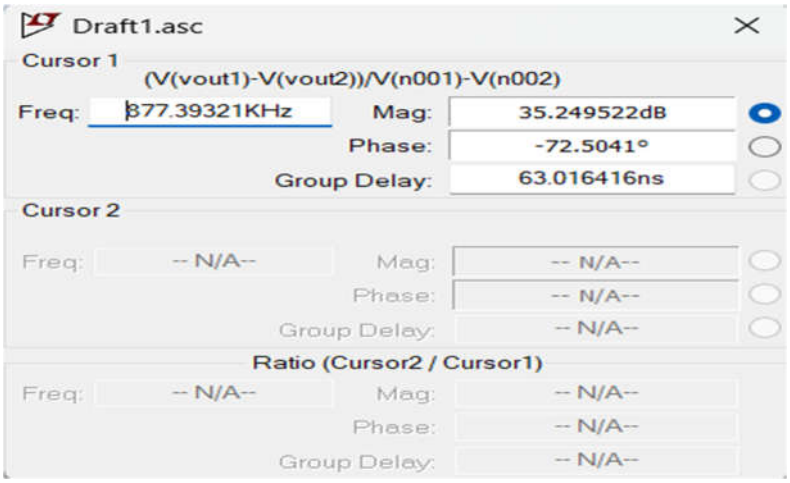
5) **Bandwidth**

As a result of the optimizations applied to the circuit, the bandwidth has decreased. While the bandwidth in the initial circuit was measured as 90 MHz , it has dropped to 877 kHz in the optimized circuit. This reduction is primarily due to the decrease in tail current (I1) and transconductance (gm). The reduction in tail current limits the acceleration capacity of the transistors, while the optimized W/L ratios increase the load capacitance, negatively impacting the bandwidth.

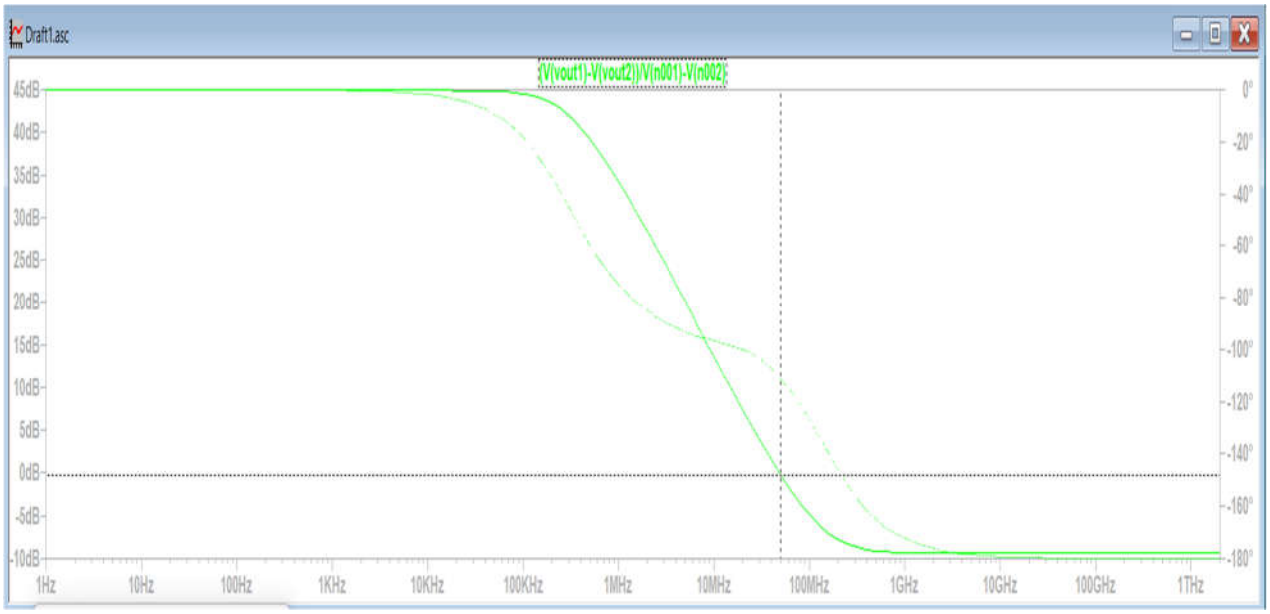
The unity gain frequency has also shifted to a lower value due to these changes. This demonstrates that while the optimized circuit improves energy efficiency, it comes at the cost of trade-offs in high-frequency performance. Consequently, this circuit becomes more suitable for low-power applications, but it may face performance limitations in applications requiring high speed or wide bandwidth.

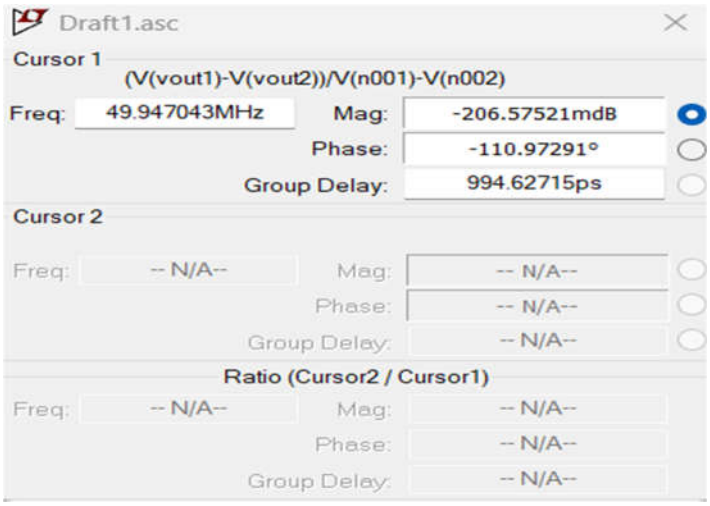
Optimized Bandwidth simulation result





Optimized Unity Gain Bandwidth simulation result





Observation

The optimizations implemented to reduce power consumption in the circuit have resulted in significant changes. The tail current (I1) was reduced from 1mA to 10nA, the supply voltage (VDD) was lowered from 1.8V to 0.25V, and the W/L ratio of the NMOS transistors was adjusted from 1u/300u to 900n/300n, while the PMOS transistors were adjusted from 15u/1u to 1.5µ/600n. These changes reduced the power consumption from 1.8mW to 2.5nW, achieving a reduction of 99.99%. However, these optimizations have resulted in a significant reduction in bandwidth; the initial circuit's bandwidth of 90MHz was reduced to 877kHz in the optimized circuit. This reduction in bandwidth can be attributed to the decrease in tail current, reduced transconductance (gm), slower transistor speeds, and the lower supply voltage.

Following the optimizations, the differential gain (Ad) increased slightly from 87.25V/V to 90V/V. On the other hand, the common-mode gain (Acm) decreased from 7.77×10^−6V/V to 5.235×10^−6V/V. As a result of these changes, the CMRR improved from 141dB to 144.7dB, indicating an enhanced capability of the circuit to suppress common-mode signals. The unity gain frequency was also significantly affected by the optimizations, decreasing substantially, which limits the circuit’s performance at higher frequencies.

The optimizations successfully improved the energy efficiency of the circuit, making it suitable for low-power applications. However, the reductions in bandwidth and high-speed performance demonstrate a clear trade-off between low power consumption and wide bandwidth. This highlights the importance of achieving a balanced optimization depending on the performance goals of the circuit design.

3) Cascode-Loaded Amplifer

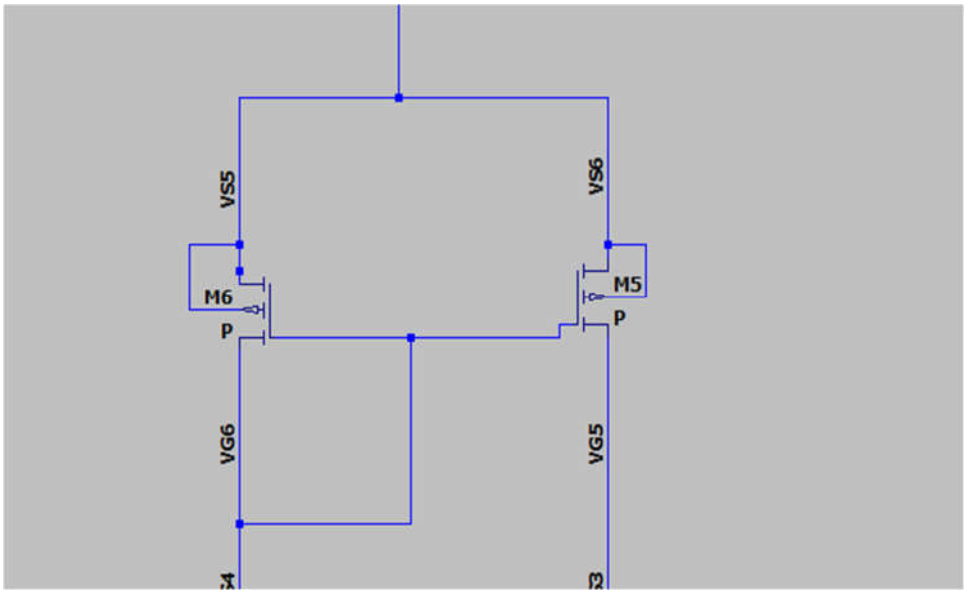
İntroduction

The cascode load configuration has been implemented in the differential amplifier to enhance the output impedance and gain while providing a more stable operation by mitigating the Miller effect. In this design, PMOS transistors (M5 and M6) are added on top of the active load transistors (M3 and M4) and configured as cascode elements. This configuration increases isolation between the output and the load, leading to improvements in gain and operational accuracy.

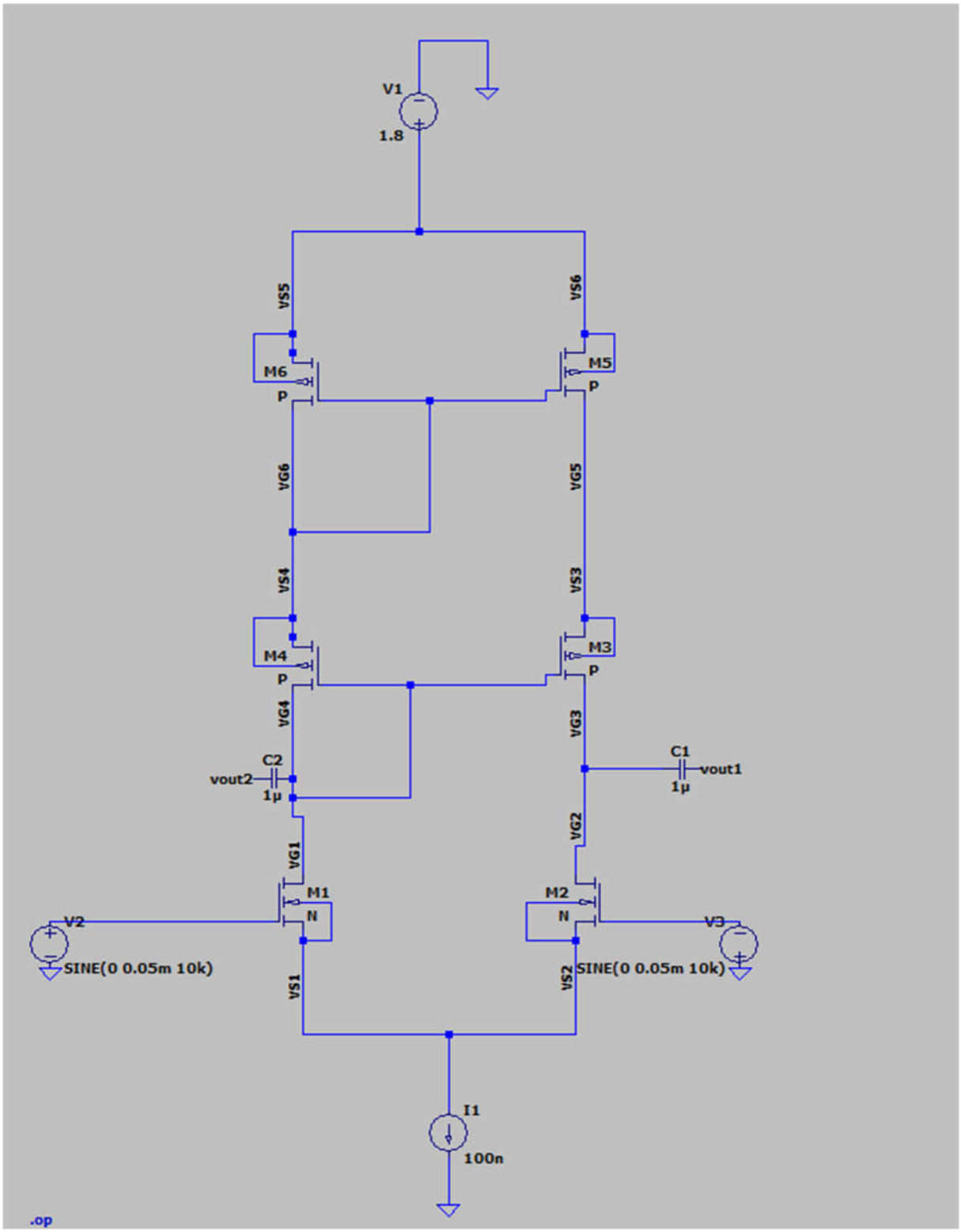
Compared to conventional active load structures, cascode designs offer higher gain and better linear performance. Additionally, the increased output impedance of the cascode structure enhances the common-mode rejection ratio (CMRR) and the differential gain (Ad). However, these advantages often come with trade-offs in terms of increased circuit complexity and a reduction in bandwidth.

The above schematic illustrates the circuit where the cascode load is integrated into the differential amplifier. PMOS transistors M5 and M6 are configured as cascode elements, while M3 and M4 continue to serve as active load elements. In the following sections, key parameters such as Ad, Acm, Rin, $Rout$, CMRR, and bandwidth are analyzed, and comparisons are made with the active load configuration.

Added circuit elements added to the first circuit for cascode



Cascode-loaded amplifier circuit design



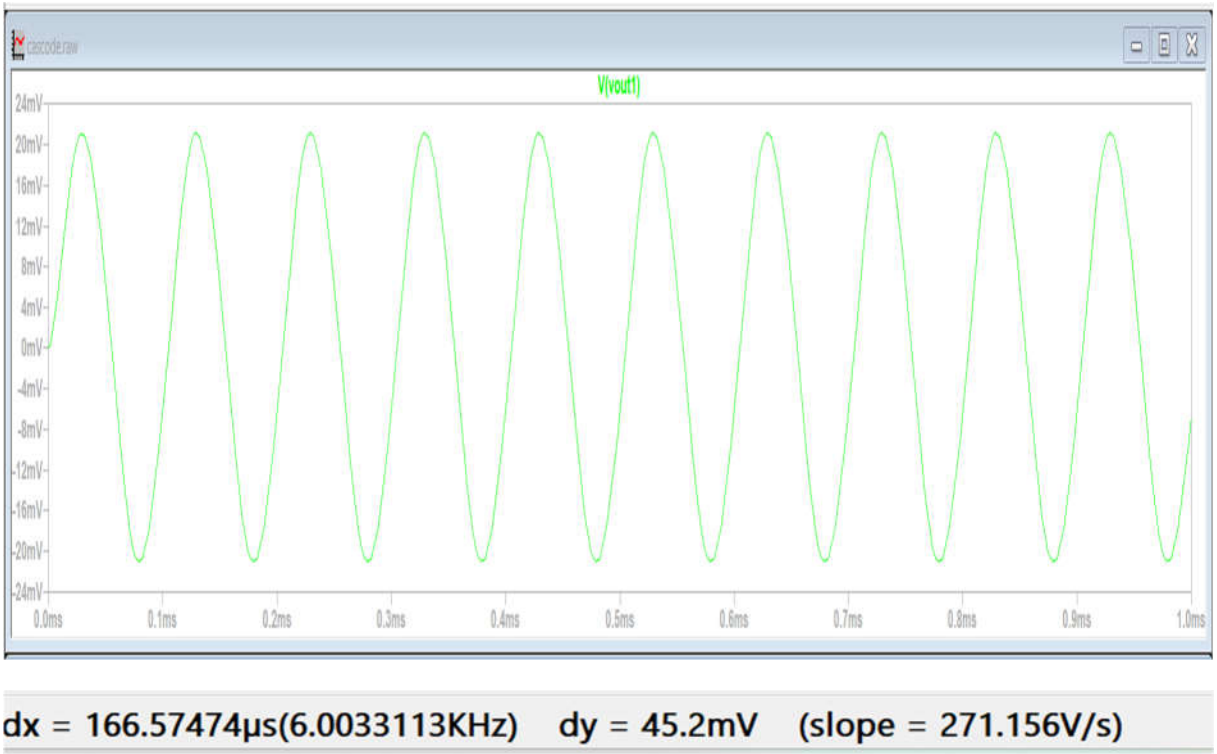
1) Cascode-Loaded Differential Gain (Ad)

In the cascode load configuration, the differential gain (Ad) has shown a significant increase. Differential gain is determined by the formula Ad=gm·Rout, and the increase in output impedance (Rout) provided by the cascode structure directly contributes to the gain improvement. This configuration enhances the isolation between the load and output, reducing the Miller effect and amplifying the impact of transistor output impedance. While the differential gain in the active load design was calculated as Ad=90 V/V , it has increased to Ad=226 V/V in the cascode load design. The primary reason for this increase is the significant enhancement of output impedance achieved by the cascode structure, providing a higher gain. This demonstrates the clear advantage of the cascode structure in applications requiring high gain.

$$Ad=(Vout1-Vout2)/(Vin1-Vin2)$$

$$Ad=45.2mV/0.2mV = 226V/V =47.005\ dB$$

Cascode-Loaded Differential Gain (Ad) simulation result



2) Cascode-Loaded Common Mode Gain (Acm)

In the cascode load configuration, the calculated ACM (common-mode gain) value shows a significant reduction compared to the active load configuration. In the initial circuit, the ACM value was measured as 1.554 nV, while in the cascode configuration, this value decreased to 1.155 nV.

This reduction is primarily due to the cascode structure's ability to increase the output impedance, thereby strengthening the isolation between the load and the signal source. Cascode transistors suppress common-mode signals, reducing their influence within the circuit. The decrease in common-mode gain indicates that the circuit can process differential signals with greater accuracy and is less sensitive to common-mode signals.

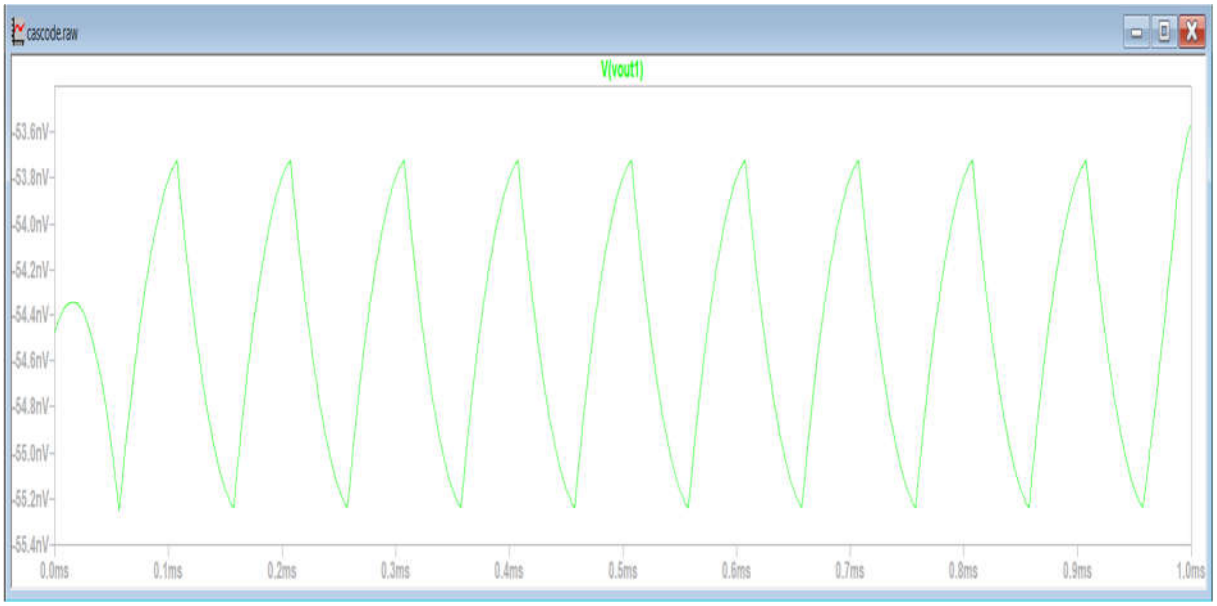
ACM calculation formula:

$$Acm=(Vout1-Vout2)/Vin1+Vin2$$

$$Acm=1.155nV/0.2mV=5.775\times10-^6\ V/V$$

Using this formula, the new ACM value highlights the effects of the increased impedance and improved signal isolation in the cascode structure. This reduction in common-mode gain also contributes to an improvement in CMRR, enhancing the circuit's overall performance.

Cascode-Loaded Common Mode Gain (Acm) simulation result



dx = 98.169717µs(10.186441KHz) dy = 1.155nV (slope = 1.17682e-05V/s)

3) Cascode-Loaded CMRR

The Cascode Loaded CMRR calculation reveals a significant improvement compared to the Active Load configuration. Initially, the Active Load circuit had a CMRR of 141.0 dB, with Ad=87.25 V/V and Acm=7.77×10−6 V/V. In the Cascode Loaded configuration, the differential gain (Ad) increased to 226 V/V, and the common-mode gain (Acm) decreased to 5.775×10^−6 V/V, resulting in a CMRR of 151.84 dB, an increase of 10.84 . This improvement is attributed to the higher output impedance provided by the cascode structure, which enhances differential gain, and the better isolation that reduces common-mode effects, thereby decreasing Acm. Overall, the cascode configuration demonstrates superior common-mode signal suppression and improved differential signal performance.

$$\text{CMRR}=20\log10(\text{Ad}/\text{Acm})$$

$$\text{CMRR}=20\cdot\log(226/5.775\times10\text{^}-6)$$

$$\text{CMRR}=20\cdot\log(3.913\times107)$$

$$\text{CMRR}=20\cdot7.592\approx151.84\text{dB}$$

4) Cascode-Loaded Rin-Rout

Rin

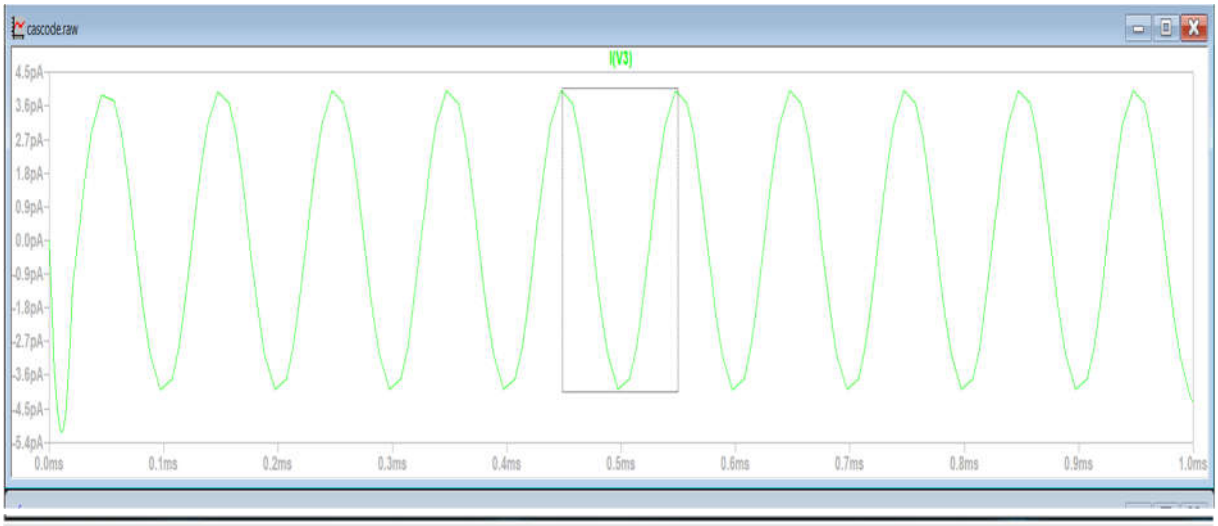
In the cascode load configuration, the input resistance (Rin) has not shown significant variation compared to the active load configuration. For the active load configuration, Rin=10.53MΩ, while in the cascode load configuration, Rin=12.31 MΩ. This slight increase indicates that the cascode structure has a limited impact on the input resistance. The value of Rin is primarily determined by the W/L ratios of the input transistors and the input circuit parameters. Consequently, a configuration like the cascode load, which primarily aims to enhance the output impedance, is not expected to significantly affect Rin. The relatively constant Rin supports the notion that the cascode structure is designed to improve the output impedance while maintaining input characteristics.

$$\text{Rin}=\text{Vin}/\text{Iin}$$

$$\text{Rin}=(0.1\times10\text{^}-3)/(8.12\times10\text{^}-12)=12.31\text{MΩ}$$

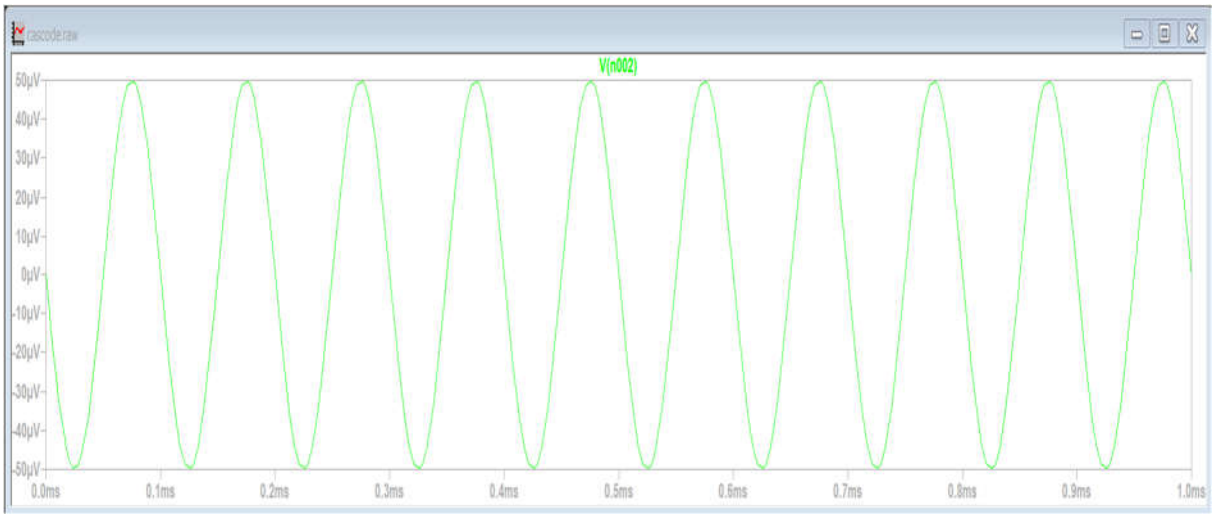
Rin Cascode-Loaded simulation result

IİN



dx = 101.54525µs(9.8478261KHz) dy = 8.12pA (slope = 7.99325e-08A/s)

VİN



dx = 125.48156µs(7.9692982KHz) dy = 100.0µV (slope = 0.79693V/s)

Rout

The Rout value for the cascode load configuration has been calculated. Rout is defined as the ratio of the output voltage to the output current:

$$Rout=Vout/Iout$$

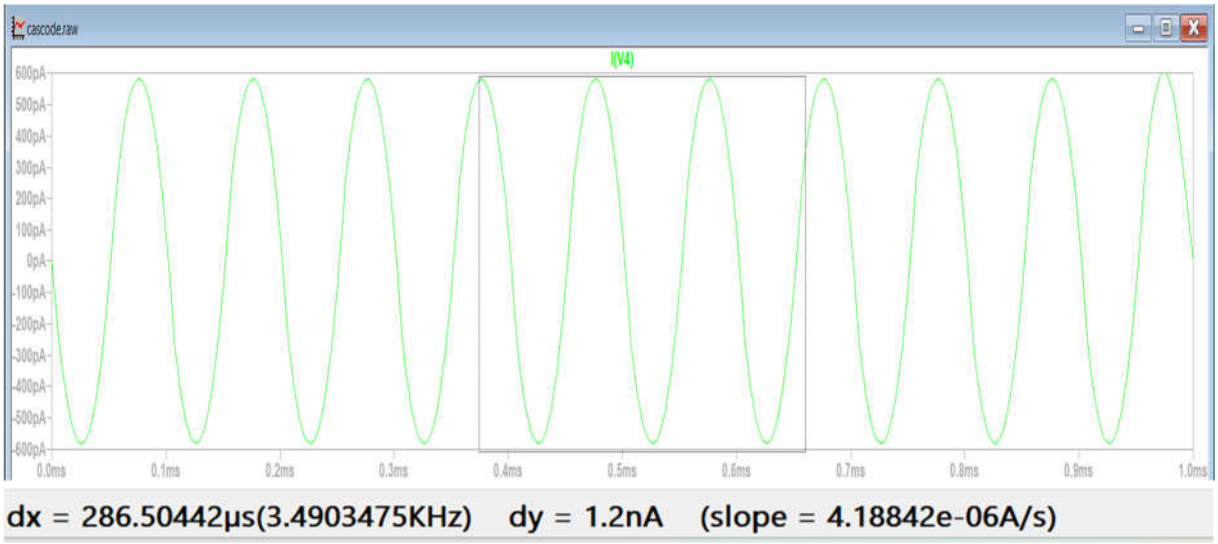
According to the simulation data, Vout=0.1 mV and Iout=1.2 nA. Using these values:

$$Rout=0.1\ Mv/1.2\ nA=83.33\ k\Omega$$

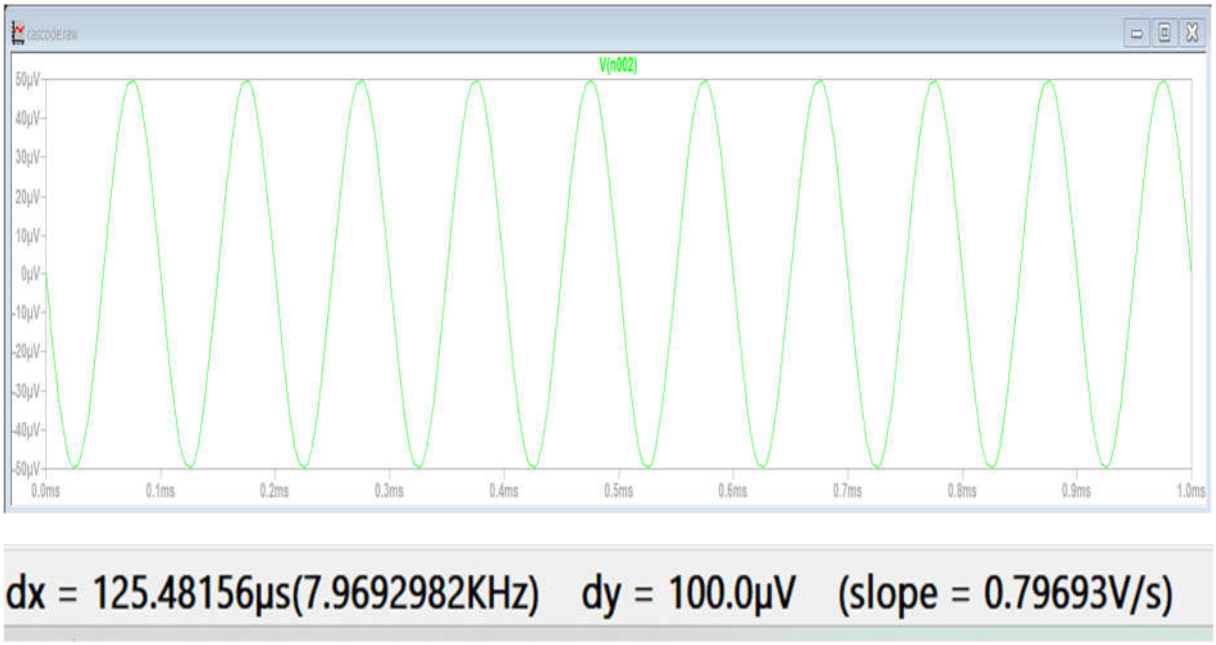
The Rout value has significantly increased in the cascode configuration. In the active load configuration, Rout≈11.76kΩ was measured. The cascode structure enhances the output impedance due to the high intrinsic resistance provided by the cascode transistors. This improvement arises because the cascode configuration effectively isolates the output node from the parasitic capacitances, leading to a much higher overall output resistance.The increased output resistance in the cascode structure contributes to higher differential gain and improved accuracy in signal processing. This makes the cascode design more suitable for applications requiring high precision and gain.

Rout Cascode-Loaded simulation result

Iout



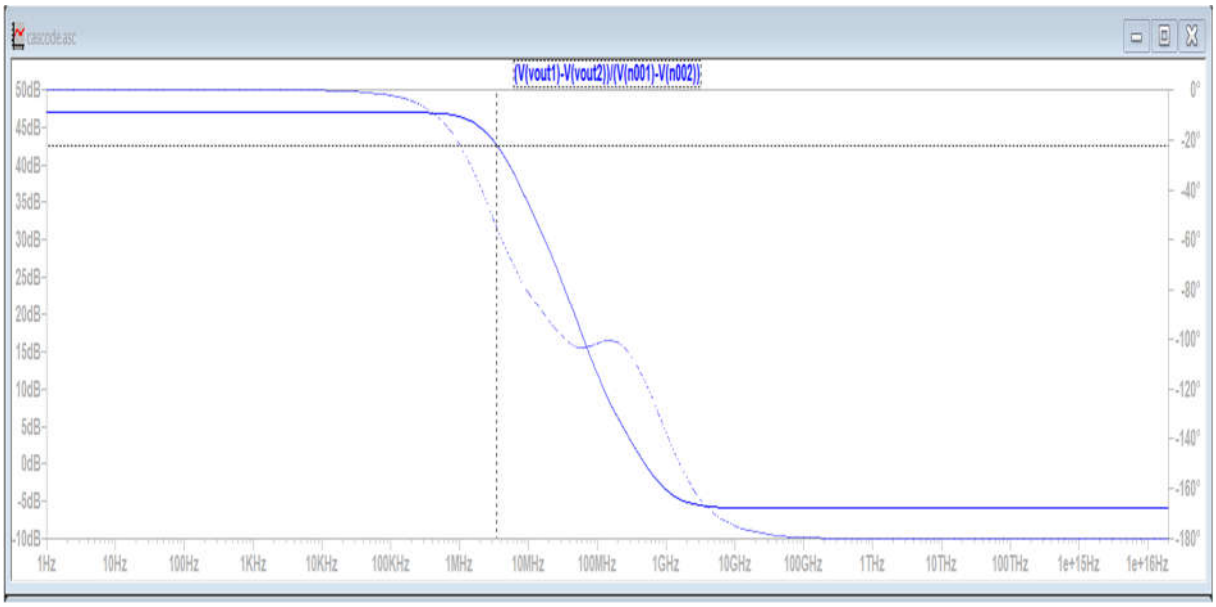
Vout

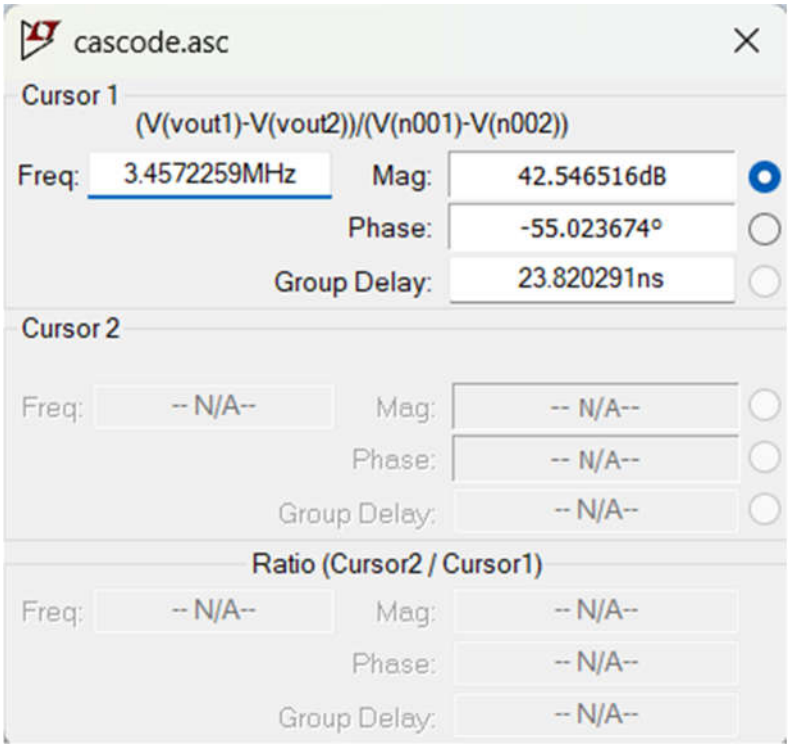


4) Cascode-Loaded Bandwidth

The cascode load design resulted in a measured bandwidth (BW) of 3.45 MHz, with a noticeable reduction observed. This decrease is attributed to the cascode configuration significantly increasing the output impedance (Rout), which, in combination with the load capacitance (Cout), raises the circuit's time constant (Rout·Cout). Additionally, while the cascode structure provides higher gain and improved accuracy, it introduces a trade-off by negatively impacting the bandwidth. Consequently, the cascode design compromises bandwidth performance to achieve enhancements in gain and precision.

Cascode-Loaded Bandwidth Simulation Result





Observation

The implementation of the cascode load configuration has led to significant changes in the performance parameters of the circuit compared to the active load design. The differential gain (Ad) has increased considerably due to the rise in output impedance (Rout), as described by the relationship Ad=gm·Rout. Similarly, the common-mode rejection ratio (CMRR) has improved as a result of the reduction in common-mode gain (Acm) and the higher output impedance provided by the cascode configuration, allowing for better suppression of common-mode signals.

However, this optimization has introduced trade-offs, particularly affecting bandwidth (BW) and input impedance (Rin). Bandwidth has significantly decreased due to the increase in Rout, which, combined with the load capacitance (Cout), increases the time constant of the circuit. The input impedance (Rin), on the other hand, has remained largely unchanged, as the cascode load primarily impacts the output stage and has limited influence on the input stage.

Overall, the cascode load configuration has enhanced gain, CMRR, and output impedance while reducing bandwidth and frequency response. This highlights the inherent trade-offs in analog circuit design, where achieving high gain and precision often requires a balance between bandwidth and frequency performance.

References

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5. "Understanding Cascode Load in Differential Amplifiers" (Video). https://www.youtube.com/watch?v=_qKFQ1H_zOI
6. "Cascode Load Design in MOSFET Differential Amplifiers" (Video). https://www.youtube.com/watch?v=Qn_ghWdCSyo