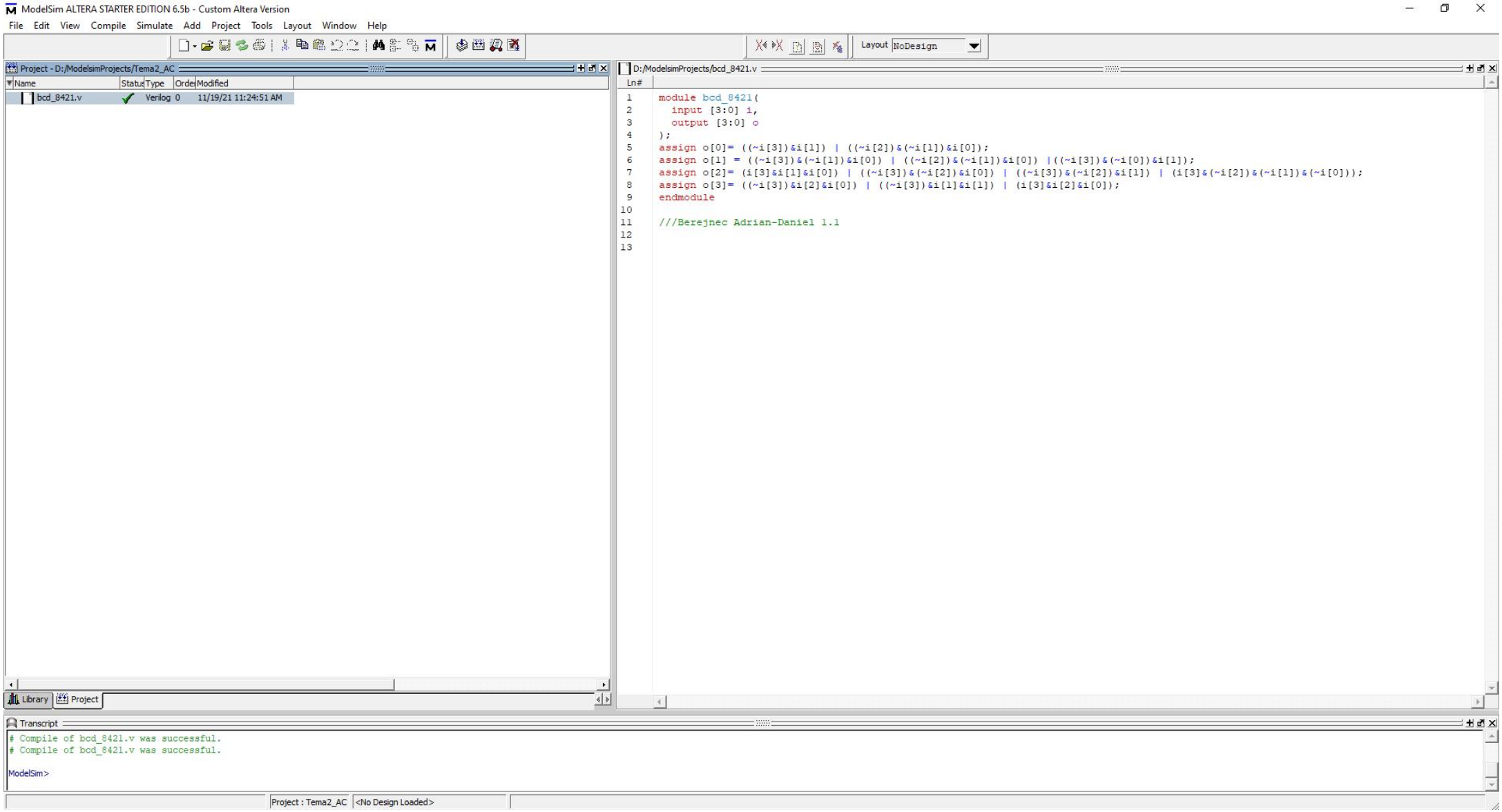
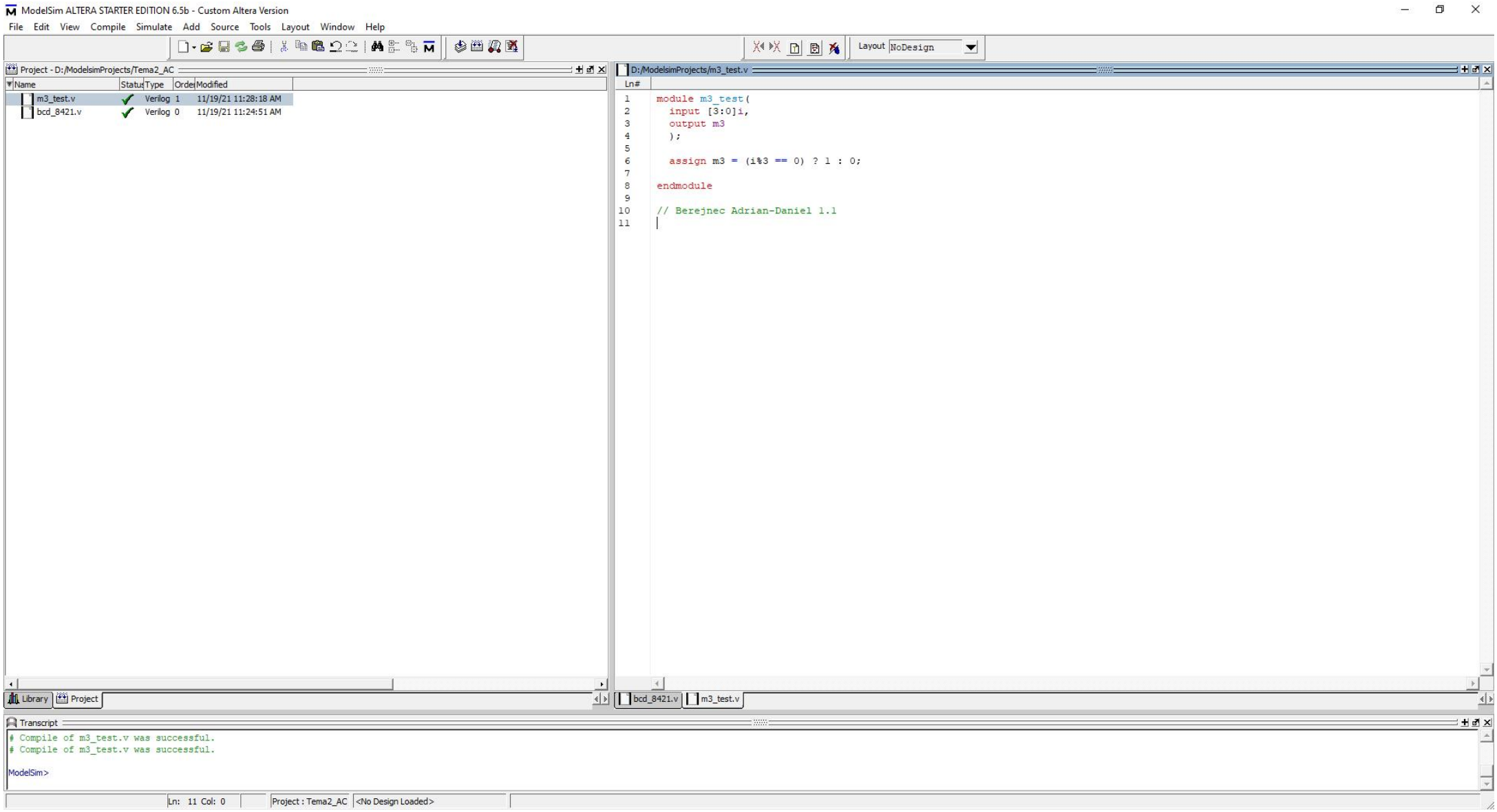
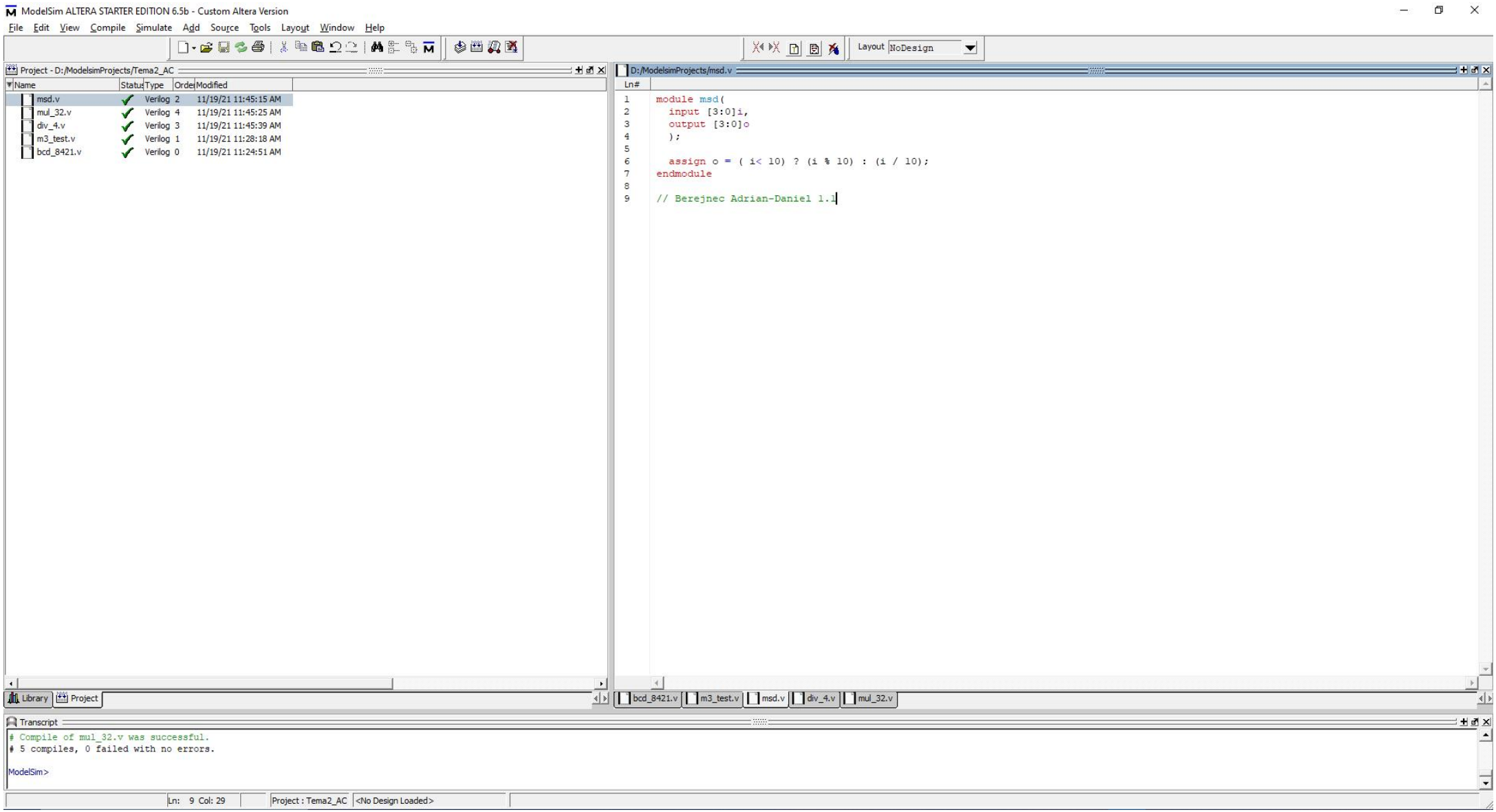
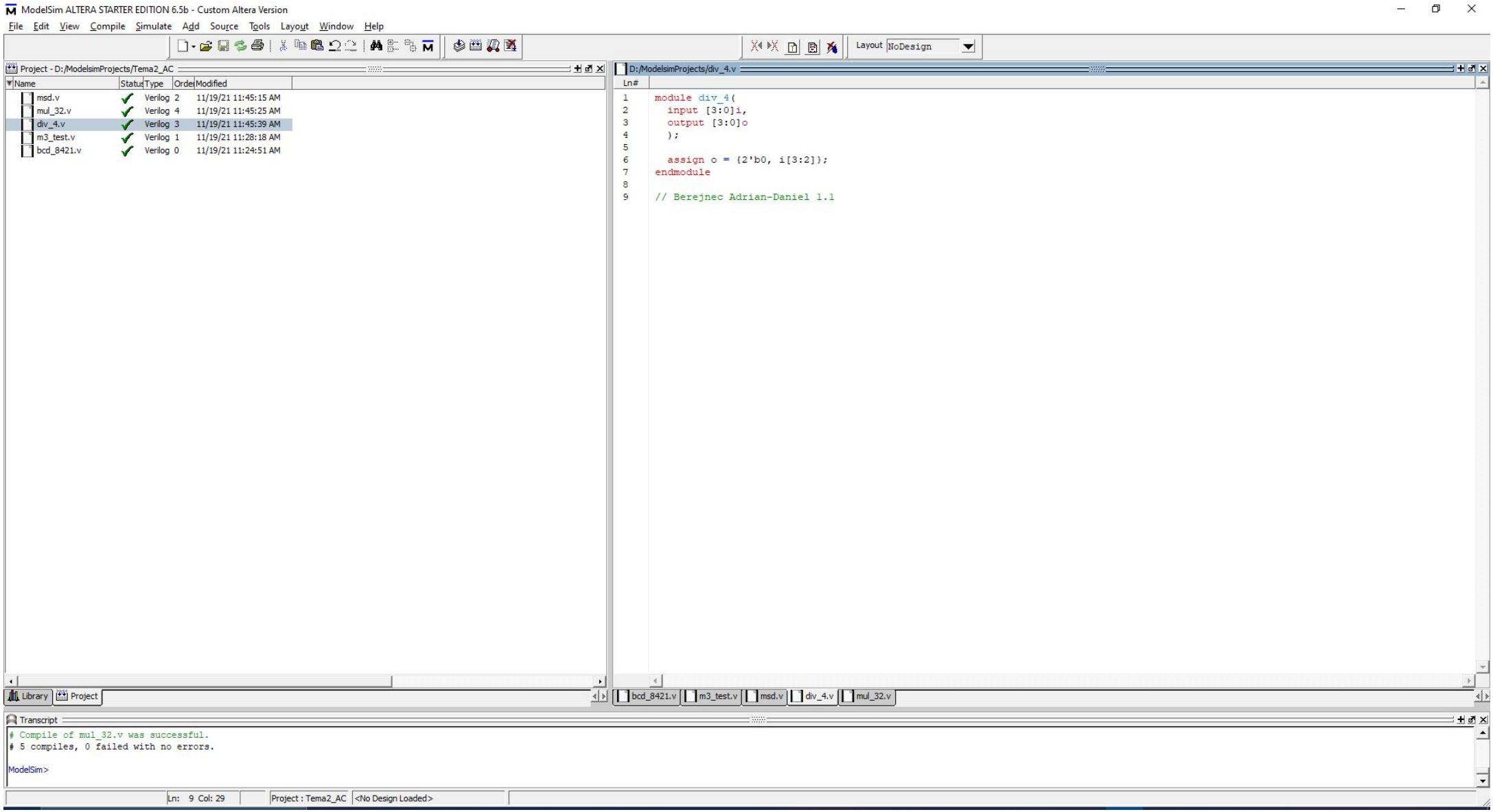
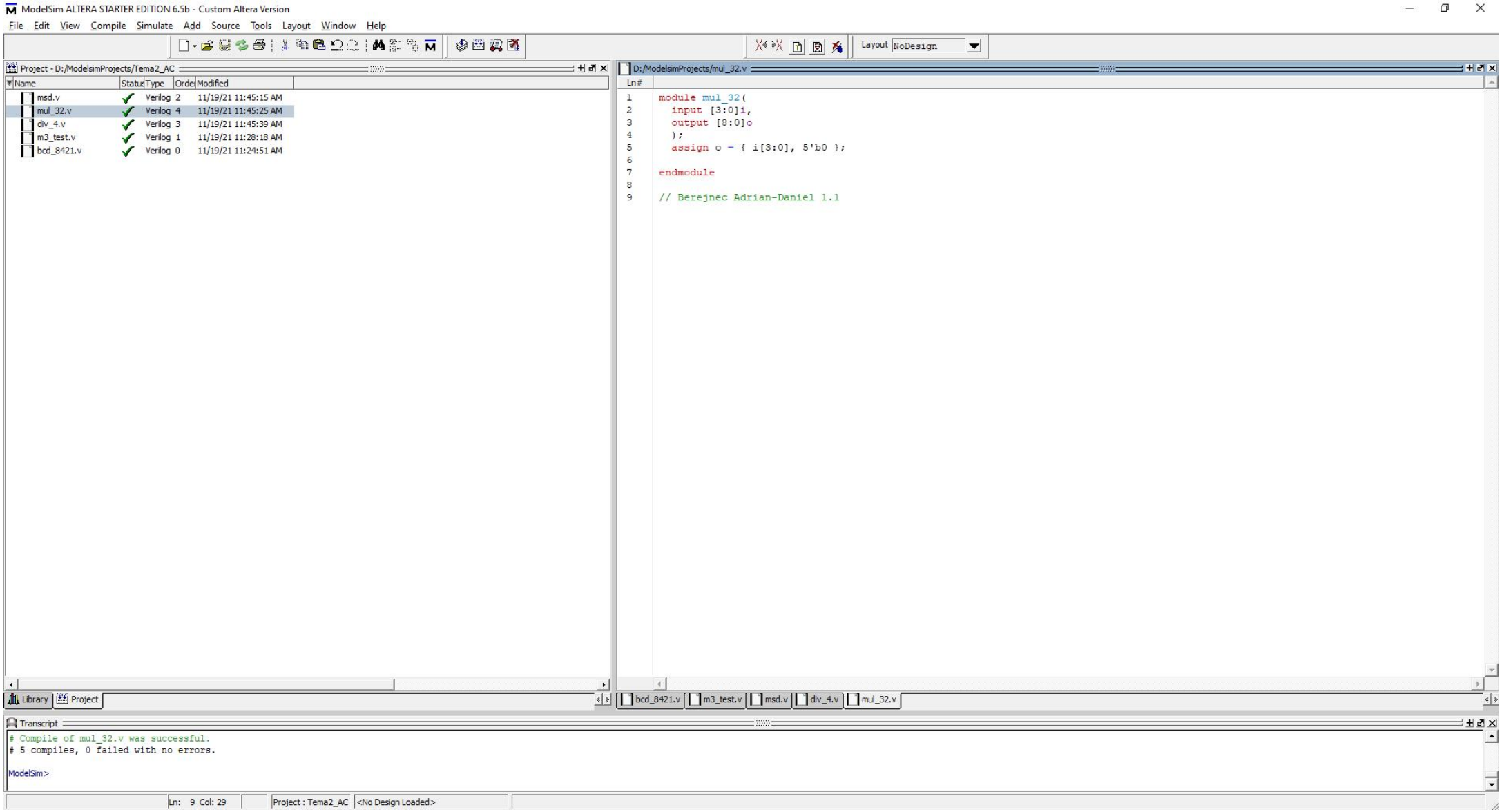

ModelSim ALTERA STARTER EDITION 6.5b - Custom Altera Version
File Edit View Compile Simulate Add Project Tools Layout Window Help
Layout NoDesign
Project - D:/ModelsimProjects/Tema2_AC
Name Status Type Order Modified
bcd_8421.v Verilog 0 11/19/21 11:24:51 AM
Library Project
D:/ModelsimProjects/bcd_8421.v
Ln#
1 module bcd_8421(
2 input [3:0] i,
3 output [3:0] o
4);
5 assign o[0]= ((~i[3])&i[1]) | ((~i[2])&(~i[1])&i[0]);
6 assign o[1] = ((~i[3])&(~i[1])&i[0]) | ((~i[2])&(~i[1])&i[0]) |((~i[3])&(~i[0])&i[1]);
7 assign o[2]= (i[3]&i[1]&i[0]) | ((~i[3])&(~i[2])&i[0]) | ((~i[3])&(~i[2])&i[1]) | (i[3]&(~i[2])&(~i[1])&(~i[0]));
8 assign o[3]= ((~i[3])&i[2]&i[0]) | ((~i[3])&i[1]&i[1]) | (i[3]&i[2]&i[0]);
9 endmodule
10
11 ///Berejnec Adrian-Daniel 1.1
12
13
Transcript
Compile of bcd_8421.v was successful.
Compile of bcd_8421.v was successful.
ModelSim>
Project : Tema2_AC
<No Design Loaded>


ModelSim ALTERA STARTER EDITION 6.5b - Custom Altera Version
File Edit View Compile Simulate Add Source Tools Layout Window Help
Layout NoDesign
Project - D:/ModelsimProjects/Tema2_AC
Name Status Type Order Modified
m3_test.v Verilog 1 11/19/21 11:28:18 AM
bcd_8421.v Verilog 0 11/19/21 11:24:51 AM
Library Project
D:/ModelsimProjects/m3_test.v
Ln#
1 module m3_test(
2 input [3:0]i,
3 output m3
4);
5
6 assign m3 = (i%3 == 0) ? 1 : 0;
7
8 endmodule
9
10 // Berejnec Adrian-Daniel 1.1
11
bcd_8421.v m3_test.v
Transcript
Compile of m3_test.v was successful.
Compile of m3_test.v was successful.
ModelSim>
Ln: 11 Col: 0
Project : Tema2_AC
<No Design Loaded>


ModelSim ALTERA STARTER EDITION 6.5b - Custom Altera Version
File Edit View Compile Simulate Add Source Tools Layout Window Help
Layout NoDesign
Project - D:/ModelsimProjects/Tema2_AC
Name Status Type Order Modified
msd.v Verilog 2 11/19/21 11:45:15 AM
mul_32.v Verilog 4 11/19/21 11:45:25 AM
div_4.v Verilog 3 11/19/21 11:45:39 AM
m3_test.v Verilog 1 11/19/21 11:28:18 AM
bcd_8421.v Verilog 0 11/19/21 11:24:51 AM
Library Project
D:/ModelsimProjects/msd.v
Ln#
1 module msd(
2 input [3:0]i,
3 output [3:0]o
4);
5
6 assign o = (i< 10) ? (i % 10) : (i / 10);
7 endmodule
8
9 // Berejnec Adrian-Daniel 1.1
bcd_8421.v m3_test.v msd.v div_4.v mul_32.v
Transcript
Compile of mul_32.v was successful.
5 compiles, 0 failed with no errors.
ModelSim>
Ln: 9 Col: 29
Project : Tema2_AC
<No Design Loaded>


ModelSim ALTERA STARTER EDITION 6.5b - Custom Altera Version
File Edit View Compile Simulate Add Source Tools Layout Window Help
Layout NoDesign
Project - D:/ModelsimProjects/Tema2_AC
Name Status Type Order Modified
msd.v Verilog 2 11/19/21 11:45:15 AM
mul_32.v Verilog 4 11/19/21 11:45:25 AM
div_4.v Verilog 3 11/19/21 11:45:39 AM
m3_test.v Verilog 1 11/19/21 11:28:18 AM
bcd_8421.v Verilog 0 11/19/21 11:24:51 AM
Library Project
D:/ModelsimProjects/div_4.v
Ln#
1 module div_4(
2 input [3:0]i,
3 output [3:0]o
4);
5
6 assign o = {2'b0, i[3:2]};
7 endmodule
8
9 // Berejnec Adrian-Daniel 1.1
bcd_8421.v m3_test.v msd.v div_4.v mul_32.v
Transcript
Compile of mul_32.v was successful.
5 compiles, 0 failed with no errors.
ModelSim>
Ln: 9 Col: 29
Project : Tema2_AC
<No Design Loaded>


ModelSim ALTERA STARTER EDITION 6.5b - Custom Altera Version
File Edit View Compile Simulate Add Source Tools Layout Window Help
Layout NoDesign
Project - D:/ModelsimProjects/Tema2_AC
Name Status Type Order Modified
msd.v Verilog 2 11/19/21 11:45:15 AM
mul_32.v Verilog 4 11/19/21 11:45:25 AM
div_4.v Verilog 3 11/19/21 11:45:39 AM
m3_test.v Verilog 1 11/19/21 11:28:18 AM
bcd_8421.v Verilog 0 11/19/21 11:24:51 AM
Library Project
D:/ModelsimProjects/mul_32.v
Ln#
1 module mul_32(
2 input [3:0]i,
3 output [8:0]o
4);
5 assign o = { i[3:0], 5'b0 };
6
7 endmodule
8
9 // Berejnec Adrian-Daniel 1.1
bcd_8421.v m3_test.v msd.v div_4.v mul_32.v
Transcript
Compile of mul_32.v was successful.
5 compiles, 0 failed with no errors.
ModelSim>
Ln: 9 Col: 29
Project : Tema2_AC
<No Design Loaded>