Berejnec Adrian-Daniel 1.1

Ex 1:

a)

D:/ModelsimProjects/mux_2s.v

```
Ln#
 1  module mux_2s # (
 2    parameter w = 4
 3    ) (
 4        input [w-1:0] d0, d1, d2, d3,
 5        input [1:0] s,
 6        output reg [w-1:0] o
 7        );
 8
 9      always @ (*) begin
10        case(s)
11          2'b00: o <= d0;
12          2'b01: o <= d1;
13          2'b10: o <= d2;
14          2'b11: o <= d3;
15        endcase
16      end
17    endmodule
```

b)

D:/ModelsimProjects/mux_2s_tb.v

```
Ln#
 1  module mux_2s_tb # ( parameter w = 4) (
 2    output reg [w-1:0] d0,d1,d2,d3,
 3    output reg [1:0] s,
 4    output [w-1:0] o
 5    );
 6
 7    mux_2s # (.w(4)) DUT (
 8        .d0(d0),
 9        .d1(d1),
10        .d2(d2),
11        .d3(d3),
12        .s(s),
13        .o(o)
14        );
15
16      integer i;
17      initial begin
18        s = 6'd0;
19        d0 = 6'd0;
20        d1 = 6'd0;
21        d2 = 6'd0;
22        d3 = 6'd0;
23        for(i = 0;i < 64; i = i + 1)
24         #50 s = 6'd0;
25         #50 d0 = 6'd0;
26         #50 d1 = 6'd0;
27         #50 d2 = 6'd0;
28         #50 d3 = 6'd0;
29        end
30      endmodule
31
```

Ex 2 :

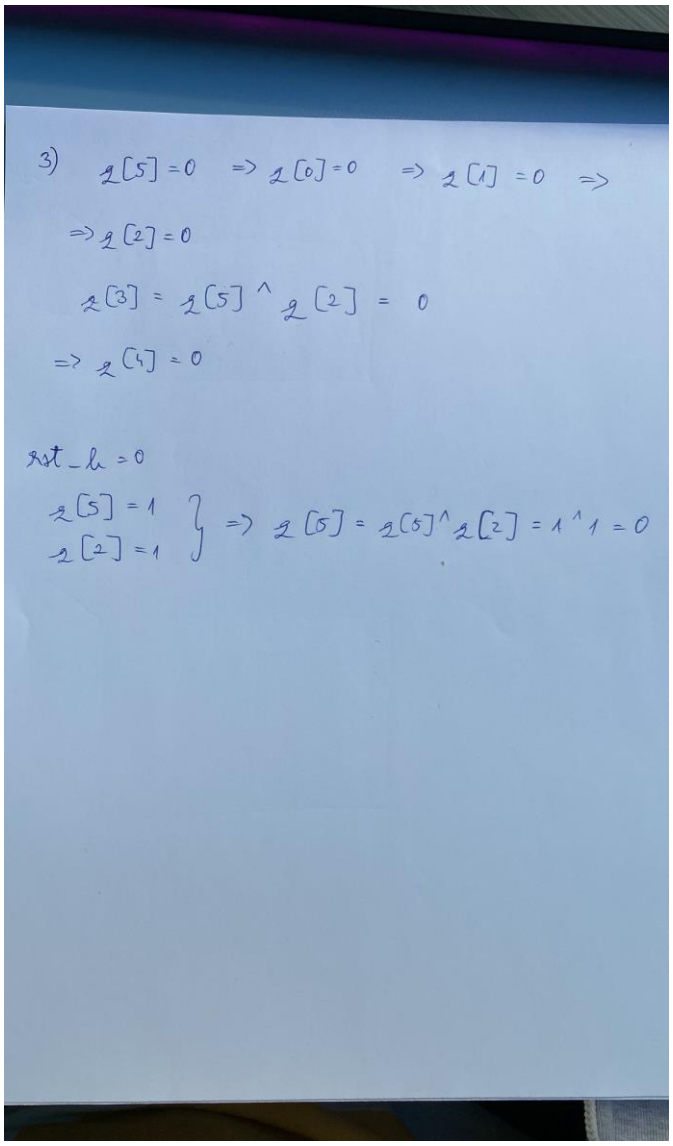
b)

D:/ModelsimProjects/minimization.v

```
Ln#
 1  module minimization (
 2    input [3:0] i,
 3    output [1:0] o
 4    );
 5
 6    assign o[0] = i[0];
 7    assign o[1] = ~i[0];
 8
 9  endmodule;
10
```

Ex 3:

a)



b)

D:/ModelsimProjects/lfsr6.v

Ln#

```
1   module LFSR6 (
2     input clk, rst_b,set_b,
3     output [5:0] q
4     );
5
6     generate
7       genvar i;
8       for(i=0;i<6;i=i+1)
9       begin: arr
10        dff dff0 ( .d(q[5]), .clk(clk), .rst_b(1'b1), .set_b(set_b), .q(q[0]) );
11        dff dff1 ( .d(q[0]), .clk(clk), .rst_b(1'b1), .set_b(set_b), .q(q[1]) );
12        dff dff2 ( .d(q[1]), .clk(clk), .rst_b(1'b1), .set_b(set_b), .q(q[2]) );
13        dff dff3 ( .d(q[2]^q[5]), .clk(clk), .rst_b(1'b1), .set_b(set_b), .q(q[3]) );
14        dff dff4 ( .d(q[3]), .clk(clk), .rst_b(1'b1), .set_b(set_b), .q(q[4]) );
15        dff dff5 ( .d(q[4]), .clk(clk), .rst_b(1'b1), .set_b(set_b), .q(q[5]) );
16      end
17    endgenerate
18
19  endmodule
```

D:/ModelsimProjects/lfsr_alternativ.v

```
Ln#
 1  module LFSR_instantions (
 2  input clk, rst_b, set_b,
 3  output [5:0] q
 4  );
 5
 6
 7  dff dff0 ( .d(q[5]),
 8  .clk(clk),
 9  .rst_b (1'b1),
10  .set_b (set_b),
11  .q (q[0]) );
12
13  dff dff1 ( .d(q[0]),
14  .clk(clk),
15  .rst_b (1'b1),
16  .set_b (set_b),
17  .q (q[1]) );
18
19  dff dff2 ( .d(q[1]),
20  .clk(clk),
21  .rst_b (1'b1),
22  .set_b (set_b),
23  .q (q[2]) );
24
25  dff dff3 ( .d(q[2] ^ q[5]),
26  .clk(clk),
27  .rst_b (1'b1),
28  .set_b (set_b),
29  .q (q[3]) );
30
31  dff dff4 ( .d(q[3]),
32  .clk(clk),
33  .rst_b (1'b1),
34  .set_b (set_b),
35  .q (q[4]) );
36
37  dff dff5 ( .d(q[4]),
38  .clk(clk),
39  .rst_b (1'b1),
40  .set_b (set_b),
41  .q (q[5]) );
42
43  endmodule
44
```

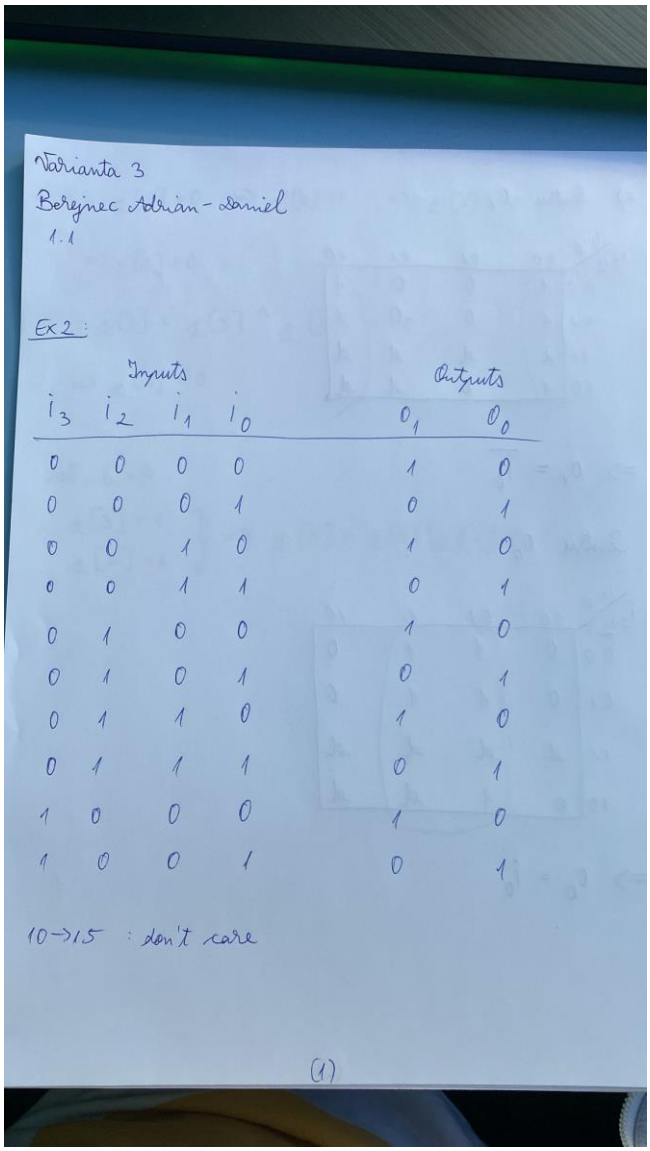
c)

D:/ModelsimProjects/lfsr6_tb.v

```
Ln#
 1  module lfsr6_tb(
 2    output reg clk, rst_b, set_b,
 3    output [5:0] q
 4    );
 5
 6    initial begin
 7      clk = 1'd1;
 8      forever #10 clk = ~clk;
 9      rst_b = 1'b0;
10      #10 rst_b = ~rst_b;
11
12      set_b = 1'b1;
13      #10 set_b = ~set_b;
14    end
15  endmodule
16
```

Ex2:

a)



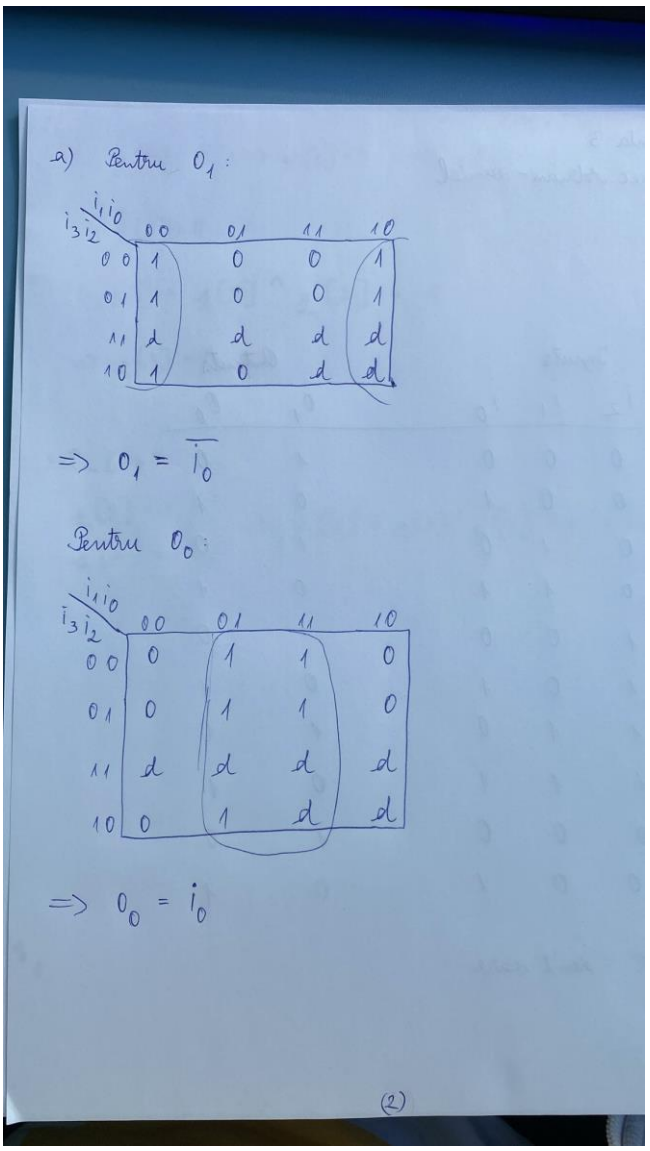
Varianta 3
Berejnec Adrian-Daniel
1.1

Ex 2:

Inputs				Outputs	
i_3	i_2	i_1	i_0	O_1	O_0
0	0	0	0	1	0
0	0	0	1	0	1
0	0	1	0	1	0
0	0	1	1	0	1
0	1	0	0	1	0
0	1	0	1	0	1
0	1	1	0	1	0
0	1	1	1	0	1
1	0	0	0	1	0
1	0	0	1	0	1

10->15 : don't care

(1)



a) Pentru O_1:

$i_3 i_2$ \ $i_1 i_0$	00	01	11	10
00	1	0	0	1
01	1	0	0	1
11	d	d	d	d
10	1	0	d	d

$\Rightarrow O_1 = \overline{i_0}$

Pentru O_0:

$i_3 i_2$ \ $i_1 i_0$	00	01	11	10
00	0	1	1	0
01	0	1	1	0
11	d	d	d	d
10	0	1	d	d

$\Rightarrow O_0 = i_0$

(2)