a)

D:/ModelsimProjects/fsm_7s.v

```
Ln#
 1  module fsm_7s(
 2    input clk, rst_b, idx, lst_pkt,
 3    output zero_pkt, st_pkt, pad_pkt, mgln_pkt, blk_val, msg_end
 4    );
 5
 6    reg [6:0] din;
 7    wire [6:0] din_nxt;
 8
 9    assign din_nxt[0] = 0;
10    assign din_nxt[1] = (din[0] & !lst_pkt) | (din[1] & idx!=0 & !lst_pkt) | (din[1] & idx==0 & !lst_pkt);
11    assign din_nxt[2] = (din[0] & lst_pkt) | (din[1] & idx!=0 & lst_pkt) | (din[1] & idx==0 & lst_pkt);
12    assign din_nxt[3] = (din[2] & idx==0) | (din[2] & idx!=0 & idx!=7) | (din[3] & idx!=7);
13    assign din_nxt[4] = (din[3] & idx==7) | (din[2] & idx==7);
14    assign din_nxt[5] = din[4];
15    assign din_nxt[6] = din[5] | din[6];
16
17    assign zero_pkt = din[3];
18    assign st_pkt = din[0] | din[1] | din[2] | din[3] | din[4];
19    assign pad_pkt = din[2];
20    assign mgln_pkt = din[4];
21    assign blk_val = (din[1] & idx==0) | (din[2] & idx==0) | din[5];
22    assign msg_end = din[5];
23
24    always @(posedge clk, negedge rst_b)
25        if(!rst_b)
26          din <= 7'd1;
27        else din <= din_nxt;
28
29    endmodule
```

b) Testbench:

D:/ModelsimProjects/fsm_7s_tb.v

```
Ln#
 1  module fsm_7s_tb(
 2    output reg clk, rst_b, lst_pkt,
 3    output reg[6:0] idx,
 4    output st_pkt, zero_pkt, pad_pkt, mgln_pkt, blk_val, msg_end
 5    );
 6
 7    fsm_7s DUT (
 8        .clk(clk),
 9        .rst_b(rst_b),
10        .lst_pkt(lst_pkt),
11        .idx(idx)
12        );
13
14    initial begin
15      clk = 1'd1;
16      forever #20 clk = ~clk;
17    end
18
19    initial begin
20      rst_b = 1'd0;
21      #10 rst_b = 1'd1;
22    end
23
24    initial begin
25      lst_pkt = 0;
26      idx = 7'd0;
27
28      #50 idx = 7'd1;
29      #50 idx = 7'd7;
30      #50 idx = 7'd0;
31    end
32  endmodule
33
```