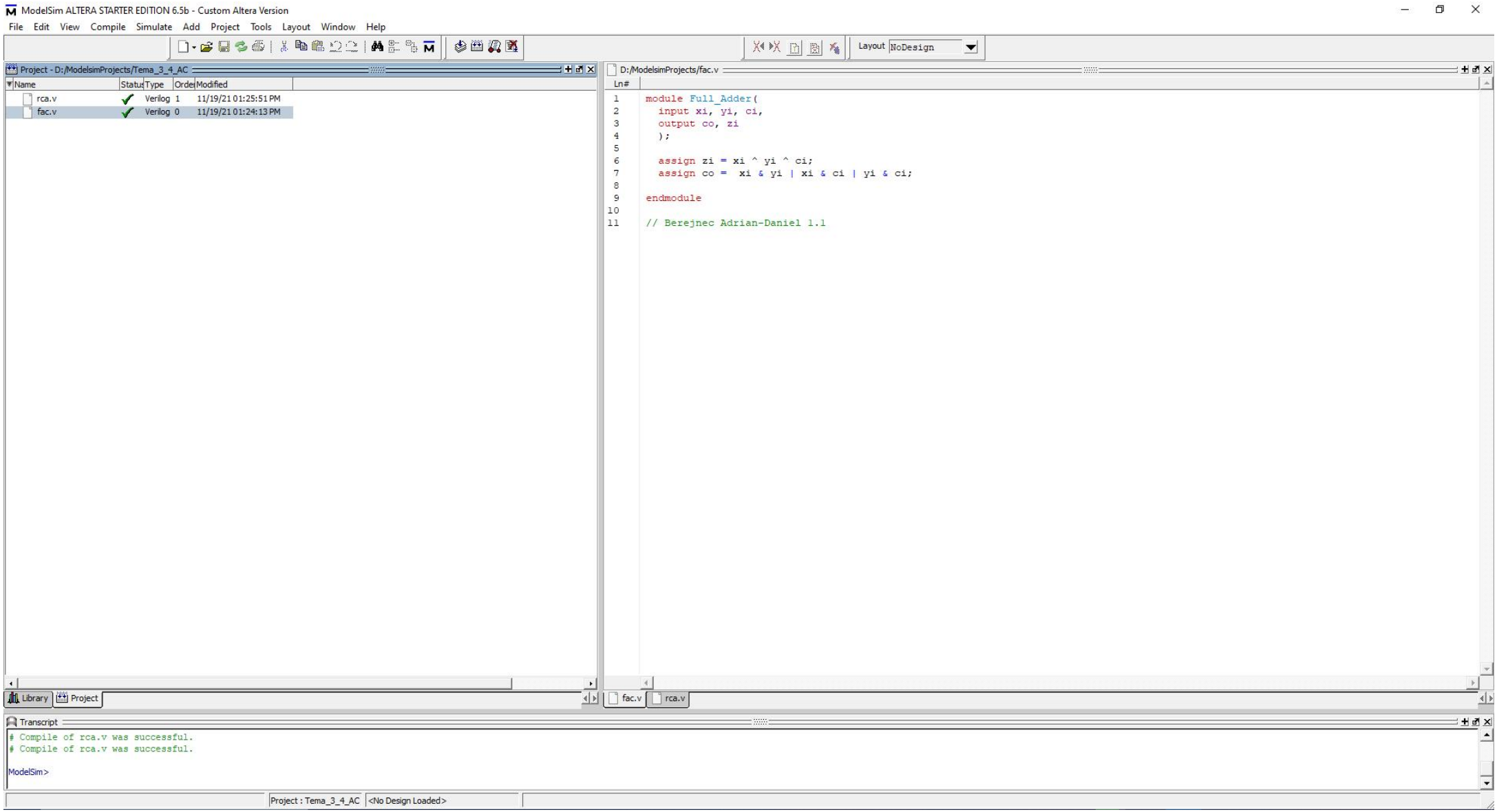
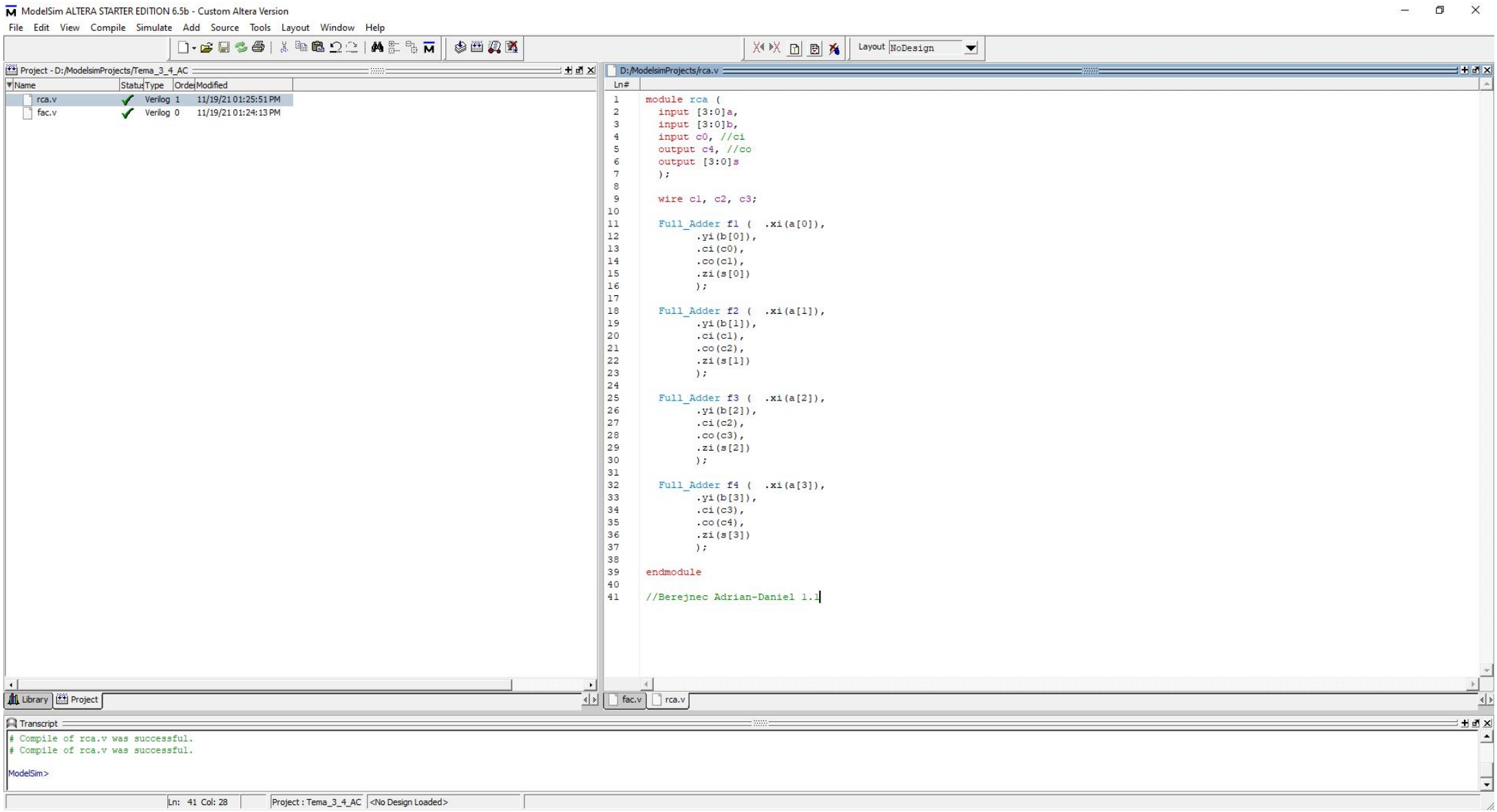
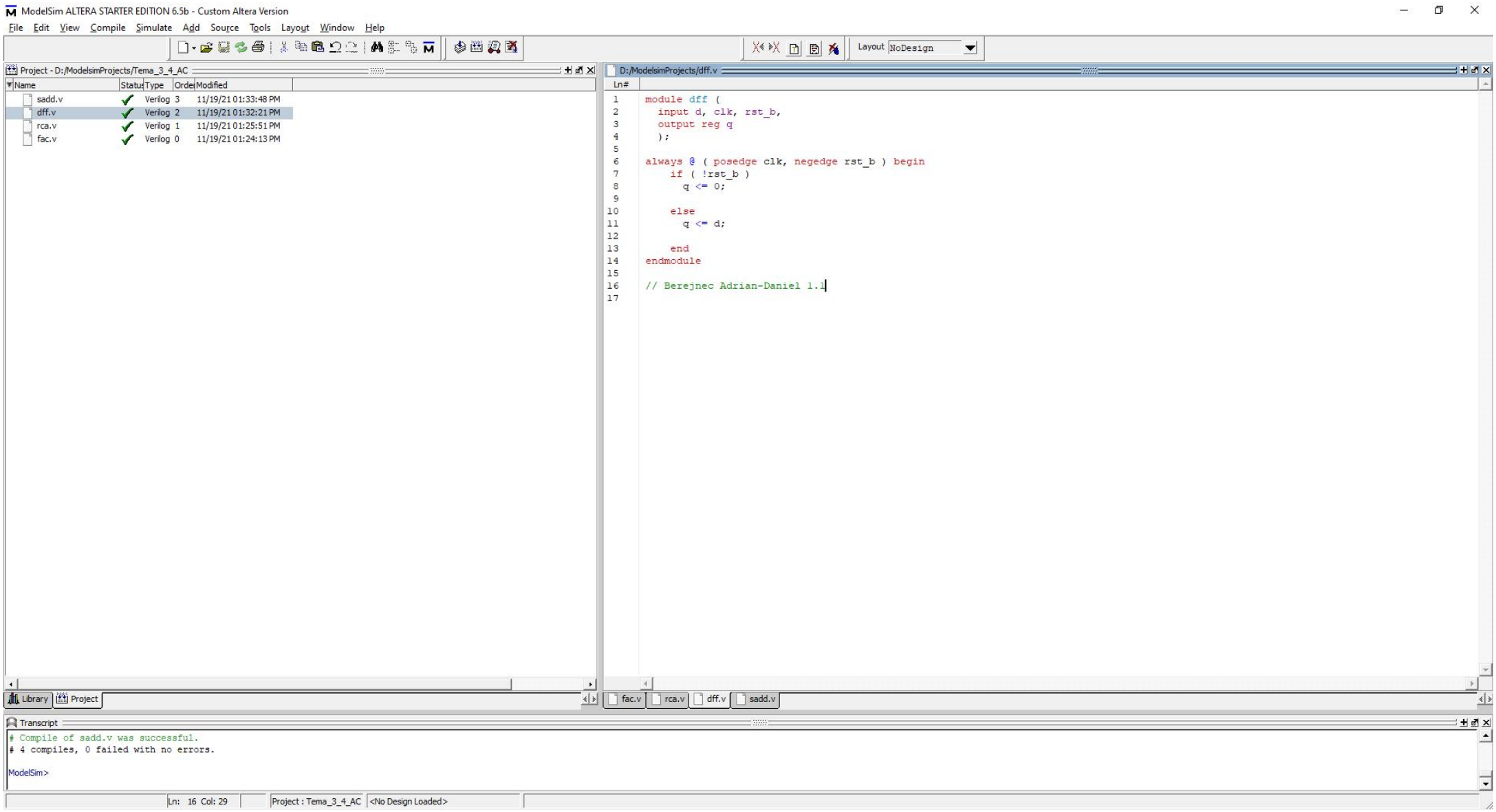
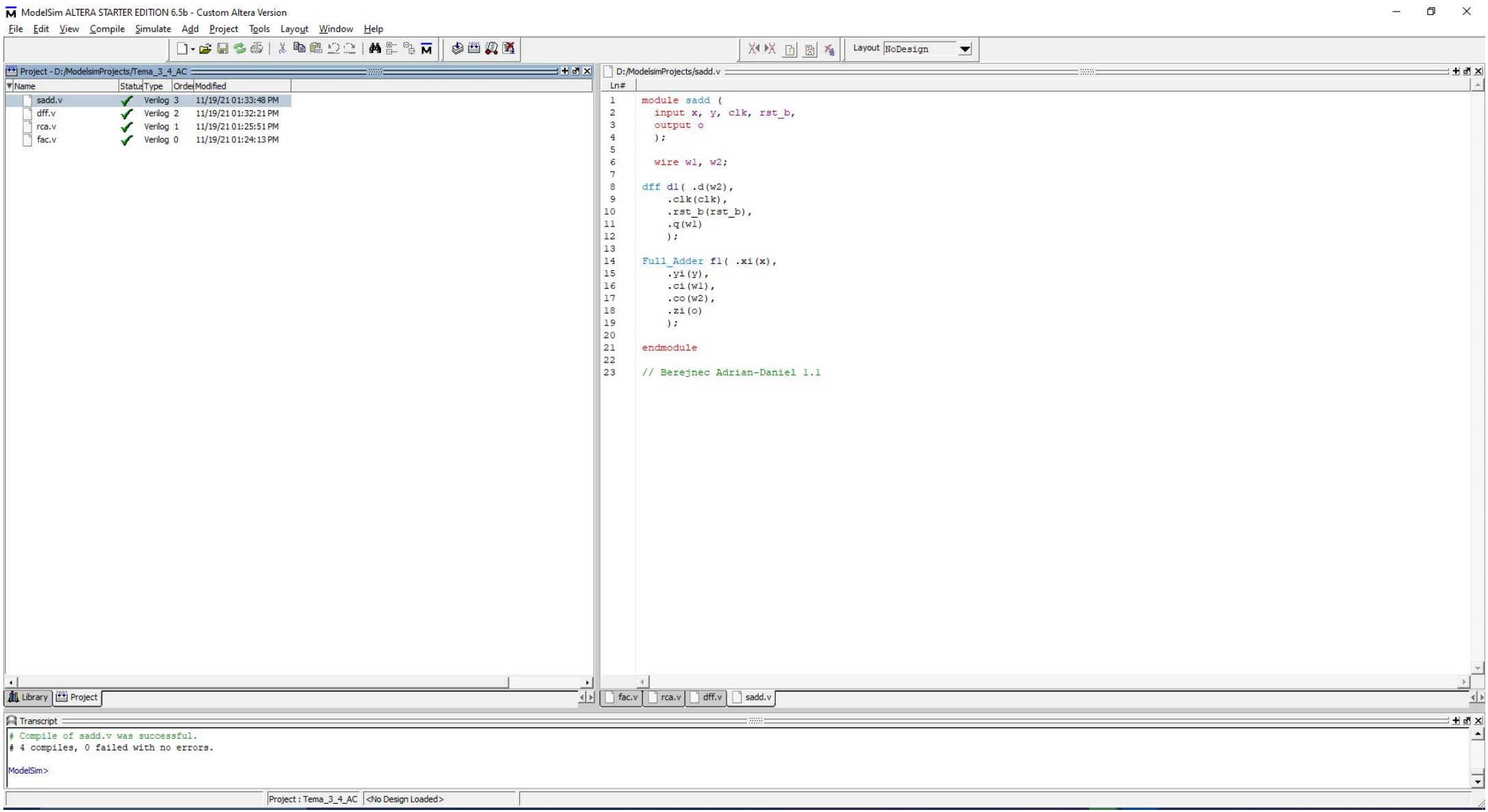
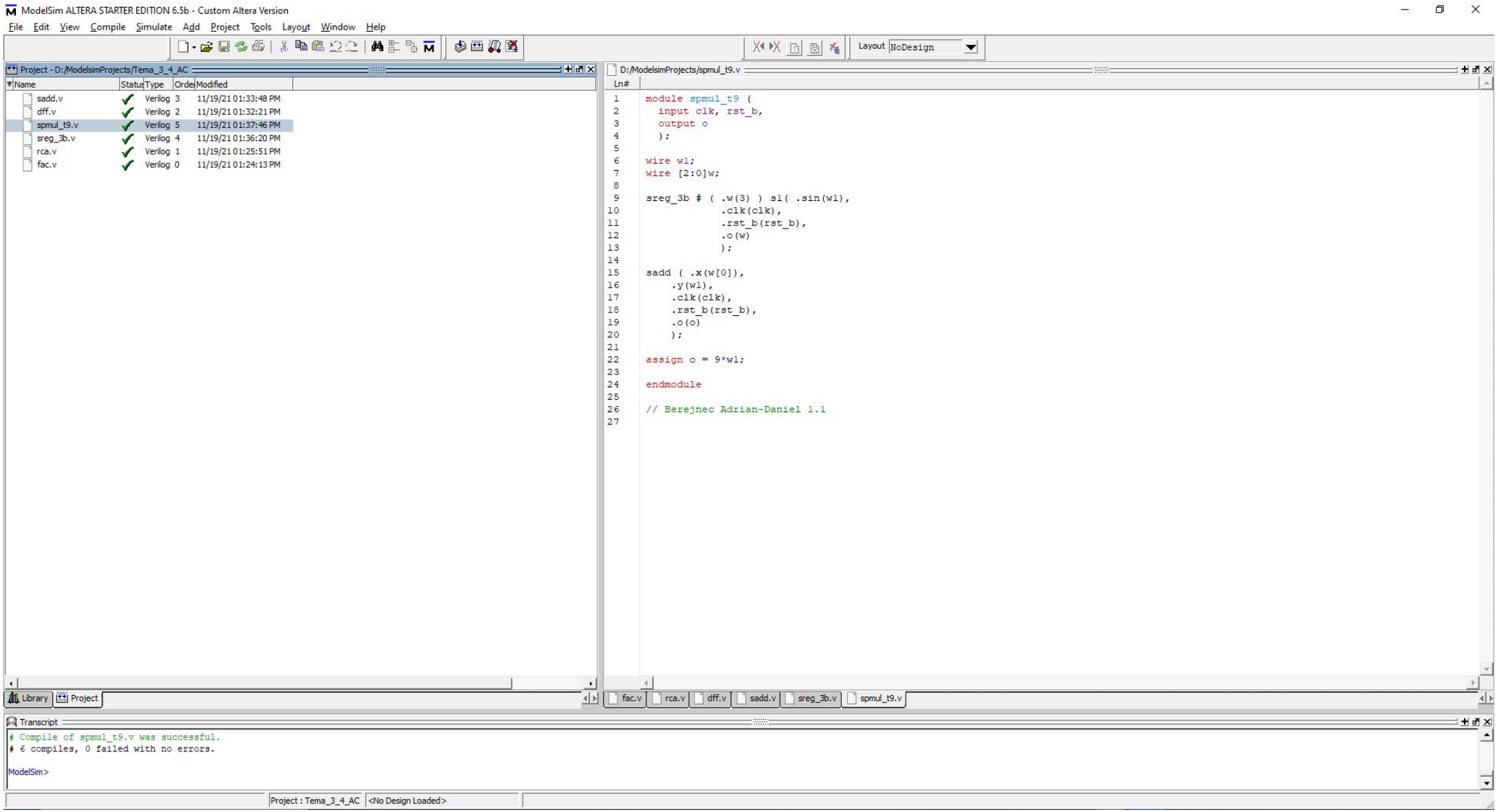
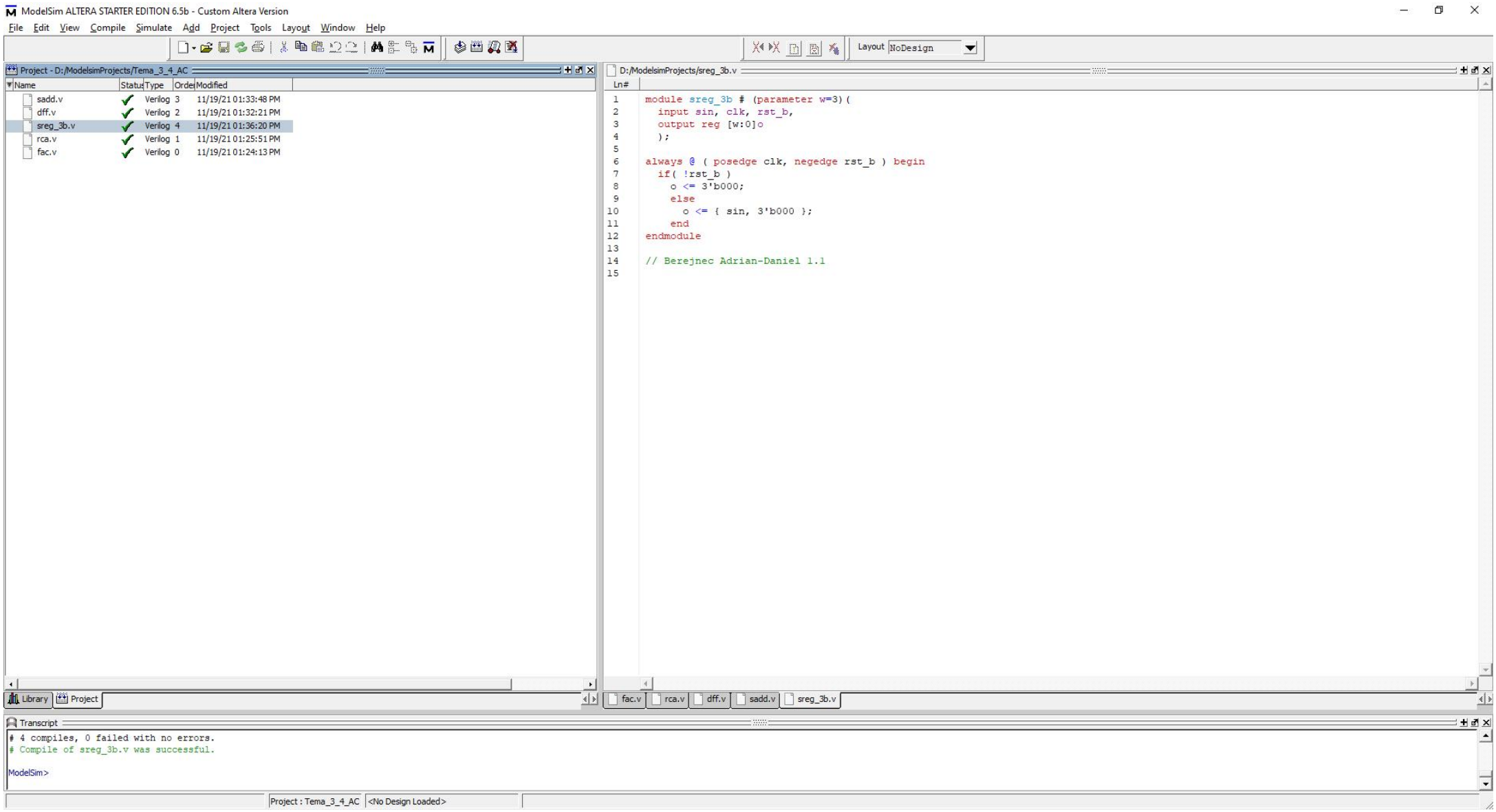

ModelSim ALTERA STARTER EDITION 6.5b - Custom Altera Version
File Edit View Compile Simulate Add Project Tools Layout Window Help
Layout NoDesign
Project - D:/ModelsimProjects/Tema_3_4_AC
Name Status Type Order Modified
rca.v Verilog 1 11/19/21 01:25:51 PM
fac.v Verilog 0 11/19/21 01:24:13 PM
Library Project
D:/ModelsimProjects/fac.v
Ln#
1 module Full_Adder(
2 input xi, yi, ci,
3 output co, zi
4);
5
6 assign zi = xi ^ yi ^ ci;
7 assign co = xi & yi | xi & ci | yi & ci;
8
9 endmodule
10
11 // Berejnec Adrian-Daniel 1.1
fac.v rca.v
Transcript
Compile of rca.v was successful.
Compile of rca.v was successful.
ModelSim>
Project : Tema_3_4_AC <No Design Loaded>

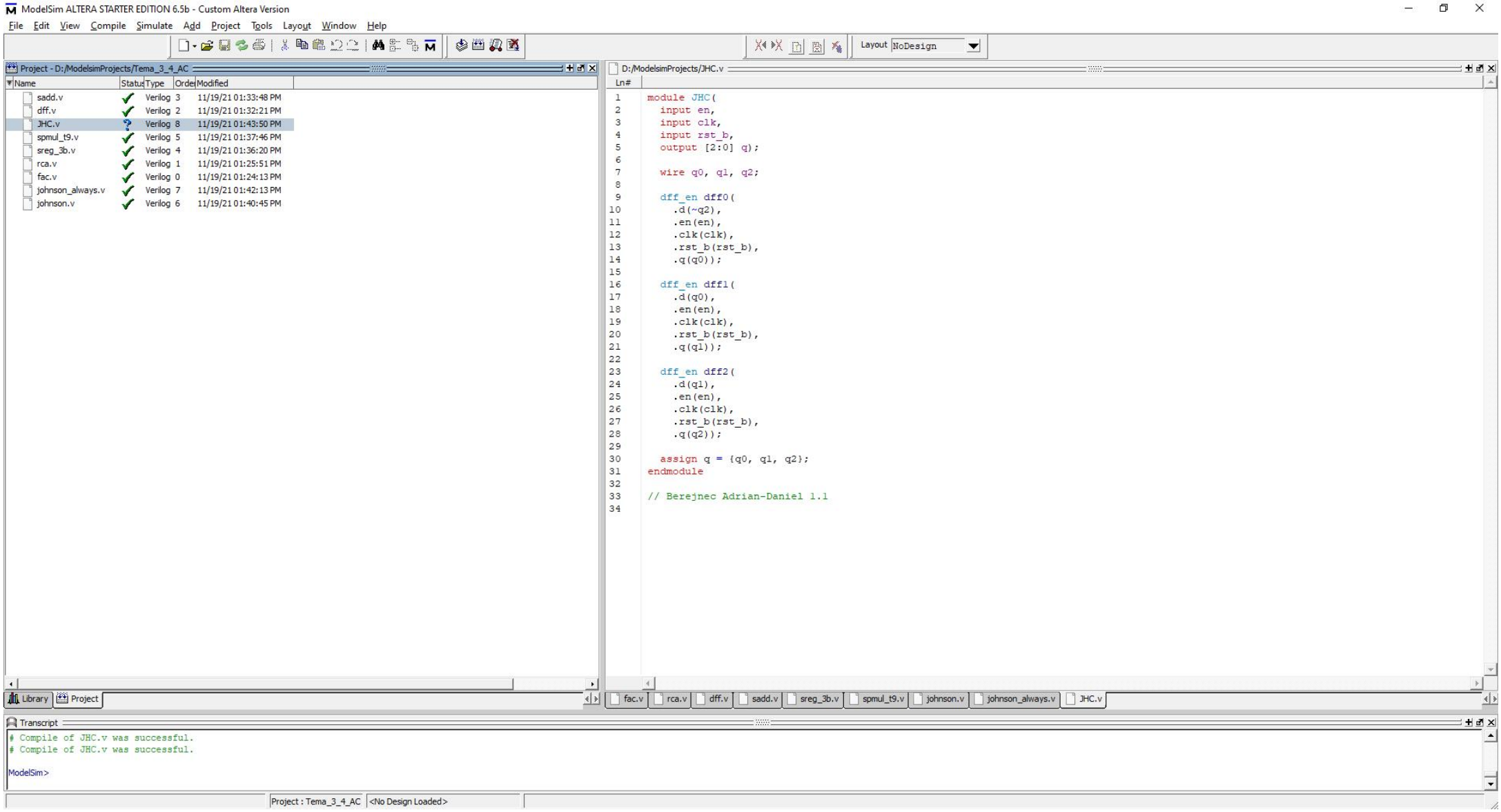

ModelSim ALTERA STARTER EDITION 6.5b - Custom Altera Version
File Edit View Compile Simulate Add Source Tools Layout Window Help
Layout NoDesign
Project - D:/ModelsimProjects/Tema_3_4_AC
Name Status Type Orde Modified
rca.v Verilog 1 11/19/21 01:25:51 PM
fac.v Verilog 0 11/19/21 01:24:13 PM
Library Project
D:/ModelsimProjects/rca.v
Ln#
1 module rca (
2 input [3:0]a,
3 input [3:0]b,
4 input c0, //ci
5 output c4, //co
6 output [3:0]s
7);
8
9 wire c1, c2, c3;
10
11 Full_Adder f1 (.xi(a[0]),
12 .yi(b[0]),
13 .ci(c0),
14 .co(c1),
15 .zi(s[0])
16);
17
18 Full_Adder f2 (.xi(a[1]),
19 .yi(b[1]),
20 .ci(c1),
21 .co(c2),
22 .zi(s[1])
23);
24
25 Full_Adder f3 (.xi(a[2]),
26 .yi(b[2]),
27 .ci(c2),
28 .co(c3),
29 .zi(s[2])
30);
31
32 Full_Adder f4 (.xi(a[3]),
33 .yi(b[3]),
34 .ci(c3),
35 .co(c4),
36 .zi(s[3])
37);
38
39 endmodule
40
41 //Berejnec Adrian-Daniel 1.1
fac.v rca.v
Transcript
Compile of rca.v was successful.
Compile of rca.v was successful.
ModelSim>
Ln: 41 Col: 28
Project : Tema_3_4_AC
<No Design Loaded>


ModelSim ALTERA STARTER EDITION 6.5b - Custom Altera Version
File Edit View Compile Simulate Add Source Tools Layout Window Help
Layout NoDesign
Project - D:/ModelsimProjects/Tema_3_4_AC
Name Status Type Orde Modified
sadd.v Verilog 3 11/19/21 01:33:48 PM
dff.v Verilog 2 11/19/21 01:32:21 PM
rca.v Verilog 1 11/19/21 01:25:51 PM
fac.v Verilog 0 11/19/21 01:24:13 PM
Library Project
D:/ModelsimProjects/dff.v
Ln#
1 module dff (
2 input d, clk, rst_b,
3 output reg q
4);
5
6 always @ (posedge clk, negedge rst_b) begin
7 if (!rst_b)
8 q <= 0;
9
10 else
11 q <= d;
12
13 end
14 endmodule
15
16 // Berejnec Adrian-Daniel 1.1
17
fac.v rca.v dff.v sadd.v
Transcript
Compile of sadd.v was successful.
4 compiles, 0 failed with no errors.
ModelSim>
Ln: 16 Col: 29
Project : Tema_3_4_AC
<No Design Loaded>


ModelSim ALTERA STARTER EDITION 6.5b - Custom Altera Version
File Edit View Compile Simulate Add Project Tools Layout Window Help
Layout NoDesign
Project - D:/ModelsimProjects/Tema_3_4_AC
Name Status Type Order Modified
sadd.v Verilog 3 11/19/21 01:33:48 PM
dff.v Verilog 2 11/19/21 01:32:21 PM
rca.v Verilog 1 11/19/21 01:25:51 PM
fac.v Verilog 0 11/19/21 01:24:13 PM
Library Project
D:/ModelsimProjects/sadd.v
Ln#
1 module sadd (
2 input x, y, clk, rst_b,
3 output o
4);
5
6 wire w1, w2;
7
8 dff d1(.d(w2),
9 .clk(clk),
10 .rst_b(rst_b),
11 .q(w1)
12);
13
14 Full_Adder f1(.xi(x),
15 .yi(y),
16 .ci(w1),
17 .co(w2),
18 .zi(o)
19);
20
21 endmodule
22
23 // Berejnec Adrian-Daniel 1.1
fac.v rca.v dff.v sadd.v
Transcript
Compile of sadd.v was successful.
4 compiles, 0 failed with no errors.
ModelSim>
Project : Tema_3_4_AC
<No Design Loaded>


ModelSim ALTERA STARTER EDITION 6.5b - Custom Altera Version
File Edit View Compile Simulate Add Project Tools Layout Window Help
Layout NoDesign
Project - D:/ModelsimProjects/Tema_3_4_AC
Name Status Type Order Modified
sadd.v Verilog 3 11/19/21 01:33:48 PM
dff.v Verilog 2 11/19/21 01:32:21 PM
spmul_t9.v Verilog 5 11/19/21 01:37:46 PM
sreg_3b.v Verilog 4 11/19/21 01:36:20 PM
rca.v Verilog 1 11/19/21 01:25:51 PM
fac.v Verilog 0 11/19/21 01:24:13 PM
Library Project
D:/ModelsimProjects/spmul_t9.v
Ln#
1 module spmul_t9 (
2 input clk, rst_b,
3 output o
4);
5
6 wire w1;
7 wire [2:0]w;
8
9 sreg_3b # (.w(3)) s1(.sin(w1),
10 .clk(clk),
11 .rst_b(rst_b),
12 .o(w)
13);
14
15 sadd (.x(w[0]),
16 .y(w1),
17 .clk(clk),
18 .rst_b(rst_b),
19 .o(o)
20);
21
22 assign o = 9*w1;
23
24 endmodule
25
26 // Berejnec Adrian-Daniel 1.1
27
fac.v rca.v dff.v sadd.v sreg_3b.v spmul_t9.v
Transcript
Compile of spmul_t9.v was successful.
6 compiles, 0 failed with no errors.
ModelSim>
Project : Tema_3_4_AC <No Design Loaded>


ModelSim ALTERA STARTER EDITION 6.5b - Custom Altera Version
File Edit View Compile Simulate Add Project Tools Layout Window Help
Layout NoDesign
Project - D:/ModelsimProjects/Tema_3_4_AC
Name Status Type Order Modified
sadd.v Verilog 3 11/19/21 01:33:48 PM
dff.v Verilog 2 11/19/21 01:32:21 PM
sreg_3b.v Verilog 4 11/19/21 01:36:20 PM
rca.v Verilog 1 11/19/21 01:25:51 PM
fac.v Verilog 0 11/19/21 01:24:13 PM
Library Project
D:/ModelsimProjects/sreg_3b.v
Ln#
1 module sreg_3b # (parameter w=3)(
2 input sin, clk, rst_b,
3 output reg [w:0]o
4);
5
6 always @ (posedge clk, negedge rst_b) begin
7 if(!rst_b)
8 o <= 3'b000;
9 else
10 o <= { sin, 3'b000 };
11 end
12 endmodule
13
14 // Berejnec Adrian-Daniel 1.1
15
fac.v rca.v dff.v sadd.v sreg_3b.v
Transcript
4 compiles, 0 failed with no errors.
Compile of sreg_3b.v was successful.
ModelSim>
Project : Tema_3_4_AC
<No Design Loaded>


ModelSim ALTERA STARTER EDITION 6.5b - Custom Altera Version
File Edit View Compile Simulate Add Project Tools Layout Window Help
Layout NoDesign
Project - D:/ModelsimProjects/Tema_3_4_AC
Name Status Type Order Modified
sadd.v Verilog 3 11/19/21 01:33:48 PM
dff.v Verilog 2 11/19/21 01:32:21 PM
JHC.v Verilog 8 11/19/21 01:43:50 PM
spmul_t9.v Verilog 5 11/19/21 01:37:46 PM
sreg_3b.v Verilog 4 11/19/21 01:36:20 PM
rca.v Verilog 1 11/19/21 01:25:51 PM
fac.v Verilog 0 11/19/21 01:24:13 PM
johnson_always.v Verilog 7 11/19/21 01:42:13 PM
johnson.v Verilog 6 11/19/21 01:40:45 PM
Library Project
D:/ModelsimProjects/JHC.v
Ln#
1 module JHC(
2 input en,
3 input clk,
4 input rst_b,
5 output [2:0] q);
6
7 wire q0, q1, q2;
8
9 dff_en dff0(
10 .d(~q2),
11 .en(en),
12 .clk(clk),
13 .rst_b(rst_b),
14 .q(q0));
15
16 dff_en dff1(
17 .d(q0),
18 .en(en),
19 .clk(clk),
20 .rst_b(rst_b),
21 .q(q1));
22
23 dff_en dff2(
24 .d(q1),
25 .en(en),
26 .clk(clk),
27 .rst_b(rst_b),
28 .q(q2));
29
30 assign q = {q0, q1, q2};
31 endmodule
32
33 // Berejnec Adrian-Daniel 1.1
34
fac.v rca.v dff.v sadd.v sreg_3b.v spmul_t9.v johnson.v johnson_always.v JHC.v
Transcript
Compile of JHC.v was successful.
Compile of JHC.v was successful.
ModelSim>
Project : Tema_3_4_AC
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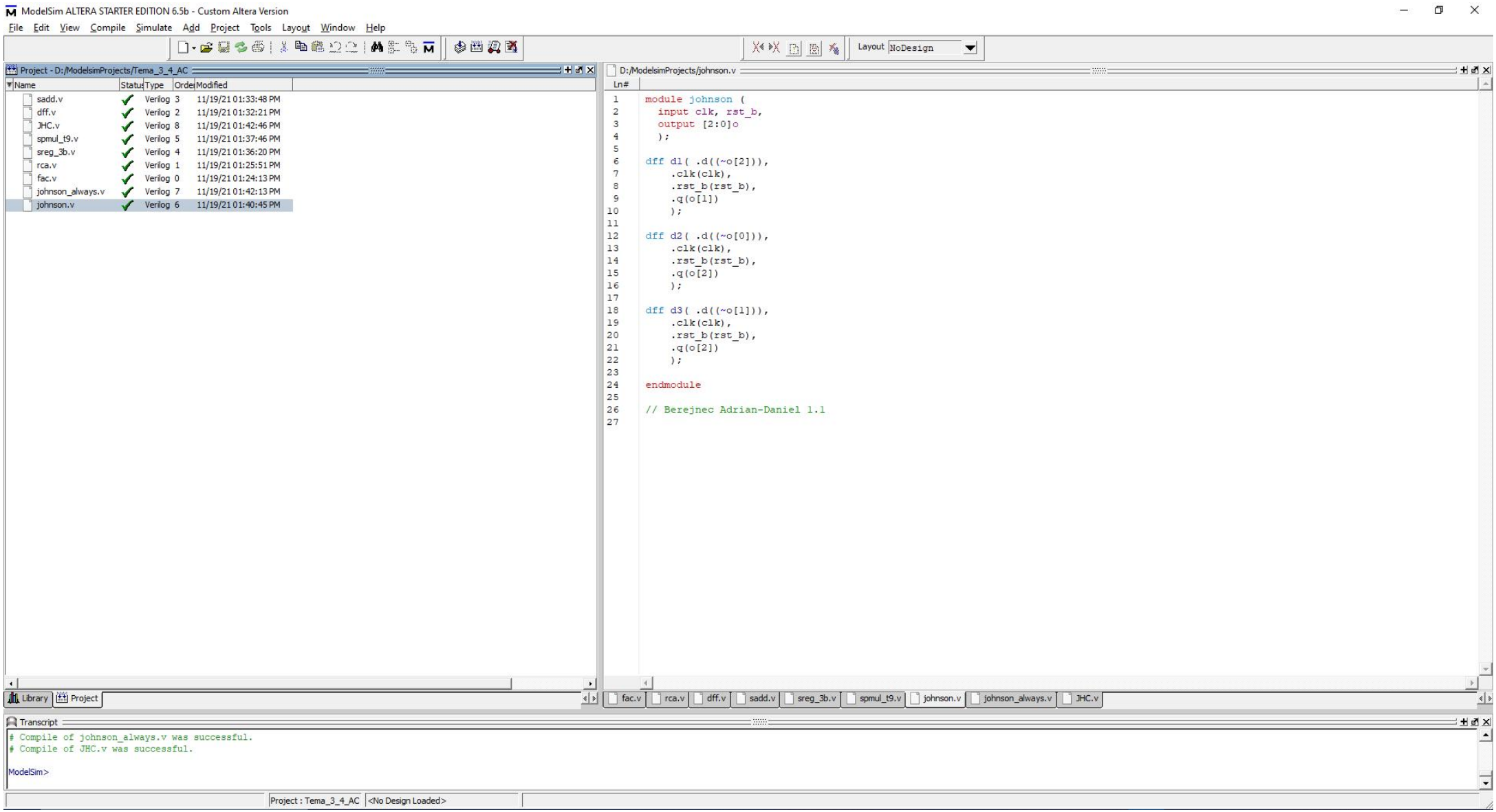
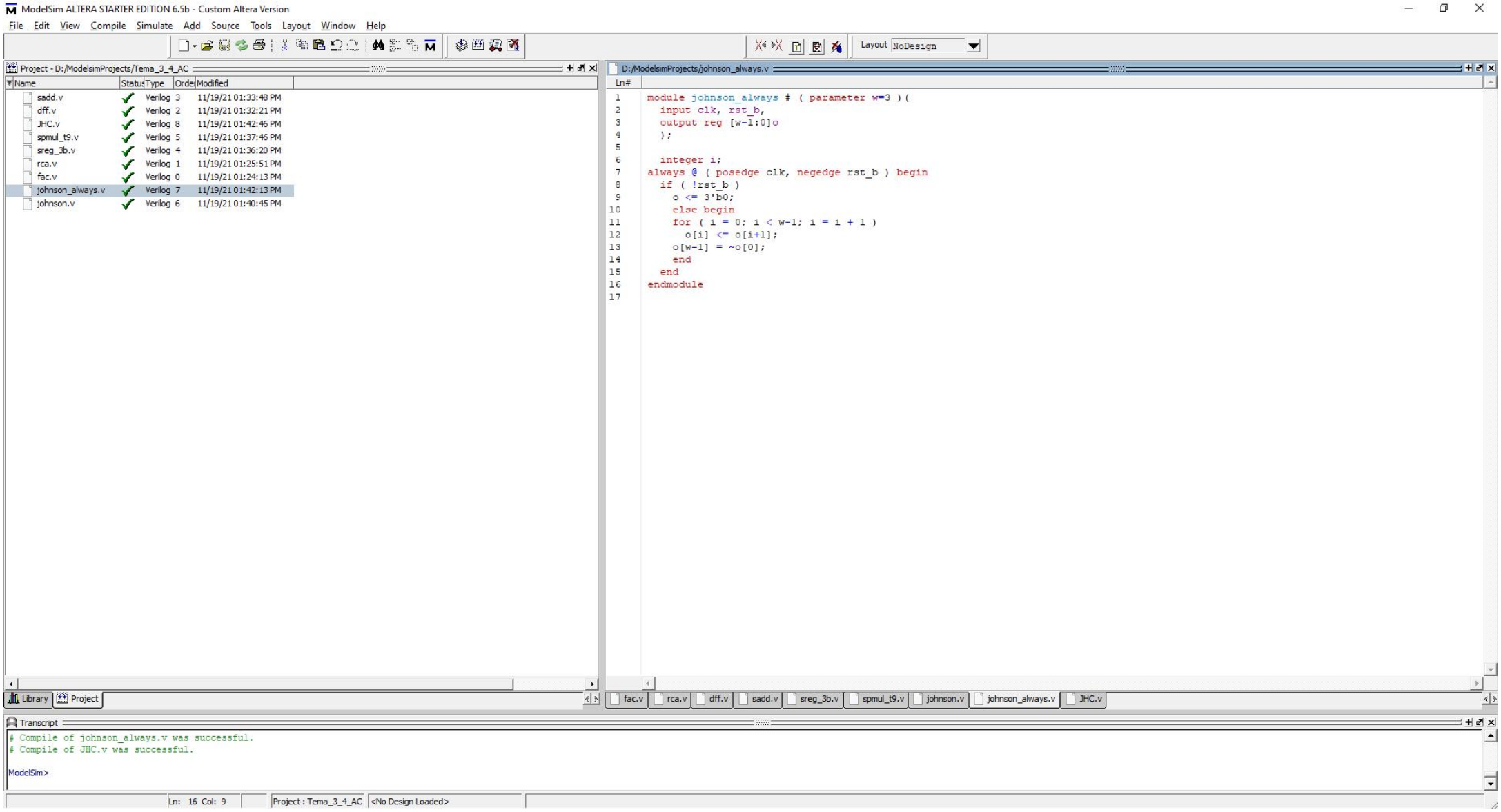

ModelSim ALTERA STARTER EDITION 6.5b - Custom Altera Version
File Edit View Compile Simulate Add Project Tools Layout Window Help
Layout NoDesign
Project - D:/ModelsimProjects/Tema_3_4_AC
Name Status Type Order Modified
sadd.v Verilog 3 11/19/21 01:33:48 PM
dff.v Verilog 2 11/19/21 01:32:21 PM
JHC.v Verilog 8 11/19/21 01:42:46 PM
spmul_t9.v Verilog 5 11/19/21 01:37:46 PM
sreg_3b.v Verilog 4 11/19/21 01:36:20 PM
rca.v Verilog 1 11/19/21 01:25:51 PM
fac.v Verilog 0 11/19/21 01:24:13 PM
johnson_always.v Verilog 7 11/19/21 01:42:13 PM
johnson.v Verilog 6 11/19/21 01:40:45 PM
Library Project
D:/ModelsimProjects/johnson.v
Ln#
1 module johnson (
2 input clk, rst_b,
3 output [2:0]o
4);
5
6 dff d1(.d((~o[2])),
7 .clk(clk),
8 .rst_b(rst_b),
9 .q(o[1])
10);
11
12 dff d2(.d((~o[0])),
13 .clk(clk),
14 .rst_b(rst_b),
15 .q(o[2])
16);
17
18 dff d3(.d((~o[1])),
19 .clk(clk),
20 .rst_b(rst_b),
21 .q(o[2])
22);
23
24 endmodule
25
26 // Berejnec Adrian-Daniel 1.1
27
fac.v rca.v dff.v sadd.v sreg_3b.v spmul_t9.v johnson.v johnson_always.v JHC.v
Transcript
Compile of johnson_always.v was successful.
Compile of JHC.v was successful.
ModelSim>
Project : Tema_3_4_AC
<No Design Loaded>


ModelSim ALTERA STARTER EDITION 6.5b - Custom Altera Version
File Edit View Compile Simulate Add Source Tools Layout Window Help
Layout NoDesign
Project - D:/ModelsimProjects/Tema_3_4_AC
Name Status Type Order Modified
sadd.v Verilog 3 11/19/21 01:33:48 PM
dff.v Verilog 2 11/19/21 01:32:21 PM
JHC.v Verilog 8 11/19/21 01:42:46 PM
spmul_t9.v Verilog 5 11/19/21 01:37:46 PM
sreg_3b.v Verilog 4 11/19/21 01:36:20 PM
rca.v Verilog 1 11/19/21 01:25:51 PM
fac.v Verilog 0 11/19/21 01:24:13 PM
johnson_always.v Verilog 7 11/19/21 01:42:13 PM
johnson.v Verilog 6 11/19/21 01:40:45 PM
Library Project
D:/ModelsimProjects/johnson_always.v
Ln#
1 module johnson_always # (parameter w=3)(
2 input clk, rst_b,
3 output reg [w-1:0]o
4);
5
6 integer i;
7 always @ (posedge clk, negedge rst_b) begin
8 if (!rst_b)
9 o <= 3'b0;
10 else begin
11 for (i = 0; i < w-1; i = i + 1)
12 o[i] <= o[i+1];
13 o[w-1] = ~o[0];
14 end
15 end
16 endmodule
17
fac.v rca.v dff.v sadd.v sreg_3b.v spmul_t9.v johnson.v johnson_always.v JHC.v
Transcript
Compile of johnson_always.v was successful.
Compile of JHC.v was successful.
ModelSim>
Ln: 16 Col: 9
Project : Tema_3_4_AC
<No Design Loaded>