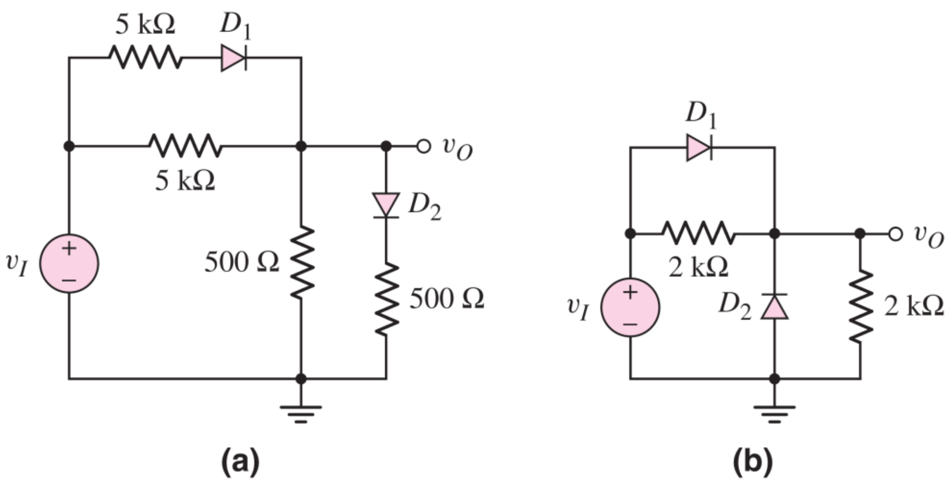
DIODE CIRCUIT EXAMPLES

1)

In each circuit shown in Figure P2.50, the diode cut-in voltage is $V_\gamma = 0.6$ V. (a) For the circuit in Figure P2.50(a), determine v_O for (i) $v_I = +5$ V and (ii) $v_I = -5$ V. (b) Repeat part (a) for the circuit in Figure P2.50(b). (c) Plot the voltage transfer characteristics, v_O versus v_I, of each circuit over the range $-5 \le v_I \le +5$ V.



(a) (i) $\upsilon_I = 5$ V, D_1 and D_2 on

$$\frac{5-(\upsilon_O+0.6)}{5}+\frac{5-\upsilon_O}{5}=\frac{\upsilon_O}{0.5}+\frac{\upsilon_O-0.6}{0.5}$$

$$0.88+1.0+1.2=\upsilon_O(0.20+0.20+2.0+2.0)\Rightarrow \upsilon_O = 0.7 \text{ V}$$

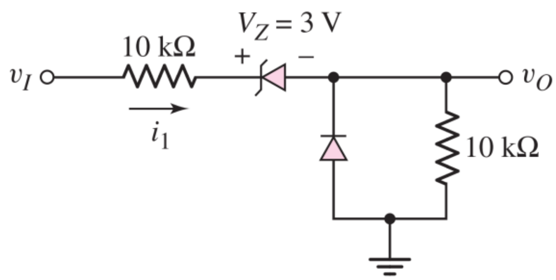
(ii) $\upsilon_I = -5$ V

$$\upsilon_O = \left(\frac{0.5}{0.5+5}\right)\upsilon_I = -0.455 \text{ V}$$

(b) (i) $\upsilon_I = 5$ V, $\upsilon_O = 4.4$ V

(ii) $\upsilon_I = -5$ V, $\upsilon_O = -0.6$ V

2)



Consider the circuit in Figure P2.31. Let $V_\gamma = 0$. (a) Plot v_O versus v_I over the range $-10 \le v_I \le +10$ V. (b) Plot i_1 over the same input voltage range as part (a).

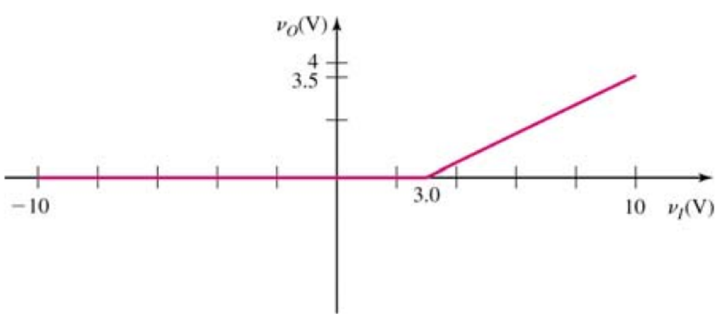
(a) For $-10 \le v_I \le 0$, both diodes are conducting $\Rightarrow v_O = 0$

For $0 \le v_I \le 3$, Zener not in breakdown, so $\underline{i_1 = 0, \quad v_O = 0}$

For $v_I > 3 \quad i_1 = \dfrac{v_I - 3}{20}\ mA$

$$v_o = \left(\frac{v_I - 3}{20}\right)(10) = \frac{1}{2}v_I - 1.5$$

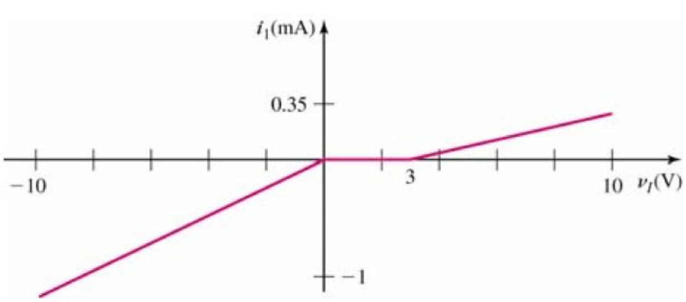
At $v_I = 10\ V$, $v_o = 3.5\ V$, $i_1 = 0.35\ mA$



(b) For $v_I < 0$, both diodes forward biased

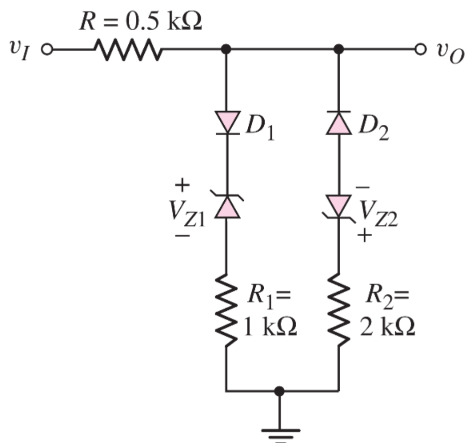
$-i_1 = \dfrac{0 - v_I}{10}$. At $v_I = -10\ V$, $i_1 = -1\ mA$

For $v_I > 3$, $i_1 = \dfrac{v_I - 3}{20}$. At $v_I = 10\ V$, $i_1 = 0.35\ mA$



3)

The parameters in the circuit shown in Figure P2.30 are $V_\gamma = 0.7$ V, $V_{Z1} = 2.3$ V, and $V_{Z2} = 5.6$ V. Plot v_O versus v_I over the range of $-10 \le v_I \le +10$ V.



For $-6.3 \le v_I \le 3$ V, $v_O = v_I$

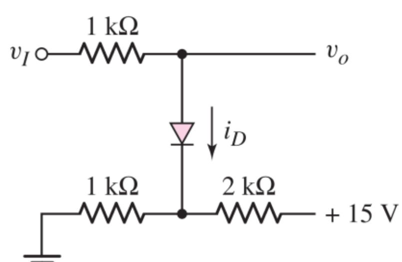
For $v_I > 3$ V, $I = \dfrac{v_I - 3}{1.5}$ and $v_O = v_I - I(0.5)$

$$v_O = v_I - (0.5)\left(\frac{v_I - 3}{1.5}\right) = 0.667 v_I + 1.0$$

For $v_I < -6.3$ V, $I = \dfrac{v_I + 6.3}{2.5}$ and $v_O = v_I - I(0.5)$

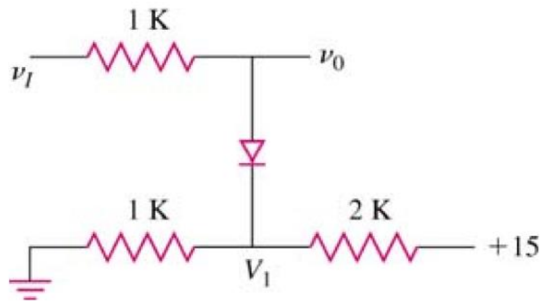
$$v_O = v_I - (0.5)\left(\frac{v_I + 6.3}{2.5}\right) = 0.8 v_I - 1.26$$

4)



For the circuit in Figure P2.32, (a) plot v_O versus v_I for $0 \leq v_I \leq 15$ V. Assume $V_\gamma = 0.7$ V. Indicate all breakpoints. (b) Plot i_D over the same range of input voltage.

(a)



$$V_1 = \frac{1}{3} \times 15 = 5 \text{ V} \Rightarrow \text{ for } v_I \leq 5.7,\ v_0 = v_I$$

For $v_I > 5.7\ V$

$$\frac{v_I - (V_1 + 0.7)}{1} + \frac{15 - V_1}{2} = \frac{V_1}{1},\ v_0 = V_1 + 0.7$$

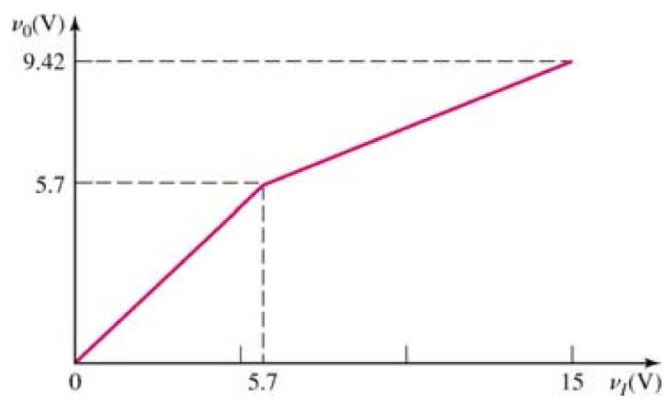
$$\frac{v_I - v_0}{1} + \frac{15 - (v_0 - 0.7)}{2} = \frac{v_0 - 0.7}{1}$$

$$\frac{v_I}{1} + \frac{15.7}{2} + \frac{0.7}{1} = v_0\left(\frac{1}{1} + \frac{1}{2} + \frac{1}{1}\right) = v_0(2.5)$$

$$v_I + 8.55 = v_0(2.5) \Rightarrow v_0 = \frac{1}{2.5} v_I + 3.42$$

$$v_I = 5.7 \Rightarrow v_0 = 5.7$$

$$v_I = 15 \Rightarrow v_0 = 9.42$$

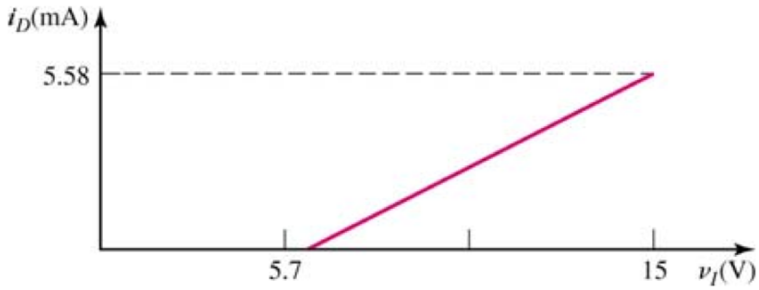


(b) $i_D = 0$ for $0 \le v_I \le 5.7$

Then for $v_I > 5.7\ V$

$$i_D = \frac{v_I - v_O}{1} = \frac{v_I - \left(\dfrac{v_I}{2.5} + 3.42\right)}{1} \quad \text{or} \quad i_D = \frac{0.6v_I - 3.42}{1}$$

For $v_I = 15$, $i_D = 5.58\ mA$



5)

(a) Consider a pn junction diode biased at $I_{DQ} = 1$ mA. A sinusoidal voltage is superimposed on V_{DQ} such that the peak-to-peak sinusoidal current is $0.05I_{DQ}$. Find the value of the applied peak-to-peak sinusoidal voltage. (b) Repeat part (a) if $I_{DQ} = 0.1$ mA.

a. $$r_d = \frac{V_T}{I_{DQ}} = \frac{(0.026)}{1} = 0.026\ \text{k}\Omega = 26\Omega$$

$$i_d = 0.05I_{DQ} = 50\ \mu\text{A} \quad \text{peak-to-peak}$$

$$v_d = i_d r_d = (26)(50)\ \ \mu\text{A} \Rightarrow \underline{v_d = 1.30\ \text{mV}\ \ \text{peak-to-peak}}$$

b. For $I_{DQ} = 0.1\ \text{mA} \Rightarrow r_d = \dfrac{(0.026)}{0.1} = 260\Omega$

$$i_d = 0.05I_{DQ} = 5\ \mu\text{A} \quad \text{peak-to-peak}$$

$$v_d = i_d r_d = (260)(5)\ \ \mu\text{V} \Rightarrow \underline{v_d = 1.30\ \text{mV}\ \ \text{peak-to-peak}}$$

All of the examples are taken from the textbook:
Microlelectronics, Circuit Analysis and Design by D. A. Neamen