

# Cavity Simulator in FPGA

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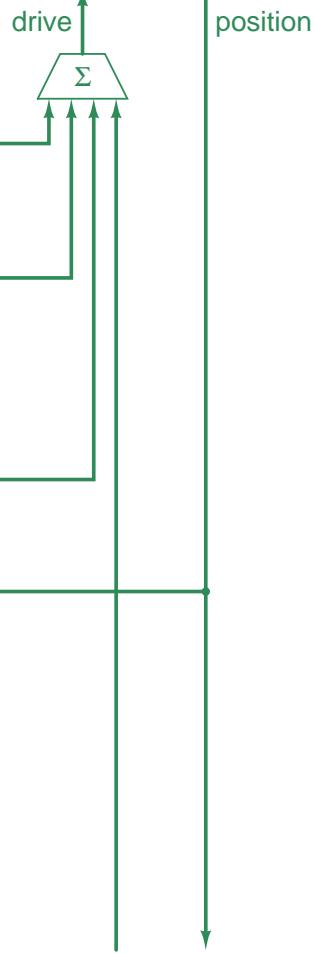
(abridged)

Clocks at ~200 MHz in Xilinx 7Axxx  
8 cavity-controller pairs could fit on AC701?

$m$  mechanical modes updated every  $2m$  cycles

Mechanical eigenmode propagator  
 $zy = My + d$

*resonator.v*



Gaussian noise  
Environmental sources?

outer  
outer\_prod.v

Piezo control

Virtual Piezo

outer  
outer\_prod.v

Beam timing

Cavity electromagnetics simulator

Electromagnetic eigenmode propagator ( $\pi$  mode)  
*cav\_mode.v*

outer  
outer\_prod.v

Electromagnetic eigenmode propagator ( $8\pi/9$  mode)  
*cav\_mode.v*

outer  
outer\_prod.v

Drive

IQ

Forward

Reflected

Probe

Outputs at IF updated every 10 ns

*cav\_elec.v*

to additional cavities