

Cavity Simulator in FPGA

Larry Doolittle, LBNL, June 2014

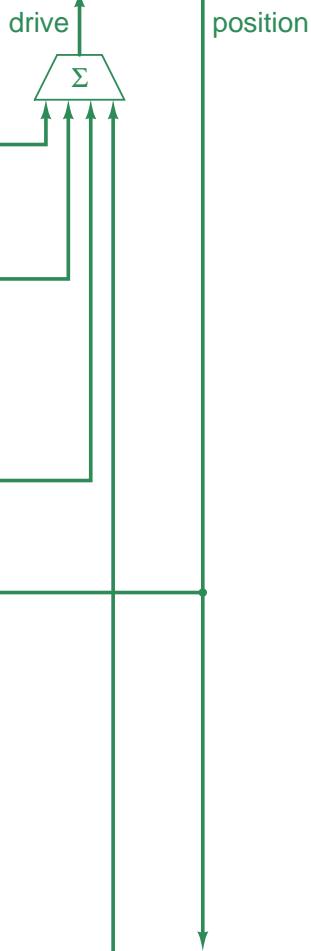
(abridged)

Clocks at ~200 MHz in Xilinx 7Axxx
8 cavity-controller pairs could fit on AC701?

m mechanical modes updated every $2m$ cycles

Mechanical eigenmode propagator
 $zy = My + d$

resonator.v



Gaussian noise
Environmental sources?

outer
outer_prod.v

Piezo control

Virtual Piezo

V
outer
outer_prod.v

Beam timing

Cavity electromagnetics simulator

Electromagnetic eigenmode propagator (π mode)
cav_mode.v

v^2
outer
outer_prod.v

$\Delta\omega$
dot
dot_prod.v

Electromagnetic eigenmode propagator ($8\pi/9$ mode)
cav_mode.v

v^2
outer
outer_prod.v

$\Delta\omega$
dot
dot_prod.v

Drive
IQ

Forward

Reflected

Probe

Outputs at IF updated every 10 ns

cav_elec.v

to additional cavities