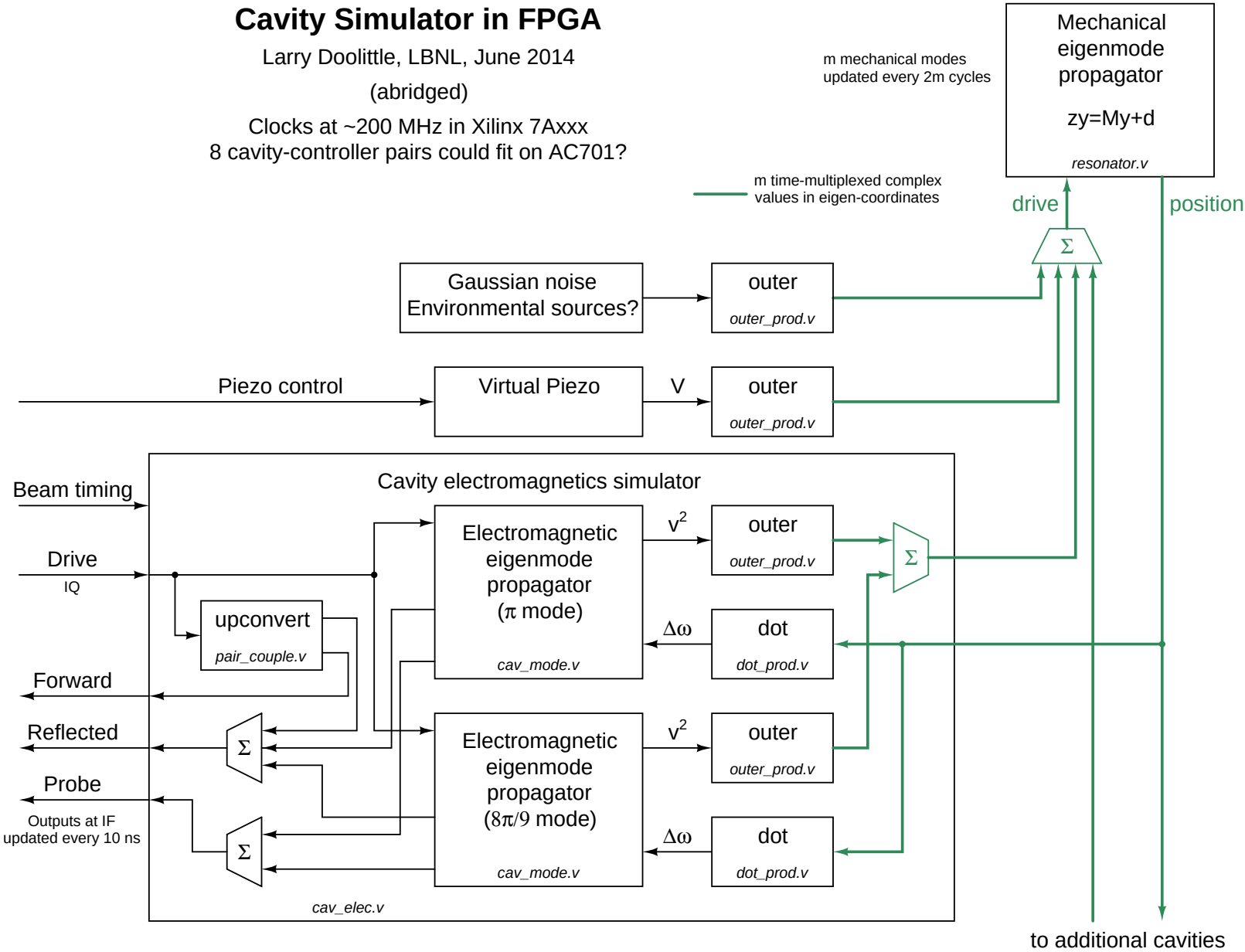
# Cavity Simulator in FPGA

Larry Doolittle, LBNL, June 2014

(abridged)

Clocks at ~200 MHz in Xilinx 7Axxx
8 cavity-controller pairs could fit on AC701?