

# Cavity Simulator in FPGA

Larry Doolittle, LBNL, June 2014

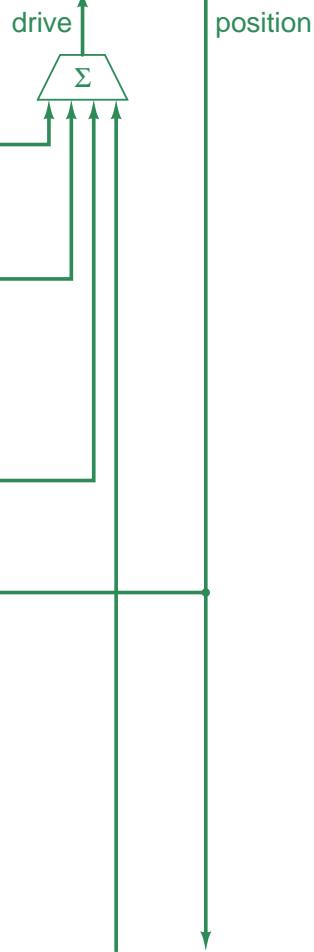
(abridged)

Clocks at ~200 MHz in Xilinx 7Axxx  
8 cavity-controller pairs could fit on AC701?

$m$  mechanical modes updated every  $2m$  cycles

Mechanical eigenmode propagator  
 $zy = My + d$

*resonator.v*



Gaussian noise  
Environmental sources?

outer  
outer\_prod.v

Piezo control

Virtual Piezo

V  
outer  
outer\_prod.v

Beam timing

Cavity electromagnetics simulator

Electromagnetic eigenmode propagator ( $\pi$  mode)  
cav\_mode.v

$v^2$   
outer  
outer\_prod.v

$\Delta\omega$   
dot  
dot\_prod.v

Electromagnetic eigenmode propagator ( $8\pi/9$  mode)  
cav\_mode.v

$v^2$   
outer  
outer\_prod.v

$\Delta\omega$   
dot  
dot\_prod.v

Drive  
IQ

Forward

Reflected

Probe

Outputs at IF updated every 10 ns

cav\_elec.v

to additional cavities