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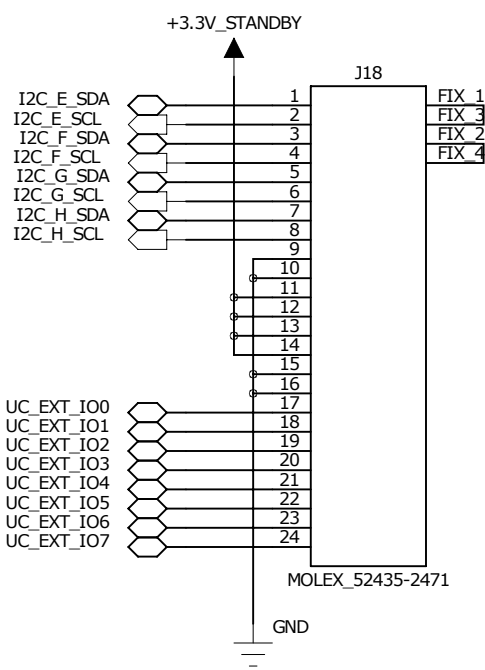
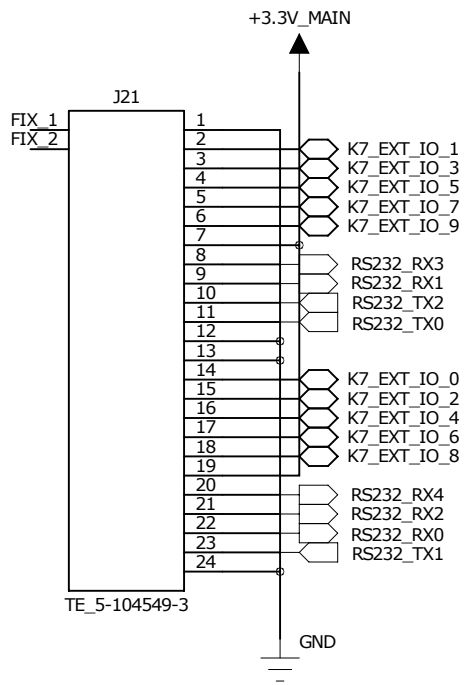
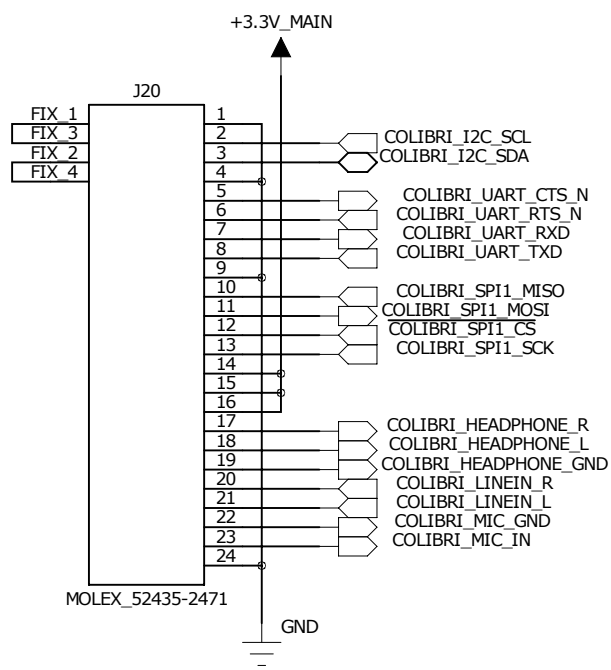
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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



Fixing holes

- 1 J1 MOUNT_HOLE
- 1 J3 MOUNT_HOLE
- 1 J5 MOUNT_HOLE
- 1 J6 MOUNT_HOLE
- 1 J22 MOUNT_HOLE

COMPANY: LBNL-ATG			
TITLE: EXTERNAL_IO			
CODE:	SIZE:	DRAWING NO:	REV:
<Code>	A2	BMB7	1
SCALE: <Scale>		SHEET: 2 OF 30	

DRAWN: John Jones	DATED: 25.2.13
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

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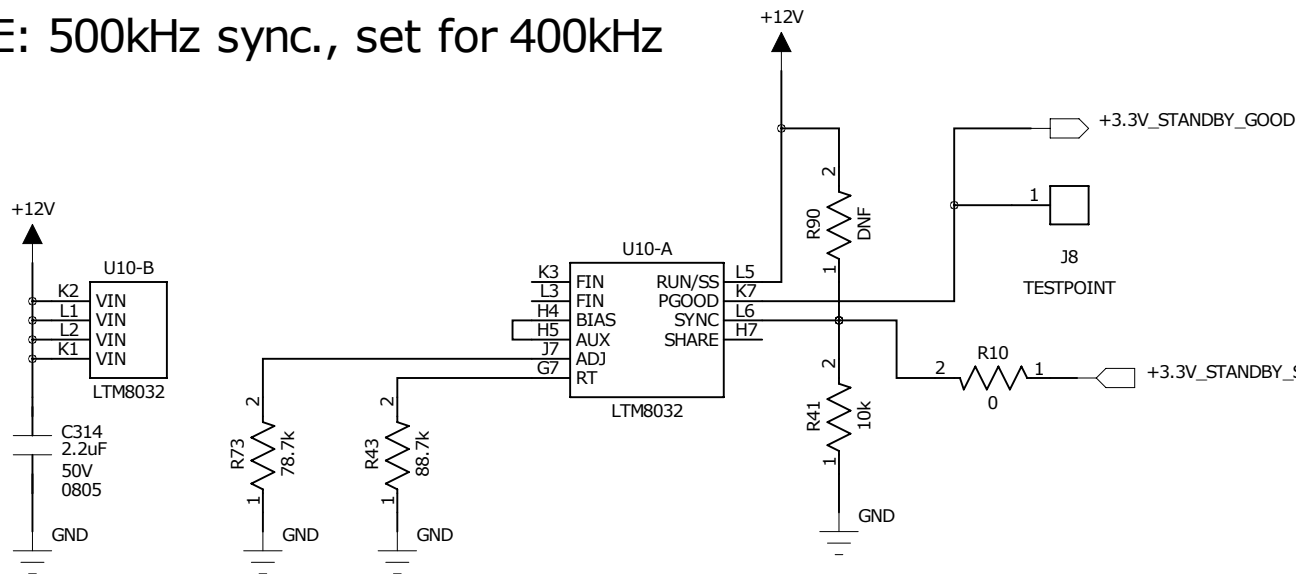
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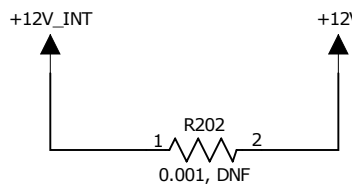
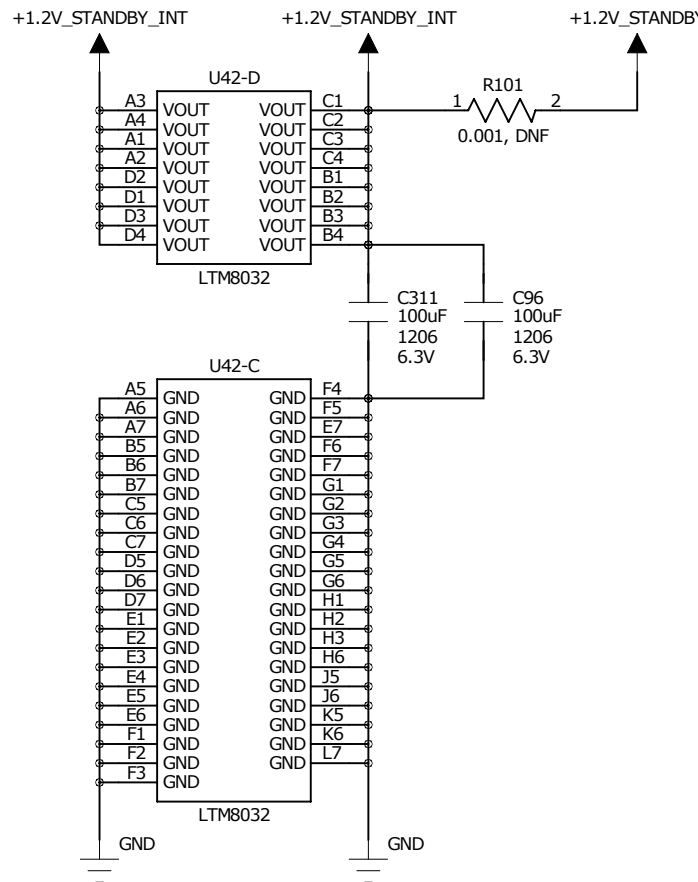
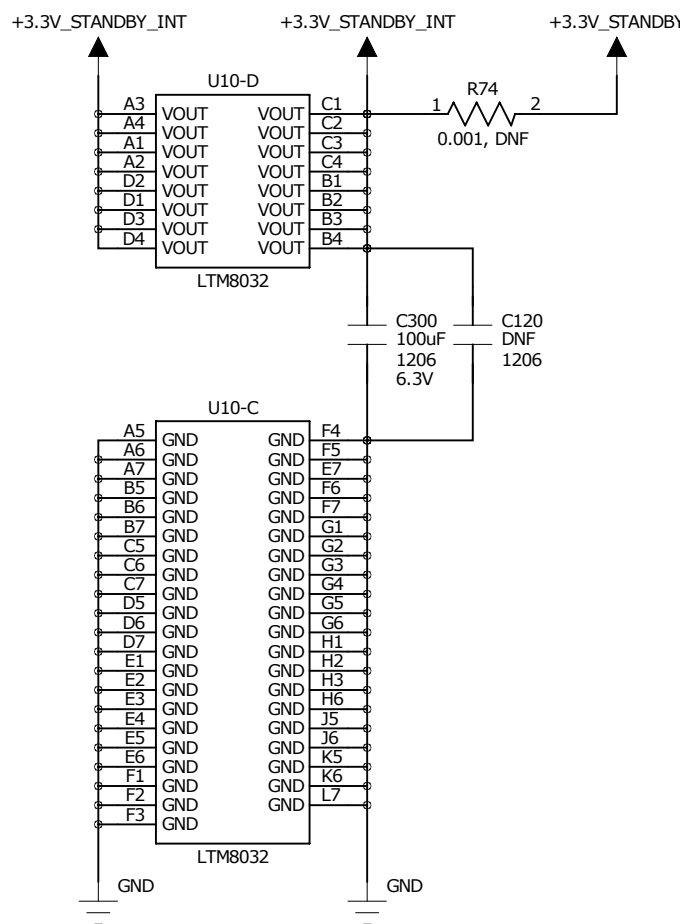
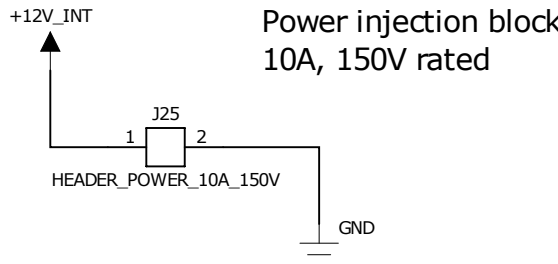
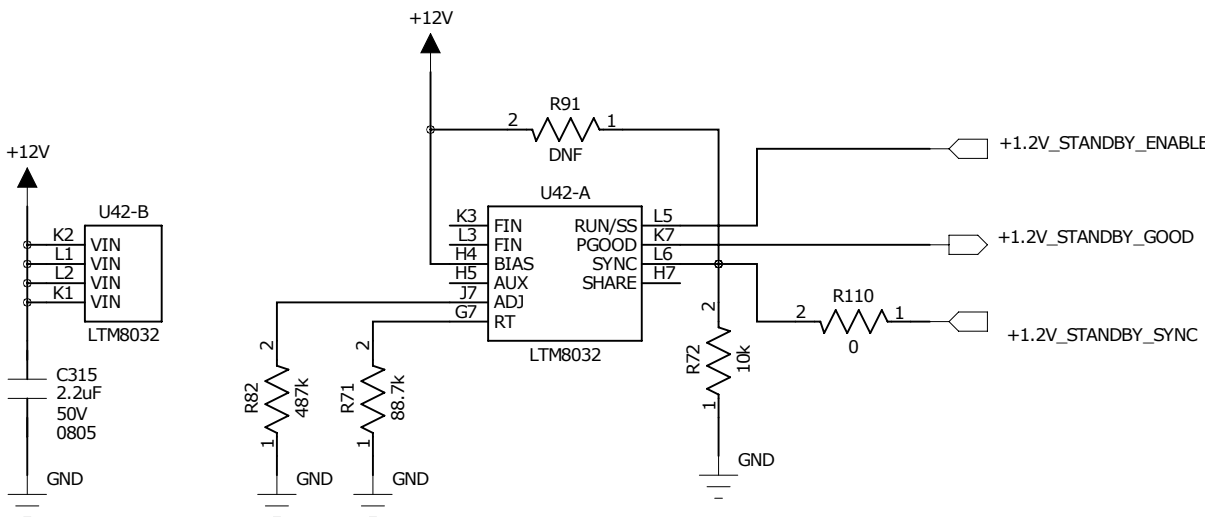
NOTE: Optimal frequency depends on output and input values, set 20% below for synchronization
NOTE: Regulators typically operate in burst mode but if too noisy can override
NOTE: +3.3V_STANDBY is expected to always be on

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

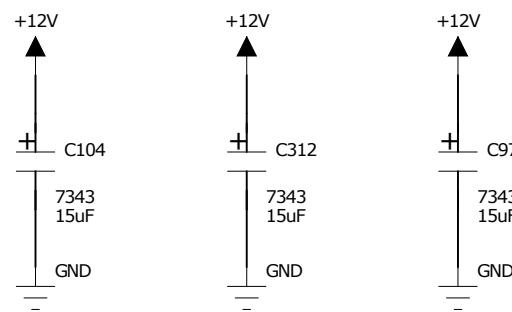
NOTE: 500kHz sync., set for 400kHz



NOTE: 500kHz sync., set for 400kHz



Place between LTMs



+3.3V_STANDBY powers: Ethernet VDDH (108mA)
WIFI VCC (250mA)
Atmel AT32UC3A (370mA)
USB 2.0 OTG (850mA)
I2C bus and port expanders

+1.2V_STANDBY powers: Ethernet VDDL (221mA)
WIFI DVDD (100mA)
GTX for S6 & K7 (via FET switch)

DRAWN:	John Jones	DATED:	25.2.13	COMPANY: LBNL-ATG			
CHECKED:	<Checked By>	DATED:	<Checked Date>	TITLE: STANDBY_POWER			
QUALITY CONTROL:	<QC By>	DATED:	<QC Date>	CODE:	SIZE: A2	DRAWING NO: BMB7	REV: 1
RELEASED:	<Released By>	DATED:	<Release Date>	SCALE: <Scale>			SHEET: 30F 30

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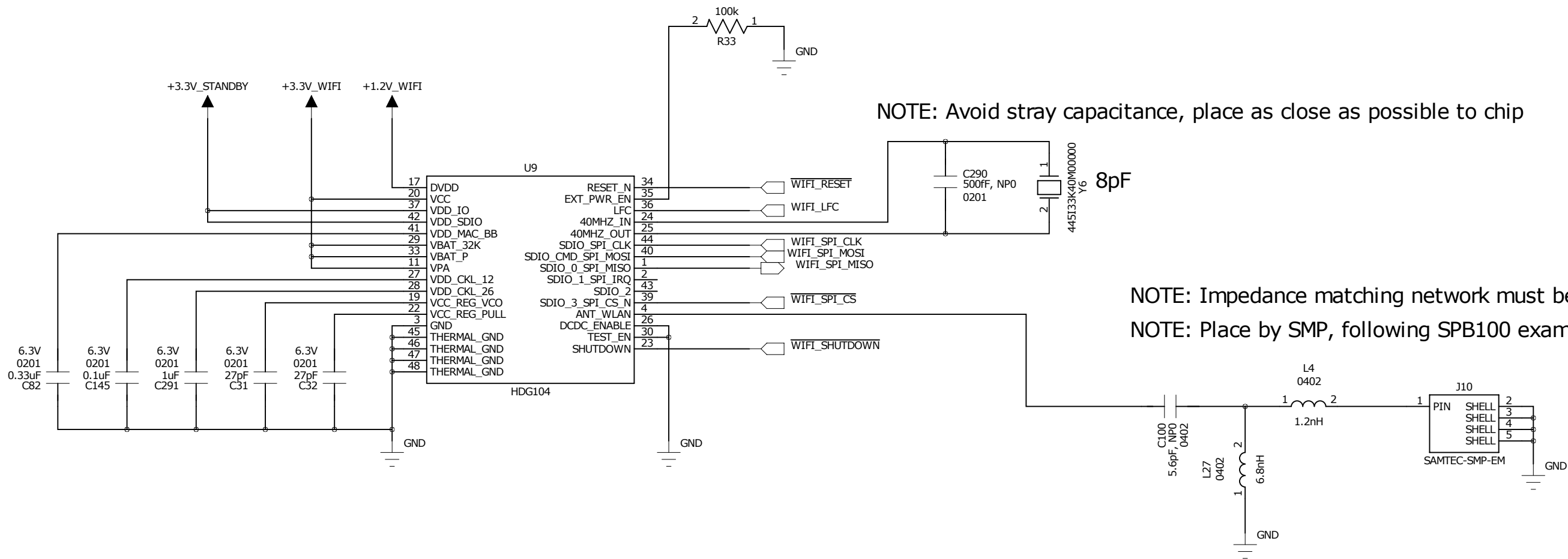
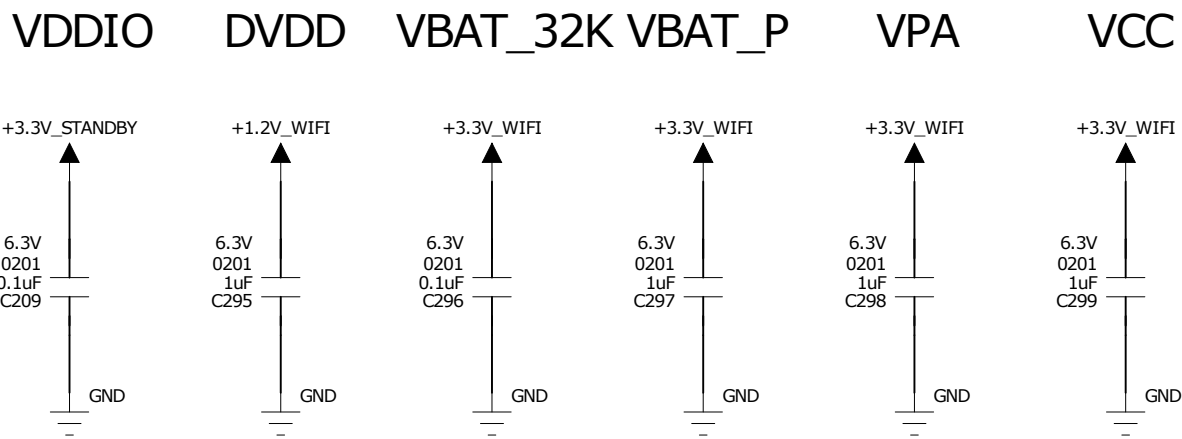
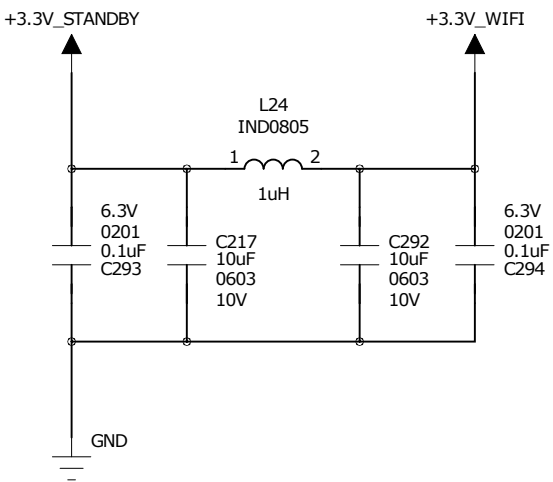
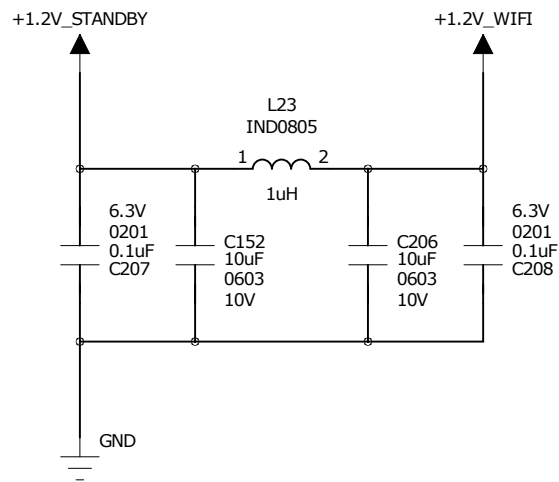
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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



NOTE: Avoid stray capacitance, place as close as possible to chip

NOTE: Impedance matching network must be carefully laid out

NOTE: Place by SMP, following SPB100 example

COMPANY: LBNL-ATG			
TITLE: WIFI			
DRAWN: John Jones	DATED: 25.2.13	CODE: <Code>	SIZE: A2
CHECKED: <Checked By>	DATED: <Checked Date>	DRAWING NO: BMB7	REV: 1
QUALITY CONTROL: <QC By>	DATED: <QC Date>	SCALE: <Scale>	SHEET: 7 of 30
RELEASED: <Released By>	DATED: <Release Date>		

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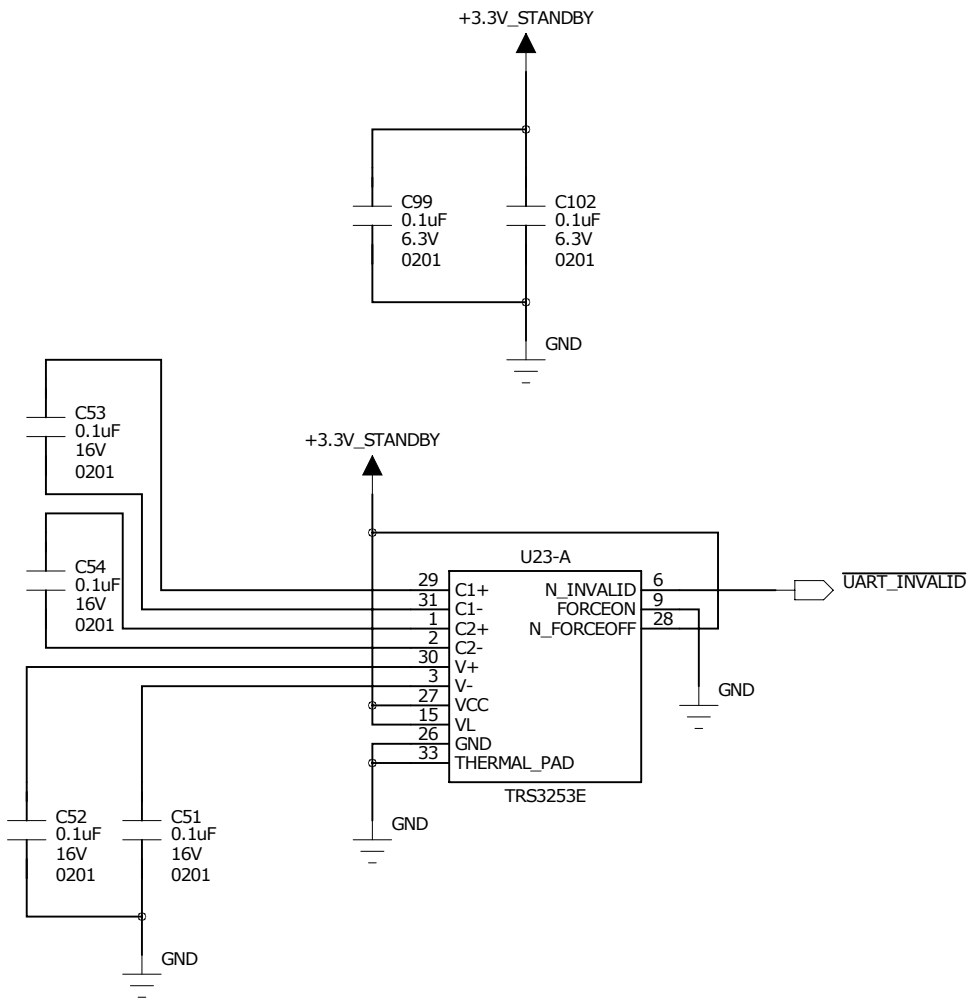
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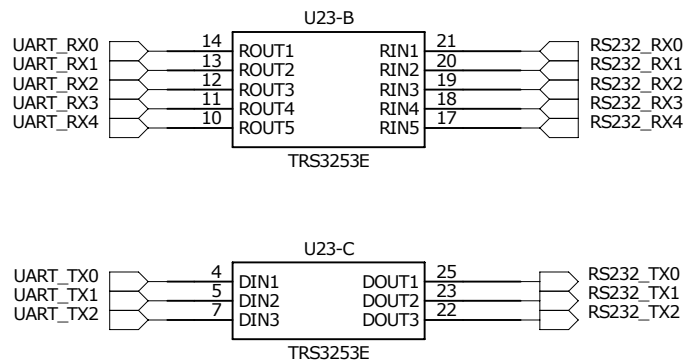
NOTE: 1 x TX & 1 x RX wired to microcontroller
NOTE: 2 x TX & 4 x RX wired to Spartan 6

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



LOGIC

RS-232



COMPANY:		LBNL-ATG		
TITLE: RS-232				
>	CODE:	SIZE:	DRAWING NO:	REV:
<Code>	A2	BMB7		1
SCALE: <Scale>			SHEET: 8 of 30	

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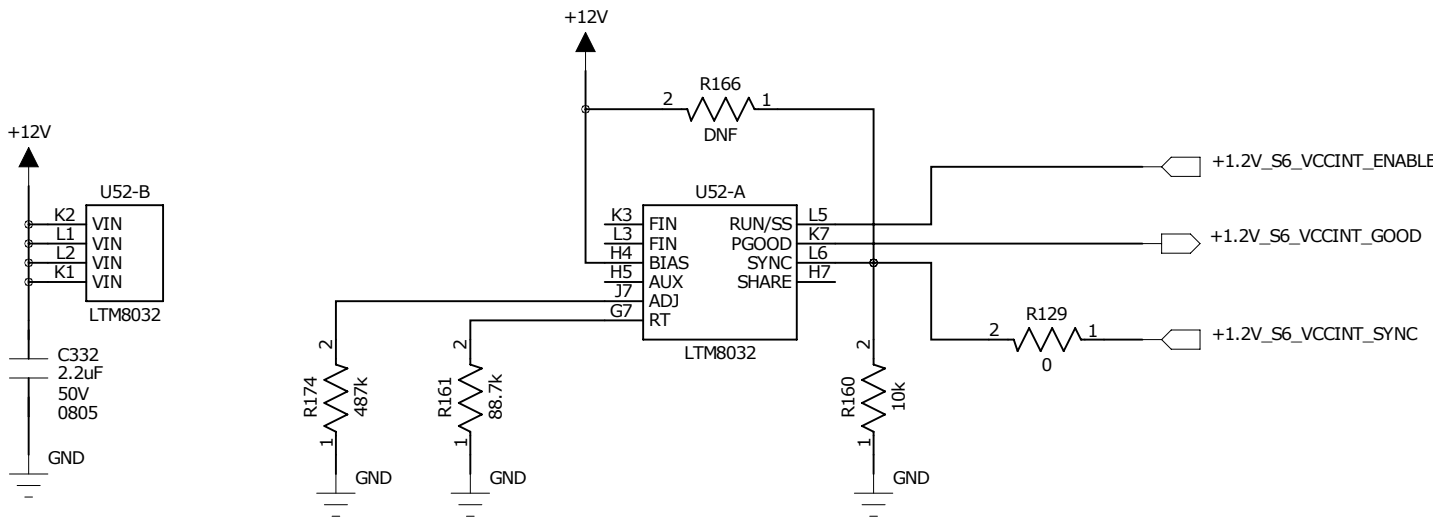
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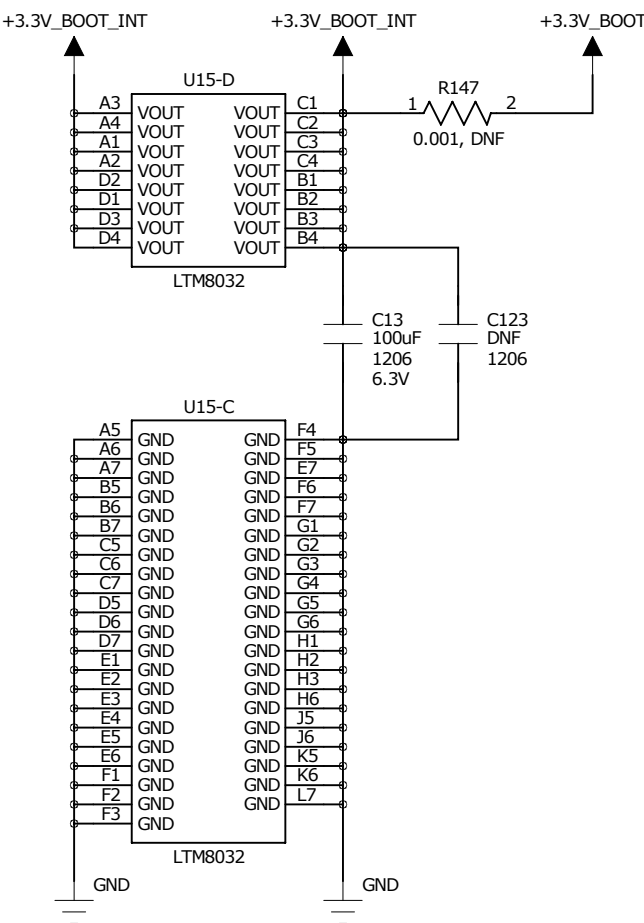
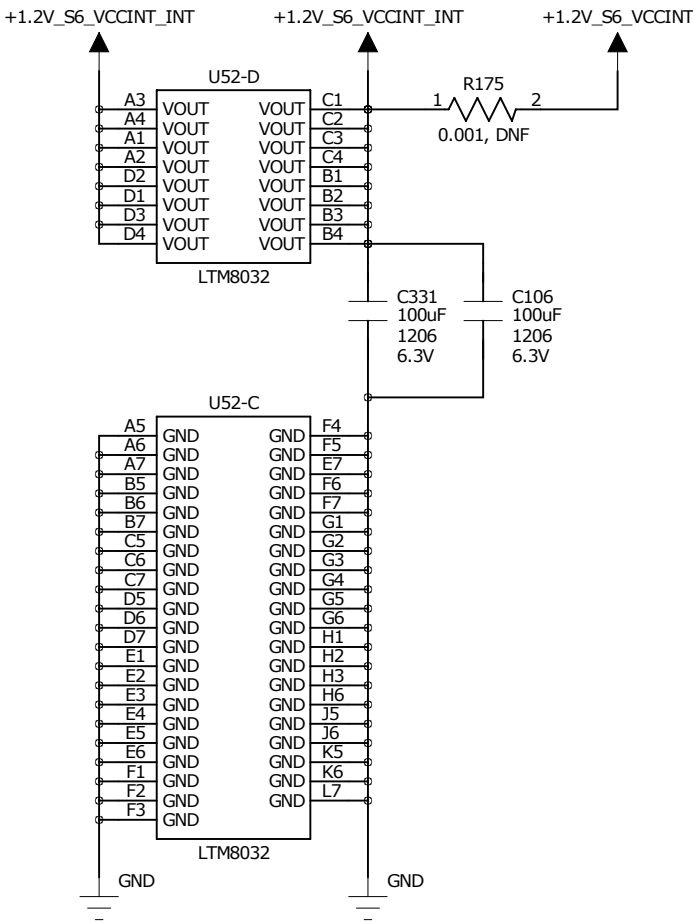
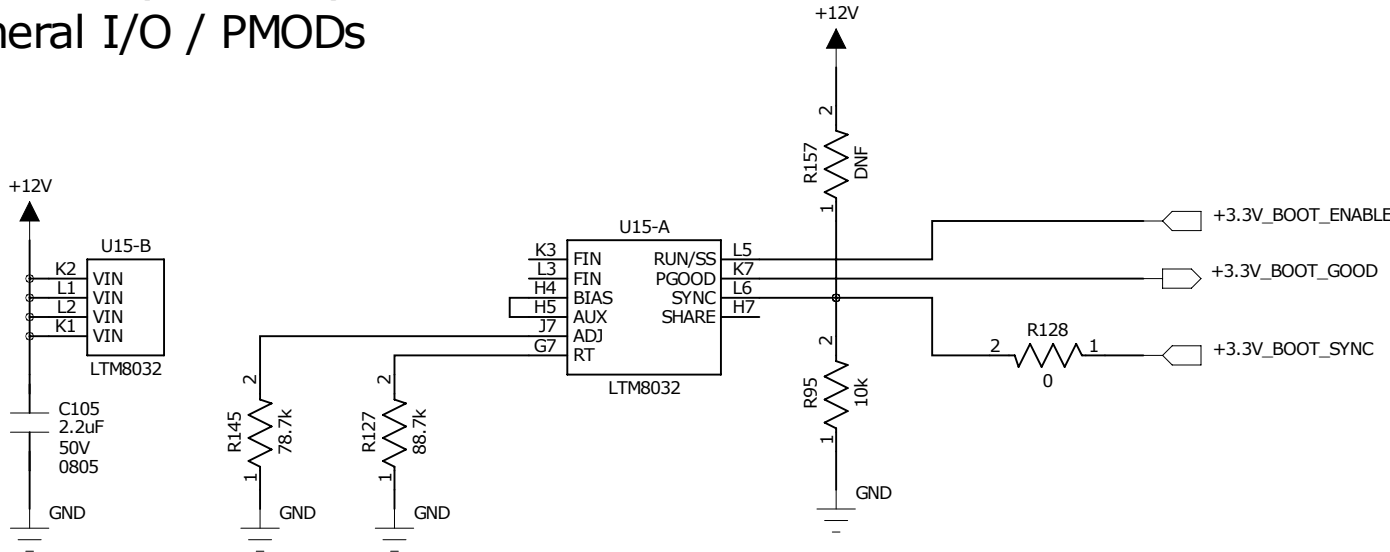
NOTE: 500kHz sync., set for 400kHz

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Spartan-6 core +1.2V (up to 2A)



+3.3V powers: Spartan-6 I/O
SFP (~1.2A)
CDCE62005 (~515mA)
Peripheral I/O / PMODs

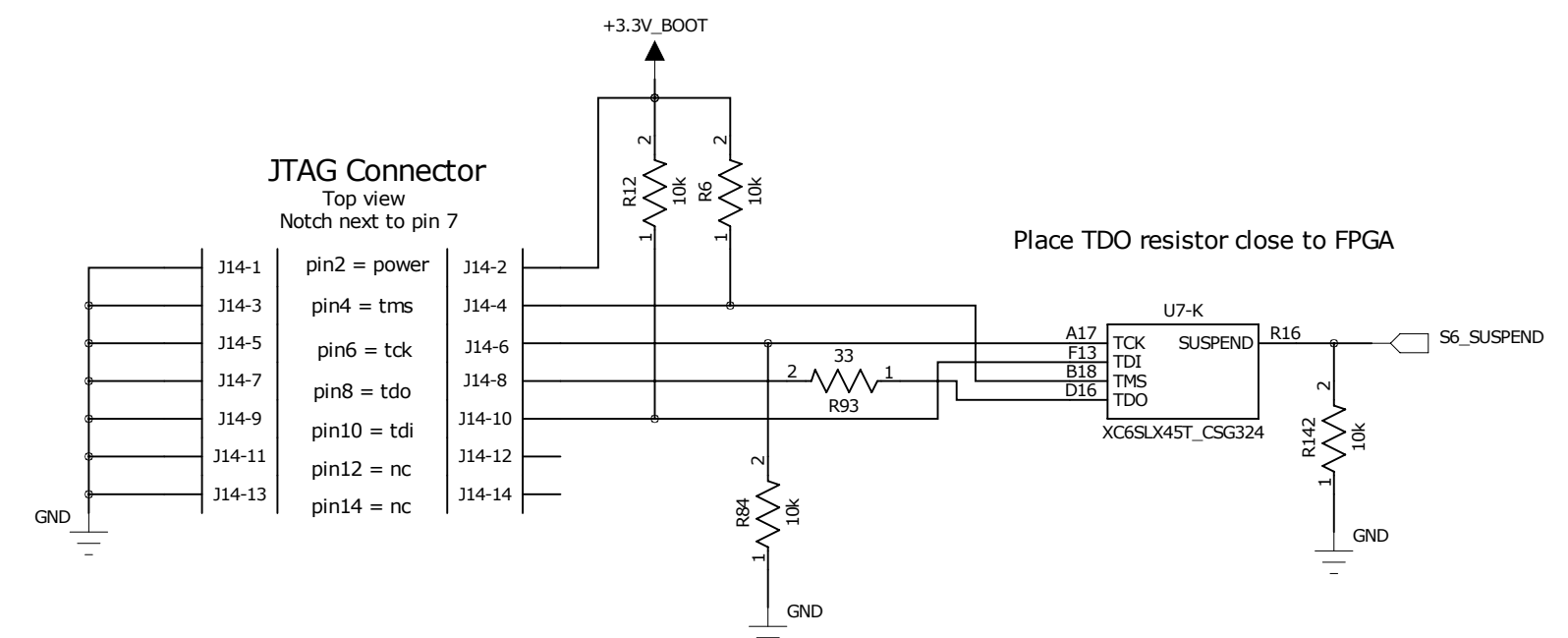
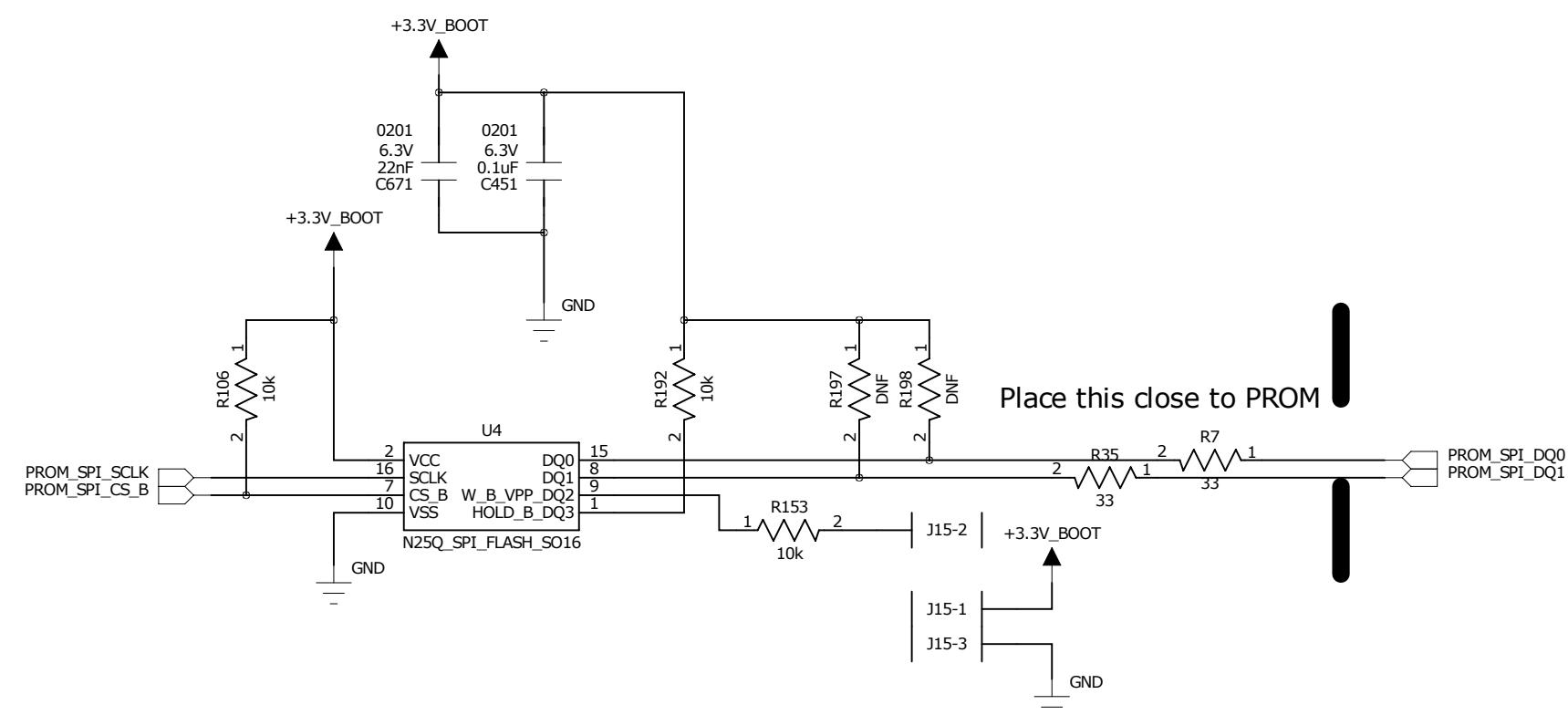
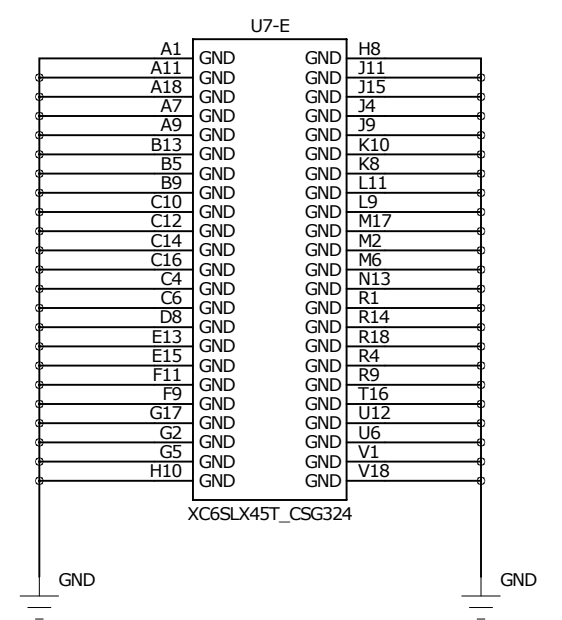
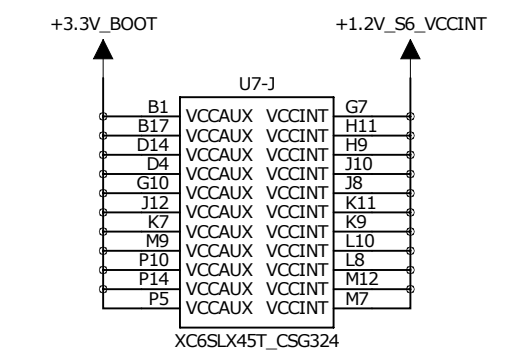
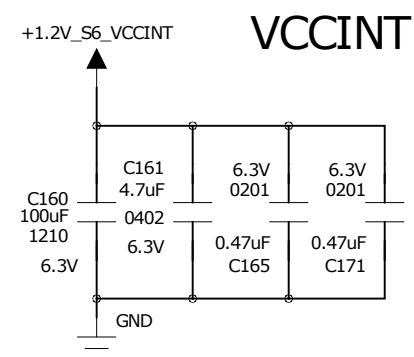
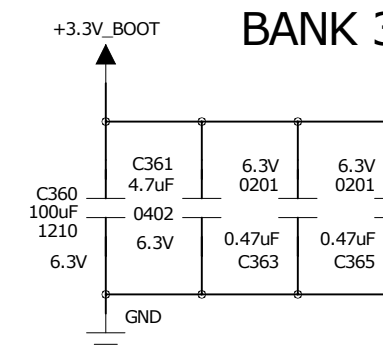
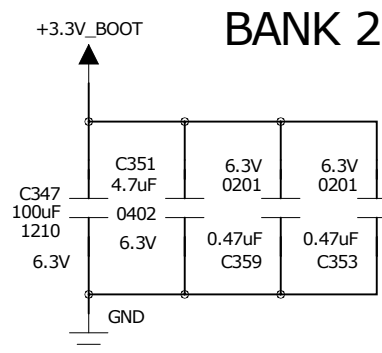
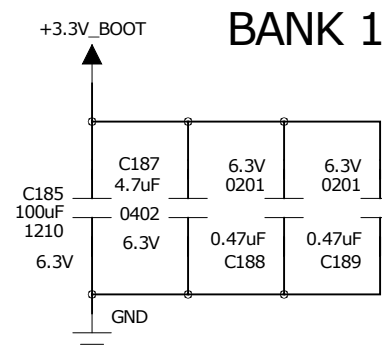
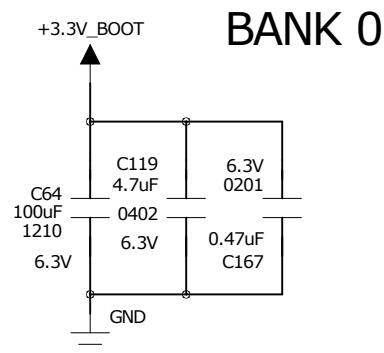
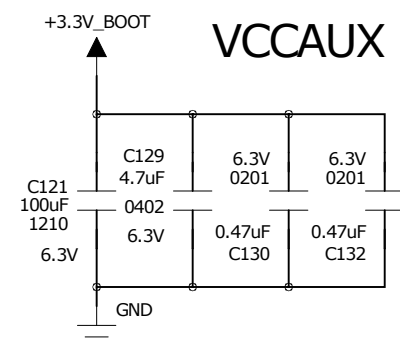


COMPANY: LBNL-ATG			
TITLE: BOOT_POWER			
DRAWN: John Jones	DATED: 25.2.13	CODE: <Code>	SIZE: A2
CHECKED: <Checked By>	DATED: <Checked Date>	DRAWING NO: BMB7	REV: 1
QUALITY CONTROL: <QC By>	DATED: <QC Date>	SCALE: <Scale>	
RELEASED: <Released By>	DATED: <Release Date>	SHEET: 1 of 30	

NOTE: S6 decoupling from UG393

NOTE: S6 VCCAUX IS +3.3V - marginally higher power dissipation on VCCAUX but simpler power etc...

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



DRAWN: John Jones		DATED: 25.2.13		S6_POWER_CFG			
CHECKED: <Checked By>		DATED: <Checked Date>		CODE: <Code>	SIZE: A2	DRAWING NO: BMB7	REV: 1
QUALITY CONTROL: <QC By>		DATED: <QC Date>					
RELEASED: <Released By>		DATED: <Release Date>		SCALE: <Scale>			SHEET: 12 30

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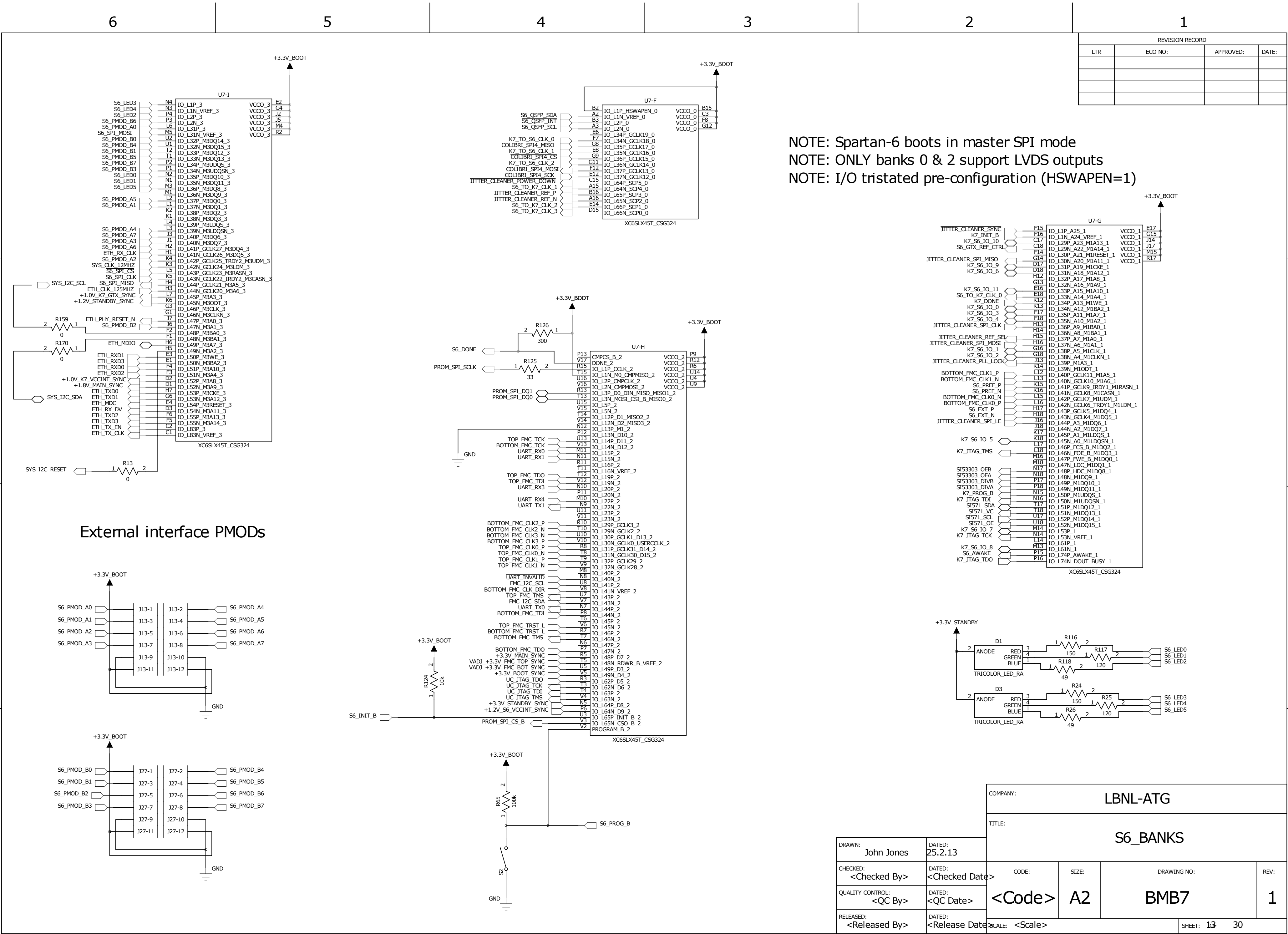
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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

NOTE: Spartan-6 boots in master SPI mode
NOTE: ONLY banks 0 & 2 support LVDS outputs
NOTE: I/O tristated pre-configuration (HSWAPEN=1)



COMPANY:		LBNL-ATG			
TITLE:		S6_BANKS			
DRAWN:	John Jones	DATED:	25.2.13	CODE:	<Code>
CHECKED:	<Checked By>	DATED:	<Checked Date>	SIZE:	A2
QUALITY CONTROL:	<QC By>	DATED:	<QC Date>	DRAWING NO:	BMB7
RELEASED:	<Released By>	DATED:	<Release Date>	REV:	1
SCALE: <Scale>				SHEET: 13 30	

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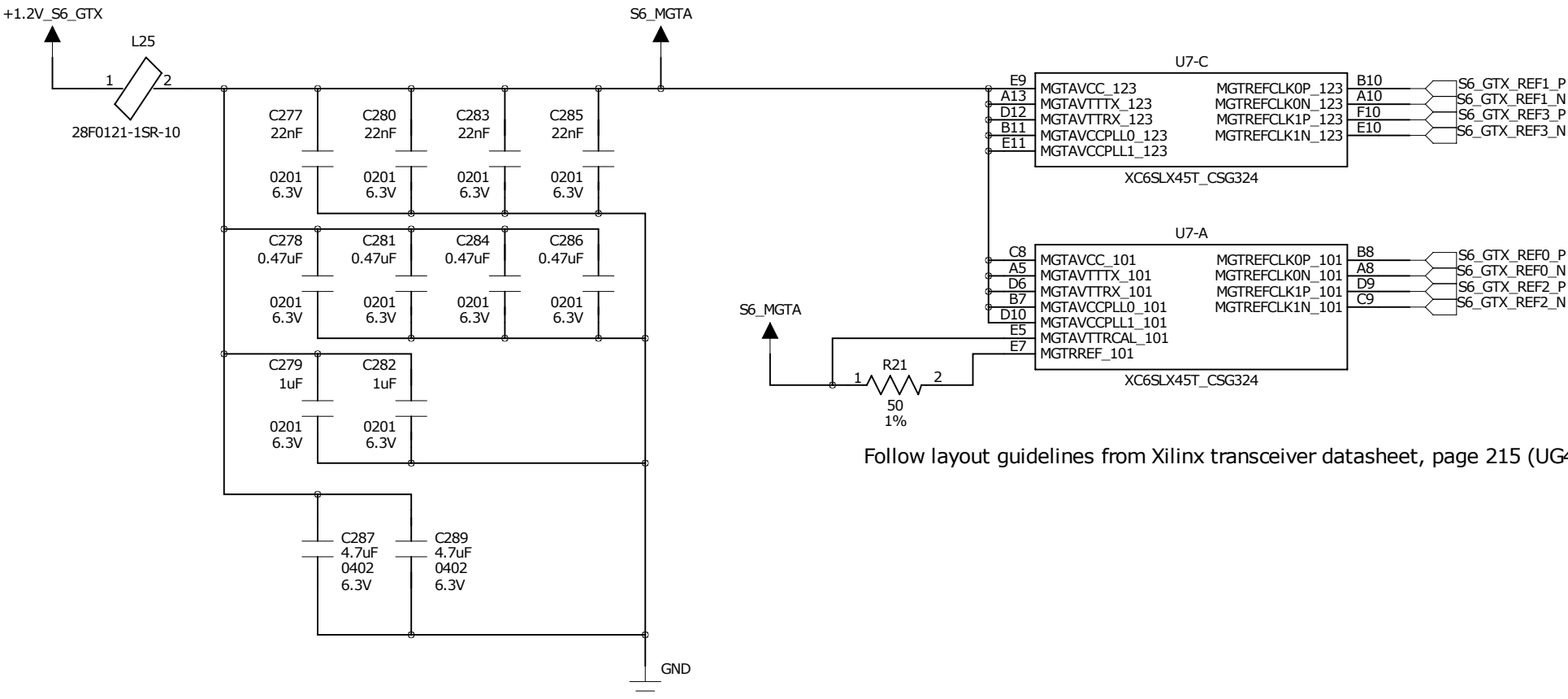
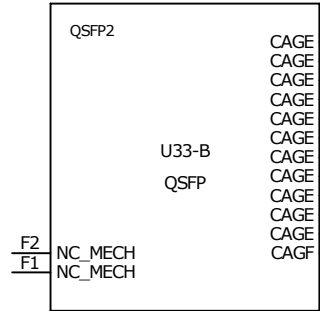
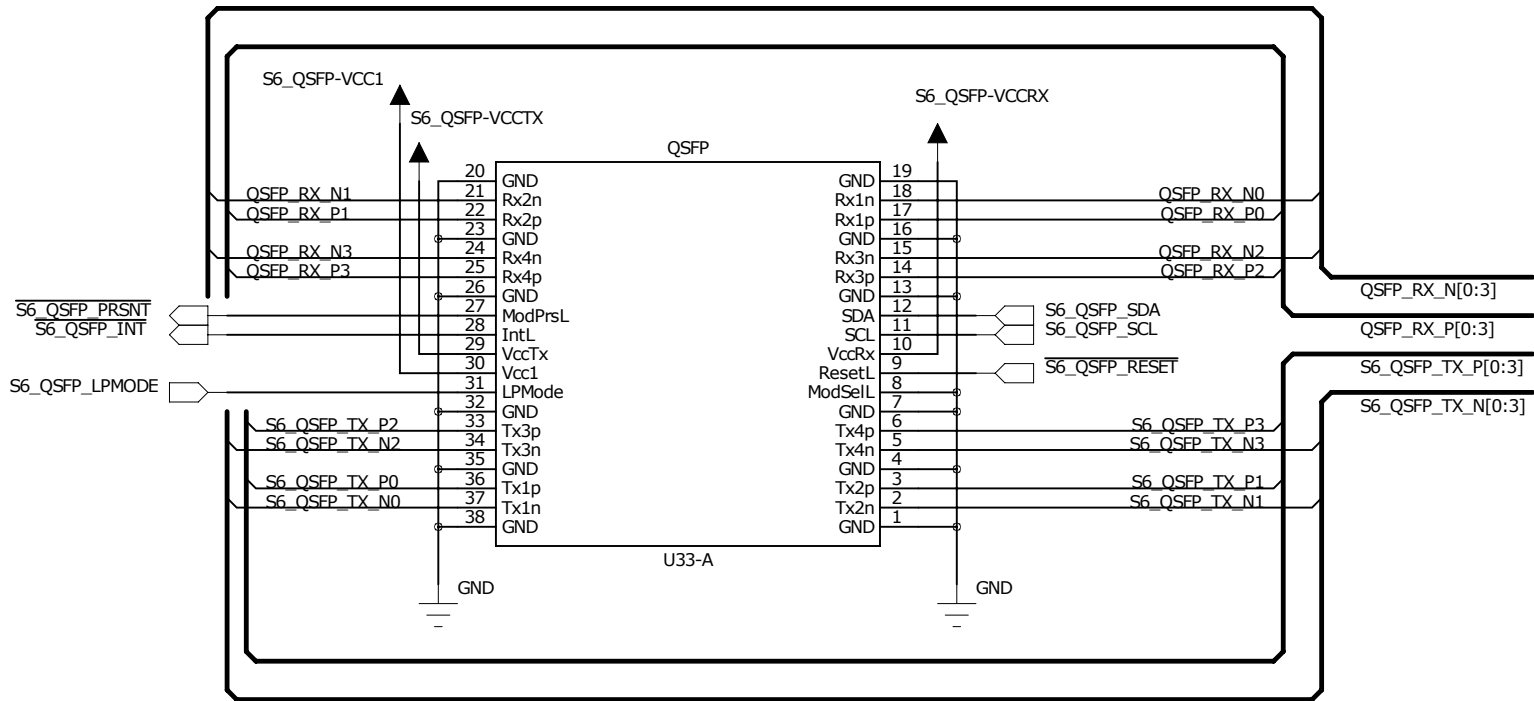
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NOTE: S6 internal pullup between 6.6k & 15k

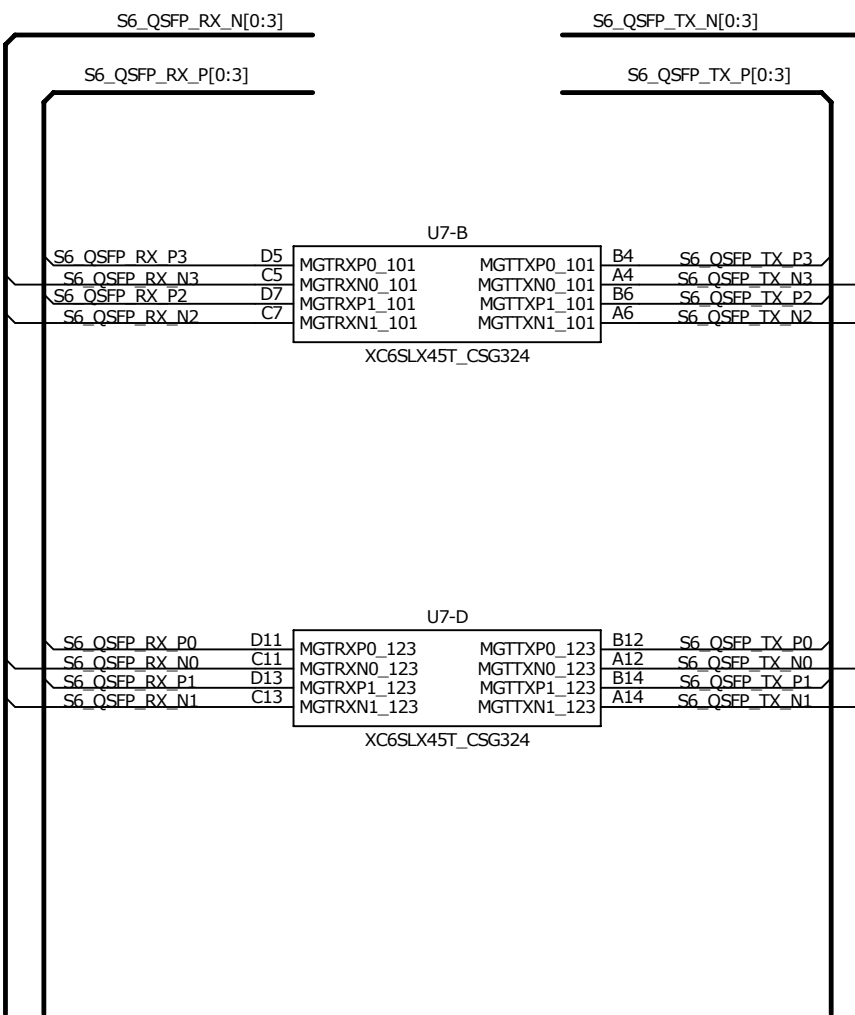
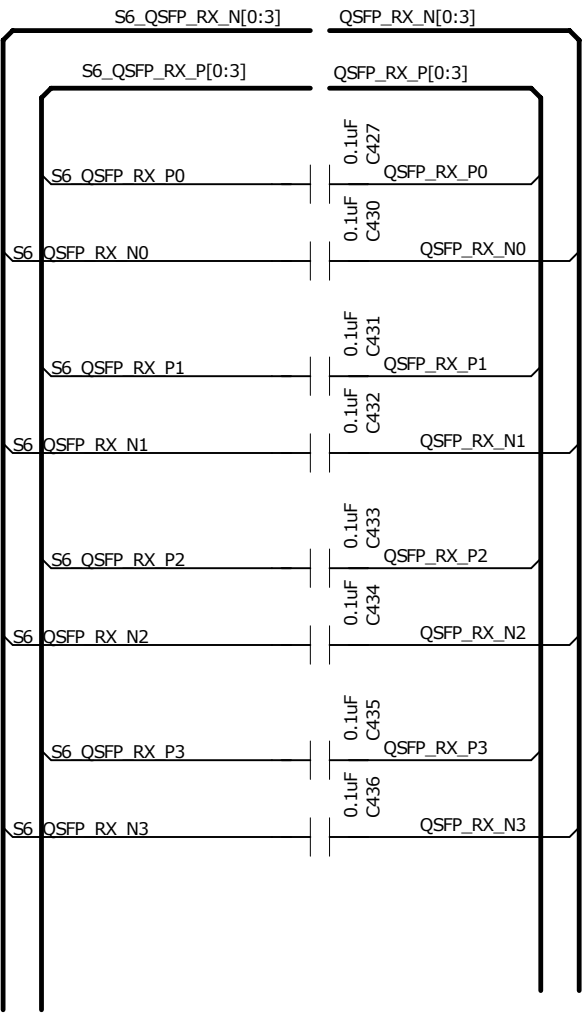
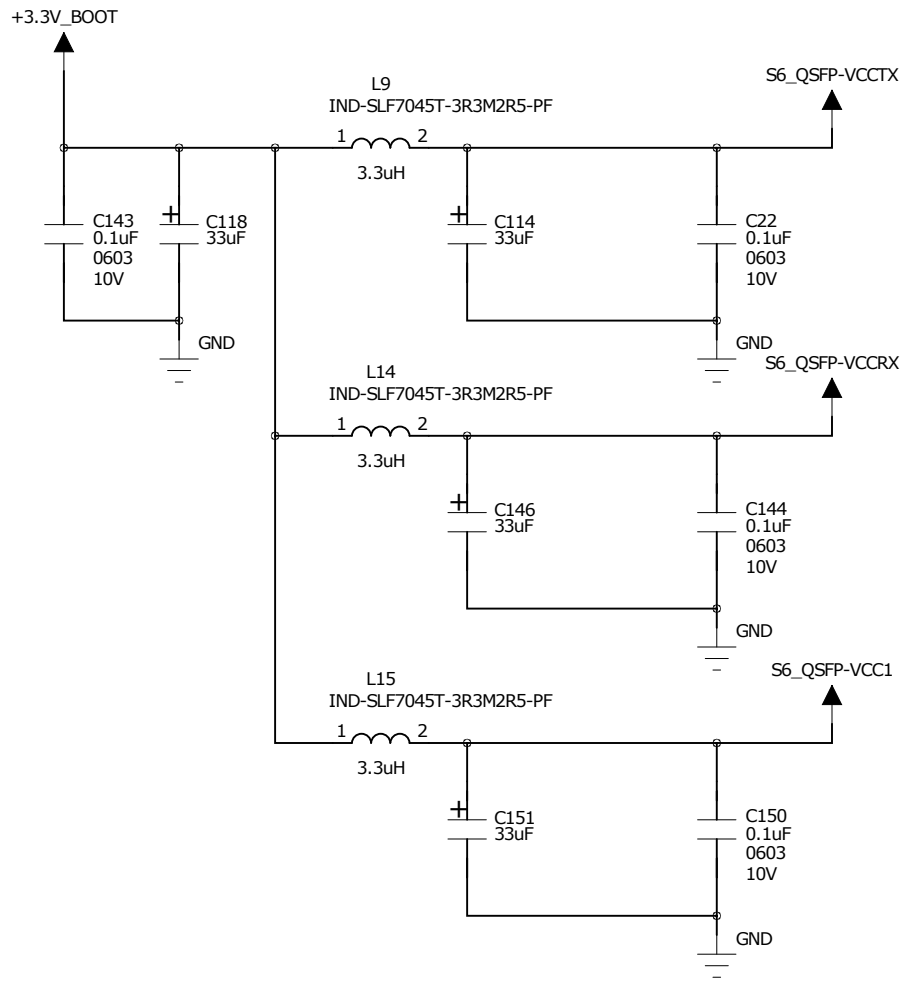
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

S6_QSFP



Follow layout guidelines from Xilinx transceiver datasheet, page 215 (UG476)

Smaller inductors/caps are available if it helps with layout.



COMPANY: LBNL-ATG			
TITLE: S6_QSFP			
DRAWN: John Jones	DATED: 25.2.13	CODE: <Code>	SIZE: A2
CHECKED: <Checked By>	DATED: <Checked Date>	DRAWING NO: BMB7	REV: 1
QUALITY CONTROL: <QC By>	DATED: <QC Date>	SCALE: <Scale>	SHEET: 14 30
RELEASED: <Released By>	DATED: <Release Date>		

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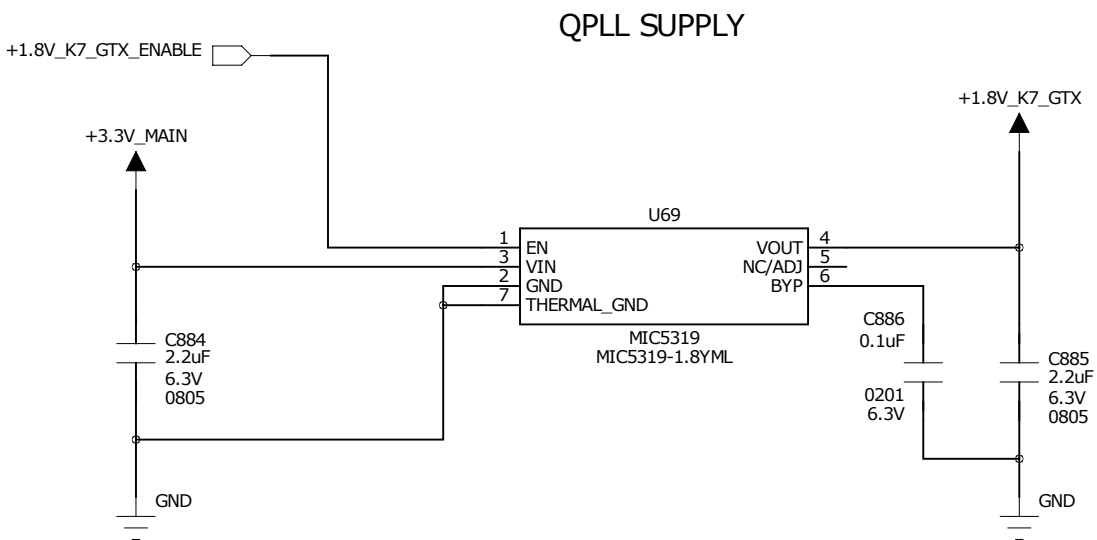
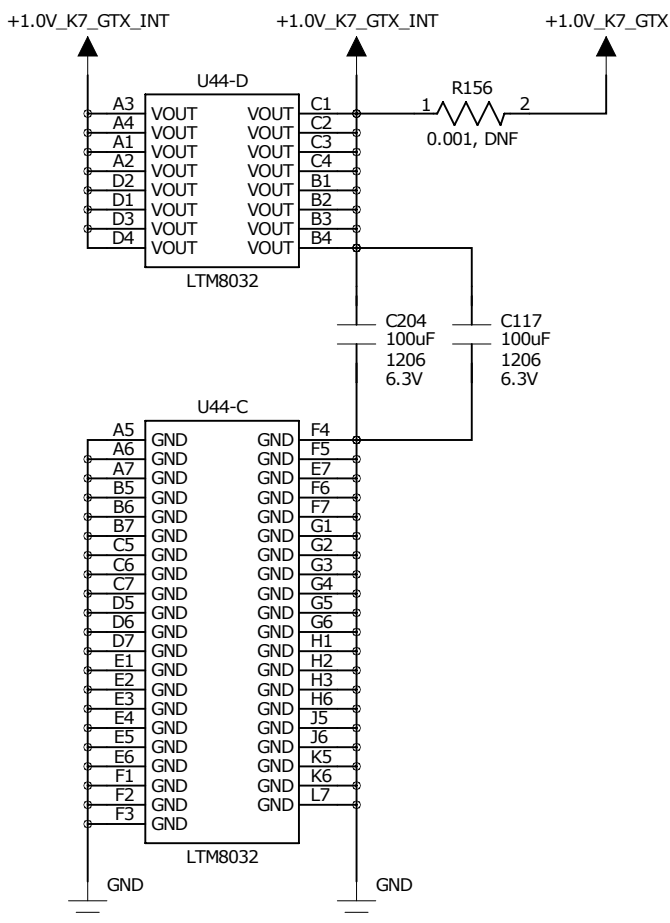
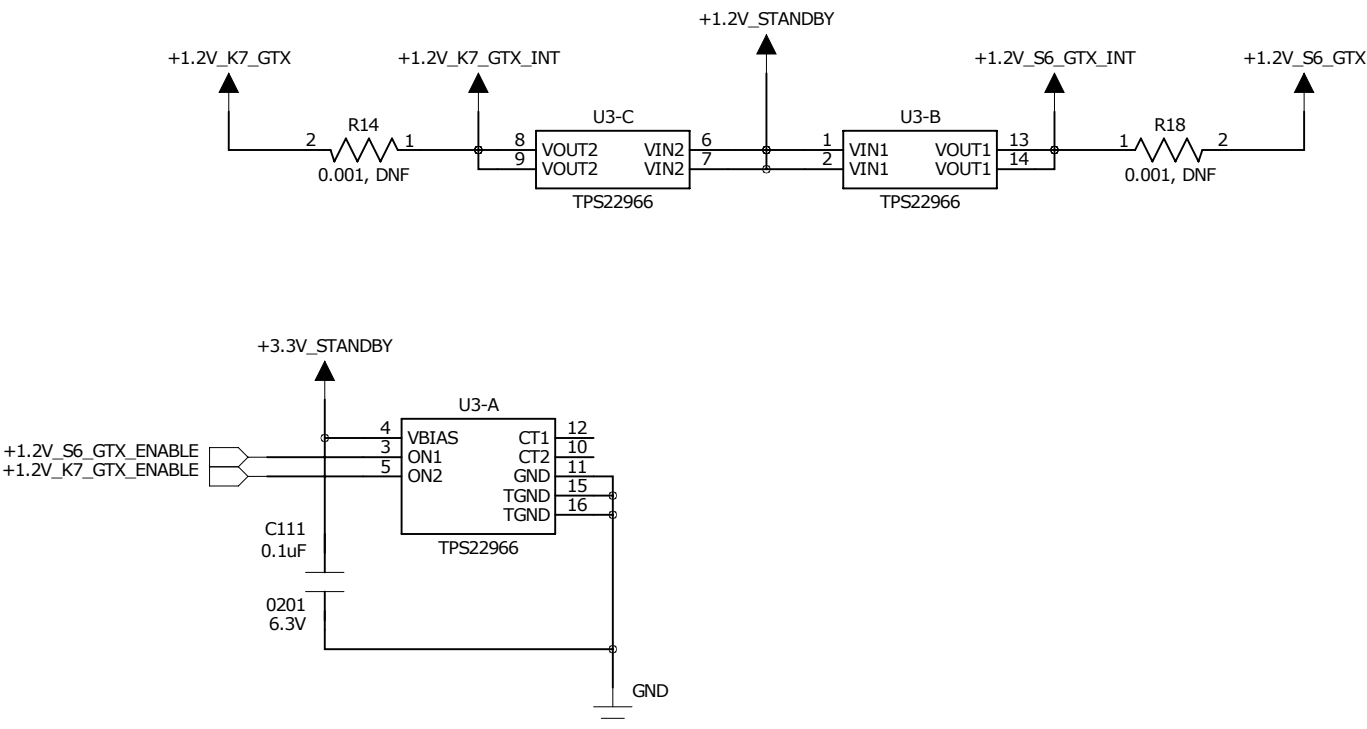
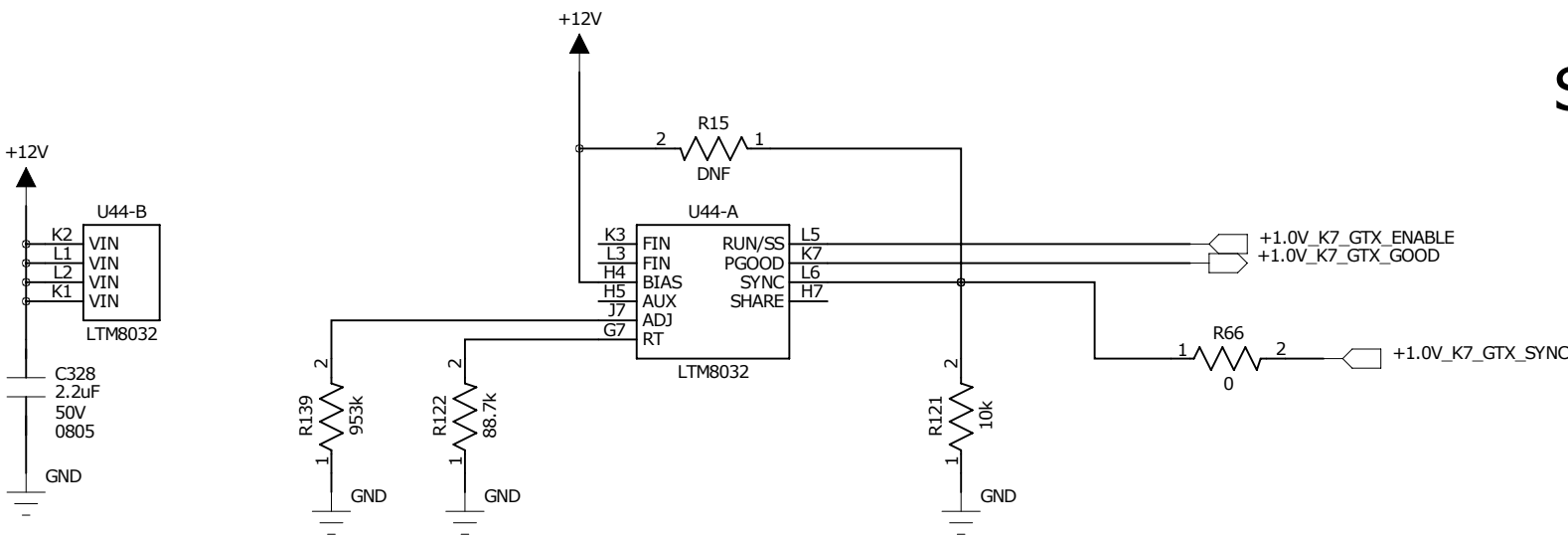
NOTE: +1.2V power is FET switched from the +1.2V_STANDBY supply

NOTE: Currently designed to operate from +4.75V to +15V at 500kHz when synchronized, but 400kHz when in freerun as per datasheet

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

Spartan-6 GTP +1.2V (~500mA)

Kintex-7 GTX +1.2V (~500mA)



COMPANY:				LBNL-ATG			
TITLE:				GT_POWER			
DRAWN:	John Jones	DATED:	25.2.13	CODE:	SIZE:	DRAWING NO:	REV:
CHECKED:	<Checked By>	DATED:	<Checked Date>	<Code>	A2	BMB7	1
QUALITY CONTROL:	<QC By>	DATED:	<QC Date>	SCALE: <Scale>			
RELEASED:	<Released By>	DATED:	<Release Date>	SHEET: 15 30			

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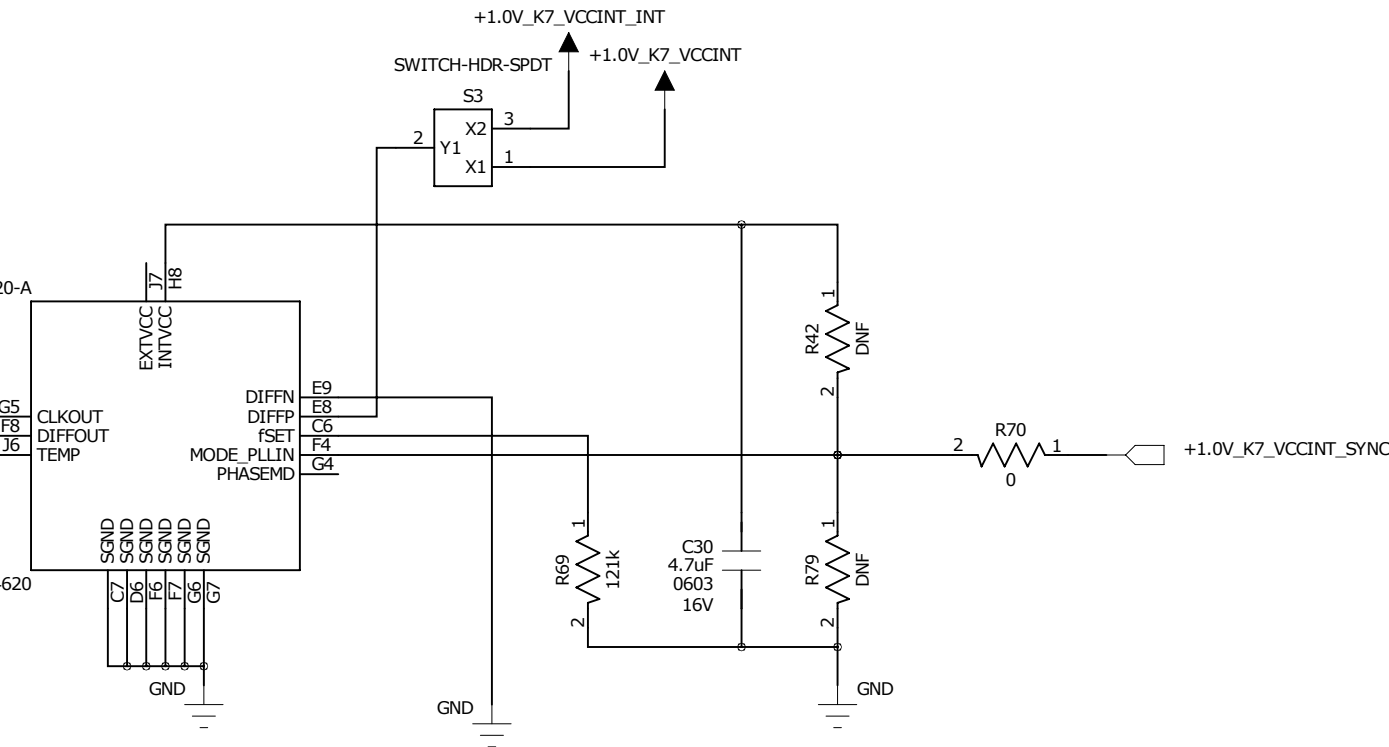
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Kintex 7 FPGA VCCINT = +1.0V, 26A

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

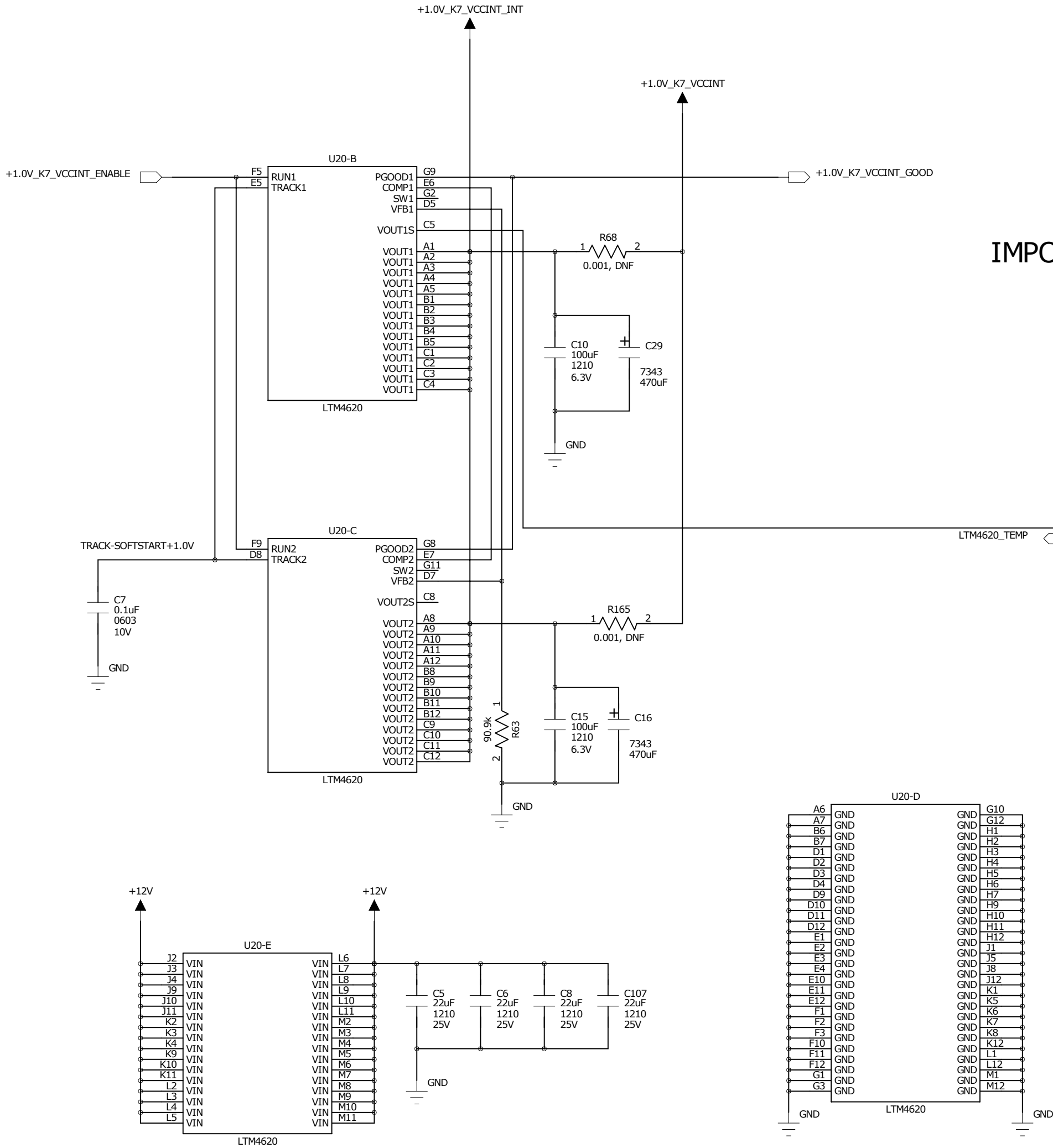
NOTE: fSET for 500kHz
NOTE: Burst mode when clock not supplied

IMPORTANT: Must be set to either local or remote voltage



Remote Sense
Run tracks to FPGA core
Make sure connection only made to power/gnd under fpga

fSET - 10uA current source - target 1.2V
 $R = 1.2 * 100000 = 120k$



COMPANY: LBNL-ATG			
TITLE: K7_VCCINT_POWER			
DRAWN: John Jones	DATED: 25.2.13	CODE: <Code>	SIZE: A2
CHECKED: <Checked By>	DATED: <Checked Date>	DRAWING NO: BMB7	REV: 1
QUALITY CONTROL: <QC By>	DATED: <QC Date>	SCALE: <Scale>	SHEET: 16 30
RELEASED: <Released By>	DATED: <Release Date>		

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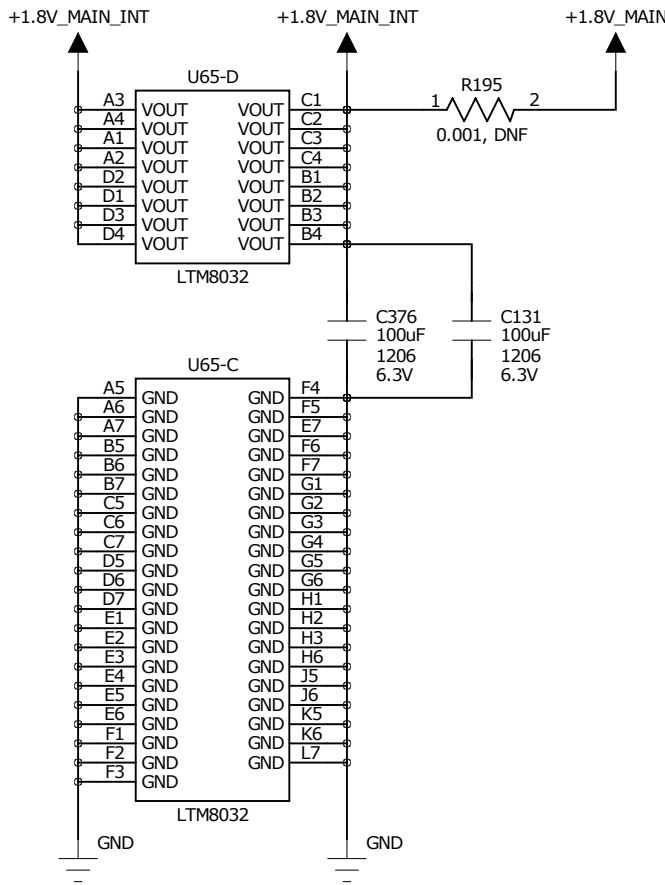
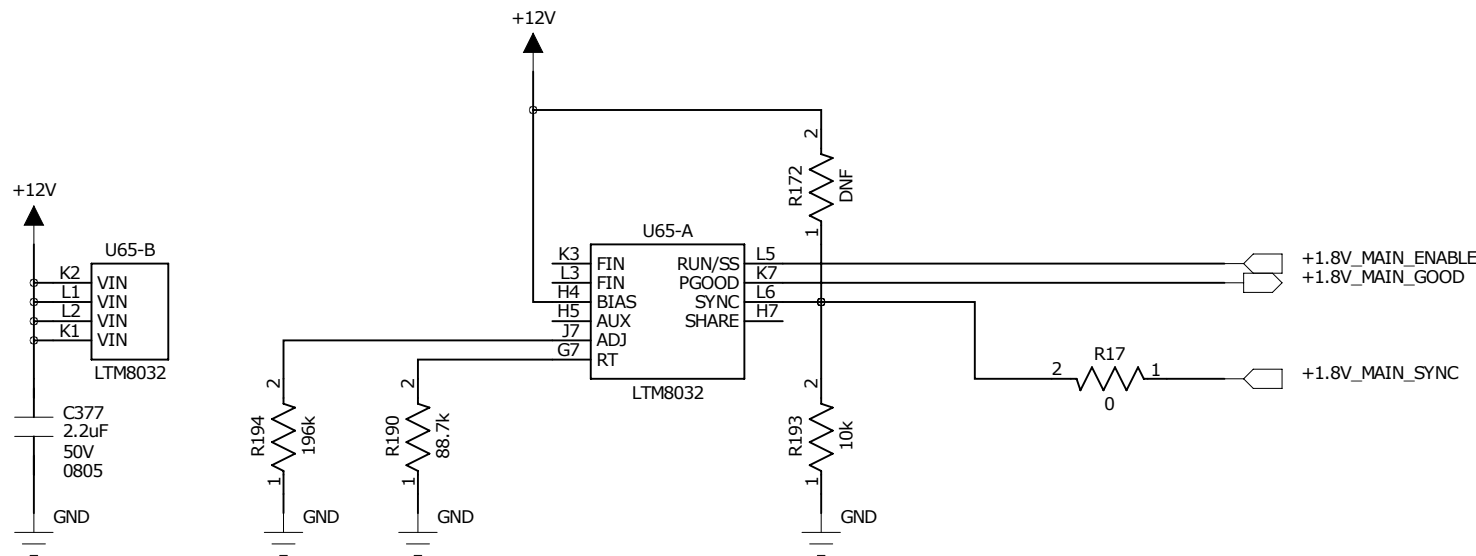
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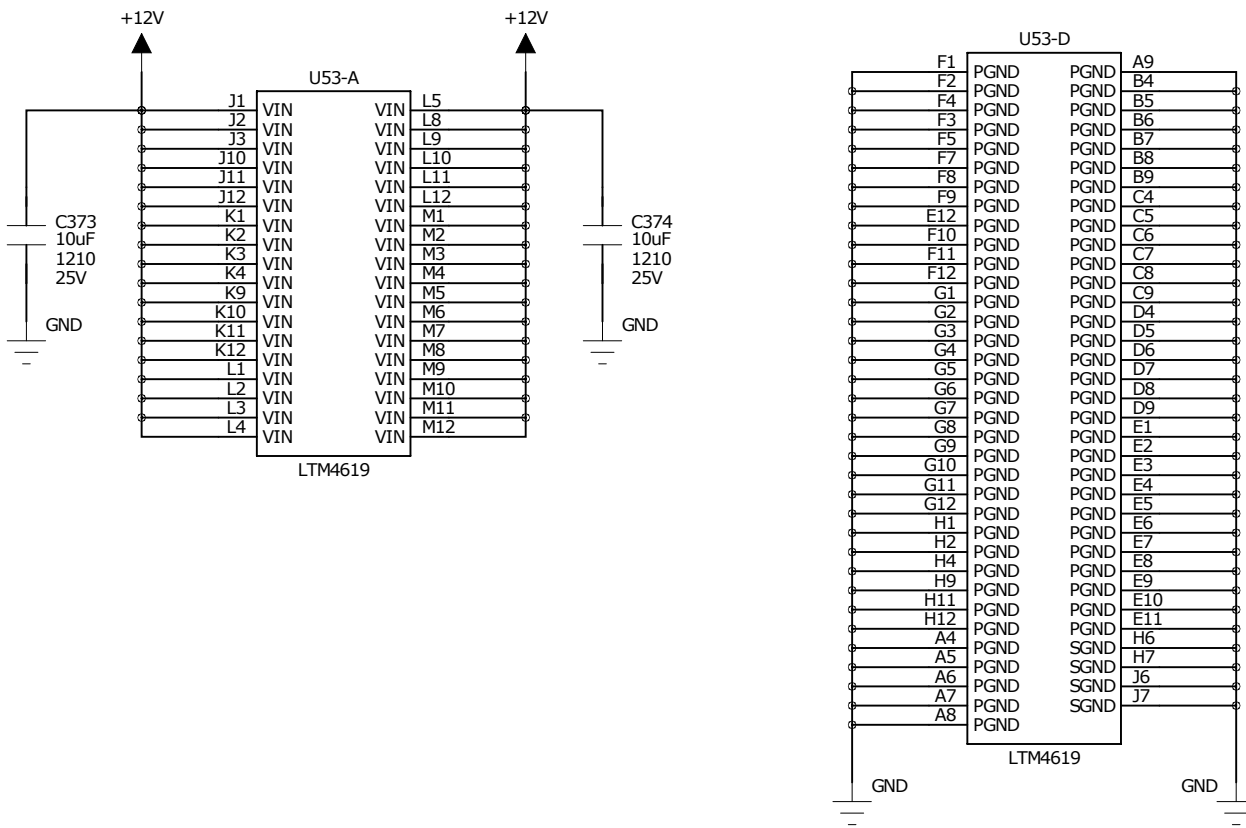
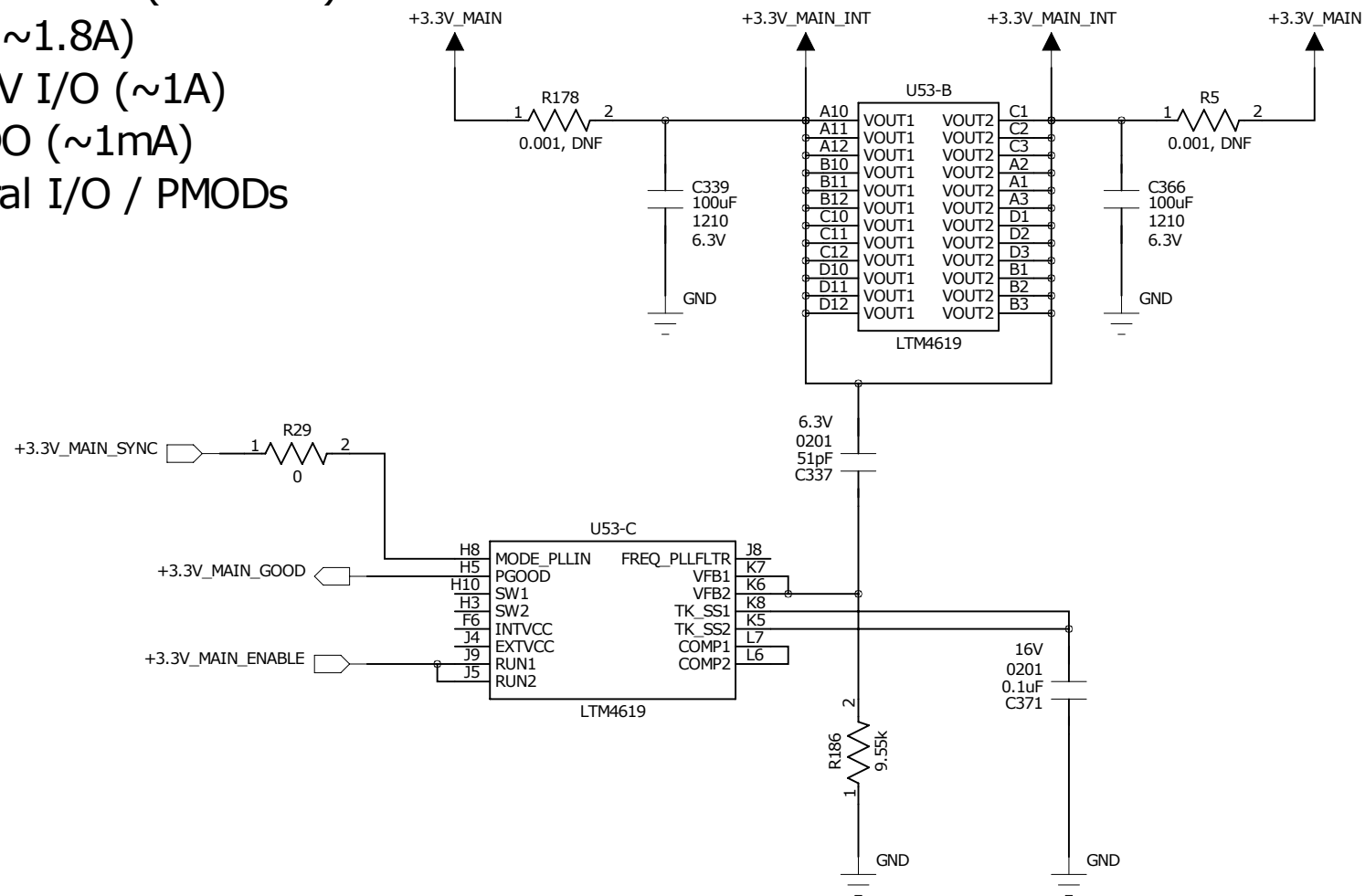
REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

+1.8V powers: K7 VCCAUX (~1A)
K7 +1.8V I/O (~400mA)



+3.3V powers:

Toradex Colibri (~822mA)
QSFP+ (~1.8A)
K7 +3.3V I/O (~1A)
QPLL LDO (~1mA)
Peripheral I/O / PMODs



COMPANY: LBNL-ATG			
TITLE: MAIN_+3.3V_+1.8V_POWER			
CODE: <Code>		SIZE: A2	DRAWING NO: BMB7
			REV: 1
SCALE: <Scale>			SHEET: 17 30

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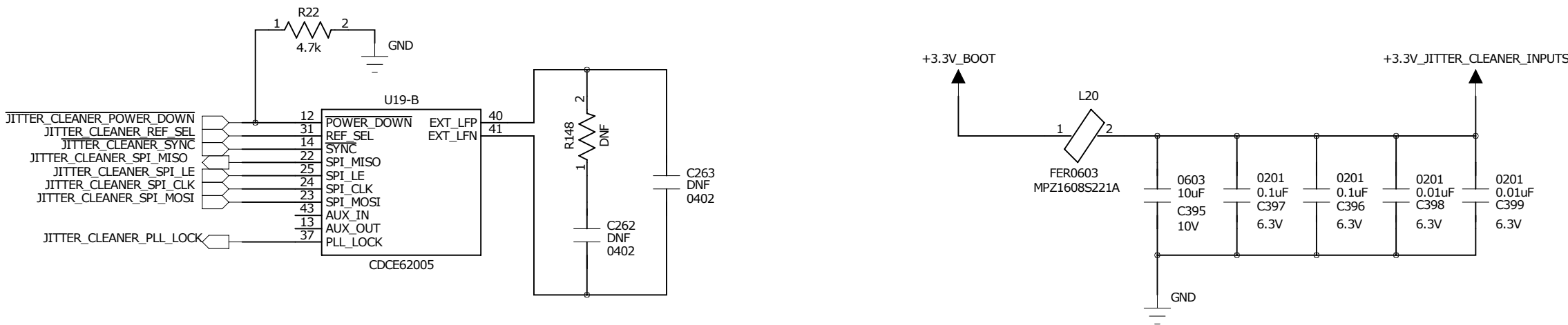
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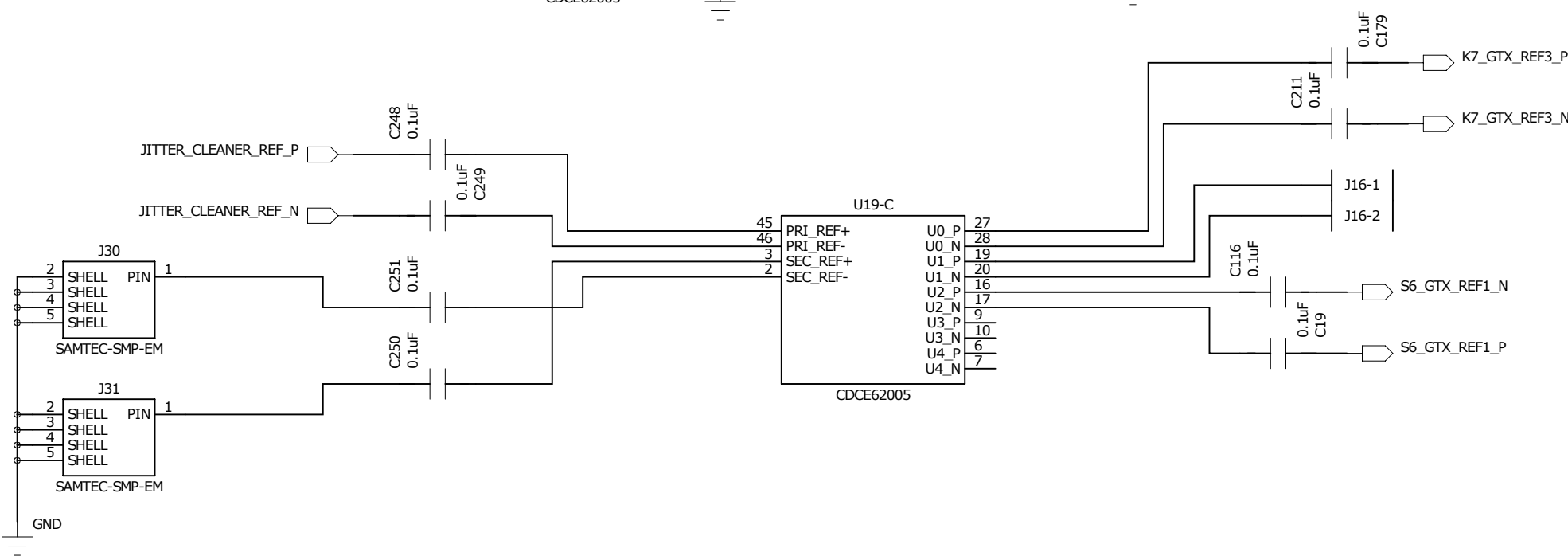
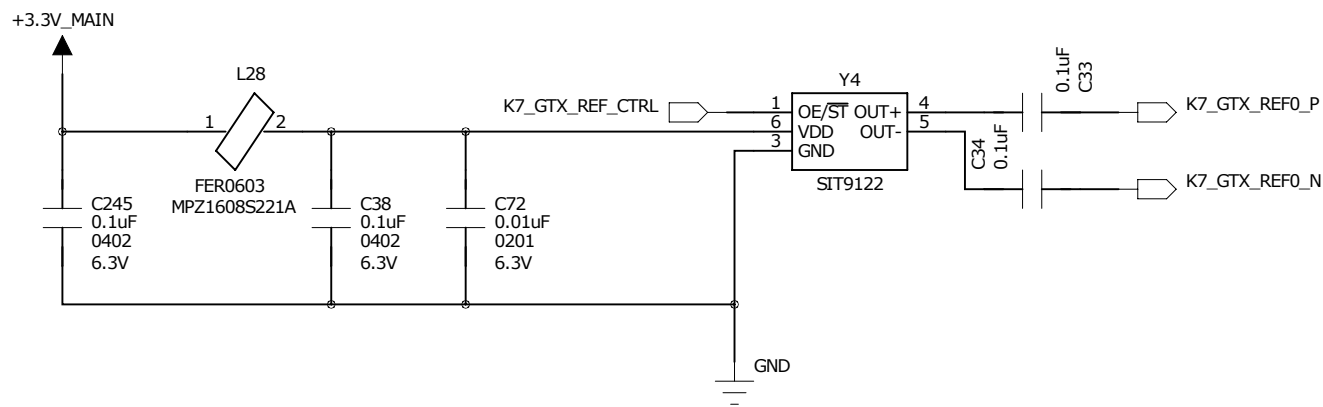
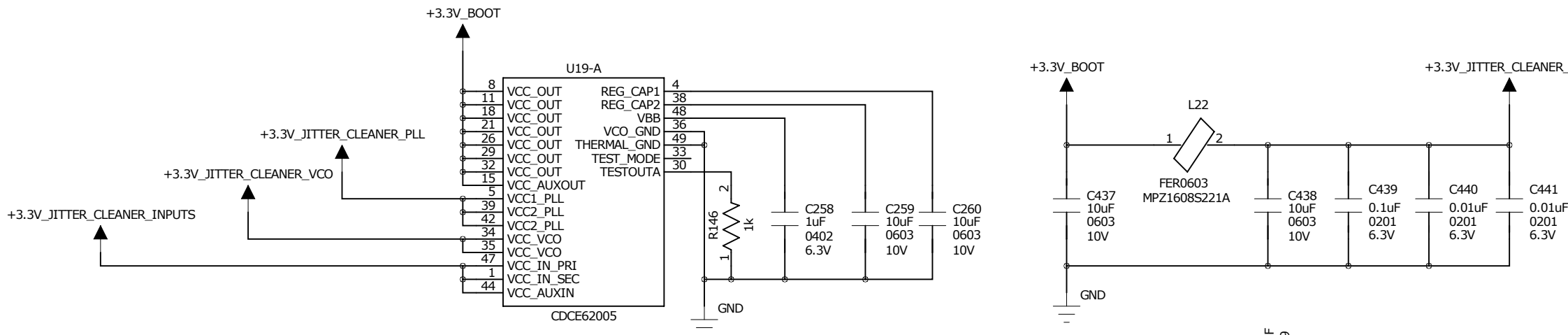
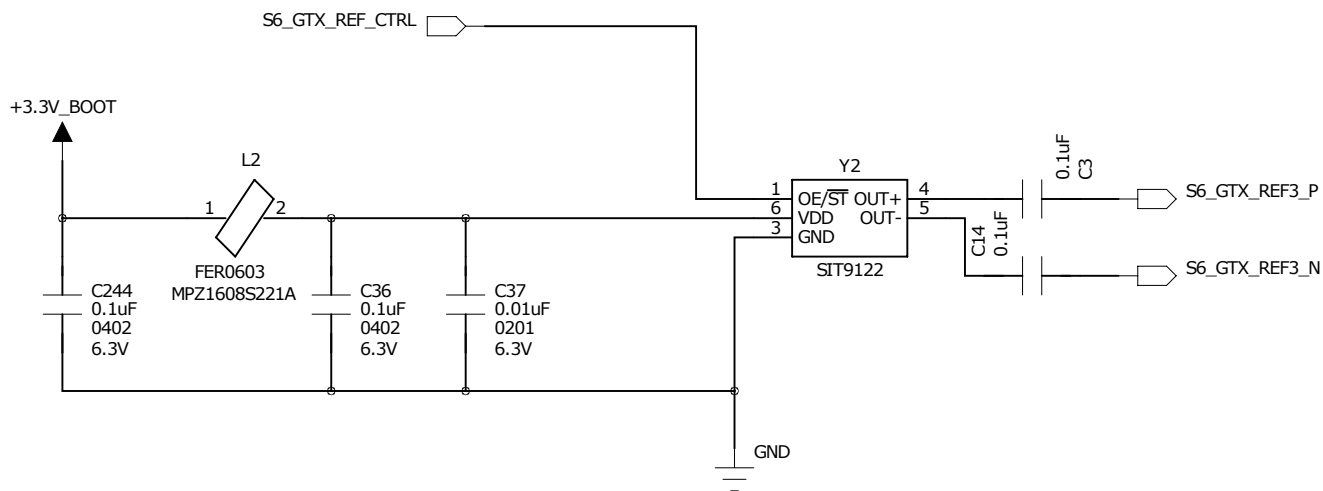
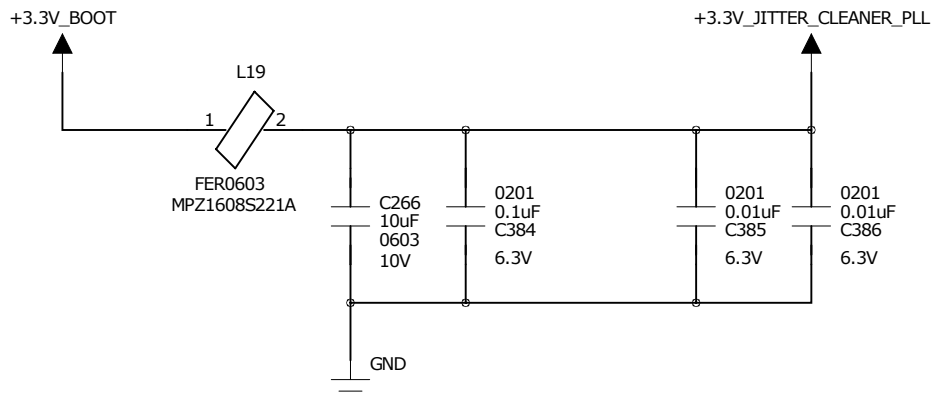
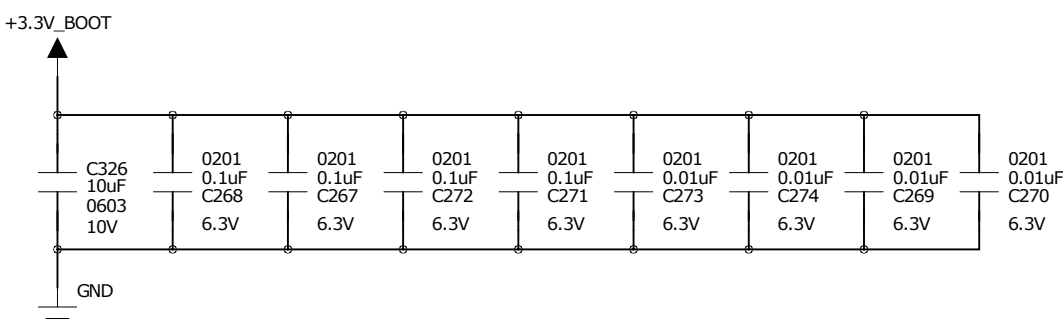
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NOTE: High-performance jitter cleaner
NOTE: Not typically required but can be very useful - can be DNF
NOTE: REFSEL is controlled by SPI

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



NOTE: Precision reference for GTX transceivers
NOTE: Also compatible with SIT3922 DCXO
NOTE: Can be used to phase-lock GTX to recovered clock at fixed frequency



COMPANY: LBNL-ATG			
TITLE: CLOCKS_A			
DRAWN: John Jones	DATED: 25.2.13	CODE: <Code>	SIZE: A2
CHECKED: <Checked By>	DATED: <Checked Date>	DRAWING NO: BMB7	REV: 1
QUALITY CONTROL: <QC By>	DATED: <QC Date>	SCALE: <Scale>	SHEET: 18 30
RELEASED: <Released By>	DATED: <Release Date>		

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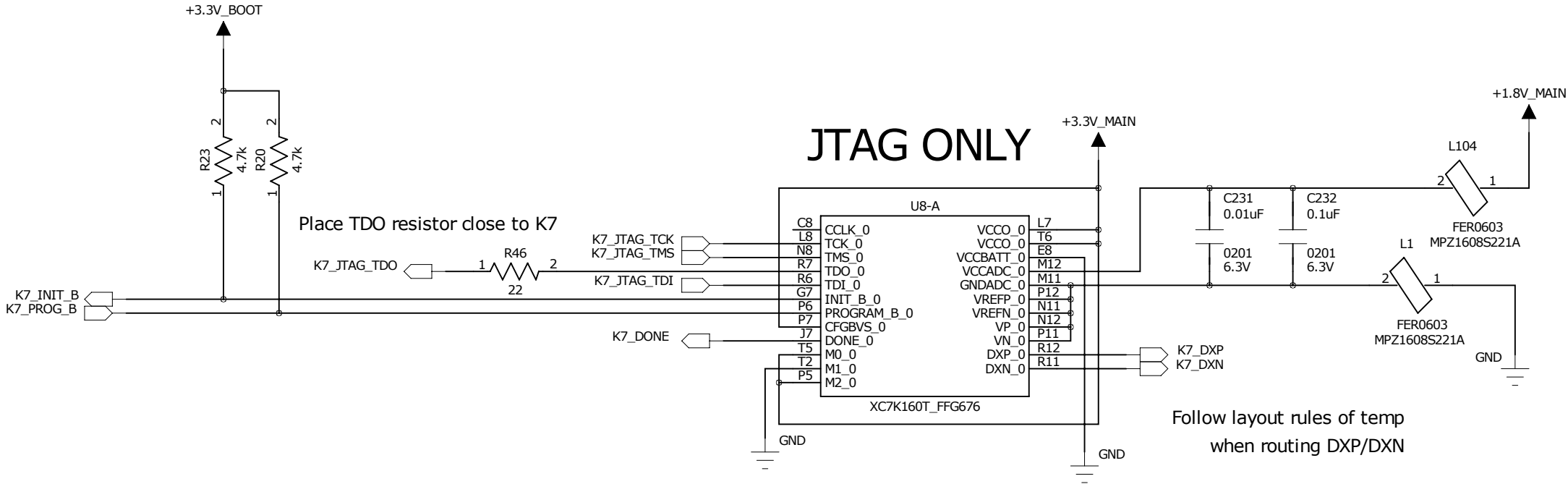
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REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

NOTE: +3.3V operation
NOTE: As we are only using JTAG for configuration this places no requirements on any other bank
NOTE: Done has an internal 10k pullup - no external required



COMPANY: LBNL-ATG			
TITLE: K7_CONFIG			
CODE:	SIZE: A2	DRAWING NO: BMB7	REV: 1
SCALE: <Scale>		SHEET: 22 30	

DRAWN: John Jones	DATED: 25.2.13
CHECKED: <Checked By>	DATED: <Checked Date>
QUALITY CONTROL: <QC By>	DATED: <QC Date>
RELEASED: <Released By>	DATED: <Release Date>

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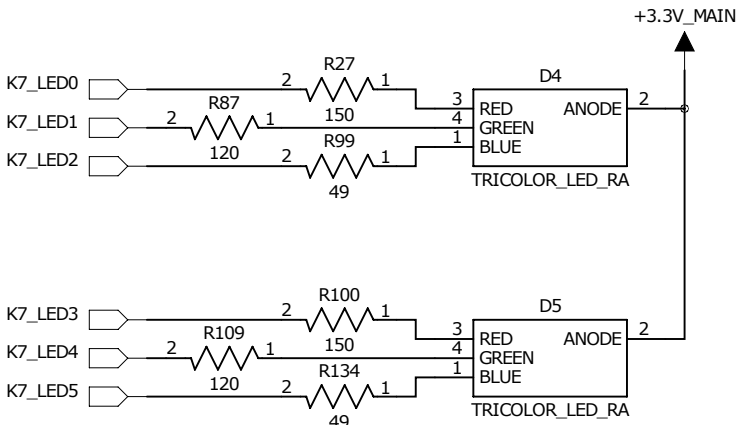
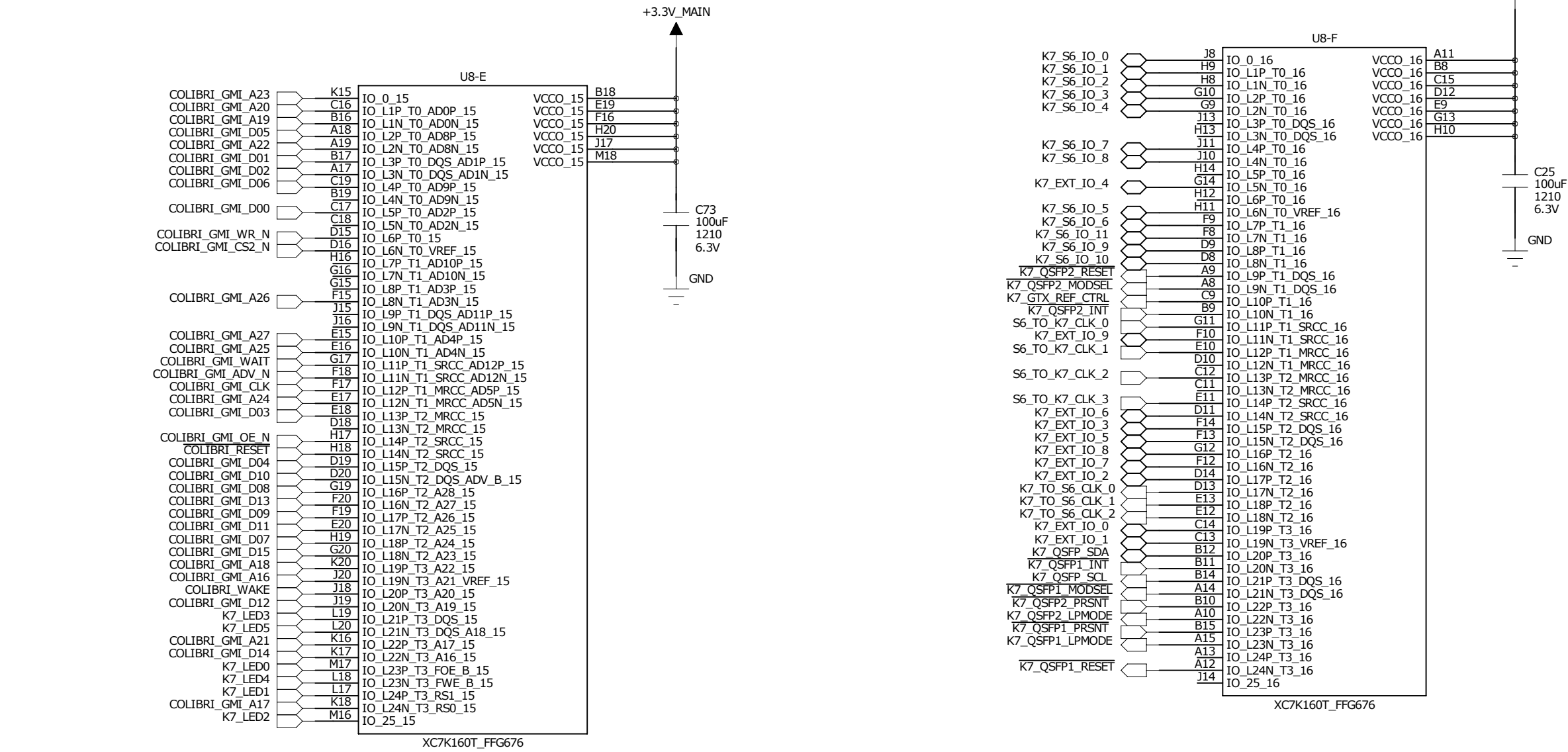
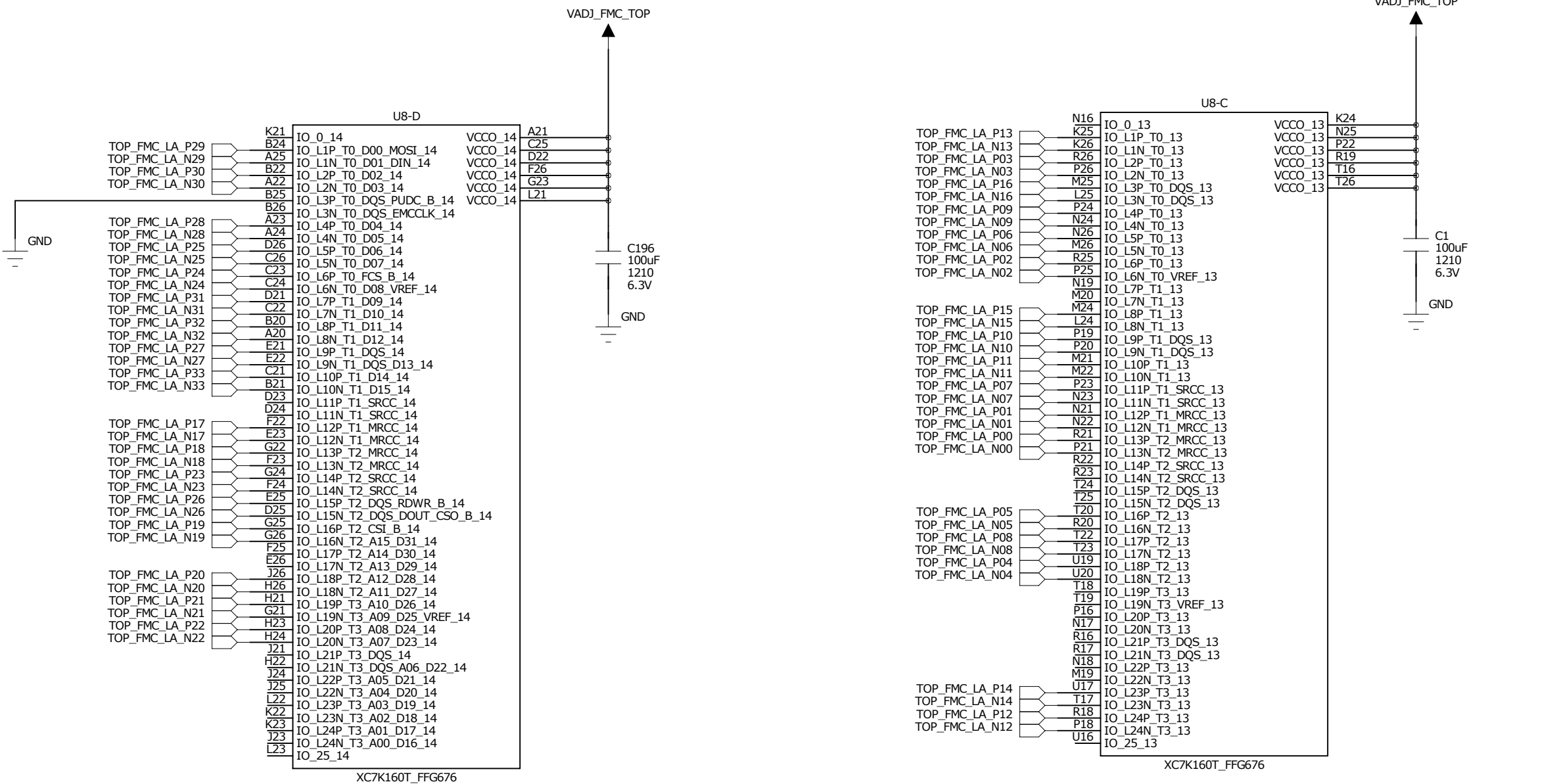
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NOTE: Set up to use internal VREF

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

NOTE: The K7 - S6 I/O are designed for single-ended use
NOTE: Differential bus would cause breakout problems in S6
NOTE: Pullups on I2C are internal - 10k - 35k



COMPANY:		LBNL-ATG			
TITLE:		K7_IO_A			
DRAWN:	DATED:	CODE:	SIZE:	DRAWING NO:	REV:
John Jones	25.2.13	<Code>	A2	BMB7	1
CHECKED:	DATED:	SCALE: <Scale>		SHEET: 23 30	
<Checked By>	<Checked Date>				
QUALITY CONTROL:	DATED:				
<QC By>	<QC Date>				
RELEASED:	DATED:				
<Released By>	<Release Date>				

6

5

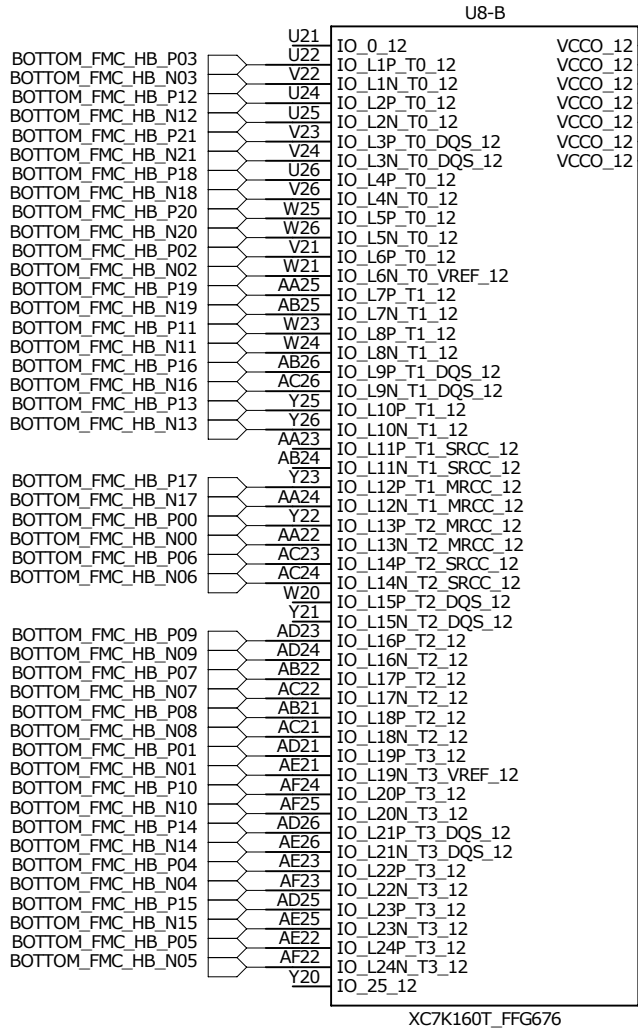
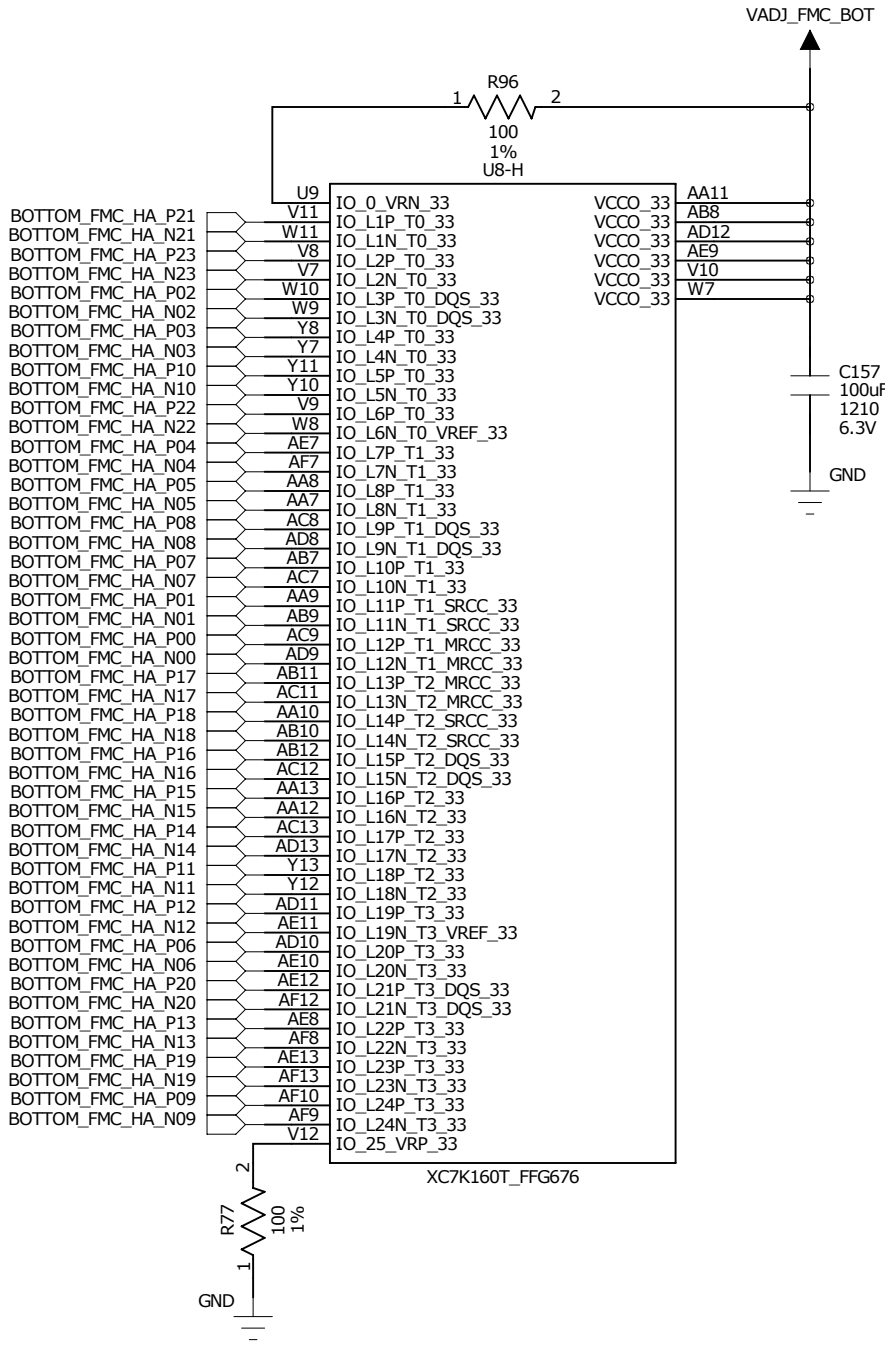
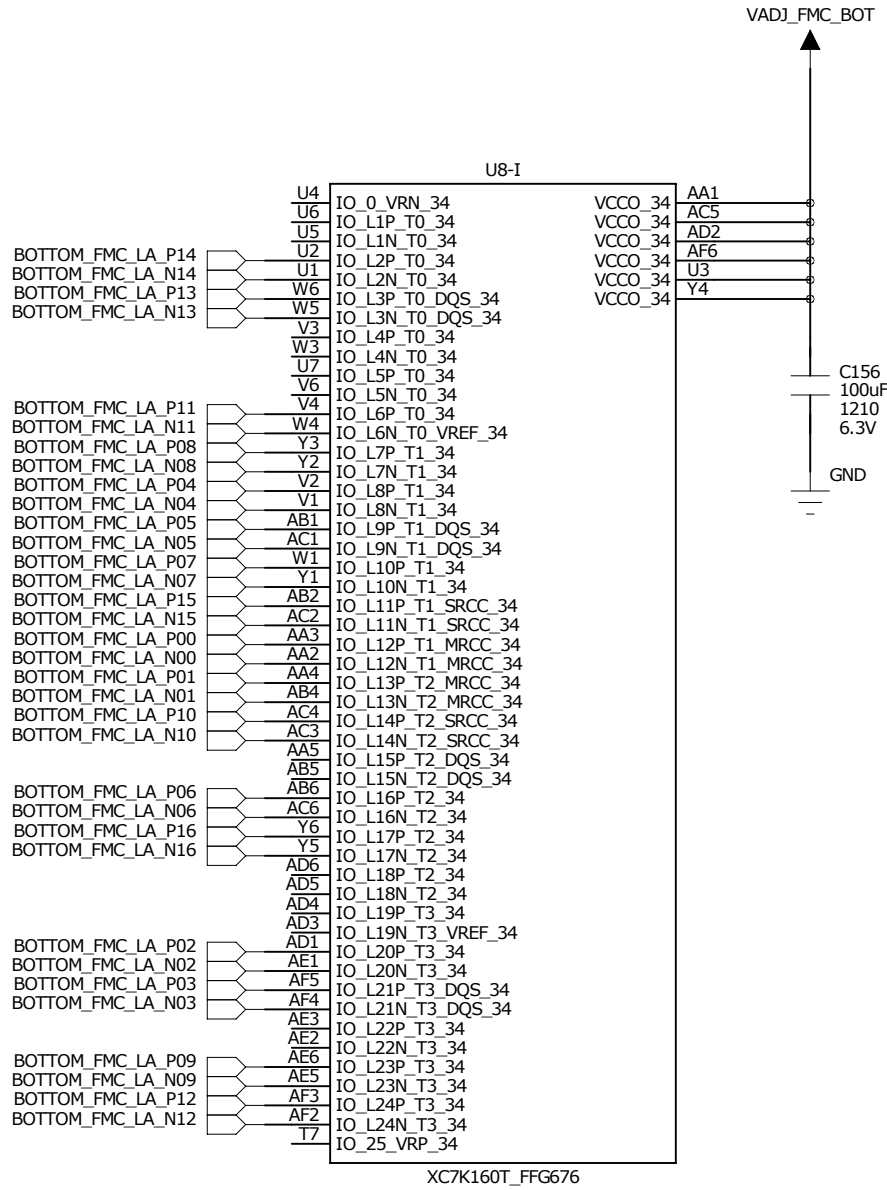
4

3

2

1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:



NOTE: Set up to use DCI cascading
NOTE: Set up to use internal VREF

TODO: Double-check decoupling cap part

DRAWN:	John Jones	DATED:	25.2.13
CHECKED:	<Checked By>	DATED:	<Checked Date>
QUALITY CONTROL:	<QC By>	DATED:	<QC Date>
RELEASED:	<Released By>	DATED:	<Release Date>

COMPANY:		LBNL-ATG		
TITLE:				
K7_IO_B				
>	CODE:	SIZE:	DRAWING NO:	REV:
<Code>	A2	BMB7		1
SCALE: <Scale>			SHEET: 24	30

6

5

4

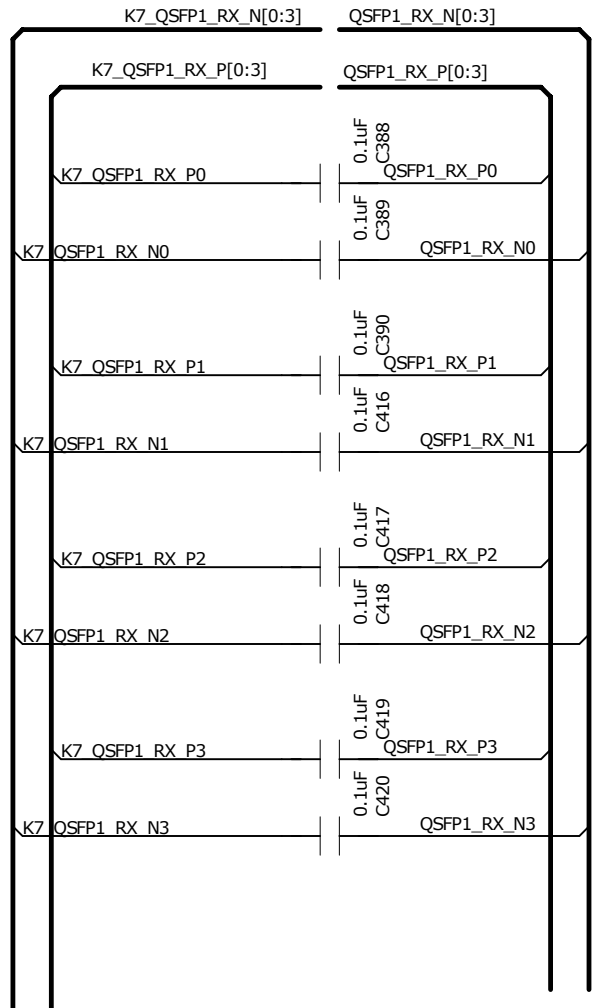
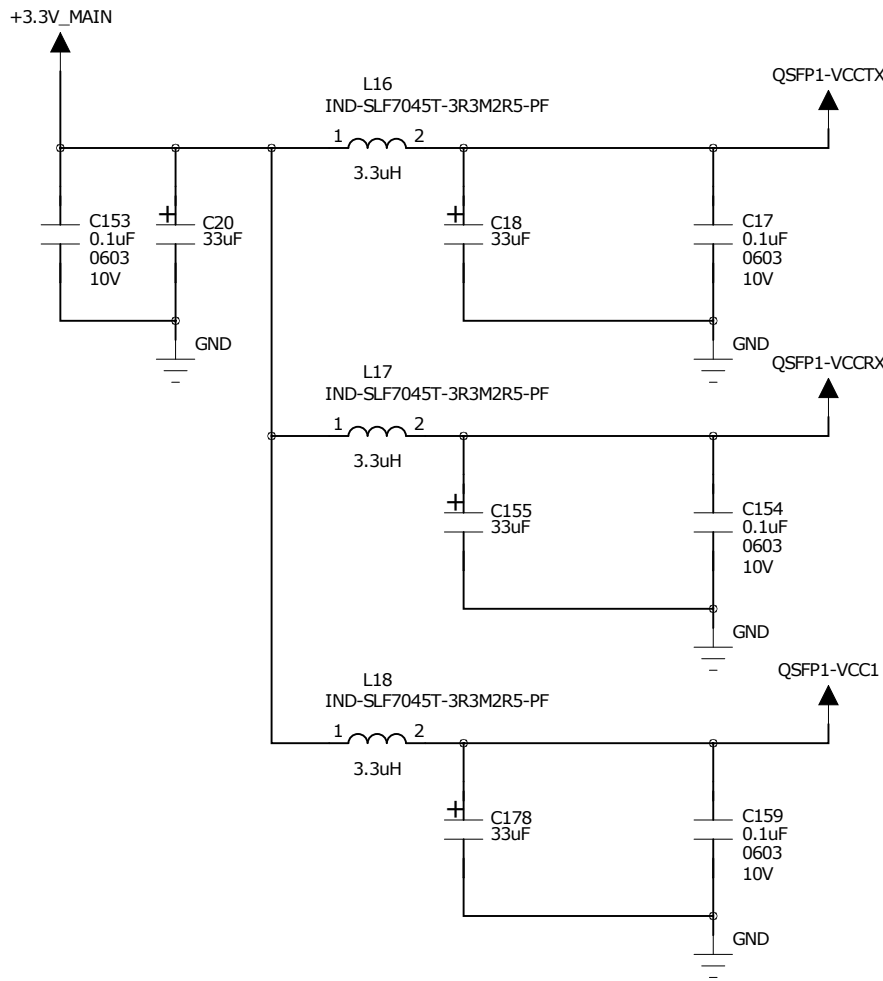
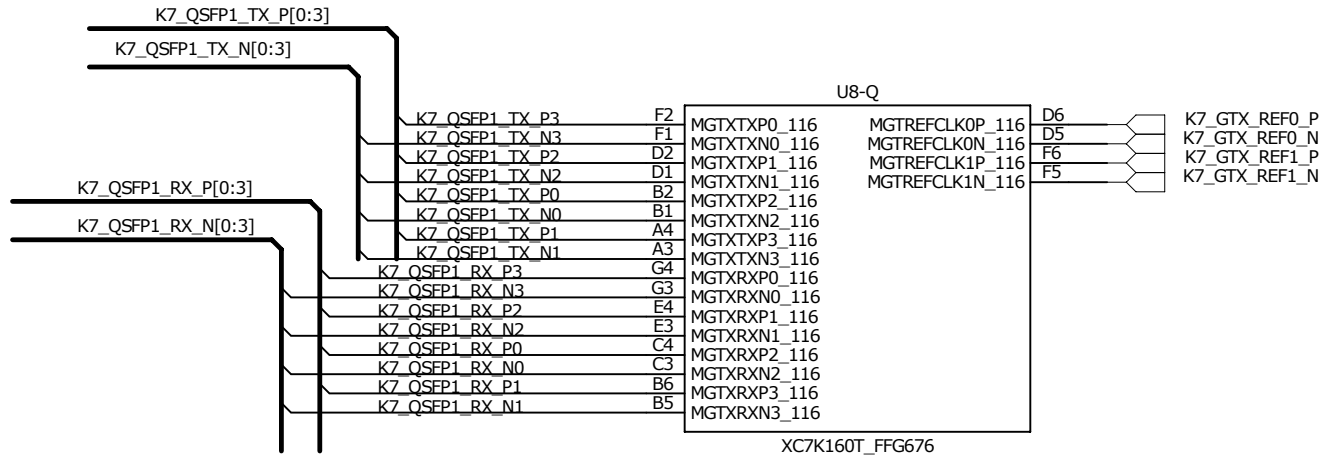
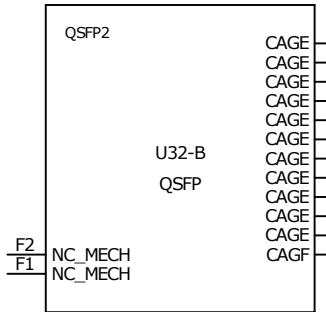
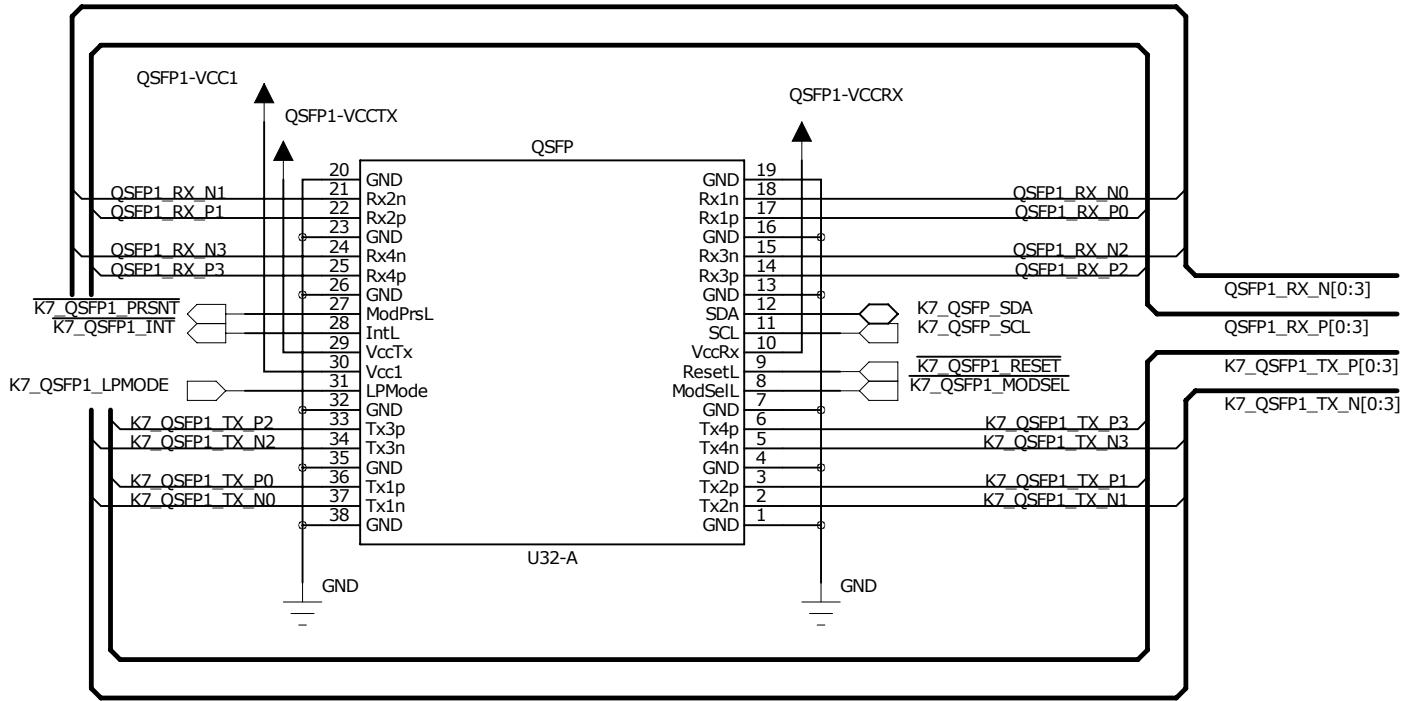
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2

1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

QSFP1



D

D

C

C

B

B

A

A

DRAWN:	John Jones	DATED:	25.2.13
CHECKED:	<Checked By>	DATED:	<Checked Date>
QUALITY CONTROL:	<QC By>	DATED:	<QC Date>
RELEASED:	<Released By>	DATED:	<Release Date>

COMPANY:		LBNL-ATG		
TITLE:		K7_QSFP_1		
>	CODE:	SIZE:	DRAWING NO:	REV:
<Code>	A2	BMB7		1
SCALE: <Scale>			SHEET: 25	30

6

5

4

3

2

1

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

D

D

C

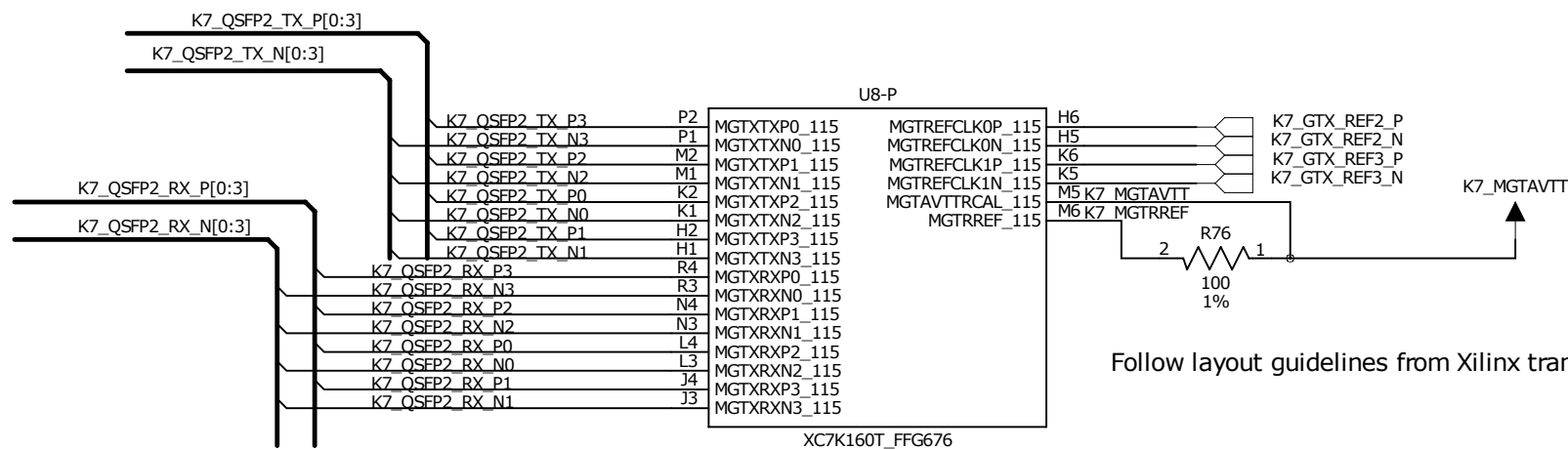
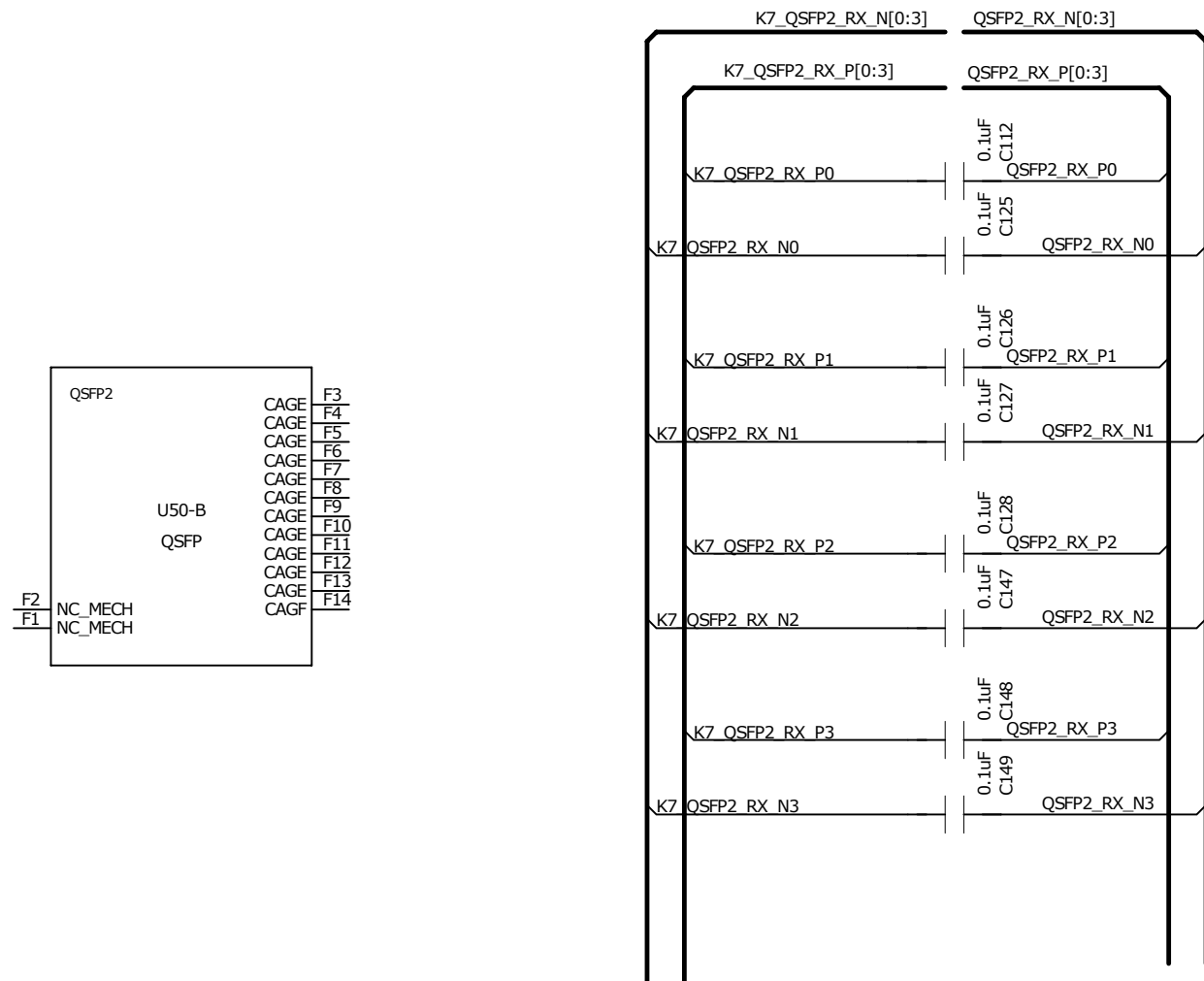
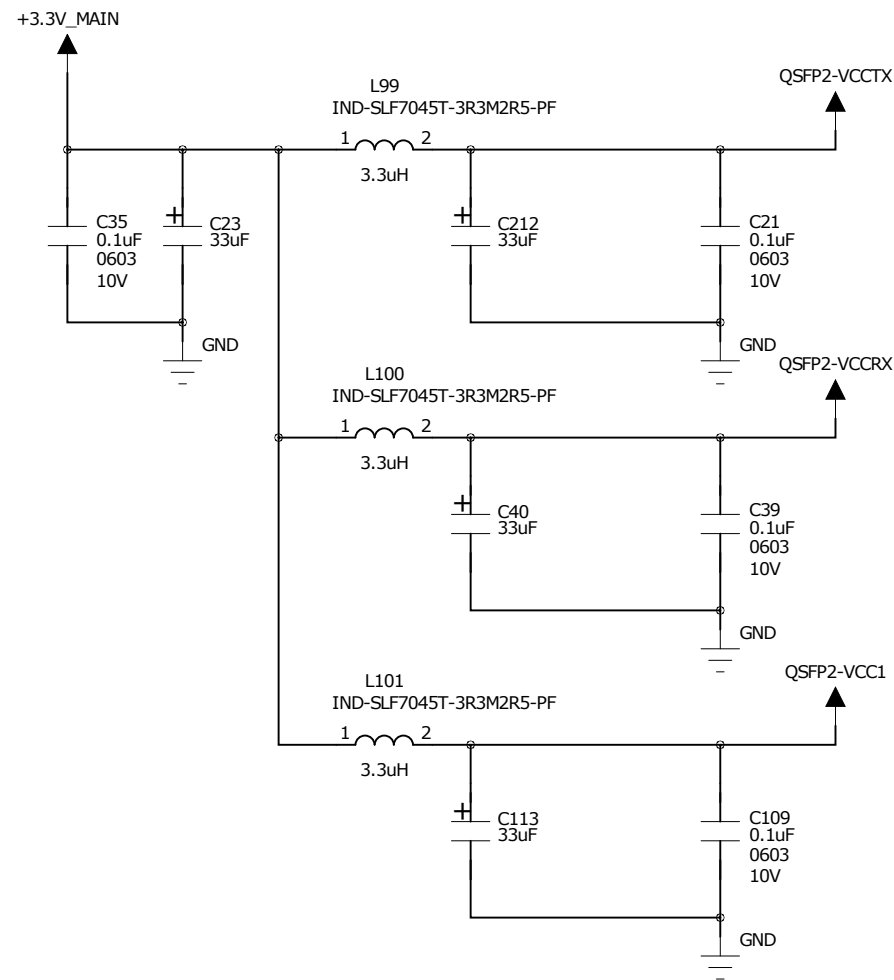
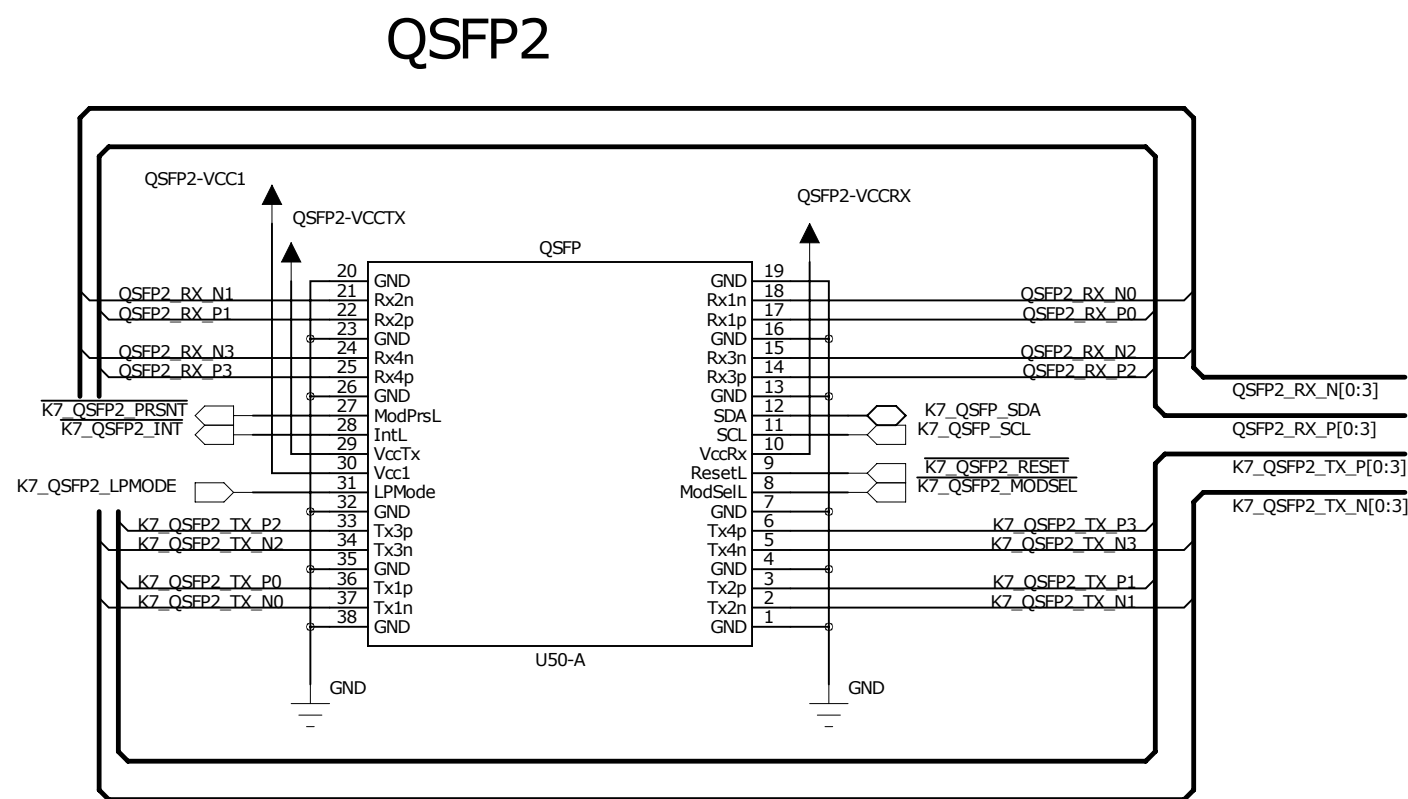
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B

B

A

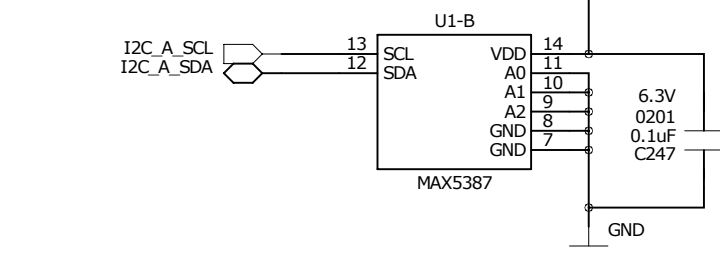
A



Follow layout guidelines from Xilinx transceiver datasheet, page 215 (UG476)

COMPANY: LBNL-ATG			
TITLE: K7_QSFP_2			
DRAWN: John Jones	DATED: 25.2.13	CODE:	SIZE: A2
CHECKED: <Checked By>	DATED: <Checked Date>	DRAWING NO: BMB7	REV: 1
QUALITY CONTROL: <QC By>	DATED: <QC Date>	SCALE: <Scale>	SHEET: 26 30
RELEASED: <Released By>	DATED: <Release Date>		

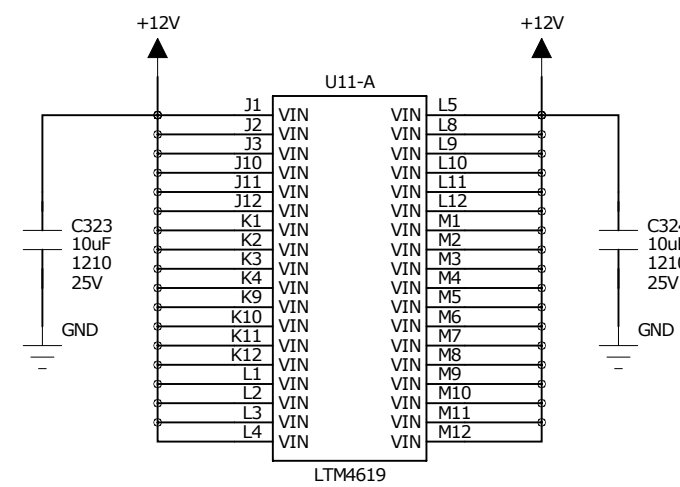
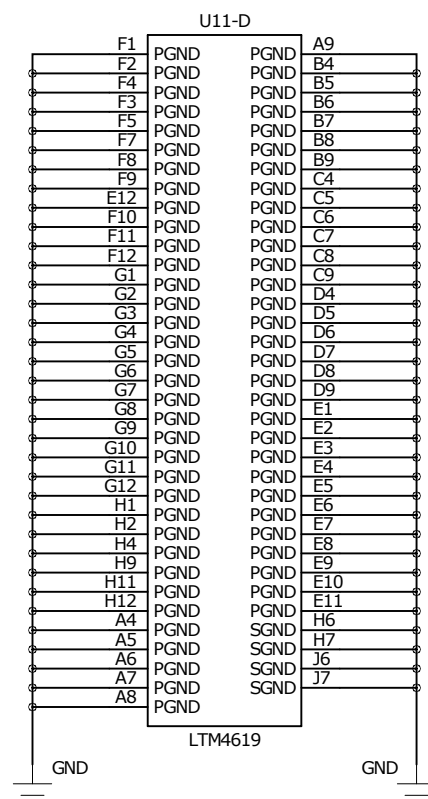
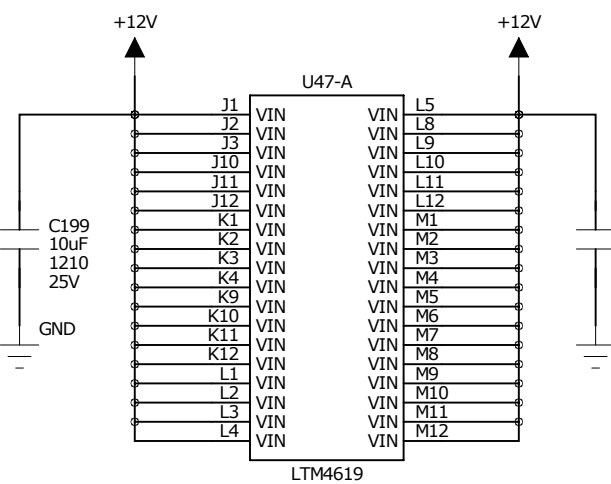
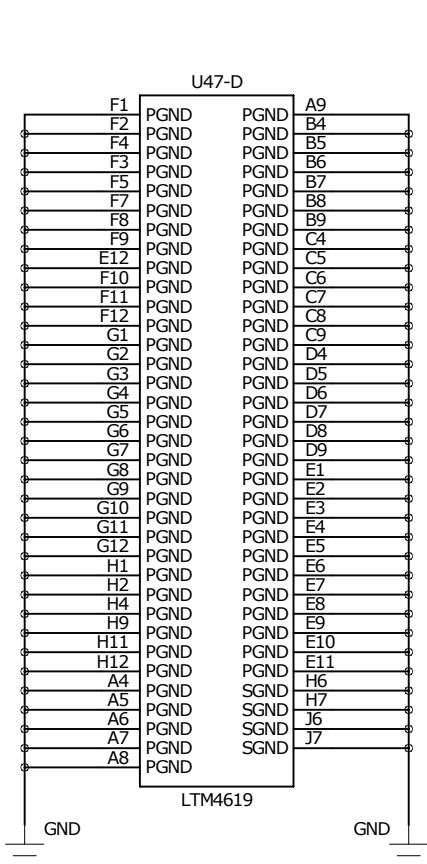
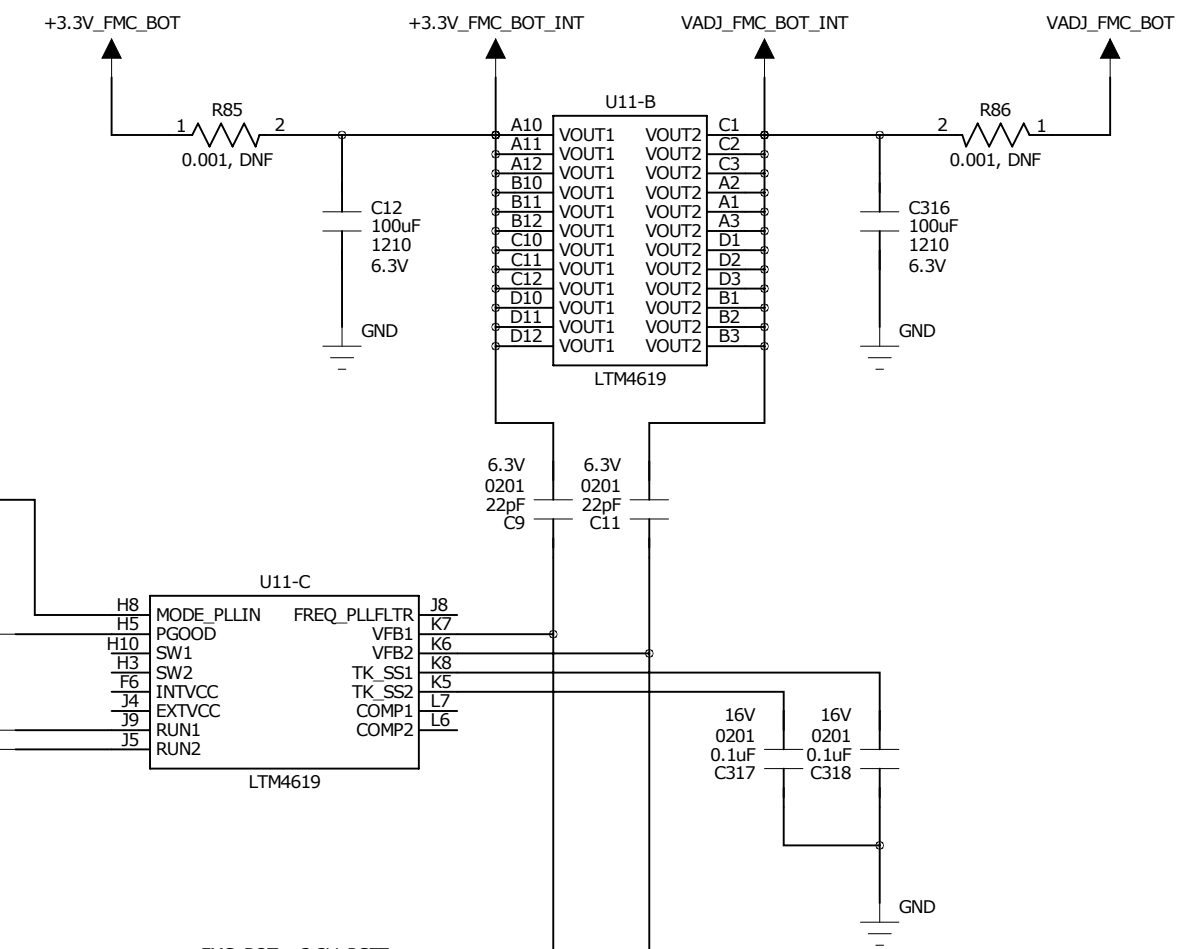
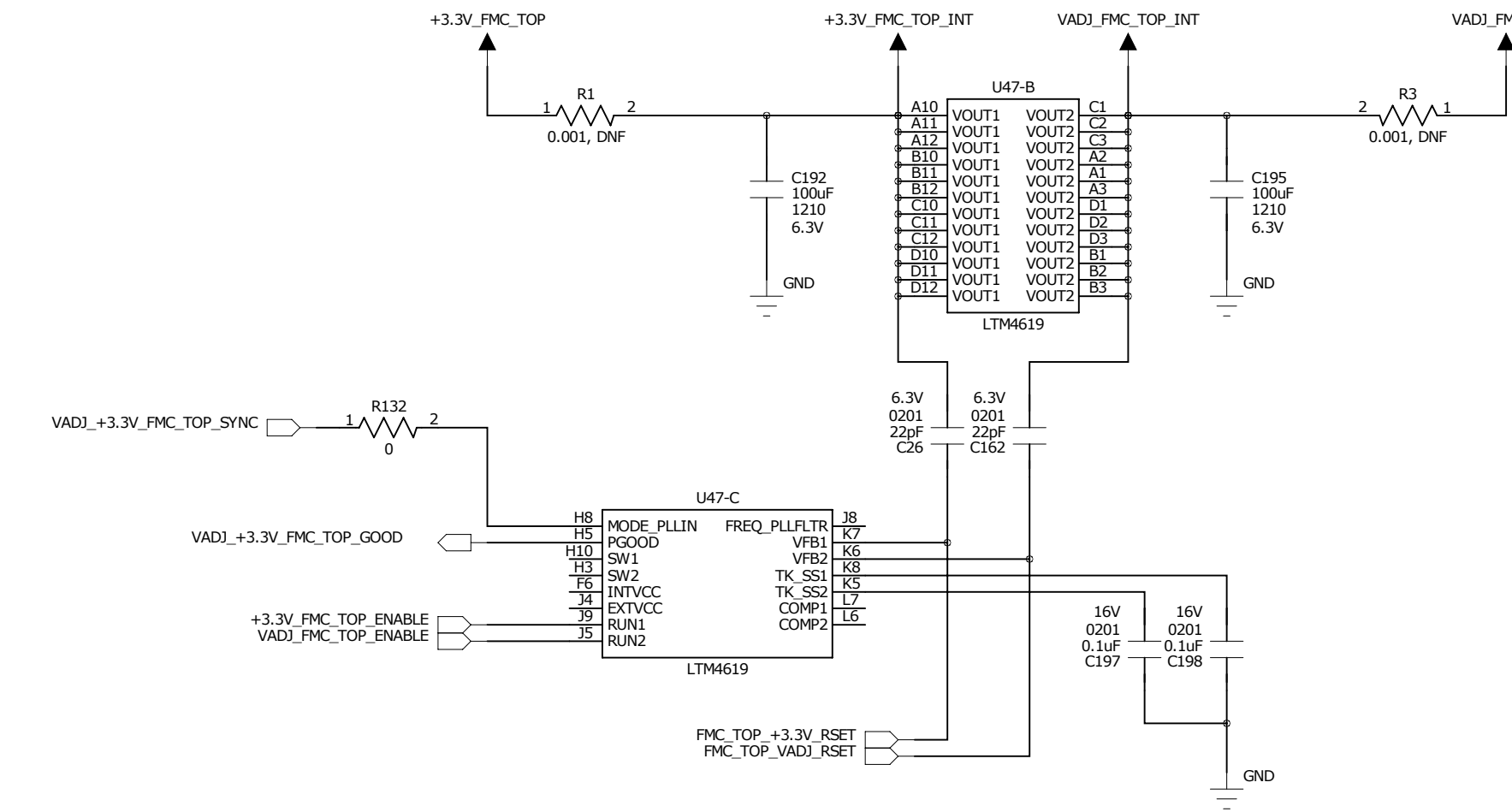
VADJ : 4A
+3.3V : 3A



I2C address: 0b0101000

19.1k caps VADJ at +3.3V
48.7k caps VADJ at +1.8V

I2C address: 0b0101001

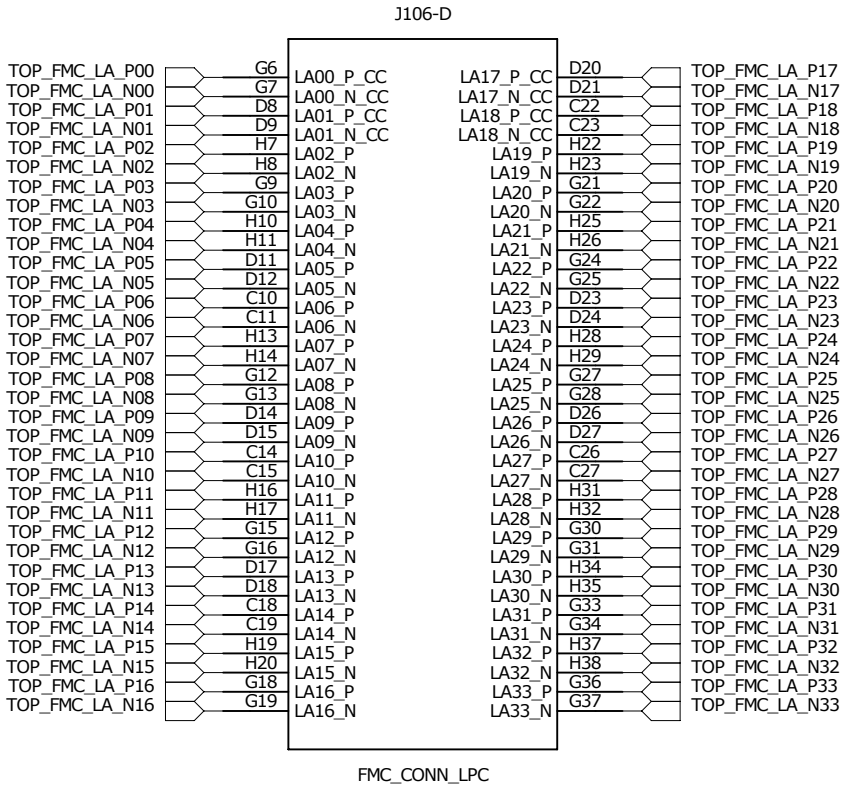
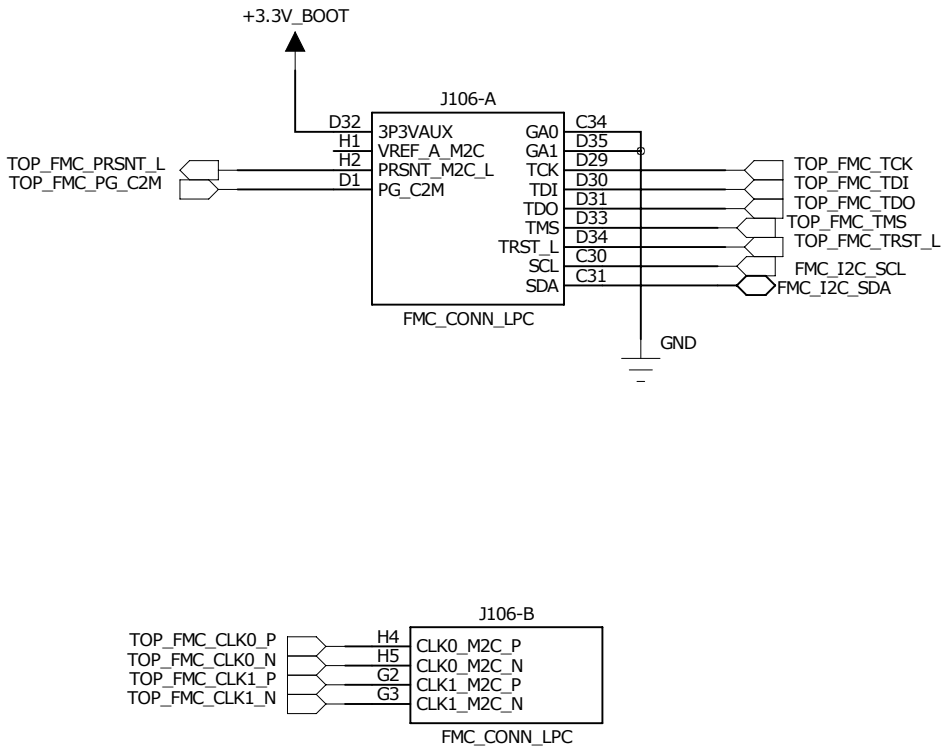


REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

COMPANY: LBNL-ATG			
TITLE: FMC_POWER_B			
DRAWN: John Jones	DATED: 25.2.13	CODE:	SIZE: A2
CHECKED: <Checked By>	DATED: <Checked Date>	CODE:	SIZE: A2
QUALITY CONTROL: <QC By>	DATED: <QC Date>	CODE:	SIZE: A2
RELEASED: <Released By>	DATED: <Release Date>	CODE:	SIZE: A2
DRAWING NO: BMB7		REV: 1	
SCALE: <Scale>		SHEET: 28 30	

REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

I2C addresss space: 0bXXXXX00X
EEPROM address: 0b1010000X



COMPANY: LBNL-ATG			
TITLE: FMC_TOP			
DRAWN: John Jones	DATED: 25.2.13	CODE:	SIZE: A2
CHECKED: <Checked By>	DATED: <Checked Date>	DRAWING NO: BMB7	REV: 1
QUALITY CONTROL: <QC By>	DATED: <QC Date>	SCALE: <Scale>	SHEET: 29 30
RELEASED: <Released By>	DATED: <Release Date>		

6

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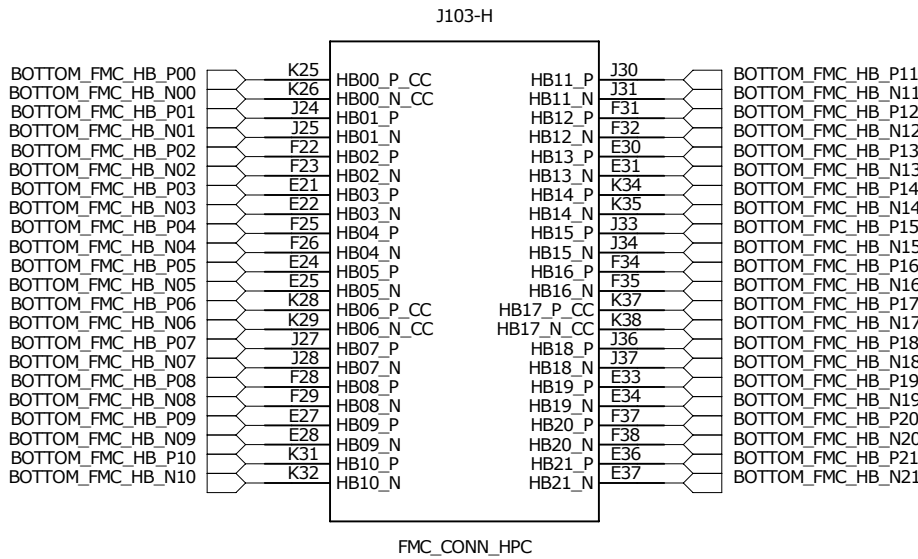
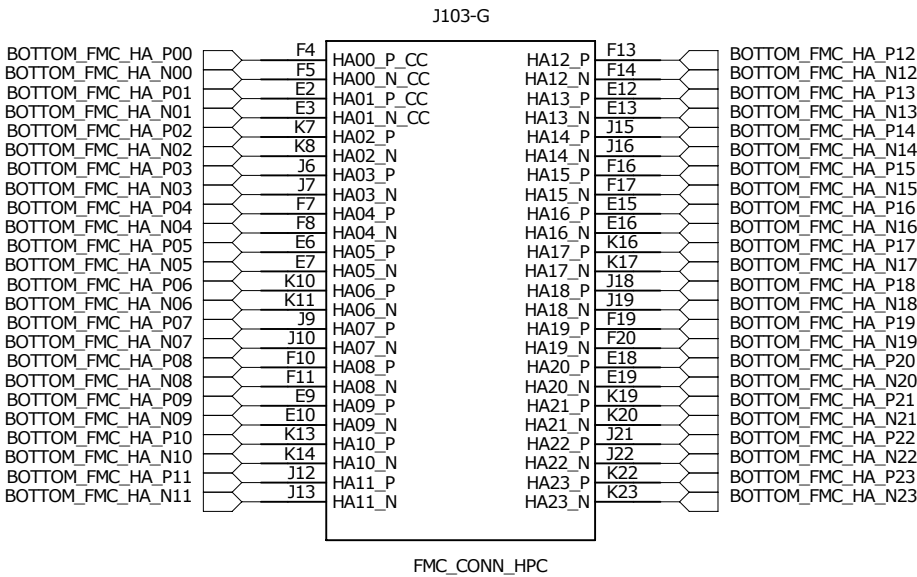
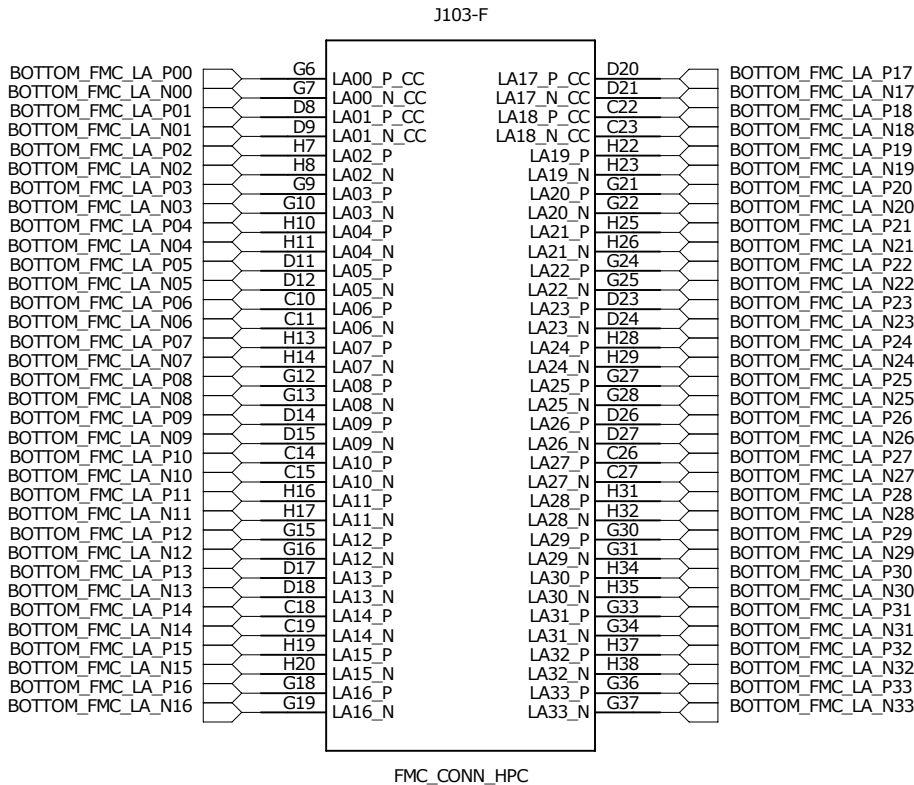
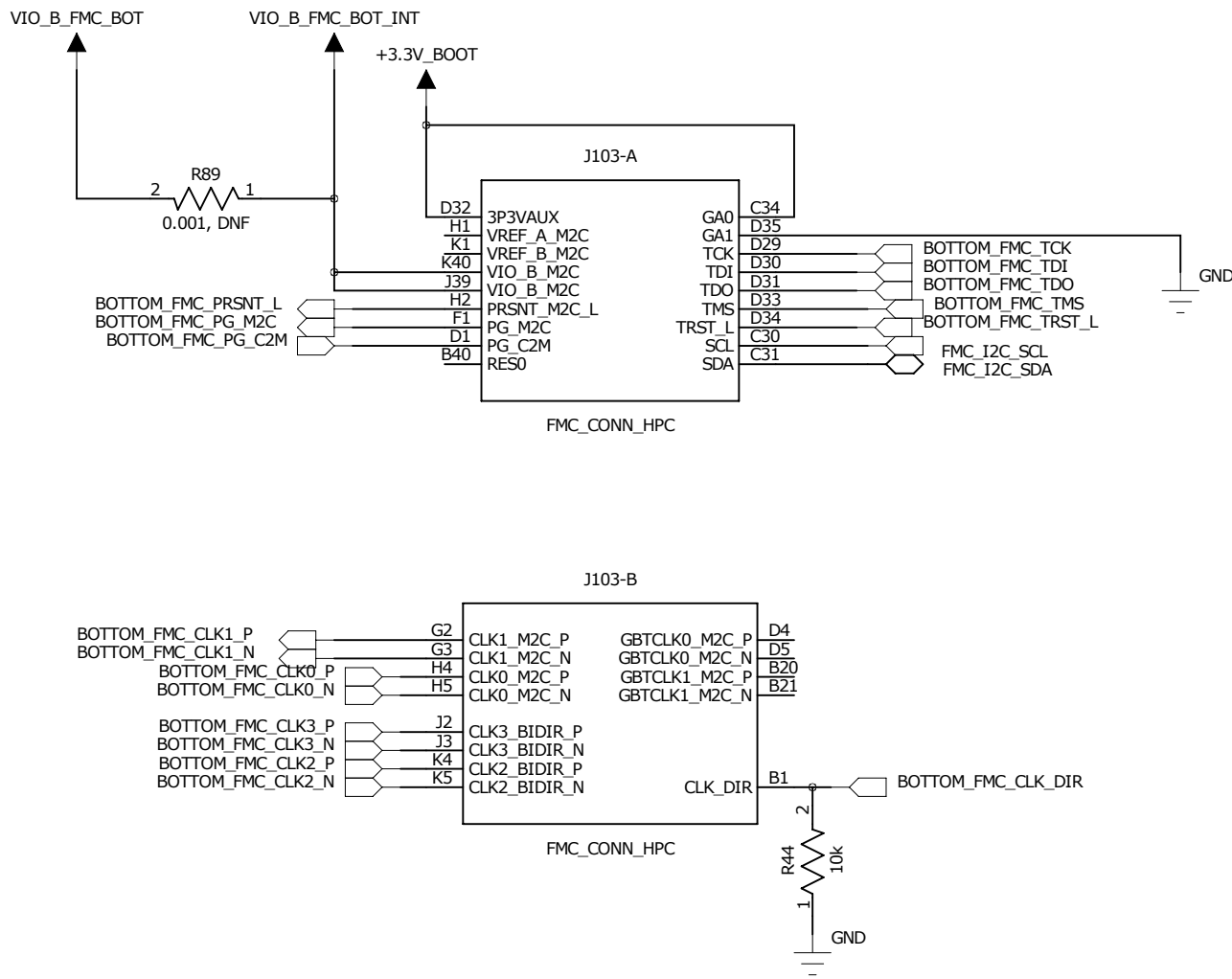
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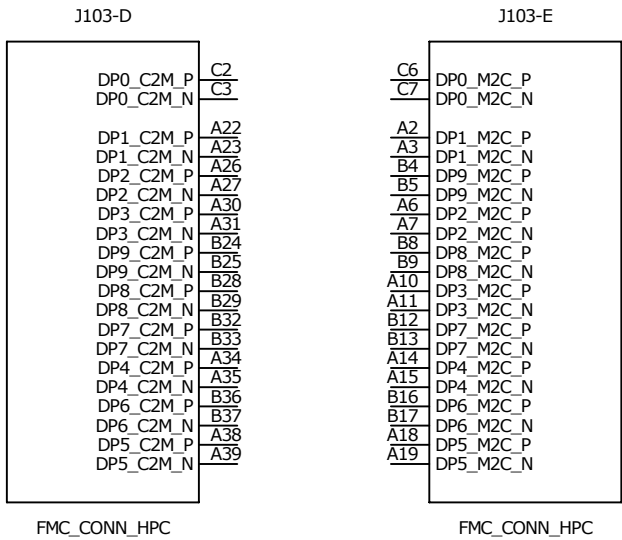
2

1

I2C addresss space: 0bXXXXX01X
EEPROM address: 0b1010001X



UNUSED CONNECTIONS



REVISION RECORD			
LTR	ECO NO:	APPROVED:	DATE:

COMPANY: LBNL-ATG				
TITLE: FMC_BOTTOM				
>	CODE:	SIZE:	DRAWING NO:	REV:
<Code>	A2	BMB7		1
SCALE: <Scale>			SHEET: 30	30