

FMC2\_PG\_C2M ■ FMC2\_PG\_C2M FMC2\_VREF\_A\_M2C
FMC2\_PRSNT\_M2C\_L

GFMC2\_PRSNT\_M2C\_L

GFMC2\_PRSNT\_M2C\_L

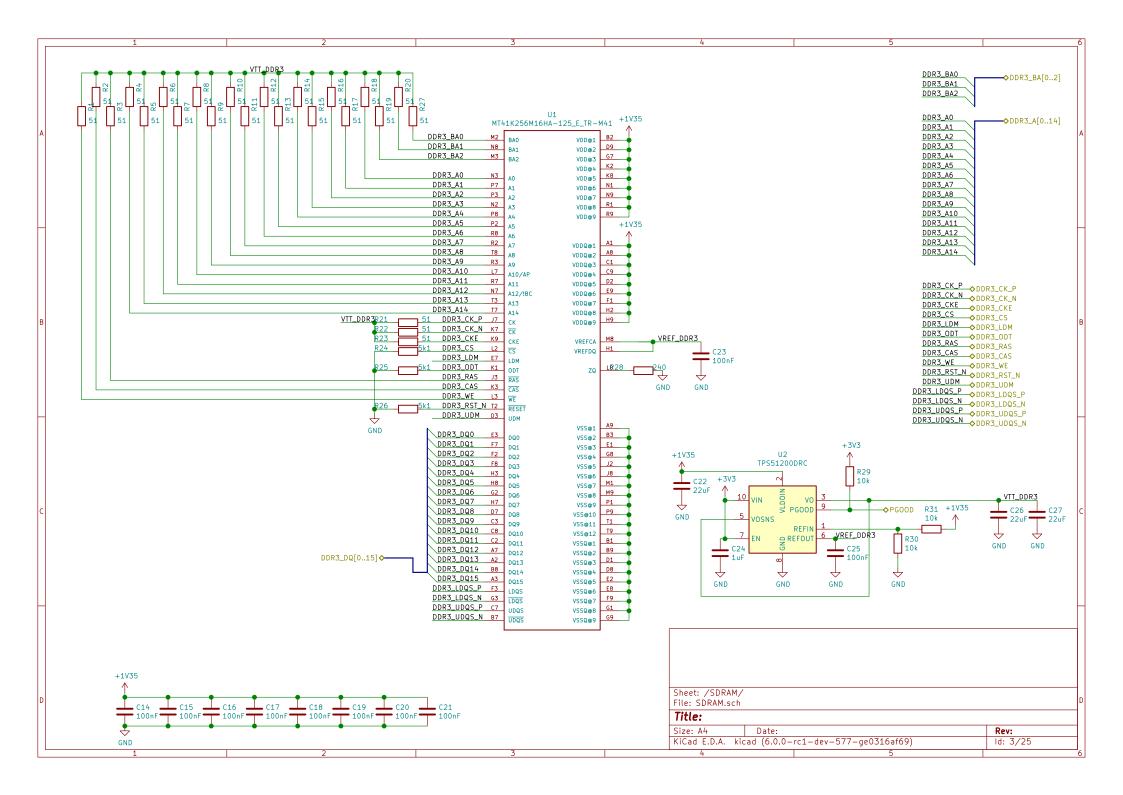
─**d**I2C\_SDA\_FMC2

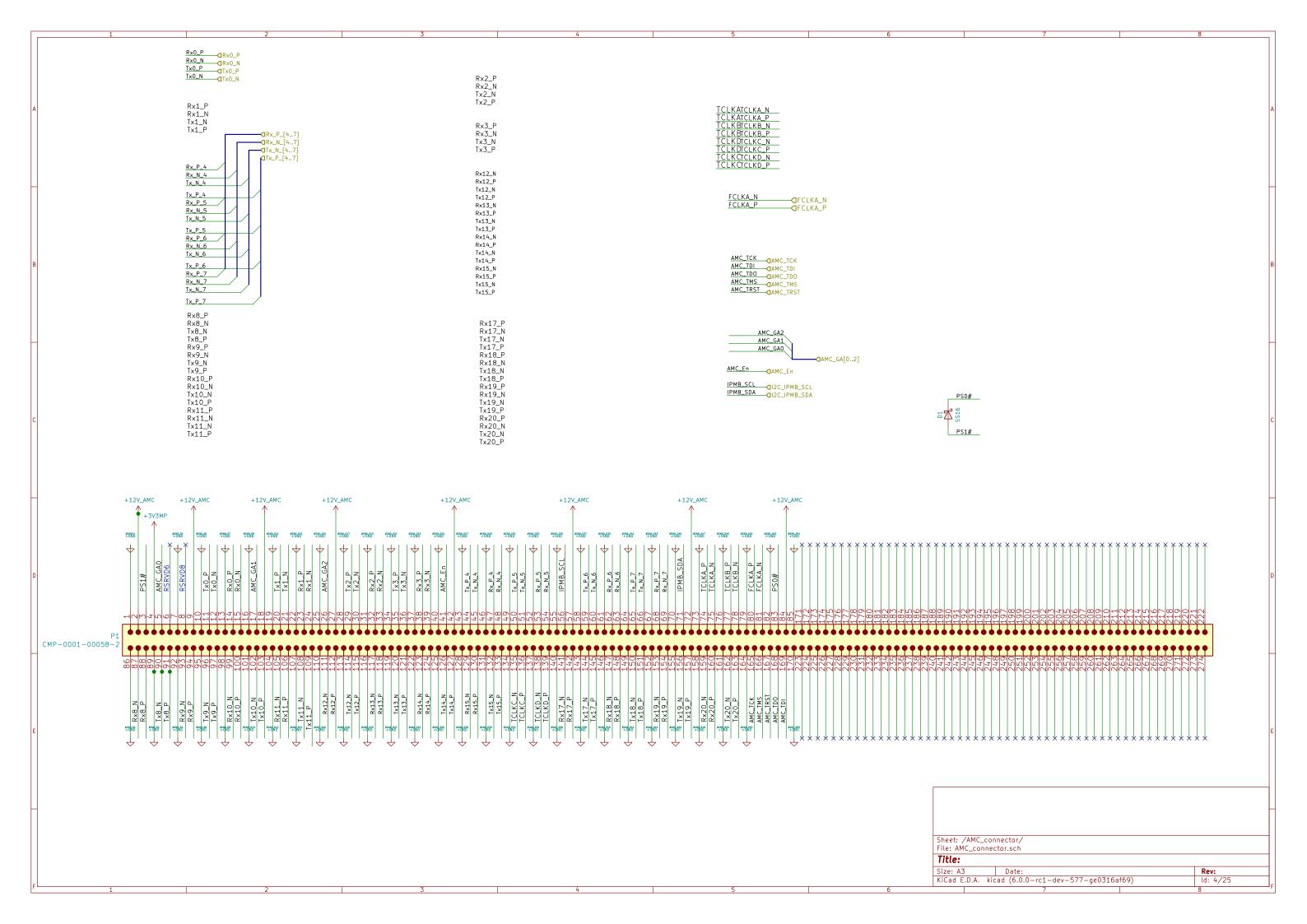
**⊸**FMC2\_TCK ■ FMC2\_TDI
■ FMC2\_TDO -dFMC2\_TRST

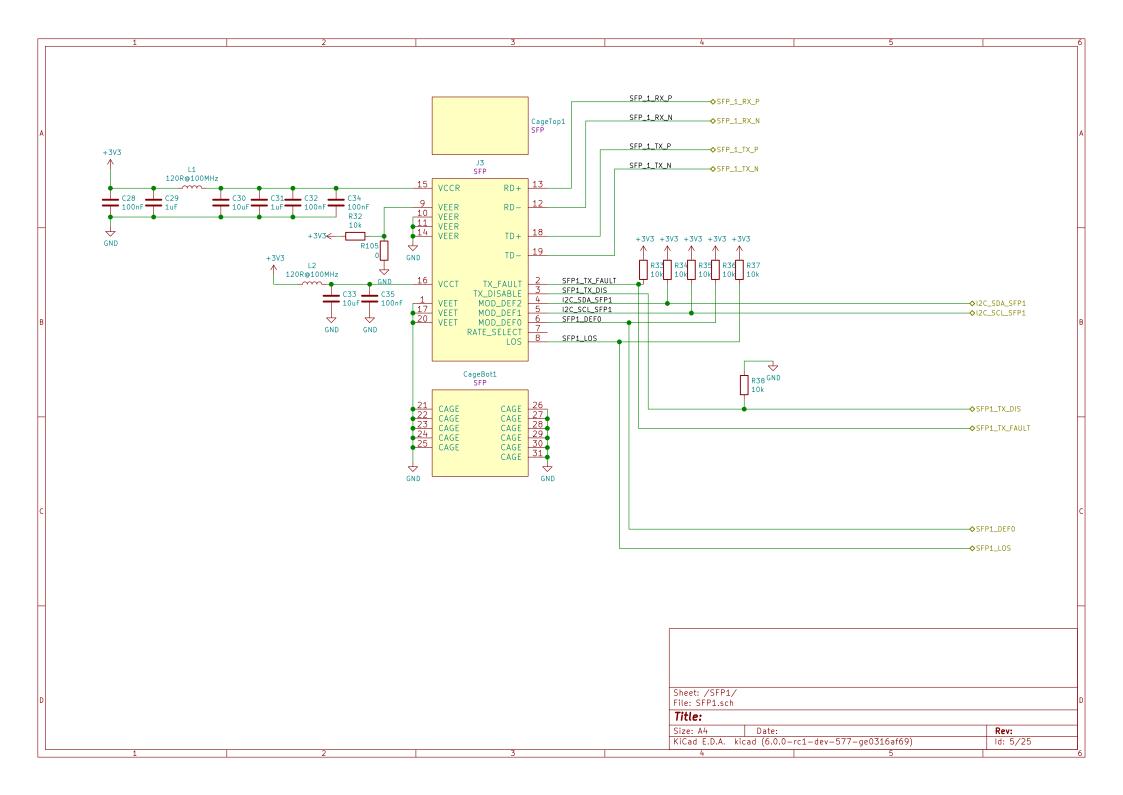
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GFMC2\_CLK1\_M2C\_N FMC2\_CLK0\_M2C\_P
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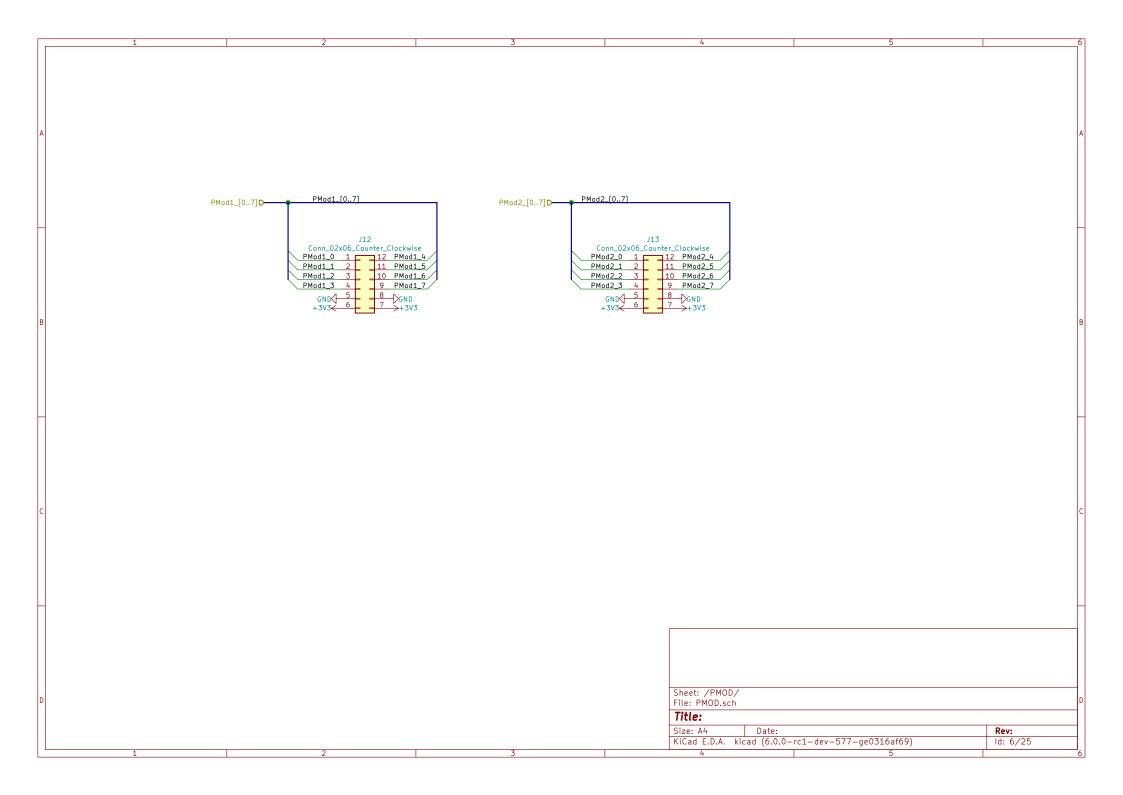
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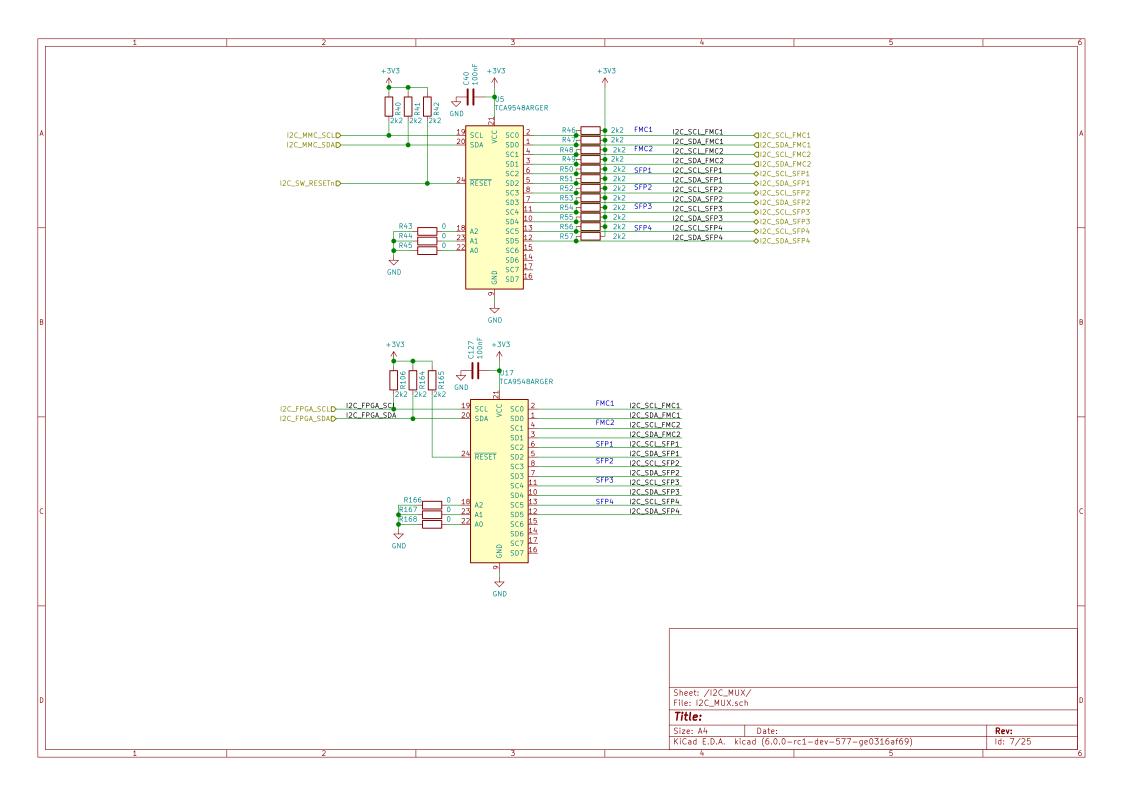
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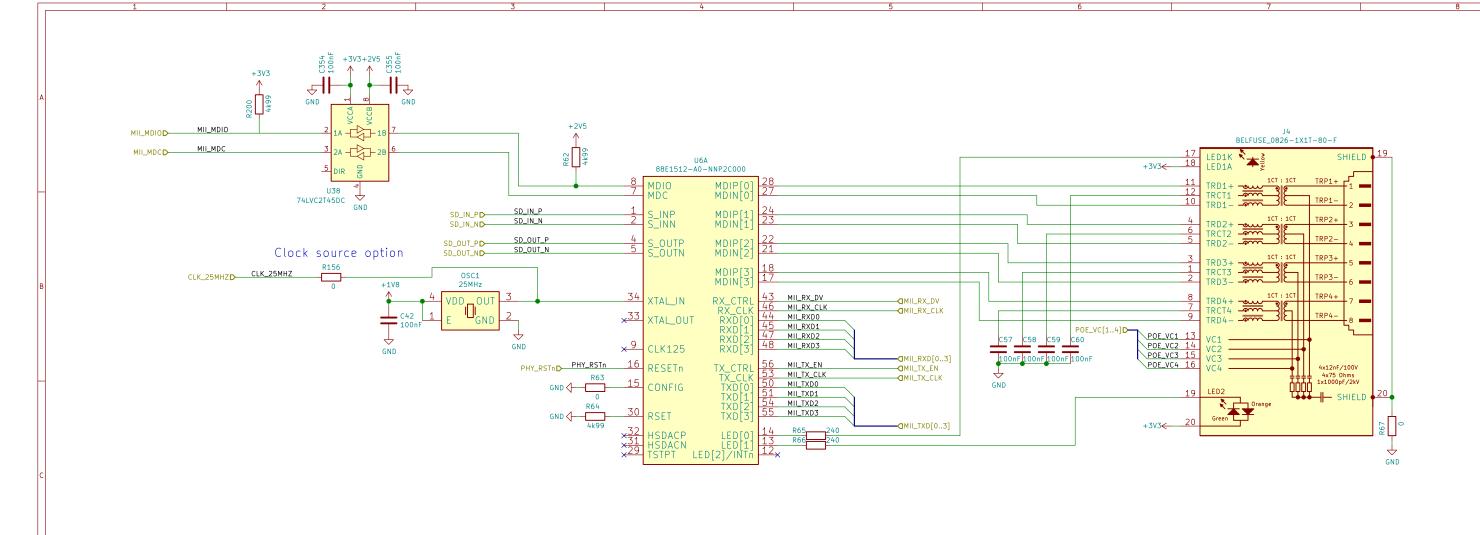


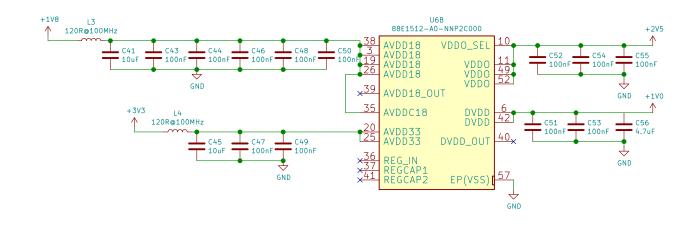


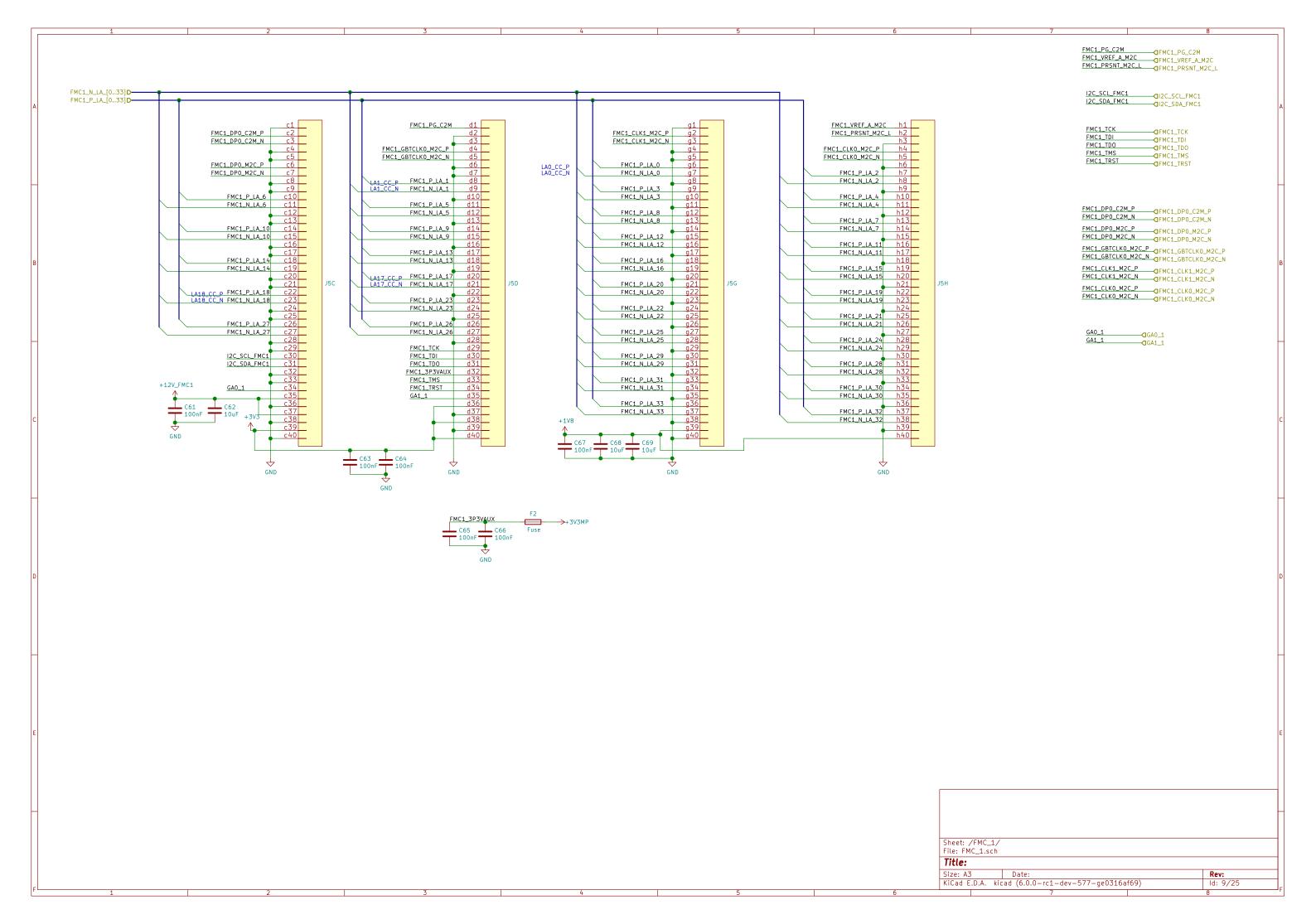


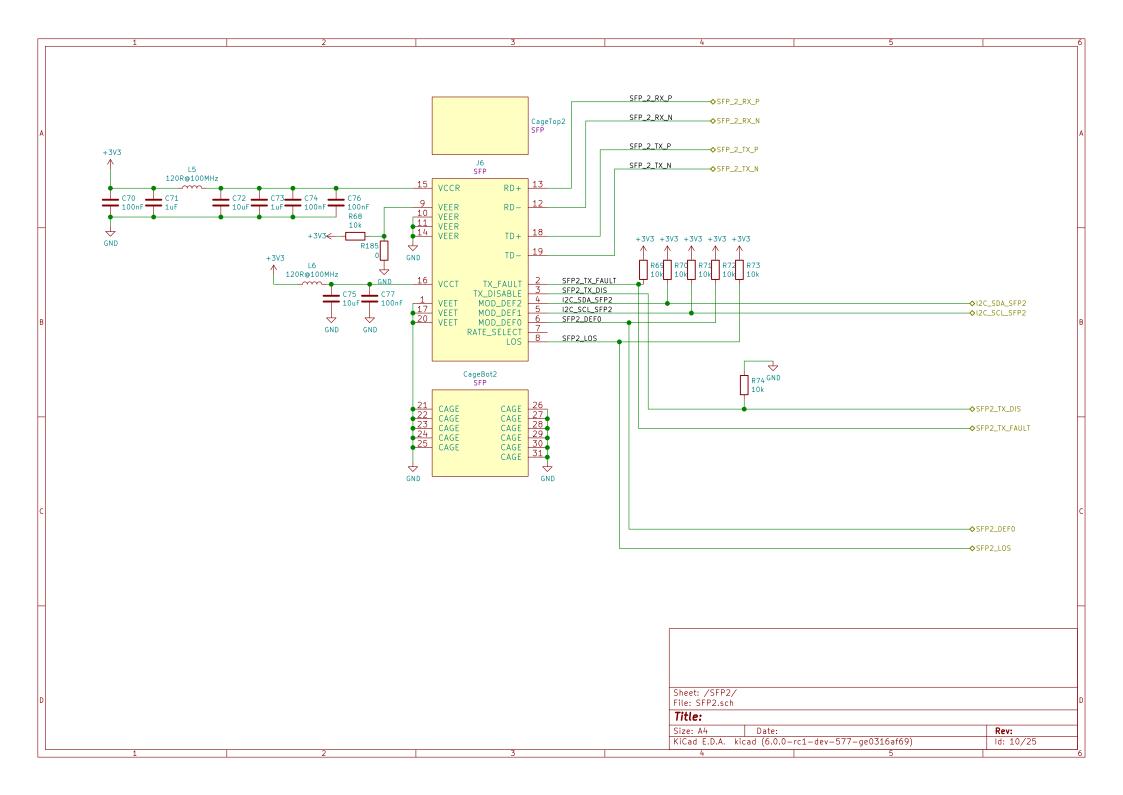


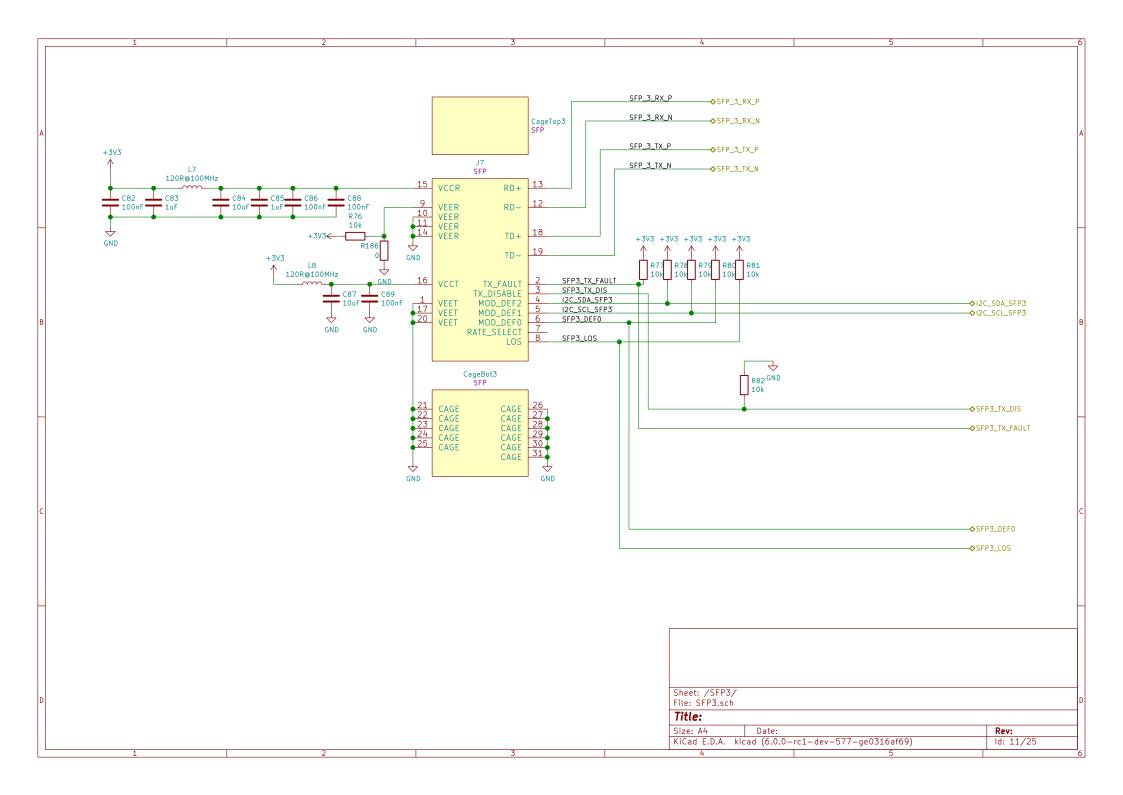


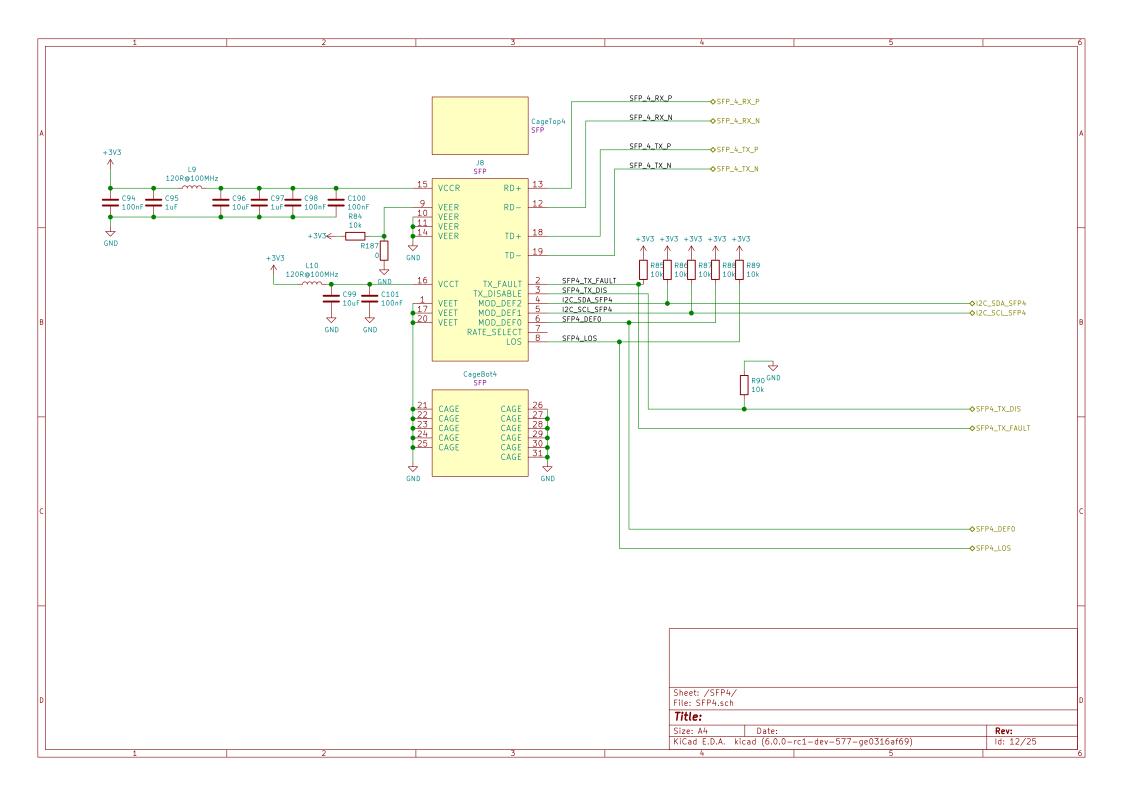


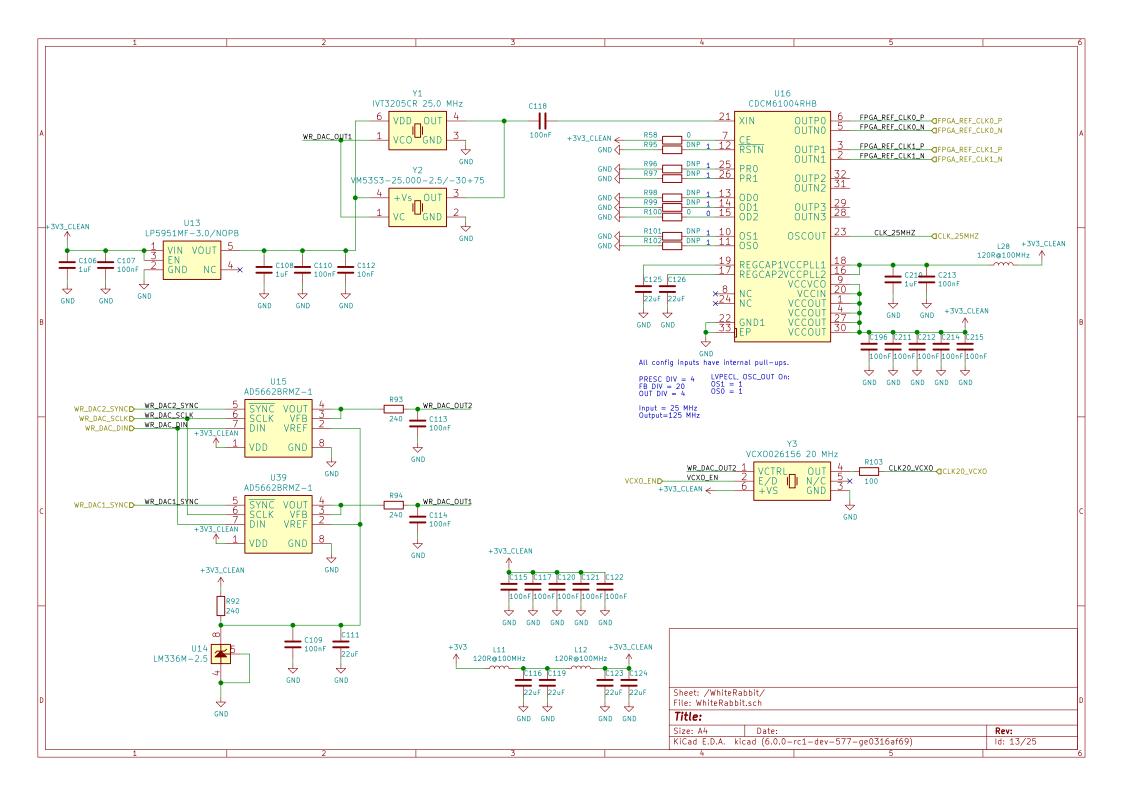


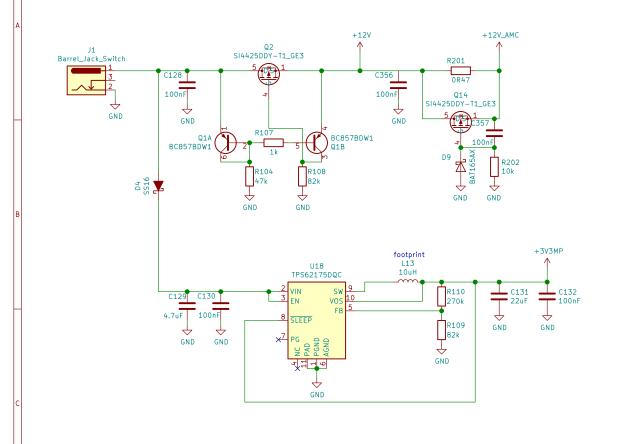


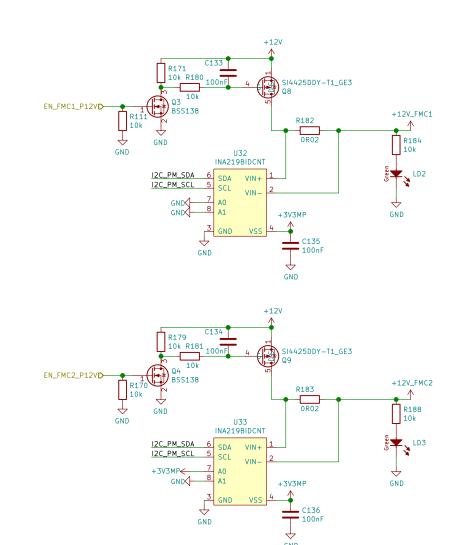


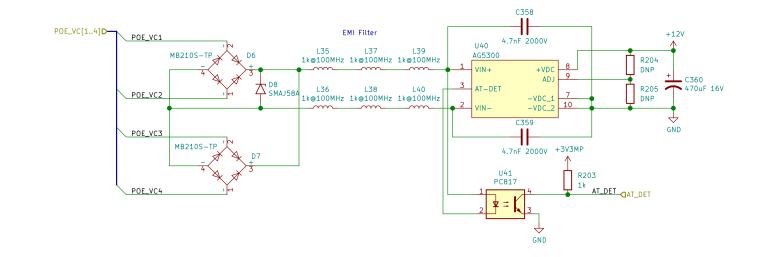


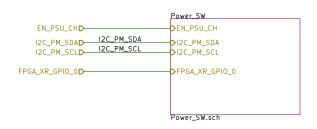


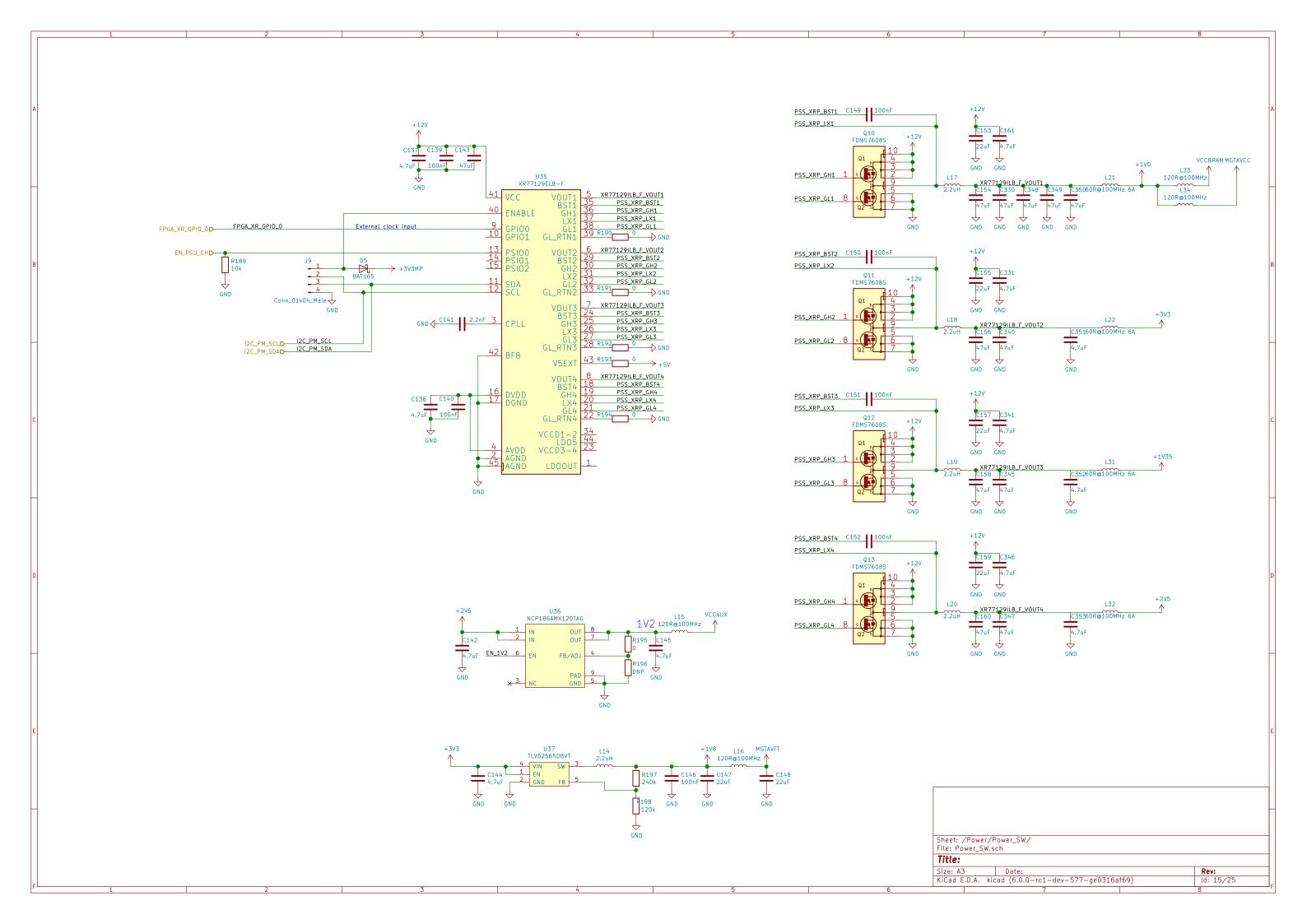


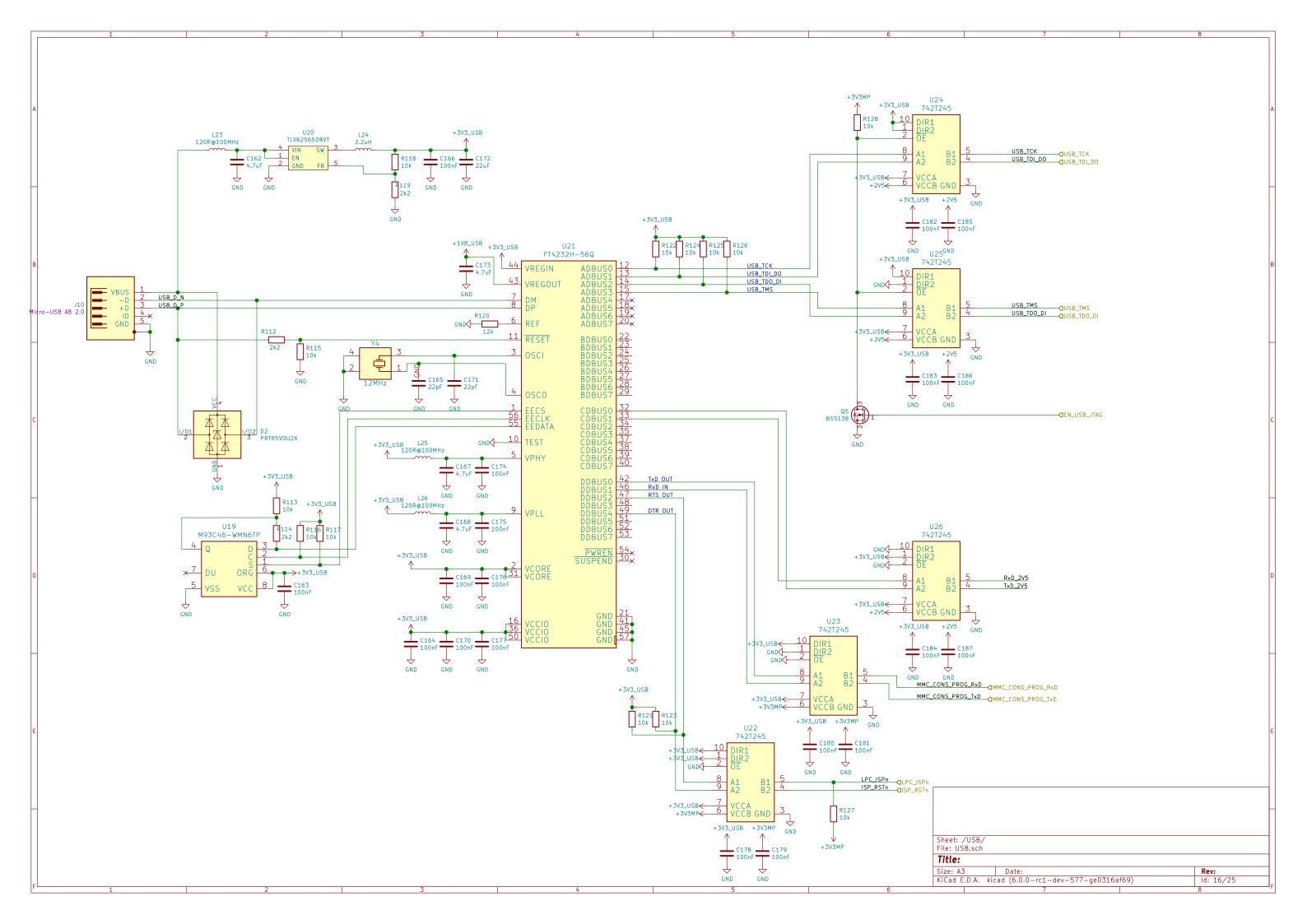


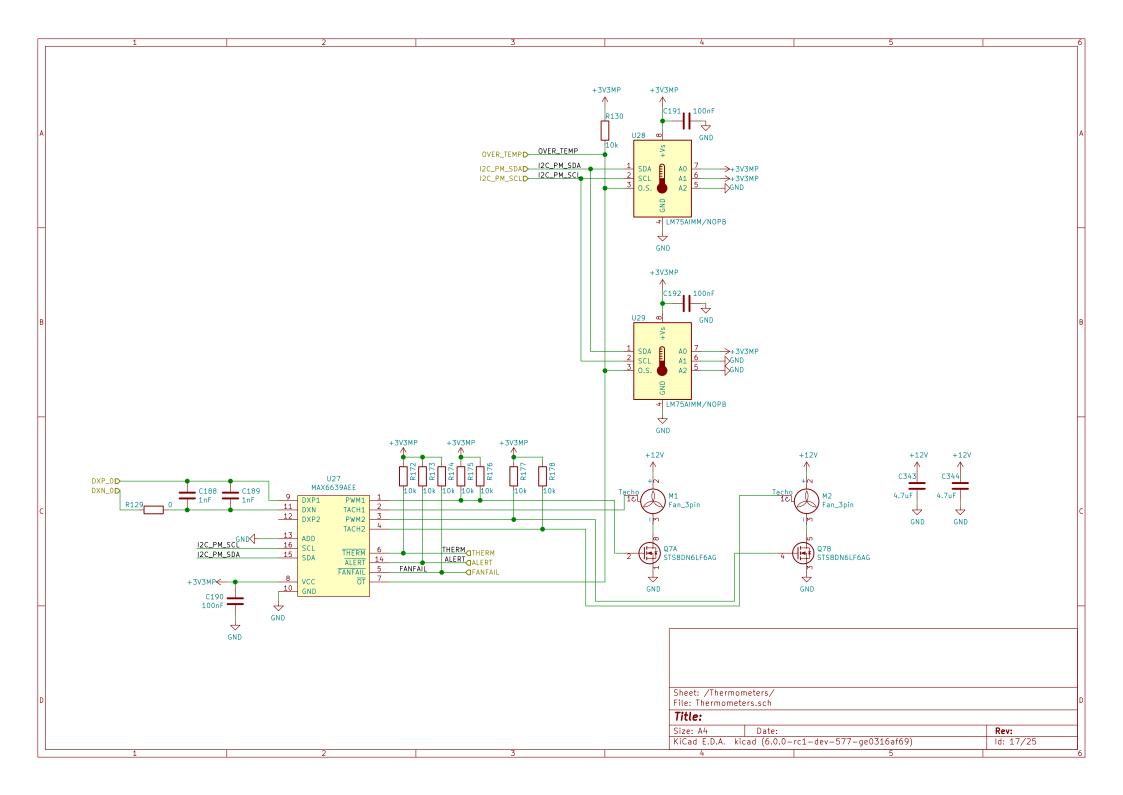


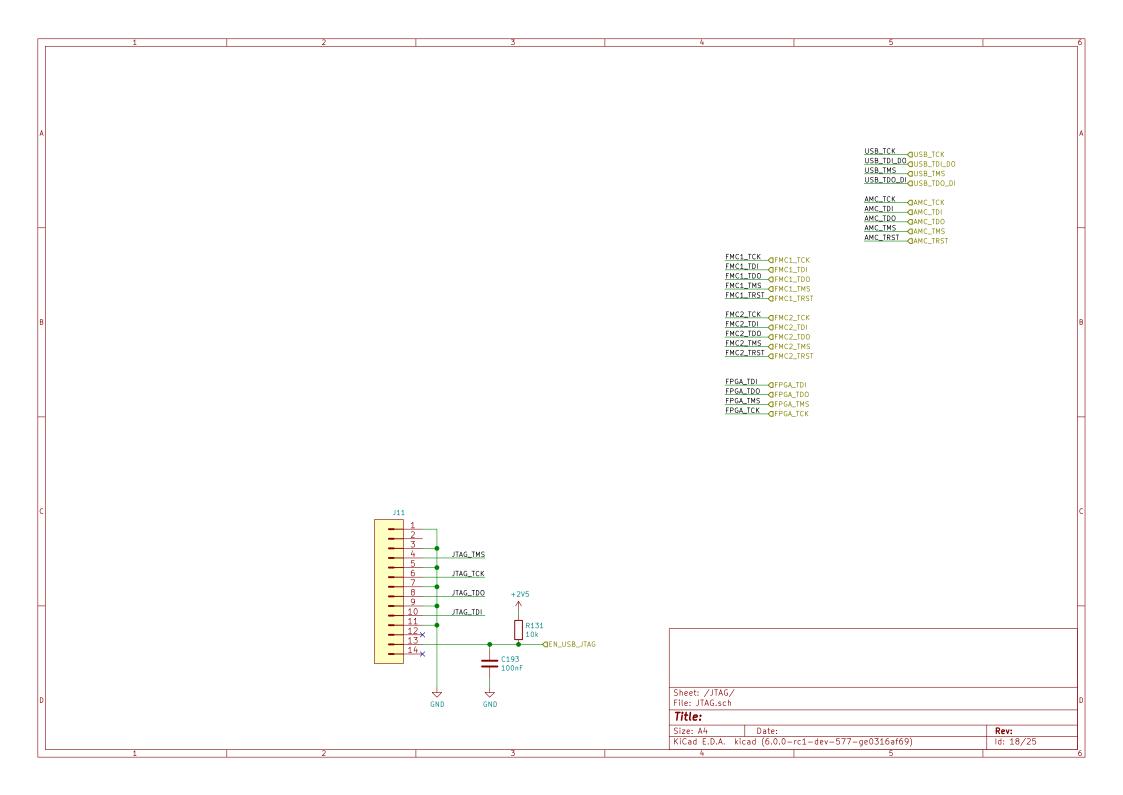


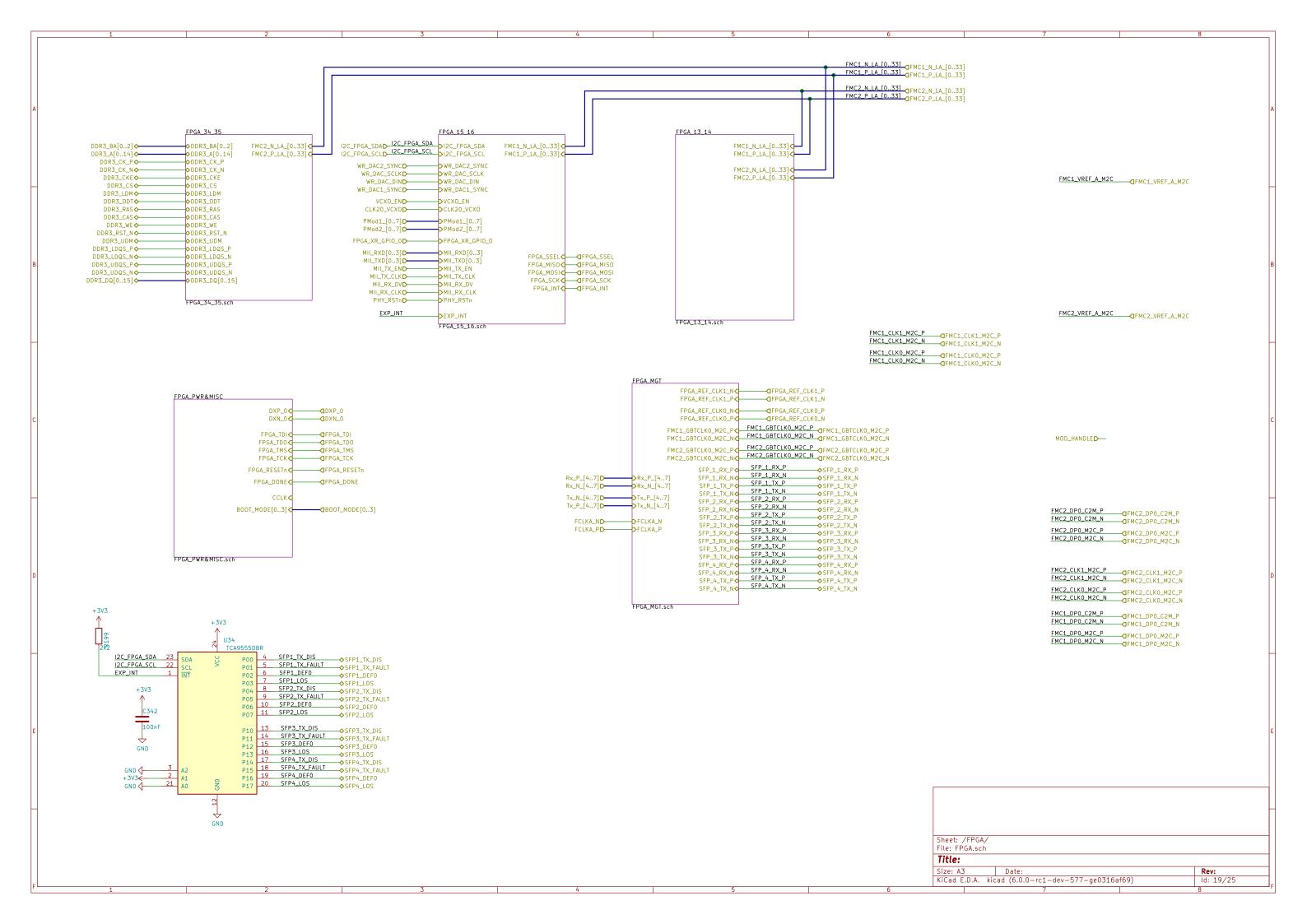


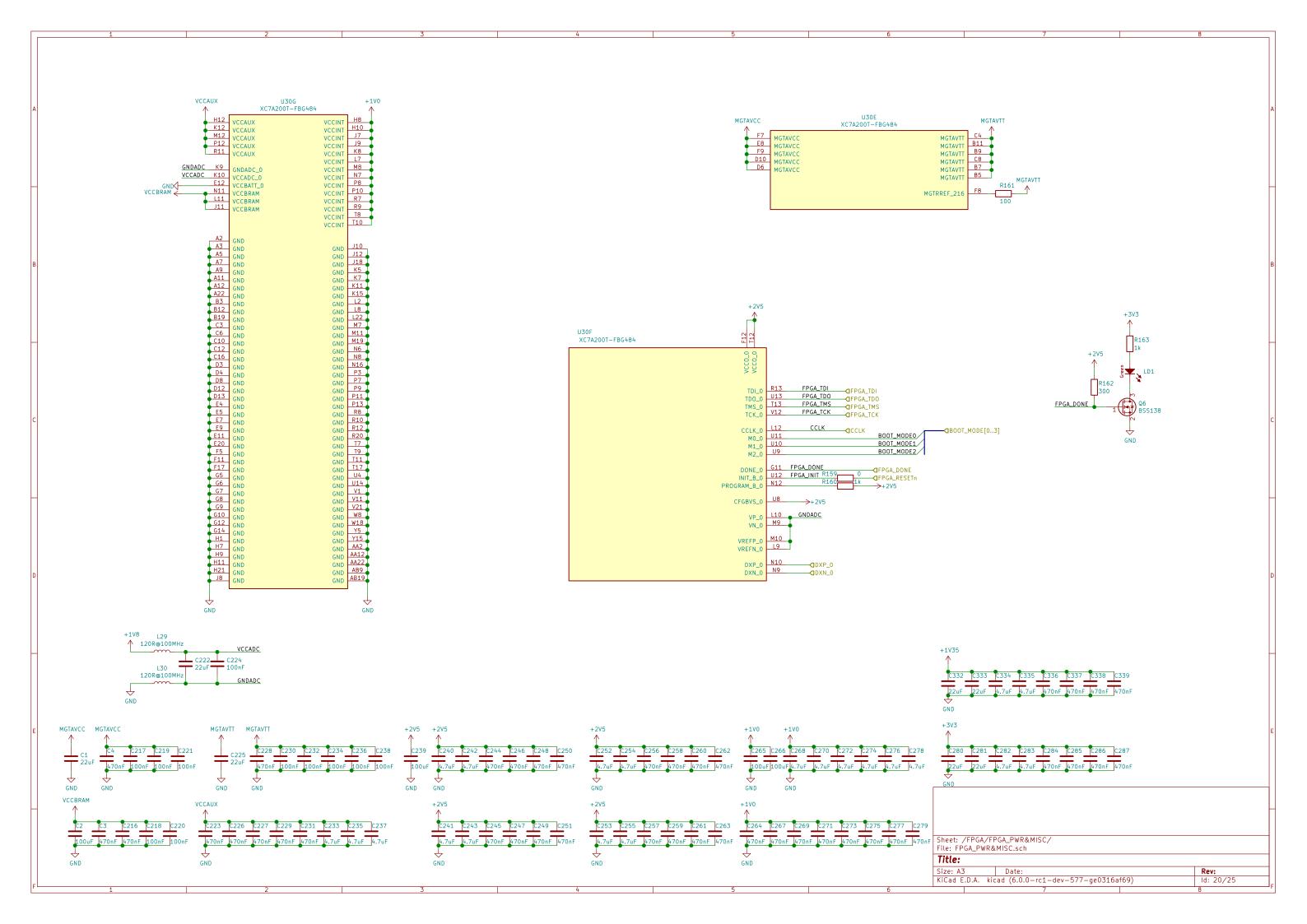


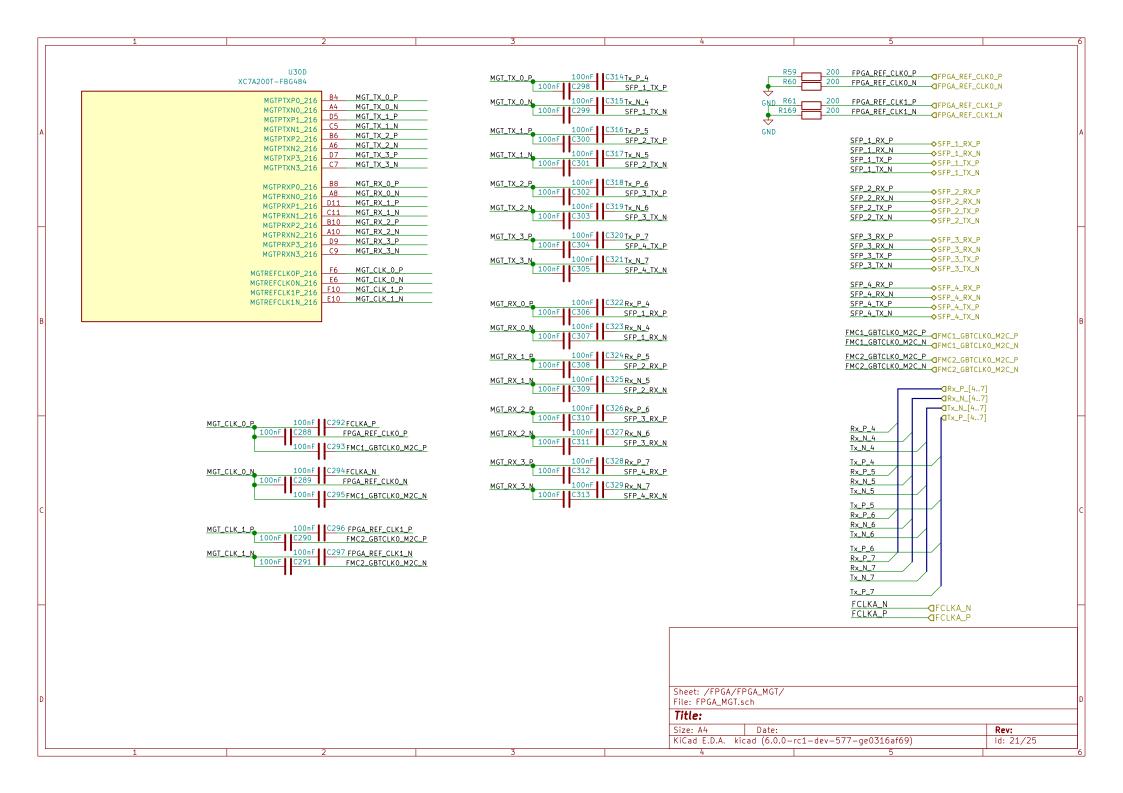


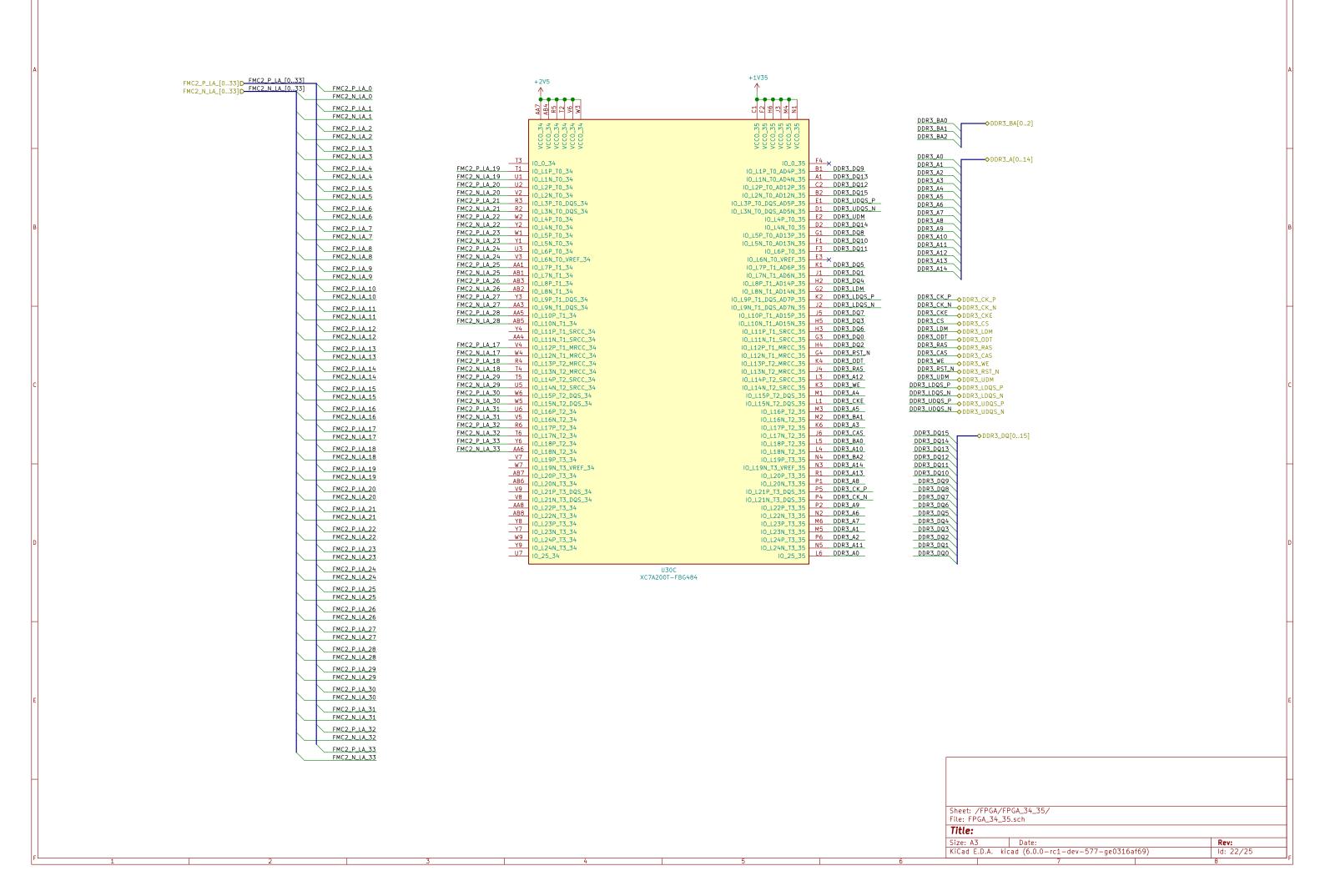












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GFPGA\_XR\_GPIO\_0 FMC1 P LA 16 N20 FMC1\_N\_LA\_16 M20 FMC1\_N\_LA\_18 D\_L18N\_T2\_A23\_15 K13 PHY RSTn D\_L19P\_T3\_A22\_15 FMC1\_P\_LA\_19 MII\_RX\_DV K14 \_\_L19N\_T3\_A21\_VREF\_15 FMC1\_N\_LA\_19 FMC1\_P\_LA\_12 M13 FMC1\_N\_LA\_12 L13 FPGA\_XR\_GPIO\_0 1 L20P T3 A20 15 FMC1\_P\_LA\_20 I2C\_SW\_RESETn FMC1\_N\_LA\_20 MII\_TX\_EN D\_L21P\_T3\_DQS\_15 D\_L21N\_T3\_DQS\_A18\_15 MII\_RXD0 J17 FMC1\_P\_LA\_21 MII\_RXD1 L14 L22P T3 A17 15 FMC1\_N\_LA\_21 MII RXD2 115 MII RXDO 0 L22N T3 A16 15 IO\_L22N\_T3\_16 IO\_L23P\_T3\_16 IO\_L23N\_T3\_16 D21 FMC1\_P\_LA\_22 MII\_RXD3 L16 MII\_RXD1 MII\_TXD0 K16
MII\_TXD1 M15 FMC1\_N\_LA\_22 MII\_RXD2 IO L23N T3 FWE B 15 MII\_RXD3 IO\_L24P\_T3\_16 G21 FMC1 P LA 23 MII\_TXD2 IO\_L24N\_T3\_16 G22 IO\_L24N\_T3\_RS0\_15 **—□**MII\_RXD[0..3] FMC1\_N\_LA\_23 F21 MII\_TXD3 M17 10\_25\_15 10\_25\_16 FMC1\_P\_LA\_24 U30B XC7A200T-FBG484 FMC1\_N\_LA\_24 MII\_TXD0 FMC1\_P\_LA\_25 MII\_TXD1 FMC1\_N\_LA\_25 MII\_TXD3 FMC1\_P\_LA\_26 **-□**MII\_TXD[0..3] FMC1\_N\_LA\_26 FMC1\_P\_LA\_27 FMC1\_N\_LA\_27 FMC1\_P\_LA\_28 FMC1\_N\_LA\_28 FMC1\_P\_LA\_29 FMC1\_N\_LA\_29 FMC1\_P\_LA\_30 FMC1\_N\_LA\_30 FMC1\_P\_LA\_31 FMC1\_N\_LA\_31 FMC1\_P\_LA\_32 FMC1\_N\_LA\_32 FMC1\_P\_LA\_33 FMC1\_N\_LA\_33 Sheet: /FPGA/FPGA\_15\_16/ File: FPGA\_15\_16.sch Title:

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