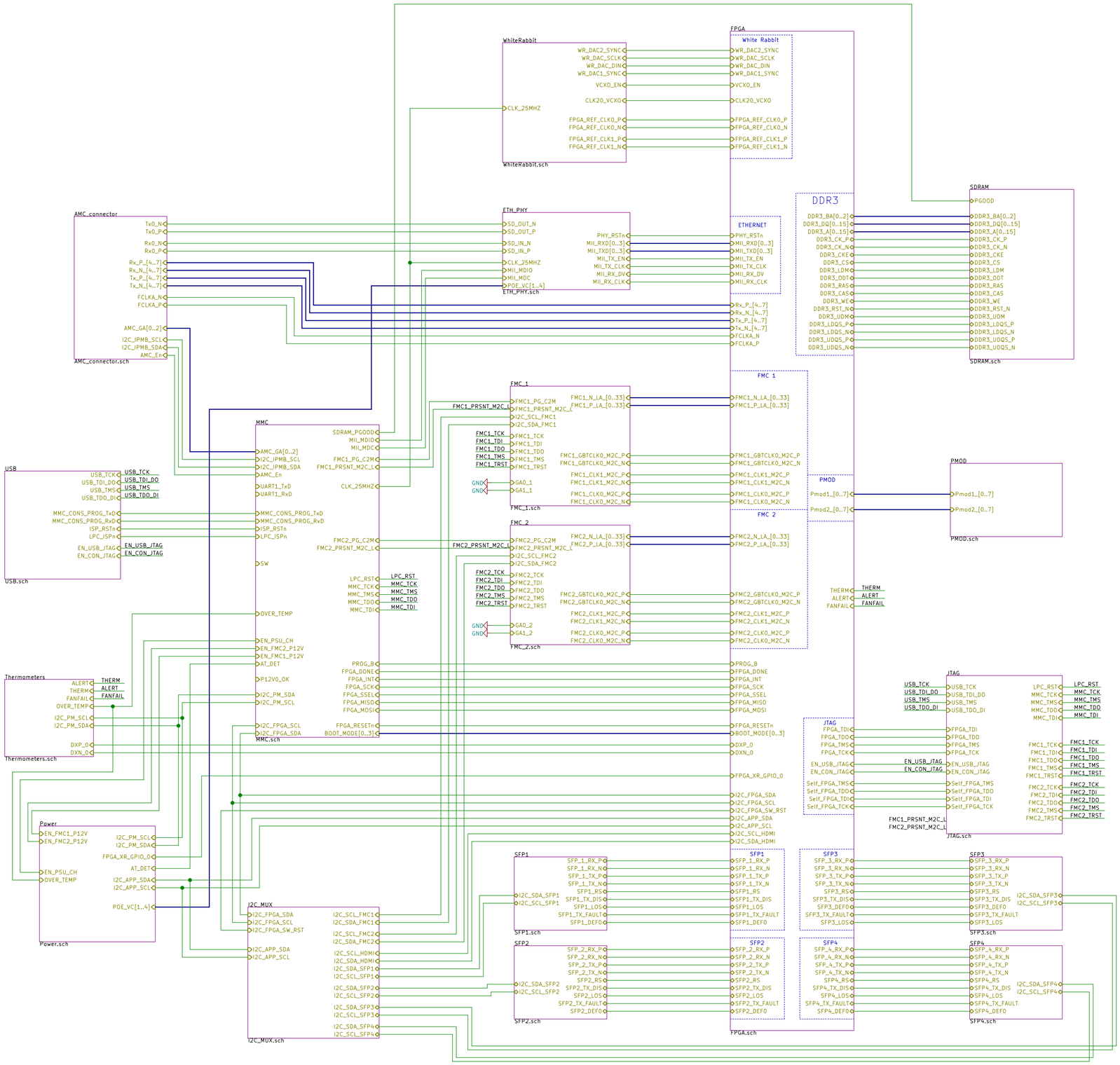
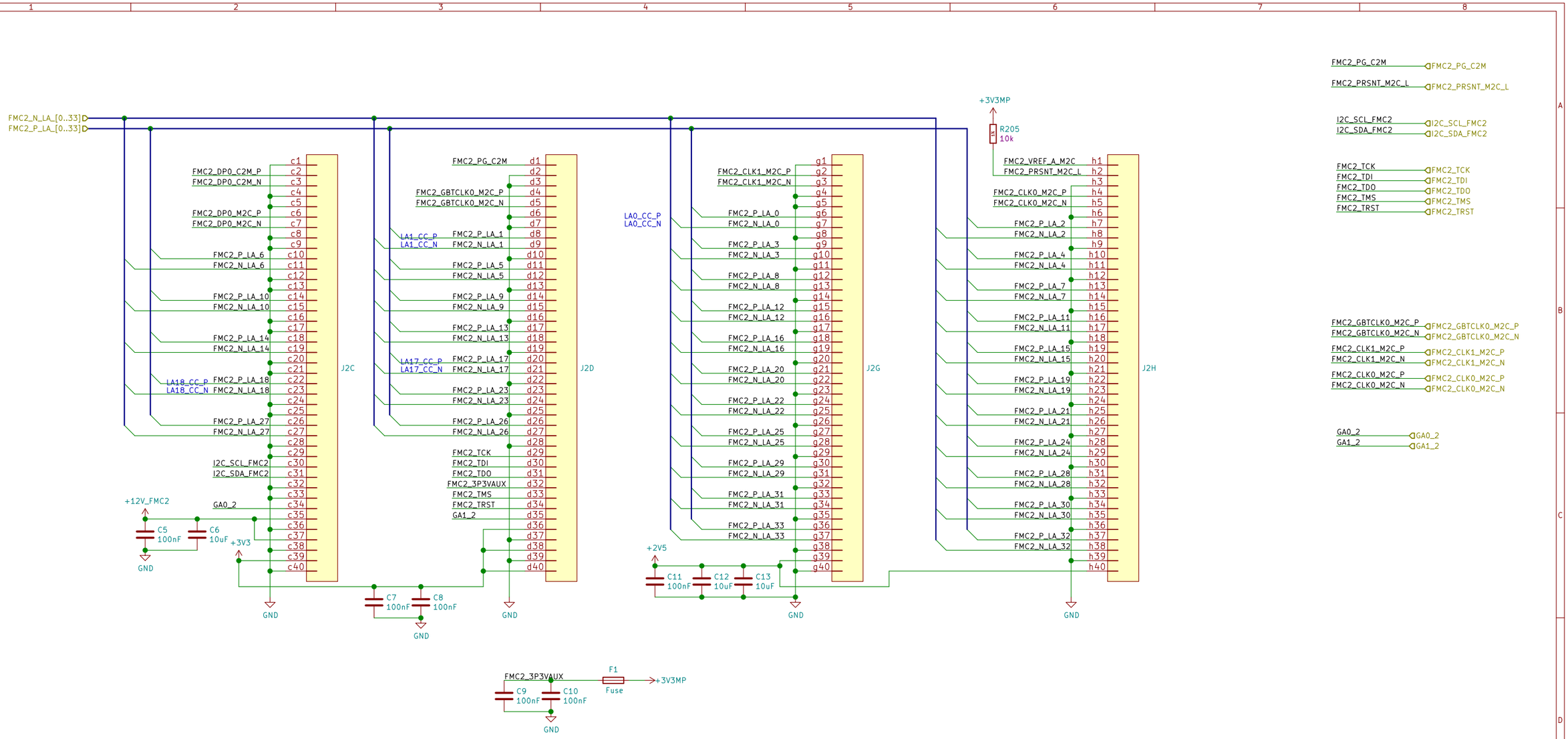


Michał Gąska / WUT

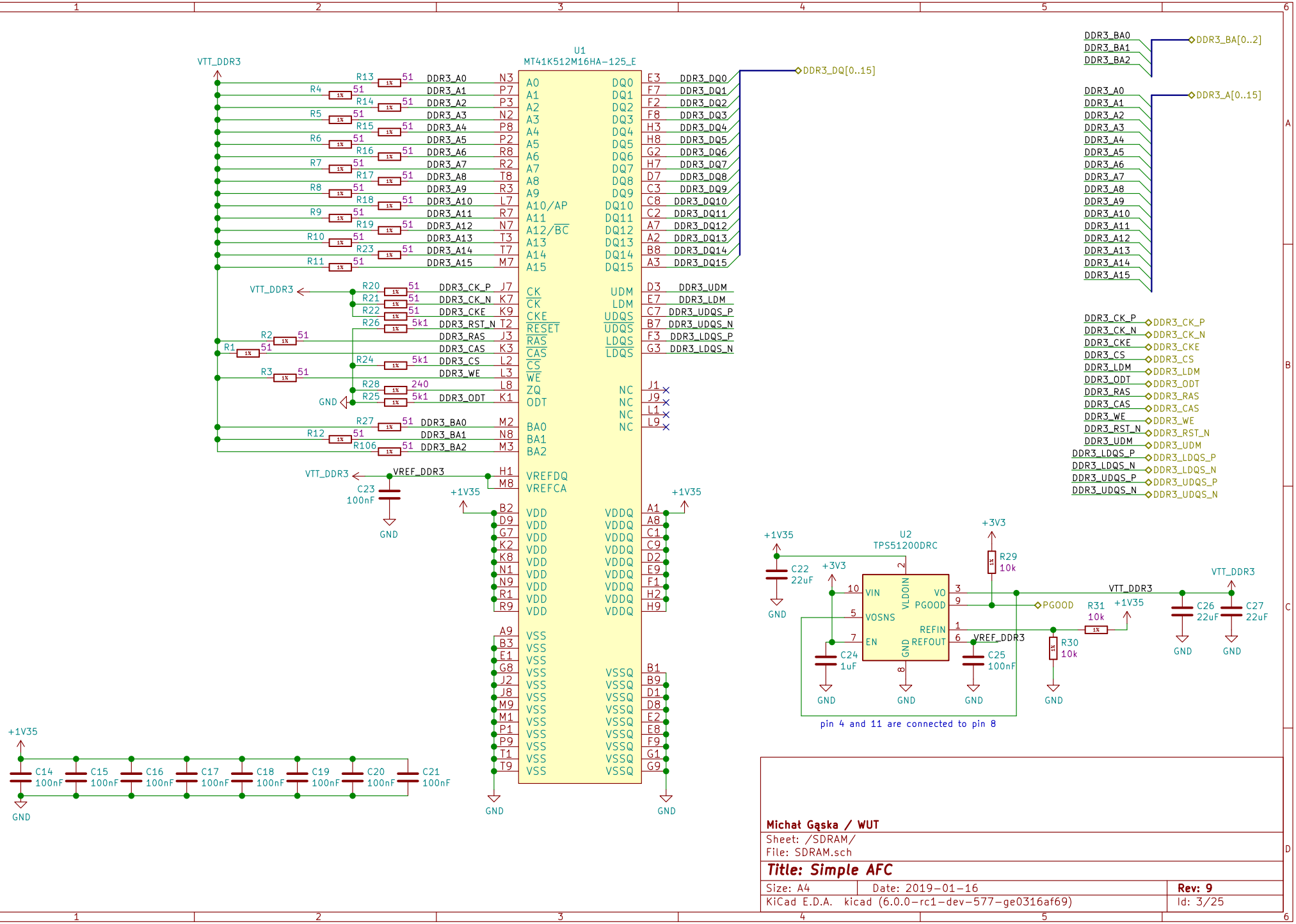
Sheet: /
File: AMC_FMC_Carrier-PcbDoc.sch

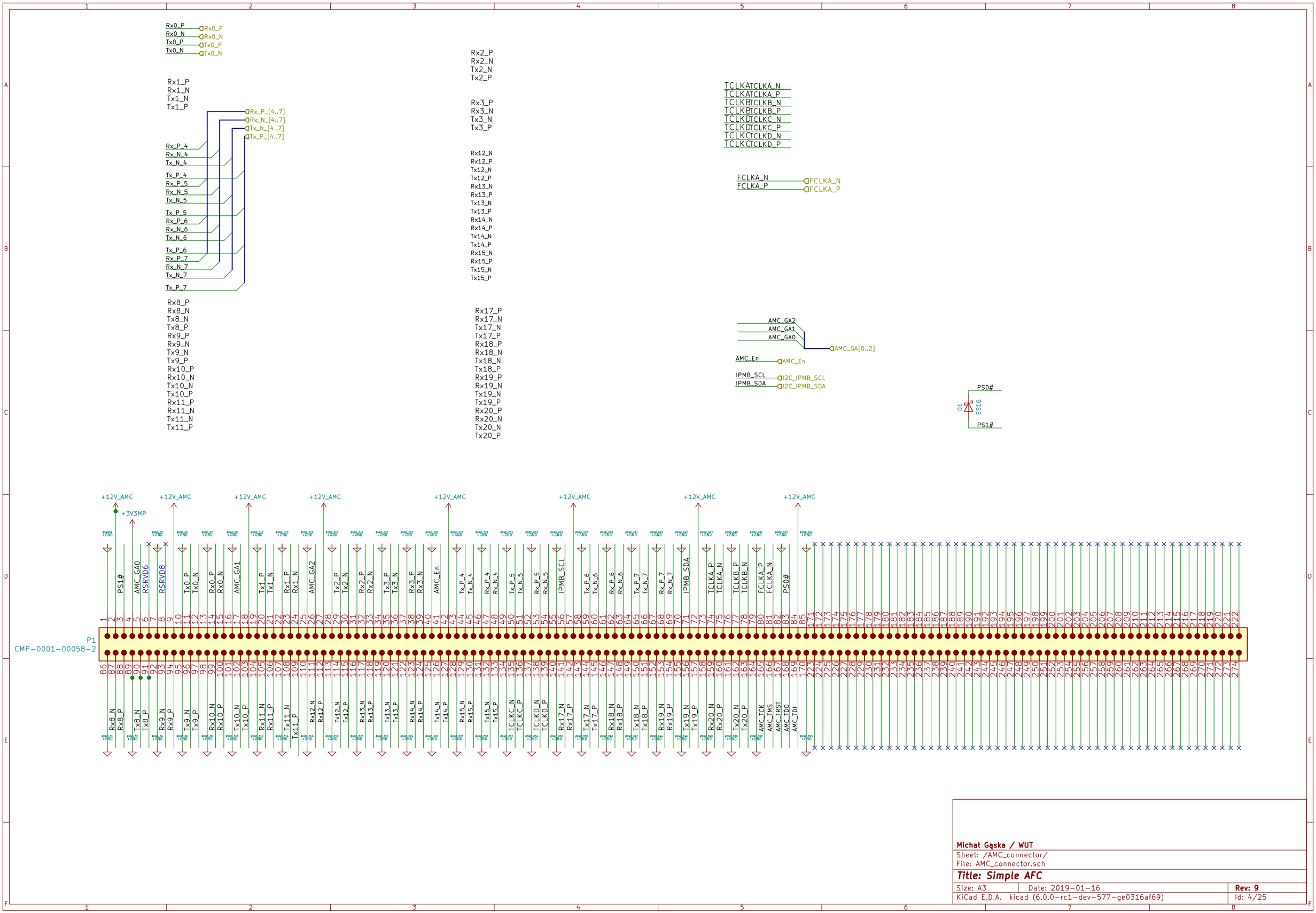
Title: Simple AFC

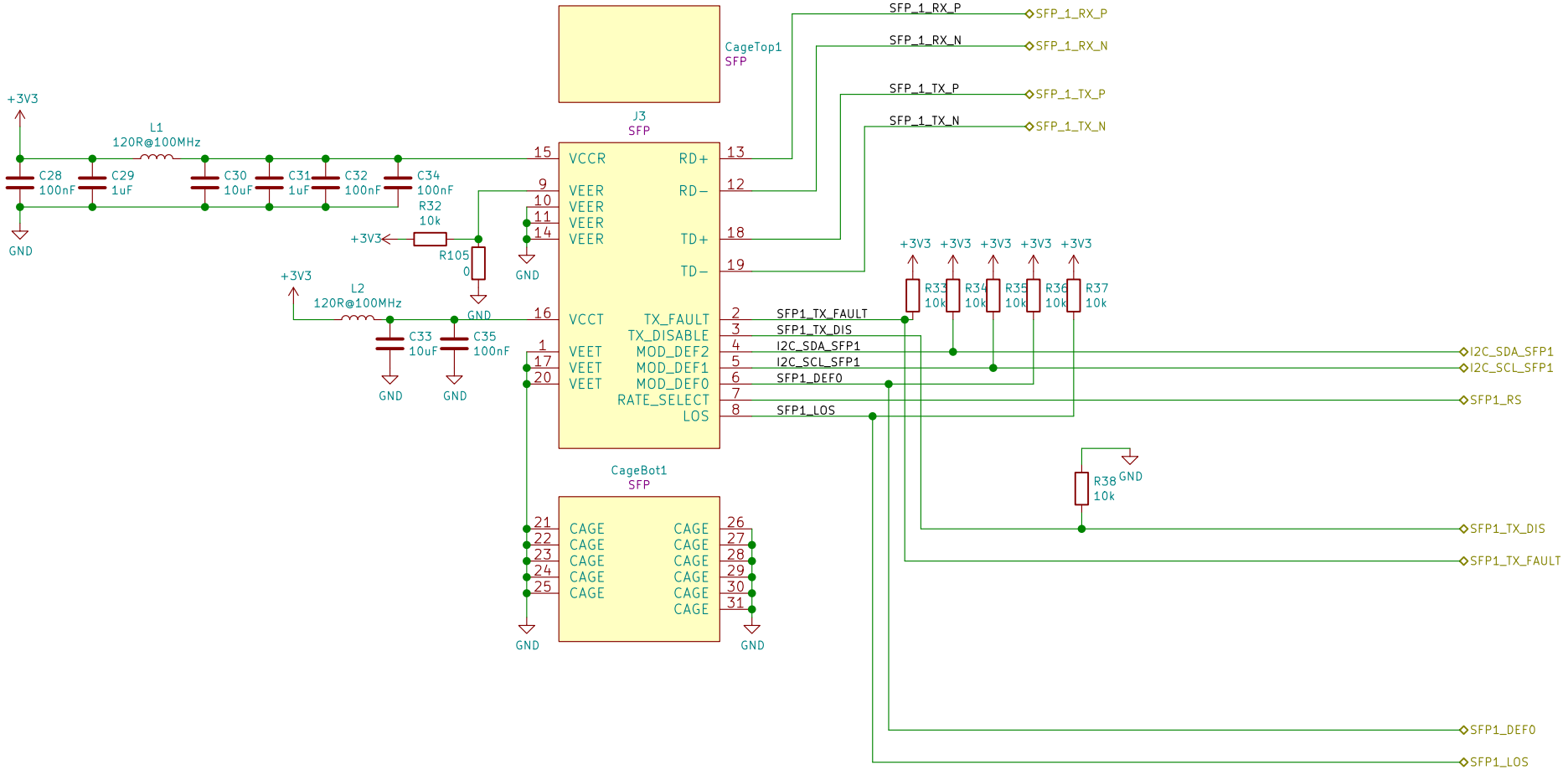
Size: A2	Date: 2019-01-16	**Rev: 9**
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)		Id: 1/25



Michał Gąska / WUT		
Sheet: /FMC_2/		
File: FMC_2.sch		
Title: Simple AFC		
Size: A3	Date: 2019-01-16	**Rev: 9**
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)		Id: 2/25

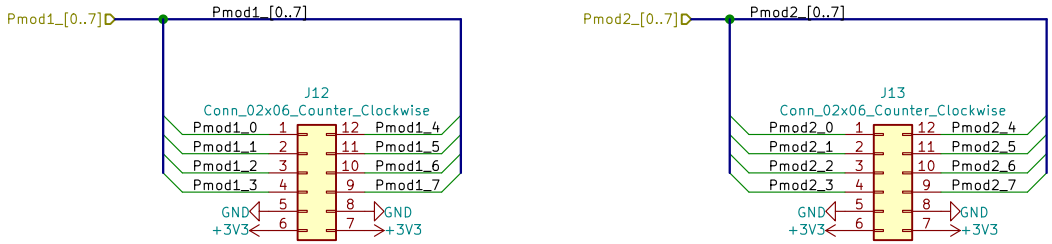

U1
MT41K512M16HA-125_E
VTT_DDR3
DDR3_DQ[0..15]
DDR3_BA[0..2]
DDR3_A[0..15]
DDR3_A0
DDR3_A1
DDR3_A2
DDR3_A3
DDR3_A4
DDR3_A5
DDR3_A6
DDR3_A7
DDR3_A8
DDR3_A9
DDR3_A10
DDR3_A11
DDR3_A12
DDR3_A13
DDR3_A14
DDR3_A15
DDR3_CK_P
DDR3_CK_N
DDR3_CKE
DDR3_RST_N
DDR3_RAS
DDR3_CAS
DDR3_CS
DDR3_WE
DDR3_ODT
DDR3_BA0
DDR3_BA1
DDR3_BA2
DDR3_UDM
DDR3_LDM
DDR3_UDQS_P
DDR3_UDQS_N
DDR3_LDQS_P
DDR3_LDQS_N
VREF_DDR3
+1V35
GND
U2
TPS51200DRC
+3V3
PGOOD
VTT_DDR3
pin 4 and 11 are connected to pin 8
Michał Gąska / WUT
Sheet: /SDRAM/
File: SDRAM.sch
Title: Simple AFC
Size: A4
Date: 2019-01-16
Rev: 9
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)
Id: 3/25


Rx0_P
Rx0_N
Tx0_P
Tx0_N
Rx0_P
Rx0_N
Tx0_P
Tx0_N
Rx1_P
Rx1_N
Tx1_N
Tx1_P
Rx_P_[4..7]
Rx_N_[4..7]
Tx_N_[4..7]
Tx_P_[4..7]
Rx_P_4
Rx_N_4
Tx_N_4
Tx_P_4
Rx_P_5
Rx_N_5
Tx_N_5
Tx_P_5
Rx_P_6
Rx_N_6
Tx_N_6
Tx_P_6
Rx_P_7
Rx_N_7
Tx_N_7
Tx_P_7
Rx8_P
Rx8_N
Tx8_N
Tx8_P
Rx9_P
Rx9_N
Tx9_N
Tx9_P
Rx10_P
Rx10_N
Tx10_N
Tx10_P
Rx11_P
Rx11_N
Tx11_N
Tx11_P
Rx2_P
Rx2_N
Tx2_N
Tx2_P
Rx3_P
Rx3_N
Tx3_N
Tx3_P
Rx12_N
Rx12_P
Tx12_N
Tx12_P
Rx13_N
Rx13_P
Tx13_N
Tx13_P
Rx14_N
Rx14_P
Tx14_N
Tx14_P
Rx15_N
Rx15_P
Tx15_N
Tx15_P
Rx17_P
Rx17_N
Tx17_N
Tx17_P
Rx18_P
Rx18_N
Tx18_N
Tx18_P
Rx19_P
Rx19_N
Tx19_N
Tx19_P
Rx20_P
Rx20_N
Tx20_N
Tx20_P
TCLKATCLKA_N
TCLKATCLKA_P
TCLKBTCLKB_N
TCLKBTCLKB_P
TCLKDTCLKC_N
TCLKDTCLKC_P
TCLKCTCLKD_N
TCLKCTCLKD_P
FCLKA_N
FCLKA_P
FCLKA_N
FCLKA_P
AMC_GA2
AMC_GA1
AMC_GA0
AMC_GA[0..2]
AMC_En
AMC_En
IPMB_SCL
IPMB_SDA
I2C_IPMB_SCL
I2C_IPMB_SDA
PS0#
D1
SS16
PS1#
+12V_AMC
+3V3MP
P1
CMP-0001-00058-2
PS1#
AMC_GA0
RSRVD6
RSRVD8
Tx0_P
Tx0_N
Rx0_P
Rx0_N
AMC_GA1
Tx1_P
Tx1_N
Rx1_P
Rx1_N
AMC_GA2
Tx2_P
Tx2_N
Rx2_P
Rx2_N
Tx3_P
Tx3_N
Rx3_P
Rx3_N
AMC_En
Tx_P_4
Tx_N_4
Rx_P_4
Rx_N_4
Tx_P_5
Tx_N_5
Rx_P_5
Rx_N_5
IPMB_SCL
Tx_P_6
Tx_N_6
Rx_P_6
Rx_N_6
Tx_P_7
Tx_N_7
Rx_P_7
Rx_N_7
IPMB_SDA
TCLKA_P
TCLKA_N
TCLKB_P
TCLKB_N
FCLKA_P
FCLKA_N
PS0#
Rx8_N
Rx8_P
Tx8_N
Tx8_P
Rx9_N
Rx9_P
Tx9_N
Tx9_P
Rx10_N
Rx10_P
Tx10_N
Tx10_P
Rx11_N
Rx11_P
Tx11_N
Tx11_P
Rx12_N
Rx12_P
Tx12_N
Tx12_P
Rx13_N
Rx13_P
Tx13_N
Tx13_P
Rx14_N
Rx14_P
Tx14_N
Tx14_P
TCLKC_N
TCLKC_P
TCLKD_N
TCLKD_P
Rx17_N
Rx17_P
Tx17_N
Tx17_P
Rx18_N
Rx18_P
Tx18_N
Tx18_P
Rx19_N
Rx19_P
Tx19_N
Tx19_P
Rx20_N
Rx20_P
Tx20_N
Tx20_P
AMC_TCK
AMC_TMS
AMC_TRST
AMC_TDO
AMC_TDI
Michał Gąska / WUT
Sheet: /AMC_connector/
File: AMC_connector.sch
Title: Simple AFC
Size: A3
Date: 2019-01-16
Rev: 9
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)
Id: 4/25



Michał Gąska / WUT	
Sheet: /SFP1/	
File: SFP1.sch	
Title: Simple AFC	
Size: A4	Date: 2019-01-16
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)	Id: 5/25

Rev: 9

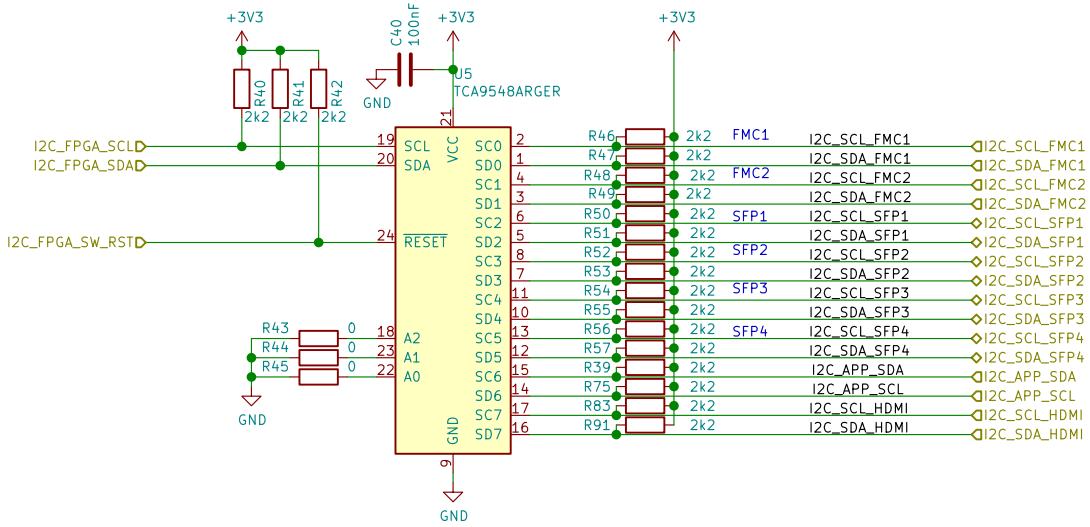


Michał Gąska / WUT

Sheet: /PMOD/
File: PMOD.sch

Title: Simple AFC

Size: A4	Date: 2019-01-16	**Rev: 9**
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)		Id: 6/25



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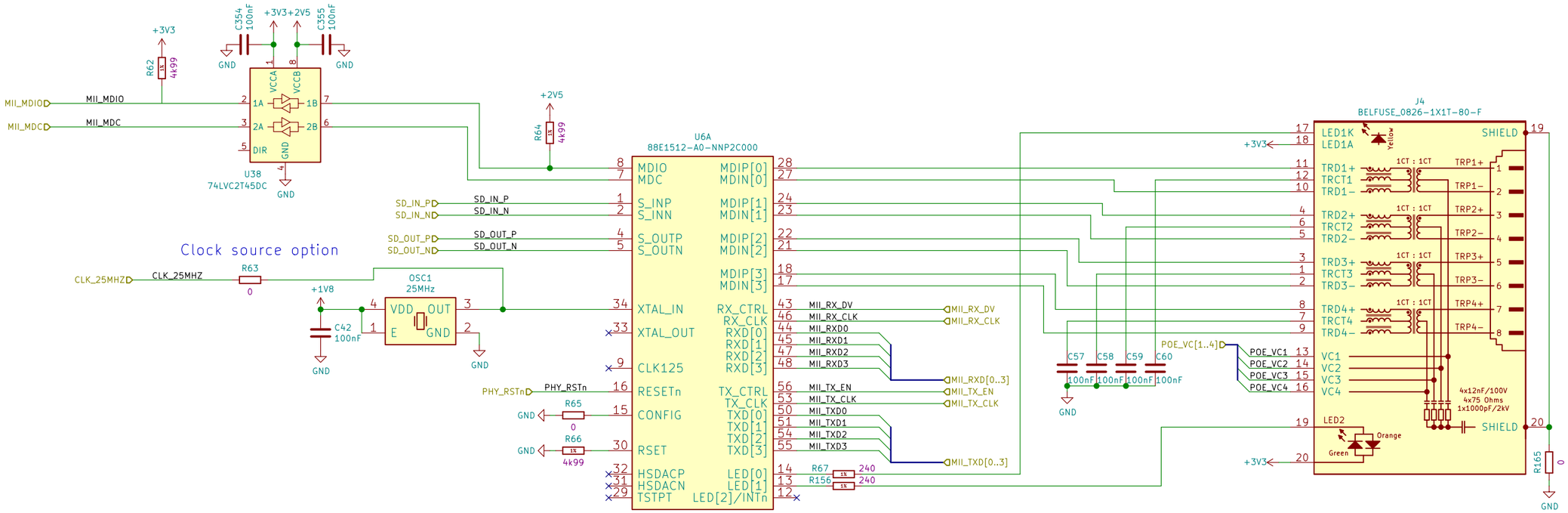
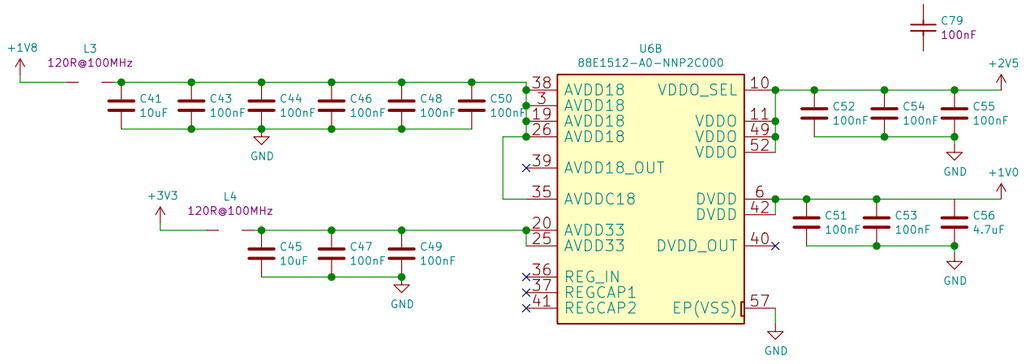
Sheet: /I2C_MUX/
File: I2C_MUX.sch

Title: Simple AFC

Size: A4	Date: 2019-01-16	**Rev: 9**
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)		Id: 7/25





Michał Gąska / WUT		
Sheet: /ETH_PHY/ File: ETH_PHY.sch		
Title: Simple AFC		
Size: A3	Date: 2019-01-16	**Rev: 9**
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)		Id: 8/25

FMC1_N_LA_[0..33]
FMC1_P_LA_[0..33]

FMC1_PG_C2M
FMC1_PRSNT_M2C_L
I2C_SCL_FMC1
I2C_SDA_FMC1
FMC1_TCK
FMC1_TDI
FMC1_TDO
FMC1_TMS
FMC1_TRST
FMC1_GBTCLK0_M2C_P
FMC1_GBTCLK0_M2C_N
FMC1_CLK1_M2C_P
FMC1_CLK1_M2C_N
FMC1_CLK0_M2C_P
FMC1_CLK0_M2C_N
GA0_1
GA1_1

+3V3MP
R234
10k

J5C

	c1		
FMC1_DP0_C2M_P	c2		
FMC1_DP0_C2M_N	c3		
	c4		
	c5		
FMC1_DP0_M2C_P	c6		
FMC1_DP0_M2C_N	c7		
	c8		
	c9		
FMC1_P_LA_6	c10		
FMC1_N_LA_6	c11		
	c12		
	c13		
FMC1_P_LA_10	c14		
FMC1_N_LA_10	c15		
	c16		
	c17		
FMC1_P_LA_14	c18		
FMC1_N_LA_14	c19		
	c20		
	c21		
LA18_CC_P FMC1_P_LA_18	c22		
LA18_CC_N FMC1_N_LA_18	c23		
	c24		
	c25		
FMC1_P_LA_27	c26		
FMC1_N_LA_27	c27		
	c28		
	c29		
I2C_SCL_FMC1	c30		
I2C_SDA_FMC1	c31		
	c32		
	c33		
GA0_1	c34		
	c35		
	c36		
	c37		
	c38		
	c39		
	c40		

+12V_FMC1
C61 100nF
C62 10uF
+3V3
GND
GND

J5D

	d1	FMC1_PG_C2M	
	d2		
	d3		
FMC1_GBTCLK0_M2C_P	d4		
FMC1_GBTCLK0_M2C_N	d5		
	d6		
	d7		
LA1_CC_P FMC1_P_LA_1	d8		
LA1_CC_N FMC1_N_LA_1	d9		
FMC1_P_LA_5	d10		
FMC1_N_LA_5	d11		
	d12		
	d13		
FMC1_P_LA_9	d14		
FMC1_N_LA_9	d15		
	d16		
FMC1_P_LA_13	d17		
FMC1_N_LA_13	d18		
	d19		
LA17_CC_P FMC1_P_LA_17	d20		
LA17_CC_N FMC1_N_LA_17	d21		
	d22		
FMC1_P_LA_23	d23		
FMC1_N_LA_23	d24		
	d25		
FMC1_P_LA_26	d26		
FMC1_N_LA_26	d27		
	d28		
FMC1_TCK	d29		
FMC1_TDI	d30		
FMC1_TDO	d31		
FMC1_3P3VAUX	d32		
FMC1_TMS	d33		
FMC1_TRST	d34		
GA1_1	d35		
	d36		
	d37		
	d38		
	d39		
	d40		

C63 100nF
C64 100nF
GND
GND

J5G

	g1	FMC1_CLK1_M2C_P	
	g2	FMC1_CLK1_M2C_N	
	g3		
	g4		
	g5		
LA0_CC_P FMC1_P_LA_0	g6		
LA0_CC_N FMC1_N_LA_0	g7		
FMC1_P_LA_3	g8		
FMC1_N_LA_3	g9		
FMC1_P_LA_8	g10		
FMC1_N_LA_8	g11		
FMC1_P_LA_12	g12		
FMC1_N_LA_12	g13		
FMC1_P_LA_16	g14		
FMC1_N_LA_16	g15		
FMC1_P_LA_20	g16		
FMC1_N_LA_20	g17		
FMC1_P_LA_22	g18		
FMC1_N_LA_22	g19		
FMC1_P_LA_25	g20		
FMC1_N_LA_25	g21		
FMC1_P_LA_29	g22		
FMC1_N_LA_29	g23		
FMC1_P_LA_31	g24		
FMC1_N_LA_31	g25		
FMC1_P_LA_33	g26		
FMC1_N_LA_33	g27		
	g28		
	g29		
	g30		
	g31		
	g32		
	g33		
	g34		
	g35		
	g36		
	g37		
	g38		
	g39		
	g40		

+2V5
C67 100nF
C68 10uF
C69 10uF
GND
GND

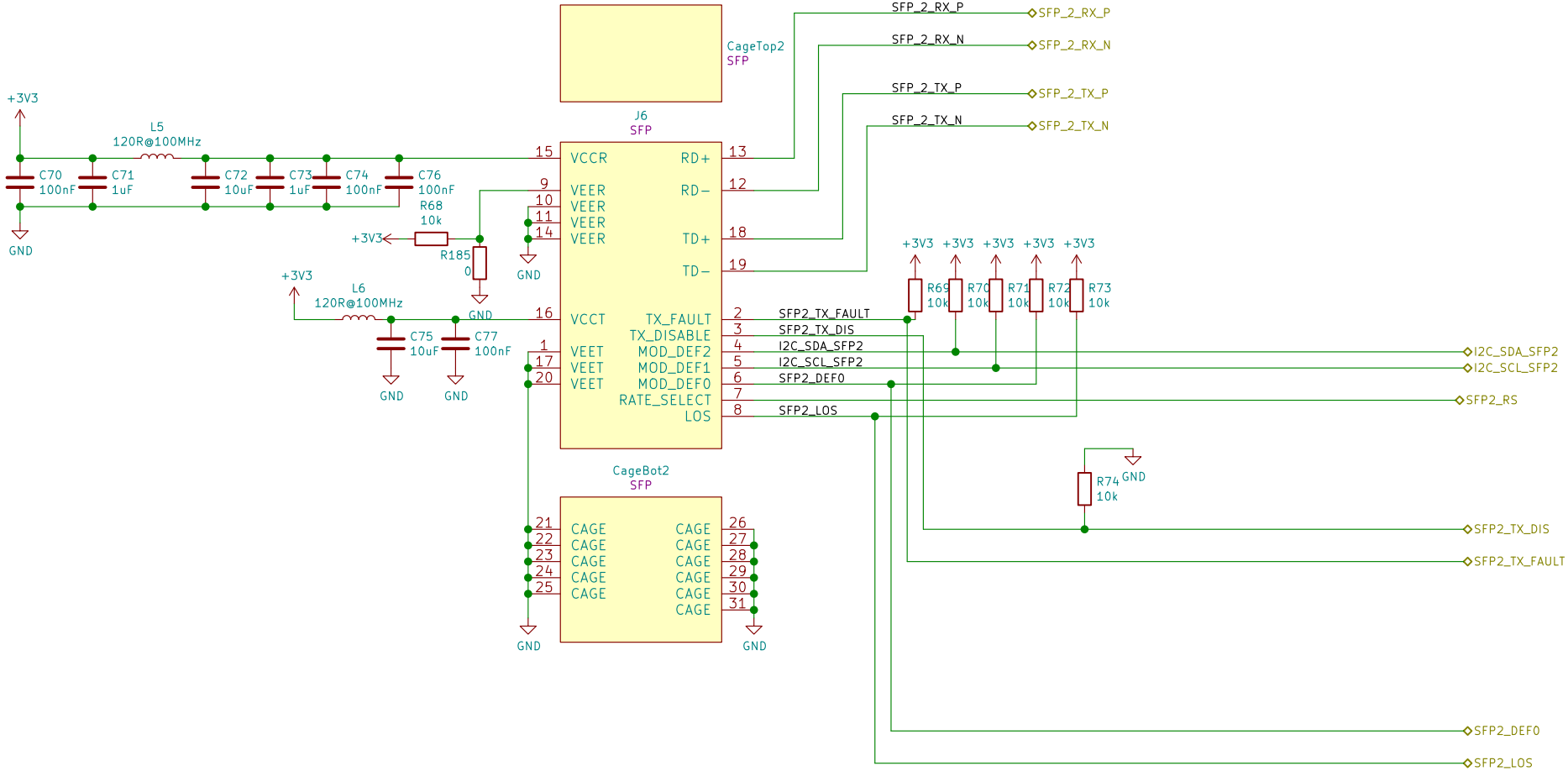
J5H

	h1	FMC1_VREF_A_M2C	
	h2	FMC1_PRSNT_M2C_L	
	h3		
FMC1_CLK0_M2C_P	h4		
FMC1_CLK0_M2C_N	h5		
	h6		
FMC1_P_LA_2	h7		
FMC1_N_LA_2	h8		
	h9		
FMC1_P_LA_4	h10		
FMC1_N_LA_4	h11		
	h12		
FMC1_P_LA_7	h13		
FMC1_N_LA_7	h14		
	h15		
FMC1_P_LA_11	h16		
FMC1_N_LA_11	h17		
	h18		
FMC1_P_LA_15	h19		
FMC1_N_LA_15	h20		
	h21		
FMC1_P_LA_19	h22		
FMC1_N_LA_19	h23		
	h24		
FMC1_P_LA_21	h25		
FMC1_N_LA_21	h26		
	h27		
FMC1_P_LA_24	h28		
FMC1_N_LA_24	h29		
	h30		
FMC1_P_LA_28	h31		
FMC1_N_LA_28	h32		
	h33		
FMC1_P_LA_30	h34		
FMC1_N_LA_30	h35		
	h36		
FMC1_P_LA_32	h37		
FMC1_N_LA_32	h38		
	h39		
	h40		

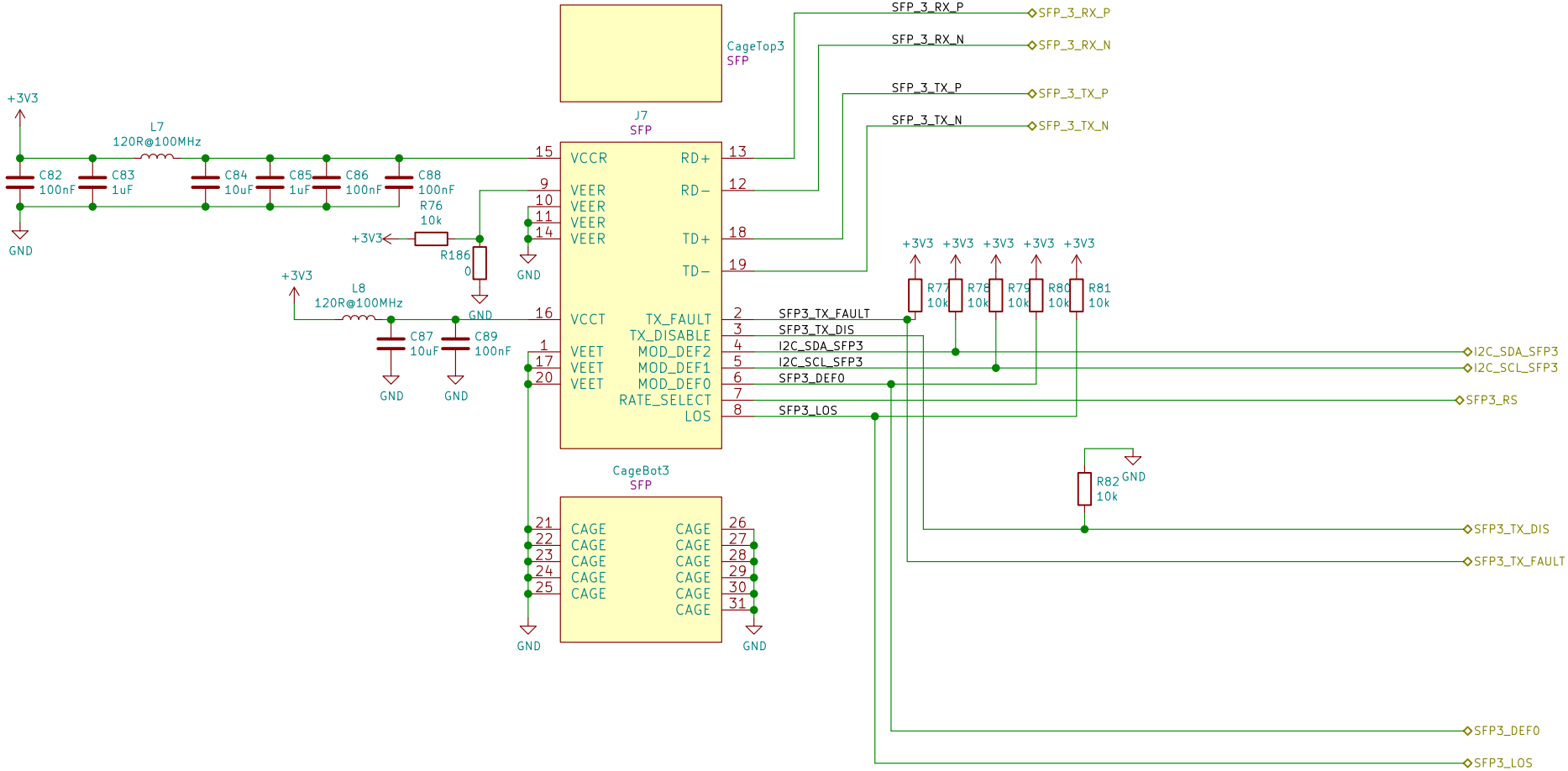
GND
GND

FMC1_3P3VAUX
F2
Fuse
+3V3MP
C65 100nF
C66 100nF
GND

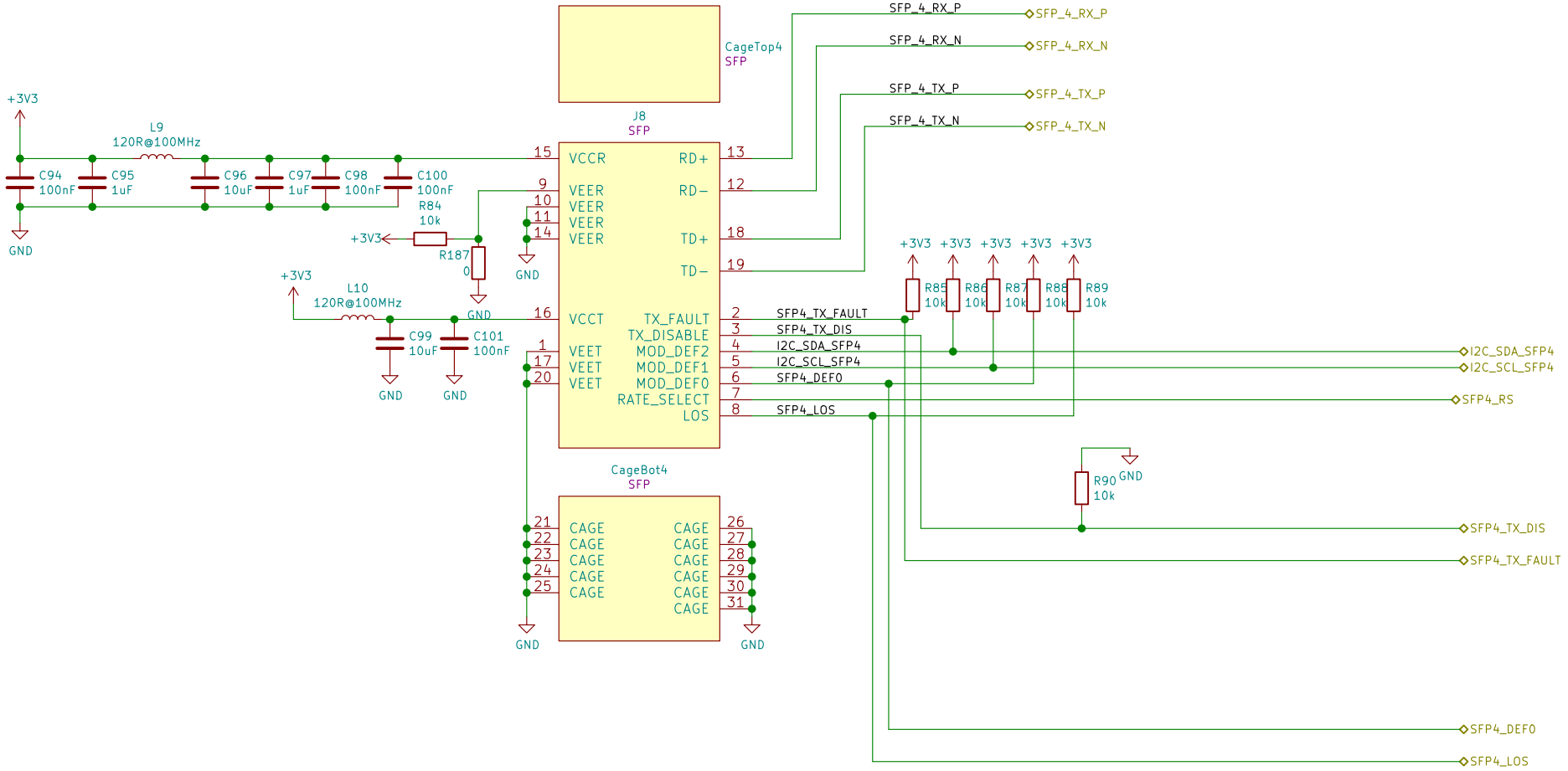
Michał Gąska / WUT
Sheet: /FMC_1/
File: FMC_1.sch
Title: Simple AFC
Size: A3 | Date: 2019-01-16 | **Rev: 9**
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69) | Id: 9/25



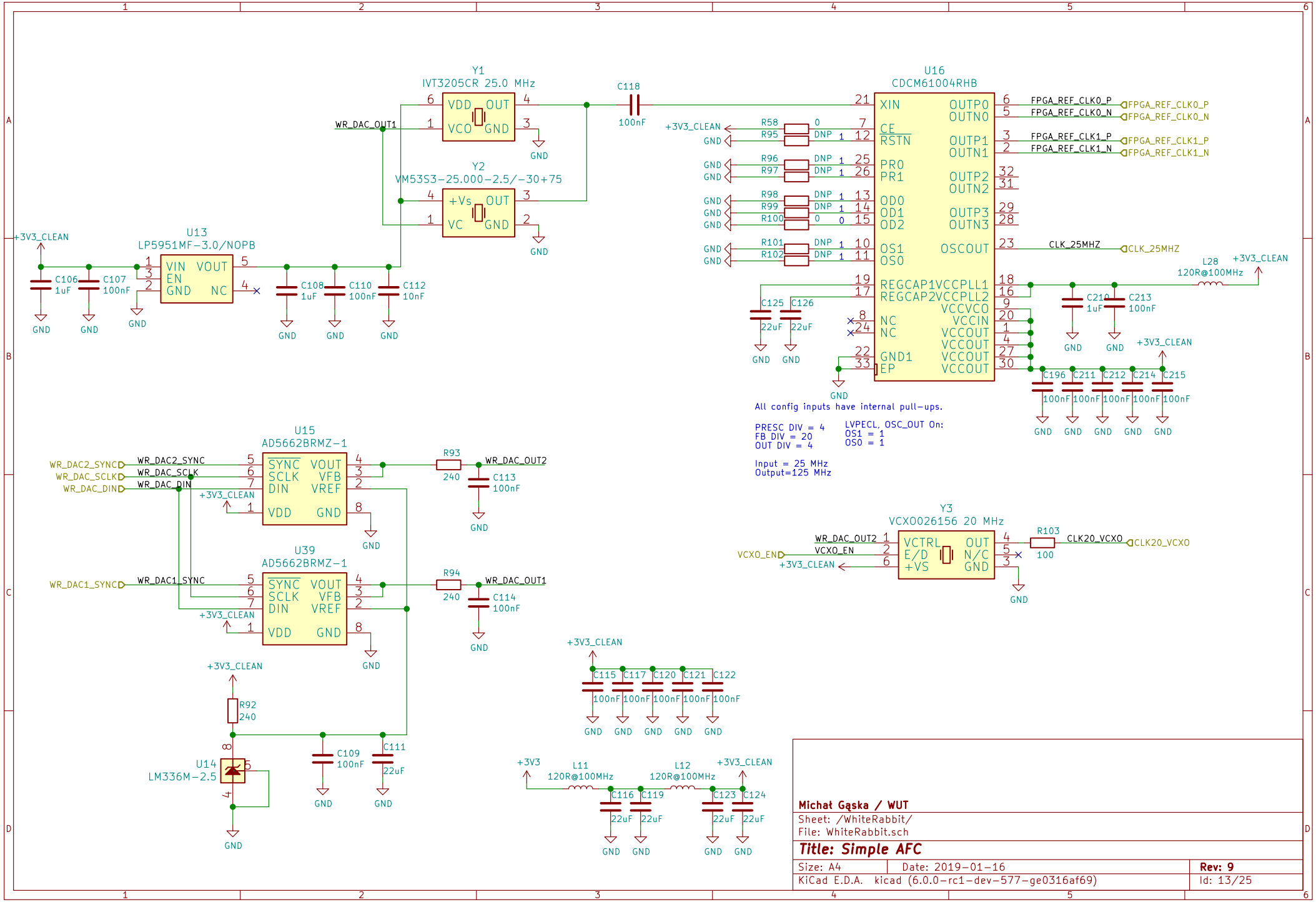
Michał Gąska / WUT		
Sheet: /SFP2/		
File: SFP2.sch		
Title: Simple AFC		
Size: A4	Date: 2019-01-16	**Rev: 9**
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)		Id: 10/25

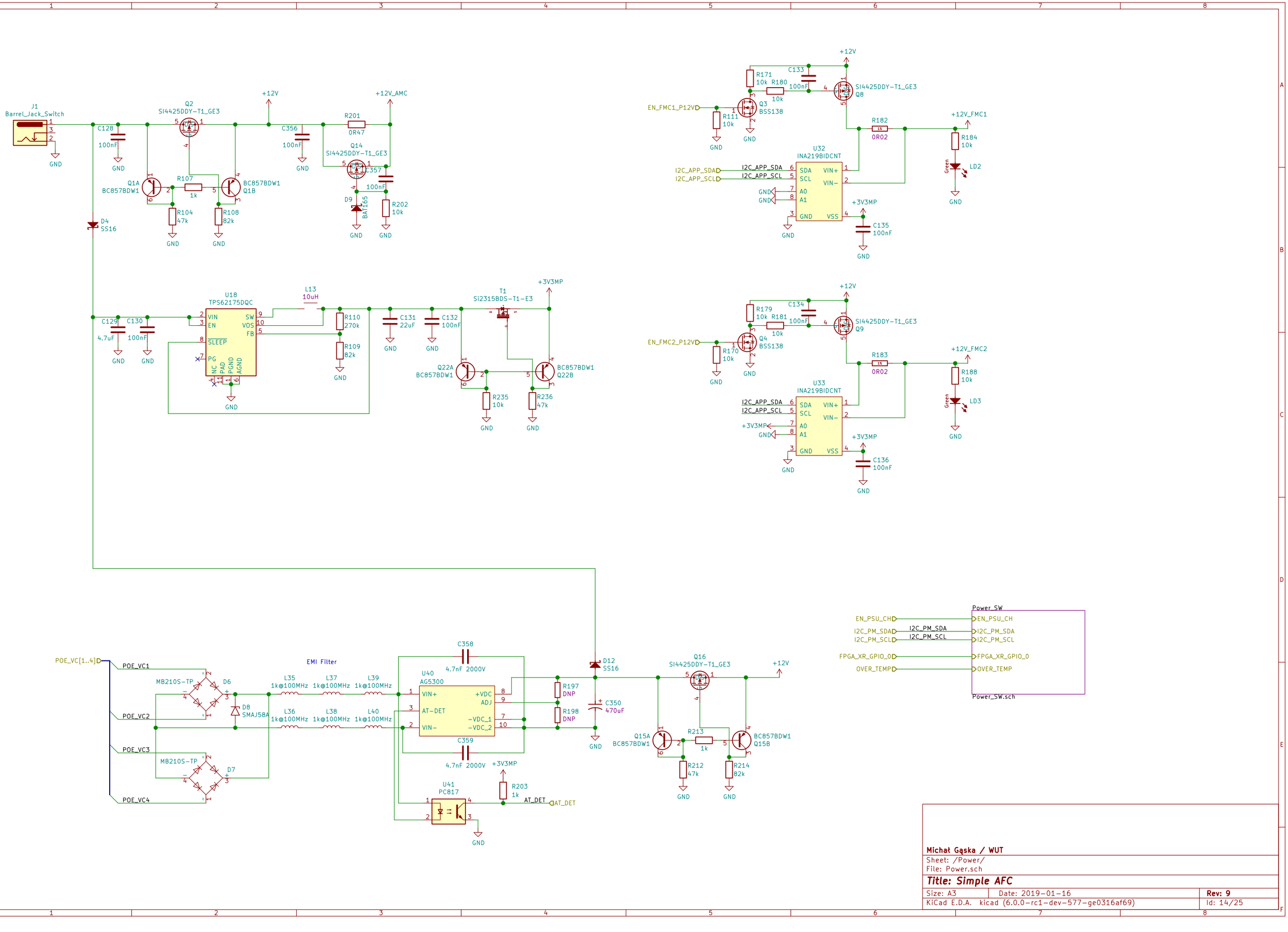


Michał Gąska / WUT		
Sheet: /SFP3/		
File: SFP3.sch		
Title: Simple AFC		
Size: A4	Date: 2019-01-16	**Rev: 9**
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)		Id: 11/25

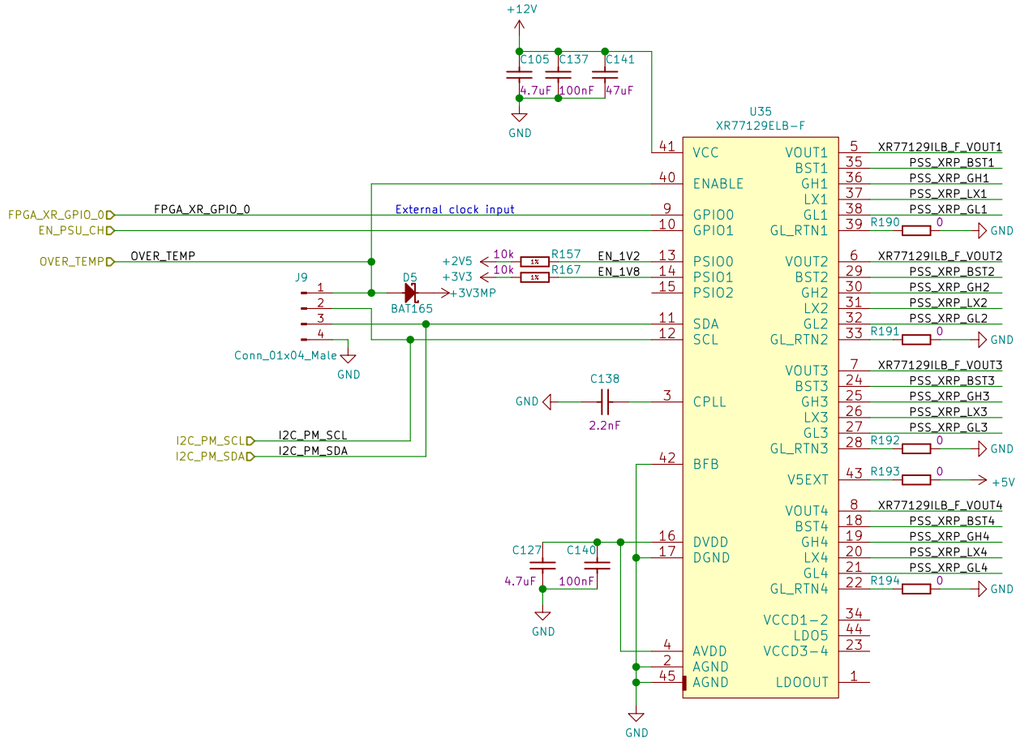


Michał Gąska / WUT		
Sheet: /SFP4/		
File: SFP4.sch		
Title: Simple AFC		
Size: A4	Date: 2019-01-16	**Rev: 9**
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)		Id: 12/25

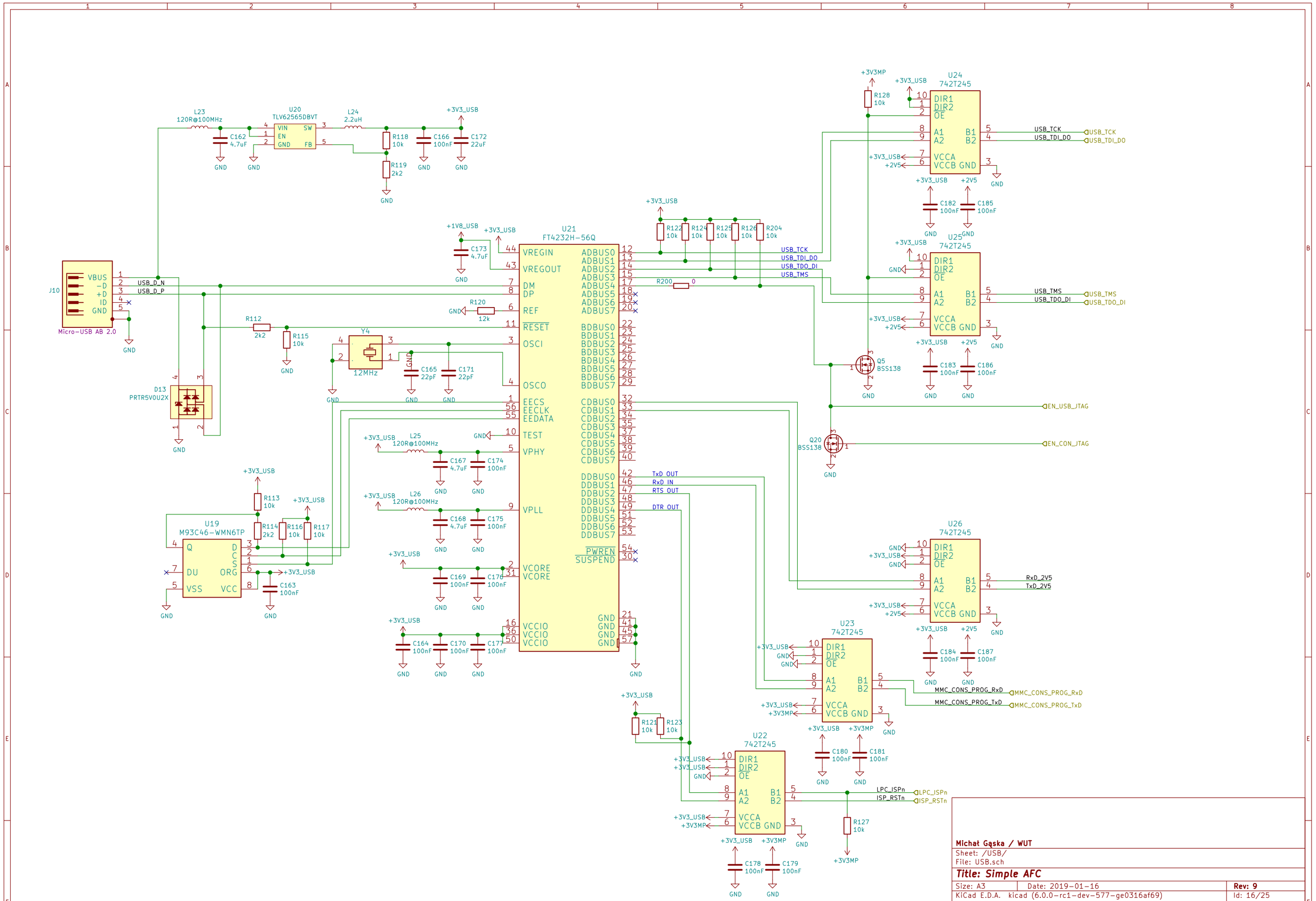

Y1
IVT3205CR 25.0 MHz
Y2
VM53S3-25.000-2.5/-30+75
C118
100nF
WR_DAC_OUT1
U16
CDCM61004RHB
XIN
CE
RSTN
PR0
PR1
OD0
OD1
OD2
OS1
OS0
REGCAP1
REGCAP2
NC
NC
GND1
EP
OUTP0
OUTN0
OUTP1
OUTN1
OUTP2
OUTN2
OUTP3
OUTN3
OSCOUT
VCCPLL1
VCCPLL2
VCCVCO
VCCIN
VCCOUT
VCCOUT
VCCOUT
VCCOUT
FPGA_REF_CLK0_P
FPGA_REF_CLK0_N
FPGA_REF_CLK1_P
FPGA_REF_CLK1_N
CLK_25MHZ
R58 0
R95 DNP
R96 DNP
R97 DNP
R98 DNP
R99 DNP
R100 0
R101 DNP
R102 DNP
C125 22uF
C126 22uF
C210 1uF
C213 100nF
L28 120R@100MHz
C196 C211 C212 C214 C215 100nF
All config inputs have internal pull-ups.
PRESC DIV = 4
FB DIV = 20
OUT DIV = 4
Input = 25 MHz
Output=125 MHz
LVPECL, OSC_OUT On:
OS1 = 1
OS0 = 1
U13
LP5951MF-3.0/NOPB
VIN
EN
GND
VOUT
NC
C106 1uF
C107 100nF
C108 1uF
C110 100nF
C112 10nF
U15
AD5662BRMZ-1
U39
AD5662BRMZ-1
SYNC
SCLK
DIN
VDD
VOUT
VFB
VREF
GND
WR_DAC2_SYNC
WR_DAC_SCLK
WR_DAC_DIN
WR_DAC1_SYNC
R93 240
R94 240
C113 100nF
C114 100nF
WR_DAC_OUT2
WR_DAC_OUT1
U14
LM336M-2.5
R92 240
C109 100nF
C111 22uF
Y3
VCXO026156 20 MHz
VCTRL
E/D
+VS
OUT
N/C
GND
WR_DAC_OUT2
VCXO_EN
R103 100
CLK20_VCXO
C115 C117 C120 C121 C122 100nF
L11 120R@100MHz
L12 120R@100MHz
C116 C119 22uF
C123 C124 22uF
+3V3_CLEAN
+3V3
GND
Michał Gąska / WUT
Sheet: /WhiteRabbit/
File: WhiteRabbit.sch
Title: Simple AFC
Size: A4
Date: 2019-01-16
Rev: 9
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)
Id: 13/25



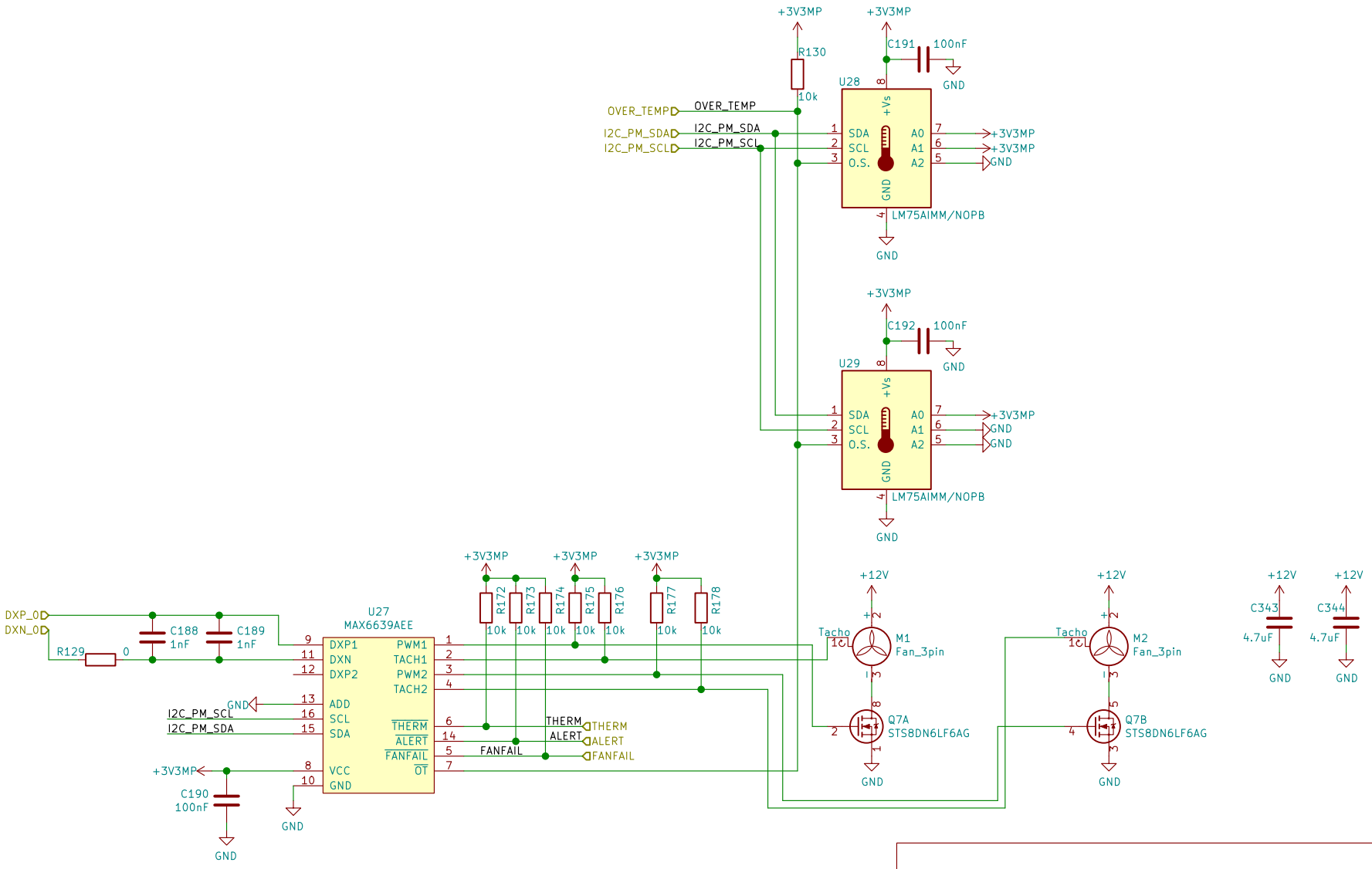
Michał Gąska / WUT	
Sheet: /Power/	
File: Power.sch	
Title: Simple AFC	
Size: A3	Date: 2019-01-16
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)	Rev: 9
	Id: 14/25



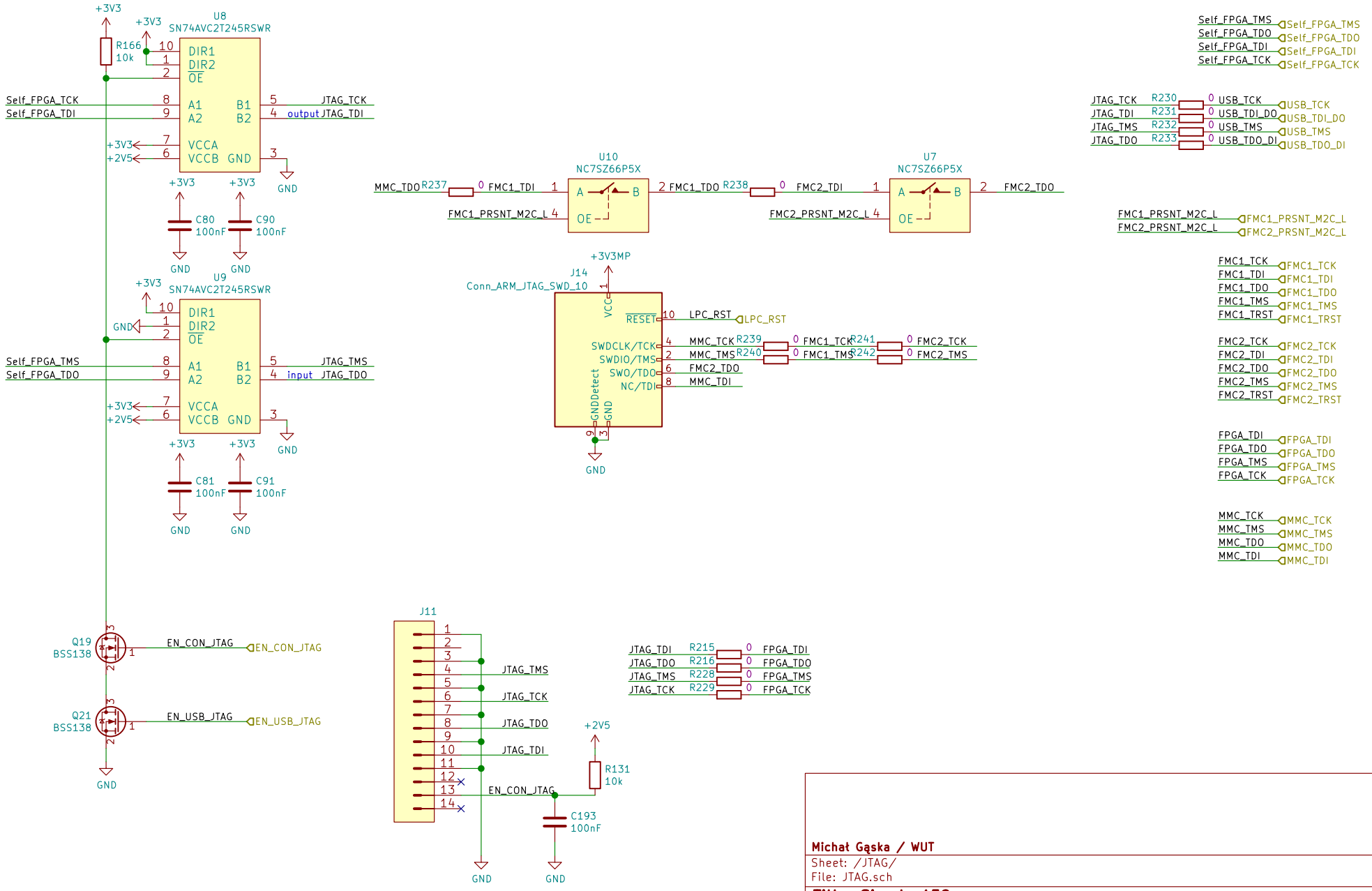
Michał Gąska / WUT	
Sheet: /Power/Power_SW/	
File: Power_SW.sch	
Title: Simple AFC	
Size: A3	Date: 2019-01-16
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)	Id: 15/25
	Rev: 9



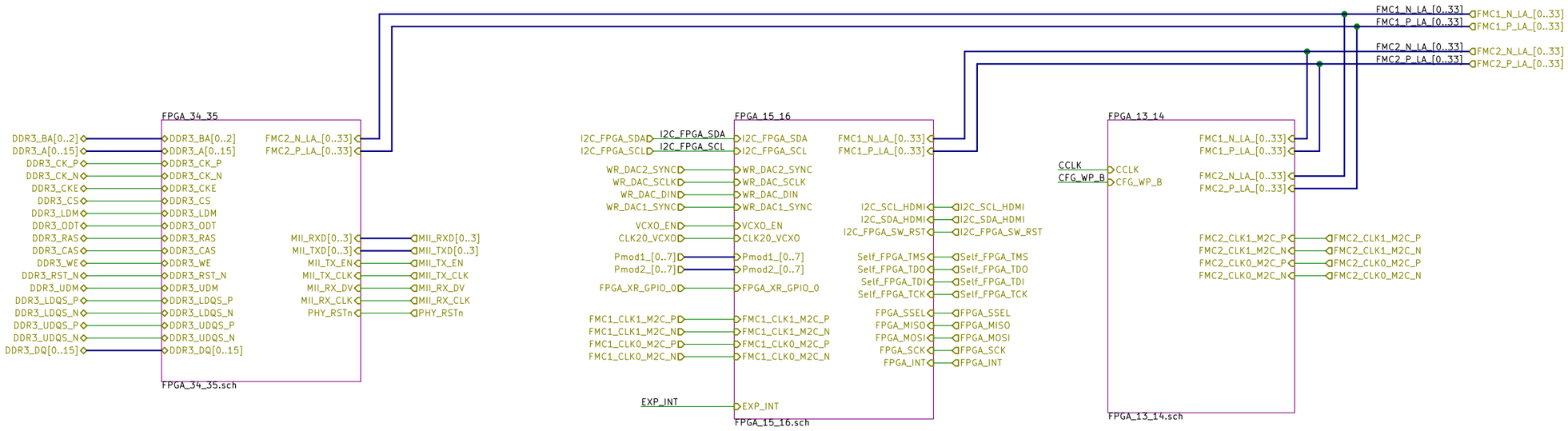
Michał Gąska / WUT			
Sheet: /USB/			
File: USB.sch			
Title: Simple AFC			
Size: A3	Date: 2019-01-16		**Rev: 9**
KiCad E.D.A.	kicad (6.0.0-rc1-dev-577-ge0316af69)		Id: 16/25

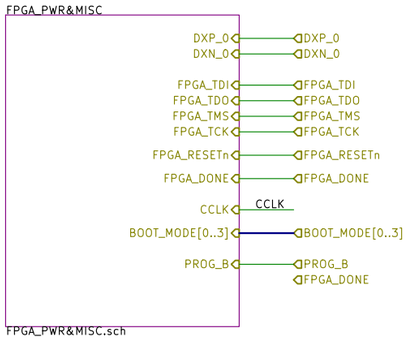


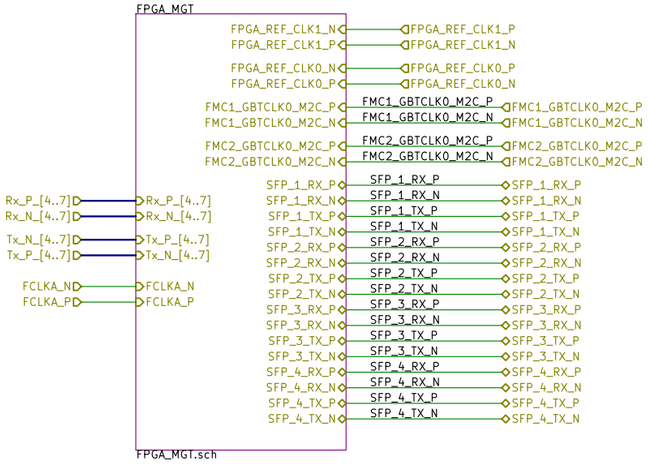
Michał Gąska / WUT	
Sheet: /Thermometers/	
File: Thermometers.sch	
Title: Simple AFC	
Size: A4	Date: 2019-01-16
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)	**Rev: 9**
	Id: 17/25

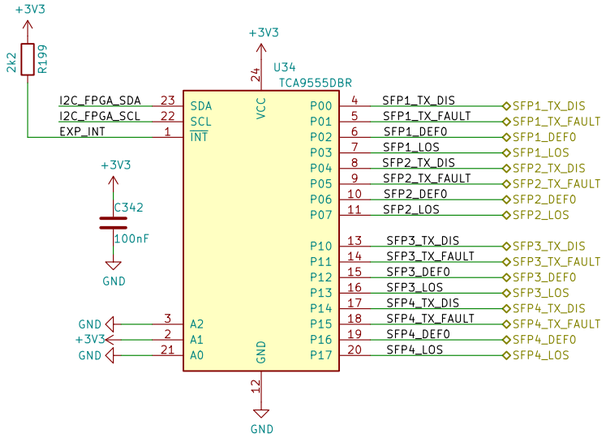


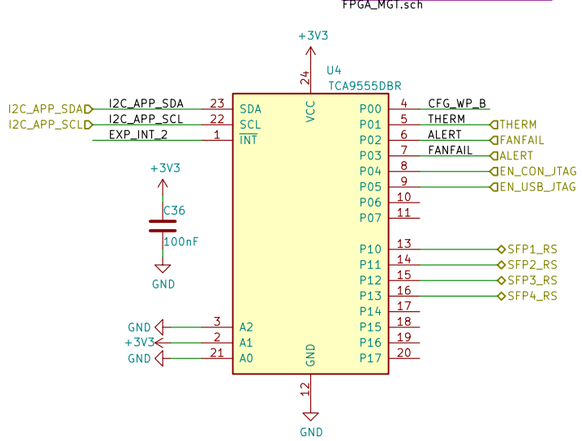
Michał Gąska / WUT	
Sheet: /JTAG/	
File: JTAG.sch	
Title: Simple AFC	
Size: A4	Date: 2019-01-16
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)	**Rev: 9**
	Id: 18/25











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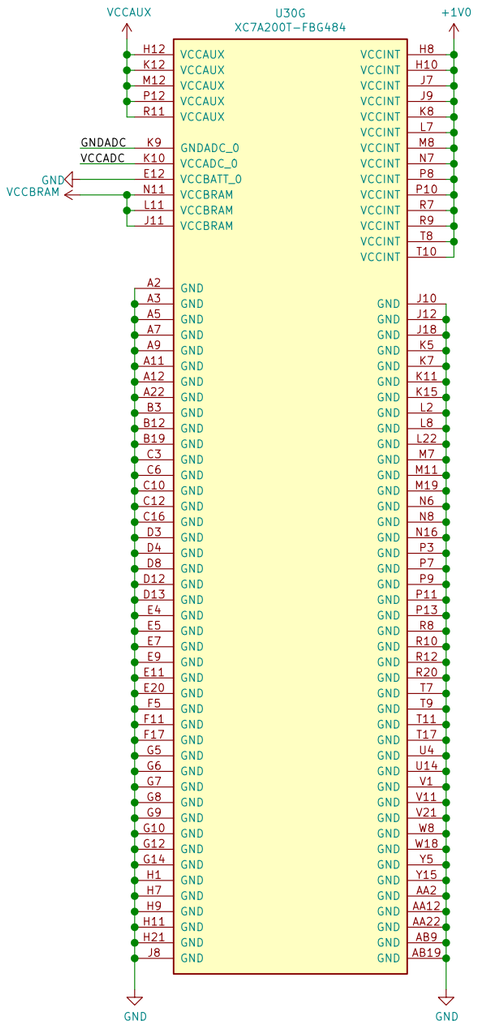
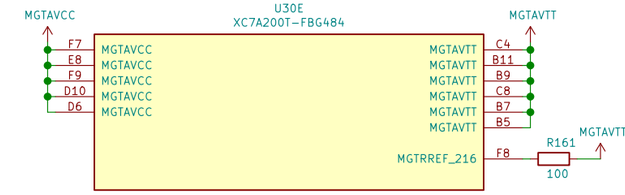
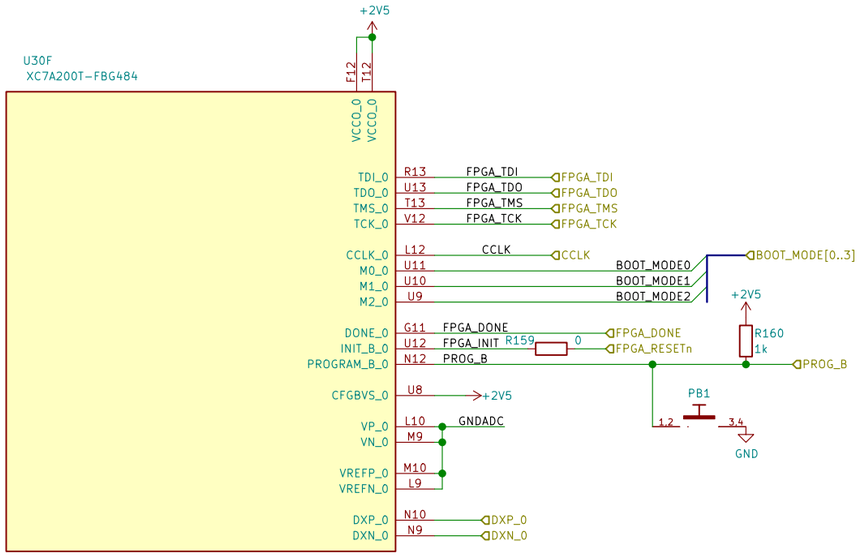
Sheet: /FPGA/
File: FPGA.sch

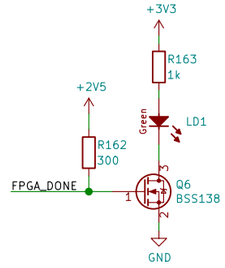
Title: Simple AFC

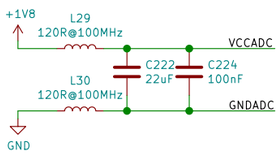
Size: A3	Date: 2019-01-16	**Rev: 9**
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)		Id: 19/25

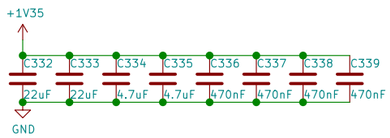


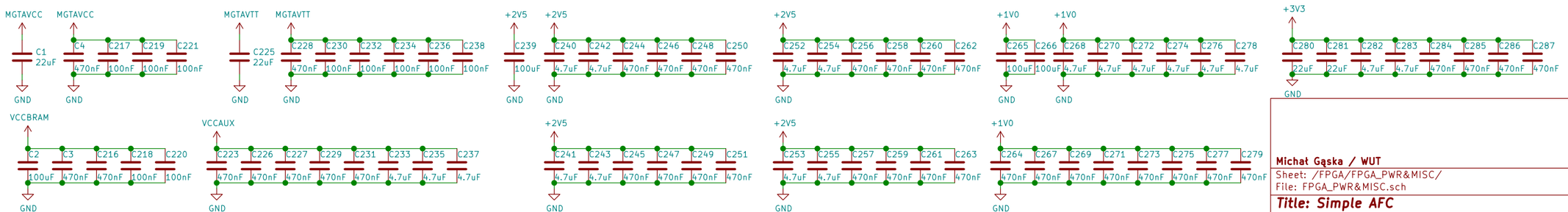












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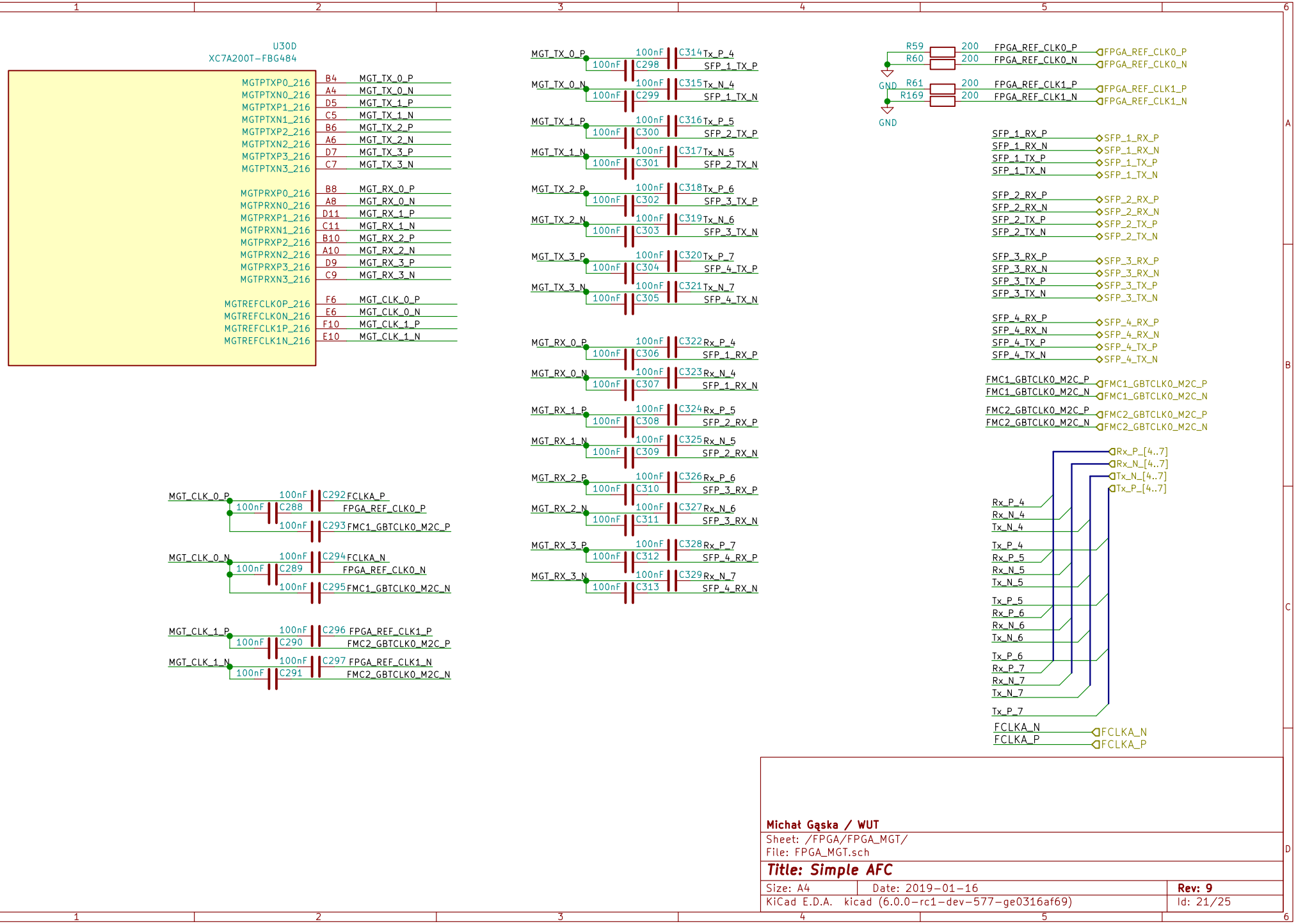
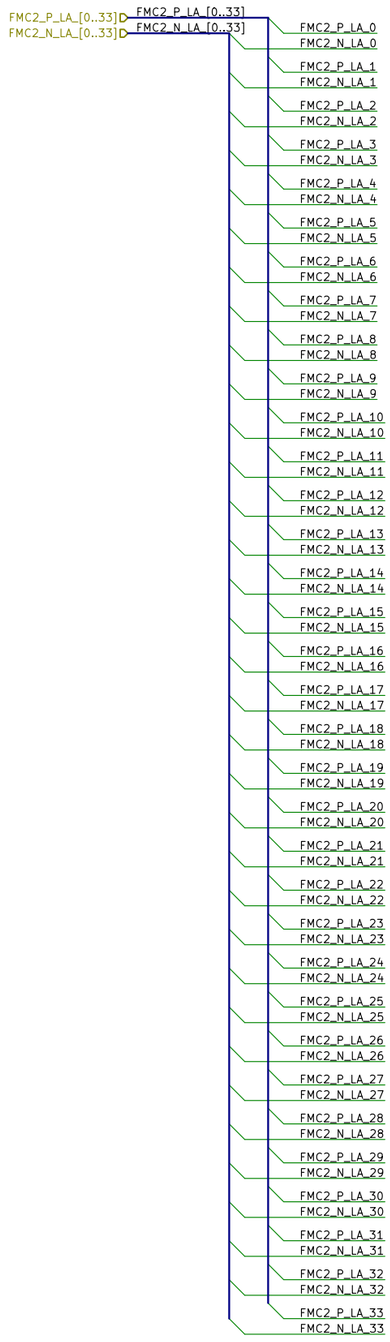
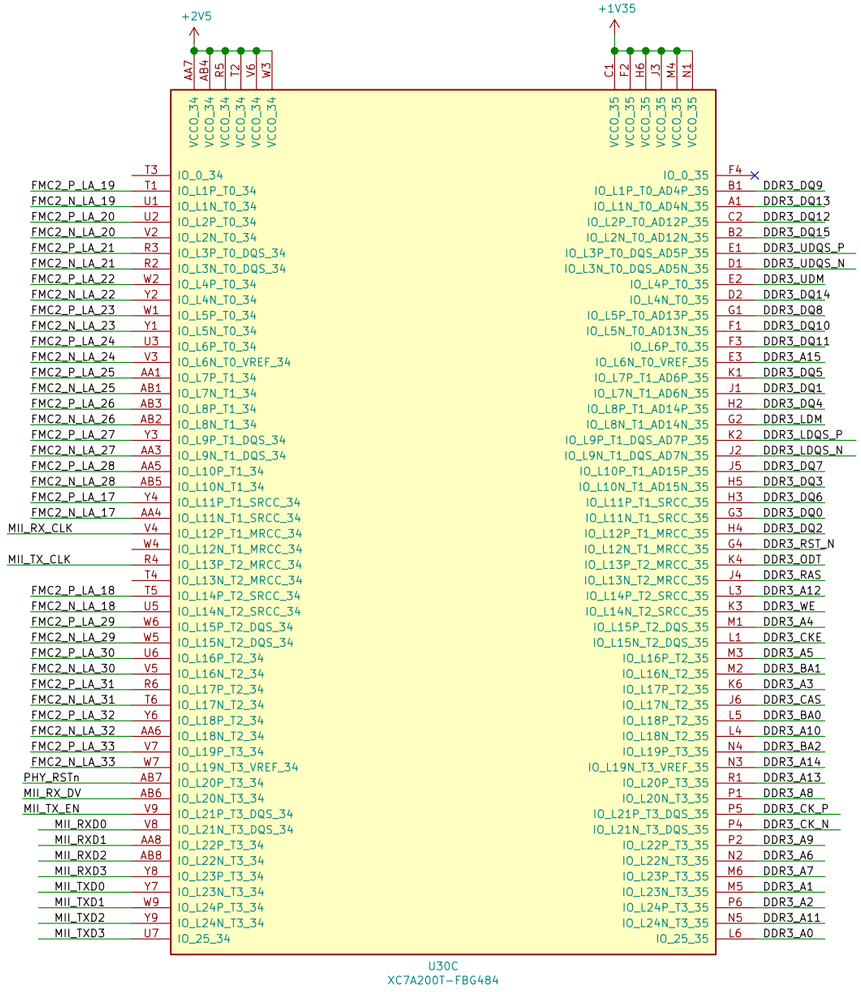
Sheet: /FPGA/FPGA_PWR&MISC/
File: FPGA_PWR&MISC.sch

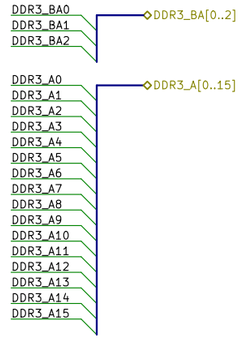
Title: Simple AFC

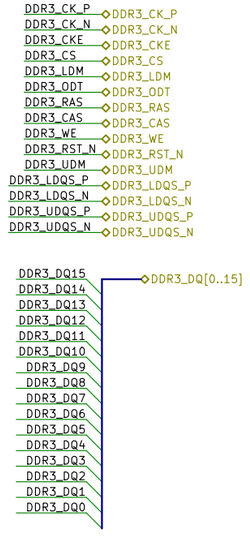
Size: A3	Date: 2019-01-16	**Rev: 9**
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)		Id: 20/25

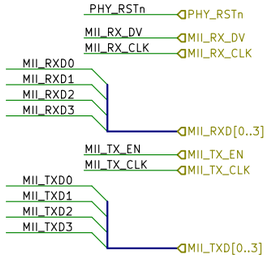

U30D
XC7A200T-FBG484
MGTPTXP0_216 B4 MGT_TX_0_P
MGTPTXN0_216 A4 MGT_TX_0_N
MGTPTXP1_216 D5 MGT_TX_1_P
MGTPTXN1_216 C5 MGT_TX_1_N
MGTPTXP2_216 B6 MGT_TX_2_P
MGTPTXN2_216 A6 MGT_TX_2_N
MGTPTXP3_216 D7 MGT_TX_3_P
MGTPTXN3_216 C7 MGT_TX_3_N
MGTPRXP0_216 B8 MGT_RX_0_P
MGTPRXN0_216 A8 MGT_RX_0_N
MGTPRXP1_216 D11 MGT_RX_1_P
MGTPRXN1_216 C11 MGT_RX_1_N
MGTPRXP2_216 B10 MGT_RX_2_P
MGTPRXN2_216 A10 MGT_RX_2_N
MGTPRXP3_216 D9 MGT_RX_3_P
MGTPRXN3_216 C9 MGT_RX_3_N
MGTREFCLK0P_216 F6 MGT_CLK_0_P
MGTREFCLK0N_216 E6 MGT_CLK_0_N
MGTREFCLK1P_216 F10 MGT_CLK_1_P
MGTREFCLK1N_216 E10 MGT_CLK_1_N
MGT_TX_0_P 100nF C314 Tx_P_4 SFP_1_TX_P
MGT_TX_0_N 100nF C315 Tx_N_4 SFP_1_TX_N
MGT_TX_1_P 100nF C316 Tx_P_5 SFP_2_TX_P
MGT_TX_1_N 100nF C317 Tx_N_5 SFP_2_TX_N
MGT_TX_2_P 100nF C318 Tx_P_6 SFP_3_TX_P
MGT_TX_2_N 100nF C319 Tx_N_6 SFP_3_TX_N
MGT_TX_3_P 100nF C320 Tx_P_7 SFP_4_TX_P
MGT_TX_3_N 100nF C321 Tx_N_7 SFP_4_TX_N
MGT_RX_0_P 100nF C322 Rx_P_4 SFP_1_RX_P
MGT_RX_0_N 100nF C323 Rx_N_4 SFP_1_RX_N
MGT_RX_1_P 100nF C324 Rx_P_5 SFP_2_RX_P
MGT_RX_1_N 100nF C325 Rx_N_5 SFP_2_RX_N
MGT_RX_2_P 100nF C326 Rx_P_6 SFP_3_RX_P
MGT_RX_2_N 100nF C327 Rx_N_6 SFP_3_RX_N
MGT_RX_3_P 100nF C328 Rx_P_7 SFP_4_RX_P
MGT_RX_3_N 100nF C329 Rx_N_7 SFP_4_RX_N
MGT_CLK_0_P 100nF C292 FCLKA_P
100nF C288 FPGA_REF_CLK0_P
100nF C293 FMC1_GBTCLK0_M2C_P
MGT_CLK_0_N 100nF C294 FCLKA_N
100nF C289 FPGA_REF_CLK0_N
100nF C295 FMC1_GBTCLK0_M2C_N
MGT_CLK_1_P 100nF C296 FPGA_REF_CLK1_P
100nF C290 FMC2_GBTCLK0_M2C_P
MGT_CLK_1_N 100nF C297 FPGA_REF_CLK1_N
100nF C291 FMC2_GBTCLK0_M2C_N
R59 200 FPGA_REF_CLK0_P FPGA_REF_CLK0_P
R60 200 FPGA_REF_CLK0_N FPGA_REF_CLK0_N
GND
R61 200 FPGA_REF_CLK1_P FPGA_REF_CLK1_P
R169 200 FPGA_REF_CLK1_N FPGA_REF_CLK1_N
GND
SFP_1_RX_P SFP_1_RX_P
SFP_1_RX_N SFP_1_RX_N
SFP_1_TX_P SFP_1_TX_P
SFP_1_TX_N SFP_1_TX_N
SFP_2_RX_P SFP_2_RX_P
SFP_2_RX_N SFP_2_RX_N
SFP_2_TX_P SFP_2_TX_P
SFP_2_TX_N SFP_2_TX_N
SFP_3_RX_P SFP_3_RX_P
SFP_3_RX_N SFP_3_RX_N
SFP_3_TX_P SFP_3_TX_P
SFP_3_TX_N SFP_3_TX_N
SFP_4_RX_P SFP_4_RX_P
SFP_4_RX_N SFP_4_RX_N
SFP_4_TX_P SFP_4_TX_P
SFP_4_TX_N SFP_4_TX_N
FMC1_GBTCLK0_M2C_P FMC1_GBTCLK0_M2C_P
FMC1_GBTCLK0_M2C_N FMC1_GBTCLK0_M2C_N
FMC2_GBTCLK0_M2C_P FMC2_GBTCLK0_M2C_P
FMC2_GBTCLK0_M2C_N FMC2_GBTCLK0_M2C_N
Rx_P_[4..7]
Rx_N_[4..7]
Tx_N_[4..7]
Tx_P_[4..7]
Rx_P_4
Rx_N_4
Tx_N_4
Tx_P_4
Rx_P_5
Rx_N_5
Tx_N_5
Tx_P_5
Rx_P_6
Rx_N_6
Tx_N_6
Tx_P_6
Rx_P_7
Rx_N_7
Tx_N_7
Tx_P_7
FCLKA_N FCLKA_N
FCLKA_P FCLKA_P
Michał Gąska / WUT
Sheet: /FPGA/FPGA_MGT/
File: FPGA_MGT.sch
Title: Simple AFC
Size: A4
Date: 2019-01-16
Rev: 9
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)
Id: 21/25











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Sheet: /FPGA/FPGA_34_35/

File: FPGA_34_35.sch

Title: Simple AFC

Size: A3	Date: 2019-01-16	**Rev: 9**
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)		Id: 22/25

FMC1_P_LA_[0..33]
FMC1_N_LA_[0..33]
FMC1_P_LA[0..33]
FMC1_N_LA[0..33]
FMC1_P_LA_0
FMC1_N_LA_0
FMC1_P_LA_1
FMC1_N_LA_1
FMC1_P_LA_2
FMC1_N_LA_2
FMC1_P_LA_3
FMC1_N_LA_3
FMC1_P_LA_4
FMC1_N_LA_4
FMC1_P_LA_5
FMC1_N_LA_5
FMC1_P_LA_6
FMC1_N_LA_6
FMC1_P_LA_7
FMC1_N_LA_7
FMC1_P_LA_8
FMC1_N_LA_8
FMC1_P_LA_9
FMC1_N_LA_9
FMC1_P_LA_10
FMC1_N_LA_10
FMC1_P_LA_11
FMC1_N_LA_11
FMC1_P_LA_12
FMC1_N_LA_12
FMC1_P_LA_13
FMC1_N_LA_13
FMC1_P_LA_14
FMC1_N_LA_14
FMC1_P_LA_15
FMC1_N_LA_15
FMC1_P_LA_16
FMC1_N_LA_16
FMC1_P_LA_17
FMC1_N_LA_17
FMC1_P_LA_18
FMC1_N_LA_18
FMC1_P_LA_19
FMC1_N_LA_19
FMC1_P_LA_20
FMC1_N_LA_20
FMC1_P_LA_21
FMC1_N_LA_21
FMC1_P_LA_22
FMC1_N_LA_22
FMC1_P_LA_23
FMC1_N_LA_23
FMC1_P_LA_24
FMC1_N_LA_24
FMC1_P_LA_25
FMC1_N_LA_25
FMC1_P_LA_26
FMC1_N_LA_26
FMC1_P_LA_27
FMC1_N_LA_27
FMC1_P_LA_28
FMC1_N_LA_28
FMC1_P_LA_29
FMC1_N_LA_29
FMC1_P_LA_30
FMC1_N_LA_30
FMC1_P_LA_31
FMC1_N_LA_31
FMC1_P_LA_32
FMC1_N_LA_32
FMC1_P_LA_33
FMC1_N_LA_33

+2V5
G19 H16 J13 K20 L17 N21
VCCO_15 VCCO_15 VCCO_15 VCCO_15 VCCO_15 VCCO_15

+3V3
A17 B14 C21 D18 E15 F22
VCCO_16 VCCO_16 VCCO_16 VCCO_16 VCCO_16 VCCO_16

J16 IO_0_15
FMC1_P_LA_2 H13 IO_L1P_T0_AD0P_15
FMC1_N_LA_2 G13 IO_L1N_T0_AD0N_15
FMC1_P_LA_3 G15 IO_L2P_T0_AD8P_15
FMC1_N_LA_3 G16 IO_L2N_T0_AD8N_15
FMC1_P_LA_4 J14 IO_L3P_T0_DQS_AD1P_15
FMC1_N_LA_4 H14 IO_L3N_T0_DQS_AD1N_15
FMC1_P_LA_5 G17 IO_L4P_T0_15
FMC1_N_LA_5 G18 IO_L4N_T0_15
FMC1_P_LA_6 J15 IO_L5P_T0_AD9P_15
FMC1_N_LA_6 H15 IO_L5N_T0_AD9N_15
FMC1_P_LA_7 H17 IO_L6P_T0_15
FMC1_N_LA_7 H18 IO_L6N_T0_VREF_15
FMC1_P_LA_8 J22 IO_L7P_T1_AD2P_15
FMC1_N_LA_8 H22 IO_L7N_T1_AD2N_15
FMC1_P_LA_9 H20 IO_L8P_T1_AD10P_15
FMC1_N_LA_9 G20 IO_L8N_T1_AD10N_15
FMC1_P_LA_10 K21 IO_L9P_T1_DQS_AD3P_15
FMC1_N_LA_10 K22 IO_L9N_T1_DQS_AD3N_15
FMC1_P_LA_11 M21 IO_L10P_T1_AD11P_15
FMC1_N_LA_11 L21 IO_L10N_T1_AD11N_15
FMC1_P_LA_0 J20 IO_L11P_T1_SRCC_15
FMC1_N_LA_0 J21 IO_L11N_T1_SRCC_15
FMC1_CLK1_M2C_P J19 IO_L12P_T1_MRCC_15
FMC1_CLK1_M2C_N H19 IO_L12N_T1_MRCC_15
FMC1_CLK0_M2C_P K18 IO_L13P_T2_MRCC_15
FMC1_CLK0_M2C_N K19 IO_L13N_T2_MRCC_15
FMC1_P_LA_1 L19 IO_L14P_T2_SRCC_15
FMC1_N_LA_1 L20 IO_L14N_T2_SRCC_15
FMC1_P_LA_13 N22 IO_L15P_T2_DQS_15
FMC1_N_LA_13 M22 IO_L15N_T2_DQS_ADV_B_15
FMC1_P_LA_14 M18 IO_L16P_T2_A28_15
FMC1_N_LA_14 L18 IO_L16N_T2_A27_15
FMC1_P_LA_15 N18 IO_L17P_T2_A26_15
FMC1_N_LA_15 N19 IO_L17N_T2_A25_15
FMC1_P_LA_16 N20 IO_L18P_T2_A24_15
FMC1_N_LA_16 M20 IO_L18N_T2_A23_15
K13 IO_L19P_T3_A22_15
K14 IO_L19N_T3_A21_VREF_15
FMC1_P_LA_12 M13 IO_L20P_T3_A20_15
FMC1_N_LA_12 L13 IO_L20N_T3_A19_15
K17 IO_L21P_T3_DQS_15
J17 IO_L21N_T3_DQS_A18_15
L14 IO_L22P_T3_A17_15
L15 IO_L22N_T3_A16_15
L16 IO_L23P_T3_FOE_B_15
K16 IO_L23N_T3_FWE_B_15
M15 IO_L24P_T3_RS1_15
M16 IO_L24N_T3_RS0_15
M17 IO_25_15

F15 IO_0_16 FPGA_MOSI
F13 IO_L1P_T0_16 FPGA_MISO
F14 IO_L1N_T0_16 FPGA_SSEL
F16 IO_L2P_T0_16 FPGA_SCK
E17 IO_L2N_T0_16 FPGA_INT
C14 IO_L3P_T0_DQS_16 Self_FPGA_TMS
C15 IO_L3N_T0_DQS_16 Self_FPGA_TDO
E13 IO_L4P_T0_16 Self_FPGA_TDI
E14 IO_L4N_T0_16 Self_FPGA_TCK
E16 IO_L5P_T0_16 TMDS2_P
D16 IO_L5N_T0_16 TMDS2_N
D14 IO_L6P_T0_16 TMDS1_P
D15 IO_L6N_T0_VREF_16 TMDS1_N
B15 IO_L7P_T1_16 TMDS0_P
B16 IO_L7N_T1_16 TMDS0_N
C13 IO_L8P_T1_16
B13 IO_L8N_T1_16 I2C_FPGA_SCL
A15 IO_L9P_T1_DQS_16 I2C_FPGA_SDA
A16 IO_L9N_T1_DQS_16 WR_DAC2_SYNC
A13 IO_L10P_T1_16 WR_DAC_SCLK
A14 IO_L10N_T1_16 WR_DAC_DIN
B17 IO_L11P_T1_SRCC_16 WR_DAC1_SYNC
B18 IO_L11N_T1_SRCC_16 Pmod1_0
D17 IO_L12P_T1_MRCC_16 CLK20_VCXO
C17 IO_L12N_T1_MRCC_16
C18 IO_L13P_T2_MRCC_16 TMDS_CLK_P
C19 IO_L13N_T2_MRCC_16 TMDS_CLK_N
E19 IO_L14P_T2_SRCC_16 Pmod1_4
D19 IO_L14N_T2_SRCC_16 Pmod1_5
F18 IO_L15P_T2_DQS_16 Pmod1_6
E18 IO_L15N_T2_DQS_16 Pmod1_7
B20 IO_L16P_T2_16 Pmod2_0
A20 IO_L16N_T2_16 Pmod2_1
A18 IO_L17P_T2_16 Pmod2_2
A19 IO_L17N_T2_16 Pmod2_3
F19 IO_L18P_T2_16 Pmod2_4
F20 IO_L18N_T2_16 Pmod2_5
D20 IO_L19P_T3_16 Pmod2_6
C20 IO_L19N_T3_VREF_16 Pmod2_7
C22 IO_L20P_T3_16 FPGA_XR_GPIO_0
B22 IO_L20N_T3_16 I2C_FPGA_SW_RST
B21 IO_L21P_T3_DQS_16 Pmod1_1
A21 IO_L21N_T3_DQS_16 VCXO_EN
E22 IO_L22P_T3_16 EXP_INT
D22 IO_L22N_T3_16 Pmod1_2
E21 IO_L23P_T3_16 Pmod1_3
D21 IO_L23N_T3_16
G21 IO_L24P_T3_16
G22 IO_L24N_T3_16
F21 IO_25_16

U30B
XC7A200T-FBG484

Self_FPGA_TMS Self_FPGA_TMS
Self_FPGA_TDO Self_FPGA_TDO
Self_FPGA_TDI Self_FPGA_TDI
Self_FPGA_TCK Self_FPGA_TCK
I2C_FPGA_SW_RST I2C_FPGA_SW_RST
FPGA_INT FPGA_INT
FPGA_MOSI FPGA_MOSI
FPGA_MISO FPGA_MISO
FPGA_SSEL FPGA_SSEL
FPGA_SCK FPGA_SCK
EXP_INT EXP_INT
I2C_FPGA_SCL I2C_FPGA_SCL
I2C_FPGA_SDA I2C_FPGA_SDA
WR_DAC2_SYNC WR_DAC2_SYNC
WR_DAC_SCLK WR_DAC_SCLK
WR_DAC_DIN WR_DAC_DIN
WR_DAC1_SYNC WR_DAC1_SYNC
VCXO_EN VCXO_EN
CLK20_VCXO CLK20_VCXO

Pmod2_[0..7] Pmod2_[0..7]
Pmod1_[0..7] Pmod1_[0..7]
Pmod2_0 Pmod1_0
Pmod2_1 Pmod1_1
Pmod2_2 Pmod1_2
Pmod2_3 Pmod1_3
Pmod2_4 Pmod1_4
Pmod2_5 Pmod1_5
Pmod2_6 Pmod1_6
Pmod2_7 Pmod1_7

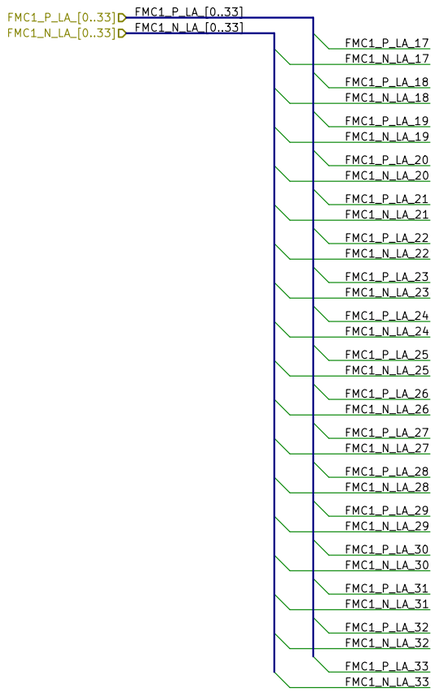
FPGA_XR_GPIO_0 FPGA_XR_GPIO_0

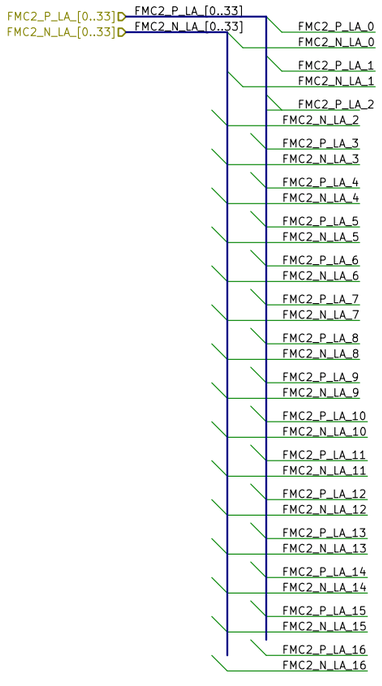
+3V3
49R9 R217 49R9 R218 49R9 R219 49R9 R220 49R9 R221 49R9 R222 49R9 R225 49R9 R226
D10
HDMIULC6-4SC6
D11
HDMIULC6-4SC6
GND
TMDS2_P
TMDS2_N
TMDS1_P
TMDS1_N
TMDS0_P
TMDS0_N
TMDS_CLK_P
TMDS_CLK_N
J15
SHIELD

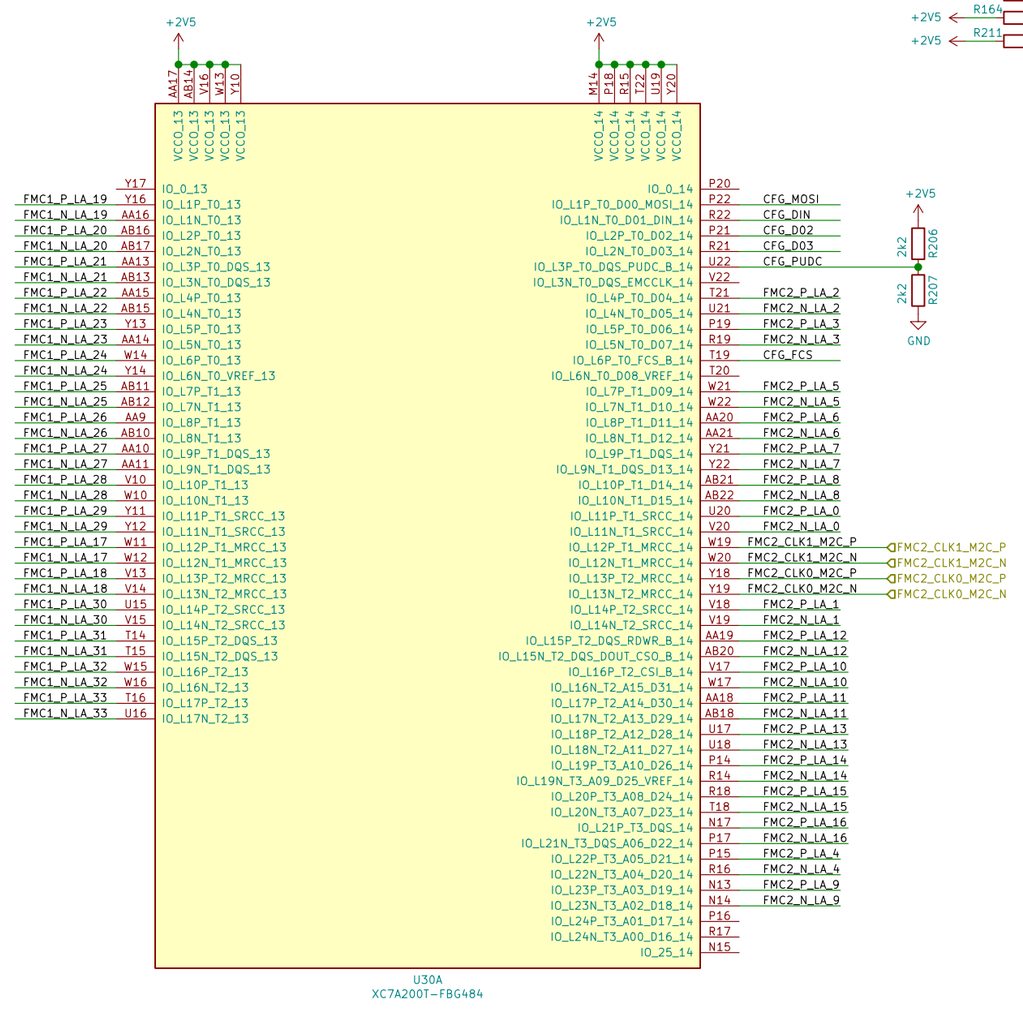
+3V3
Q17
BSS138
I2C_SCL_HDMI
HDMI_5V
R223 2k2
Q18
BSS138
I2C_SDA_HDMI
HDMI_5V
R224 2k2
HDMI_5V
C37 100nF
R227 2k2
HDMI_HPD
GND

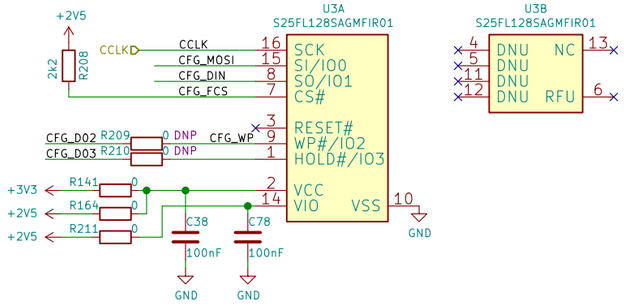
U12
MC78L05ACDR2G
+12V
VIN VOUT
NC NC
GND GND
GND GND
C103 4.7uF
C104 4.7uF
HDMI_5V
GND

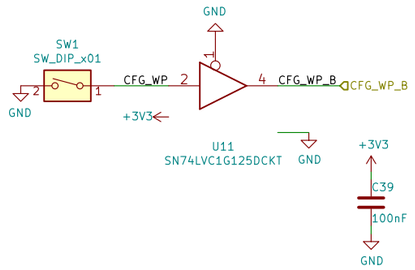
Michał Gąska / WUT
Sheet: /FPGA/FPGA_15_16/
File: FPGA_15_16.sch
Title: Simple AFC
Size: A3 | Date: 2019-01-16 | Rev: 9
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69) | Id: 23/25











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Sheet: /FPGA/FPGA_13_14/

File: FPGA_13_14.sch

Title: Simple AFC

Size: A3	Date: 2019-01-16	**Rev: 9**
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69)		Id: 24/25

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I2C_PM_SDA	M10	P0[0]/CAN_RD1/U3_TXD/I2C1_SDA/U0_TXD
I2C_PM_SCL	N11	P0[1]/CAN_TD1/U3_RXD/I2C1_SCL/U0_RXD
MMC_CONS_PROG_TxD	D5	P0[2]/U0_TXD/U3_TXD
MMC_CONS_PROG_RxD	A3	P0[3]/U0_RXD/U3_RXD
	A11	P0[4]/I2S_RX_SCK/CAN_RD2/T2_CAP0
	B11	P0[5]/I2S_RX_WS/CAN_TD2/T2_CAP1
	D11	P0[6]/I2S_RX_SDA/SSP1_SSEL/T2_MAT0/U1_RTS
PROG_B	B12	P0[7]/I2S_TX_SCK/SSP1_SCK/T2_MAT1/RTC_EV0
FPGA_DONE	C12	P0[8]/I2S_TX_WS/SSP1_MISO/T2_MAT2/RTC_EV1
	A13	P0[9]/I2S_TX_SDA/SSP1_MOSI/T2_MAT3/RTC_EV2
I2C_FPGA_SDA (R135 0)	L10	P0[10]/U2_TXD/I2C2_SDA/T3_MAT0
I2C_FPGA_SCL (R136 0)	P12	P0[11]/U2_RXD/I2C2_SCL/T3_MAT1
EN_FLASH_UPDATE	J4	P0[12]/USB_PPWR2/SSP1_MISO/ADC0_IN[6]
MMC_FPGA_INIT_B	J5	P0[13]/USB_UP_LED2/SSP1_MOSI/ADC0_IN[7]
FPGA_STATUS	M5	P0[14]/USB_HSTEN2/SSP1_SSEL/USB_CONNECT2
FPGA_SCK	H13	P0[15]/U1_TXD/SSP0_SCK
FPGA_SSEL	H14	P0[16]/U1_RXD/SSP0_SSEL
FPGA_MISO	J12	P0[17]/U1_CTS/SSP0_MISO
FPGA_MOSI	J13	P0[18]/U1_DCD/SSP0_MOSI
FPGA_INT	J10	P0[19]/U1_DSR/SD_CLK/I2C1_SDA
	K14	P0[20]/U1_DTR/SD_CMD/I2C1_SCL
	K11	P0[21]/U1_RI/SD_PWR/U4_OE/CAN_RD1/U4_SCLK
	L14	P0[22]/U1_RTS/SD_DAT[0]/U4_TXD/CAN_TD1
	F5	P0[23]/ADC0_IN[0]/I2S_RX_SCK/T3_CAP0
	F1	P0[24]/ADC0_IN[1]/I2S_RX_WS/T3_CAP1
	E4	P0[25]/ADC0_IN[2]/I2S_RX_SDA/U3_TXD
	D1	P0[26]/ADC0_IN[3]/DAC_OUT/U3_RXD
I2C_IPMB_SDA	L3	P0[27]/I2C0_SDA/USB_SDA1
I2C_IPMB_SCL	M1	P0[28]/I2C0_SCL/USB_SCL1
OVER_TEMP	K5	P0[29]/USB_D+1/EINT0
P12V0_OK	N1	P0[30]/USB_D-1/EINT1
	N4	P0[31]/USB_D+2
AT_DET	B5	P1[0]/ENET_TXD0/T3_CAP1/SSP2_SCK
	A5	P1[1]/ENET_TXD1/T3_MAT3/SSP2_MOSI
	B7	P1[2]/ENET_TXD2/SD_CLK/PWM0[1]
	A9	P1[3]/ENET_TXD3/SD_CMD/PWM0[2]
	C6	P1[4]/ENET_TX_EN/T3_MAT2/SSP2_MISO
	B13	P1[5]/ENET_TX_ER/SD_PWR/PWM0[3]
	B10	P1[6]/ENET_TX_CLK/SD_DAT[0]/PWM0[4]
	C13	P1[7]/ENET_COL/SD_DAT[1]/PWM0[5]
	B6	P1[8]/ENET_CRS(ENET_CRS_DV)/T3_MAT1/SSP2_SSEL
	D7	P1[9]/ENET_RXD0/T3_MAT0
	A7	P1[10]/ENET_RXD1/T3_CAP0
	A12	P1[11]/ENET_RXD2/SD_DAT[2]/PWM0[6]
	A14	P1[12]/ENET_RXD3/SD_DAT[3]/PWM0_CAP0
	D14	P1[13]/ENET_RX_DV
	D8	P1[14]/ENET_RX_ER/T2_CAP0
	A8	P1[15]/ENET_RX_CLK(ENET_REF_CLK)/I2C2_SDA
MII_MDC	B8	P1[16]/ENET_MDC/I2S_TX_MCLK
MII_MDIO	C9	P1[17]/ENET_MDIO/I2S_RX_MCLK
EN_FMC2_P12V	L5	P1[18]/USB_UP_LED1/PWM1[1]/T1_CAP0/SSP1_MISO
FLASH_UPD_CLK	P5	P1[19]/USB_TX_E1/USB_PPWR1/T1_CAP1/MC_0A/SSP1_SCK/U2_OE
FLASH_UPD_CSB	K6	P1[20]/USB_TX_DP1/PWM1[2]/QEI_PHA/MC_FB0/SSP0_SCK
PGOOD_P5V0	N6	P1[21]/USB_TX_DM1/PWM1[3]/SSP0_SSEL/MC_ABORT
FLASH_UPD_MISO	M6	P1[22]/USB_RCV1/USB_PWRD1/T1_MAT0/MC_0B/SSP1_MOSI
FLASH_UPD_MOSI	N7	P1[23]/USB_RX_DP1/PWM1[4]/QEI_PHB/MC_FB1/SSP0_MISO
	P7	P1[24]/USB_RX_DM1/PWM1[5]/QEI_IDX/MC_FB2/SSP0_MOSI
	L7	P1[25]/USB_LS1/USB_HSTEN1/T1_MAT1/MC_1A/CLKOUT
	P8	P1[26]/USB_SSPND1/PWM1[6]/T0_CAP0/MC_1B/SSP1_SSEL
EN_FMC1_P12V	M9	P1[27]/USB_INT1/USB_OVRCR1/T0_CAP1/CLKOUT
EN_VCCINT	P10	P1[28]/USB_SCL1/PWM1_CAP0/T0_MAT0/MC_2A/SSP0_SSEL
EN_P5V0	N10	P1[29]/USB_SDA1/PWM1_CAP1/T0_MAT1/MC_2B/U4_TXD
	K3	P1[30]/USB_PWRD2/USB_VBUS/ADC0_IN[4]/I2C0_SDA/U3_OE
EN_PSU_CH	K2	P1[31]/USB_OVRCR2/SSP1_SCK/ADC0_IN[5]/I2C0_SCL

+3V3MP — R133 2k2, R134 2k2

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+3V3MP — R143 10k, R145 10k

AMC_En (R158 100)	J11	P4[0]/EMC_A[0]
FPGA_RESETn	H12	P4[1]/EMC_A[1]
	G12	P4[2]/EMC_A[2]
SW	F11	P4[3]/EMC_A[3]
	F10	P4[4]/EMC_A[4]
R142 10k — GND	B14	P4[5]/EMC_A[5]
	E8	P4[6]/EMC_A[6]
	C10	P4[7]/EMC_A[7]
	N12	P4[8]/EMC_A[8]
	N13	P4[9]/EMC_A[9]
	P14	P4[10]/EMC_A[10]
	M14	P4[11]/EMC_A[11]
	C8	P4[12]/EMC_A[12]
	D9	P4[13]/EMC_A[13]
	K13	P4[14]/EMC_A[14]
	F14	P4[15]/EMC_A[15]
	D10	P4[16]/EMC_A[16]
	B9	P4[17]/EMC_A[17]
	C7	P4[18]/EMC_A[18]
	E7	P4[19]/EMC_A[19]
		P4[24]/EMC_OE
		P4[25]/EMC_WE
		P4[26]/EMC_BLS0
		P4[27]/EMC_BLS1
		P4[28]/EMC_BLS2/U3_TXD/T2_MAT0
		P4[29]/EMC_BLS3/U3_RXD/T2_MAT1/I2C2_SCL
		P4[30]/EMC_CS0
		P4[31]/EMC_CS1
	E5	P5[0]/EMC_A[24]/SSP2_MOSI/T2_MAT2
	H1	P5[1]/EMC_A[25]/SSP2_MISO/T2_MAT3
	L12	P5[2]/T3_MAT2/I2C0_SDA
UART4_RxD	G10	P5[3]/U4_RXD/I2C0_SCL
UART4_TxD	C4	P5[4]/U0_OE/T3_MAT3/U4_TXD

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UART1_TxD	D12	P2[0]/PWM1[1]/U1_TXD
UART1_RxD	C14	P2[1]/PWM1[2]/U1_RXD
	E11	P2[2]/PWM1[3]/U1_CTS/T2_MAT3/TRACEDATA[3]
	E13	P2[3]/PWM1[4]/U1_DCD/T2_MAT2/TRACEDATA[2]
SDRAM_PGOOD	E14	P2[4]/PWM1[5]/U1_DSR/T2_MAT1/TRACEDATA[1]
	F12	P2[5]/PWM1[6]/U1_DTR/T2_MAT0/TRACEDATA[0]
	F13	P2[6]/PWM1_CAP0/U1_RI/T2_CAP0/U2_OE/TRACECLK
	G11	P2[7]/CAN_RD2/U1_RTS
	G14	P2[8]/CAN_TD2/U2_TXD/U1_CTS/ENET_MDC
	H11	P2[9]/USB_CONNECT1/U2_RXD/U4_RXD/ENET_MDIO
LPC_ISPn	M13	P2[10]/EINT0/NMI
	M12	P2[11]/EINT1/SD_DAT[1]/I2S_TX_SCK
	N14	P2[12]/EINT2/SD_DAT[2]/I2S_TX_WS
	M11	P2[13]/EINT3/SD_DAT[3]/I2S_TX_SDA
BOOT_MODE[0..3]	P9	P2[16]/EMC_CAS
	P11	P2[17]/EMC_RAS
	P3	P2[18]/EMC_CLK[0]
	N5	P2[19]/EMC_CLK[1]
	P6	P2[20]/EMC_DYCS0
	N8	P2[21]/EMC_DYCS1
	P1	P2[24]/EMC_CKE0
	P2	P2[25]/EMC_CKE1
	M2	P2[28]/EMC_DQM0
	L1	P2[29]/EMC_DQM1
AMC_GA[0..2]	D6	P3[0]/EMC_D[0]
	E6	P3[1]/EMC_D[1]
	A2	P3[2]/EMC_D[2]
	G5	P3[3]/EMC_D[3]
	D3	P3[4]/EMC_D[4]
	E3	P3[5]/EMC_D[5]
FMC1_PRSNT_M2C_L (R151 100)	F4	P3[6]/EMC_D[6]
FMC2_PRSNT_M2C_L (R152 100)	G3	P3[7]/EMC_D[7]
	A6	P3[8]/EMC_D[8]
	A4	P3[9]/EMC_D[9]
FMC1_PG_C2M (R153 100)	B3	P3[10]/EMC_D[10]
FMC2_PG_C2M (R154 100)	B2	P3[11]/EMC_D[11]
	A1	P3[12]/EMC_D[12]
	C1	P3[13]/EMC_D[13]
	F1	P3[14]/EMC_D[14]
	G4	P3[15]/EMC_D[15]
HW_ID0	M4	P3[23]/EMC_D[23]/PWM1_CAP0/T0_CAP0
HW_ID1	N3	P3[24]/EMC_D[24]/PWM1[1]/T0_CAP1
HW_ID2	M3	P3[25]/EMC_D[25]/PWM1[2]/T0_MAT0
HW_ID3	K7	P3[26]/EMC_D[26]/PWM1[3]/T0_MAT1/STCLK

R144 10k, R146 10k, R147 10k, R155 10k — GND

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	N2	USB_D-2
ISP_RSTn (D3 BAT165)	J1	RESET
	H2	RSTOUT
	C3	JTAG_TDI
	B1	JTAG_TDO(SWO)
	D2	JTAG_TCK(SWDCLK)
	C2	JTAG_TMS(SWDIO)
	D4	JTAG_TRST
Clock source option — Y5 8MHz, C92 22pF, C93 22pF	L2	XTAL1
C102 100pF, R132 0 — GND	K4	XTAL2
	J2	RTCX1
	J3	RTCX2
	H5	RTC_ALARM

LPC_RST → LPC_RST
MMC_TDI → MMC_TDI
MMC_TDO → MMC_TDO
MMC_TCK → MMC_TCK
MMC_TMS → MMC_TMS
MMC_TRST
R137 10k, R138 10k, R139 10k, R140 10k — GND, +3V3MP
CLK_25MHZ → CLK_25MHZ

+3V3MP — L27 120R@100MHz — C199 100nF — GND

U31E
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	K1	VBAT	
	F2	VDDA	VSSA F3
	C5	VDD(3V3)	VSS B4
	E10	VDD(3V3)	VSS C11
	E12	VDD(3V3)	VSS D13
	F2	VDD(3V3)	VSS G13
	J14	VDD(3V3)	VSS H4
	K8	VDD(3V3)	VSS L13
	L11	VDD(3V3)	VSS L9
	L4	VDD(3V3)	VSS P4
	E9	VDD(REG)(3V3)	VSSREG A10
	G1	VDD(REG)(3V3)	VSSREG H3
	N9	VDD(REG)(3V3)	VSSREG L8
	G2	VREFP	

GND

+3V3MP — C197 100nF, C200 100nF, C202 100nF, C204 100nF, C206 100nF, C208 100nF — GND
+3V3MP — C198 100nF, C201 100nF, C203 100nF, C205 100nF, C207 100nF, C209 100nF — GND

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Sheet: /MMC/
File: MMC.sch
Title: Simple AFC
Size: A3 | Date: 2019-01-16 | Rev: 9
KiCad E.D.A. kicad (6.0.0-rc1-dev-577-ge0316af69) | Id: 25/25