Non-IQ Digital Down-Conversion

Introduction to digital Low-Level Radio Frequency Controls in Accelerators

Lab 10

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Contents

1 Introduction

This lab is a demonstration of a working Non-IQ Digital Down-Conversion (DDC) that is part of the LLRF firmware in this class. Read http://recycle.lbl.gov/~ldoolitt/llrf/down/reconstruct.pdf for more information.

The test bench injects a sinusoidal waveform with amplitude of `SIG_AMP_CNT` and phase of `SIG_PHS_DEG` after clock cycle `CC_N0` to the DDC module `noniq_ddc.v`, which takes 6 clock cycles of latency, to produce an interleaved stream of base band I,Q signals, which is then separated with interpolation by `fiq_interp.v` by 4 cycles.

The test bench also checks the expected amplitude and phase response with the produced signals, using the equations we showed in the lecture.

2 Exercises

2.1 Run simulation

The following command will generate a waveform file, and check results.

```
make noniq_ddc.vcd
```

Inspect the waveform for timing and scaling of the process. Adjust parameters of the test bench file `noniq_ddc_tb.v` for stimulus signal amplitude and phase and check results.