

1. Description

1.1. Project

Project Name	SnakeGameTest
Board Name	NUCLEO-F303K8
Generated with:	STM32CubeMX 6.15.0
Date	07/22/2025

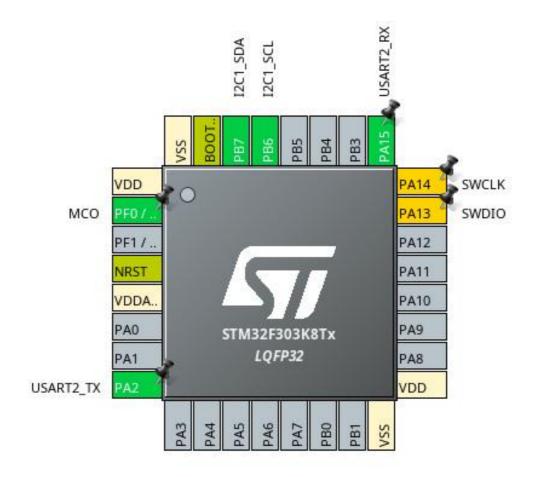
1.2. MCU

MCU Series	STM32F3
MCU Line	STM32F303
MCU name	STM32F303K8Tx
MCU Package	LQFP32
MCU Pin number	32

1.3. Core(s) information

Core(s)	Arm Cortex-M4

2. Pinout Configuration

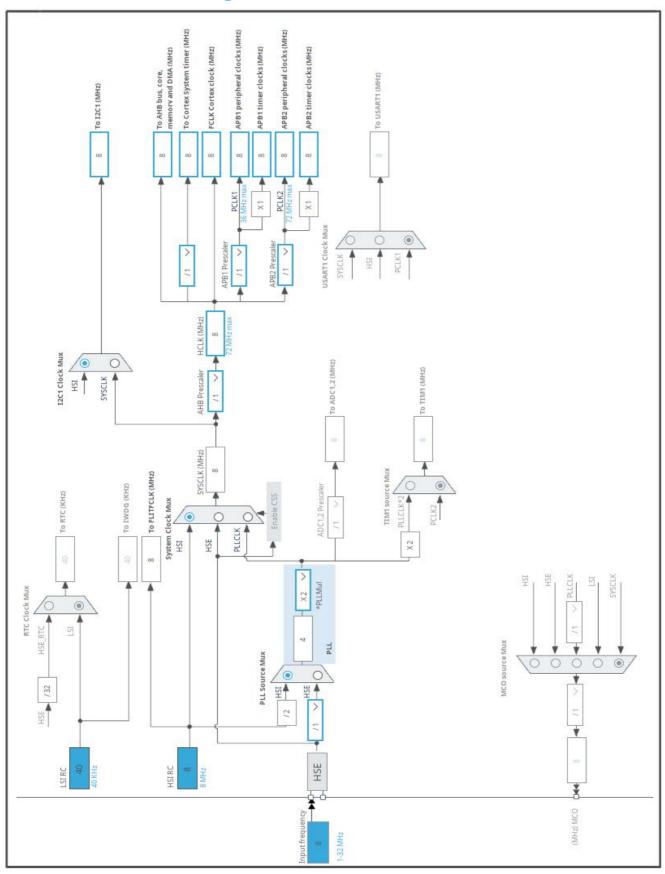


3. Pins Configuration

Pin Number LQFP32	Pin Name (function after reset)	Pin Type	Alternate Function(s)	Label
1	VDD	Power		
2	PF0/OSC_IN	I/O	RCC_OSC_IN	МСО
4	NRST	Reset		
5	VDDA/VREF+	Power		
8	PA2	I/O	USART2_TX	
16	VSS	Power		
17	VDD	Power		
23	PA13 *	I/O	SYS_JTMS-SWDIO	SWDIO
24	PA14 *	I/O	SYS_JTCK-SWCLK	SWCLK
25	PA15	I/O	USART2_RX	
29	PB6	I/O	I2C1_SCL	
30	PB7	I/O	I2C1_SDA	
31	воото	Boot		
32	VSS	Power		

^{*} The pin is affected with a peripheral function but no peripheral mode is activated

4. Clock Tree Configuration



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1. Power Consumption Calculator report

1.1. Microcontroller Selection

Series	STM32F3
Line	STM32F303
MCU	STM32F303K8Tx
Datasheet	DS9866_Rev5

1.2. Parameter Selection

Temperature	25
Vdd	3.6

1.3. Battery Selection

Battery	Li-SOCL2(A3400)
Capacity	3400.0 mAh
Self Discharge	0.08 %/month
Nominal Voltage	3.6 V
Max Cont Current	100.0 mA
Max Pulse Current	200.0 mA
Cells in series	1
Cells in parallel	1

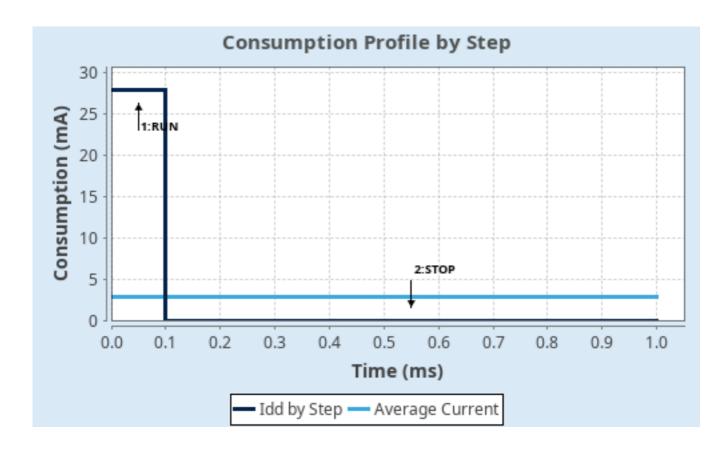
1.4. Sequence

	1	
Step	Step1	Step2
Mode	RUN	STOP
Vdd	3.6	3.6
Voltage Source	Battery	Battery
Range	No Scale	No Scale
Fetch Type	RAM	n/a
CPU Frequency	72 MHz	0 Hz
Clock Configuration	HSEBYP PLL	Regulator LP
Clock Source Frequency	8 MHz	0 Hz
Peripherals		
Additional Cons.	0 mA	0 mA
Average Current	27.84 mA	9.55 μΑ
Duration	0.1 ms	0.9 ms
DMIPS	90.0	0.0
Ta Max	98.99	105
Category	In DS Table	In DS Table

1.5. Results

Sequence Time	1 ms	Average Current	2.79 mA
Battery Life	1 month, 20 days,	Average DMIPS	90.0 DMIPS
	5 hours		

1.6. Chart



2. Software Project

2.1. Project Settings

Name	Value
Project Name	SnakeGameTest
Project Folder	/home/berke/STM32CubeIDE/workspace_1.19.0/SnakeGameTest
Toolchain / IDE	STM32CubeIDE
Firmware Package Name and Version	STM32Cube FW_F3 V1.11.5
Application Structure	Advanced
Generate Under Root	Yes
Do not generate the main()	No
Minimum Heap Size	0x200
Minimum Stack Size	0x400

2.2. Code Generation Settings

Name	Value
STM32Cube MCU packages and embedded software	Copy only the necessary library files
Generate peripheral initialization as a pair of '.c/.h' files	No
Backup previously generated files when re-generating	No
Keep User Code when re-generating	Yes
Delete previously generated files when not re-generated	Yes
Set all free pins as analog (to optimize the power	No
consumption)	
Enable Full Assert	No

2.3. Advanced Settings - Generated Function Calls

Rank	Function Name	Peripheral Instance Name
1	SystemClock_Config	RCC
2	MX_GPIO_Init	GPIO
3 MX_I2C1_Init		I2C1
4	MX_USART2_UART_Init	USART2

3. Peripherals and Middlewares Configuration

3.1. I2C1

12C: 12C

3.1.1. Parameter Settings:

Timing configuration:

I2C Speed Mode Standard Mode

I2C Speed Frequency (KHz)100Rise Time (ns)100Fall Time (ns)100Coefficient of Digital Filter0

Analog Filter Enabled

Timing 0x00201D2B *

Slave Features:

Clock No Stretch Mode Disabled
General Call Address Detection Disabled
Primary Address Length selection 7-bit
Dual Address Acknowledged Disabled
Primary slave address 0

3.2. RCC

High Speed Clock (HSE): BYPASS Clock Source

3.2.1. Parameter Settings:

System Parameters:

VDD voltage (V) 3.3
Prefetch Buffer Enabled

Flash Latency(WS) 0 WS (1 CPU cycle)

RCC Parameters:

HSI Calibration Value 16
HSE Startup Timout Value (ms) 100
LSE Startup Timout Value (ms) 5000

3.3. SYS

Timebase Source: TIM6

3.4. **USART2**

Mode: Asynchronous

3.4.1. Parameter Settings:

Basic Parameters:

Baud Rate 38400

Word Length 8 Bits (including Parity)

Parity None Stop Bits 1

Advanced Parameters:

Data Direction Receive and Transmit

Over Sampling 16 Samples
Single Sample Disable

Advanced Features:

TX Pin Active Level Inversion

RX Pin Active Level Inversion

Disable

Data Inversion

Disable

TX and RX Pins Swapping

Overrun

Enable

DMA on RX Error

Enable

MSB First

Disable

3.5. FREERTOS

Interface: CMSIS_V2

3.5.1. Config parameters:

API:

FreeRTOS API CMSIS v2

Versions:

FreeRTOS version 10.0.1 CMSIS-RTOS version 2.00

Kernel settings:

USE_PREEMPTION Enabled

CPU_CLOCK_HZ SystemCoreClock

TICK_RATE_HZ 1000
MAX_PRIORITIES 56
MINIMAL_STACK_SIZE 128
MAX_TASK_NAME_LEN 16

Disabled USE_16_BIT_TICKS Enabled IDLE_SHOULD_YIELD Enabled USE_MUTEXES USE_RECURSIVE_MUTEXES Enabled Enabled USE_COUNTING_SEMAPHORES QUEUE_REGISTRY_SIZE 8 USE_APPLICATION_TASK_TAG Disabled Enabled ENABLE_BACKWARD_COMPATIBILITY USE_PORT_OPTIMISED_TASK_SELECTION Disabled Disabled USE_TICKLESS_IDLE Enabled USE_TASK_NOTIFICATIONS Disabled RECORD_STACK_HIGH_ADDRESS

Memory management settings:

Memory Allocation Dynamic / Static

TOTAL_HEAP_SIZE 3072

Memory Management scheme heap_4

Hook function related definitions:

USE_IDLE_HOOK Disabled
USE_TICK_HOOK Disabled
USE_MALLOC_FAILED_HOOK Disabled
USE_DAEMON_TASK_STARTUP_HOOK Disabled
CHECK_FOR_STACK_OVERFLOW Disabled

Run time and task stats gathering related definitions:

GENERATE_RUN_TIME_STATS Disabled
USE_TRACE_FACILITY Enabled
USE_STATS_FORMATTING_FUNCTIONS Disabled

Co-routine related definitions:

USE_CO_ROUTINES Disabled MAX_CO_ROUTINE_PRIORITIES 2

Software timer definitions:

USE_TIMERS Enabled
TIMER_TASK_PRIORITY 2
TIMER_QUEUE_LENGTH 10
TIMER_TASK_STACK_DEPTH 256

Interrupt nesting behaviour configuration:

LIBRARY_LOWEST_INTERRUPT_PRIORITY 15
LIBRARY_MAX_SYSCALL_INTERRUPT_PRIORITY 5

3.5.2. Include parameters:

Include definitions:

vTaskPrioritySet Enabled uxTaskPriorityGet Enabled Enabled vTaskDelete vTaskCleanUpResources Disabled Enabled vTaskSuspend Enabled vTaskDelayUntil Enabled vTaskDelay Enabled xTaskGetSchedulerState xTaskResumeFromISR Enabled xQueueGetMutexHolder Enabled Disabled xSemaphoreGetMutexHolder Disabled pcTaskGetTaskName Enabled uxTaskGetStackHighWaterMark Disabled xTaskGetCurrentTaskHandle Enabled eTaskGetState Disabled $x \\ Event Group Set Bit From ISR$ Enabled xTimerPendFunctionCall xTaskAbortDelay Disabled xTaskGetHandle Disabled

3.5.3. Advanced settings:

Newlib settings (see parameter description first):

USE_NEWLIB_REENTRANT Enabled *

Project settings (see parameter description first):

Use FW pack heap file Enabled

^{*} User modified value

4. System Configuration

4.1. GPIO configuration

IP	Pin	Signal	GPIO mode	GPIO pull/up pull down	Max Speed	User Label
I2C1	PB6	I2C1_SCL	Alternate Function Open Drain	No pull-up and no pull-down	High *	
	PB7	I2C1_SDA	Alternate Function Open Drain	No pull-up and no pull-down	High *	
RCC	PF0 / OSC_IN	RCC_OSC_IN	n/a	n/a	n/a	MCO
USART2	PA2	USART2_TX	Alternate Function Push Pull	No pull-up and no pull-down	High *	
	PA15	USART2_RX	Alternate Function Push Pull	No pull-up and no pull-down	High *	
Single Mapped	PA13	SYS_JTMS- SWDIO	n/a	n/a	n/a	SWDIO
Signals	PA14	SYS_JTCK- SWCLK	n/a	n/a	n/a	SWCLK

4.2. DMA configuration

nothing configured in DMA service

4.3. NVIC configuration

4.3.1. NVIC

Interrupt Table	Enable	Preenmption Priority	SubPriority
Non maskable interrupt	true	0	0
Hard fault interrupt	true	0	0
Memory management fault	true	0	0
Pre-fetch fault, memory access fault	true	0	0
Undefined instruction or illegal state	true	0	0
System service call via SWI instruction	true	0	0
Debug monitor	true	0	0
Pendable request for system service	true	15	0
System tick timer	true	15	0
USART2 global interrupt / USART2 wake-up interrupt through EXT line 26	true	5	0
TIM6 global and DAC1 underrun error interrupts	true	15	0
PVD interrupt through EXTI line 16		unused	
Flash global interrupt		unused	
RCC global interrupt		unused	
I2C1 event global interrupt / I2C1 wake-up interrupt through EXT line 23		unused	
I2C1 error interrupt		unused	
Floating point unit interrupt		unused	

4.3.2. NVIC Code generation

Enabled interrupt Table	Select for init sequence ordering	Generate IRQ handler	Call HAL handler
Non maskable interrupt	false	true	false
Hard fault interrupt	false	true	false
Memory management fault	false	true	false
Pre-fetch fault, memory access fault	false	true	false
Undefined instruction or illegal state	false	true	false
System service call via SWI instruction	false	false	false
Debug monitor	false	true	false
Pendable request for system service	false	false	false
System tick timer	false	false	true
USART2 global interrupt / USART2 wake- up interrupt through EXT line 26	false	true	true
TIM6 global and DAC1 underrun error interrupts	false	true	true

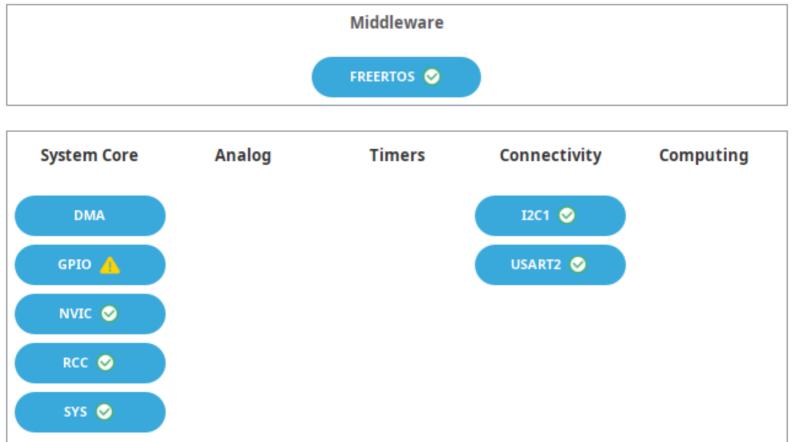
SnakeGameTest Proje	ect
Configuration Rep	ort

* User modified value

5. System Views

5.1. Category view

5.1.1. Current



6. Docs & Resources

Type Link

BSDL files https://www.st.com/resource/en/bsdl_model/stm32f3_bsdl.zip

System View https://www.st.com/resource/en/svd/stm32f3-svd.zip

Description

Presentations https://www.st.com/resource/en/product_presentation/stm32-

stm8_embedded_software_solutions.pdf

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tools_portfolio.pdf

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onal-safety-packages.pdf

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Security Bulletin https://www.st.com/resource/en/technical_note/tn1489-security-bulletin-

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- Application Notes https://www.st.com/resource/en/application_note/an4228-migrating-from-stm32f1-series-to-stm32f3-series-microcontrollers-stmicroelectronics.pdf
- Application Notes https://www.st.com/resource/en/application_note/an4232-getting-started-with-analog-comparators-for-stm32f3-series-and-stm32g4-series-devices-stmicroelectronics.pdf
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& Software

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& Software stm32cube-stmicroelectronics.pdf

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