JTAG

Confiabilidade e Segurança de Hardware

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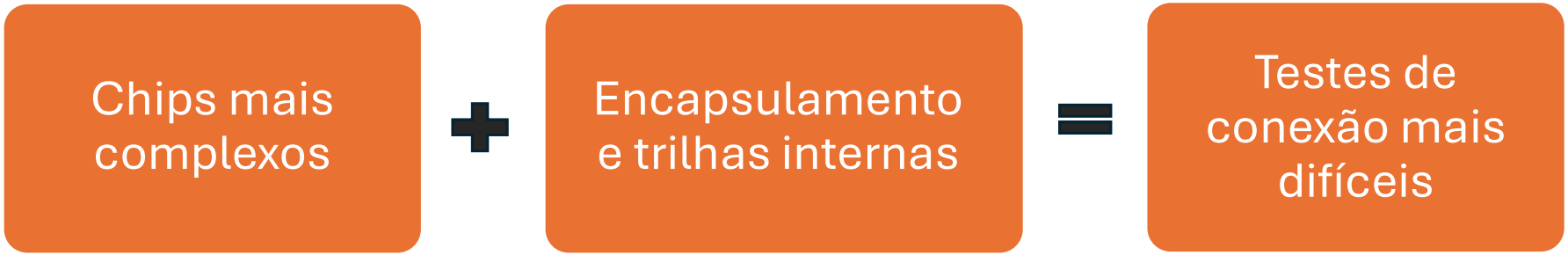
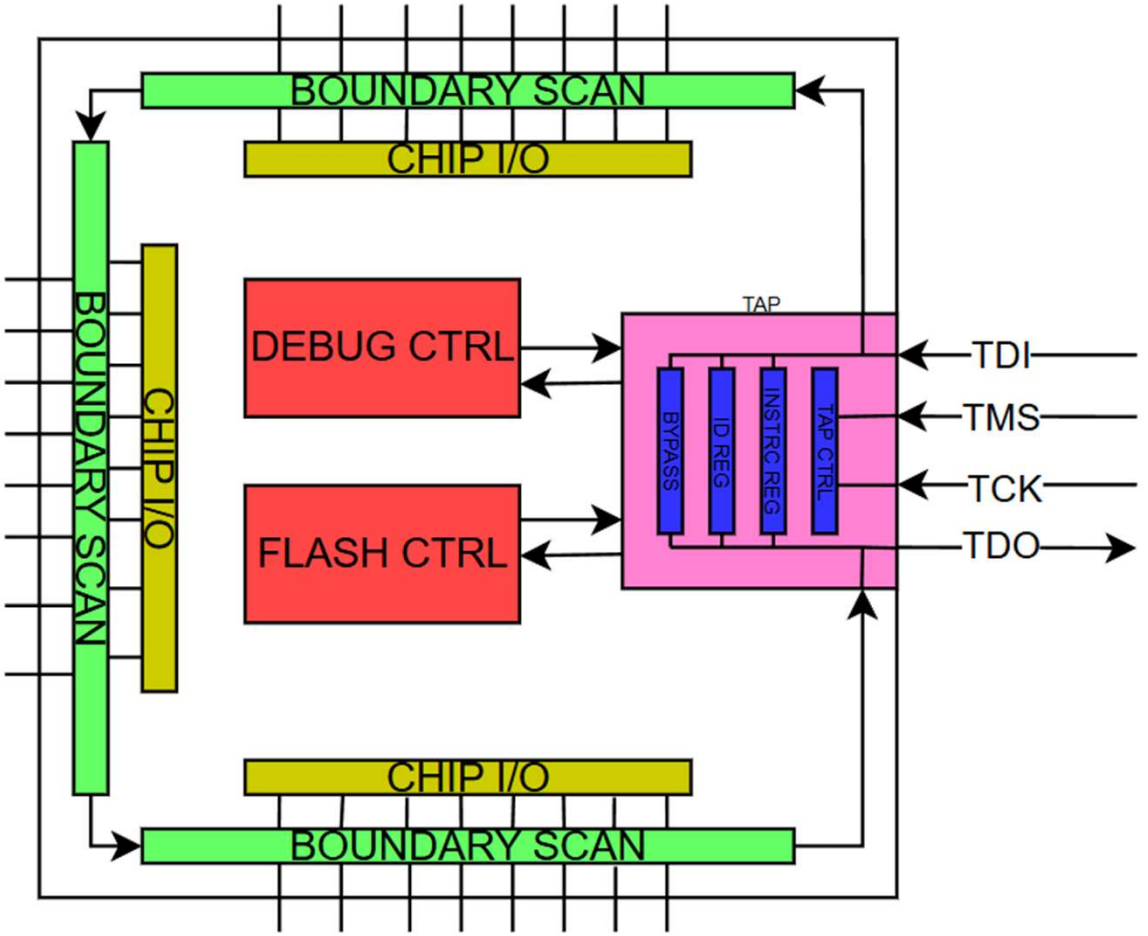
Motivação


Chips mais complexos
+
Encapsulamento e trilhas internas
=
Testes de conexão mais difíceis

JTAG (Join Test Action Group)

- Interface serial com 4–5 fios (TCK, TMS, TDI, TDO, TRST).
- Estrutura interna:
  - TAP Controller (FSM)
  - Instruction Register
  - Data Registers (IDCODE, BYPASS...)
  - Boundary Scan Cells nos IOs
- Acesso pode atingir: debug, flash, periféricos e registradores internos.



SWD (Serial Wire Debug)

- Alternativa moderna da ARM ao JTAG.
- Usa apenas 2 fios: SWCLK + SWDIO.
- Oferece:
  - controle da CPU
  - leitura/escrita de memória
  - breakpoints e debug completo
- Não possui boundary scan.

Demonstração Prática (SWD + J-Link)

- Instalar o software oficial da Segger.
- Conectar STM -> JLink -> PC.
- Configurar Device.
- Pronto para debug.

```
# Pinout Jtag - SWD

                  ┌─────────┐
  Vref 3.3        | 1  | 2  |  Vref 3.3
 nTRST   ---      | 3  | 4  |  GND
 TDI     ---      | 5  | 6  |  GND
 RMS     SWIO     | 7  | 8  |  GND
 TCK     SWCK     | 9  | 10 |  GND
 RTCK    ---      | 11 | 12 |  GND
 SWO     TDO      | 13 | 14 |  GND
    RESET         | 15 | 16 |  GND
 DBGRO   ---      | 17 | 18 |  GND
    RESET         | 15 | 16 |  GND
   5v supply      | 19 | 20 |  GND
                  └─────────┘

# Pinout SWD STM32 CN4

  Nucleo CN4         J-Link/SWD
     Pin 2 (TCK)  <--> Pin 9  (SWCLK / TCK)
     Pin 3 (GND)  <--> Pin 4  (GND)
     Pin 4 (TMS)  <--> Pin 7  (SWDIO / TMS)
     Pin 5 (NRST) <--> Pin 15 (nRST)
     Pin 6 (SWO)  <--> Pin 13 (SWO / TDO)
     Any Vdd Pin  <--> Pin 1  (VTref)
```

J-Link v9

STM32F072RB