

MIPS: Logic and arithmetic instructions:

| MIPS instruction | | | Meaning |
|---------------------------------------|------------------|--------------------------|---|
| Mnemonic | Operands | Description | Operation |
| sll | \$rd, \$rt, num | Shift left logical | $\$rd \leftarrow \$rt \ll \text{num}$ |
| srl | \$rd, \$rt, num | Shift right logical | $\$rd \leftarrow \$rt \gg \text{num}$ |
| sra | \$rd, \$rt, num | Shift right arithmetic | $\$rd \leftarrow \$rt \gg \text{num} + \text{msb}$ |
| sllv | \$rd, \$rt, \$rs | Shift left logic. var. | $\$rd \leftarrow \$rt \ll \$rs$ |
| srlv | \$rd, \$rt, \$rs | Shift right logic. var. | $\$rd \leftarrow \$rt \gg \$rs$ |
| srav | \$rd, \$rt, \$rs | Shift right arithm. var. | $\$rd \leftarrow \$rt \gg \$rs + \text{msb}$ |
| num: (decimal) 0...31 | | | |
| add | \$rd, \$rt, \$rs | Add | $\$rd \leftarrow \$rt + \$rs$ |
| addu | \$rd, \$rt, \$rs | Add unsigned | $\$rd \leftarrow \$rt + \$rs$ |
| sub | \$rd, \$rt, \$rs | Subtract | $\$rd \leftarrow \$rt - \$rs$ |
| subu | \$rd, \$rt, \$rs | Subtract unsigned | $\$rd \leftarrow \$rt - \$rs$ |
| addi | \$rd, \$rt, imm | Add immediate | $\$rd \leftarrow \$rt + \text{imm}$ |
| addiu | \$rd, \$rt, imm | Add imm. unsign. | $\$rd \leftarrow \$rt + \text{imm}$ |
| mul | \$rd, \$rt, \$rs | Multiply | $\$rd \leftarrow \$rt * \$rs$ |
| mult | \$rt, \$rs | Multiply | $\$hi, \$lo \leftarrow \$rt * \rs |
| multu | \$rt, \$rs | Multiply unsigned | $\$hi, \$lo \leftarrow \$rt * \rs |
| div | \$rt, \$rs | Divide | $\$lo \leftarrow \$rt / \$rs$ |
| divu | \$rt, \$rs | Divide unsigned | $\$hi \leftarrow \$rt \% \$rs$ $\$lo \leftarrow \$rt / \$rs$ $\$hi \leftarrow \$rt \% \$rs$ |
| imm: halfword | | | |
| and | \$rd, \$rt, \$rs | AND | $\$rd \leftarrow \$rs \& \$rt$ |
| or | \$rd, \$rt, \$rs | OR | $\$rd \leftarrow \$rt \$rs$ |
| nor | \$rd, \$rt, \$rs | NOR | $\$rd \leftarrow !(\$rt \$rs)$ |
| xor | \$rd, \$rt, \$rs | XOR | $\$rd \leftarrow \$rt \wedge \$rs$ |
| andi | \$rd, \$rt, imm | AND immediate | $\$rd \leftarrow \$rt \& \text{imm}$ |
| ori | \$rd, \$rt, imm | OR immediate | $\$rd \leftarrow \$rt \text{imm}$ |
| xori | \$rd, \$rt, imm | XOR immediate | $\$rd \leftarrow \$rt \wedge \text{imm}$ |
| imm: halfword | | | |
| slt | \$rd, \$rt, \$rs | Set (1) if less than* | $\$rd \leftarrow (\$rt < \$rs) ? 1 : 0$ |
| sltu | \$rd, \$rt, \$rs | slt unsigned | $\$rd \leftarrow (\$rt < \$rs) ? 1 : 0$ |
| slti | \$rd, \$rt, imm | slt immediate | $\$rd \leftarrow (\$rt < \text{imm}) ? 1 : 0$ |
| sltiu | \$rd, \$rt, imm | slt imm. unsigned | $\$rd \leftarrow (\$rt < \text{imm}) ? 1 : 0$ |
| imm: halfword. *: Unset (0) otherwise | | | |

MIPS: Logic and arithmetic instructions:

| MIPS instruction | | Machine code | | | |
|-----------------------|------------------|--------------|--------|-----------|---------------|
| Mnemonic | Operands | format | opcode | \$A | \$B \$C imm |
| sll | \$rd, \$rt, num | R | 00/00 | 0 | \$rt \$rd num |
| srl | \$rd, \$rt, num | R | 00/02 | 0 | \$rt \$rd num |
| sra | \$rd, \$rt, num | R | 00/03 | 0 | \$rt \$rd num |
| sllv | \$rd, \$rt, \$rs | R | 00/04 | \$rs | \$rt \$rd 0 |
| srlv | \$rd, \$rt, \$rs | R | 00/06 | \$rs | \$rt \$rd 0 |
| srav | \$rd, \$rt, \$rs | R | 00/07 | \$rs | \$rt \$rd 0 |
| num: (decimal) 0...31 | | | | | |
| add | \$rd, \$rt, \$rs | R | 00/20 | \$rt \$rs | \$rd 0 |
| addu | \$rd, \$rt, \$rs | R | 00/21 | \$rt \$rs | \$rd 0 |
| sub | \$rd, \$rt, \$rs | R | 00/22 | \$rt \$rs | \$rd 0 |
| subu | \$rd, \$rt, \$rs | R | 00/23 | \$rt \$rs | \$rd 0 |
| addi | \$rd, \$rt, imm | I | 08/- | \$rt \$rd | - imm |
| addiu | \$rd, \$rt, imm | I | 09/- | \$rt \$rd | - imm |
| mul | \$rd, \$rt, \$rs | R | 1c/20 | \$rt \$rs | \$rd 0 |
| mult | \$rt, \$rs | R | 00/18 | \$rt \$rs | 0 0 |
| multu | \$rt, \$rs | R | 00/19 | \$rt \$rs | 0 0 |
| div | \$rt, \$rs | R | 00/1a | \$rt \$rs | 0 0 |
| divu | \$rt, \$rs | R | 00/1b | \$rt \$rs | 0 0 |
| imm: halfword | | | | | |
| and | \$rd, \$rt, \$rs | R | 00/24 | \$rt \$rs | \$rd 0 |
| or | \$rd, \$rt, \$rs | R | 00/25 | \$rt \$rs | \$rd 0 |
| nor | \$rd, \$rt, \$rs | R | 00/27 | \$rt \$rs | \$rd 0 |
| xor | \$rd, \$rt, \$rs | R | 00/26 | \$rt \$rs | \$rd 0 |
| andi | \$rd, \$rt, imm | I | 0c/- | \$rt \$rd | - imm |
| ori | \$rd, \$rt, imm | I | 0d/- | \$rt \$rd | - imm |
| xori | \$rd, \$rt, imm | I | 0e/- | \$rt \$rd | - imm |
| imm: halfword | | | | | |
| slt | \$rd, \$rt, \$rs | R | 00/2a | \$rt \$rs | \$rd 0 |
| sltu | \$rd, \$rt, \$rs | R | 00/2b | \$rt \$rs | \$rd 0 |
| slti | \$rd, \$rt, imm | I | 0a/- | \$rt \$rd | - imm |
| sltiu | \$rd, \$rt, imm | I | 0b/- | \$rt \$rd | - imm |
| imm: halfword | | | | | |

MIPS: Jump, branch and memory instructions:

| MIPS instruction | | Meaning | |
|---|---|---|--|
| Mnemonic | Operands | Description | Operation |
| j jal jr jalr | addr addr \$rs \$rs, \$rd | Jump Jump and link Jump register Jump and link register | pc←addr pc←addr, \$ra←pc+4 pc←\$rs pc←\$rs, \$rd←pc+4 |
| beq bne bltz bgtz blez bgez | \$rt, \$rs, addr \$rt, \$rs, addr \$rt, addr \$rt, addr \$rt, addr \$rt, addr | Branch if equal Branch if not equal Branch if < 0 Branch if > 0 Branch if <= 0 Branch if >= 0 | \$rs== \$rt?pc←addr \$rs!= \$rt?pc←addr \$rt<0?pc←addr \$rt>0?pc←addr \$rt<=0?pc←addr \$rt>=0?pc←addr |
| if condition is false: pc←pc+4. See pseudo-instructions for more branching instructions | | | |
| mfi mthi mflo mtlo | \$rd \$rs \$rd \$rs | Move from HI Move to HI Move from LO Move to LO | \$rd←hi \$rs→hi \$rd←lo \$rs→lo |
| lb lbu lh lhu lui lw sb sh sw | \$rd, offset(\$rt) \$rd, offset(\$rt) \$rd, offset(\$rt) \$rd, offset(\$rt) \$rd, imm \$rd, offset(\$rt) \$rs, offset(\$rt) \$rs, offset(\$rt) \$rs, offset(\$rt) | Load byte Load byte unsigned Load halfword Load halfword unsigned Load upper immediate Load word Store byte Store halfword Store word | \$rd←M[\$rt+offset] \$rd←M[\$rt+offset] \$rd←M[\$rt+offset] \$rd←M[\$rt+offset] \$rd←imm<<16 \$rd←M[\$rt+offset] \$rs→M[\$rt+offset] \$rs→M[\$rt+offset] \$rs→M[\$rt+offset] |

appropriate bits only, rest unchanged. M: memory. offset: halfword

MIPS: Jump, branch and memory instructions:

| MIPS instruction | | Machine code | | | | | |
|---|--------------------|--------------|-----------------|------|------|------|----------|
| Mne- monic | Operands | for- mat | opcode/ func | \$A | \$B | \$C | imm |
| j | addr | J | 02/- | - | - | - | mask |
| jal | addr | J | 03/- | - | - | - | mask |
| jr | \$rs | R | 00/08 | \$rs | 0 | 0 | 0 |
| jalr | \$rs, \$rd | R | 00/09 | \$rs | 0 | \$rd | 0 |
| imm: 26-bit unsigned value. addr=page*4+imm, page=pc&\$F0000000 mask=(addr&0FFFFFFF)/4 | | | | | | | |
| beq | \$rt, \$rs, addr | I | 04/- | \$rt | \$rs | - | relative |
| bne | \$rt, \$rs, addr | I | 05/- | \$rt | \$rs | - | relative |
| bltz | \$rt, addr | I | 01/- | \$rt | 0 | - | relative |
| bgtz | \$rt, addr | I | 07/- | \$rt | 0 | - | relative |
| blez | \$rt, addr | I | 06/- | \$rt | 0 | - | relative |
| bgez | \$rt, addr | I | 01/- | \$rt | 1 | - | relative |
| imm: 16-bit two's-complement signed value. relative=(addr-pc-4)/4 | | | | | | | |
| mghi | \$rd | R | 00/10 | 0 | 0 | \$rd | 0 |
| mthi | \$rs | R | 00/11 | \$rs | 0 | 0 | 0 |
| mflo | \$rd | R | 00/12 | 0 | 0 | \$rd | 0 |
| mtlo | \$rs | R | 00/13 | \$rs | 0 | 0 | 0 |
| | | | | | | | |
| lb | \$rd, offset(\$rt) | I | 20/- | \$rt | \$rd | - | offset |
| lbu | \$rd, offset(\$rt) | I | 24/- | \$rt | \$rd | - | offset |
| lh | \$rd, offset(\$rt) | I | 21/- | \$rt | \$rd | - | offset |
| lhu | \$rd, offset(\$rt) | I | 25/- | \$rt | \$rd | - | offset |
| lui | \$rd, imm | I | 0f/- | 0 | \$rd | - | imm |
| lw | \$rd, offset(\$rt) | I | 23/- | \$rt | \$rd | - | offset |
| sb | \$rs, offset(\$rt) | I | 28/- | \$rt | \$rs | - | offset |
| sh | \$rs, offset(\$rt) | I | 29/- | \$rt | \$rs | - | offset |
| sw | \$rs, offset(\$rt) | I | 2b/- | \$rt | \$rs | - | offset |

appropriate bits only, rest unchanged. offset: halfword
imm,offset: 16-bit two's-complement signed value.

MIPS: Floating-point instructions:

| MIPS instruction | | Meaning |
|--|-------------------------------|---|
| Mnemonic | Operands | Description Operation |
| <code>lwc1</code> | <code>\$fd, offs(\$rt)</code> | Load single $\$fd \leftarrow M[\$rt + \text{offs}]$ |
| <code>ldc1</code> | <code>\$fd, offs(\$rt)</code> | Load double $\$fd \leftarrow M[\$rt + \text{offs}]$ |
| <code>swc1</code> | <code>\$fs, offs(\$rt)</code> | Store single $\$fs \rightarrow M[\$rt + \text{offs}]$ |
| <code>sdcl</code> | <code>\$fs, offs(\$rt)</code> | Store double $\$fs \rightarrow M[\$rt + \text{offs}]$ |
| M: memory | | |
| Mnemonic | Operands | Description Operation |
| <code>c.eq.SIZE</code> | <code>\$fs, \$ft</code> | FPs equal $\text{cflag} \leftarrow (\$fs == \$ft) ? 1 : 0$ |
| <code>c.lt.SIZE</code> | <code>\$fs, \$ft</code> | FPs less than $\text{cflag} \leftarrow (\$fs < \$ft) ? 1 : 0$ |
| <code>c.le.SIZE</code> | <code>\$fs, \$ft</code> | FPs less or equal $\text{cflag} \leftarrow (\$fs \leq \$ft) ? 1 : 0$ |
| <code>cvt.TO.FROM</code> | <code>\$fd, \$fs</code> | Convert $\$fd = \text{convert}(\$fs)$ |
| <code>add.SIZE</code> | <code>\$fd, \$ft, \$fs</code> | FP add $\$fd \leftarrow \$ft + \$fs$ |
| <code>sub.SIZE</code> | <code>\$fd, \$ft, \$fs</code> | FP subtract $\$fd \leftarrow \$ft - \$fs$ |
| <code>mul.SIZE</code> | <code>\$fd, \$ft, \$fs</code> | FP multiply $\$fd \leftarrow \$ft * \$fs$ |
| <code>div.SIZE</code> | <code>\$fd, \$ft, \$fs</code> | FP divide $\$fd \leftarrow \$ft / \$fs$ |
| <code>mov.SIZE</code> | <code>\$fd, \$fs</code> | Copy $\$fd \leftarrow \fs |
| <code>mfc1</code> | <code>\$rd, \$fs</code> | Copy from co-proc. $\$rd \leftarrow \fs |
| <code>mtc1</code> | <code>\$rs, \$fd</code> | Copy to co-proc. $\$rs \rightarrow \fd |
| $\text{SIZE} = \{s, d\}. \{TO, FROM\} = \{s, d, w\}$ | | |
| Mnemonic | Operands | Description Operation |
| <code>bc1t</code> | <code>addr</code> | Branch if <code>cflag</code> true $\text{cflag} ? \text{pc} \leftarrow \text{addr}$ |
| <code>bc1f</code> | <code>addr</code> | Branch if <code>cflag</code> false $\text{cflag} ? \text{pc} \leftarrow \text{addr}$ |
| Otherwise: $\text{pc} \leftarrow \text{pc} + 4$ | | |
| Mnemonic | Operands | Description Operation |
| <code>sycall</code> | <code>num</code> | System call Exit with exception * |
| <code>break</code> | <code>num</code> | Exit with exception |

*: Specify type of `sycall` by `$v0`.

MIPS: Floating-point instructions:

| MIPS instruction | | Machine code |
|--|-------------------------------|---|
| Mnemonic | Operands | form opcode \$A \$B imm |
| <code>lwc1</code> | <code>\$fd, offs(\$rt)</code> | I 31 <code>\$rt</code> <code>\$fd</code> offs |
| <code>ldc1</code> | <code>\$fd, offs(\$rt)</code> | I 35 <code>\$rt</code> <code>\$fd</code> offs |
| <code>swc1</code> | <code>\$fs, offs(\$rt)</code> | I 39 <code>\$rt</code> <code>\$fs</code> offs |
| <code>sdcl</code> | <code>\$fs, offs(\$rt)</code> | I 3d <code>\$rt</code> <code>\$fs</code> offs |
| offs: 16-bit two's-complement signed value. | | |
| Mnemonic | Operands | form opc/typ \$A \$B \$C func |
| <code>c.eq.SIZE</code> | <code>\$fs, \$ft</code> | fr 11/tp <code>\$ft</code> <code>\$fs</code> 0 32 |
| <code>c.lt.SIZE</code> | <code>\$fs, \$ft</code> | fr 11/tp <code>\$ft</code> <code>\$fs</code> 0 3c |
| <code>c.le.SIZE</code> | <code>\$fs, \$ft</code> | fr 11/tp <code>\$ft</code> <code>\$fs</code> 0 3e |
| <code>cvt.TO.FROM</code> | <code>\$fd, \$fs</code> | fr 11/from 0 <code>\$fs</code> <code>\$fd</code> to |
| <code>add.SIZE</code> | <code>\$fd, \$ft, \$fs</code> | fr 11/tp <code>\$fs</code> <code>\$ft</code> <code>\$fd</code> 00 |
| <code>sub.SIZE</code> | <code>\$fd, \$ft, \$fs</code> | fr 11/tp <code>\$fs</code> <code>\$ft</code> <code>\$fd</code> 01 |
| <code>mul.SIZE</code> | <code>\$fd, \$ft, \$fs</code> | fr 11/tp <code>\$fs</code> <code>\$ft</code> <code>\$fd</code> 02 |
| <code>div.SIZE</code> | <code>\$fd, \$ft, \$fs</code> | fr 11/tp <code>\$fs</code> <code>\$ft</code> <code>\$fd</code> 03 |
| <code>mov.SIZE</code> | <code>\$fd, \$fs</code> | fr 11/tp <code>\$fd</code> <code>\$fs</code> 0 06 |
| <code>mfc1</code> | <code>\$rd, \$fs</code> | fr 11/00 <code>\$rd</code> <code>\$fs</code> 0 00 |
| <code>mtc1</code> | <code>\$rs, \$fd</code> | fr 11/04 <code>\$rs</code> <code>\$fd</code> 0 00 |
| $\text{SIZE}, \text{TO}, \text{FROM}: \{\text{tp}, \text{from}\} = 10 (s), 11 (d), 14 (w). \text{to} = 20 (s), 21 (d), 24 (w)$ | | |
| Mnemonic | Operands | form opc/typ \$A imm |
| <code>bc1t</code> | <code>addr</code> | fl 21/08 1 relative |
| <code>bc1f</code> | <code>addr</code> | fl 21/08 0 relative |
| imm: 16-bit two's-complement signed value. $\text{relative} = (\text{addr} - \text{pc} - 4) / 4$ | | |
| Mnemonic | Operands | form opc/func \$A \$B \$C imm |
| <code>sycall</code> | <code>num</code> | R 00/0c 0 0 0 0 |
| <code>break</code> | <code>num</code> | R 00/0d 0 0 0 0 |

MIPS: (Some) pseudo-instructions:

| | | | |
|------|--|-------------------------|--------------------|
| rol | \$rd, \$rt, num | Rotate left | \$rd←rol(\$rt,num) |
| | srl \$at, \$rt, 32-num | | |
| | sll \$rd, \$rt, num or \$rd, \$rd, \$at | | |
| ror | \$rd, \$rt, num | Rotate right | \$rd←ror(\$rt,num) |
| | sll \$at, \$rt, 32-num | | |
| | srl \$rd, \$rt, num or \$rd, \$rd, \$at | | |
| blt | \$rt, \$rs, addr | Branch if less than | \$rt<\$rs?pc←addr |
| | slt \$at, \$rt, \$rs bne \$at, \$zero, addr | | |
| bgt | \$rt, \$rs, addr | Branch if greater than | \$rt>\$rs?pc←addr |
| | slt \$at, \$rs, \$rt bne \$at, \$zero, addr | | |
| ble | \$rt, \$rs, addr | Branch if less/equal | \$rt<=\$rs?pc←addr |
| | slt \$at, \$rs, \$rt beq \$at, \$zero, addr | | |
| bge | \$rt, \$rs, addr | Branch if greater/equal | \$rt<=\$rs?pc←addr |
| | slt \$at, \$rt, \$rs beq \$at, \$zero, addr | | |
| beqz | \$rt, addr | Branch if equal zero | \$rt==0?pc←addr |
| | beq \$rt, \$zero, addr | | |
| bnez | \$rt, addr | Branch if not equal 0 | \$rt!=0?pc←addr |
| | bne \$rt, \$zero, addr | | |
| move | \$rd, \$rs | Copy | \$rd←\$rs |
| | ori \$rd, \$zero, \$rs | | |
| jalr | \$rs | Jump and link register | pc←\$rs,\$ra←pc+4 |
| | jalr \$rs, \$ra | | |

MIPS: (Some) pseudo-instructions (cont.):

| | | | |
|--|--|------------------------|----------------|
| lw | \$rd, addr | Load word from address | \$rd←M[addr] |
| | lui \$at, addr≫16 lw \$rd, [addr AND 0x0000FFFF](\$at), | | |
| li | \$rd, word | Load immediate | \$rd←word |
| | lui \$at, word≫16 ori \$rd, \$at, word AND 0x0000FFFF | | |
| lh | \$rd, halfword | Load immediate | \$rd←halfword |
| | ori \$rd, \$zero, halfword | | |
| lh | \$rd, addr | Load address | \$rd←addr |
| | lui \$at, addr≫16 ori \$rd, \$at, addr AND 0x0000FFFF | | |
| Note: equal to instruction li \$rd, addr | | | |
| to be implemented by macros: | | | |
| inc | \$rt | Increment | \$rt←\$rt+1 |
| | addi \$rt, \$rt, 1 | | |
| dec | \$rt | Decrement | \$rt←\$rt-1 |
| | subi \$rt, \$rt, 1 | | |
| push | \$rs | Push onto stack | M[-\$sp]←\$rs |
| | addiu \$sp, \$sp, -4 sw \$rs, 0(\$sp) | | |
| pop | \$rd | Pop from stack | \$rd←M[\$sp++] |
| | lw \$rd, 0(\$sp) addiu \$sp, \$sp, 4 | | |
| return | | Return from subroutine | pc←\$ra |
| | jr \$ra | | |
| done | | Terminate | |
| | li \$v0, 10 syscall | | |

(MARS) MIPS system calls:

| function | \$v0 | argument(s) | return value(s) |
|------------------------------|------|--|--|
| print integer | 1 | \$a0 = integer | |
| print float | 2 | \$f12 = float | |
| print double | 3 | \$f12, \$f13 = double | |
| print string | 4 | \$a0 = address of null-terminated string | |
| read integer | 5 | | \$v0 integer read |
| read float | 6 | | \$f0 float read |
| read double | 7 | | \$f0,\$f1 double read |
| read string | 8 | \$a0 = address of buffer \$a1 = max. length | |
| exit (terminate execution) | 10 | | |
| print character | 11 | \$a0 = character | |
| read character | 12 | | \$v0 character read |
| open file | 13 | \$a0 = address of filename \$a1 = flags (0=read, 1=overwrite,9=append) \$a2 = mode (0) | \$v0 file descriptor |
| read from file | 14 | \$a0 = file descriptor \$a1 = addr. input buffer \$a2 = max length | \$v0 number of chars read (0:end-of-file, <0:error) |
| write to file | 15 | \$a0 = file descriptor \$a1 = addr. output buffer \$a2 = number of chars | \$v0 number of chars written (<0: error) |
| close file | 16 | \$a0 = file descriptor | |
| exit (terminate with value) | 17 | \$a0 = termination result | |
| print integer in hexadecimal | 34 | \$a0 = integer | |
| print integer in binary | 35 | \$a0 = integer | |
| print integer as unsigned | 36 | \$a0 = integer | |
| set random seed | 40 | \$a0 = integer | |
| random int | 41 | \$a0 = integer | \$a0: next random int |
| random int in range | 42 | \$a0 = integer \$a1 = limit | \$a0: next random int in range 0...\$a1-1 |
| random float | 43 | \$a0 = integer | \$f0: 0.0...0.999... |
| random double | 44 | \$a0 = integer | \$f0, \$f1: 0.0...0.999... |

MIPS registers:

| | | | | | | | |
|---|--------|----|------|----|------|----|------|
| 0 | \$zero | 8 | \$t0 | 16 | \$s0 | 24 | \$t8 |
| 1 | \$at | 9 | \$t1 | 17 | \$s1 | 25 | \$t9 |
| 2 | \$v0 | 10 | \$t2 | 18 | \$s2 | 26 | \$k0 |
| 3 | \$v1 | 11 | \$t3 | 19 | \$s3 | 27 | \$k1 |
| 4 | \$a0 | 12 | \$t4 | 20 | \$s4 | 28 | \$gp |
| 5 | \$a1 | 13 | \$t5 | 21 | \$s5 | 29 | \$sp |
| 6 | \$a2 | 14 | \$t6 | 22 | \$s6 | 30 | \$fp |
| 7 | \$a3 | 15 | \$t7 | 23 | \$s7 | 31 | \$ra |

MIPS instruction format types:

| | | | | | | | | | | | | |
|------|--------|------|-----|-----|-----|------|----|----|----|---|---|---|
| R : | 31 | 26 | 25 | 21 | 20 | 16 | 15 | 11 | 10 | 6 | 5 | 0 |
| | opcode | \$A | \$B | \$C | imm | func | | | | | | |
| I : | opcode | \$A | \$B | imm | | | | | | | | |
| J : | opcode | imm | | | | | | | | | | |
| fR : | opcode | type | \$A | \$B | \$C | func | | | | | | |
| fI : | opcode | type | \$A | imm | | | | | | | | |
| | 6 | 5 | 5 | 5 | 5 | 5 | 6 | | | | | |

Values in the tables are hexadecimal, unless otherwise specified

MARS (MIPS) assembler directives:

| Directive | Example | Meaning |
|---|--------------------------------------|--|
| <code>.data</code> | | Start of data segment |
| <code>.text</code> | | Start of code segment |
| <code>.globl</code> | <code>.globl main</code> | Entry point for external reference (linker) |
| <code>.space n</code> | | Reserve <i>n</i> bytes of space on the heap |
| <code>myarray: .space 12</code> | | |
| <code>.ascii "string"</code> | <code>mystring: .ascii "Ajax"</code> | Store string in heap memory |
| <code>.asciiz "string"</code> | | |
| <code>mytext: .asciiz "Benfica"</code> | | Store string+0x00 in heap memory |
| <code>.byte b1, b2,...bn</code> | | Store byte(s) in heap memory |
| <code>.half h1, h2,...hn</code> | | Store half-word(s) in memory |
| <code>.word w1, w2,...wn</code> | | Store word(s) in heap memory |
| <code>myvector: .word 1, 2, 4</code> | | |
| <code>.float f1, f2,...fn</code> | | Store float(s) in heap memory |
| <code>myvector: .float 1.0, 2.1, 3.6</code> | | |
| <code>.double d1, d2,...dn</code> | | Store double-precision float(s) in heap memory |
| <code>pi: .double 3.1415926E03</code> | | |
| <code>.eqv text text</code> | | Define a substitution |
| <code>.eqv myvalue 64</code> | | |
| <code>.macroend_macro</code> | | Define a macro* |
| <code>.macro endprog</code> | | (not a function) |
| <code>li \$v0, 10</code> | | |
| <code>syscall</code> | | |
| <code>.end_macro</code> | | |

*: (does not store it in memory)