PSoC® Creator™
Project Datasheet for MartinsMouseOhneWheel

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Table of Contents

1 Overview

The Cypress PSoC 4 is a family of 32-bit devices with the following characteristics:

- Digital system that includes configurable Universal Digital Blocks (UDBs) and specific function peripherals such as PWM, UART, SPI and I2C
- Analog subsystem that includes 12-bit SAR ADC, comparators, op amps, CapSense, LCD drive and more
- Several types of memory elements, including SRAM and flash
- Programming and debug system through Serial Wire Debug (SWD)
- High-performance 32-bit ARM Cortex-M0 core with a nested vectored interrupt controller (NVIC)
- Flexible routing to all pins

Figure 1 shows the major components of a typical PSoC 4200 BLE series member PSoC 4 device. For details on all the systems listed above, please refer to the PSoC 4 Technical Reference Manual .

Figure 1. PSoC 4200 BLE Device Series Block Diagram

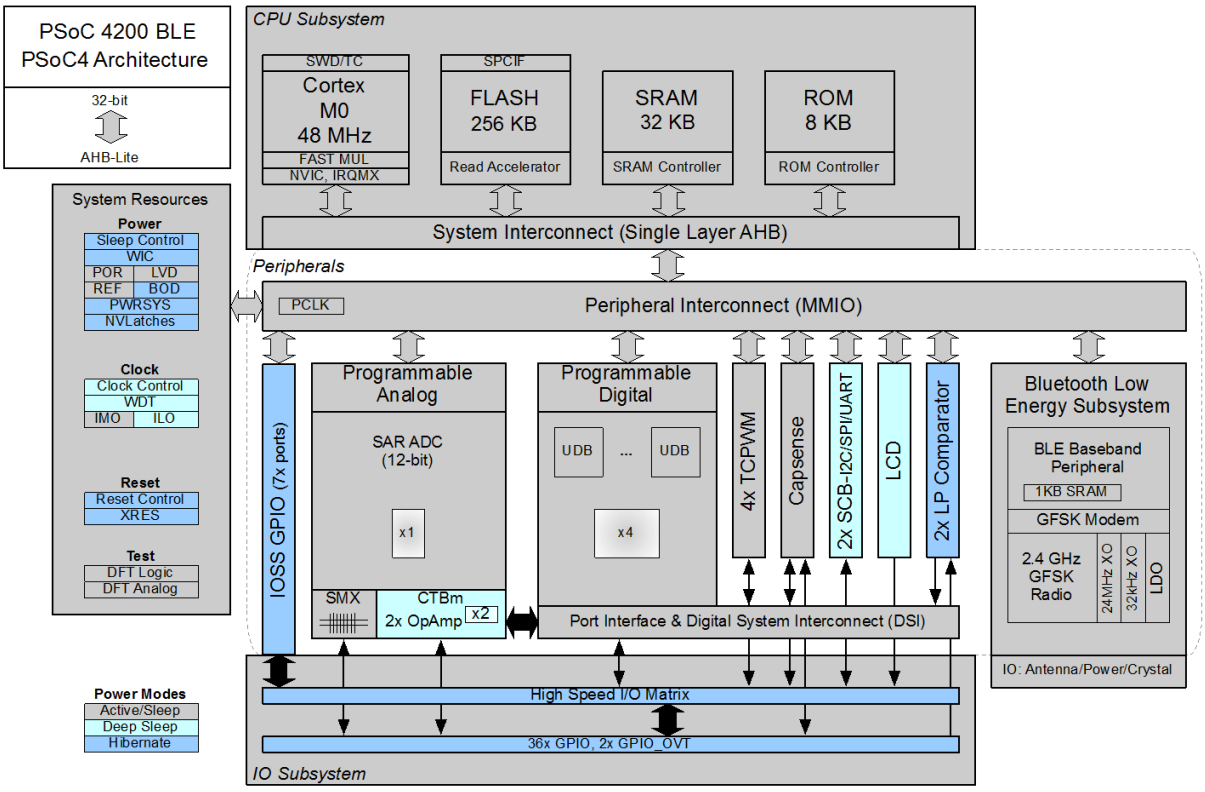


Table 1 lists the key characteristics of this device.

Table 1. Device Characteristics

Name	Value
Part Number	CYBLE-214015-01
Package Name	32-SMT
Family	PSoC 4
Series	PSoC 4200 BLE
Max CPU speed (MHz)	48
Flash size (kB)	256
SRAM size (kB)	32
Vdd range (V)	1.9 to 5.5
Automotive qualified	No (Industrial Grade Only)
Temp range (Celsius)	-40 to 85

NOTE: The CPU speed noted above is the maximum available speed. The CPU is clocked by HFCLK, listed in the System Clocks section below.

Table 2 lists the device resources that this design uses:

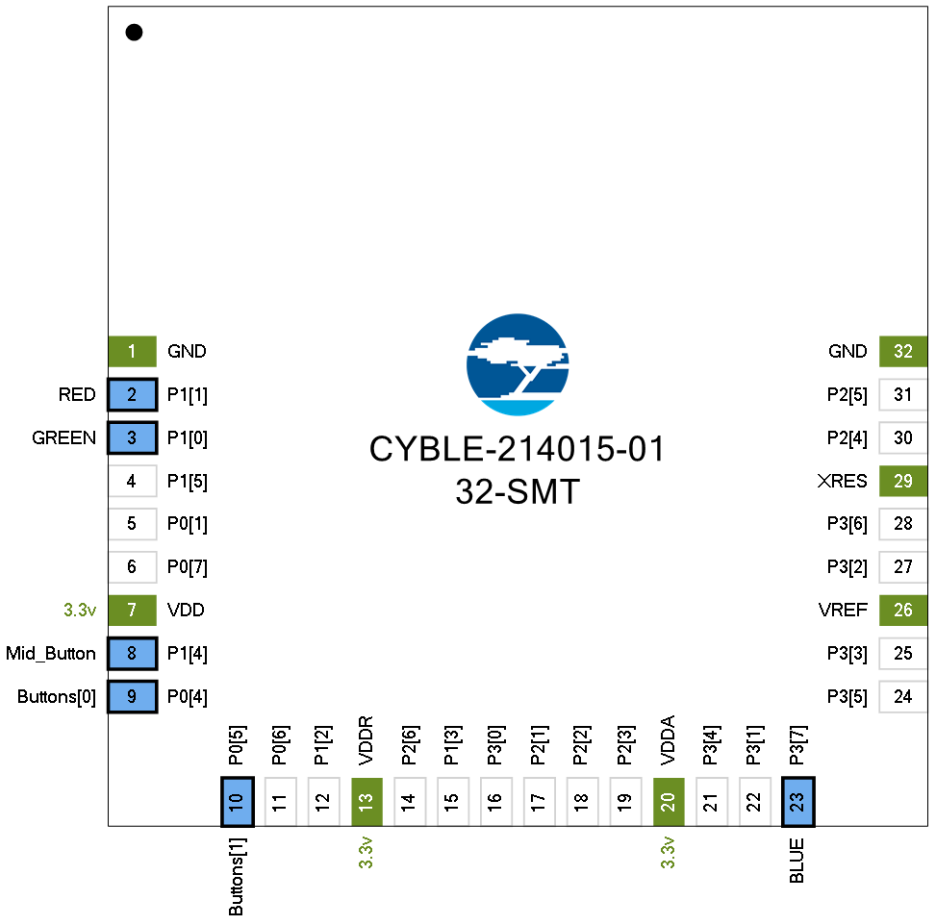
Table 2. Device Resources

Resource Type	Used	Free	Max	% Used
Digital Clocks	0	4	4	0.00 %
Interrupts	3	29	32	9.38 %
IO	6	21	27	22.22 %
Segment LCD	0	1	1	0.00 %
CapSense	0	1	1	0.00 %
Die Temp	0	1	1	0.00 %
Serial Communication (SCB)	0	2	2	0.00 %
BLE	1	0	1	100.00 %
DMA Channels	0	8	8	0.00 %
Timer/Counter/PWM	0	4	4	0.00 %
UDB				
Macrocells	0	32	32	0.00 %
Unique P-terms	0	64	64	0.00 %
Total P-terms	0			
Datapath Cells	0	4	4	0.00 %
Status Cells	0	4	4	0.00 %
Control Cells	0	4	4	0.00 %
Comparator/Opamp	0	4	4	0.00 %
LP Comparator	0	1	1	0.00 %
SAR ADC	0	1	1	0.00 %
DAC				
7-bit IDAC	0	1	1	0.00 %
8-bit IDAC	0	1	1	0.00 %

2 Pins

Figure 2 shows the pin layout of this device.

Figure 2. Device Pin Layout



2.1 Hardware Pins

Table 3 contains information about the pins on this device in device pin order. (No connection ["n/c"] pins have been omitted.)

Table 3. Device Pins

Pin	Port	Name	Type	Drive Mode
6	GND	GND	Power	
15	P0[5]	Buttons[1]	Software In/Out	Res pull up
16	P0[6]	GPIO [unused]		
17	P1[2]	GPIO [unused]		
18	VDDR	VDDR	Power	
19	P2[6]	GPIO [unused]		
20	P1[3]	GPIO [unused]		
21	P3[0]	GPIO [unused]		
22	P2[1]	GPIO [unused]		
23	P2[2]	GPIO [unused]		
24	P2[3]	GPIO [unused]		
7	P1[1]	RED	Software In/Out	HiZ digital
25	VDDA	VDDA	Power	
26	P3[4]	GPIO [unused]		
27	P3[1]	GPIO [unused]		
28	P3[7]	BLUE	Software In/Out	HiZ digital
29	P3[5]	GPIO [unused]		
30	P3[3]	GPIO [unused]		
31	VREF	VREF	Dedicated	
32	P3[2]	GPIO [unused]		
33	P3[6]	GPIO [unused]		
34	XRES	XRES	Dedicated	
8	P1[0]	GREEN	Software In/Out	HiZ digital
35	P2[4]	GPIO [unused]		
36	P2[5]	GPIO [unused]		
37	GND	GND	Power	
196	C_MOD	GPIO [unused]		
197	C_SH	GPIO [unused]		
9	P1[5]	GPIO [unused]		
10	P0[1]	GPIO [unused]		
11	P0[7]	GPIO [unused]		
12	VDD	VDD	Power	
13	P1[4]	Mid_Button	Software In/Out	Res pull up
14	P0[4]	Buttons[0]	Software In/Out	Res pull up

Abbreviations used in Table 3 have the following meanings:

- Res pull up = Resistive pull up
- HiZ digital = High impedance digital

2.2 Hardware Ports

Table 4 contains information about the pins on this device in device port order. (No connection ["n/c"], power and dedicated pins have been omitted.)

Table 4. Device Ports

Port	Pin	Name	Type	Drive Mode
C_MOD	196	GPIO [unused]		
C_SH	197	GPIO [unused]		
P0[1]	10	GPIO [unused]		
P0[4]	14	Buttons[0]	Software In/Out	Res pull up
P0[5]	15	Buttons[1]	Software In/Out	Res pull up
P0[6]	16	GPIO [unused]		
P0[7]	11	GPIO [unused]		
P1[0]	8	GREEN	Software In/Out	HiZ digital
P1[1]	7	RED	Software In/Out	HiZ digital
P1[2]	17	GPIO [unused]		
P1[3]	20	GPIO [unused]		
P1[4]	13	Mid_Button	Software In/Out	Res pull up
P1[5]	9	GPIO [unused]		
P2[1]	22	GPIO [unused]		
P2[2]	23	GPIO [unused]		
P2[3]	24	GPIO [unused]		
P2[4]	35	GPIO [unused]		
P2[5]	36	GPIO [unused]		
P2[6]	19	GPIO [unused]		
P3[0]	21	GPIO [unused]		
P3[1]	27	GPIO [unused]		
P3[2]	32	GPIO [unused]		
P3[3]	30	GPIO [unused]		
P3[4]	26	GPIO [unused]		
P3[5]	29	GPIO [unused]		
P3[6]	33	GPIO [unused]		
P3[7]	28	BLUE	Software In/Out	HiZ digital

Abbreviations used in Table 4 have the following meanings:

- Res pull up = Resistive pull up
- HiZ digital = High impedance digital

2.3 Software Pins

Table 5 contains information about the software pins on this device in alphabetical order. (Only software-accessible pins are shown.)

Table 5. Software Pins

Name	Port	Type
BLUE	P3[7]	Software In/Out
Buttons[0]	P0[4]	Software In/Out
Buttons[1]	P0[5]	Software In/Out
GPIO [unused]	P2[5]	
GPIO [unused]	P3[6]	
GPIO [unused]	P3[3]	
GPIO [unused]	P3[5]	
GPIO [unused]	P3[2]	
GPIO [unused]	P1[5]	
GPIO [unused]	P0[1]	
GPIO [unused]	P0[7]	
GPIO [unused]	P2[4]	
GPIO [unused]	C_MOD	
GPIO [unused]	C_SH	
GPIO [unused]	P1[3]	
GPIO [unused]	P3[0]	
GPIO [unused]	P2[1]	
GPIO [unused]	P0[6]	
GPIO [unused]	P1[2]	
GPIO [unused]	P2[6]	
GPIO [unused]	P2[3]	
GPIO [unused]	P3[1]	
GPIO [unused]	P3[4]	
GPIO [unused]	P2[2]	
GREEN	P1[0]	Software In/Out
Mid_Button	P1[4]	Software In/Out
RED	P1[1]	Software In/Out

For more information on reading, writing and configuring pins, please refer to:

- Pins chapter in the System Reference Guide
  - o CyPins API routines
- Programming Application Interface section in the cy_pins component datasheet

3 System Settings

3.1 System Configuration

Table 6. System Configuration Settings

Name	Value
Device Configuration Mode	Compressed
Unused Bonded IO	Allow but warn
Heap Size (bytes)	0x00
Stack Size (bytes)	0x0800
Include CMSIS Core Peripheral Library Files	True

3.2 System Debug Settings

Table 7. System Debug Settings

Name	Value
Debug Select	GPIO
Chip Protection	Open

3.3 System Operating Conditions

Table 8. System Operating Conditions

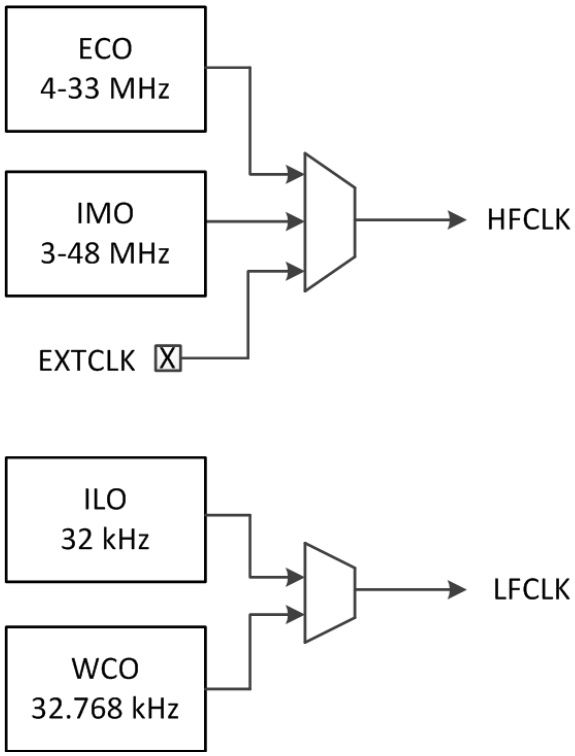
Name	Value
VDD (V)	3.3
VDDA (V)	3.3
VDDR (V)	3.3
Variable VDDA	True

4 Clocks

The clock system includes these clock resources:

- Four internal clock sources:
  - 3 to 48 MHz Internal Main Oscillator (IMO) ±2% at 3 MHz
  - 4 to 33 MHz External Crystal Oscillator (ECO)
  - 32 kHz Internal Low Speed Oscillator (ILO) output
  - 32.768 kHz Watch Crystal Oscillator (ILO) output
- HFCLK can be generated using an external signal from EXTCLK pin
- Twelve clock dividers, each with 16-bit divide capability:
  - Eight can be used for fixed-function blocks
  - Four can be used for the UDBs

Figure 3. System Clock Configuration



4.1 System Clocks

Table 9 lists the system clocks used in this design.

Table 9. System Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
ECO	NONE		24 MHz	24 MHz	±0	True	True
SYSCLK	NONE	HFCLK	? MHz	12 MHz	±2	True	True
DBL_Sel	NONE	IMO	12 MHz	12 MHz	±2	True	True
PLL_Sel	NONE	IMO	12 MHz	12 MHz	±2	True	True
Direct_Sel	NONE	IMO	12 MHz	12 MHz	±2	True	True
HFCLK	NONE	Direct_Sel	12 MHz	12 MHz	±2	True	True
IMO	NONE		12 MHz	12 MHz	±2	True	True
LFCLK	NONE	WCO	? MHz	32.768 kHz	±0	True	True
WCO	NONE		32.768 kHz	32.768 kHz	±0	True	True
ILO	NONE		32 kHz	32 kHz	±60	True	True
Timer1 (WDT1)	NONE	LFCLK	? MHz	50.027 Hz	±0	False	True
RTC_Sel	NONE	None	? MHz	? MHz	±0	True	True
DigSig3	NONE		? MHz	? MHz	±0	False	False
DigSig4	NONE		? MHz	? MHz	±0	False	False
DigSig2	NONE		? MHz	? MHz	±0	False	False
DigSig1	NONE		? MHz	? MHz	±0	False	False
EXTCLK	NONE		24 MHz	? MHz	±0	False	False
Timer2 (WDT2)	NONE	LFClk	? MHz	? MHz	±0	False	False
Timer0 (WDT0)	NONE	LFClk	? MHz	? MHz	±0	False	False

4.2 Local and Design Wide Clocks

Local clocks drive individual analog and digital blocks. Design wide clocks are a user-defined optimization, where two or more analog or digital blocks that share a common clock profile (frequency, etc) can be driven from the same clock divider output source.

Figure 4. Local and Design Wide Clock Configuration

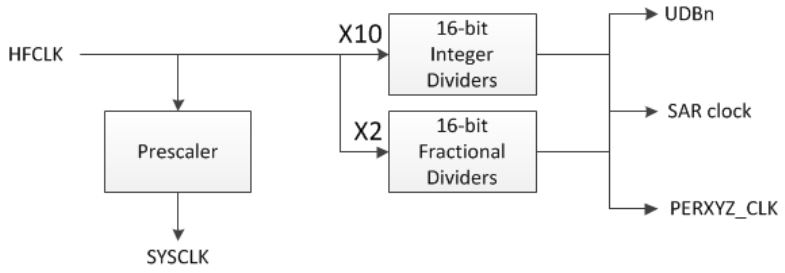


Table 10 lists the local clocks used in this design.

Table 10. Local Clocks

Name	Domain	Source	Desired Freq	Nominal Freq	Accuracy (%)	Start at Reset	Enabled
BLE_LFCLK	NONE	LFCLK	32.768 kHz	32.768 kHz	±0	True	True

For more information on clocking resources, please refer to:

- Clocking System chapter in the PSoC 4 Technical Reference Manual
- Clocking chapter in the System Reference Guide
  - CySysClkImo API routines
  - CySysClkIlo API routines
  - CySysClkEco API routines
  - CySysClkWco API routines
  - CySysClkWrite API routines

5 Interrupts and DMAs

5.1 Interrupts

This design contains the following interrupt components: (0 is the highest priority)

Table 11. Interrupts

Name	Intr Num	Vector	Priority
isr_buttons	0	0	3
isr_mid_button	1	1	3
BLE_bless_isr	12	12	2

For more information on interrupts, please refer to:

- Interrupt Controller chapter in the PSoC 4 Technical Reference Manual
- Interrupts chapter in the System Reference Guide
  - CyInt API routines and related registers
- Datasheet for cy_isr component

5.2 DMAs

This design contains no DMA components.

6 Flash Memory

PSoC 4 devices offer a host of Flash protection options and device security features that you can leverage to meet the security and protection requirements of an application. These requirements range from protecting configuration settings or Flash data to locking the entire device from external access.

Table 12 lists the Flash protection settings for your design.

Table 12. Flash Protection Settings

Start Address	End Address	Protection Level
0x0	0x3FFFF	U - Unprotected

Flash memory is organized as rows with each row of flash having 256 bytes. Each flash row can be assigned one of four protection levels:

- U - Unprotected
- W - Full Protection

For more information on Flash memory and protection, please refer to:

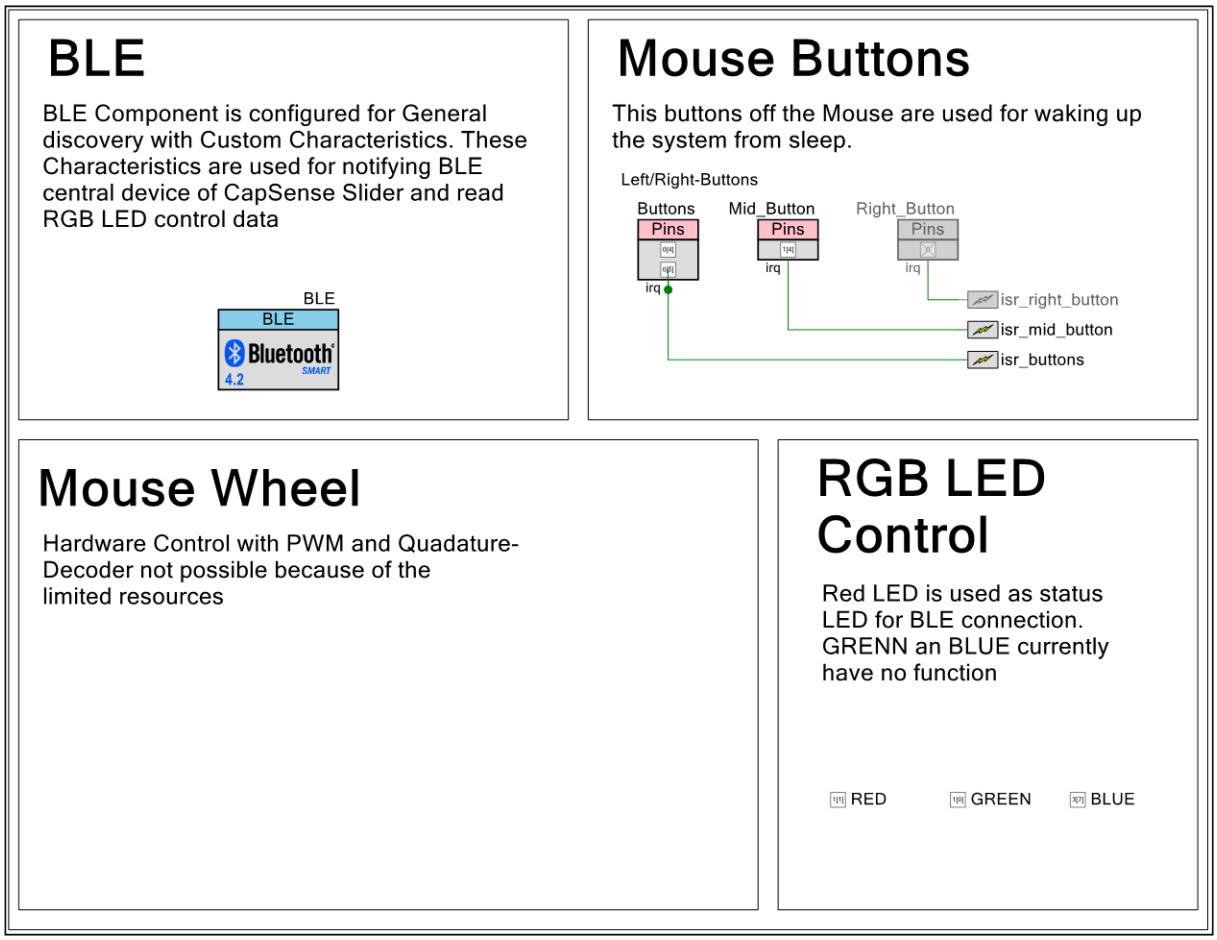
- Flash Protection chapter in the PSoC 4 Technical Reference Manual
- Flash and EEPROM chapter in the System Reference Guide
  - CySysFlash API routines

7 Design Contents

This design's schematic content consists of the following 2 schematic sheets:

7.1 Schematic Sheet: PSoC 4 BLE

Figure 5. Schematic Sheet: PSoC 4 BLE



This schematic sheet contains the following component instances:

- Instance BLE (type: BLE_v3_40)

7.2 Schematic Sheet: Page 1

Figure 6. Schematic Sheet: Page 1

8 Components

8.1 Component type: BLE [v3.40]

8.1.1 Instance BLE

Description: Bluetooth Low Energy (BLE)
Instance type: BLE [v3.40]
Datasheet: online component datasheet for BLE

Table 13. Component Parameters for BLE

Parameter Name	Value	Description
AutopopulateWhitelist	false	Provides an option to link the whitelist to the bonded device list.
EnableExternalPAcontrol	false	Enables external power amplifier control signal with align with internal PA on time. High active.
EnableExternalPrepWriteBuff	false	Enables application to provide dynamically allocated buffer for prepare write request. The buffer should be allocated and provided after CYBLE_EVT_-MEMORY_REQUEST event from stack.
EnableL2capLogicalChannels	true	Enables L2CAP logical channels support.
EnableLinkLayerPrivacy	false	Enables LL Privacy 1.2 feature of Bluetooth 4.2.
HalBaudRate	115200	UART baud rate
HalCtsEnable	true	In the HCI mode, the parameter enables the cts output in the UART.
HalCtsPolarity	Active Low	In the HCI mode, the parameter specifies the active polarity of the output cts signal of the UART.
HalRtsEnable	true	In the HCI mode, the parameter enables the rts output in the UART.
HalRtsPolarity	Active Low	In the HCI mode, the parameter specifies the active polarity of the output rts signal of the UART.
HalRtsTriggerLevel	4	In the HCI mode, the parameter specifies the number of entries in the RX FIFO to activate the rts output signal of the UART.
HciMode	UART	Defines the HCI interface.
ImportFilePath		The path to the file shared by another BLE component instance.

Parameter Name	Value	Description
KeypressNotifications	false	Provides an option for a keyboard-only device during the LE secure pairing process to send key press notifications when the user enters or deletes a key.
L2capMpsSize	23	The maximum size of payload data that the L2CAP layer is capable of accepting.
L2capMtuSize	23	The maximum SDU size of an L2CAP packet.
L2capNumChannels	1	The number of LE L2CAP connection oriented logical channels required by the application.
L2capNumPsm	1	The number of PSMs required by the application.
LLMaxRxPayloadSize	27	The maximum link layer receive payload size to be used in the design.
LLMaxTxPayloadSize	27	The maximum link layer transmit payload size to be used in the design.
MaxAttrNoOfBuffer	1	Number of buffers can be increased from 1 to 10 to achieve better throughput if attribute mtu > 32.
MaxBondedDevices	8	The maximum number of bonded devices to be supported by this device.
MaxResolvableDevices	8	The maximum number of peer devices whose addresses should be resolved by this device.
MaxWhitelistSize	8	The maximum number of devices that can be added to the whitelist.
Mode	Profile	Defines the component operating mode.
SharingMode	None	Defines if some parts of code are shared between two BLE components.
StackMode	Release	Determines the internal stack mode. Is used to switch the operation for debugging.
StrictPairing	false	Provides an option to use only the selected security features and doesn’t fallback to an unsecure connection if the peer device doesn’t support the selected security features.
UseDeepSleep	true	Indicates whether deep sleep mode is used.
User Comments		Instance-specific comments.

9 Other Resources

The following documents contain important information on Cypress software APIs that might be relevant to this design:

- Standard Types and Defines chapter in the System Reference Guide
  - Software base types
  - Hardware register types
  - Compiler defines
  - Cypress API return codes
  - Interrupt types and macros
- Registers
  - The full PSoC 4 register map is covered in the PSoC 4 Registers Technical Reference Manual
  - Register Access chapter in the System Reference Guide
    - CY_GET API routines
    - CY_SET API routines
- System Functions chapter in the System Reference Guide
  - General API routines
  - CyDelay API routines
  - CyVd Voltage Detect API routines
- Power Management
  - Power Supply and Monitoring chapter in the PSoC 4 Technical Reference Manual
  - Low Power Modes chapter in the PSoC 4 Technical Reference Manual
  - Power Management chapter in the System Reference Guide
    - CyPm API routines
- Watchdog Timer chapter in the System Reference Guide
  - CyWdt API routines