

**Digital Design and Computer Architecture LU**

# **Lab Protocol**

## **Exercise IV**

Group ?

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## Task 1: Forwarding Simulation

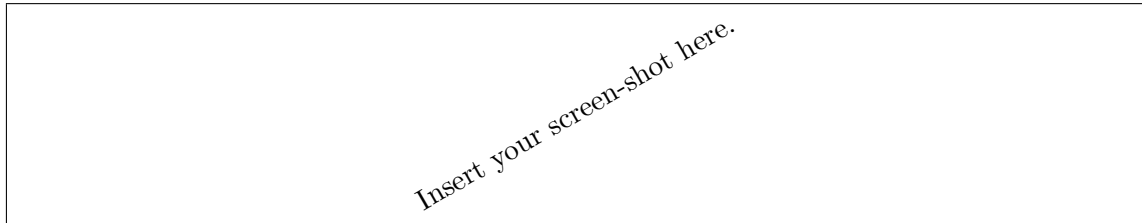


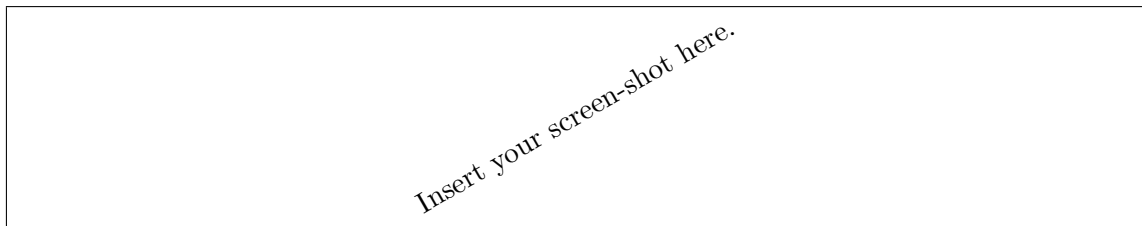
Figure 1: Simulation screenshot for Listing 1.

Make sure that at least the following signals are visible in Figure 1: the program counter in the fetch stage, the instruction being fetched, the content of registers `x1` and `x2` as well as the signals `wraddr`, `wrdata` and `regwrite` of the register file.

Listing 1: Assembler example with forwarding

```
addi x1, x0, 7
addi x2, x0, 5
and x1, x2, x1
nop
nop
```

## Task 2: Branch Hazards Simulation



clk	1
res_n	1
fetch	
stall	0
flush	0
pc_in	16'h0000
pcsrc	0
mem_in	0 (32'h03801000)
instr	32'h00108093
mem_busy	0
pc_out	16'h0004
mem_out	(14'h0002) 1 0 (4'hF) (32'h00000000)
decode	
stall	0
flush	0
instr	32'h00108093
pc_in	16'h0004
reg_write	0 (5'h00) (32'h00000000)
write	0
reg	5'h0
data	32'h00000000
exec_op	ALU_NOP 0 0 1 (5'h00) (5'h00)
aluop	ALU_NOP
alusr1	0
alusr2	0
alusr3	1
rs1	5'h0
rs2	5'h0
readdata1	32'h00000000
readdata2	32'h00000000
mem	32'h00000000
mem_op	BR_BR (0 0 MEM_W)
wb_op	(5'h00) 1 WBS_OPC
pc_out	16'h0000
exc_dec	0

Figure 2: Simulation screenshot for Listing 2.

Make sure that at least the following signals are visible in Figure 2: the program counter in the fetch stage, the instruction being fetched, the content of registers **x1**, **x2** and **x3** as well as the signals **wraddr**, **wrdata** and **regwrite** of the register file.

Listing 2: Assembler example for branches

```

loop:    j  loop
         addi x1, x1, 1
         addi x2, x2, 1
         addi x3, x3, 1

```

### Task 3: Synthesis Results

Table 1: Resource usage by entity, including resources used by sub-entities.

	LC Combinationals	LC Registers	Memory Bits
Fetch Stage			
Decode Stage			
– Register File			
Execute Stage			
– ALU			
Memory Stage			
– Memory Unit			
Write-Back Stage			
Forwarding Unit			
Control Unit			
Sum			

**Question:** What is the maximum frequency of your design?

**Answer:**

**Question:** Where is the critical path of your design?

**Answer:**

## **Task 4: Workflow**

Describe how you organized the work within the group on the way to the submission, i.e., summarize how you partitioned the work, which group member was (mainly) responsible for which subtask(s), how you organized testing and integration, how well your time plan worked, which re-adjustments needed to be done, and how well your collaboration worked.