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| --- | --- | --- | --- | --- | --- |
| Sl No. | Scenario | Expectation | Checks | Coverage | Coverage Intentions |
|  | **WRITES** | **Valid means when the reset is de-asserted** |  | Coverpoint Addr, coverpoint pwrite | All address covered |
| 1 | Valid Writes to address 0:511 | Mem0 with the same address is written with the value in pwdata and dut acknowledges with pready for the write |  | Cross paddr with pwrite | All address are written and read from |
| 2 | Valid Writes to address 512:767 | Mem1 with the same address is written with the value in pwdata and dut acknowledges with pready for the write |  | Coverpoint pwdata | All kinds of pwdata is written.  //It's a redundant as we are unable to cover a 32 bit data |
| 3 | Valid writes with value 'h55555555  And value 'haaaaaaaa,  Followed by read from that address | 'h5 is 'b0101 and 'ha is 'b1010, By writing these values a certain address we make sure all the bits of memory are working fine. |  | Coverpoint mem\_integrity- bins 'h55555555,'haaaaaaaa    Cross mem\_integrity with addr, pwrite |  |
|  | Valid Writes to invalid address outside 0:767 | Neither Mem0 or Mem1 is written to and the dut responds with pslverr assertion on pready assertion and pslverr is deasserted one clock cycle later |  | Coverpoint pslverr,  Cross pslverr with pwrite | Pslverr is covered.  Pslverr is covered for both reads and writes |
| 4 | Writes during Reset | Neither Mem0 or Mem1 is written, Dut doesn't acknowledge the reads or writes with assertion of pready, prdata or pslverr |  |  |  |
|  | **READS** |  |  |  |  |
| 5 | Valid Reads to address 0:511 | Dut returns data value with address from paddr from mem0 on pready | The value from prdata should match what is written to the same address. |  |  |
| 6 | Valid Reads to address 512:767 | Dut returns data value with address from paddr from mem1 on pready | The value from prdata should match what is written to the same address. |  |  |
| 7 | Valid Reads to invalid address outside 0:767 | Dut asserts pslverr on pready which is deassserted one clock cycle later. | SVA check to make sure pslverr is deasserted one clock cycle later when it is asserted | Coverpoint prdata | //It's a redundant as we are unable to cover a 32 bit data |
| 8 | Reads during Reset | No output from dut, no pslverr, no pready assertion. Data on prdata line is not to be trusted without pready | Memory checks to be performed to make sure all the memory are reset. |  |  |
|  | **PROTOCOL VIOLATION** |  |  |  |  |
|  |  | Penable to be asserted one clock cycle later when psel is asserted if not asserted previously | SVA check to make sure of this/ apb\_monitor check |  |  |
|  |  | Pslverr to be asserted for only one clock cycle and deasserted | SVA check to make sure pslverr is deasserted one clock cycle later when it is asserted |  |  |
|  | **MISC CHECK** |  |  |  |  |
|  |  |  | At the end of the simulation, The entire dut memory is checked against reference model implemented in the checker for mismatch |  |  |