INTERSIL

DATA BOOK

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Data Book

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INTRODUCTION

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Intersil, Inc. is a forward-integrated multi-technology company involved in the design, development, manufacture and marketing of large-scale integrated circuits, analog devices, microsystems, and systems for computers, computer-related equipment, and a wide range of other digital and analog applications.

The company produces analog and digital integrated circuits, using CMOS/LSI, MOS/LSI, low-power CMOS and bipolar LSI technologies. Applications and markets include data processing, industrial process control, portable and fixed instrumentation, RF and telecommunications and data acquisition, conversion and processing.

Our systems division is a major manufacturer of add-on memories for upgrading IBM's 303X series computers and the mid-sized 370 mainframes. This group manufactures a number of custom and standard microsystems and memory expansion boards for numerous micro and minicomputer applications.

Significant new semiconductor products introduced in 1979 include:

- VMOS Power FETs — A major breakthrough in power transistor technology, with ultra-fast 2 nanosecond switching times and direct digital logic drive. The product line includes 2 amp, 5 amp and 13 amp families with breakdowns to 400V for excellent linearity and reduced cost/size, for applications including pulse generator, power supply switching, and RF equipment.
- CMOS Multiplexers — One-of-16, 2-of-8, 1-of-8 and 2-of-4 single ended and differential analog multiplexers which feature very low power consumption and low error terms.
- CMOS Micropower Op Amps — A complete family of high-performance op amps - singles, duals, triples, and quads - which feature rail-to-rail and output voltage swings at V_S from ±0.5V to ±8.0V.
- ICL7112 Monolithic MOS D/A Converter — Employs laser trimming and absolute matrix positioning for improved performance at low cost.
- ICL7109 Monolithic 12-Bit A/D Converter — Specifically designed for direct interface with most popular microprocessors for data-logging operations.
- ICL7600/ICL7605 CAZ Amps — A family of revolutionary new ultra-stable operational and instrumentation amplifiers, in which a unique commutating auto-zero principle virtually eliminates V_{OS} and drift with temperature and time.
- ICM7217/ICM7227 Multipurpose Up/Down Counters — The first four-digit devices to incorporate five counting functions on a single chip.
- ICM7216/ICM7226 Microprocessor-Compatible Counters — A family of universal counter chips capable of dramatically improving the design and performance of portable and laboratory counting instrumentation.
- IM6653/IM6654 CMOS EPROMs — A series of ultraviolet erasable and reprogrammable 4K read-only memories.
- 2147 4K Static RAM — A random access memory chip featuring access times of less than 100 nanoseconds and employing Intersil's exclusive Selox™ fine-geometry process technology.
- IM87C48/87C41 8-bit Monolithic CMOS Microprocessors — Pin-and-function compatible with the NMOS 8748/8741 microprocessors, but which employ an advanced high-density technology for reduced power dissipation and improved noise linearity.

Intersil's full range of quality integrated circuits and discrete devices is available through a worldwide network of stocking distributors. Field sales offices are located in all major market areas of the United States and Canada to provide a high level of product support. A complete listing of these distributors, Sales Representatives and Company Sales Offices is included at the end of this publication.

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HOW TO USE THIS PUBLICATION

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BASE NUMBER INDEX

If you have only the basic part number of a device on which you seek further information, use the Base Number Index as a locator aid. The Base Number Index is organized in numeric-alpha sequence, with prefix letters appearing in bold type. Devices are arranged in this index according to the numeric value of the first digit on the left, then the value of the second digit, then the third, and so on. For example, device number ICM 7218 precedes ICL 741. No package/temperature/pin number suffixes are included, but may be obtained from the specific product data page to which you are directed.

CROSS-REFERENCE GUIDES

Two cross-reference guides are provided, including one for discrete devices and one for integrated circuits.

The discrete device cross reference indicates whether Intersil can provide the industry-standard type, or an Intersil-preferred part instead.

The IC alternate source cross-reference lists competitive manufacturer device types for which Intersil makes pin-for-pin replacements. In the left-hand column, the competitive device part number is organized alphabetically by manufacturer. The Intersil pin-for-pin replacement appears in the right-hand column.

FUNCTIONAL INDEX

Provides an index of Intersil device types categorized by product grouping and function. The first major subsection, DISCRETES, is further subdivided into categories for JFETs, MOSFETs and special function devices. VMOS, the next major subsection, is arranged according to device characteristics for $r_{DS(ON)}$. All remaining major subsections (ANALOG SWITCHES/MULTIPLEXERS, DATA ACQUISITION, LINEAR, TIMERS/COUNTERS, MEMORIES, MICROPROCESSORS/PERIPHERALS and DEVELOPMENT SYSTEMS) are organized alphabetically by function within each grouping. The Functional Index appears in its entirety in the front matter section of this publication, and an appropriate sub-index appears at the beginning of each major product subsection.

SELECTOR GUIDES

Selector guide tables appear at the front of each major product category subsection, and provide a quick-reference of key parameters for the devices contained in that section.

DEVICE FUNCTION/PACKAGE CODES

Diagrams which provide decoding information for device prefix and suffix codes are provided as rear matter material.

DIE SELECTION CRITERIA

Many of Intersil's semiconductor products are available in die form. This section contains general information on criteria for transistor and integrated circuit die selection, including physical parameters, packaging for shipment, assembly, testing, and purchase options.

HIGH-RELIABILITY PROCESSING

Defines Intersil's committment to 100 percent compliance with MIL-STD-883, MIL-STD-750, MIL-M-38510 and MIL-S-19500 specifications. Also outlines Intersil's programs for quality conformance, quality testing and limited use qualification, and includes a glossary of military/aerospace Hi-Rel terms.

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LF256	LF256
LF257	LF257
LF355	LF355
LF356	LF356
LF357	LF357
LH2301	LH2301
LH2311	LH2311
LM101	AD101
LM102	LM102
LM105	LM105
LM107	LM107
LM108	LM108
LM110	LM110
LM111	LM111
LM124	LM124
LM201	AD201
LM202	LM202
LM205	LM205
LM207	LM207
LM208	LM208
LM210	LM210
LM211	LM211
LM224	LM224
LM301	AD301
LM302	LM302
LM305	LM305
LM307	LM307
LM308	LM308
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μA556	NE556
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LF257	LF257
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LF356	LF356
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LM107	LM107
LM110	LM110
LM111	LM111
LM124	LM124
LM201	AD201
LM205	LM205
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LM210	LM210
LM211	LM211
LM224	LM224
LM301	AD301
LM305	LM305
LM307	LM307
LM308	LM308
LM310	LM310
LM311	LM311
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LF156	LF156
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LF256	LF256
LF257	LF257
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LH2108	LH2108
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LH2111	LH2111
LH2301	LH2301
LH2308	LH2308
LH2310	LH2310
LH2311	LH2311
LM100	LM100
LM101	AD101
LM102	LM102
LM105	LM105
LM107	LM107
LM108	LM108
LM110	LM110
LM111	LM111
LM124	LM124
LM200	LM200
LM201	AD201
LM202	LM202
LM205	LM205
LM207	LM207
LM208	LM208
LM210	LM210
LM211	LM211
LM224	LM224
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LM301	AD301
LM302	LM302
LM305	LM305
LM307	LM307
LM308	LM308
LM310	LM310
LM311	LM311
LM4250	LM4250
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LM556	NE556
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PM255	LF255
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LF156	LF156
LF157	LF157
LF255	LF255
LF256	LF256
LF257	LF257
LF355	LF355
LF356	LF356
LF357	LF357
LH2101	LH2101
LH2301	LH2301
LH2311	LH2311
LM101	AD101
LM105	LM105
LM107	LM107
LM108	LM108
LM124	LM124
LM201	AD201
LM205	LM205
LM207	LM207
LM208	LM208
LM211	LM211
LM224	LM224
LM2902	LM2902
LM301	AD301
LM305	LM305
LM307	LM307
LM308	LM308
LM311	LM311
LM324	LM324
RC555	NE555
RC556	NE556
RC723	LM723
RC733	μA733
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RC748	LM748
RM723	LM723
RM741	ICL741
RM748	LM748
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RCA	Intersil
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CA107	LM107
CA111	LM111
CA124	LM124
CA201	AD201
CA207	LM207
CA208	LM208
CA211	LM211
CA224	LM224
CA301	AD301
CA307	LM307
CA308	LM308
CA311	LM311
CA324	LM324
CA555	NE555
CA723	LM723
CA741	ICL741
CA748	LM748
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Signetics	Intersil
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μA733	μA733
μ740	LM740
μA741	μA741
μA748	LM748
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LF156	LF156
LF157	LF157
LF255	LF255
LF256	LF256
LF257	LF257
LF355	LF355
LF356	LF356
LF357	LF357
LH2101	LH2101
LH2108	LH2108
LH2301	LH2301
LH2308	LH2308
LH2311	LH2311
LM101	AD101
LM107	LM107
LM111	LM111
LM124	LM124
LM201	AD201
LM207	LM207
LM224	LM224
LM2902	LM2902
LM301	AD301
LM307	LM307
LM308	LM308
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SG108	LM108
SG110	LM110
SG111	LM111
SG124	LM124
SG201	AD201
SG205	LM205
SG207	LM207
SG208	LM208
SG210	LM210
SG211	LM211
SG224	LM224
SG301	AD301
SG305	LM305
SG307	LM307
SG308	LM308
SG311	LM311
SG324	LM324
SG3302	MC3302
SG4250	LM4250
SG555	NE555
SG556	NE556
SG723	LM723
SG733	μA733
SG741	ICL741
SG748	LM748

Siliconix	Intersil
DG111	DG111
DG116	DG116
DG123	DG123
DG125	DG125
DG126	DG126
	DG426
DG129	DG129
DG133	DG133
DG134	DG134
DG139	DG139
DG140	DG140
DG141	DG141
DG142	DG142
DG143	DG143
DG144	DG144
DG145	DG145
DG146	DG146
DG151	DG151
DG152	DG152
DG153	DG153
DG154	DG154
DG161	DG161
DG162	DG162
DG163	DG163
DG164	DG464
DG172	DG118
DG180	DG180
DG181	IH5048
DG181	DG181
DG182	DG182
DG183	DG183
DG184	DG184
	IH5049
DG185	DG185
DG186	DG186
DG187	DG187
	IH5050
DG188	DG188
DG189	DG189
DG190	DG190
	IH5051
DG191	DG191
D123	D123
D125	D125
G115	G115
G116	G116
G117	G117
G118	G118
G119	G119
G123	G123
G125	G125
G126	G126
G127	G127
G128	G128
G129	G129
G130	G130
G131	G131
G132	G132
LD110	LD110
LD111	LD111
LD114	LD114
SI452	MM452
SI455	MM455
SI552	MM552
SI555	MM555

Synertek	Intersil
SY2114	IM7114

TI	Intersil
μA723	LM723
μA733	μA733
μ741	μA741
μA748	LM748
μA777	μA777
LF155	LF155
LF156	LF156
LF157	LF157
LF255	LF255
LF256	LF256
LF257	LF257
LF355	LF355
LF356	LF356
LF357	LF357
LM101	AD101
LM105	LM105
LM107	LM107
LM111	LM111
LM124	LM124
LM201	AD201
LM224	LM224
LM2902	LM2902
LM301	AD301
LM305	LM305
LM307	LM307
LM311	LM311
LM324	LM324
NE555	NE555
NE556	NE556
SN54S188	IM5600
SN54S287	IM5623
SN54S288	IM5610
SN54S387	IM5603
SN54S474	IM5625
SN54S475	IM5605
SN74S188	IM5600
SN74S287	IM5623
SN74S288	IM5610
SN74S387	IM5603
SN74S474	IM5625
SN74S475	IM5605
TMS4027	IM7027
	MK4027
TMS4044	IM7141
TMS4045	IM7114
TMS4116	IM4116

Zilog	Intersil
Z6116	IM4116

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INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
100S	2N5458	233S	2N3956	2N3044	IT122
100U	2N3684	234S	2N3957	2N3045	IT122
102M	2N5686	235S	2N3958	2N3046	IT121
102S	2N5457	241U	2N4869	2N3047	IT122
103M	2N5457	250U	2N4091	2N3048	IT122
103S	2N5459	251U	2N4392	2N3066	2N4340
104M	2N5458	2N2060	IT120	2N3067	2N4338
105M	2N5459	2N2060A	IT121	2N3068	2N4338
105U	2N5222	2N2223	IT122	2N3069	2N4341
105U	2N4340	2N2223A	IT121	2N3070	2N4339
106M	2N5485	2N2386	2N2608	2N3071	2N4338
107M	2N5485	2N2386A	2N2608	2N3084	2N4339
110U	2N3685	2N2453	2N2453	2N3085	2N4339
120U	2N3686	2N2453A	2N2453A	2N3086	2N4339
125U	2N4339	2N2480	IT122	2N3087	2N4339
1277A	2N3822	2N2480A	IT121	2N3088	2N4339
1278A	2N3821	2N2497	2N2608	2N3088A	2N4339
1279A	2N3821	2N2498	2N2608	2N3089	2N4339
1280A	2N4224	2N2499	2N2609	2N3089A	2N4339
1281A	2N3822	2N2500	2N2608	2N3113	2N2607
1282A	2N4341	2N2606	2N2606	2N3277	2N2606
1283A	2N4340	2N2607	2N2607	2N3278	2N2607
1284A	2N4222	2N2608	2N2608	2N3328	2N5265
1285A	2N3821	2N2609	2N2609	2N3329	2N3329
1286A	2N4220	2N2609JANTX	2N2609JANTX	2N3330	2N3330
130U	2N3687	2N2639	IT120	2N3331	2N3331
1325A	2N4222	2N2640	IT122	2N3332	2N3330
135U	2N4339	2N2641	IT122	2N3347	IT137
14T	2N4224	2N2642	IT120	2N3348	IT138
155U	2N4416	2N2643	IT122	2N3349	IT139
1714A	2N4340	2N2644	IT122	2N3350	IT137
182S	2N4391	2N2652	IT120	2N3351	IT138
183S	2N3823	2N2652A	IT120	2N3352	IT139
197S	2N4338	2N2720	IT120	2N3365	2N4340
198S	2N4340	2N2721	IT122	2N3366	2N4338
199S	2N4341	2N2722	IT120	2N3367	2N4338
2000M	2N3823	2N2841	2N2607	2N3368	2N4341
2001M	2N3823	2N2842	2N2607	2N3369	2N4339
200S	2N4392	2N2843	2N2607	2N3370	2N4338
200U	2N3824	2N2844	2N2607	2N3376	2N3329
201S	2N4391	2N2903	IT122	2N3378	2N3330
202S	2N4392	2N2903A	IT120	2N3380	2N3331
203S	2N3821	2N2913	IT122	2N3382	2N3994
204S	2N3821	2N2914	IT120	2N3384	2N3992
2078A	2N3955	2N2915	IT120	2N3386	2N3386
2079A	2N3955	2N2915A	IT120	2N3425	IT122
2080A	2N3955A	2N2916	IT120	2N3436	2N4341
2081A	2N3955A	2N2916A	IT120	2N3437	2N4340
2093M	2N3687	2N2917	IT122	2N3438	2N4338
2094M	2N3686	2N2918	IT122	2N3452	2N4220
2095M	2N3686	2N2919	IT120	2N3453	2N4338
2098A	2N3954	2N2919A	IT120	2N3454	2N4338
2099A	2N3955A	2N2920	2N2920	2N3455	2N4340
210U	2N4416	2N2920A	2N2920A	2N3456	2N4338
2130U	2N5452	2N2936	IT120	2N3457	2N4338
2132U	2N3955	2N2937	IT120	2N3458	2N4341
2134U	2N3956	2N2972	IT122	2N3459	2N4339
2136U	2N3957	2N2973	IT122	2N3460	2N4338
2138U	2N3958	2N2974	IT120	2N3574	2N5265
2139U	2N3958	2N2975	IT120	2N3575	2N5265
2147U	2N3958	2N2976	IT120	2N3578	2N2608
2148U	2N3958	2N2977	IT120	2N3608	3N172
2149U	2N3958	2N2978	IT120	2N3680	IT120
231S	2N3954	2N2979	IT120	2N3684	2N3684
232S	2N3955	2N3043	IT121	2N3684A	2N3684

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INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
2N3685	2N3685	2N4018	IT139	2N4856JANTX	2N4856JANTX
2N3685A	2N3685	2N4019	IT139	2N4857	2N4857
2N3686	2N3686	2N4020	IT139	2N4857A	2N4857A
2N3686A	2N3686	2N4021	IT139	2N4857JANTX	2N4857JANTX
2N3687	2N3687	2N4022	IT139	2N4858	2N4858
2N3687A	2N3687	2N4023	IT137	2N4858A	2N4858A
2N3726	IT131	2N4024	IT137	2N4858JANTX	2N4858JANTX
2N3727	IT130	2N4025	IT137	2N4859	2N4860
2N3800	IT132	2N4026	3N163	2N4859A	2N4860
2N3801	IT132	2N4066	3N166	2N4859JANTX	2N4860JANTX
2N3802	IT132	2N4067	3N166	2N4860	2N4857
2N3803	IT132	2N4082	SU2366	2N4860A	2N4857A
2N3804	IT130	2N4083	SU2368	2N4860JANTX	2N4857JANTX
2N3804A	IT130A	2N4084	2N3954	2N4861	2N4858
2N3805	IT130	2N4085	2N3955	2N4861A	2N4858A
2N3805A	IT130A	2N4091	2N4091	2N4861JANTX	2N4858JANTX
2N3806	2N3806	2N4091A	2N4091	2N4867	2N4867
2N3807	2N3807	2N4091JANTX	2N4091JANTX	2N4867A	2N4867A
2N3808	2N3808	2N4092	2N4092	2N4868	2N4868
2N3809	2N3809	2N4092A	2N4092	2N4868A	2N4868A
2N3810	2N3810	2N4092JANTX	2N4092JANTX	2N4869	2N4869
2N3810A	2N3810A	2N4093	2N4093	2N4869A	2N4869A
2N3811	2N3811	2N4093A	2N4093	2N4878	2N4878
2N3811A	2N3811A	2N4093JANTX	2N4093JANTX	2N4879	2N4879
2N3812	IT132	2N4100	2N4100	2N4880	2N4880
2N3814	IT132	2N4117	2N4117	2N4937	IT131
2N3815	IT132	2N4117A	2N4117A	2N4938	IT132
2N3816	IT130	2N4118	2N4118	2N4939	IT132
2N3816A	IT130A	2N4118A	2N4118A	2N4940	IT132
2N3817	IT130	2N4119	2N4119	2N4941	IT131
2N3817A	IT130A	2N4119A	2N4119A	2N4942	IT132
2N3819	2N5484	2N4120	3N163	2N4955	IT122
2N3820	2N2608	2N4139	2N3822	2N4956	IT122
2N3821	2N3821	2N4220	2N4220	2N4977	2N5433
2N3821JANTX	2N3821JANTX	2N4220A	2N4220A	2N4978	2N5433
2N3822	2N3822	2N4221	2N4221	2N4979	2N4859
2N3823	2N3823	2N4221A	2N4221A	2N5018	2N5114
2N3823JANTX	2N3823JANTX	2N4222	2N4222	2N5019	2N5115
2N3824	2N3824	2N4222A	2N4222A	2N5020	2N2843
2N3838	IT122	2N4223	2N4223	2N5021	2N2607
2N3907	IT120	2N4224	2N4224	2N5033	2N5460
2N3908	IT120	2N4267	3N163	2N5045	2N5453
2N3909	2N3331	2N4268	3N160	2N5046	2N5454
2N3909A	2N3331	2N4302	2N5457	2N5047	2N5454
2N3913	IT132	2N4303	2N5459	2N5078	2N5397
2N3921	2N3921	2N4304	2N5458	2N5103	2N4416
2N3922	2N3922	2N4338	2N4338	2N5104	2N4416
2N3954	2N3954	2N4339	2N4339	2N5105	2N4416
2N3954A	2N3954A	2N4340	2N4340	2N5114	2N5114
2N3955	2N3955	2N4341	2N4341	2N5114JANTX	2N5114JANTX
2N3955A	2N3955A	2N4342	2N5461	2N5115	2N5115
2N3956	2N3956	2N4343	2N5462	2N5115JANTX	2N5115JANTX
2N3957	2N3957	2N4351	2N4351	2N5116	2N5116
2N3958	2N3958	2N4352	3N163	2N5116JANTX	2N5116JANTX
2N3965A	2N3685	2N4353	3N172	2N5117	2N5117
2N3966	2N4416	2N4360	2N5460	2N5118	2N5118
2N3967	2N4221	2N4381	2N2609	2N5119	2N5119
2N3968	2N3685	2N4382	2N5115	2N5158	2N5434
2N3969	2N3686	2N4391	2N4391	2N5159	2N5433
2N3969A	2N3686	2N4392	2N4392	2N5163	2N3822
2N3970	2N3970	2N4393	2N4393	2N5196	2N5196
2N3971	2N3971	2N4416	2N4416	2N5197	2N5197
2N3972	2N3972	2N4416A	2N4416A	2N5198	2N5198
2N3993	2N3993	2N4417	2N4416	2N5199	2N5199
2N3993A	2N3993	2N4445	2N5432	2N5245	2N4416
2N3994	2N3994	2N4446	2N5434	2N5246	2N5484
2N3994A	2N3994	2N4447	2N5432	2N5247	2N5486
2N4015	IT139	2N4448	2N5434	2N5248	2N5486
2N4016	IT137	2N4856	2N4856	2N5254	IT132
2N4017	IT139	2N4856A	2N4856A	2N5255	IT132

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INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
2N5256	IT130	2N5561	2N5561	3N147	3N189
2N5257	2N5457	2N5562	2N5562	3N148	3N189
2N5258	2N5485	2N5563	2N5563	3N149	3N160
2N5258	2N5458	2N5564	2N5564	3N150	3N163
2N5259	2N5459	2N5565	2N5565	3N151	3N190
2N5265	2N5265	2N5566	2N5566	3N155	3N163
2N5266	2N5266	2N5592	2N3822	3N155A	3N163
2N5267	2N5267	2N5593	2N3822	3N156	3N163
2N5268	2N5268	2N5594	2N3822	3N156A	3N163
2N5269	2N5269	2N5638	2N5638	3N157	3N163
2N5270	2N5270	2N5639	2N5639	3N157A	3N163
2N5277	2N4341	2N5640	2N5640	3N158	3N163
2N5278	2N4341	2N5647	2N4117A	3N158A	3N163
2N5358	2N5358	2N5648	2N4117A	3N160	3N160
2N5359	2N5359	2N5649	2N4117A	3N161	3N161
2N5360	2N5360	2N5653	2N5638	3N163	3N163
2N5361	2N5361	2N5654	2N5639	3N164	3N164
2N5362	2N5362	2N5668	2N5484	3N165	3N165
2N5363	2N5363	2N5669	2N5485	3N166	3N166
2N5364	2N5364	2N5670	2N5486	3N167	3N161
2N5391	2N4867A	2N5793	IT129	3N168	3N161
2N5392	2N4868A	2N5794	IT129	3N169	3N169
2N5393	2N4869A	2N5795	IT139	3N170	3N170
2N5394	2N4869A	2N5796	IT139	3N171	3N171
2N5395	2N4869A	2N5797	2N2608	3N172	3N172
2N5396	2N4869A	2N5798	2N2608	3N173	3N173
2N5397	2N5397	2N5799	2N2608	3N174	3N163
2N5398	2N5398	2N5800	2N2608	3N175	3N169
2N5432	2N5432	2N5801	2N4393	3N176	3N170
2N5433	2N5433	2N5802	2N4393	3N177	3N171
2N5434	2N5434	2N5803	2N4392	3N178	3N172
2N5452	2N5452	2N5902	2N5902	3N179	3N172
2N5453	2N5453	2N5903	2N5903	3N180	3N172
2N5454	2N5454	2N5904	2N5904	3N181	3N161
2N5457	2N5457	2N5905	2N5905	3N182	3N161
2N5458	2N5458	2N5906	2N5906	3N183	3N161
2N5459	2N5459	2N5907	2N5907	3N188	3N188
2N5460	2N5460	2N5908	2N5908	3N189	3N189
2N5461	2N5461	2N5909	2N5909	3N190	3N190
2N5462	2N5462	2N5911	2N5911	3N191	3N191
2N5463	2N5463	2N5912	2N5912	42T	2N4392
2N5464	2N5464	2N5949	2N5486	588U	2N4416
2N5465	2N5465	2N5950	2N5486	58T	2N5457
2N5471	2N5265	2N5951	2N5486	59T	2N4416
2N5472	2N5265	2N5952	2N5484	703U	2N4220
2N5473	2N5265	2N5953	2N5484	704U	2N4220
2N5474	2N5265	2N6441	2N6441	705U	2N4224
2N5475	2N5265	2N6442	2N6442	707U	2N4860
2N5476	2N5266	2N6443	2N6443	714U	2N3822
2N5484	2N5484	2N6444	2N6444	734EU	2N4416
2N5485	2N5485	2N6445	2N6445	734U	2N5516
2N5486	2N5486	2N6446	2N6446	751U	2N4340
2N5515	2N5515	2N6447	2N6447	752U	2N4340
2N5516	2N5516	2N6448	2N6448	753U	2N4341
2N5517	2N5517	2N6451	U311	754U	2N4340
2N5518	2N5518	2N6452	U311	755U	2N4341
2N5519	2N5519	2N6453	U311	756U	2N4340
2N5520	2N5520	2N6454	U311	A192	2N4416
2N5521	2N5521	2N6483	2N6483	A5T3821	2N5484
2N5522	2N5522	2N6484	2N6484	A5T3822	2N5484
2N5523	2N5523	2N6485	2N6485	A5T3823	2N4416
2N5524	2N5524	2N6568	2N54321	A5T3824	2N4341
2N5545	2N3954	2N6656	2N6657	AD3954	2N3954
2N5546	2N3955A	2N6657	2N6657	AD3954A	2N3954A
2N5547	2N3955	2N6658	2N6658	AD3955	2N3955
2N5549	2N5492	2N6659	2N6660	AD3956	2N3956
2N5555	2N5555	2N6660	2N6660	AD3958	2N3958
2N5556	2N3685	2N6661	2N6661	AD5905	2N5905
2N5557	2N3684	3N145	3N163	AD5906	2N5906
2N5558	2N3684	3N146	3N163	AD5907	2N5907

INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
AD5908	2N5908	BFW11	2N3822	DN3066A	2N3821
AD5909	2N5909	BFW54	2N3822	DN3067A	2N4338
AD810	2N4878	BFW55	2N3822	DN3068A	2N4338
AD811	2N4878	BFW56	2N4860	DN3069A	2N3822
AD812	2N4878	BFW61	2N4224	DN3070A	2N3821
AD813	2N4878	BSV22	2N4416	DN3071A	2N4338
AD814	IT124	BSV78	2N4856A	DN3365A	2N4220
AD815	IT124	BSV79	2N4857A	DN3365B	2N4091
AD816	IT120A	BSV80	2N4858A	DN3366A	2N3686
AD820	IT132	C413N	2N5434	DN3366B	2N4091
AD821	IT130A	C6690	2N4341	DN3367A	2N3687
AD822	IT130A	C6691	2N4341	DN3367B	2N4091
AD830	2N5520	C6692	2N4339	DN3368A	2N4341
AD831	2N5521	C673	2N4341	DN3368B	2N4221
AD832	2N5522	C674	2N4341	DN3369A	2N4339
AD833	2N5523	C680	2N4338	DN3369B	2N4220
AD833A	2N5524	C680A	2N4338	DN3370A	2N4338
AD835	SU2365	C681	2N4338	DN3370B	2N4338
AD836	SU2366	C681A	2N4338	DN3436A	2N4341
AD837	SU2367	C682	2N4339	DN3436B	2N4222
AD838	SU2368	C682A	2N4339	DN3437A	2N4340
AD839	SU2369	C683	2N4339	DN3437B	2N4220
AD840	2N5520	C683A	2N4339	DN3438A	2N4338
AD841	2N5521	C684	2N4220	DN3438B	2N4339
AD842	2N5523	C684A	2N4220	DN3458A	2N4341
BC264	2N5458	C685	2N4220	DN3458B	2N4222
BC264A	2N5457	C685A	2N4220	DN3459A	2N4339
BC264B	2N5458	CM600	2N4092	DN3459B	2N4220
BC264C	2N5458	CM601	2N4091	DN3460A	2N4338
BC264D	2N4416	CM602	2N4091	DN3460B	2N4220
BD522	VN88AF	CM603	2N4091	DU4339	2N5397
BF244	2N5486	CM640	2N4093	DU4340	2N5398
BF244A	2N5484	CM641	2N4093	E100	2N5458
BF244B	2N5485	CM642	2N4093	E101	2N4338
BF244C	2N5486	CM643	2N4092	E102	2N5457
BF245A	2N4416	CM644	2N4092	E103	2N5459
BF245B	2N4416	CM645	2N4092	E106	2N5433
BF245C	2N4416	CM646	2N4092	E107	2N5433
BF246	2N5639	CM647	2N4091	E108	2N5433
BF246A	2N5639	CM650	2N5432	E109	2N5433
BF246B	2N5638	CM651	2N5433	E110	2N5434
BF246C	2N5638	CM652	2N5432	E111	ITE4391
BF247	2N4091	CM653	2N5433	E111A	ITE4091
BF247A	2N4091	CM697	2N5433	E112	ITE4392
BF247B	2N4091	CM800	2N5433	E112A	ITE4092
BF247C	2N4091	CMX740	2N5432	E113	ITE4393
BF256A	2N5484	CP640	2N4091	E113A	ITE4093
BF256B	2N4416	CP643	2N5434	E114	2N5555
BF256C	2N4416	CP650	2N5432	E174	2N5114
BF320	2N5461	CP651	2N5433	E175	2N5115
BF348	2N5555	CP652	2N5433	E176	2N5116
BFR45	2N4416	CP653	2N5433	E201	2N4338
BFS21	2N5199	D1101	2N3821	E202	2N4340
BFS21A	2N5199	D1102	2N3821	E203	2N4341
BFS67	2N3821	D1103	2N4338	E204	2N4339
BFS67P	2N5459	D1177	2N3821	E210	2N5397
BFS68	2N3823	D1178	2N3821	E211	2N5397
BFS68P	2N4416	D1179	2N4338	E212	2N5397
BFS70	2N3821	D1180	2N3822	E230	2N4340
BFS71	2N3822	D1181	2N4338	E231	2N4341
BFS72	2N3823	D1182	2N4338	E232	2N4341
BFS73	2N3821	D1183	2N4341	E270	2N5116
BFS74	2N4856	D1184	2N4340	E271	2N5116
BFS75	2N4857	D1185	2N4339	E300	2N5397
BFS76	2N4858	D1201	2N4224	E304	2N5486
BFS77	2N4859	D1202	2N3821	E305	2N5484
BFS78	2N4860	D1203	2N5358	E308	U308/TO-92
BFS79	2N4861	D1301	2N4222	E309	U309/TO-92
BFS80	2N4416A	D1302	2N4220	E310	U310/TO-92
BFW10	2N3823	D1303	2N4220	E311	U311/TO-92

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INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
E312	2N5397	FM1210	2N3955A	IT501P	IT501P
E400	2N3955	FM1211	2N3958	IT502	IT502
E401	2N3955	FM3954	2N3954	IT502P	IT502P
E402	2N3957	FM3954A	2N3954A	IT503	IT503
E410	2N3955	FM3955	2N3955	IT503P	IT503P
E411	2N3958	FM3955A	2N3955A	IT5911	IT5911
E412	2N3958	FM3956	2N3956	IT5912	IT5912
E413	2N5454	FM3957	2N3957	ITC2972	IT122
E414	2N3956	FM3958	2N3958	ITC2973	IT122
E415	2N3957	FT0654A	2N5486	ITC2974	IT120
E420	IT5911	FT0654B	2N5486	ITC2975	IT120
E421	IT5912	FT0654C	2N4221	ITC2976	IT120
E430	2N5566	FT0654D	2N4221	ITC2977	IT120
E431	2N5566	FVN2	VN67AB	ITC2978	IT120
FE0654A	2N4386	GET5457	2N5457	ITC2979	IT120
FE0654B	2N5485	GET5458	2N5458	ITC3347	IT137
FE100	2N3821	GET5459	2N5459	ITC3348	IT138
FE100A	2N3821	HDIG1030	3N163	ITC3349	IT139
FE102	2N4119	ID100	ID100	ITC3350	IT137
FE102A	2N4119	ID101	ID101	ITC3351	IT138
FE104	2N4118	IMF3954	2N3954	ITC3352	IT139
FE104A	2N4118	IMF3954A	2N3954A	ITC3800	IT132
FE200	2N3821	IMF3955	2N3955	ITC3802	IT132
FE202	2N3821	IMF3955A	2N3955A	ITC3804	IT130
FE204	2N3821	IMF3956	2N3956	ITC3806	IT132
FE300	2N3822	IMF3957	2N3957	ITC3807	IT132
FE302	2N3821	IMF3958	2N3958	ITC3808	IT132
FE304	2N3821	IMF5564	IMF5564	ITC3809	IT132
FE5245	2N4416	IMF5565	IMF5565	ITC3810	IT130
FE5246	2N5484	IMF5566	IMF5566	ITC3811	IT130
FE5247	2N5486	IMF5911	IMF5911	ITC4017	IT139
FE5457	2N5457	IMF5912	IMF5912	ITC4018	IT139
FE5458	2N5458	IMF6485	IMF6485	ITC4019	IT139
FE5459	2N5459	IT100	IT100	ITC4020	IT139
FE5484	2N5484	IT101	IT101	ITC4021	IT139
FE5485	2N5485	IT108	IT108	ITC4022	IT139
FE5486	2N5486	IT109	IT109	ITC4023	IT137
FM1100	2N3954A	IT110	IT110	ITC4024	IT137
FM1100A	2N5906	IT111	IT111	ITC4025	IT137
FM1101A	2N5906	IT120	IT120	ITE2453	IT120
FM1102	2N3954	IT120A	IT120A	ITE2639	IT120
FM1102A	2N5906	IT121	IT121	ITE2640	IT122
FM1103	2N3955	IT122	IT122	ITE2641	IT122
FM1103A	2N5908	IT124	IT124	ITE2642	IT120
FM1104	2N3957	IT124A	IT124A	ITE2643	IT122
FM1104A	2N5909	IT124B	IT124B	ITE2644	IT122
FM1105	2N3954A	IT125	IT125	ITE2720	IT120
FM1105A	IT500	IT126	IT126	ITE2721	IT122
FM1106	2N3954A	IT127	IT127	ITE2722	IT120
FM1106A	IT500	IT128	IT128	ITE2903	IT122
FM1107	2N3954	IT129	IT129	ITE2913	IT122
FM1107A	IT500	IT130	IT130	ITE2914	IT122
FM1108	2N3955	IT130A	IT130A	ITE2915	IT120
FM1108A	IT502	IT131	IT131	ITE2916	IT120
FM1109	2N3957	IT132	IT132	ITE2917	IT122
FM1109A	IT503	IT136	IT136	ITE2918	IT122
FM1110	2N3955	IT137	IT137	ITE2919	IT120
FM1110A	2N5908	IT138	IT138	ITE2920	IT120
FM1111	2N3957	IT139	IT139	ITE2936	IT120
FM1111A	2N5909	IT1700	IT1700	ITE2937	IT120
FM1200	2N3954	IT1701	3N172	ITE2972	IT122
FM1201	2N3954	IT1702	3N163	ITE2973	IT122
FM1202	2N3954	IT1750	IT1750	ITE2974	IT120
FM1203	2N3955A	IT2700	3N165	ITE2975	IT120
FM1204	2N3955	IT2710	3N165	ITE2976	IT120
FM1205	2N3954	IT400	2N4392	ITE2977	IT120
FM1206	2N3954	IT404	IT404	ITE2978	IT120
FM1207	2N3954	IT500	IT500	ITE2979	IT120
FM1208	2N3955A	IT500P	IT500P	ITE3066	2N3685
FM1209	2N3955	IT501	IT501	ITE3067	2N3686

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INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
ITE3068	2N3687	IVN5201KND	IVN5201KND	J316	U309
ITE3347	IT137	IVN5201KNE	IVN5201KNE	J317	U310
ITE3348	IT138	IVN5201KNF	IVN5201KNF	J401	IT501P
ITE3349	IT139	IVN5201TND	IVN5201TND	J402	IT502P
ITE3350	IT137	IVN5201TNE	IVN5201TNE	J403	IT503P
ITE3351	IT138	IVN5201TNF	IVN5201TNF	J404	IT503P
ITE3680	IT120	J100	2N5458	J405	IT503P
ITE3800	IT132	J101	2N4338	J406	IT503P
ITE3802	IT132	J102	2N5457	J410	IT502P
ITE3804	IT130	J103	2N5459	J411	IT503P
ITE3806	IT132	J105	2N5433	J412	IT503P
ITE3807	IT132	J105-18	2N5433	J420	IT5911
ITE3808	IT132	J106	2N5433	J421	IT5912
ITE3809	IT132	J106-18	2N5433	J430	2N5566
ITE3810	IT130	J107	2N5433	J431	2N5566
ITE3811	IT130	J107-18	2N5433	K114-18	2N5555
ITE3907	IT120	J108	2N5433	K210-18	2N5397
ITE3908	IT120	J108-18	2N5433	K211-18	2N5397
ITE4017	IT139	J109	2N5433	K212-18	2N5397
ITE4018	IT139	J109-18	2N5433	K300-18	2N5397
ITE4019	IT139	J110	2N5433	K304-18	2N5486
ITE4020	IT139	J110-18	2N5433	K305-18	2N5484
ITE4021	IT139	J111	J111	K308-18	U308/TO-92
ITE4022	IT139	J111-18	J111	K309-18	U309/TO-92
ITE4023	IT137	J111A	J111	K310-18	U310/TO-92
ITE4024	IT137	J111A-18	J111	KE3684	2N3684
ITE4025	IT137	J112	J112	KE3685	2N3685
ITE4091	ITE4091	J112-18	J112	KE3686	2N3686
ITE4092	ITE4092	J112A	J112	KE3687	2N3687
ITE4093	ITE4093	J112A-18	J112	KE3823	2N3823
ITE4117	2N4117	J113	J113	KE3970	2N4391
ITE4118	2N4118	J113-18	J113	KE3971	2N4392
ITE4119	2N4119	J113A	J113	KE3972	2N4393
ITE4338	2N4338	J113A-18	J113	KE4091	ITE4091
ITE4339	2N4339	J114	2N5555	KE4092	ITE4092
ITE4340	2N4340	J1401	IT501P	KE4093	ITE4093
ITE4341	2N4341	J1402	IT502P	KE4220	2N5457
ITE4391	ITE4391	J1403	IT503P	KE4221	2N5459
ITE4392	ITE4392	J1404	IT503P	KE4222	2N5459
ITE4393	ITE4393	J1405	IT503P	KE4223	2N4223
ITE4416	ITE4416	J1406	IT503P	KE4391	ITE4391
ITE4867	2N4867	J174	J174	KE4392	ITE4392
ITE4868	2N4868	J174-18	J174	KE4393	ITE4393
ITE4869	2N4869	J175	J175	KE4416	ITE4416
IVN5000AND	IVN5000AND	J175-18	J175	KE4856	2N4391
IVN5000ANE	IVN5000ANE	J176	J176	KE4857	2N4392
IVN5000ANF	IVN5000ANF	J176-18	J176	KE4859	2N4391
IVN5000SND	IVN5000SND	J177	J177	KE4860	2N4392
IVN5000SNE	IVN5000SNE	J177-18	J177	KE4861	2N4393
IVN5000SNF	IVN5000SNF	J201	2N4338	KE5103	2N4221
IVN5001AND	IVN5001AND	J201-18	2N4338	KE5104	2N4416
IVN5001ANE	IVN5001ANE	J202	2N4340	KE5105	2N4416
IVN5001ANF	IVN5001ANF	J202-18	2N4340	KH5196	2N5196
IVN5001SND	IVN5001SND	J203	2N4341	KH5197	2N5197
IVN5001SNE	IVN5001SNE	J203-18	2N4341	KH5198	2N5198
IVN5001SNF	IVN5001SNF	J204	2N4339	KH5199	2N5199
IVN5200HND	IVN5200HND	J204-18	2N4339	LDF603	2N4221
IVN5200HNE	IVN5200HNE	J210	2N5397	LDF604	2N4221
IVN5200HNF	IVN5200HNF	J211	2N5397	LDF605	2N4221
IVN5200KND	IVN5200KND	J212	2N5397	LM114	LM114
IVN5200KNE	IVN5200KNE	J270	J270	LM114A	LM114A
IVN5200KNF	IVN5200KNF	J270-18	J270	LM114AH	LM114AH
IVN5200TND	IVN5200TND	J271	J271	LM114H	LM114H
IVN5200TNE	IVN5200TNE	J271-18	J271	LM115	LM115
IVN5201CND	IVN5201CND	J304	2N5486	LM115A	LM115A
IVN5201CNE	IVN5201CNE	J305	2N5484	LM115AH	LM115AH
IVN5201CNF	IVN5201CNF	J308	J308	LM115H	LM115H
IVN5201HND	IVN5201HND	J309	J309	LM194	LM194
IVN5201HNE	IVN5201HNE	J310	J310	LM394	LM394
IVN5201HNF	IVN5201HNF	J315	2N5397	M100	**

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INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
M101	••	MEM517	3N172	MP350	IT132
M103	3N161	MEM517A	3N172	MP351	IT130
M104	3N161	MEM517B	3N172	MP352	IT130
M106	3N166	MEM517C	3N172	MP358	IT130A
M107	3N189	MEM520	3N160	MP3954	2N3954
M108	3N191	MEM520C	3N164	MP3954A	2N3954A
M113	3N161	MEM550	3N189	MP3955	2N3955
M114	3N161	MEM550C	3N189	MP3956	2N3956
M116	M116	MEM550F	3N189	MP3958	2N3958
M117	2N4351	MEM551	3N190	MP5905	2N5905
M119	3N161	MEM551C	3N189	MP5906	2N5906
M163	3N163	MEM556	3N172	MP5907	2N5907
M164	3N164	MEM556C	3N172	MP5908	2N5908
M511	3N172	MEM560C	3N161	MP5909	2N5909
M511A	3N172	MEM561	3N163	MP5911	2N5911
M517	3N163	MEM561C	3N163	MP5912	2N5912
MD2974	IT120	MEM562	2N4351	MP804	2N5520
MD2975	IT120	MEM562C	2N4351	MP830	2N5520
MD2978	IT120	MEM563	2N4351	MP831	2N5521
MD2979	IT120	MEM563C	2N4351	MP832	2N5522
MD3008	IT120	MEM560	3N161	MP833	2N5523
MD8001	IT120	MEM806	3N163	MP835	SU2365
MD8002	IT120	MEM806A	3N163	MP836	SU2366
MEF103	2N5457	MEM807	3N172	MP837	SU2367
MEF104	2N5459	MEM807A	3N172	MP838	SU2368
MEF3069	2N4341	MEM814	3N161	MP839	SU2369
MEF3070	2N4339	MEM816	3N172	MP841	2N5521
MEF3458	2N4341	MFE2000	2N4416	MP842	2N5523
MEF3459	2N4339	MFE2001	2N4416	MPF102	2N5486
MEF3460	2N4338	MFE2004	2N4093	MPF103	2N5457
MEF3684	2N3684	MFE2005	2N4092	MPF104	2N5458
MEF3685	2N3685	MFE2006	2N4091	MPF105	2N5459
MEF3686	2N3686	MFE2007	2N4860	MPF106	2N5485
MEF3687	2N3687	MFE2008	2N4859	MPF107	2N5486
MEF3821	2N3821	MFE2009	2N4859	MPF108	2N5486
MEF3822	2N3822	MFE2010	2N4859	MPF109	2N5484
MEF3823	2N3823	MFE2011	2N5433	MPF111	2N5458
MEF3954	2N3954	MFE2093	2N4338	MPF112	2N5458
MEF3955	2N3955	MFE2094	2N4339	MPF161	2N5398
MEF3956	2N3956	MFE2095	2N4340	MPF4391	ITE4391
MEF3957	2N3957	MFE2912	2N5433	MPF4392	ITE4392
MEF3958	2N3958	MFE3002	3N169	MPF4393	ITE4393
MEF3959	2N3959	MFE3003	3N164	MPF820	U310/TO-92
MEF4223	2N4223	MFE3020	3N166	MPF970	2N5114
MEF4224	2N4224	MFE3021	3N166	MPF971	2N5115
MEF4391	ITE4391	MFE4007	2N3686	MTF103	2N5457
MEF4392	ITE4392	MFE4008	2N3686	MTF104	2N5459
MEF4393	ITE4393	MFE4009	2N3685	NDF9401	IT500
MEF4416	ITE4416	MFE4010	2N3330	NDF9402	IT501
MEF4856	2N4856	MFE4011	2N3330	NDF9403	IT502
MEF4857	2N4857	MFE4012	2N3331	NDF9404	IT503
MEF4858	2N4858	MFE590	SD306	NDF9405	IT503
MEF4859	2N4859	MFE591	SD300	NDF9406	IT500
MEF4860	2N4860	MFE823	MFE823	NDF9407	IT501
MEF4861	2N4861	MFE824	MFE824	NDF9408	IT502
MEF5103	ITE4416	MK10	2N4416	NDF9409	IT503
MEF5104	ITE4416	MMF1	2N5197	NDF9410	IT503
MEF5105	ITE4416	MMF2	2N3921	NF4302	2N5457
MEF5245	ITE4416	MMF3	2N5198	NF4303	2N5459
MEF5246	2N5484	MMF4	2N3922	NF4304	2N5458
MEF5247	2N5486	MMF5	2N5199	NF4445	2N5432
MEF5248	2N5486	MMF6	2N3955A	NF4446	2N5433
MEF5284	2N5484	MMT3823	2N3823	NF4447	2N5433
MEF5285	2N5485	MP301	IT124B	NF4448	2N5433
MEF5286	2N5486	MP302	IT125	NF500	2N4224
MEF5561	2N5561	MP303	IT124B	NF501	2N4224
MEF5562	2N5562	MP310	2N4045	NF506	2N4416
MEF5563	2N5563	MP311	2N4045	NF510	NF510
MEM511	3N172	MP312	2N4044	NF5101	2N4867
MEM511C	3N172	MP318	IT120A	NF5102	2N4867

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INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
NF5103	2N4867	SD306	SD306	TIS73	2N4391
NF511	2N4860	SDF1001	2N5432	TIS74	2N4392
NF5163	2N4341	SDF1002	2N5433	TIS75	2N4393
NF520	2N3684	SDF1003	2N5434	TIS88	2N4416
NF521	2N3685	SDF500	2N5520	TIS88A	2N4416
NF522	2N3686	SDF501	2N5520	TIXS33	2N4392
NF523	2N3865	SDF502	2N5520	TIXS41	2N4859
NF530	2N4341	SDF503	2N5520	TIXS42	2N5639
NF531	2N4339	SDF504	2N5520	TN4117	2N4117
NF532	2N4341	SDF505	2N5520	TN4117	2N4117
NF533	2N4339	SDF506	2N5520	TN4117A	2N4117A
NF5457	2N5457	SDF507	2N5520	TN4117A	2N4117A
NF5458	2N5458	SDF508	2N5520	TN4118	2N4118
NF5459	2N5459	SDF509	2N5520	TN4118	2N4118
NF5484	2N5484	SDF510	2N3954	TN4118A	2N4118A
NF5485	2N5485	SDF512	2N3954	TN4118A	2N4118A
NF5486	2N5486	SDF513	2N3954	TN4119	2N4119
NF5638	2N5638	SDF514	2N3954	TN4119	2N4119
NF5639	2N5638	SU2078	2N3955	TN4119A	2N4119A
NF5640	2N5640	SU2079	2N3955	TN4119A	2N4119A
NF5653	2N4860	SU2098	2N5197	TN4338	2N4338
NF5654	2N4861	SU2098A	2N5197	TN4339	2N4339
NF580	2N5432	SU2098B	2N5196	TN4340	2N4340
NF581	2N5432	SU2099	2N5197	TN4341	2N4341
NF582	2N5433	SU2099A	2N5197	TP5114	2N5114
NF583	2N5434	SU2365	SU2365	TP5115	2N5115
NF584	2N5433	SU2365A	SU2365A	TP5116	2N5116
NF585	2N4859	SU2366	SU2366	U110	2N2608
NPD5564	2N5564	SU2366A	SU2366A	U112	2N2608
NPD5565	2N5565	SU2367	SU2367	U1177	2N4220
NPD5566	2N5566	SU2367A	SU2367A	U1178	2N3821
NPD8301	2N3954	SU2368	SU2368	U1179	2N3821
NPD8302	2N3955	SU2368A	SU2368A	U1180	2N4221
NPD8303	2N3956	SU2369	SU2369	U1181	2N4220
P1069E	2N2609	SU2369A	SU2369A	U1182	2N3821
P1086E	2N5115	SU2410	2N5097	U1277	2N3684
P1087E	2N5516	SU2411	2N5908	U1278	2N3865
P1117E	2N5640	SU2412	2N5909	U1279	2N3686
P1118E	2N5641	TD5432	2N5432	U1280	2N3684
P1119E	2N5640	TD5433	2N5433	U1281	2N3822
PF5101	2N4867	TD5434	2N5434	U1282	2N4341
PF5102	2N4867	TD5902	2N5902	U1283	2N4340
PF5103	2N4867	TD5902A	2N5902	U1284	2N4341
PN3684	2N3684	TD5903	2N5903	U1285	2N4220
PN3685	2N3685	TD5903A	2N5903	U1286	2N4341
PN3686	2N3686	TD5904	2N5904	U1287	2N4092
PN3687	2N3687	TD5904A	2N5904	U1321	2N4860
PN4091	ITE4091	TD5905	2N5905	U1322	2N3822
PN4092	ITE4092	TD5905A	2N5905	U1323	2N3822
PN4093	ITE4093	TD5906	2N5906	U1324	2N3687
PN4220	2N4220	TD5906A	2N5906	U1325	2N3686
PN4221	2N4221	TD5907	2N5907	U133	2N2608
PN4222	2N4222	TD5907A	2N5907	U1420	2N3821
PN4223	2N4223	TD5908	2N5908	U1421	2N3822
PN4224	2N4224	TD5908A	2N5908	U1422	2N3822
PN4342	2N5461	TD5909	2N5909	U146	2N2608
PN4360	2N5460	TD5909A	2N5909	U147	2N2608
PN4391	ITE4391	TD5911	IT5911	U148	2N2608
PN4392	ITE4392	TD5911A	IT5911	U149	2N2609
PN4416	ITE4416	TD5912	IT5912	U168	2N2609
PN4856	2N4856	TD5912A	IT5912	U1714	2N4340
PN4857	2N4857	TIS14	2N4340	U182	2N4857
PN4858	2N4858	TIS15	2N3954	U183	2N3824
PN4859	2N4859	TIS26	2N3954	U1837E	2N5486
PN4860	2N4860	TIS27	2N3955	U184	2N5078
PN4861	2N4861	TIS41	2N4859	U1897E	U1897
PN5033	2N5460	TIS58	2N5484	U1898E	U1898
SD300	SD300	TIS59	2N5486	U1899E	U1899
SD301	SD301	TIS69	2N3955A	U197	2N4339
SD304	SD304	TIS70	2N3956	U198	2N4340

A

INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT	INDUSTRY STANDARD	NEAREST INTERSIL EQUIVALENT
U199	2N4341	U329	**	UC754	2N4340
U1994E	2N4416	U330	**	UC755	2N4341
U200	U200	U331	**	UC756	2N4340
U201	U201	U401	U401	UC805	2N3331
U202	U202	U402	U402	UC807	2N5115
U2047E	2N4416	U403	U403	UC814	2N3331
U221	2N4391	U404	U404	UC851	2N2608
U222	2N4391	U405	U405	UC853	2N2608
U231	U231	U406	U406	UC854	2N2608
U232	U232	U421	U421	UC855	2N2609
U233	U233	U422	U422	VCR10N	2N4869
U234	U234	U423	U423	VCR11N	2N3958
U235	U235	U424	U424	VCR12N	2N3958
U240	2N5432	U425	U425	VCR13N	2N3958
U241	2N5433	U426	U426	VCR20N	2N4341
U242	2N5432	U430	2N5566	VCR2N	VCR2N
U243	2N5433	U431	2N5566	VCR3P	VCR2P
U248	2N5902	UC100	2N3684	VCR4N	VCR4N
U248A	2N5906	UC110	2N3685	VCR5P	VCR5P
U249	2N4903	UC115	2N4340	VCR6P	VCR6P
U249A	2N5907	UC120	2N3686	VCR7N	VCR7N
U250	2N5904	UC130	2N3687	VMP1	**
U250A	2N5908	UC155	2N4416	VMP11	**
U251	2N5905	UC1700	3N163	VMP12	**
U251A	2N5909	UC1764	3N163	VMP2	**
U254	2N4859	UC20	2N3686	VMP21	**
U255	2N4860	UC200	2N3824	VMP22	**
U256	2N4861	UC201	2N3824	VMP4	**
U257	U257	UC21	2N3687	VN30AA	VN30AA
U257/TO-71	U257/TO-71	UC210	2N4416	VN30AB	VN30AB
U273	2N4118A	UC2130	2N5452	VN33AJ	VN35AJ
U273A	2N4118A	UC2132	2N5453	VN33AK	VN35AK
U274	2N4119A	UC2134	2N5454	VN35AA	VN35AA
U274A	2N4119A	UC2136	2N5454	VN35AB	VN35AB
U275	2N4119A	UC2138	2N5454	VN35AJ	VN35AJ
U275A	2N4119A	UC2139	2N3958	VN35AK	VN35AK
U280	2N5452	UC2147	2N3958	VN40AF	VN40AF
U281	2N5453	UC2148	2N3958	VN46AF	VN46AF
U282	2N5453	UC2149	2N3958	VN64GA	**
U283	2N5453	UC220	2N3822	VN66AF	VN66AF
U284	2N5454	UC240	2N4869	VN66AJ	VN66AJ
U285	2N5454	UC241	2N4869	VN66AK	VN66AK
U290	2N5432	UC250	2N4091	VN67AA	VN67AA
U291	2N5434	UC251	2N4392	VN67AB	VN67AB
U295	2N5432	UC2766	3N166	VN67AF	VN67AF
U296	2N5434	UC300	2N2608	VN67AJ	VN67AJ
U300	2N5114	UC310	2N2607	VN67AK	VN67AK
U3000	2N4341	UC320	2N2607	VN86HF	**
U3001	2N4339	UC330	2N2607	VN88AF	VN88AF
U3002	2N4338	UC340	2N2607	VN89AA	VN89AA
U301	2N5115	UC40	2N2608	VN89AB	VN89AB
U3010	2N4341	UC400	2N3331	VN89AF	VN89AF
U3011	2N4340	UC401	2N5116	VN90AA	VN90AA
U3012	2N4338	UC41	2N2608	VN90AB	VN90AB
U304	U304	UC410	2N3330	VN98AJ	VN98AJ
U305	U305	UC420	2N3329	VN98AK	VN98AK
U306	U306	UC450	2N5114	VN99AJ	VN99AJ
U308	U308	UC451	2N5116	VN99AK	VN99AK
U309	U309	UC588	2N4416	W245A	ITE4416
U310	U310	UC703	2N4220	W245B	ITE4416
U311	U311	UC704	2N4220	W245C	ITE4416
U312	2N5397	UC705	2N4224	W300	2N5398
U314	2N5555	UC707	2N4860	W300A	2N5397
U315	2N5397	UC714	2N3822	W300B	2N5397
U316	U309	UC714E	2N4341	W300C	2N5397
U317	U310	UC734	2N4416	W300D	2N5398
U320	2N5433	UC734E	2N4416	WK5457	2N5457
U321	2N5434	UC751	2N4340	WK5458	2N5458
U322	2N5433	UC752	2N4340	WK5459	2N5459
U328	**	UC753	2N4341		

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Switches—Junction FET

Ordering Information Preferred Part Number	Package	$r_{DS(on)}$ max ohm	V_P min/max V		I_{GSS} max pA	BV_{GSS} min V	$I_{D(off)}$ max pA	I_{DSS} min/max mA		t_{ap} max nS	C_{iss} max pf	C_{rss} max pf
N-channel: Generally requires driver circuit to translate the popular logic levels to voltages required to drive the JFET.												
2N3970	TO-18	30	−4.0	−10.0	—	−40	250	50	150	50	25	6.0
2N3971	TO-18	60	−2.0	−5.0	—	−40	250	25	75	90	25	6.0
2N3972	TO-18	100	−0.5	−3.0	—	−40	250	5	30	180	25	6.0
2N4091	TO-18 TO-92	30	−5.0	−10.0	−200	−40	200	30		65	16	5.0
2N4092	TO-18 TO-92	50	−2.0	−7.0	−200	−40	200	15		95	16	5.0
2N4093	TO-18 TO-92	80	−1.0	−5.0	−200	−40	200	8		140	16	5.0
2N4391	TO-18 TO-92	30	−4.0	−10.0	−100	−40	100	50	150	55	14	3.5
2N4392	TO-18 TO-92	60	−2.0	−5.0	−100	−40	100	25	75	75	14	3.5
2N4393	TO-18 TO-92	100	−0.5	−3.0	−100	−40	100	5	30	100	14	3.5
2N4856	TO-18	25	−4.0	−10.0	−250	−40	250	50		34	18	6.0
2N4857	TO-18	40	−2.0	−6.0	−250	−40	250	20	100	60	18	6.0
2N4858	TO-18	60	−0.8	−4.0	−250	−40	250	8	80	120	18	6.0
2N4859	TO-18 TO-92	25	−4.0	−10.0	−250	−30	250	50		34	18	8.0
2N4860	TO-18 TO-92	40	−2.0	−6.0	−250	−30	250	20	100	60	18	8.0
2N4861	TO-18 TO-92	60	−0.8	−4.0	−250	−30	250	8	80	120	18	8.0
2N5432	TO-52 TO-92	5	−4.0	−10.0	−200	−25	200	150		41	30	15.0
2N5433	TO-52 TO-92	7	−3.0	−9.0	−200	−25	200	100		41	30	15.0
2N5434	TO-52 TO-92	10	−1.0	−4.0	−200	−25	200	30		41	30	15.0
2N5555	TO-92	150		−10.0	−1 nA	−25	10 nA	15		35	5	1.2
2N5638	TO-92	30		−12.0	−1 nA	−30	1 nA	50		24	10	4.0
2N5639	TO-92	60		−8.0	−1 nA	−30	1 nA	25		54	10	4.0
2N5640	TO-92	100		−6.0	−1 nA	−30	1 nA	5		63	10	4.0
ITE4091	TO-18 TO-92	30	−5.0	−10.0	−200	−40	200	30		65	16	5.0
ITE4092	TO-18 TO-92	50	−2.0	−10.0	−200	−40	200	15		95	16	5.0
ITE4093	TO-18 TO-92	80	−1.0	−10.0	−200	−40	200	8		140	16	5.0
ITE4391	TO-18 TO-92	60	−4.0	−10.0	−100	−40	100	50	150	55	14	3.5
ITE4392	TO-18 TO-92	100	−2.0	−10.0	−100	−40	100	25	75	75	14	3.5
ITE4393	TO-18 TO-92	30	−0.5	−10.0	−100	−40	100	5	30	100	14	3.5
J111	TO-92	30	−3.0	−10.0	1 nA	35	1 nA	20		—	—	—
J112	TO-92	50	−1.0	−5.0	1 nA	35	1 nA	5		—	—	—
J113	TO-92	100	−0.5	−3.0	1 nA	35	1 nA	2		—	—	—
P-channel: Can be used to switch into inverting input of op-amps and needs no driver circuit; can be switched directly from TTL logic.												
2N3993	TO-72	150	4.0	9.5	1.2 nA	25	1.2 nA	−10			16	4.5
2N3994	TO-72	300	1.0	5.5	1.2 nA	25	1.2 nA	−2			16	4.5
2N5114	TO-18 TO-92	75	5.0	10.0	500	30	500	−30	−90	37	25	7.0
2N5115	TO-18 TO-92	100	3.0	6.0	500	30	500	−15	−60	68	25	7.0
2N5116	TO-18 TO-92	150	1.0	4.0	500	30	500	−5	−25	102	25	7.0
IT100	TO-18 TO-92	75	2.0	4.5	200	35	100	−10			35	12.0
IT101	TO-18 TO-92	60	4.0	10.0	200	35	100	−20			35	12.0
J174	TO-92	85	5.0	10.0	1 nA	30	−1 nA	−20	−100	—	—	—
J175	TO-92	125	3.0	6.0	1 nA	30	−1 nA	−7	−60	—	—	—
J176	TO-92	250	1.0	4.0	1 nA	30	−1 nA	−2	−25	—	—	—
J177	TO-92	300	0.8	2.25	1 nA	30	−1 nA	−1.5	−20	—	—	—
J270	TO-92	—	0.5	2.0	200	30	—	−2	−15	—	20	5.0
J271	TO-92	—	1.5	4.5	200	30	—	−6	−50	—	20	5.0

Switches and Amplifiers—MOSFET

Ordering Information Preferred Part Number	Package	$V_{GS(TH)}$ *$V_{GS(off)}$ min/max V		BV_{GSS} min V	I_{DSS} max pA	I_{GSS} max pA	g_{FS} min μ mho	$r_{DS(on)}$ max ohm	$I_{D(on)}$ min mA	
P-channel Enhancement: Gen. used where max isolation btwn. signal source and logic drive req'd: sw. "On" resistance varies with signal amplitude										
3N160	TO-72	−1.5	−5.0	−25	−10 nA	−50.0	3.5	—	−40	−120
3N161	TO-72	−1.5	−5.0	−25	−10 nA	−100.0	3500.0		−40	−120 Diode Protected
3N163	TO-72	−2.0	−5.0	−40	−200	−10.0	2000.0	250	−5	−30
3N164	TO-72	−2.0	−5.0	−30	400	10.0	1.0	300	−3	−30
3N172	TO-72	−2.0	−5.0	−40	−400	−10.0	1500.0	250	−5	−30 Diode Protected
3N173	TO-72	−2.0	−5.0	−30	−10 nA	−500.0	—	350	−5	−30
IT1700	TO-72	0.2	−5.0	−40	200	10.0	2.0	400	2	—
N-channel Enhancement: Can switch positive signals directly from TTL logic; gen. requires driver or translator circuit to switch bipolar signals										
2N4351	TO-72	1.0	5.0	25	10 nA	10.0	1000.0	300	3	
3N169	TO-72	0.5	1.5	25	10 nA	10.0	1000.0	200	10	
3N170	TO-72	1.0	2.0	25	10 nA	10.0	1000.0	200	10	
3N171	TO-72	1.5	3.0	25	10 nA	10.0	1000.0	200	10	
IT1750	TO-72	0.5	3.0	25	10 nA	10.0	30.0	50	10	100
M116	TO-72	1.0	5.0	30	—	100.0	—	100	—	—

Amplifiers—N-Channel Junction FET

Ordering Information Preferred Part Number	Package	g_{FS} min μmho	I_{DSS} min/max mA		V_P min/max V		I_{GSS} max pA	BV_{GSS} min V	C_{ISS} max pf	C_{RSS} max pf	e_n max nv/√Hz
2N3684	TO-72 TO-92	2000	2.5	7.5	−2.0	−5.0	−100	−50	4	1.2	140 @ 100 Hz
2N3685	TO-72 TO-92	1500	1.0	3.0	−1.0	−3.5	−100	−50	4	1.2	140 @ 100 Hz
2N3686	TO-72 TO-92	1000	0.4	1.2	−0.6	−2.0	−100	−50	4	1.2	140 @ 100 Hz
2N3687	TO-72 TO-92	500	0.1	0.5	−0.3	−1.2	−100	−50	4	1.2	140 @ 100 Hz
2N3821	TO-72	1500	0.5	2.5	−4.0		−0.1 nA	−50	6	3.0	200 @ 10 Hz
2N3822	TO-72 TO-92	3000	2.0	10.0		−6.0	−100	−50	6	3.0	200 @ 10 Hz
2N3823	TO-72	3500	4.0	20.0	−8.0		−0.5 nA	−30	6	2.0	—
2N3824	TO-72	—	—	—			−0.1 nA	−50	6	3.0	—
2N4117	TO-72 TO-92	70	0.03	0.09	−0.6	−1.8	−10	−40	3	1.5	
2N4117A	TO-72 TO-92	70	0.03	0.09	−0.6	−1.8	−1	−40		1.5	
2N4118	TO-72 TO-92	80	0.08	0.24	−1.0	−3.0	−10	−40	3	1.5	
2N4118A	TO-72 TO-92	80	0.08	0.24	−1.0	−3.0	−1	−40	3	1.5	
2N4119	TO-72 TO-92	100	0.2	0.6	−2.0	−6.0	−10	−40	3	1.5	
2N4119A	TO-72 TO-92	100	0.2	0.6	−2.0	−6.0	−1	−40	3	1.5	
2N4220	TO-72 TO-92	1000	0.5	3.0		−4.0	−100	−30	6	2.0	
2N4221	TO-72 TO-92	2000	2.0	6.0		−6.0	−100	−30	6	2.0	
2N4222	TO-72 TO-92	2500	5.0	15.0		−8.0	−100	−30	6	2.0	
2N4223	TO-72	3000	3.0	18.0	−0.1	−8.0	−250	−30	6	2.0	
2N4224	TO-72	2000	2.0	20.0	−0.1	−0.8	−150	−30	6	2.0	
2N4338	TO-18 TO-92	600	0.2	0.6	−0.3	−1.0	−100	−50	7	3.0	65 @ 1 kHz
2N4339	TO-18 TO-92	800	0.5	1.5	−0.6	−1.8	−100	−50	7	3.0	65 @ 1 kHz
2N4340	TO-18 TO-92	1300	1.2	3.6	−1.0	−3.0	−100	−50	7	3.0	65 @ 1 kHz
2N4341	TO-18 TO-92	2000	3.0	9.0	−2.0	−6.0	−100	−50	7	3.0	65 @ 1 kHz
2N4416	TO-72 TO-92	4500	5.0	15.0		−6.0	−100	−30	4	2.0	
2N4867	TO-72 TO-92	700	0.4	1.2	−0.7	−2.0	−250	−40	25	5.0	10 @ 1 kHz
2N4867A	TO-72 TO-92	700	0.4	1.2	−0.7	−2.0	−250	−40	25	5.0	5 @ 1 kHz
2N4868	TO-72 TO-92	1000	1.0	3.0	−1.0	−3.0	−250	−40	25	5.0	10 @ 1 kHz
2N4868A	TO-72 TO-92	1000	1.0	3.0	−1.0	−3.0	−250	−40	25	5.0	5 @ 1 kHz
2N4869	TO-72 TO-92	1300	2.5	7.5	−1.8	−5.0	−250	−40	25	5.0	10 @ 1 kHz
2N4869A	TO-72 TO-92	1300	2.5	7.5	−1.8	−5.0	−250	−40	25	5.0	5 @ 1 kHz
2N5397	TO-72 TO-92	6000 @ 1 mA	10.0	30.0	−1.0	−6.0	−100	−25	5	1.2	3 db @ 450 mHz
2N5398	TO-72	5000	5.0	40.0	−1.6	−0.1		−25	5.5	1.3	
2N5457	TO-92	1000	1.0	5.0	−0.5	−6.0	1 nA	25	7	3.0	3 dB @ 450 mHz
2N5458	TO-92	1500	2.0	9.0	−1.0	−7.0	1 nA	25	7	3.0	3 dB @ 450 mHz
2N5459	TO-92	2000	4.0	16.0	−2.0	−8.0	−1 nA	−25	7	3.0	3 dB @ 450 mHz
2N5484	TO-92	3000	1.0	5.0	−0.3	−3.0	−1 nA	−25	5	1.0	120 @ 1 kHz
2N5485	TO-92	3500	4.0	10.0	−0.5	−4.0	−1 nA	−25	5	1.0	120 @ 1 kHz
ITE4416	TO-72 TO-92	4500	5.0	15.0		−6.0	−100	−30	4	2.0	
2N5486	TO-92	4000	8.0	20.0	−2.0	−6.0	−1 nA	−25	5	1.0	120 @ 1 kHz
U308	TO-52 TO-92	10,000	12.0	60.0	−1.0	−6.0	−150	−25	7 typ.	4.0 typ.	10 @ 10 Hz typ.
U309	TO-52 TO-92	10,000	12.0	30.0	−1.0	−4.0	−150	−25	7 typ.	4.0 typ.	10 @ 10 Hz typ.
U310	TO-52 TO-92	10,000	24.0	60.0	−2.5	−6.0	−150	−25	7 typ.	4.0 typ.	10 @ 10 Hz typ.
U311	TO-92	10,000	20.0	60.0	−1.0		−150	−25	—	—	10 @ 100 Hz
J308	TO-92	8000	12.0	60.0	−1.0		−1 nA	−25	—	—	10 @ 100 Hz
J309	TO-92	10,000	12.0	30.0	−1.0		−1 nA	−25	—	—	10 @ 100 Hz
J310	TO-92	8000	24.0	60.0	−2.0		−1 nA	−25	—	—	10 @ 100 Hz

Amplifiers—P-Channel Junction FET

Ordering Information Preferred Part Number	Package	g_{FS} min μmho	I_{DSS} min/max mA		V_P min/max V		I_{GSS} max nA	BV_{GSS} min V	C_{ISS} max pf	C_{RSS} max pf	e_n max nV/√Hz
2N2606	TO-18 TO-92	110	−0.1	−0.5	1.0	4.0	1	30	7	2	400 @ 1 kHz
2N2607	TO-18 TO-92	330	−0.3	−1.5	1.0	4.0	3	30	7	2	400 @ 1 kHz
2N2608	TO-18 TO-92	1000	−0.9	−4.5	1.0	4.0	10	30	7	2	180 @ 1 kHz
2N2609	TO-18 TO-92	2500	−2.0	−10.0	1.0	4.0	30	30	7	2	180 @ 1 kHz
2N3329	TO-72	1000 @ −1 mA	−1.0	−3.0		5.0	10	20	7	2	400 @ 1 kHz
2N3330	TO-72	1500 @ −2 mA	−2.0	−6.0		6.0	10	20	7	2	400 @ 1 kHz
2N3331	TO-72	200 @ −5 mA	−5.0	−15.0		8.0	10	20	7	2	400 @ 1 kHz
2N5265	TO-72	900	−0.5	−1.0		3.0	2	60	7	2	115 @ 100 Hz
2N5266	TO-72	1000	−0.8	−1.6		3.0	2	60	7	2	115 @ 100 Hz
2N5267	TO-72	1500	−1.5	−3.0		6.0	2	60	7	2	115 @ 100 Hz
2N5268	TO-72	2000	−2.5	−5.0		6.0	2	60	7	2	115 @ 100 Hz
2N5269	TO-72	2200	−4.0	−8.0		8.0	2	60	7	2	115 @ 100 Hz
2N5270	TO-72	2500	−7.0	−14.0		8.0	2	60	7	2	115 @ 100 Hz
2N5460	TO-92	1000	−1.0	−5.0	0.75	6.0	5	40	7	2	115 @ 100 Hz
2N5461	TO-92	1500	−2.0	−9.0	1.0	7.5	5	40	7	2	115 @ 100 Hz
2N5462	TO-92	2500	−4.0	−16.0	1.5	9.0	5	40	7	2	115 @ 100 Hz
2N5463	TO-92	1000	−1.0	−5.0	0.75	6.0	5	60	7	2	115 @ 100 Hz
2N5464	TO-92	1500	−2.0	−9.0	1.0	7.5	5	60	7	2	115 @ 100 Hz
2N5465	TO-92	2500	−4.0	16.0	1.8	9.0	5	60	7	2	115 @ 100 Hz
U304	TO-18		−30	−90		5	.5	30	27	7	—
U305	TO-18		−15	−60		3	.5	30	27	7	—
U306	TO-18		−5	−25		1	.5	30	27	7	—

Differential Amplifiers-Dual Monolithic N-Channel Junction FETS

Ordering Information Preferred Part Number	Package	V_{GS1-2} max mV	ΔV_{GS} max μV/°C	I_G max pA	BV_{GSS} min V	V_p min/max V		g_{fs} min/max μ mho		I_{DSS} min/max mA		e_n max nV/√Hz
2N3921	TO-71	5	10	−250	−50	—	−3.0	1500	7500	1.0	10.0	—
2N3922	TO-71	5	25	−250	−50	—	−3.0	1500	7500	1.0	10.0	—
2N3954	TO-71	5	10	−50	−50	−1.0	−4.5	1	3	0.5	5.0	160 @ 100 Hz
2N3954A	TO-71	5	5	−50	−50	−1.0	−4.5	1	3	0.5	5.0	160 @ 100 Hz
2N3955	TO-71	10	25	−50	−50	−1.0	−4.5	1	3	0.5	5.0	160 @ 100 Hz
2N3955A	TO-71	10	15	−50	−50	−1.0	−4.5	1	3	0.5	5.0	160 @ 100 Hz
2N3956	TO-71	15	50	−50	−50	−1.0	−4.5	1	3	0.5	5.0	160 @ 100 Hz
2N3957	TO-71	20	75	−50	−50	−1.0	−4.5	1	3	0.5	5.0	160 @ 100 Hz
2N3958	TO-71	25	100	−50	−50	−1.0	−4.5	1	3	0.5	5.0	160 @ 100 Hz
2N5196	TO-71	5	5	−15	−50	−0.7	−4.0	700 @ 200 μA		0.7	7.0	20 @ 1 kHz
2N5197	TO-71	5	10	−15	−50	−0.7	−4.0	700 @ 200 μA		0.7	7.0	20 @ 1 kHz
2N5198	TO-71	10	20	−15	−50	−0.7	−4.0	700 @ 200 μA		0.7	7.0	20 @ 1 kHz
2N5199	TO-71	15	40	−15	−50	−0.7	−4.0	700 @ 200 μA		0.7	7.0	20 @ 1 kHz
2N5452	TO-71	5	5	IGSS−100	−50	−1.0	−4.5	1	4	0.5	5.0	20 @ 1 kHz
2N5453	TO-71	10	10	IGSS−100	−50	−1.0	−4.5	1	4	0.5	5.0	20 @ 1 kHz
2N5454	TO-71	15	25	IGSS−100	−50	−1.0	−4.5	1	4	0.5	5.0	20 @ 1 kHz
2N5515	TO-71	5	5	−100	−40	−0.7	−4.0	1	4	0.5	7.5	30 @ 10 Hz
2N5516	TO-71	5	10	−100	−40	−0.7	−4.0	1	4	0.5	7.5	30 @ 10 Hz
2N5517	TO-71	10	20	−100	−40	−0.7	−4.0	1	4	0.5	7.5	30 @ 10 Hz
2N5518	TO-71	15	40	−100	−40	−0.7	−4.0	1	4	0.5	7.5	30 @ 10 Hz
2N5519	TO-71	15	80	−100	−40	−0.7	−4.0	1	4	0.5	7.5	30 @ 10 Hz
2N5520	TO-71	5	5	−100	−40	−0.7	−4.0	1	4	0.5	7.5	15 @ 10 Hz
2N5521	TO-71	5	10	−100	−40	−0.7	−4.0	1	4	0.5	7.5	15 @ 10 Hz
2N5522	TO-71	10	20	−100	−40	−0.7	−4.0	1	4	0.5	7.5	15 @ 10 Hz
2N5523	TO-71	15	40	−100	−40	−0.7	−4.0	1	4	0.5	7.5	15 @ 10 Hz
2N5524	TO-71	15	80	−100	−40	−0.7	−4.0	1	4	0.5	7.5	15 @ 10 Hz
2N5902	TO-99	5	5	−3	−40	−0.6	−4.5	70	250	0.3	0.5	100 @ 1 kHz
2N5903	TO-99	5	10	−3	−40	−0.6	−4.5	70	250	0.03	.05	100 @ 1 kHz
2N5904	TO-99	10	20	−3	−40	−0.6	−4.5	70	250	0.03	.05	100 @ 1 kHz
2N5905	TO-99	15	40	−3	−40	−0.6	−4.5	70	250	0.03	0.5	100 @ 1 kHz
2N5906	TO-99	5	5	−1	−40	−0.6	−4.5	70	250	0.03	0.5	100 @ 1 kHz
2N5907	TO-99	5	10	−1	−40	−0.6	−4.5	70	250	0.03	0.5	100 @ 1 kHz
2N5908	TO-99	10	20	−1	−40	−0.6	−4.5	70	250	0.03	0.5	100 @ 1 kHz
2N5909	TO-99	15	40	−1	−40	−0.6	−4.5	70	250	0.03	0.5	100 @ 1 kHz
2N5911	TO-99	10	20	−100	−25	−1.0	−5.0	5/10 @ 5 mA		7.0	40.0	20 @ 10 kHz
2N5912	TO-99	15	40	−100	−25	−1.0	−5.0	5/10 @ 5 mA		7.0	40.0	20 @ 10 kHz
2N6483	TO-71	5	5	−100	−50	−0.7	−4.0	1000	4000	0.5	7.5	10 @ 10 Hz
2N6484	TO-71	10	10	−100	−50	−0.7	−4.0	1000	4000	0.5	7.5	10 @ 10 Hz
2N6485	TO-71	15	25	−100	−50	−0.7	−4.0	1000	4000	0.5	7.5	10 @ 10 Hz
IMF5911	TO-99	10	20	−100	−25	−1.0	−5.0	5/10 @ 5 mA		7.0	40.0	20 @ 10 kHz
IMF5912	TO-99	15	40	−100	−25	−1.0	−5.0	5/10 @ 5 mA		7.0	40.0	20 @ 10 kHz
IMF6485	TO-71	25	40	−100	−50	−0.7	−4.0	1000	4000	0.5	7.5	15 @ 10 Hz
IT500	TO-52	5	5	−5	−50	−0.7	−4.0	700	1600	0.7	7.0	35 @ 10 Hz
IT501	TO-52	5	10	−5	−50	−0.7	−4.0	700	1600	0.7	7.0	35 @ 10 Hz
IT502	TO-52	10	20	−5	−50	−0.7	−4.0	700	1600	0.7	7.0	35 @ 10 Hz
IT503	TO-52	15	40	−5	−50	−0.7	−4.0	700	1600	0.7	7.0	35 @ 10 Hz
SU2365	TO-71	5	10	−100	−30		−3.5	1/2 @ 200 μA		0.5	10.0	15 @ 1 kHz
SU2365A	TO-71	5	10	−20	−30		−3.5	1/2 @ 200 μA		0.5	10.0	50 @ 1 kHz
SU2366	TO-71	10	10	−100	−30		−3.5	1/2 @ 200 μA		0.5	10.0	15 @ 1 kHz
SU2366A	TO-71	10	10	−20	−30		−3.5	1/2 @ 200 μA		0.5	10.0	50 @ 1 kHz
SU2367	TO-71	10	25	−100	−30		−3.5	1/2 @ 200 μA		0.5	10.0	15 @ 1 kHz
SU2367A	TO-71	10	25	−20	−30		−3.5	1/2 @ 200 μA		0.5	10.0	50 @ 1 kHz
SU2368	TO-71	15	25	−100	−30		−3.5	1/2 @ 200 μA		0.5	10.0	15 @ 1 kHz
SU2368A	TO-71	15	25	−20	−30		−3.5	1/2 @ 200 μA		0.5	10.0	50 @ 1 kHz
U231	TO-71	5	10	−50	−50	−0.5	−4.5	600	1600	0.5	5.0	80 @ 100 Hz
U232	TO-71	10	20	−50	−50	−0.5	−4.5	600	1600	0.5	5.0	80 @ 100 Hz
U233	TO-71	15	50	−50	−50	−0.5	−4.5	600	1600	0.5	5.0	80 @ 100 Hz
U234	TO-71	20	75	−50	−50	−0.5	−4.5	600	1600	0.5	5.0	80 @ 100 Hz
U235	TO-71	25	100	−50	−50	−0.5	−4.5	600	1600	0.5	5.0	80 @ 100 Hz
U401	TO-71	5	10	−15	−50	−0.5	−2.5	2000	7000	0.5	10.0	20 @ 10 Hz
U402	TO-71	10	10	−15	−50	−0.5	−2.5	2000	7000	0.5	10.0	20 @ 10 Hz
U403	TO-71	10	25	−15	−50	−0.5	−2.5	2000	7000	0.5	10.0	20 @ 10 Hz
U404	TO-71	15	25	−15	−50	−0.5	−2.5	2000	7000	0.5	10.0	20 @ 10 Hz
U405	TO-71	20	40	−15	−50	−0.5	−2.5	2000	7000	0.5	10.0	20 @ 10 Hz
U406	TO-71	40	80	−15	−50	−0.5	−2.5	2000	7000	0.5	10.0	20 @ 10 Hz
U421	TO-99	10	10	0.1	−60	0.4	2.0	300	800	60-1000 μA		20 @ 10 Hz
U422	TO-99	15	25	0.1	−60	0.4	2.0	300	800	60-1000 μA		20 @ 10 Hz
U423	TO-99	25	40	0.1	−60	0.4	2.0	300	800	60-1000 μA		20 @ 10 Hz
U424	TO-99	10	10	0.5	−60	0.4	3.0	300	1000	60-1800 μA		20 @ 10 Hz
U425	TO-99	15	25	0.5	−60	0.4	3.0	300	1000	60-1800 μA		20 @ 10 Hz
U426	TO-99	25	40	0.5	−60	0.4	3.0	300	1000	60-1800 μA		20 @ 10 Hz
2N5564	TO-71	5	10	—	−40	−0.5	−3.0	7.5	12.5	5.0	30.0	10 @ 10 Hz
2N5565	TO-71	10	25	—	−40	−0.5	−3.0	7.5	12.5	5.0	30.0	10 @ 10 Hz
2N5566	TO-71	20	50	—	−40	−0.5	−3.0	7.5	12.5	5.0	30.0	10 @ 10 Hz
IMF5564	TO-71	5	10	—	−40	−0.5	−3.0	7.5	12.5	5.0	30.0	10 @ 10 Hz
IMF5565	TO-71	10	25	—	−40	−0.5	−3.0	7.5	12.5	5.0	30.0	10 @ 10 Hz
IMF5566	TO-71	20	50	—	−40	−0.5	−3.0	7.5	12.5	5.0	30.0	10 @ 10 Hz

)ifferential Amplifiers—Dual Monolithic P-Channel MOSFETS Enhancement)

Ordering Information Preferred Part Number	Package	$V_{GS(TH)}$ min/max V		BV_{DSS} min/max V	I_{DSS} max pA	I_{GSS} max pA	g_{FS} min μmho	$I_{D(on)}$ min/max mA		$r_{DS(on)}$ max ohm	V_{GS1-2} max mV
3N165	TO-99	−2	−5	−40	−200	−10	1500	−5.0	−30	300	100
3N166	TO-99	−2	−5	−40	−200	−10	1500	−5.0	−30	300	
3N188	TO-99	−2	−5	−40	−200	−200	1500	−5.0	−30	300	100 Zener Protected
3N189	TO-99	−2	−5	−40	−200	−200	1500	−5.0	−30	300	Zener Protected
3N190	TO-99	−2	−5	−40	−200	−200	1500	−5.0	−30	300	
3N191	TO-99	−2	−5	−40	−200	−200	1500	−5.0	−30	300	

)ifferential Amplifiers—Dual NPN Bipolar Transistors

Ordering Information Preferred Part Number	Package	V_{BE1-2} mV max	ΔV_{BE} μV/°C max	h_{FE} @ $I_C = 10\,\mu A$ $V_{CE} = 5V$ min	I_{B1-2} @ $I_C = 10\,\mu A$ $V_{CE} = 5V$ nA max	BV_{CEO} V min	I_{CBO} nA max	Noise dB max	f_t MHz @ I_c min	C_{obo} pf max	Structure
2N2453	TO-78	3	10	80		30	5	7	150 @ 1 mA	8	Junc. Isol.
2N2453A	TO-78	3	5	80	.6 μA @ 100 μA	60	5	4	150 @ 1 mA	4	Junc. Isol.
2N4044	TO-78	3	3	200	5	60	.1	2	200 @ 1 mA	.8	Dielec. Isol.
2N4045	TO-78	5	10	80	25	45	.1	3	150 @ 1 mA	.8	Dielec. Isol.
2N4100	TO-78	5	5	150	10	55	.1	3	150 @ 1 mA	.8	Dielec. Isol.
2N4878	TO-71	3	3	200	5	60	.1	2	200 @ 1 mA	.8	Dielec. Isol.
2N4879	TO-71	5	5	150	10	55	.1	3	150 @ 1 mA	.8	Dielec. Isol.
2N4880	TO-71	5	10	80	25	45	.1	3	150 @ 1 mA	.8	Dielec. Isol.
IT120	TO-78 TO-71	2	5	200	5	45	1	2 typ.	150 @ 1 mA	2	Junc. Isol.
IT120A	TO-78 TO-71	1	3	200	2.5	60	1	2 typ.	150 @ 1 mA	2	Junc. Isol.
IT124	TO-78	5	10	1500	.6 A V_{CE} = IV	2	.1	3	100 @ 200 μA	.8	Dielec. Isol.
IT124A	TO-78	3.2	15	1500	0.6A V_{CE} = 1V	2	.1	3	100 @ 100 μA	.8	
IT124B	TO-78	5	15	4000	0.6A V_{CE} = 1V	2	.1	3	100 @ 100 μA	.8	
IT125	TO-78	—	—	1000	0.6A V_{CE} = 1V	2	.1	3	100 @ 100 μA	.8	
IT126	TO-78 TO-71	1	3	200	2.5	60	.1	1 typ.	250 @ 10 mA	4	Dielec. Isol.
IT-127	TO-78 TO-71	2	5	200	5	45	.1	1 typ.	250 @ 10 mA	4	Dielec. Isol.
IT128	TO-78 TO-71	5	10	100	10	45	.5	1 typ.	250 @ 10 mA	4	Dielec. Isol.
IT129	TO-78 TO-71	10	20	100	25	45	.5	1 typ.	250 @ 10 mA	4	Dielec. Isol.
LM194	TO-5	0.05	0.3	300	—	40	—	—	—	—	
LM394	TO-5	0.15	0.8	200	—	40	—	—	—		

)ifferential Amplifiers—Dual PNP Bipolar Transistors

Ordering Information Preferred Part Number	Package	V_{BE1-2} mV max	ΔV_{BE} μV/°C max	h_{FE} @ $I_C = 10\,\mu A$ $V_{CE} = 5V$ min	I_{B1-2} @ $I_C = 10\,\mu A$ $V_{CE} = 5V$ nA max	BV_{CEO} V min	I_{CBO} nA max	Noise dB max	f_t MHz @ I_c min	C_{obo} pf max	Structure
2N5117	TO-78	3	3	100	10	45	.1	4	100 @ .5 mA	.8	Dielec. Isol.
2N5118	TO-78	5	5	100	15	45	.1	4	100 @ .5 mA	.8	Dielec. Isol.
2N5119	TO-78	5	10	50	40	45	.1	4	100 @ .5 mA	.8	Dielec. Isol.
IT130	TO-78 TO-71	2	5	200	5	−45	1	2 typ.	150 @ 1 mA	2	Junc. Isol.
IT130A	TO-78 TO-71	1	3	200	2.5	−60	1	2 typ.	150 @ 1 mA	2	Junc. Isol.
IT131	TO-78 TO-71	5	10	80	10	−45	1	2 typ.	150 @ 1 mA	2	Junc. Isol.
IT132	TO-78 TO-71	10	20	80	25	−45	1	2 typ.	150 @ 1 mA	2	Junc. Isol.
IT136	TO-78 TO-71	1	3	200	2.5	−60	.1	2 typ.	250 @ 10 mA	4	Dielec. Isol.
IT137	TO-78 TO-71	2	5	200	5	−45	.1	2 typ.	250 @ 10 mA	4	Dielec. Isol.
IT138	TO-78 TO-71	5	10	100	10	−45	.5	2 typ.	250 @ 10 mA	4	Dielec. Isol.
IT139	TO-78 TO-71	10	20	100	25	−45	.5	2 typ.	250 @ 10 mA	4	Dielec. Isol.

Specialty Items

ID-100 ID-101	This product is a back to back diode combination used to protect P-channel MOSFET duals (non-diode protected). Their chief characteristic is < 1 pa leakage when voltage across them is less than 5 mV. If voltage across diodes is adjusted to 0V ± 0.1 mV, leakage is less than 0.01 pa.
VCR2N VCR3P VCR4N VCR5P VCR7N	The VCR family consists of three terminal variable resistors where the resistance value between two of the terminals is controlled by the voltage potential applied to the third.

N-channel depletion mode JFET, single

Leakage I_G (max)	Noise en @ 10 Hz max	Resistance r_{DS} (max)	g_{FS} (min)	Breakdown Voltage BV_{GSS} (min)
1pA 2N4117A-9A **10pA** 2N4117-9	**10 nV/√Hz** 2N4867A-9A • J308-11 typ. U308-11 typ. **20 nV/√Hz** 2N4867-9 2N4091-3 typ. 2N5432 • ITE4091-3 typ. • J111-3 typ.	**5-10Ω** 2N5432-4 **25-40Ω** 2N4391 2N4856-7 2N4859-60 • 2N5638 • ITE4391 • J111 **50-80Ω** 2N4092-3 2N4392 2N4858 2N4861 • 2N5639 • ITE4092-3 • ITE4392 • J112 **100Ω** 2N4393 • 2N5640 • ITE4393 • J113 **150Ω** • 2N5555 2N5397-8 typ.	**70-100 μmho** 2N4117A-9A **500-999 μmho** 2N3687 2N4338-9 **1000-1499 μmho** 2N3686 2N4220, A 2N4340 2N4868-9, A • 2N5457 **1500-2499 μmho** 2N3684-5 2N3821 2N4221, A 2N4341 • 2N5458-9 **2500-4999 μmho** 2N3822 2N4222, A 2N4223 2N4416, A • 2N5484-6 **5000 up** 2N5397-8 • 2N5555 typ. • J308-10 U308-11	**80V** 2N4338-41 typ. • 2N5457-9 typ. **50V** 2N3684 2N3821-2 2N3824 2N4338-41 **40V** 2N4117-9, A 2N4867-9, A 2N4091-3 2N4391-3 • ITE4091-3 • ITE4391-3

• T092 Plastic case
others metal can.

P-channel depletion mode JFET, Single

r_{DS} (max)	g_{FS} (min)	BV_{GSS} (min)
60-85Ω 2N5114 IT100-1 J174 U304 **100-125Ω** 2N5115 • J175 U305 **150-180Ω** 2N3993 2N5116 U306 **250Ω-300Ω** 2N3994 • J176-7	**100-499 μmho** 2N2606-7 **500-999 μmho** 2N3330-1 2N5265 **1000-2499 μmho** 2N2608 2N3329 2N5266-70 • 2N5460-5 **2500-7499 μmho** 2N3993-4 **7500 μmho** 2N5114-6 typ. IT100-1 J174-7 typ U304-6 typ	**60V** 2N5265-70 • 2N5463-5 **40V** • 2N5460-2

• TO92 Plastic Case

N-channel dual depletion mode JFET

Low Leakage I_G (max)	Low Noise e_n (max) at 10 Hz	g_{fs} (min)	r_{DS} (max)	Offset V_{GS1-2} (max)
0.5pA U424-6 **1 pA** 2N5902-5 **3pA** 2N5906-9	**10 nV/√Hz** 2N6483-5 • IMF5564-6 • IMF5911-2 **15 nV/√Hz** 2N5520-4 IMF6485 **20 nV/√Hz** 2N5911-2 U401-6 **30 nV/√Hz** 2N5515-9	**70-300 μmho** 2N5902-9 U421-6 **100-1500 μmho** 2N3921-2 2N3954-8 2N5196-9 2N5452-4 2N5515-24 IT500-3 U401-6 **5000-7500 μmho** 2N5564-6 2N5911-2 • IMF5564-6 • IMF5911-2 IT5911-2 U257	**100Ω** 2N5564-6 2N5911-2 typ IMF5564-6 IMF5911-2 typ. IT5911-2 typ. **250-750Ω** 2N3921-2 typ. 2N3954-8 typ. 2N5196-9 typ. 2N5515-24 typ. 2N6483-5 typ. IMF6485 typ. IT500-3 typ.	**5 mV** 2N3921-2 2N3954, A 2N3955A 2N5196-7 2N5452 2N5515-6 2N5520-1 2N5564 2N6483 IMF5564 U401

• dielectrically isolated

N-channel single enhancement mode MOSFET

$r_{DS\ (max)}$	Protection
500-100Ω IT1750 M116 **200Ω** 3N169-71 **300Ω** 2N4351	Diode protected M116 **No diode** 2N4351 3N169-71 IT1750

P-channel single enhancement mode MOSFET

$r_{DS\ (max)}$	Protection
250Ω 3N163 3N172 **300-400Ω** 3N164 3N173 IT1700	Diode protected 3N161 3N172-3 **No diode** 3N160 3N163-4 IT1700

P-channel dual enhancement mode MOSFET

$r_{DS\ (max)}$	Protection	Offset $V_{GS1-2\ (max)}$
300Ω 3N165-6 3N188-91	Diode protected 3N188-9 **No diode** 3N165-6 3N190-1	**100 mV** 3N165 3N188 3N190

NPN Dual Bipolar Transistors

$h_{FE\ (min)}$ $I_C = 10\ \mu A$	Offset $V_{BE\ 1-2\ (max)}$	Breakdown $V_{CEO\ (min)}$
50-250 2N2453,A • 2N4044-5 • 2N4100 • 2N4878-80 2N6441-8 IT120-2 • IT126-9 **1000-1500** IT124, A IT125 **4000 up** IT124B	**1 mV** IT120A IT126 **2 mV** IT120 IT127 **3 mV** 2N2453, A 2N4044 2N4878 2N6445-8 IT124A	**60V** 2N2453A 2N4044 2N4878 IT120A IT126 **55V** 2N4100 2N4878

PNP Dual Bipolar Transistors

$h_{FE\ (min)}$ $I_C = 10\ \mu A$	Offset $V_{BE\ 1-2\ (max)}$	Breakdown $V_{CEO\ (min)}$
50-250 2N3810-1, A • 2N5117-9 IT130-2 • IT136-9	**1 mV** IT130A IT136 **2 mV** IT130 IT137	**−60V** 2N3810-1, A IT130A IT137

• Dielectrically isolated

INTERSIL

2N3970, 2N3971, 2N3972
N-Channel Silicon J-FET

FOR ANALOG SWITCHES, CHOPPERS AND AMPLIFIERS

- $R_{DS(on)}$ < 30 ohms (2N3970)
- $I_{D(off)}$ < 250 pA
- Fast Switching

PACKAGE DIMENSIONS

TO-18

NOTE: All dimensions in parenthesis are metric.

PIN	OUT
1	S
2	D
3	G, C

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain Voltage ..... −40V
Gate-Source Voltage ..... −40V
Gate Current ..... 50 mA
Total Device Dissipation at 25°C Case Temperature ..... 1.8 W
Storage Temperature Range ..... −65 to +200°C
Lead Temperature (116" from case for 60 seconds) ..... 300°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

CHARACTERISTIC		2N3970 MIN	2N3970 MAX	2N3971 MIN	2N3971 MAX	2N3972 MIN	2N3972 MAX	UNIT	TEST CONDITIONS	
BV_{GSS}	Gate Reverse Breakdown Voltage	−40		−40		−40		V	$I_G = -1\mu A$, $V_{DS} = 0$	
I_{DGO}	Drain Reverse Current		250		250		250	pA	$V_{DG} = 20V$, $I_S = 0$	
			500		500		500	nA		150°C
$I_{D(off)}$	Drain Cutoff Current		250		250		250	pA	$V_{DG} = 20V$, $V_{GS} = -12V$	
			500		500		500	nA		150°C
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−4	−10	−2	−5	−0.5	−3	V	$V_{DS} = 20V$, $I_D = 1$ nA	
I_{DSS}	Saturation Drain Current (Pulse width 300μs, duty cycle ≤ 3%)	50	150	25	75	5	30	mA	$V_{DS} = 20V$, $V_{GS} = 0$	
$V_{DS(on)}$	Drain-Source ON Voltage						2	V	$V_{GS} = 0$	$I_D = 5$ mA
					1.5					$I_D = 10$ mA
			1							$I_D = 20$ mA
$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0$, $I_D = 1$ mA	
$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100	Ω	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
C_{iss}	Common-Source Input Capacitance		25		25		25	pF	$V_{DS} = 20V$, $V_{GS} = 0$	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		6		6		6	pF	$V_{DS} = 0$, $V_{GS} = -12V$	f = 1 MHz
t_d	Turn-On Delay Time		10		15		40	ns	$V_{DD} = 10V$, $V_{GS(on)} = 0$	
t_r	Rise Time		10		15		40	ns		
t_{off}	Turn-Off Time		30		60		100	ns		

	$I_{D(on)}$	$V_{GS(off)}$
2N3970	20 mA	−10V
2N3971	10 mA	− 5V
2N3972	5 mA	− 3V

INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75 ns
PULSE WIDTH 200 ns
PULSE RATE 550 pps

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.5 pF

INTERSIL

2N4091 JAN TX 2N4091
2N4092 JAN TX 2N4092
2N4093 JAN TX 2N4093
N-Channel Silicon JFET

FEATURES

- $r_{DS(ON)}$ < 30 ohms (2N4091)
- Fast Switching
- $I_{D(OFF)}$ < 100 pA (JAN TX Types)

DESCRIPTION:

This family of junction FETs are characterized for analog switching applications requiring zero dc offset voltage, low ON resistance and fast switching speeds. The JAN TX versions are fully tested to meet the specifications of Mil-S-19500/431.

ABSOLUTE MAXIMUM RATINGS

(@25°C unless otherwise noted)

Maximum Temperatures	
Storage Temperature	−55 to +200°C
Operating Junction Temperature	−55 to +175°C
Lead Temperature (soldering, 10 sec. limit)	300°C
Maximum Power Dissipation	
Device Dissipation @ Free Air Temperature	360 mW
Linear Derating (TO18)	10 mW/°C
Maximum Voltages & Currents	
V_{GS} Gate to Source Voltage	−40 V
V_{DS} Drain to Source Voltage	−40 V
V_{DG} Drain to Gate Voltage	40 V
I_G Gate Current	10 mA

PACKAGE DIMENSIONS:

ORDERING INFORMATION

TO18	WAFER	CHIP
2N4091	2N4091/W	2N4091/D
2N4092	2N4092/W	2N4092/D
2N4093	2N4093/W	2N4093/D
JAN TX 2N4091		
JAN TX 2N4092		
JAN TX 2N4093		

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise otherwise)

Characteristic			2N4091 Min.	2N4091 Max.	2N4092 Min.	2N4092 Max.	2N4093 Min.	2N4093 Max.	Unit	Test Conditions		
BV_{GSS}	Gate-Source Breakdown Voltage		−40		−40		−40		V	I_G = −1 μA, V_{DS} = 0		
I_{DGO}	Drain Reverse Current			200		200		200	pA	V_{GD} = −20 V, I_S = 0		25°C
	(Not JAN TX Specified)			400		400		400	nA			150°C
I_{GSS}	Gate Reverse Current			−100		−100		−100	pA	V_{GS} = −20 V, V_{DS} = 0		25°C
	(JAN TX Only)			−200		−200		−200	nA			150°C
$I_{D(OFF)}$	Drain Cutoff Current							100	pA	V_{DS} = 20 V	V_{GS} = − 6 V	25°C
								200	nA			150°C
		JAN TX Only				100			pA		V_{GS} = − 8 V	25°C
						200			nA			150°C
				100					pA		V_{GS} = −12 V	25°C
				200					nA			150°C
								200	pA		V_{GS} = − 6 V	25°C
								400	nA			150°C
						200			pA		V_{GS} = − 8 V	25°C
						400			nA			150°C
				200					pA		V_{GS} = −12 V	25°C
				400					nA			150°C
V_P	Gate-Source Pinch-Off Voltage		−5	−10	−2	−7	−1	−5	V	V_{DS} = 20 V, I_D = 1 nA		
I_{DSS}	Drain Current at Zero Gate Voltage		30		15		8		mA	V_{DS} = 20 V, V_{GS} = 0, Pulse-Test Duration = 2 ms		
$V_{DS(ON)}$	Drain-Source ON Voltage							0.2	V	V_{GS} = 0	I_D = 2.5 mA	
						0.2					I_D = 4 mA	
				0.2							I_D = 6.6 mA	
$r_{DS(ON)}$	Static Drain-Source ON Resistance			30		50		80	Ω	V_{GS} = 0, I_D = 1 mA		
$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance			30		50		80	Ω	V_{GS} = 0, I_D = 0, f = 1 kHz		
C_{iss}	Common-Source Input Capacitance			16		16		16	pF	V_{DS} = 20 V, V_{GS} = 0, f = 1 MHz		
C_{rss}	Common-Source Reverse Transfer Capacitance	JAN TX Only		5		5		5	pF	V_{DS} = 20 V, V_{GS} = 0, f = 1 MHz		
				5		5		5	pF	V_{DS} = 0, V_{GS} = −20 V, f = 1 MHz		

INTERSIL

2N4391, 2N4392, 2N4393
N-Channel Silicon Planar Epitaxial JFET

FEATURES

- $r_{ON} < 30$ ohms (2N4391)
- $I_{D(off)} < 100$ pA
- Switches ±10 VAC with ±15 V Supplies (2N4392, 2N4393)

GENERAL DESCRIPTION

Most widely used solid state switching element. Generally require a translator circuit to boost logic levels up to ±15 V levels. Ideal for S & H circuits, R/2R ladder network and high frequency switching.

ABSOLUTE MAXIMUM RATINGS

@25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	+300°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C

Maximum Voltages & Current

V_{GS}	Gate to Source Voltage	−40 V
V_{GD}	Gate to Drain Voltage	−40 V
I_G	Gate Current	50 mA

ORDERING INFORMATION

TO18	WAFER	CHIP
2N4391	2N4391/W	2N4391/D
2N4392	2N4392/W	2N4392/D
2N4393	2N4393/W	2N4393/D

PACKAGE DIMENSIONS:

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

CHARACTERISTIC		2N4391 MIN	2N4391 MAX	2N4392 MIN	2N4392 MAX	2N4393 MIN	2N4393 MAX	UNIT	TEST CONDITIONS		
I_{GSS}	Gate Reverse Current		−100		−100		−100	pA	V_{GS} = −20 V, V_{DS} = 0		
			−200		−200		−200	nA			150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		−40		V	I_G = 1 μA, V_{DS} = 0		
$I_{D(off)}$	Drain Cutoff Current						100	pA	V_{DS} = 20 V	V_{GS} = −5 V	
							200	nA			150°C
					100			pA		V_{GS} = −7 V	
					200			nA			150°C
			100					pA		V_{GS} = −12 V	
			200					nA			150°C
$V_{GS(f)}$	Gate-Source Forward Voltage		1		1		1	V	I_G = 1 mA, V_{DS} = 0		
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−4	−10	−2	−5	−0.5	−3		V_{DS} = 20 V, I_D = 1 nA		
I_{DSS}	Saturation Drain Current (Note 1)	50	150	25	75	5	30	mA	V_{DS} = 20 V, V_{GS} = 0		
$V_{DS(on)}$	Drain Source ON Voltage						0.4	V	V_{GS} = 0	I_D = 3 mA	
					0.4					I_D = 6 mA	
			0.4							I_D = 12 mA	
$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 1 mA		
$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 0		f = 1 kHz
C_{iss}	Common-Source Input Capacitance		14		14		14	pF	V_{DS} = 20 V, V_{GS} = 0		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance						3.5		V_{DS} = 0	V_{GS} = −5 V	
					3.5					V_{GS} = −7 V	
			3.5							V_{GS} = −12 V	
t_d	Turn-ON Delay Time		15		15		15	ns	V_{DD} = 10 V, $V_{GS(on)}$ = 0		
t_r	Rise Time		5		5		5			$I_{D(on)}$	$V_{GS(off)}$
t_{off}	Turn-OFF Delay Time		20		35		50		2N4391	12 mA	−12 V
t_f	Fall Time		15		20		30		2N4392	6	−7
									2N4393	3	−5

NOTE:
1. Pulse test required, pulse width = 300 μs, duty cycle ≤ 3%

INPUT PULSE
RISE TIME < 0.5 ns
FALL TIME < 0.5 ns
PULSE DUTY CYCLE 1%

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 50 Ω

INTERSIL

2N4856/JAN TX 2N4856
2N4857/JAN TX 2N4857
2N4858/JAN TX 2N4858
2N4859 thru 2N4861
N-Channel Silicon Planar Epitaxial JFET Analog Switches

GENERAL DESCRIPTION

For analog switches, commutators and choppers.

ABSOLUTE MAXIMUM RATINGS

@25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature TO18	-65°C to +200°C
Operating Junction Temperature TO18	+200°C
Lead Temperature (Soldering, 10 sec time limit)	+300°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	1.8w
Linear Derating TO18	10mW/°C

Maximum Voltages & Current

		2N4856-7-8	2N4859-60-61
V_{GS}	Gate to Source Voltage	-40 V	-30V
V_{GD}	Gate to Drain Voltage	-40 V	-30 V
I_G	Gate Current	50 mA	50 mA

FEATURES

- $r_{DS(ON)} < 25\Omega$ (2N4856, 2N4859)
- $I_{D(off)} < 250$ pA
- Switches ±10 V Signals with ±15 V Supplies (2N4858, 2N4861)

PACKAGE DIMENSIONS

PIN	OUT
1	S
2	D
3	G, C

ORDERING INFORMATION

TO18	WAFER	CHIP
2N4856	2N4856/W	2N4856/D
2N4857	2N4857/W	2N4857/D
2N4858	2N4858/W	2N4858/D
2N4859	2N4859/W	2N4859/D
2N4860	2N4860/W	2N4860/D
2N4861	2N4861/W	2N4861/D

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

CHARACTERISTIC			2N4856,59 MIN	2N4856,59 MAX	2N4857,60 MIN	2N4857,60 MAX	2N4858,61 MIN	2N4858,61 MAX	UNIT	TEST CONDITIONS	
BV_{GSS}	Gate-Source Breakdown Voltage	2N4856-58	-40		-40		-40		V	$I_G = 1\ \mu A$, $V_{DS} = 0$	
		2N4859-61	-30		-30		-30				
I_{GSS}	Gate Reverse Current	2N4856-58		-250		-250		-250	pA	$V_{GS} = -20$ V, $V_{DS} = 0$	
		2N4859-61		-500		-500		-500	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	150°C
$I_{D(off)}$	Drain Cutoff Current			250		250		250	pA	$V_{DS} = 15$ V, $V_{GS} = -10$ V	
				500		500		500	nA		150°C
$V_{GS(off)}$	Gate-Source Cutoff Voltage		-4	-10	-2	-6	-0.8	-4	V	$V_{DS} = 15$ V, $I_D = 0.5$ nA	
I_{DSS}	Saturation Drain Current (Note 1)		50		20	100	8	80	mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
$V_{DS(on)}$	Drain-Source ON Voltage			0.75 (20)		0.50 (10)		0.50 (5)	V (mA)	$V_{GS} = 0$, $I_D = (\ )$	
$r_{ds(on)}$	Drain-Source ON Resistance			25		40		60	ohm	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
C_{iss}	Common-Source Input Capacitance			18		18		18	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance			8		8		8			
t_d	Turn-ON Delay Time			6 (20) [-10]		6 (10) [-6]		10 (5) [-4]	ns (mA) [V]	$V_{DD} = 10$ V, $R_L =$ 464 Ω 2N4856,59; 953 Ω 2N4857,60; 1910 Ω 2N4858,61; $V_{GS(on)} = 0$; $I_{D(on)} = (\ )$, $V_{GS(off)} = (\ )$	
t_r	Rise Time			3 (20) [-10]		4 (10) [-6]		10 (5) [-4]	ns (mA) [V]		
t_{off}	Turn-OFF Time			25 (20) [-10]		50 (10) [-6]		100 (5) [-4]	ns (mA) [V]		

NOTE:

1. Pulse test required, pulsewidth = 100 μs, duty cycle ≤ 10%.

INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75
PULSE WIDTH 100 ns
PULSE DUTY CYCLE < 10%

SAMPLING SCOPE
RISE TIME 0.75 ns
INPUT RESISTANCE 1 M
INPUT CAPACITANCE 2.5 pf

INTERSIL

2N5432 2N5433 2N5434
N-Channel Silicon Planar Epitaxial JFET

FEATURES

- $r_{DS} < 5$ ohms
- Excellent Switching — Turn-On < 4 ns
  Turn-Off < 6 ns
- Low Cutoff Current — $I_{D(off)} < 200$ pA

GENERAL DESCRIPTION

Lowest $r_{DS(on)}$ for analog switches, commutators and choppers

ABSOLUTE MAXIMUM RATINGS

@25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	+260°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	2.3 mW/°C

Maximum Voltages & Current

V_{GS}	Gate to Source Voltage	−25 V
V_{GD}	Gate to Drain Voltage	−25 V
I_G	Gate Current	100 mA
I_D	Drain Current	400 mA

ORDERING INFORMATION

TO52	WAFER	CHIP
2N5432	2N5432/W	2N5432/D
2N5433	2N5433/W	2N5433/D
2N5434	2N5434/W	2N5434/D

PACKAGE DIMENSIONS

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

CHARACTERISTIC		2N5432 MIN	2N5432 MAX	2N5433 MIN	2N5433 MAX	2N5434 MIN	2N5434 MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−200		−200		−200	pA	$V_{GS} = -15$ V, $V_{DS} = 0$	
			−200		−200		−200	nA		150°C
BV_{GSS}	Gate Source Breakdown Voltage	−25		−25		−25		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
$I_{D(off)}$	Drain Cutoff Current		200		200		200	pA	$V_{DS} = 5$ V, $V_{GS} = -10$ V	
			200		200		200	nA		150°C
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−4	−10	−3	−9	−1	−4	V	$V_{DS} = 5$ V, $I_D = 3$ nA	
I_{DSS}	Saturation Drain Current (Note 1)	150		100		30		mA	$V_{DS} = 15$ V, $V_{GS} = 0$	
$r_{DS(on)}$	Static Drain-Source ON Resistance	2	5		7		10	ohm	$V_{GS} = 0$, $I_D = 10$ mA	
$V_{DS(on)}$	Drain-Source ON Voltage		50		70		100	mV		
$r_{ds(on)}$	Drain-Source ON Resistance		5		7		10	ohm	$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
C_{iss}	Common-Source Input Capacitance		30		30		30	pF	$V_{DS} = 0$, $V_{GS} = -10$ V	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		15		15		15			
t_d	Turn-ON Delay Time		4		4		4	ns	$V_{DD} = 1.5$ V, $V_{GS(on)} = 0$, $V_{GS(off)} = -12$ V, $I_{D(on)} = 10$ mA	
t_r	Rise Time		1		1		1			
t_{off}	Turn-OFF Delay Time		6		6		6			
t_f	Fall Time		30		30		30			

NOTE: 1. Pulse test required pulsewidth 300 μs, duty cycle ≤ 3%.

INPUT PULSE
RISE TIME 0.25 ns
FALL TIME 0.75
PULSE WIDTH 200 ns
PULSE RATE 550 pps

SAMPLING SCOPE
RISE TIME 0.4 ns
INPUT RESISTANCE 10 M
INPUT CAPACITANCE 1.5 pF

INTERSIL

2N5555
N-Channel Silicon Planar Epitaxial JFET

FEATURES

- Good Combination of $r_{DS(on)}$ [< 150Ω] and Low C_{GS} (< 1.2 pF)

GENERAL DESCRIPTION

Makes ideal sample and hold switch. Low C_{GS} gives very low charge injection; low $I_{D(off)}$ produces super low S & H drift rate. $V_{GS(off)}$ less than 5 V allows switching up to ±10 VAC with ±15 V supplies.

ABSOLUTE MAXIMUM RATINGS

@25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	−55°C to +125°C
Operating Junction Temperature @ Free Air Temperature	+125°C
Lead Temperature (Soldering, 10 second time limit)	+300°C
Maximum Power Dissipation	
Device Dissipation	300 mW
Linear Derating	3.0 mW/°C
Maximum Voltages & Current	
V_{SG} Source to Gate Voltage	25 V
V_{DS} Drain to Source Voltage	25 V
V_{DG} Drain to Gate Voltage	25 V
I_G Gate Current	10 mA

ORDERING INFORMATION

TO92	WAFER	CHIP
2N5555	2N5555/W	2N5555/D

PACKAGE DIMENSIONS

TO-92

5011

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN	MAX	UNIT	TEST CONDITIONS
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	25	—	Vdc	I_G = 10 μAdc, V_{DS} = 0
I_{GSS}	Gate Reverse Current	—	1.0	nAdc	V_{GS} = 15 Vdc, V_{DS} = 0
$I_{D(off)}$	Drain Cutoff Current	—	100	pAdc	V_{DS} = 12 Vdc, V_{GS} = 10 Vdc
		—	2.0	μAdc	V_{DS} = 12 Vdc, V_{GS} = 10 Vdc, T_A = 100°C)
$V_{GS(off)}$	Gate-Source to Gate-Source Drain Cut-off Voltage	—	5	Vdc	@V_{DS} = 10 V, @ I_D = 1 nA
I_{DSS}	Zero-Gate Voltage Drain Current	15	—	mAdc	V_{DS} = 15 Vdc, V_{GS} = 0
$V_{GS(f)}$	Gate-Source Forward Voltage	—	1.0	Vdc	$I_{G(f)}$ = 1.0 mAdc, V_{DS} = 0
$V_{DS(on)}$	Drain-Source "ON" Voltage	—	1.5	Vdc	I_D = 7.0 mAdc, V_{GS} = 0
$r_{DS(on)}$	Static Drain-Source "ON" Resistance	—	150	Ohms	I_D = 0.1 mAdc, V_{GS} = 0

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	—	5.0	ns	V_{DD} = 10 Vdc, $I_{D(on)}$ = 7.0 mAdc,
t_r	Rise Time	—	5.0	ns	
$t_{d(off)}$	Turn-Off Delay Time	—	15	ns	$V_{GS(on)}$ = 0, $V_{GS(off)}$ = −10 Vdc
t_f	Full Time	—	10	ns	

SWITCHING TIMES TEST CIRCUIT

INPUT PULSE
Rise Time < 1.0 ns
Fall Time < 1.0 ns
Nominal Value of "on" Pulse Width = 400 ns
Duty Cycle ≤ 1.0%
Generator Source Impedance = 50 Ohms

INTERSIL

2N5638 2N5639 2N5640

N-Channel Silicon Epitaxial JFET

FEATURES

For analog switches, commutator and choppers.

- Economy Packaging
- Fast Switching – $t_{rise} < 5$ nsec (2N5638)
- Low Drain-Source 'ON' Resistance < 30 Ω (2N5638)

ABSOLUTE MAXIMUM RATINGS

Drain-Source Breakdown Voltage	30 V
Drain-Gate Breakdown Voltage	30 V
Source-Gate Breakdown Voltage	30 V
Forward Gate Current	10 mA
Total Device Dissipation at 25°C	310 mW
Derate above 25°C	2.82 mW/°C
Operating Junction Temperature Range	−65 to +135°C
Storage Temperature Range	−65 to +150°C

1

PACKAGE DIMENSIONS

TO-92

PIN	OUT
1	D
2	S
3	G

NOTE: FOR DIE STRUCTURE, REFER TO 2N4391 FAMILY

5001B

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

CHARACTERISTIC		2N5638 MIN	2N5638 MAX	2N5639 MIN	2N5639 MAX	2N5640 MIN	2N5640 MAX	UNIT	TEST CONDITIONS	
BV_{GSS}	Gate Reverse Breakdown Voltage	−30		−30		−30		V	$I_G = -10\ \mu A$, $V_{DS} = 0$	
I_{GSS}	Gate Reverse Current		−1.0		−1.0		−1.0	nA	$V_{GS} = -15$ V, $V_{DS} = 0$	
			−1.0		−1.0		−1.0	μA		$T_A = +100°C$
$I_{D(off)}$	Drain Cutoff Current		1.0		1.0		1.0	nA	$V_{DS} = 15$ V, $V_{GS} = -12$ V (2N5638)	
			1.0		1.0		1.0	μA	$V_{GS} = -8$ V (2N5639), $V_{GS} = -6$ V (2N5640)	$T_A = +100°C$
I_{DSS}	Saturation Drain Current	50		25		5.0		mA	$V_{DS} = 20$ V, $V_{GS} = 0$ (Note 1)	
$V_{DS(on)}$	Drain-Source ON Voltage		0.5		0.5		0.5	V	$V_{GS} = 0$, $I_D = 12$ mA (2N5638), $I_D = 6$ mA (2N5639), $I_D = 3$ mA (2N5640)	
$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	$I_D = 1$ mA, $V_{GS} = 0$	
$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100		$V_{GS} = 0$, $I_D = 0$	f = 1 kHz
C_{iss}	Common-Source Input Capacitance		10		10		10	pF	$V_{GS} = -12$ V, $V_{DS} = 0$	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		4.0		4.0		4.0			
$t_{d(on)}$	Turn-On Delay Time		4.0		6.0		8.0	ns	$V_{DD} = 10$ V, $V_{GS(on)} = 0$, $V_{GS(off)} = -10$ V, $R_G = 50\ \Omega$; $I_{D(on)} = 12$ mA (2N5638), $I_{D(on)} = 6$ mA (2N5639), $I_{D(on)} = 3$ mA (2N5640)	
t_r	Rise Time		5.0		8.0		10			
t_d	Turn-OFF Delay Time		5.0		10		15			
t_f	Fall Time		10		20		30			

NOTE: 1. Pulse test PW ≤ 300 μs, duty cycle ≤ 3.0%.

INTERSIL

ITE4091, ITE4092, ITE4093
N-Channel Silicon JFET

FEATURES
- $r_{DS(ON)}$ < 30 ohms (ITE4091)
- $I_{D(OFF)}$ < 200 pA
- Fast Switching

GENERAL DESCRIPTION:
This family of junction FETs are characterized for analog switching applications requiring zero dc offset voltage, low ON resistance and fast switching speeds.

ABSOLUTE MAXIMUM RATINGS
(@25°C unless otherwise noted)

Maximum Temperatures
- Storage Temperature ..... −55 to +200°C
- Operating Junction Temperature ..... −55 to +175°C
- Lead Temperature (soldering, 10 sec. limit) ..... 300°C

Maximum Power Dissipation
- Device Dissipation @ Free Air Temperature .. 360 mW
- Linear Derating (TO92) ..... 16 mW/°C

Maximum Voltages & Currents
- V_{GS} Gate to Source Voltage ..... −40V
- V_{DS} Drain to Source Voltage ..... −40V
- V_{DG} Drain to Gate Voltage 40V
- I_G Gate Current ..... 10 mA

PACKAGE DIMENSIONS

TO-92

PIN	OUT
1	S
2	D
3	G

5001B

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

Characteristic		ITE4091 Min.	ITE4091 Max.	ITE4092 Min.	ITE4092 Max.	ITE4093 Min.	ITE4093 Max.	Unit	Test Conditions		
BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		−40		V	$I_G = -1\mu A$, $V_{DS} = 0$		
I_{DGO}	Drain Reverse Current		200		200		200	pA	$V_{GS} = -20V$, $I_S = 0$		25C
			400		400		400	nA			150C
I_{GSS}	Gate Reverse Current		−100		−100		−100	pA	$V_{GS} = -20V$, $V_{DS} = 0$		25C
											150C
$I_{D(OFF)}$	Drain Cutoff Current						200	pA	$V_{DS} = 20V$		25C
							400	nA		$V_{GS} = -6V$	150C
					200			pA			25C
					400			nA		$V_{GS} = -8V$	150C
			200					pA			25C
			400					nA		$V_{GS} = -12V$	150C
V_P	Gate Source Pinch Off Voltage	−5	−10	−2	−7	−1	−5	V	$V_{DS} = 20V$, $I_D = 1$ nA		
I_{DSS}	Drain Current at Zero Gate Voltage	30		15		8		mA	$V_{DS} = 20V$, $V_{GS} = 0$, Pulse Test Duration = 2ms		
							0.2			$I_D = 2.5mA$	
$V_{DS(ON)}$	Drain Source ON Voltage				0.2			V	$V_{GS} = 0$	$I_D = 4$ mA	
			0.2							$I_D = 6.6$ mA	
$r_{DS(ON)}$	Static Drain-Source ON Resistance		30		50		80	Ω	$V_{GS} = 0$, $I_D = 1$ mA		
$r_{ds(on)}$	Small Signal Drain-Source ON Resistance		30		50		80	Ω	$V_{GS} = 0$, $I_D \doteq 0$, f = 1 kHz		
C_{iss}	Common Source Input Capacitance		16		16		16	pF	$V_{DS} = 20V$, $V_{GS} = 0$, f = 1 MHz		
C_{rss}	Common Source Reverse Transfer Capacitance		5		5		5	pF	$V_{DS} = 0$, $V_{GS} = -20V$, f = 1 MHz		

INTERSIL

ITE4391, ITE4392, ITE4393

N-Channel Silicon Planar Epitaxial JFET

FEATURES

- $r_{DS(on)}$ < 30 ohms (ITE4391)
- $I_{D(off)}$ < 100 pA
- Switches ±10 VAC with ±15V Supplies (ITE4392, ITE4393)

GENERAL DESCRIPTION

Most widely used solid state switching element. Generally require a translator circuit to boost logic levels up to ±15V levels. Ideal for S & H circuits, R/2R ladder network and high frequency switching.

ABSOLUTE MAXIMUM RATINGS

@25°C (unless otherwise noted)

Maximum Temperatures
- Storage Temperature TO92 ..... −55°C to +125°C
- Operating Junction Temperature TO92 ..... +125°C
- Lead Temperature (Soldering, 10 sec time limit) +300°C

Maximum Power Dissipation
- Device Dissipation @ Free Air Temperature .. 300 mW
- Linear Derating TO92 ..... 3.0 mW/°C

Maximum Voltages & Current
- V_{GS} Gate to Source Voltage ..... −40V
- V_{GD} Gate to Drain Voltage ..... −40V
- I_G Gate Current ..... 50 mA

PACKAGE DIMENSIONS

TO-92

PIN	OUT
1	S
2	D
3	G

5001B

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

CHARACTERISTIC		ITE4391 MIN	ITE4391 MAX	ITE4392 MIN	ITE4392 MAX	ITE4393 MIN	ITE4393 MAX	UNIT	TEST CONDITIONS		
I_{GSS}	Gate Reverse Current		−100		−100		−100	pA	V_{GS} = −20V, V_{DS} = 0		
			−200		−200		−200	nA			150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		−40		V	I_G = 1μA, V_{DS} = 0		
$I_{D(off)}$	Drain Cutoff Current						100	pA	V_{DS} = 20V	V_{GS} = −5V	
							200	nA			150°C
					100			pA		V_{GS} = −7V	
					200			nA			150°C
			100					pA		V_{GS} = −12V	
			200					nA			150°C
$V_{GS(f)}$	Gate-Source Forward Voltage		1		1		1	V	I_G = 1 mA, V_{DS} = 0		
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−4	−10	−2	−5	−0.5	−3		V_{DS} = 20V, I_D = 1 nA		
I_{DSS}	Saturation Drain Current (Note 1)	50	150	25	75	5	30	mA	V_{DS} = 20V, V_{GS} = 0		
$V_{DS(on)}$	Drain Source ON Voltage						0.4	V	V_{GS} = 0	I_D = 3 mA	
					0.4					I_D = 6 mA	
			0.4							I_D = 12 mA	
$r_{DS(on)}$	Static Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 1 mA		
$r_{ds(on)}$	Drain-Source ON Resistance		30		60		100	Ω	V_{GS} = 0, I_D = 0		f = 1 kHz
C_{iss}	Common Source Input Capacitance		14		14		14	pF	V_{DS} = 20V, V_{GS} = 0		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance						3.5		V_{DS} = 0	V_{GS} = −5V	
					3.5					V_{GS} = −7V	
			3.5							V_{GS} = −12V	
t_d	Turn-ON Delay Time		15		15		15	ns	V_{DD} = 10V, $V_{GS(on)}$ = 0		
t_r	Rise Time		5		5		5			$I_{D(on)}$	$V_{GS(off)}$
t_{off}	Turn-OFF Delay Time		20		35		50		ITE4391	12 mA	−12V
t_f	Fall Time		15		20		30		ITE4392	6	−7
									ITE4393	3	−5

NOTE 1: Pulse test required, pulse width = 300μs, duty cycle ≤ 3%

INTERSIL

J111, J112, J113
N-Channel J-FET

DESIGNED FOR USE AS
- Analog Switches
- Choppers
- Commutators

FEATURES
- Low Cost
- Automated Insertion Package
- Low Insertion Loss
  - $R_{DS(on)} < 30\Omega$ (J111)
- No Offset or Error Voltage Generated by Closed Switch
  - Purely Resistive
  - High Isolation Resistance from Driver
- Fast Switching
  - $t_{D(on)} + t_r = 13$ ns Typical
- Short Sample and Hold Aperture Time
  - $C_{gd(off)} < 5$ pF
  - $C_{gs(off)} < 5$ pF

PACKAGE DIMENSIONS

TO-92

PIN	OUT
1	D
2	S
3	G

ABSOLUTE MAXIMUM RATINGS (@ 25°C)

Gate-Drain or Gate-Source Voltage ..... −35V
Gate Current ..... 50 mA
Total Device Dissipation (T_{LEAD} = 25°C) ..... 625 mW
Power Derating (to +135°C) ..... 5.68 mW/°C
Storage Temperature Range ..... −55°C to +135°C
Operating Temperature Range ..... −55°C to +135°C
Lead Temperature (1/16" from case for 10 seconds) ..... +300°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

		PARAMETERS		J111 MIN	J111 TYP	J111 MAX	J112 MIN	J112 TYP	J112 MAX	J113 MIN	J113 TYP	J113 MAX	UNIT	TEST CONDITIONS
1	S	I_{GSS}	Gate Reverse Current (Note 1)			1			1			1	nA	V_{DS} = 0V, V_{GS} = −15V
2	T	$V_{GS(off)}$	Gate Source Cutoff Voltage	3		10	1		5	0.5		3	V	V_{DS} = 5V, I_D = 1μA
3	A	BV_{GSS}	Gate Source Breakdown Voltage	35			35			35				V_{DS} = 0V, I_G = −1μA
4	T	I_{DSS}	Drain Saturation Current (Note 2)	20			5			2			mA	V_{DS} = 15V, V_{GS} = 0V
5	I	$I_{D(off)}$	Drain Cutoff Current (Note 1)			1			1			1	nA	V_{DS} = 5V, V_{GS} = −10V
6	C	$r_{DS(on)}$	Drain Source ON Resistance			30			50			100	Ω	V_{DS} = 0.1V, V_{GS} = 0V
7	D	$C_{dg(off)}$	Drain Gate OFF Capacitance			5			5			5	pF	V_{DS} = 0V, V_{GS} = −10V, f = 1 MHz
8	Y	$C_{sg(off)}$	Source Gate OFF Capacitance			5			5			5		
9	N A	$C_{dg(on)} + C_{sg(on)}$	Drain Gate Plus Source Gate ON Capacitance			28			28			28		V_{DS} = V_{GS} = 0, f = 1 MHz
10	M	$t_{d(on)}$	Turn On Delay Time		7			7			7		ns	Switching Time Test Conditions
11	I	t_r	Rise Time		6			6			6			
12	C	$t_{d(off)}$	Turn Off Delay Time		20			20			20			
13		t_f	Fall Time		15			15			15			

	J111	J112	J113
V_{DD}	10V	10V	10V
$V_{GS(off)}$	−12V	−7V	−5V
R_L	800Ω	1,600Ω	3,200Ω

NOTES:
1. Approximately doubles for every 10°C increase in T_A.
2. Pulse Test duration 300μs; duty cycle ≤ 3%.

INTERSIL

2N3993, 2N3994
P-Channel Silicon Planar Epitaxial JFET

FEATURES

- Low $r_{DS(on)}$ – 150Ω Max (2N3993)
- High $|Y_{fs}|/C_{iss}$ Ratio (High-Frequency Figure-of-Merit)

GENERAL DESCRIPTION

Used in high-speed commutator and chopper applications. Also ideal for "Virtual Gnd" switching; needs no ext. translator circuit to switch ±10 VAC. Can be driven direct from T^2L or CMOS logic.

MAXIMUM RATINGS

@25°C free-air temperature (unless otherwise noted)

Drain-Gate Voltage	–25 V
Drain-Source Voltage	–25 V
Reverse Gate-Source Voltage	+25 V
Continuous Forward Gate Current	–10 mA
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature (See Note 1)	300 mW
Storage Temperature Range	–65°C to 200°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	300°C

PACKAGE DIMENSIONS

TO-72

PIN	OUT
1	S
2	G
3	D
4	C

NOTE: FOR DIE STRUCTURE, SEE 2N5114 FAMILY.

5508B

*ELECTRICAL CHARACTERISTICS @ 25°C free-air temperature (unless otherwise noted)

PARAMETER		TEST CONDITIONS†		2N3993 MIN	2N3993 MAX	2N3994 MIN	2N3994 MAX	UNIT
BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = 1\ \mu A$,	$V_{DS} = 0$	25		25		V
I_{DGO}	Drain Reverse Current	$V_{DG} = -15$ V,	$I_S = 0$		–1.2		–1.2	nA
		$V_{DG} = -15$ V,	$I_S = 0$, $T_A = 150°C$		–1.2		–1.2	μA
I_{DSS}	Zero-Gate-Voltage Drain Current	$V_{DS} = -10$ V,	$V_{GS} = 0$, See Note 2	–10		–2		mA
$I_{D(off)}$	Drain Cutoff Current	$V_{DS} = -10$ V,	$V_{GS} = 6$ V				–1.2	nA
		$V_{DS} = -10$ V,	$V_{GS} = 6$ V, $T_A = 150°C$				–1	μA
		$V_{DS} = -10$ V,	$V_{GS} = 10$ V		–1.2			nA
		$V_{DS} = -10$ V,	$V_{GS} = 10$ V, $T_A = 150°C$		–1			μA
$V_{GS(off)}$	Gate-Source Voltage	$V_{DS} = -10$ V,	$I_D = -1\ \mu A$	4	9.5	1	5.5	V
$r_{ds(on)}$	Small-Signal Drain-Source On-State Resistance	$V_{GS} = 0$, f = 1 kHz	$I_D = 0$,		150		300	Ω
$\|y_{fs}\|$	Small-Signal Common-Source Forward Transfer Admittance	$V_{DS} = -10$ V, f = 1 kHz,	$V_{GS} = 0$, See Note 2	6	12	4	10	mmho
C_{iss}	Common-Source Short-Circuit Input Capacitance	$V_{DS} = -10$ V, f = 1 MHz,	$V_{GS} = 0$, See Note 3		16		16	pF
C_{rss}	Common-Source Short-Circuit Reverse Transfer Capacitance	$V_{DS} = 0$, f = 1 MHz	$V_{GS} = 6$ V,				5	pF
		$V_{DS} = 0$, f = 1 MHz	$V_{GS} = 10$ V,		4.5		4.5	pF

NOTES: 2. These parameters must be measured using pulse techniques. $t_p = 100$ ms, duty cycle ≤ 10%.
3. This parameter must be measured with bias voltages applied for less than 5 seconds to avoid overheating.

*Indicates JEDEC registered data.

†The fourth lead (case) is connected to the source for all measurements.

INTERSIL

2N5114/JAN TX 2N5114
2N5115/JAN TX 2N5115
2N5116/JAN TX 2N5116
P-Channel Silicon Planar Epitaxial JFET

FEATURES

- ON Resistance < 75 ohms on 2N5114
- $I_{D(off)}$ < 500 pA
- Switches directly from T^2L Logic (2N5116)

GENERAL DESCRIPTION

Ideal for inverting switching or "Virtual Gnd" switching into inverting input of Op. Amp. No driver is required and ±10 VAC signals can be handled using only +5V logic (T^2L or CMOS).

ABSOLUTE MAXIMUM RATINGS

@25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	+260°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	500 mW
Linear Derating	3.0 mW/°C

Maximum Voltages & Current

V_{GS}	Gate to Source Voltage	30 V
V_{GD}	Gate to Drain Voltage	30 V
I_G	Gate Current	50 mA

ORDERING INFORMATION

TO18	WAFER	CHIP
2N5114	2N5114/W	2N5114/D
2N5115	2N5115/W	2N5115/D
2N5116	2N5116/W	2N5116/D
JAN TX 2N5114		
JAN TX 2N5115		
JAN TX 2N5116		

PACKAGE DIMENSIONS

TO-18

5508B

NOTE: SUBSTRATE IS GATE

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

CHARACTERISTIC		2N5114 MIN	2N5114 MAX	2N5115 MIN	2N5115 MAX	2N5116 MIN	2N5116 MAX	UNIT	TEST CONDITIONS	
BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	I_G = 1 μA, V_{DS} = 0	
I_{GSS}	Gate Reverse Current		500		500		500	pA	V_{GS} = 20 V, V_{DS} = 0	25°C
			1.0		1.0		1.0	μA		150°C
$I_{D(OFF)}$	Drain Cutoff Current		−500		−500		−500	pA	V_{DS} = −15 V, V_{GS} = 2N5114 = 12 V, 2N5115 = 7 V, 2N5116 = 5 V	25°C
			−1.0		−1.0		−1.0	μA		150°C
V_P	Gate-Source Pinch-Off Voltage	5	10	3	6	1	4	V	V_{DS} = −15 V, I_D = −1 nA	
I_{DSS}	Drain Current at Zero Gate Voltage	−30	−90	−15	−60	−5	−25	mA	V_{GS} = 0, V_{DS} = 2N5114 = −18 V, 2N5115 = −15 V, 2N5116 = −15 V	
$V_{GS(f)}$	Forward Gate-Source Voltage		−1		−1		−1	V	Pulse Test Duration = 2 ms, I_G = −1 mA, V_{DS} = 0	
$V_{DS(ON)}$	Drain-Source ON Voltage		−1.3		−0.8		−0.6	V	V_{GS} = 0, I_D = 2N5114 = −15 mA, 2N5115 = − 7 mA, 2N5116 = − 3 mA	
$R_{DS(ON)}$	Static Drain-Source ON Resistance		75		100		100	Ω	V_{GS} = 0, I_D = −1 mA	
$r_{ds(ON)}$	Small-Signal Drain-Source ON Resistance		75		100		150	Ω	V_{GS} = 0, I_D = 0, f = 1 kHz	
	Jan TX only		75		100		175	Ω		
C_{iss}	Common-Source Input Capacitance		25		25		25	pF	V_{DS} = −15 V, V_{GS} = 0, f = 1 MHz	
	Jan TX only		25		25		27	pF		
C_{rss}	Common-Source Reverse Transfer Capacitance		7		7		7	pF	V_{DS} = 0, V_{GS} = 2N5114 = 12 V, 2N5115 = 7 V, 2N5116 = 5 V, f = 1 MHz	

INTERSIL

IT100 IT101
P-Channel Silicon Planar Epitaxial JFET Analog Switches

FEATURES

- Interfaces Directly with T^2L Logic Elements so that No Extra Driver Stage is Required.
- $R_{DS(ON)} < 75\Omega$ for 5 V Logic Drive
- $I_{D(OFF)} < 100$ pA

GENERAL DESCRIPTION

This P-channel JFET has been designed to directly interface with T^2L logic, thus eliminating the need for costly drivers, in analog gate circuitry. Bipolar inputs of ±15 V can be switched. The FET is OFF for hi level inputs (+5 V or +15 V) and ON for low level inputs (< 0.5 V for IT100 < 1.5 V for IT101.

ABSOLUTE MAXIMUM RATINGS

@25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	(TO18)	-65°C to +200°C
Storage Temperature	(TO92)	-55°C to +125°C
Operating Junction Temperature	(TO18)	+200°C
Operating Junction Temperature	(TO92)	+125°C
Lead Temperature (Soldering, 10 sec time limit)		+300°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature		300 mW
Linear Derating	(TO18)	1.7 mW/°C
	(TO92)	3.0 mW/°C

Maximum Voltages & Current

V_{GS}	Gate to Source Voltage	35V
V_{GD}	Gate to Drain Voltage	35V
I_G	Gate Current	50 mA

ORDERING INFORMATION

TO18	TO92	WAFER FORM	CHIP
IT100	IT100-TO92	IT100/W	IT100/D
IT101	IT101-TO92	IT101/W	IT101/D

PACKAGE DIMENSIONS

ELECTRICAL CHARACTERISTICS @25°C (unless otherwise noted)

	CHARACTERISTIC	IT100 MIN	IT100 MAX	IT101 MIN	IT101 MAX	UNIT	TEST CONDITIONS
I_{DSS}	Max Drain Current	-10	–	-20	–	mA	$V_{GS} = 0$, $V_{DS} = -15$ V
V_P	Pinch Off Voltage	2	4.5	4	10	V	$I_D = 1$ nA, $V_{DS} = -15$ V
BV_{GSS}	Gate-Source Breakdown Voltage	35		35		V	$I_G = 1\ \mu A$, $V_{DS} = 0$
I_{GSS}	Gate Leakage Current		200		200	pA	$V_{GS} = 20$ V, $V_{DS} = 0$
g_{fs}	Transconductance	-8		-8		mmho	$V_{GS} = 0$, $V_{DS} = -15$ V
g_{os}	Output Conductance		-1		-1	mmho	$V_{GS} = 0$, $V_{DS} = -15$ V
$I_{D(OFF)}$	Drain (OFF) Leakage		-100		-100	pA	$V_{DS} = 10$ V, $V_{GS} = -15$ V
$R_{DS(ON)}$	Drain-Source "ON" Resistance		75		60	Ω	$V_{GS} = 0$, $V_{DS} = -0.1$ V
C_{iss}	Input Capacity		35		35	pF	$V_{DG} = -20$ V, $V_{GS} = 0$
C_{rss}	Reverse Transfer Capacity		12		12	pF	$V_{DG} = -10$ V, $I_S = 0$

INTERSIL

J174, J175, J176, J177
P-Channel J-FETS

DESIGNED FOR USE AS
- Analog Switches
- Choppers
- Commutators

FEATURES
- Low Cost
- Low Insertion Loss
  $R_{DS(on)}$ < 85Ω (J174)
- No Offset or Error Voltages Generated by Closed Switch
  Purely Resistive
  High Isolation Resistance from Driver
- Short Sample and Hold Aperture Time
  $C_{sg(off)}$ < 5.5 pF
  $C_{dg(off)}$ < 5.5 pF
- Fast Switching
  $t_{d(on)} + t_r$ = 7 ns Typical

PACKAGE DIMENSIONS

TO-92

PIN	FET
1	S
2	G
3	D

1

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) 30V
Gate Current ..... 50 mA
Total Device Dissipation (25°C Free-Air Temperature) ..... 350 mW
Power Derating (to +125°C) ..... 3.5 mW/°C
Storage Temperature Range ..... −55 to +125°C
Operating Temperature Range ..... −55 to +125°C
Lead Temperature (1/16" from case for 10 seconds) ..... 300°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

		PARAMETERS		J174 MIN	J174 TYP	J174 MAX	J175 MIN	J175 TYP	J175 MAX	J176 MIN	J176 TYP	J176 MAX	J177 MIN	J177 TYP	J177 MAX	UNIT	TEST CONDITIONS
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			1			1			1			1	nA	V_{DS} = 0, V_{GS} = 20V
2	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	5		10	3		6	1		4	0.8		2.25	V	V_{DS} = −15V, I_D = −10nA
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30			30			30			30			V	V_{DS} = 0, I_G = 1μA
4	STATIC	I_{DSS}	Saturation Drain Current (Note 3)	−20		−100	−7		−60	−2		−25	−1.5		−20	mA	V_{DS} = −15V, V_{GS} = 0
5	STATIC	$I_{D(off)}$	Drain Cutoff Current (Note 2)			−1			−1			−1			−1	nA	V_{DS} = −15V, V_{GS} = 10V
6	STATIC	$r_{DS(on)}$	Drain-Source ON Resistance			85			125			250			300	Ω	V_{GS} = 0, V_{DS} = −0.1V
7	DYNAMIC	$C_{dg(off)}$	Drain-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	V_{DS} = 0, V_{GS} = 10V; f = 1 MHz
8	DYNAMIC	$C_{sg(off)}$	Source-Gate OFF Capacitance		5.5			5.5			5.5			5.5		pF	V_{DS} = 0, V_{GS} = 10V; f = 1 MHz
9	DYNAMIC	$C_{dg(on)} + C_{sg(on)}$	Drain-Gate Plus Source Gate ON Capacitance		40			40			40			40		pF	V_{DS} = V_{GS} = 0; f = 1 MHz
10	DYNAMIC	$t_{d(on)}$	Turn On Delay Time		2			5			15			20		ns	Switching Time Test Conditions
11	DYNAMIC	t_r	Rise Time		5			10			20			25		ns	
12	DYNAMIC	$t_{d(off)}$	Turn Off Delay Time		5			10			15			20		ns	
13	DYNAMIC	t_f	Fall Time		10			20			20			25		ns	

	J174	J175	J176	J177
V_{DD}	−10V	−6V	−6V	−6V
$V_{GS(off)}$	12V	8V	6V	3V
R_L	560Ω	12KΩ	5.6KΩ	10KΩ
$V_{GS(on)}$	0V	0V	0V	0V

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration −300μs; duty cycle ≤ 3%.

INTERSIL

J270, J271
P-Channel J-FET

DESIGNED FOR USE AS
- General Purpose Amplifiers

FEATURES
- Low Cost
- Automatic Insertion Package
- High Gain Amplifiers
  g_{fs} = 14,000 μmho Typical (J271)
- Low Noise
  e_n = 6 nV/√Hz at 1 kHz Typical

PACKAGE DIMENSIONS

TO-92

PIN	FET
1	S
2	G
3	D

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage (Note 1) 30V
Gate Current ..... −50mA
Total Device Dissipation (25°C Free-Air Temperature) ..... 350 mW
Power Derating (to +125°C) ..... 3.5 mW/°C
Storage Temperature Range ..... −55 to +125°C
Operating Temperature Range ..... −55 to +125°C
Lead Temperature (1/16" from case for 10 seconds) ..... 300°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

		PARAMETERS		J270 MIN	J270 TYP	J270 MAX	J271 MIN	J271 TYP	J271 MAX	UNIT	TEST CONDITIONS	
1	STATIC	I_{GSS}	Gate Reverse Current (Note 2)			200			200	pA	V_{DS} = 0, V_{GS} = 20V	
2		$V_{GS(off)}$	Gate-Source Cutoff Voltage	0.5		2.0	1.5		4.5	V	V_{DS} = −15V, I_D = −1nA	
3		BV_{GSS}	Gate-Source Breakdown Voltage	30			30				V_{DS} = 0, I_G = 1μA	
4		I_{DSS}	Saturation Drain Current (Note 3)	−2		−15	−6		−50	mA	V_{DS} = −15V, V_{GS} = 0	
5		I_G	Gate Current (Note 2)		15			60		pA	V_{DG} = −15V, I_D = $I_{DSS(min)}$	
6	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 3)	6,000		15,000	8,000		18,000	μmho	V_{DS} = −15V, V_{GS} = 0	f = 1 kHz
7		g_{os}	Common-Source Output Conductance			200			500			
8		C_{iss}	Common-Source Input Capacitance		20			20		pF		f = 1 MHz
9		C_{rss}	Common-Source Reverse Transfer Capacitance		5			5				
10		e_n	Equivalent Short-Circuit Input Noise Voltage		6			6		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = −10V, I_D = $I_{DSS(min)}$	f = 1 kHz

NOTES:
1. Geometry is symmetrical. Units may be operated with source and drain leads interchanged.
2. Approximately doubles for every 10°C increase in T_A.
3. Pulse test duration = 2 ms.

INTERSIL

2N5564/2N5565/2N5566 Dual Matched N-Channel JFET

FEATURES

- Specified Matching Characteristics
- High Gain — 7500μmho Minimum
- Low "ON" Resistance — 100Ω Maximum

DESIGNED FOR USE AS:

- Dual Matched Switches
- Wideband Differential Amplifiers

ABSOLUTE MAXIMUM RATINGS

(25°C unless otherwise noted)

Gate-Gate Voltage ..... ±80V
Gate-Drain or Gate-Source Voltage ..... −40V
Gate Current 50mA
Device Dissipation (Each Side), $T_A = 25°C$
(Derate 2.2 mW/°C) 325mW
Total Device Dissipation, $T_A = 25°C$
(Derate 3.3 mW/°C) 650mW
Storage Temperature Range ..... −65°C to +200°C
Lead Temperature
(1/16" from case for 10 seconds) ..... 300°C

PACKAGE DIMENSIONS TO—71

PIN	OUT	PIN	OUT
1	S_1	5	S_2
2	D_1	6	D_2
3	G_1	7	G_2

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

	SYMBOL	PARAMETERS	CONDITIONS		MIN.	MAX.	UNIT
STATIC	I_{GSS}	Gate-Reverse Current	$V_{GS} = -20V$, $V_{DS} = 0$			−100	pA
				150°C		−200	nA
	BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu A$, $V_{DS} = 0$		−40		V
	$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15V$, $I_D = 1nA$		−0.5	−3	
	$V_{GS(f)}$	Gate-Source Voltage	$V_{DS} = 0V$, $I_G = 2mA$			1.0	
	I_{DSS}	Saturation Drain Current (Note 1)	$V_{DS} = 15V$, $V_{GS} = 0$		5	30	mA
	$r_{DS(on)}$	Static Drain Source ON Resistance	$I_D = 1mA$, $V_{GS} = 0$			100	Ω
DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	$V_{DG} = 15V$, $I_D = 2mA$	f = 1kHz	7500	12,500	μmho
				f = 100MHz	7000		
	g_{os}	Common-Source Output Conductance		f = 1kHz		45	
	C_{rss}	Common-Source Reverse Transfer Capacitance		f = 1MHz		3	pF
	C_{iss}	Common-Source Input Capacitance				12	
	NF	Spot Noise Figure		f = 10Hz, $R_g = 1M$		1.0	dB
	$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		f = 10Hz		50	$\frac{nV}{\sqrt{Hz}}$

	SYMBOL	PARAMETERS	CONDITIONS		2N5564 MIN.	2N5564 MAX.	2N5565 MIN.	2N5565 MAX.	2N5566 MIN.	2N5566 MAX.	UNIT
MATCHING	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	$V_{DS} = 15V$, $V_{GS} = 0$		0.95	1	0.95	1	0.95	1	—
	$V_{GS1}-V_{GS2}$	Differential Gate-Source Voltage				5		10		20	mV
	$\frac{\Delta V_{GS1}-V_{GS2}}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)	$V_{DS} = 15V$, $I_D = 2mA$	$T_A = 25°C$, $T_B = 125°C$		10		25		50	μV/°C
				$T_A = -55°C$, $T_B = 25°C$		10		25		50	
	$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1 and 2)	$V_{DS} = 15V$, $I_D = 2mA$	f = 1kHz	0.95	1	0.90	1	0.90	1	—

NOTES:
1. Pulse test required, pulse width 300μs, duty cycle ≤3%.
2. Assumes smaller value in numerator.
3. Measured at end points, T_A and T_B.

INTERSIL

IMF5564/IMF5565/IMF5566 Dielectrically Isolated Dual Monolithic Matched N-Channel JFET

FEATURES

- Low Noise (10nV/$\sqrt{Hz}$ at 10Hz)
- High Gain — 7500 μmho Minimum
- Specified Matching Characteristics
- Low "ON" Resistance — 100Ω Maximum

DESIGNED FOR USE IN:

- Dual Matched Switches
- Wideband Differential Amplifiers

ABSOLUTE MAXIMUM RATINGS

(25°C unless otherwise noted)

Gate-Gate Voltage ..... ±80V
Gate-Drain or Gate-Source Voltage ..... −40V
Gate Current 50mA
Device Dissipation (Each Side), $T_A = 25°C$
(Derate 2.2 mW/°C) 325mW
Total Device Dissipation, $T_A = 25°C$
(Derate 3.3 mW/°C) 650mW
Storage Temperature Range ..... −65°C to +200°C
Lead Temperature
(1/16" from case for 10 seconds) ..... 300°C

PACKAGE DIMENSIONS TO—71

PIN	OUT	PIN	OUT
1	S_1	5	S_2
2	D_1	6	D_2
3	G_1	7	G_2

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

	SYMBOL	PARAMETERS	CONDITIONS		MIN.	MAX.	UNIT
STATIC	I_{GSS}	Gate-Reverse Current	$V_{GS} = -20V$, $V_{DS} = 0$			−100	pA
				150°C		−200	nA
	BV_{GSS}	Gate-Source Breakdown Voltage	$I_G = -1\mu A$, $V_{DS} = 0$		−40		V
	$V_{GS(off)}$	Gate-Source Cutoff Voltage	$V_{DS} = 15V$, $I_D = 1nA$		−0.5	−3	
	$V_{GS(f)}$	Gate-Source Voltage	$V_{DS} = 0V$, $I_G = 2mA$			1.0	
	I_{DSS}	Saturation Drain Current (Note 1)	$V_{DS} = 15V$, $V_{GS} = 0$		5	30	mA
	$r_{DS(on)}$	Static Drain Source ON Resistance	$I_D = 1mA$, $V_{GS} = 0$			100	Ω
DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	$V_{DG} = 15V$, $I_D = 2mA$	f = 1kHz	7500	12,500	μmho
				f = 100MHz	7000		
	g_{os}	Common-Source Output Conductance		f = 1kHz		45	
	C_{rss}	Common-Source Reverse Transfer Capacitance		f = 1MHz		3	pF
	C_{iss}	Common-Source Input Capacitance				12	
	NF	Spot Noise Figure		f = 10Hz, $R_g = 1M$		1.0	dB
	$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		f = 10Hz		50	$\frac{nV}{\sqrt{Hz}}$

	SYMBOL	PARAMETERS	CONDITIONS		IMF5564 MIN.	IMF5564 MAX.	IMF5565 MIN.	IMF5565 MAX.	IMF5566 MIN.	IMF5566 MAX.	UNIT
MATCHING	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Notes 1 and 2)	$V_{DS} = 15V$, $V_{GS} = 0$		0.95	1	0.95	1	0.95	1	—
	$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage				5		10		20	mV
	$\Delta \frac{\lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 3)	$V_{DS} = 15V$, $I_D = 2mA$	$T_A = 25°C$, $T_B = 125°C$		10		25		50	μV/°C
				$T_A = -55°C$, $T_B = 25°C$		10		25		50	
	$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Notes 1 and 2)	$V_{DS} = 15V$, $I_D = 2mA$	f = 1kHz	0.95	1	0.90	1	0.90	1	—

NOTES:

1. Pulse test required, pulse width 300μs, duty cycle ≤3%.
2. Assumes smaller value in numerator.
3. Measured at ends points, T_A and T_B.

INTERSIL

2N3684 2N3685 2N3686 2N3687
N-Channel Silicon Planar Epitaxial JFET

FEATURES

- $C_{GSS} < 1.2$ pF

GENERAL DESCRIPTION

- Exceptionally high figure of merit
- Radiation Immunity
- Symmetrical devices for low-level choppers, data switches, multiplexers and low noise amplifiers
- Extremely low noise and capacitance
- High input impedance
- Zero offset
- High reliability silicon epitaxial planar construction

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	+260°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C

Maximum Voltages & Current

V_{GS}	Gate to Source Voltage	-50 V
V_{GD}	Gate to Drain Voltage	-50 V
I_G	Gate Current	50 mA

ORDERING INFORMATION

TO72	WAFER	CHIP
2N3684	2N3684/W	2N3684/D
2N3685	2N3685/W	2N3685/D
2N3686	2N3686/W	2N3686/D
2N3687	2N3687/W	2N3687/D

PACKAGE DIMENSIONS

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER		2N3684		2N3685		2N3686		2N3687		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate to Source Breakdown Voltage	-50		-50		-50		-50		V	V_{DS} = 0 V, I_G = 1.0 μA
V_P	Pinch-Off Voltage	2.0	5.0	1.0	3.5	0.6	2.0	0.3	1.2	V	V_{DS} = 20 V, I_D = 0.001 μA
I_{GSS}	Total Gate Leakage Current		-0.1		-0.1		-0.1		-0.1	nA	V_{GS} = -30 V, V_{DS} = 0
I_{GSS}	Total Gate Leakage Current (150°C)		-0.5		-0.5		-0.5		-0.5	μA	V_{GS} = -30 V, V_{DS} = 0 @150°C
I_{DSS}	Saturation Current, Drain-to-Source	2.5	7.5	1.0	3.0	0.4	1.2	0.1	0.5	mA	V_{GS} = 0 V, V_{DS} = 20 V
$\|Y_{fs}\|$	Forward Transadmittance	2000	3000	1500	2500	1000	2000	500	1500	μmhos	V_{DS} = 20 V, V_{GS} = 0 V f = 1 kHz
C_{iss}	Common Source Input Capacitance (Output Shorted)		4.0		4.0		4.0		4.0	pF	V_{DS} = 20 V, V_{GS} = 0, f = 1 kHz
G_{os}	Small Signal, Common Source Output Conductance (input shorted)		50		25		10		5	μmhos	V_{DS} = 20 V, V_{GS} = 0, f = 1 kHz
C_{rss}	Small Signal, Common Source Short Circuit Reverse Transfer Capacitance		1.2		1.2		1.2		1.2	pF	V_{DS} = 20 V, V_{GS} = 0, f = 1 kHz
R_{on}	On Resistance		600		800		1200		2400	Ohms	V_{DS} = 0, V_{GS} = 0
NF	Noise Figure (Spot)		0.5		0.5		0.5		0.5	dB	f = 100 Hz, R_G = 10 MΩ NBW = 6 Hz, V_{DS} = 10 V

INTERSIL

2N3821, 2N3822
N-Channel Silicon Planar Epitaxial JFET

FEATURES

- Low Capacity
- Up to 6500 μmho Transconductance

GENERAL DESCRIPTION

For small signal amplifier and oscillator applications.

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	+260°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C

Maximum Voltages & Current

V_{GS} Gate to Source Voltage	−50 V
V_{GD} Gate to Drain Voltage	−50 V
I_G Gate Current	10 mA

ORDERING INFORMATION

TO72	WAFER	CHIP
2N3821	2N3821/W	2N3821/D
2N3822	2N3822/W	2N3822/D

PACKAGE DIMENSIONS

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N3821 MIN	2N3821 MAX	2N3822 MIN	2N3822 MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−0.1		−0.1	nA	V_{GS} = −30 V, V_{DS} = 0	
			−0.1		−0.1	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−50		−50		V	I_G = −1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		−4		−6		V_{DS} = 15 V, I_D = 0.5 nA	
V_{GS}	Gate-Source Voltage	−0.5	−2				V_{DS} = 15 V, I_D = 50 μA	
				−1	−4		V_{DS} = 15 V, I_D = 200 μA	
I_{DSS}	Saturation Drain Current	0.5	2.5	2	10	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 3)	
g_{fs}	Common-Source Forward Transconductance (Note 1)	1500	4500	3000	6500	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
$\lvert y_{fs} \rvert$	Common-Source Forward Transadmittance	1500		3000				f = 100 MHz
g_{os}	Common-Source Output Conductance (Note 1)		10		20			f = 1 kHz
C_{iss}	Common-Source Input Capacitance		6		6	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		3		3			
NF	Noise Figure		5		5	dB	V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1 meg, BW = 5 Hz	f = 10 Hz
$\overline{e_n}$	Equivalent Input Noise Voltage		200		200	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 15 V, V_{GS} = 0, BW = 5 Hz	

NOTE: 1. These parameters are measured during a 2 msec interval 100 msec after d-c power is applied.

INTERSIL

2N3823
N-Channel Silicon J-FET

FOR VHF AMPLIFIER OSCILLATOR MIXER APPLICATIONS

- **Noise Figure < 2.5 dB at 100 MHz**
- **Low Capacitance**
- **Transconductance up to 6500 μmho**

PACKAGE DIMENSIONS

TO-72

NOTE: All dimensions in parenthesis are metric.

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Source Voltage ..... −30V
Gate-Drain Voltage ..... −30V
Gate Current ..... 10 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature ..... 300 mW
Storage Temperature Range ..... −65 to +200°C
Lead Temperature 1/16" From Case to 10 Sec ..... 300°C

PIN	OUT
1	S
2	D
3	G
4	C

ELECTRICAL CHARACTERISTICS (25°C)

CHARACTERISTIC		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−0.5	nA	V_{GS} = −20V, V_{DS} = 0	
			−0.5	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−30		V	I_G = 1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		−8		V_{DS} = 15V, I_D = 0.5 nA	
V_{GS}	Gate-Source Voltage	−1.0	−7.5		V_{DS} = 15V, I_D = 400 μA	
I_{DSS}	Saturation Drain Current	4	20	mA	V_{DS} = 15V, V_{GS} = 0 (Note 3)	
g_{fs}	Common-Source Forward Transconductance	3,500	6,500	μmho	V_{DS} = 15V, V_{GS} = 0	f = 1 kHz (Note 1)
$\|y_{fs}\|$	Common-Source Forward Transadmittance	3,200				f = 100 MHz
g_{os}	Common-Source Output Transconductance		35			f = 1 kHz (Note 1)
g_{iss}	Common-Source Input Conductance		800			f = 200 MHz
g_{oss}	Common-Source Output Conductance		200			
C_{iss}	Common-Source Input Capacitance		6	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		2			
NF	Noise Figure		2.5	dB	V_{DS} = 15V, V_{GS} = 0 R_G = 1 kΩ	f = 100 MHz

INTERSIL

2N3824
N-Channel
Silicon J-FET

FOR HIGH SPEED COMMUTATORS AND CHOPPERS

- r_{ds} < **250 ohms**
- $I_{D(off)}$ < **0.1 nA**

PACKAGE DIMENSIONS

TO-72

NOTE: All dimensions in parenthesis are metric.

PIN	OUT
1	S
2	D
3	G
4	C

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Source Voltage ..... −50V
Gate-Drain Voltage ..... −50V
Gate Current ..... 10 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature ..... 300 mW
Storage Temperature Range ..... −65 to +200°C
Lead Temperature (1/16" from case for 10 seconds) ..... 300°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

CHARACTERISTIC		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−0.1	nA	V_{GS} = −30V, V_{DS} = 0	
			−0.1	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−50		V	I_G = 1 μA, V_{DS} = 0	
$I_{D(off)}$	Drain Cutoff Current		0.1	nA	V_{DS} = 15V, V_{GS} = −8V	
			0.1	μA		150°C
$r_{ds(on)}$	Drain-Source ON Resistance		250	Ω	V_{GS} = 0V, I_D = 0	f = 1 kHz
C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 15V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		3	pF	V_{GS} = −8V, V_{DS} = 0	

INTERSIL

2N4117/A, 2N4118/A, 2N4119/A

N-Channel Silicon Planar Epitaxial JFET

FEATURES

- Low Leakage – $I_{GSS} < 1$ pA
- Low Capacitance – $C_{rss} < 1.5$ pF

GENERAL DESCRIPTION

Low leakage for low power avoid amplifiers.

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	-65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	300°C
Maximum Power Dissipation	
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C
Maximum Voltages & Current	
V_{GS} Gate to Source Voltage	-40 V
V_{GD} Gate to Drain Voltage	-40 V
I_G Gate Current	50 mA

ORDERING INFORMATION

TO72	WAFER	CHIP
2N4117	2N4117/W	2N4117/D
2N4117A	2N4117A/W	2N4117A/D
2N4118	2N4118/W	2N4118/D
2N4118A	2N4118A/W	2N4118A/D
2N4119	2N4119/W	2N4119/D
2N4119A	2N4119A/W	2N4119A/D

PACKAGE DIMENSIONS

PIN	OUT
1	S
2	D
3	G
4	C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4117 2N4117A*		2N4118 2N4118A*		2N4119 2N4119A*		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
BV_{GSS}	Gate-Source Breakdown Voltage	-40		-40		-40		V	$I_G = -1\ \mu A$, $V_{DS} = 0$
I_{GSS}	Gate Reverse Current		-10 -1*		-10 -1*		-10 -1*	pA	$V_{GS} = -20$ V, $V_{DS} = 0$
I_{GSS} (+100°C)	Gate Reverse Current		-25 -2.5*		-25 -2.5*		-25 -2.5*	nA	$V_{GS} = -20$ V, $V_{DS} = 0$
V_{GS} (off)	Gate-Source Pinch-Off Voltage	-0.6	-1.8	-1	-3	-2	-6	V	$V_{DS} = 10$ V, $I_D = 1$ nA
I_{DSS}	Drain Current at Zero Gate Voltage (Note 1)	0.02	0.09	0.08	0.24	0.20	0.60	mA	$V_{DS} = 10$ V $V_{GS} = 0$
g_{fs}	Common-Source Forward Transconductance (Note 1)	70	210	80	250	100	330	μmho	$V_{DS} = 10$ V f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	60		70		90		μmho	$V_{GS} = 0$, f = 30 MHz
g_{os}	Common-Source Output Conductance		3		5		10	μmho	$V_{DS} = 10$ V, $V_{GS} = 0$, f = 1 kHz
C_{iss}	Common-Source Input Capacitance		3		3		3	pF	$V_{DS} = 10$ V, $V_{GS} = 0$, f = 1 kHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5		1.5	pF	$V_{DS} = 10$ V, $V_{GS} = 0$, f = 1 kHz

NOTE: 1. Pulse test: Pulse duration of 2 ms used during test.

INTERSIL

2N4220/A, 2N4221/A, 2N4222/A

N-Channel Silicon Planar Epitaxial JFET

FEATURES

- $C_{rss} < 2$ pF
- Moderately High Forward Transconductance

GENERAL DESCRIPTION

For small signal applications – UHF amplifier, oscillator and mixer applications.

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	+260°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C

Maximum Voltages & Current

V_{GS}	Gate to Source Voltage	-30 V
V_{GD}	Gate to Drain Voltage	-30 V
I_G	Gate Current	10 mA

ORDERING INFORMATION

TO72	WAFER	CHIP
2N4220	2N4220/W	2N4220/D
2N4221	2N4221/W	2N4221/D
2N4222	2N4222/W	2N4222/D

PACKAGE DIMENSIONS

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4220,A MIN	2N4220,A MAX	2N4221,A MIN	2N4221,A MAX	2N4222,A MIN	2N4222,A MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-0.1		-0.1		-0.1	nA	V_{GS} = -15 V, V_{DS} = 0	
			-0.1		-0.1		-0.1	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	-30		-30		-30		V	I_G = -10 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		-4		-6		-8		V_{DS} = 15 V, I_D = 0.1 nA	
V_{GS}	Gate-Source Voltage	-0.5	-2.5	-1	-5	-2	-6	V	V_{DS} = 15 V, I_D = ( )	
		(50)	(50)	(200)	(200)	(500)	(500)	(μA)		
I_{DSS}	Saturation Drain Current (Note 3)	0.5	3	2	6	5	15	mA	V_{DS} = 15 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 3)	1000	4000	2000	5000	2500	6000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
$\|y_{fs}\|$	Common-Source Forward Transadmittance	750		750		750				f = 100 MHz
g_{os}	Common-Source Output Conductance (Note 3)		10		20		40			f = 1 kHz
C_{iss}	Common-Source Input Capacitance		6		6		6	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		2		2		2			
NF	Noise Figure ("A" Versions Only)		2.5		2.5		2.5	dB	V_{DS} = 15V, V_{GS} = 0 R_{GEN} = 1 MEG	f = 100 Hz

INTERSIL

2N4223, 2N4224

N-Channel Silicon Planar Epitaxial JFET

FEATURES

- NF = 3 dB Typical at 200 MHz
- $C_{rss} < 2$ pF

GENERAL DESCRIPTION

For VHF amplifier and mixer applications.

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Gate-Drain or Gate-Source Voltage	−30 V
Gate Current	10 mA
Drain Current	20 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature	300 mW
Storage Temperature Range	−65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

PACKAGE DIMENSIONS

TO-72

PIN	OUT
1	S
2	D
3	G
4	C

NOTE: FOR DIE STRUCTURE, REFER TO 2N4416

5000

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4223 MIN	2N4223 MAX	2N4224 MIN	2N4224 MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−0.25		−0.5	nA	V_{GS} = −20 V, V_{DS} = 0	
			−0.25		−0.5	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−30		−30		V	I_G = −10 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.1	−8	−0.1	−8	V	V_{DS} = 15 V, I_D = ( )	
		(0.25)	(0.25)	(0.5)	(0.5)	(nA)		
V_{GS}	Gate-Source Voltage	−1.0	−7.0	−1.0	−7.5	V		
		(0.3)	(0.3)	(0.2)	(0.2)	(mA)		
I_{DSS}	Saturation Drain Current	3	18	2	20	mA	V_{DS} = 15 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	3000	7000	2000	7500	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
C_{iss}	Common-Source Input Capacitance (Output Shorted)		6		6	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		2		2			
$\|y_{fs}\|$	Common-Source Forward Transadmittance	2700		1700		μmho	V_{DS} = 15 V, V_{GS} = 0	f = 200 MHz
g_{iss}	Common-Source Input Conductance (Output Shorted)		800		800			
g_{oss}	Common-Source Output Conductance (Input Shorted)		200		200			
G_{ps}	Small Signal Power Gain	10				dB		
NF	Noise Figure		5				V_{DS} = 15 V, V_{GS} = 0, R_{gen} = 1 K	

INTERSIL

2N4338, 2N4339 2N4340, 2N4341

N-Channel Silicon Planar Epitaxial JFET

FEATURES

- Exceptionally high figure of merit
- Radiation Immunity
- Symmetrical devices for low-level choppers, data switches, multiplexers and low noise amplifiers
- Extremely low noise and capacitance
- High input impedance
- Zero offset
- High reliability silicon epitaxial planar construction

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	+260°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C

Maximum Voltages & Current

V_{GS}	Gate to Source Voltage	−50 V
V_{GD}	Gate to Drain Voltage	−50 V
I_G	Gate Current	50 mA

ORDERING INFORMATION

TO18	WAFER	CHIP
2N4338	2N4338/W	2N4338/D
2N4339	2N4339/W	2N4339/D
2N4340	2N4340/W	2N4340/D
2N4341	2N4341/W	2N4341/D

PACKAGE DIMENSIONS

ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

PARAMETER		2N4338		2N4339		2N4340		2N4341		UNITS	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
I_{GSS}	Gate Reverse Current		−0.1		−0.1		−0.1		−0.1	nA	V_{GS} = −30 V, V_{DS} = 0	
			−0.1		−0.1		−0.1		−0.1	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−50		−50		−50		−50		V	I_G = −1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.3	−1	−0.6	−1.8	−1	−3	−2	−6		V_{DS} = 15 V, I_D = 0.1 μA	
$I_{D(off)}$	Drain Cutoff Current		0.05 (−5)		0.05 (−5)		0.05 (−5)		0.07 (−10)	nA (V)	V_{DS} = 15 V V_{GS} = ( )	
I_{DSS}	Saturation Drain Current (Note 3)	0.2	0.6	0.5	1.5	1.2	3.6	3	9	mA	V_{DS} = 15 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 3)	600	1800	800	2400	1300	3000	2000	4000	μmho	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
g_{os}	Common-Source Output Conductance		5		15		30		60			
r_{ds}	Drain-Source ON Resistance		2500		1700		1500		800	ohm	V_{DS} = 0, V_{GS} = 0	
C_{iss}	Common-Source Input Capacitance		7		7		7		7	pF	V_{DS} = 15 V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		3		3		3		3			
NF	Noise Figure		1		1		1		1	dB	V_{DS} = 15 V, V_{GS} = 0 R_{gen} = 1 meg, BW = 200 Hz	f = 1 kHz

INTERSIL

2N4416/A
N-Channel Silicon Planar Epitaxial JFET

FEATURES

- Silicon Planar Epitaxial Construction
- Low Noise – NF = 2.0 dB max. @ 100 MHz
  NF = 4.0 dB max. @ 400 MHz
- Low Feedback Capacitance – C_{rss} = 0.8 pF max.
- Low Output Capacitance – C_{oss} = 2.0 pF max.
- High Transconductance – g_{fs} = 4000 μmho min.
- High Power Gain – G_{ps} = 18 dB min. @ 100 MHz
  G_{ps} = 10 dB min. @ 400 MHz

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature TO72	−65°C to +200°C
Operating Junction Temperature TO72	+200°C
Lead Temperature (Soldering, 10 sec time limit)	+300°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	300 mW
Linear Derating TO72	1.7 mW/°C

Maximum Voltages & Current

		2N4416	2N4416A
V_{GS}	Gate to Source Voltage	−30 V	−35 V
V_{GD}	Gate to Drain Voltage	−30 V	−35 V
I_G	Gate Current	10 mA	10 mA

GENERAL DESCRIPTION

For UHF amplifier and mixer applications

ORDERING INFORMATION

TO92	WAFER	CHIP
2N4416	2N4416/W	2N4416/D
2N4416A	2N4416A/W	2N4416A/D

PACKAGE DIMENSIONS

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−0.1	nA	V_{GS} = −20 V, V_{DS} = 0	
			−0.1	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−30		V	I_G = −1 μA, V_{DS} = 0	2N4416
		−35				2N4416A
$V_{GS(off)}$	Gate-Source Cutoff Voltage		−6	V	V_{DS} = 15 V, I_D = 1 nA	2N4416
		−2.5	−6			2N4416A
I_{DSS}	Drain Current at Zero Gate Voltage	5	15	mA	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	4500	7500	μmho		
g_{os}	Common-Source Output Conductance		50	μmho		
C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	pF		f = 1 MHz
C_{iss}	Common-Source Input Capacitance		4	pF		
C_{oss}	Common-Source Output Capacitance		2			

PARAMETER		100 MHz MIN	100 MHz MAX	400 MHz MIN	400 MHz MAX	UNIT	TEST CONDITIONS
g_{iss}	Common-Source Input Conductance		100		1000	μmho	V_{DS} = 15 V, V_{GS} = 0
b_{iss}	Common-Source Input Susceptance		2500		10,000	μmho	
g_{oss}	Common-Source Output Conductance		75		100	μmho	
b_{oss}	Common-Source Output Susceptance		1000		4000	μmho	
g_{fs}	Common-Source Forward Transconductance			4000		μmho	
G_{ps}	Common-Source Power Gain	18		10		dB	V_{DS} = 15 V, I_D = 5 mA
NF	Noise Figure		2		4	dB	V_{DS} = 15 V, I_D = 5 mA, R_G = 1 KΩ

INTERSIL

2N4867/A 2N4868/A 2N4869/A N-Channel Silicon Planar Epitaxial JFET

FEATURES

- Lowest Noise Voltage – $e_n \leqslant 5\ nV/\sqrt{Hz}$
- Low Leakage – $I_{GSS} \leqslant 0.25\ nA$
- High Gain – $Y_{fs} \geqslant 1300 \leqslant 4000\ \mu mho$

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	+260°C
Maximum Power Dissipation	
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C
Maximum Voltages & Current	
V_{GS} Gate to Source Voltage	−40 V
V_{GD} Gate to Drain Voltage	−40 V
I_G Gate Current	50 mA

ORDERING INFORMATION

TO72	WAFER	CHIP
2N4867	2N4867/W	2N4867/D
2N4867A	2N4867A/W	2N4867A/D
2N4868	2N4868/W	2N4868/D
2N4868A	2N4868A/W	2N4868A/D
2N4869	2N4869/W	2N4869/D
2N4869A	2N4869A/W	2N4869A/D

PACKAGE DIMENSIONS

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4867 2N4867A MIN	2N4867 2N4867A MAX	2N4868 2N4868A MIN	2N4868 2N4868A MAX	2N4869 2N4869A MIN	2N4869 2N4869A MAX	UNIT	TEST CONDITIONS		
I_{GSS}	Gate Reverse Current		−0.25		−0.25		−0.25	nA	$V_{GS} = -30\ V,\ V_{DS} = 0$		150°C
			−0.25		−0.25		−0.25	μA			
BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		−40		V	$I_G = -1\ \mu A,\ V_{DS} = 0$		
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.7	−2	−1	−3	−1.8	−5		$V_{DS} = 20\ V,\ I_D = 1\ \mu A$		
I_{DSS}	Saturation Drain Current (Note 1)	0.4	1.2	1	3	2.5	7.5	mA	$V_{DS} = 20\ V,\ V_{GS} = 0$		
g_{fs}	Common-Source Forward Transconductance (Note 1)	700	2000	1000	3000	1300	4000	μmho	$V_{DS} = 20\ V,\ V_{GS} = 0$		f = 1 kHz
g_{os}	Common-Source Output Conductance		1.5		4		10				
C_{rss}	Common-Source Reverse Transfer Capacitance		5		5		5	pF			f = 1 MHz
C_{iss}	Common-Source Input Capacitance		25		25		25				
$\bar{e}_n$	Short Circuit Equivalent Input Noise Voltage		20		20		20	nV/√Hz	$V_{DS} = 10\ V,\ V_{GS} = 0$	2N4867 Series	f = 10 Hz
			10		10		10			2N4867A Series	
			10		10		10			2N4867 Series	f = 1 kHz
			5		5		5			2N4867A Series	
NF	Spot Noise Figure		1		1		1	dB	$V_{DS} = 10\ V,\ V_{GS} = 0$; $R_{gen} = 20\ K$, 2N4867 Series; $5\ K$, 2N4867A Series		f = 1 kHz

NOTE: 1. Pulse test duration 2 ms.

INTERSIL

2N5397 2N5398
N-Channel Silicon Planar Epitaxial JFET

FEATURES

- G_{ps} = 10 dB Typical (Common Gate) at 450 MHz
- NF = 3.5 dB Typical at 450 MHz
- C_{rss} = 1 pF Typical

GENERAL DESCRIPTION

For UHF amplifier, mixer and oscillator and video amplifier applications

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (Soldering, 10 sec time limit)	300°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C

Maximum Voltages & Current

V_{GS}	Gate to Source Voltage	−25 V
V_{GD}	Gate to Drain Voltage	−25 V
I_G	Gate Current	10 mA

ORDERING INFORMATION

TO72	WAFER	CHIP
2N5397	2N5397/W	2N5397/D

PACKAGE DIMENSIONS

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5397 MIN	2N5397 MAX	2N5398 MIN	2N5398 MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−0.1		−0.1	nA	V_{GS} = −15 V, V_{DS} = 0	
			−0.1		−0.1	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−25		−25		V	V_{DS} = 0, I_G = −1 μA	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−1.0	−6.0	−1.0	−6.0		V_{DS} = 10 V, I_D = 1 nA	
I_{DSS}	Saturation Drain Current	10	30	5	40	mA	V_{DS} = 10 V, V_{DS} = 0	
$V_{GS(f)}$	Gate-Source Forward Voltage		1		1	V	V_{DS} = 0, I_G = 1 mA	
g_{fs}	Common-Source Forward Transconductance (Note 1)	6000	10,000	5500	10,000	μmho	V_{DS} = 10V, I_D = 10 mA V_{DS} = 10 V, V_{GS} = 0	f = 1 kHz
g_{oss}	Common-Source Output Conductance		200		400		V_{DS} = 10 V, I_D = 10 mA V_{DS} = 10 V, V_{GS} = 0	
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.3	pF	V_{DS} = 10 V, I_D = 10 mA V_{DS} = 10 V, V_{GS} = 0	f = 1 MHz
C_{iss}	Common-Source Input Capacitance		5.0		5.5		V_{DG} = 10 V, I_D = 10 mA V_{DS} = 10 V, V_{GS} = 0	
g_{iss}	Common-Source Input Conductance		2000		3000	μmho	V_{DG} = 10 V, I_D = 10 mA V_{DG} = 10 V, V_{GS} = 0	f = 450 MHz
g_{oss}	Common-Source Output Conductance		400		500		V_{DG} = 10 V, I_D = 10 mA V_{DS} = 10 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 1)	5500	9000	5000	10,000		V_{DG} = 10 V, I_D = 10 mA V_{DS} = 10 V, V_{GS} = 0	
G_{ps}	Common-Source Power Gain (neutralized)	15				dB	V_{DG} = 10 V, I_D = 10 mA	
NF	Common-Source, Spot Noise Figure (neutralized)		3.5					

Note 1: Pulse test duration = 2ms

INTERSIL

2N5457, 2N5458, 2N5459
N-Channel Silicon JFET

SMALL-SIGNAL AMPLIFIERS, CHOPPERS AND CONTROLLED RESISTORS

ABSOLUTE MAXIUMUM RATINGS
(25°C unless otherwise noted)

SYMBOL	RATING	VALUE	UNIT
V_{DS}	Drain-Source Voltage	25	Vdc
V_{DG}	Drain-Gate Voltage	25	Vdc
$V_{GS(r)}$	Reverse Gate-Source Voltage	25	Vdc
I_G	Gate Current	10	mAdc
P_D	Total Device Dissipation @ T_A = 25°C Derate above 25°C	310 2.82	mW mW/°C
T_J	Operating Junction Temperature	135	°C
T_{stg}	Storage Temperature Range	−65 to +150	°C

PACKAGE DIMENSIONS

TO-92

PIN	OUT
1	D
2	S
3	G

NOTE: FOR DIE STRUCTURE, REFER TO 2N4338 FAMILY.

5010

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
OFF CHARACTERISTICS							
BV_{GSS}	Gate-Source Breakdown Voltage	−25	−60		Vdc	I_G = −10 μAdc, V_{DS} = 0	
I_{GSS}	Gate Reverse Current		.05	−1.0 −200	nAdc	V_{GS} = −15 Vdc, V_{DS} = 0 V_{GS} = −15 Vdc, V_{DS} = 0, T_A = 100°C	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5 −1.0 −2.0		−6.0 −7.0 −8.0	Vdc	V_{DS} = 15 Vdc, I_D = 10 nAdc	2N5457 2N5458 2N5459
V_{GS}	Gate-Source Voltage		2.5 3.5 4.5		Vdc	V_{DS} = 15 Vdc, I_D = 100 μAdc V_{DS} = 15 Vdc, I_D = 200 μAdc V_{DS} = 15 Vdc, I_D = 400 μAdc	2N5457 2N5458 2N5459
ON CHARACTERISTICS							
I_{DSS}	Zero-Gate-Voltage Drain Current	1.0 2.0 4.0	3.0 6.0 9.0	5.0 9.0 16	mAdc	V_{DS} = 15 Vdc, V_{GS} = 0	2N5457 2N5458 2N5459
DYNAMIC CHARACTERISTICS							
$\|y_{fs}\|$	Forward Transfer Admittance	1000 1500 2000	3000 4000 4500	5000 5500 6000	μmhos	V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 kHz	2N5457 2N5458 2N5459
$\|y_{os}\|$	Output Admittance		10	50	μmhos	V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 kHz	
C_{iss}	Input Capacitance		4.5	7.0	pF	V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 MHz	
C_{rss}	Reverse Transfer Capacitance		1.5	3.0	pF	V_{DS} = 15 Vdc, V_{GS} = 0, f = 1 MHz	

INTERSIL

2N5484 2N5485 2N5486

N-Channel Silicon Planar Epitaxial JFET

GENERAL DESCRIPTION

For VHF/UHF amplifier, mixer and oscillator applications.

FEATURES

- Specified for 400 MHz Operation
- Can Be Used as a Low Capacitance Switch
- Economy Packaging
- $C_{rss} < 1.0$ pF

ABSOLUTE MAXIMUM RATINGS

Drain-Gate Voltage	25 V
Source Gate Voltage	25 V
Drain Current	30 mA
Forward Gate Current	10 mA
Total Device Dissipation @ 25°C	310 mW
Derate above 25°C	2.82 mW/°C
Operating Junction Temperature Range	−65°C to +150°C
Storage Temperature Range	−65°C to +150°C

PACKAGE DIMENSIONS

TO-92

PIN	OUT
1	D
2	S
3	G

NOTE: FOR DIE STRUCTURE, SEE 2N4416

5000

1

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5484 MIN	2N5484 MAX	2N5485 MIN	2N5485 MAX	2N5486 MIN	2N5486 MAX	UNITS	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−1.0		−1.0		−1.0	nA	V_{GS} = −20 V, V_{DS} = 0	
			−200		−200		−200			T_A = +100°C
BV_{GSS}	Gate-Source Breakdown Voltage	−25		−25		−25		V	I_G = −1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.3	−3.0	−0.5	−4.0	−2.0	−6.0		V_{DS} = 15 V, I_D = 10 nA	
I_{DSS}	Saturation Drain Current	1.0	5.0	4.0	10	8.0	20	mA	V_{DS} = 15 V, V_{GS} = 0 (Note 1)	
g_{fs}	Common-Source Forward Transconductance	3000	6000	3500	7000	4000	8000	μmhos	V_{DS} = 15 V, V_{GS} = 0	f = 1 kHz
g_{os}	Common-Source Output Conductance		50		60		75			
$Re(y_{fs})$	Common-Source Forward Transconductance	2500								f = 100 MHz
				3000		3500				f = 400 MHz
$Re(y_{os})$	Common-Source Output Conductance		75							f = 100 MHz
					100		100			f = 400 MHz
$Re(y_{is})$	Common-Source Input Conductance		100							f = 100 MHz
					1000		1000			f = 400 MHz
C_{iss}	Common-Source Input Capacitance		5.0		5.0		5.0	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.0		1.0		1.0			
C_{oss}	Common-Source Output Capacitance		2.0		2.0		2.0			
NF	Noise Figure		2.5		2.5		2.5	dB	V_{DS} = 15 V, V_{GS} = 0, R_G = 1 MΩ	f = 1 kHz
			3.0						V_{DS} = 15 V, I_D = 1 mA, R_G = 1 kΩ	f = 100 MHz
					2.0		2.0		V_{DS} = 15 V, I_D = 4 mA, R_G = 1 kΩ	
					4.0		4.0			f = 400 MHz
G_{ps}	Common-Source Power Gain	16	25						V_{DS} = 15 V, I_D = 1 mA	f = 100 MHz
				18	30	18	30		V_{DS} = 15 V, I_D = 4 mA	
				10	20	10	20			f = 400 MHz

INTERSIL

ITE4416

N-Channel Silicon Planar Epitaxial JFET

FEATURES

- **Silicon Planar Epitaxial Construction**
- **Low Noise — NF = 2.0 dB max. @ 100 MHz**
  NF = 4.0 dB max. @ 400 MHz
- **Low Feedback Capacitance — C_{rss} = 0.8 pF max.**
- **Low Output Capacitance — C_{oss} = 2.0 pF max.**
- **High Transconductance — g_{fs} = 4000 μmho min.**
- **High Power Gain — G_{ps} = 18 dB min. @ 100 MHz**
  G_{ps} = 10 dB min. @ 400 MHz

1

GENERAL DESCRIPTION

For UHF amplifier and mixer applications

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures
- Storage Temperature TO92 ..... -55°C to +125°C
- Operating Junction Temperature TO92 ..... +125°C
- Lead Temperature (Soldering, 10 sec time limit) +300°C

Maximum Power Dissipation
- Device Dissipation @ Free Air Temperature .. 300 mW
- Linear Derating TO92 ..... 3.0 mW/°C

Maximum Voltages & Current ITE4416
- V_{GS} Gate to Source Voltage ..... -30V
- V_{GD} Gate to Drain Voltage ..... -30V
- I_G Gate Current ..... 10 mA

PACKAGE DIMENSIONS

TO-92

PIN	OUT
1	S
2	D
3	G

5000

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-0.1	nA	V_{GS} = -20V, V_{DS} = 0	
			-0.1	μA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	-30		V	I_G = -1μA, V_{DS} = 0	ITE4416
$V_{GS(off)}$	Gate-Source Cutoff Voltage		-6		V_{DS} = 15V, I_D = 1 nA	ITE4416
I_{DSS}	Drain Current at Zero Gate Voltage	5	15	mA	V_{DS} = 15V, V_{GS} = 0	f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	4500	7500	μmho		
g_{os}	Common-Source Output Conductance		50			
C_{rss}	Common-Source Reverse Transfer Capacitance		0.8	pF		f = 1 MHz
C_{iss}	Common-Source Input Capacitance		4			
C_{oss}	Common-Source Output Capacitance		2			

	PARAMETER	100 MHz MIN	100 MHz MAX	400 MHz MIN	400 MHz MAX	UNIT	TEST CONDITIONS
g_{iss}	Common-Source Input Conductance		100		1000	μmho	V_{DS} = 15V, V_{GS} = 0
b_{iss}	Common-Source Input Susceptance		2500		10,000		
g_{oss}	Common-Source Output Conductance		75		100		
b_{oss}	Common-Source Output Susceptance		1000		4000		
g_{fs}	Common-Source Forward Transconductance			4000			
G_{ps}	Common-Source Power Gain	18		10		dB	V_{DS} = 15V, I_D = 5 mA
NF	Noise Figure		2		4		V_{DS} = 15V, I_D = 5 mA, R_G = 1 KΩ

INTERSIL

U308, U309, U310, U311
N-Channel Silicon JFET

FEATURES

- High Power Gain
  - 15dB Typical at 100MHz, Common Gate
  - 10dB Typical at 450MHz, Common Gate
- Low Single Sideband Noise Figure
  - 1.5dB Typical at 100MHz, Common Gate
  - 3.2dB Typical at 450MHz, Common Gate
- Wide Dynamic Range – Greater than 100dB
- Offered in Wide Variety of Packages for Most Any Circuit Configuration.

GENERAL DESCRIPTION

This family of N-channel Junction FETs are designed and characterized for VHF and UHF applications requiring high gain and low noise figure. The forward transconductance is relatively flat out to 1000MHz. Applications for these devices in military, commercial and consumer communications equipment include low noise, high gain RF amplifiers, low noise mixers with conversion gain, and low noise, ultra stable RF oscillators.

ORDERING INFORMATION

TO52	TO72	TO92	WAFER	CHIP
U308		U308-TO92	U308/W	U308/D
U309		U309-TO92	U309/W	U309/D
U310		U310-TO92	U310/W	U310/D
	U311		U311/W	U311/D

1

PACKAGE DIMENSIONS

PIN	OUT
1	S
2	D
3	G
4	C

PIN	OUT
1	S
2	D
3	G

PIN	OUT
1	S
2	D
3	G

ABSOLUTE MAXIMUM RATINGS (25°C)

	TO-52	TO-72	TO-92
Gate-Drain or Gate-Source Voltage	–25V	–25V	–25V
Gate Current	20mA	10mA	10mA
Total Power Dissipation	500mW	300mW	300mW
Power Derating (to maximum operating temperature)	4.0mW/°C	2.4mW/°C	3.0mW/°C
Operating Temperature Range	–65 to 150°C	–65 to +150°C	–55 to +125°C
Storage Temperature Range	–65 to 200°C	–65 to +200°C	–55 to +125°C
Lead Temperature (1/16" from case for 10 sec)	300°C	300°C	300°C

ELECTRICAL CHARACTERISTICS FOR U308, U309 and U310 (25°C unless otherwise noted)

CHARACTERISTIC		U308 MIN	U308 TYP	U308 MAX	U309 MIN	U309 TYP	U309 MAX	U310 MIN	U310 TYP	U310 MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current			-150			-150			-150	pA	V_{GS} = -15 V	
				-150			-150			-150	nA	V_{GS} = 0	T = 125°C
BV_{GSS}	Gate-Source Breakdown Voltage	-25			-25			-25			V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1.0		-6.0	-1.0		-4.0	-2.5		-6.0	V	V_{DS} = 10 V, I_D = 1 nA	
I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	V_{DS} = 10 V, V_{GS} = 0	
$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	I_G = 10 mA, V_{DS} = 0	
g_{fg}	Common-Gate Forward Transconductance (Note 1)	10		20	10		20	10		18	mmho	V_{DS} = 10 V, I_D = 10 mA	f = 1 kHz
g_{ogs}	Common-Gate Output Conductance			150			150			150	μmho		
C_{gd}	Drain-Gate Capacitance			2.5			2.5			2.5	pF	V_{GS} = -10 V, V_{DS} = 10 V	f = 1 MHz
C_{gs}	Gate-Source Capacitance			5.0			5.0			5.0			
$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 10 V, I_D = 10 mA	f = 100 Hz
g_{fg}	Common-Gate Forward Transconductance		12			12			12		mmho	V_{DS} = 10 V, I_D = 10 mA	f = 100 MHz
			11			11			11				f = 450 MHz
g_{ogs}	Common-Gate Output Conductance		0.18			0.18			0.18				f = 100 MHz
			0.7			0.7			0.7				f = 450 MHz
G_{pg}	Common-Gate Power Gain		15			15			15		dB		f = 100 MHz
			10			10			10				f = 450 MHz
NF	Noise Figure		1.5			1.5			1.5				f = 100 MHz
			3.2			3.2			3.2				f = 450 MHz

ELECTRICAL CHARACTERISTICS FOR U311 (25°C unless otherwise noted)

CHARACTERISTIC		U311 MIN	U311 MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-150	pA	V_{GS} = -15V, V_{DS} = 0	
			-150	nA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	-25		V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-6		V_{DS} = 10V, I_D = 1 nA	
I_{DSS}	Saturation Drain Current (Note 1)	20	60	mA	V_{DS} = 10V, V_{GS} = 0	
$V_{GS(f)}$	Gate-Source Forward Voltage		1	V	I_G = 1 mA, V_{DS} = 0	
g_{fg}	Common-Gate Forward Transconductance (Note 1)	10,000	20,000	μmho	V_{DS} = 10V, I_D = 10 mA	f = 1 kHz
g_{ogs}	Common-Gate Output Conductance		150			
C_{gd}	Gate-Drain Capacitance		2.5	pF	V_{DG} = 10V, I_D = 5 mA	f = 1 MHz
C_{gs}	Gate-Source Capacitance		5.0			

NOTE: 1. Pulse test duration = 2 ms.

INTERSIL

J308, J309, J310
N-Channel Silicon J-FET

DESIGNED FOR USE AS
- VHF/UHF Amplifiers
- Oscillators
- Mixers

FEATURES
- Industry Standard Part In Low Cost Plastic Package
- High Power Gain
  11 dB Typical at 450 MHz
  Common-Gate
- Low Noise - 2.7 dB Typical at 450 MHz
- Wide Dynamic Range Greater than 100 dB
- Easily Matches to 75 Ω Input

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage 25V
Source-Gate Voltage 25V
Forward Gate Current ..... 10 mA
Total Device Dissipation (T_{LEAD} = 25°C) ..... 625 mW
Derate above 25°C ..... 5.68 mW/°C
Storage Temperature Range ..... −55 to +150°C
Operating Junction Temperature Range .... −55 to +135°C

PACKAGE DIMENSIONS

TO-92

PIN	OUT
1	D
2	S
3	G

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

		PARAMETERS		J308 MIN	J308 TYP	J308 MAX	J309 MIN	J309 TYP	J309 MAX	J310 MIN	J310 TYP	J310 MAX	UNIT	TEST CONDITIONS	
1		BV_{GSS}	Gate-Source Breakdown Voltage	−25			−25			−25			V	$I_G = -1\mu A$, $V_{DS} = 0$	
2	S	I_{GSS}	Gate Reverse Current			−1.0			−1.0			−1.0	nA	$V_{GS} = -15V$,	
3	T					−1.0			−1.0			−1.0	μA	$V_{DS} = 0$	T = +125°C
4	A	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−1.0		−6.5	−1.0		−4.0	−2.0		−6.5	V	$V_{DS} = 10V$, $I_D = 1nA$	
5	T I C	I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	$V_{DS} = 10V$, $V_{GS} = 0$	
6		$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	$V_{DS} = 0$, $I_G = 1$ mA	
7		g_{fs}	Common-Source Forward Transconductance	8,000		20,000	10,000		20,000	8,000		18,000			
8		g_{os}	Common-Source Output Conductance			200			200			200			
9	D Y N	g_{fg}	Common-Gate Forward Transconductance		13,000			13,000			12,000		μmhos	$V_{DS} = 10V$, $I_D = 10mA$	f = 1 kHz
10	A M	g_{og}	Common Gate Output Conductance		150			150			150				
11	I C	C_{gd}	Gate-Drain Capacitance		1.8	2.5		1.8	2.5		1.8	2.5			
12		C_{gs}	Gate-Source Capacitance		4.3	5.0		4.3	5.0		4.3	5.0	pF	$V_{DS} = 0$, $V_{GS} = -10V$	f = 1 MHz
13		e_n	Equivalent Short-Circuit Input Noise Voltage		10			10			10		$\frac{nV}{\sqrt{Hz}}$	$V_{DS} = 10V$, $I_D = 10$ mA	f = 100 Hz
14		$Re(y_{fs})$	Common-Source Forward Transconductance		12			12			12				
15		$Re(y_{fg})$	Common-Gate Input Conductance		14			14			14				
16	H I	$Re(y_{is})$	Common-Source Input Conductance		0.4			0.4			0.4		mmho		f = 105 MHz
17	F	$Re(y_{os})$	Common-Source Output Conductance		0.15			0.15			0.15			$V_{DS} = 10V$, $I_D = 10mA$	
18	R E	G_{pg}	Common-Gate Power Gain at Noise Match		16			16			16				
19	Q	NF	Noise Figure		1.5			1.5			1.5		dB		
20		G_{pg}	Common-Gate Power Gain at Noise Match		11			11			11				f = 450 MHz
21		NF	Noise Figure		2.7			2.7			2.7				

INTERSIL

J308, J309, J310
N-Channel Silicon J-FET

DESIGNED FOR USE AS
- VHF/UHF Amplifiers
- Oscillators
- Mixers

FEATURES
- Industry Standard Part In Low Cost Plastic Package
- High Power Gain
  - 11 dB Typical at 450 MHz
  - Common-Gate
- Low Noise - 2.7 dB Typical at 450 MHz
- Wide Dynamic Range Greater than 100 dB
- Easily Matches to 75 Ω Input

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-Gate Voltage 25V
Source-Gate Voltage 25V
Forward Gate Current ..... 10 mA
Total Device Dissipation (T_{LEAD} = 25°C) ..... 625 mW
Derate above 25°C ..... 5.68 mW/°C
Storage Temperature Range ..... −55 to +150°C
Operating Junction Temperature Range .... −55 to +135°C

PACKAGE DIMENSIONS

TO-92

PIN	OUT
1	D
2	S
3	G

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

		PARAMETERS		J308 MIN	J308 TYP	J308 MAX	J309 MIN	J309 TYP	J309 MAX	J310 MIN	J310 TYP	J310 MAX	UNIT	TEST CONDITIONS	
1		BV_{GSS}	Gate-Source Breakdown Voltage	−25			−25			−25			V	I_G 1μA, V_{DS} = 0	
2	STATIC	I_{GSS}	Gate Reverse Current			−1.0			−1.0			−1.0	nA	V_{GS} −15V,	
3						−1.0			−1.0			−1.0	μA	V_{DS} 0	T = +125°C
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−1.0		−6.5	−1.0		−4.0	−2.0		−6.5	V	V_{DS} 10V, I_D = 1nA	
5		I_{DSS}	Saturation Drain Current (Note 1)	12		60	12		30	24		60	mA	V_{DS} 10V, V_{GS} = 0	
6		$V_{GS(f)}$	Gate-Source Forward Voltage			1.0			1.0			1.0	V	V_{DS} 0, I_G = 1 mA	
7	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	8,000		20,000	10,000		20,000	8,000		18,000	μmhos	V_{DS} = 10V, I_D 10mA	f = 1 kHz
8		g_{os}	Common-Source Output Conductance			200			200			200			
9		g_{fg}	Common-Gate Forward Transconductance		13,000			13,000			12,000				
10		g_{og}	Common Gate Output Conductance		150			150			150				
11		C_{gd}	Gate-Drain Capacitance		1.8	2.5		1.8	2.5		1.8	2.5	pF	V_{DS} = 0, V_{GS} = −10V	f = 1 MHz
12		C_{gs}	Gate-Source Capacitance		4.3	5.0		4.3	5.0		4.3	5.0			
13		e_n	Equivalent Short-Circuit Input Noise Voltage		10			10			10		nV/√Hz	V_{DS} = 10V, I_D = 10 mA	f = 100 Hz
14	HIGH FREQ	$Re(y_{fs})$	Common-Source Forward Transconductance		12			12			12		mmho	V_{DS} = 10V, I_D = 10mA	f = 105 MHz
15		$Re(y_{ig})$	Common-Gate Input Conductance		14			14			14				
16		$Re(y_{is})$	Common-Source Input Conductance		0.4			0.4			0.4				
17		$Re(y_{os})$	Common-Source Output Conductance		0.15			0.15			0.15				
18		G_{pg}	Common-Gate Power Gain at Noise Match		16			16			16		dB		
19		NF	Noise Figure		1.5			1.5			1.5				
20		G_{pg}	Common-Gate Power Gain at Noise Match		11			11			11				f = 450 MHz
21		NF	Noise Figure		2.7			2.7			2.7				

INTERSIL

2N2606
2N2607, 2N2608
2N2609/2N2609 JTX
P-Channel Silicon Planar Epitaxial JFET

GENERAL DESCRIPTION

- Low-level Choppers
- Data Switches
- Commutators

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +200°C
Operating Junction Temperature	+175°C
Lead Temperature (Soldering, 10 sec. time limit)	+260°C

Maximum Power Dissipation

Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	2.0 mW/°C

Maximum Voltages & Current

V_{DG}	Drain to Gate Voltage	30 V
V_{SG}	Source to Gate Voltage	30 V
I_G	Gate Current	50 mA

PACKAGE DIMENSIONS

TO-18

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

Characteristic		Test Conditions		2N2606 Min	2N2606 Max	2N2607 Min	2N2607 Max	2N2608 Min	2N2608 Max	2N2609 Min	2N2609 Max	Unit
I_{GSS}	Gate-Source Cutoff Current †	V_{GS} = 30 V, V_{DS} = 0			1		3		10		30	nA
		V_{GS} = 5 V, V_{DS} = 0, T_A = 150° C			1		3		10		30	μA
BV_{GDS}	Gate-Drain Breakdown Voltage	I_G = 1 μA, V_{DS} = 0		30		30		30		30		V
V_P	Gate-Source Pinch-Off Voltage	V_{DS} = -5 V, I_D = -1 μA		1	4	1	4	1	4	1	4	V
I_{DSS}	Drain Current at Zero Gate Voltage	V_{DS} = -5 V, V_{GS} = 0		-0.10	-0.50	-0.30	-1.50	-0.90	-4.50	-2	-10	mA
g_{fs}	Small-Signal Common-Source Forward Transconductance	V_{DS} = -5 V, V_{GS} = 0, f = 1 kHz		110		330		1000		2500		μmho
C_{iss}	Gate-Source Input Capacitance	V_{DS} = -5 V, V_{GS} = 1 V, f = 140 kHz			6		10		17		30	pF
NF	Noise Figure	V_{DS} = -5 V, V_{GS} = 0, f = 1 kHz	R_G = 10 MΩ		3		3					dB
			R_G = 1 MΩ						3		3	

INTERSIL

2N3329 2N3330 2N3331
P-Channel Silicon Planar Epitaxial JFET

GENERAL DESCRIPTION

For
- Multi-Purpose Amplifiers
- Analog Multipliers
- Modulators

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Gate-Drain and Gate-Source Voltage	20 V
Gate Current	10 mA
Total Device Dissipation at (or below) 25°C Free-Air Temperature	0.3 W
Storage Temperature Range	−65°C to +200°C
Lead Temperature (1/16" from case for 10 seconds)	230°C

1

PACKAGE DIMENSIONS

TO-72

PIN	OUT
1	S
2	G
3	D
4	C

NOTE: FOR DIE STRUCTURE, SEE 2N5460 FAMILY

5503B

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N3329 MIN	2N3329 MAX	2N3330 MIN	2N3330 MAX	2N3331 MIN	2N3331 MAX	UNITS	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		0.01		0.01		0.01	μA	V_{GS} = 10 V, V_{DS} = 0	
			10		10		10		V_{GS} = 10 V, V_{DS} = 0, T_A = 150°C	
BV_{GSS}	Gate-Source Breakdown Voltage	20		20		20		V	I_G = 10 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		5		6		8		V_{DS} = −5 V, I_D = −10 μA	
I_{DSS}	Saturation Drain Current	−1	−3	−2	−6	−5	−15	mA	V_{DS} = −10 V, V_{GS} = 0	
$r_{DS(on)}$	Drain-Source ON Resistance		1000		800		600	Ω	I_D = −100 μA, V_{GS} = 0	
g_{is}	Common-Source Input Conductance		0.2		0.2		0.2	μmho	V_{DS} = −10 V; 2N3329: I_D = −1 mA; 2N3330: I_D = −2 mA; 2N3331: I_D = −5 mA	f = 1 kHz
g_{rs}	Common-Source Reverse Transfer Conductance		0.1		0.1		0.1			
g_{os}	Common-Source Output Conductance		20		40		100			
g_{fs}	Common-Source Forward Transconductance	1000	2000	1500	3000	2000	4000			
		900		1350		1800				f = 10 MHz
C_{iss}	Common-Source Input Capacitance		20		20		20	pF	V_{DS} = −10 V, V_{GS} = 1 V	f = 1 MHz
NF	Noise Figure		3		3		4	dB	V_{DS} = −5 V, I_D = −1 mA, R_{gen} = 1 MΩ	f = 1 kHz
NF	Noise Figure								V_{DS} = −5 V, I_D = −1 mA, R_{gen} = 10 MΩ	f = 10 Hz

INTERSIL

2N5265 thru 2N5270
P-Channel Silicon Planar Epitaxial JFET

GENERAL DESCRIPTION

P-Channel junction depletion mode (Type A) field-effect transistors designed for general-purpose amplifier applications.

MAXIMUM RATINGS

SYMBOL	RATING	VALUE	UNIT
V_{DS}	Drain-Source Voltage	60	Vdc
V_{DG}	Drain-Gate Voltage	60	Vdc
$V_{GS(r)}$	Reverse Gate-Source Voltage	60	Vdc
I_D	Drain Current	20	mAdc
$I_{G(f)}$	Gate Current-Forward	10	mAdc
P_D	Total Device Dissipation @ $T_A = 25°C$	300	mW
	Derate above 25°C	2.0	mW/°C
T_{stg}	Storage Temperature Range	−65 to +200	°C
T_J	Operating Junction Temperature Range	−65 to +175	°C

PACKAGE DIMENSIONS

PIN	OUT
1	S
2	G
3	D
4	C

NOTE: FOR DIE STRUCTURE, SEE 2N5460 FAMILY.

5503B

ELECTRICAL CHARACTERISTICS ($T_A = 25°C$ unless otherwise noted)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
OFF CHARACTERISTICS						
$V_{(BR)GSS}$	Gate-Source Breakdwon Voltage	60		Vdc	$I_G = 10\ \mu Adc$, $V_{DS} = 0$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		3.0	Vdc	$V_{DS} = 15$ Vdc, $I_D = 1.0\ \mu Adc$	2N5265, 2N5266
			6.0			2N5267, 2N5268
			8.0			2N5269, 2N5270
I_{GSS}	Gate Reverse Current		2.0	nAdc	$V_{GS} = 30$ Vdc, $V_{DS} = 0$	
			2.0	μAdc	$V_{GS} = 30$ Vdc, $V_{DS} = 0$, $T_A = 150°C$	
ON CHARACTERISTICS						
I_{DSS}	Zero-Gate Voltage Drain Current	0.5	1.0	mAdc	$V_{DS} = 15$ Vdc, $V_{GS} = 0$	2N5265
		0.8	1.6			2N5266
		1.5	3.0			2N5267
		2.5	5.0			2N5268
		4.0	8.0			2N5269
		7.0	14			2N5270
V_{GS}	Gate-Source Voltage	0.3	1.5	Vdc	$V_{DS} = 15$ Vdc, $I_D = 0.05$ mAdc	2N5265
		0.4	2.0		$V_{DS} = 15$ Vdc, $I_D = 0.08$ mAdc	2N5266
		1.0	4.0		$V_{DS} = 15$ Vdc, $I_D = 0.15$ mAdc	2N5267
		1.0	4.0		$V_{DS} = 15$ Vdc, $I_D = 0.25$ mAdc	2N5268
		2.0	6.0		$V_{DS} = 15$ Vdc, $I_D = 0.4$ mAdc	2N5269
		2.0	6.0		$V_{DS} = 15$ Vdc, $I_D = 0.7$ mAdc	2N5270
SMALL-SIGNAL CHARACTERISTICS						
$\lvert y_{fs} \rvert$	Forward Transadmittance	900	2700	μmhos	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 kHz	2N5265
		1000	3000			2N5266
		1500	3500			2N5267
		2000	4000			2N5268
		2200	4500			2N5269
		2500	5000			2N5270
g_{fs}	Forward Transconductance	800		μmhos	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 100 MHz	2N5265
		900				2N5266
		1400				2N5267
		1700				2N5268
		1900				2N5269
		2100				2N5270
$\lvert y_{os} \rvert$	Output Admittance		75	μmhos	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 kHz	
C_{iss}	Input Capacitance		7.0	pF	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 MHz	
C_{rss}	Reverse Transfer Capacitance		2.0	pF	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 MHz	
NF	Common-Source Noise Figure		2.5	dB	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, $R_G = 1.0$ M ohm, f = 100 Hz, BW = 1.0 Hz	
$\overline{e}_n$	Equivalent Short-Circuit Input Noise Voltage		115	$nV/\sqrt{Hz}$	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 100 Hz, BW = 1.0 Hz	

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INTERSIL

2N5460 thru 2N5465
P-Channel Silicon Planar Epitaxial JFET

MAXIMUM RATINGS

RATING	SYMBOL	2N5460 2N5461 2N5462	2N5463 2N5464 2N5465	UNITS
Drain-Gate Voltage	V_{DG}	40	60	Vdc
Reverse Gate-Source Voltage	$V_{GS(r)}$	40	60	Vdc
Forward Gate Current	$I_{G(f)}$	10		mAdc
Total Device Dissipation @ $T_A = 25°C$	P_D	310		mW
Derate above 25°C		2.82		mW/°C
Storage Temperature Range	T_{stg}	−65 to +150		°C
Operating Junction Temperature Range	T_J	−65 to +135		°C

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PACKAGE DIMENSIONS

5503B

TO-92

PIN	OUT
1	S
2	D
3	G

ORDERING INFORMATION

TO92	WAFER	CHIP
2N5460	2N5460/W	2N5460/D
2N5461	2N5461/W	2N5461/D
2N5462	2N5462/W	2N5462/D
2N5463	2N5463/W	2N5463/D
2N5464	2N5464/W	2N5464/D
2N5465	2N5465/W	2N5465/D

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS	
$V_{(BR)GSS}$	Gate-Source Breakdown Voltage	40 60			Vdc	$I_G = 10\ \mu Adc$, $V_{DS} = 0$	2N5460, 2N5461, 2N5462 2N5463, 2N5464, 2N5465
$V_{GS(off)}$	Gate-Source Cutoff Voltage	0.75 1.0 1.8		6.0 7.5 9.0	Vdc	$V_{DS} = 15$ Vdc, $I_D = 1.0\ \mu Adc$	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465
I_{GSS}	Gate Reverse Current			5.0 5.0 1.0 1.0	na na μAdc na	$V_{GS} = 20$ Vdc, $V_{DS} = 0$ $V_{GS} = 30$ Vdc, $V_{DS} = 0$ $V_{GS} = 20$ Vdc, $V_{DS} = 0$, $T_A = 100°C$ $V_{GS} = 30$ Vdc, $V_{DS} = 0$, $T_A = 100°C$	2N5460, 2N5461, 2N5462 2N5463, 2N5464, 2N5465 2N5460, 2N5461, 2N5462 2N5463, 2N5464, 2N5465
ON CHARACTERISTICS							
I_{DSS}	Zero-Gate Voltage Drain Current	1.0 2.0 4.0		5.0 9.0 16	mAdc	$V_{DS} = 15$ Vdc, $V_{GS} = 0$	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465
V_{GS}	Gate-Source Voltage	0.5 0.8 1.5		4.0 4.5 6.0	Vdc	$V_{DS} = 15$ Vdc, $I_D = 0.1$ mAdc $V_{DS} = 15$ Vdc, $I_D = 0.2$ mAdc $V_{DS} = 15$ Vdc, $I_D = 0.4$ mAdc	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465
SMALL-SIGNAL CHARACTERISTICS							
g_{fs}	Forward Transadmittance	1000 1500 2000		4000 5000 6000	μmhos	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 kHz	2N5460, 2N5463 2N5461, 2N5464 2N5462, 2N5465
g_{os}	Output Admittance			75	μmhos	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 kHz	
C_{iss}	Input Capacitance		5.0	7	pF	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 MHz	
C_{rss}	Reverse Transfer Capacitance		1.0	2.0	pF	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 1.0 MHz	
NF	Common-Source Noise Figure		1.0	2.5	dB	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, $R_G = 1.0$ Megohm, f = 100 Hz, BW = 1.0 Hz	
$\overline{e_n}$	Equivalent Short-Circuit Input Noise Voltage		60	115	$nV/\sqrt{Hz}$	$V_{DS} = 15$ Vdc, $V_{GS} = 0$, f = 100 Hz, BW = 1.0 Hz	

INTERSIL

U304, U305, U306
P-Channel JFET

DESIGNED FOR USE IN
- Analog Switches
- Commutators
- Choppers

FEATURES
- ON Resistance <85 ohms on U304
- $I_{D(off)}$ <500 pA
- Switches directly from T^2L Logic (U306)

PACKAGE DIMENSIONS

5508B

NOTE: SUBSTRATE IS GATE

TO-18

PIN	OUT
1	S
2	G-C
3	D

ABSOLUTE MAXIMUM RATINGS (25°C)

Reverse Gate-Drain or Gate-Source Voltage (Note 1) 30V
Gate Current ..... 50 mA
Total Device Dissipation, Free-Air
(Derate 2.8 mW/°C) ..... 350 mW
Storage Temperature Range ..... −65 to +150°C
Lead Temperature
(1/16" from case for 60 seconds) ..... 300°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted.

		Characteristic		U304 Min	U304 Max	U305 Min	U305 Max	U306 Min	U306 Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		500		500		500	pA	V_{GS} = 20V, V_{DS} = 0	
2	STATIC	I_{GSS}	Gate Reverse Current		1.0		1.0		1.0	μA	V_{GS} = 20V, V_{DS} = 0	150°C
3	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	30		30		30		V	I_G = 1 μA, V_{DS} = 0	
4	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	5	10	3	6	1	4	V	V_{DS} = −15V, I_D = −1μA	
5	STATIC	$V_{DS(on)}$	Drain-Source ON Voltage		−1.3		−0.8		−0.6	V	V_{GS} = 0, I_D = −15mA(U304), I_D = −7mA (U305), I_D = −3mA (U306)	
6	STATIC	I_{DSS}	Saturation Drain Current (Note 2)	−30	−90	−15	−60	−5	−25	mA	V_{DS} = −15V, V_{GS} = 0	
7	STATIC	$I_{D(off)}$	Drain Cutoff Current		−500		−500		−500	pA	V_{DS} = −15V, V_{GS} = 12V (U304), V_{GS} = 7V (U305), V_{GS} = 5V (U306)	
8	STATIC	$I_{D(off)}$	Drain Cutoff Current		−1.0		−1.0		−1.0	μA	V_{DS} = −15V, V_{GS} = 12V (U304), V_{GS} = 7V (U305), V_{GS} = 5V (U306)	150°C
9	STATIC	$r_{DS(on)}$	Static Drain-Source ON Resistance		85		110		175	Ω	V_{GS} = 0V, I_D = −1mA	
10	DYN	$r_{ds(on)}$	Drain-Source ON Resistance		85		110		175	Ω	V_{GS} = 0V, I_D = 0	f = 1 kHz
11	DYN	C_{iss}	Common-Source Input Capacitance		27		27		27	pF	V_{DS} = −15V, V_{GS} = 0	f = 1 MHz
12	DYN	C_{rss}	Common-Source Reverse Transfer Capacitance		7		7		7	pF	V_{DS} = 0, V_{GS} = 12V (U304) V_{GS} = 7V (U305), V_{GS} = 5V (U306)	f = 1 MHz
13	SWITCH	$t_{d(on)}$	Turn-ON Delay Time		20		25		25	ns		
14	SWITCH	t_r	Rise Time		15		25		35	ns		
15	SWITCH	$t_{d(off)}$	Turn-OFF Delay Time		10		15		20	ns		
16	SWITCH	t_f	Fall Time		25		40		60	ns		

	U304	U305	U306
V_{DD}	−10V	−6V	−6V
$V_{GS(off)}$	12V	7V	5V
R_L	580Ω	743Ω	1800Ω
$V_{GS(on)}$	0	0	0
$I_{D(on)}$	−15mA	−7mA	−3mA

NOTES:
1. Due to symmetrical geometry these units may be operated with source and drain leads interchanged.
2. Pulse test pulsewidth = 300μs, duty cycle ≤3%.

INTERSIL

2N3921, 2N3922 Dual Monolithic Matched N-Channel J-FETS (Pair)

MATCHED FET PAIRS FOR DIFFERENTIAL AMPLIFIERS

- I_G < 250 pA (25 nA at 100°C)
- g_{oss} < 20 μmhos (I_D = 700 μA)
- Matched V_{GS}, ΔV_{GS}, and g_{fs}

PACKAGE DIMENSIONS

TO-71

NOTE: All dimensions in parenthesis are metric.

PIN	OUT	PIN	OUT
1	S_1	5	S_2
2	D_1	6	D_2
3	G_1	7	G_2

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage ..... −50V
Gate Current ..... 50 mA
Total Device Dissipation (Derate 1.7 mW/°C to 200°C) ..... 300 mW
Storage Temperature Range ..... −65 to +200°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

CHARACTERISTIC		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−1	nA	V_{GS} = −30V, V_{DS} = 0	
			−1	μA		100°C
BV_{DGO}	Drain-Gate Breakdown Voltage	50			I_D = 1 μA, I_S = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage		−3	V	V_{DS} = 10V, I_D = 1 nA	
V_{GS}	Gate-Source Voltage	−0.2	−2.7		V_{DS} = 10V, I_D = 100μA	
I_G	Gate Operating Current		−250	pA	V_{DG} = 10V, I_D = 700μA	
			−25	nA		100°C
I_{DSS}	Saturation Drain Current (Note 1)	1	10	mA	V_{DS} = 10V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 1)	1500	7500	μmho	V_{DS} = 10V, V_{GS} = 0	f = 1 kHz
g_{os}	Common-Source Output Conductance		35			
C_{iss}	Common-Source Input Capacitance		18	pF		
C_{rss}	Common-Source Reverse Transfer Capacitance		6			
g_{fs}	Common-Source Forward Transconductance	1500		μmho	V_{DG} = 10V, I_D = 700 μA	f = 1 kHz
g_{oss}	Common-Source Output Conductance		20			
NF	Spot Noise Figure		2	dB	V_{DS} = 10V, V_{GS} = 0	f = 1 kHz, R_G = 1 meg

CHARACTERISTIC		2N3921		2N3922		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX			
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5	mV	V_{DG} = 10V, I_D = 700 μA	
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature		10		25	μV/°C		T_A = 0°C t_B = 100°C
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.95	1.0	0.95	1.0	—		f = 1 kHz

INTERSIL

2N3954 2N3954A 2N3955 2N3955A 2N3956 2N3957 2N3958

Monolithic Dual, Matched N-Channel JFETS (Pair)

GENERAL DESCRIPTION

Matched FET pairs for differential amplifiers. This family of general purpose FETs is characterized for low and medium frequency differential amplifiers requiring low offset voltage, drift, noise, and capacitance.

FEATURES

- Offset Voltage < 5 mV • Drift < 5 μV/°C
- Low Capacitance – C_{iss} = 4 pF Max
- Spot Noise Figure = 0.5 dB Max
- Superior Tracking Ability
- Low Output Conductance – g_{os} = 35 μmho Max

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Any Case-To-Lead Voltage	±100 V
Gate-Drain or Gate-Source Voltage	–50 V
Gate-To-Gate Voltage	±100 V
Gate Current	50 mA
Total Device Dissipation 85°C (Each Side)	250 mW
Case Temperature (Both Sides)	500 mW
Power Derating (Each Side)	2.86 mW/°C
(Both Sides)	4.3 mW/°C
Storage Temperature Range	–65°C to +125°C
Lead Temperature (1/16" from case for 10 seconds)	300°C

ORDERING INFORMATION

TO71	WAFER	CHIP
2N3954	2N3954/W	2N3954/D
2N2954A	2N3954A/W	2N3954A/D
2N3955	2N3955/W	2N3955/D
2N3955A	2N3955A/W	2N3955A/D
2N3956	2N3956/W	2N3956/D
2N3957	2N3957/W	2N3957/D
2N3958	2N3958/W	2N3958/D

TO-71

PACKAGE DIMENSIONS

6017

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N3954		2N3954A		2N3955		2N3955A		2N3956		2N3957		2N3958		UNIT	TEST CONDITIONS	
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX			
I_{GSS}	Gate Reverse Current		–100		–100		–100		–100		–100		–100		–100	pA	V_{GS} = –30 V, V_{DS} = 0	
			–500		–500		–500		–500		–500		–500		–500	nA		T_A = 125°C
BV_{GSS}	Gate-Source Breakdown Voltage	–50		–50		–50		–50		–50		–50		–50		V	V_{DS} = 0, I_G = 1 μA	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	–1.0	–4.5	–1.0	–4.5	–1.0	–4.5	–1.0	–4.5	–1.0	–4.5	–1.0	–4.5	–1.0	–4.5	V	V_{DS} = 20 V, I_D = 1 nA	
$V_{GS(f)}$	Gate-Source Forward Voltage		2.0		2.0		2.0		2.0		2.0		2.0		2.0	V	V_{DS} = 0, I_G = 1 mA	
V_{GS}	Gate-Source Voltage		–4.2		–4.2		–4.2		–4.2		–4.2		–4.2		–4.2	V	V_{DS} = 20 V	I_D = 50 μA
		–0.5	–4.0	–0.5	–4.0	–0.5	–4.0	–0.4	–4.0	–0.5	–4.0	–0.5	–4.0	–0.5	–4.0	V		I_D = 200 μA
I_G	Gate Operating Current		–50		–50		–50		–50		–50		–50		–50	pA	V_{DS} = 20 V, I_D = 200 μA	
			–250		–250		–250		–250		–250		–250		–250	nA		T_A = 125°C
I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
		1000		1000		1000		1000		1000		1000		1000				f = 200 MHz
g_{os}	Common-Source Output Conductance		35		35		35		35		35		35		35			f = 1 kHz
C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0		4.0		4.0		4.0		4.0	pF		f = 1 MHz
C_{rss}	Common Source Reverse Transfer Capacitance		1.2		1.2		1.2		1.2		1.2		1.2		1.2			
C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5		1.5		1.5		1.5		1.5		V_{DG} = 10 V, I_S = 0	
NF	Common-Source Spot Noise Figure		0.5		0.5		0.5		0.5		0.5		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = 0, R_G = 10 MΩ	f = 100 Hz
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		10		10		10		10		10		10		10	nA	V_{DS} = 20 V, I_D = 200 μA	T = 125°C
I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.90	1.0	0.85	1.0		V_{DS} = 20 V, V_{GS} = 0	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5.0		5.0		10.0		5.0		15		20		25	mV	V_{DS} = 20 V, I_D = 200 μA	
$\Delta\lvert V_{GS1}-V_{GS2}\rvert$	Gate-Source Differential Voltage Change with Temperature		0.8		0.4		2.0		1.2		4.0		6.0		8.0			T = 25°C to –55°C
			1.0		0.5		2.5		1.5		5.0		7.5		10.0			T = 25°C to 125°C
g_{fs1}/g_{fs2}	Transconductance Ratio	0.97	1.0	0.97	1.0	0.97	1.0	0.95	1.0	0.95	1.0	0.90	1.0	0.85	1.0			f = 1 kHz

INTERSIL

2N5196 2N5197 2N5198 2N5199
Low Noise Monolithic Dual Matched N-Channel JFETs (PAIR)

ABSOLUTE MAXIMUM RATINGS (Note 1)
@ 25°C (unless otherwise noted)

Maximum Temperatures
- Storage Temperature: -65°C to +200°C
- Operating Junction Temperature: +150°C
- Lead Temperature (Soldering, 10 sec. time limit): +300°C

Maximum Power Dissipation
- Device Dissipation @ 85°C Free Air Temperature
  - One Side: 250 mW
  - Both Sides: 500 mW
- Linear Derating
  - One Side: 2.56 mW/°C
  - Both Sides: 4.3 mW/°C

Maximum Voltages & Currents
- V_{GS} Gate to Source Voltage: -50 V
- V_{GD} Gate to Drain Voltage: -50 V
- I_G Gate Current: 50 mA

ORDERING INFORMATION

TO71	WAFER	CHIP
2N5196	2N5196/W	2N5196/D
2N5197	2N5197/W	2N5197/D
2N5198	2N5198/W	2N5198/D
2N5199	2N5199/W	2N5199/D

6017

SOURCE 3 x 6 MIL
DRAIN 3 x 3 MIL
GATE 3 x 3 MIL

PACKAGE DIMENSIONS

TO-71

ELECTRICAL CHARACTERISTICS (25°C unless otherwise specified)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-25	pA	V_{GS} = -30 V, V_{DS} = 0	
			-50	nA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-0.7	-4		V_{DS} = 20 V, I_D = 1 nA	
V_{GS}	Gate-Source Voltage	-0.2	-3.8			
I_G	Gate Operating Current		-15	pA	V_{DG} = 20 V, I_D = 200 μA	
			-15	nA		125°C
I_{DSS}	Saturation Drain Current (Note 1)	0.7	7	mA	V_{DS} = 20 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	4000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
g_{fs}	Common-Source Forward Transconductance (Note 1)	700	1500		V_{DG} = 20 V, I_D = 200 μA	
g_{os}	Common-Source Output Conductance		50		V_{DS} = 20 V, V_{GS} = 0	
g_{os}	Common-Source Output Conductance		4		V_{DG} = 20 V, I_D = 200 μA	
C_{iss}	Common-Source Input Capacitance		6	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		2			
NF	Spot Noise Figure		0.5	dB		f = 100 Hz, R_G = 10 MΩ
$\overline{e}_n$	Equivalent Input Noise Voltage		0.020 20	$\frac{\mu}{\sqrt{Hz}}$		f = 1 kHz

PARAMETER		2N5196 MIN	2N5196 MAX	2N5197 MIN	2N5197 MAX	2N5198 MIN	2N5198 MAX	2N5199 MIN	2N5199 MAX	UNIT	TEST CONDITIONS	
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		5		5		5		5	nA	V_{DG} = 20 V, I_D = 200 μA	125°C
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.95	1	—	V_{DS} = 20 V, V_{GS} = 0 V	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.95	1	—	V_{DG} = 20 V, I_D = 200 μA	f = 1 kHz
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15	mV		
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temperature (Note 2)		5		10		20		40	μV/°C		T_A = 25°C, T_B = 125°C
			5		10		20		40			T_A = -55°C, T_B = 25°C
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		1		1		1		1	μmho		f = 1 kHz

NOTE: 1. Pulse test required, pulsewidth = 300 μs, duty cycle ≤ 3%.
2. Measured at end points, T_A and T_B.

INTERSIL

2N5452, 2N5453, 2N5454
Monolithic Dual Matched N-Channel JFETS (PAIR)

FEATURES

- Offset Voltage 5 mV
- Drift 5 μV/°C
- Low Capacitance
- Low Output Conductance — 1 μmho Max

GENERAL DESCRIPTION

Matched FET pairs for differential amplifiers. This family of general purpose FETs is characterized for low and medium frequency differential amplifier applications requiring low drift and low offset voltage.

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures
- Storage Temperature — -65°C to +200°C
- Operating Junction Temperature — +150°C
- Lead Temperature (Soldering, 10 sec. time limit) — +300°C

Maximum Power Dissipation
- Device Dissipation @ 85°C Free Air Temperature
  - One Side — 250 mW
  - Both Sides — 500 mW
- Linear Derating
  - One Side — 2.86 mW/°C
  - Both Sides — 4.3 mW/°C

Maximum Voltages & Currents
- V_{GS} Gate to Source Voltage — -50 V
- V_{GD} Gate to Drain Voltage — -50 V

PACKAGE DIMENSIONS

TO-71

NOTE: FOR DIE STRUCTURE, SEE 2N5196 FAMILY

6017

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ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	PARAMETER	2N5452 MIN	2N5452 MAX	2N5453 MIN	2N5453 MAX	2N5454 MIN	2N5454 MAX	UNITS	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		-100		-100		-100	pA	V_{GS} = -30 V, V_{DS} = 0	
			-200		-200		-200	nA		T_A = 150°C
BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		V	V_{DS} = 0, I_G = -1 μA	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	-1	-4.5	-1	-4.5	-1	-4.5	V	V_{DS} = 20 V, I_D = 1 nA	
V_{GS}	Gate-Source Voltage	-0.2	-4.2	-0.2	-4.2	-0.2	-4.2	V	V_{DS} = 20 V, I_D = 50 μA	
$V_{GS(f)}$	Gate-Source Forward Voltage		2		2		2	V	V_{DS} = 0, I_G = 1 mA	
I_{DSS}	Saturation Drain Current	0.5	5.0	0.5	5.0	0.5	5.0	mA	V_{DS} = 20 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	1000	3000	1000	3000	1000	3000	μmho	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
		1000		1000		1000		μmho		f = 100 MHz
g_{os}	Common-Source Output Conductance		3.0		3.0		3.0	μmho		f = 1 kHz
			1.0		1.0		1.0	μmho	V_{DS} = 20 V, I_D = 200 μA	
C_{iss}	Common-Source Input Capacitance		4.0		4.0		4.0	pF	V_{DS} = 20 V, V_{GS} = 0	f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2		1.2		1.2	pF		
C_{dgo}	Drain-Gate Capacitance		1.5		1.5		1.5	pF	V_{DG} = 10 V, I_S = 0	
$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 20 V, V_{GS} = 0	f = 1 kHz
NF	Common-Source Spot Noise Figure		0.5		0.5		0.5	dB	V_{DS} = 20 V, V_{GS} = 0, R_G = 10 MΩ	f = 100 Hz
I_{DSS1}/I_{DSS2}	Drain Saturation Current Ratio	0.95	1.0	0.95	1.0	0.95	1.0		V_{DS} = 20 V, V_{GS} = 0	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5.0		10.0		15.0	mV	V_{DS} = 20 V, I_D = 200 μA	
$\Delta\lvert V_{GS1}-V_{GS2}\rvert$	Gate-Source Voltage Differential Change with Temperature		0.4		0.8		2.0	mV		T = 25°C to -55°C
			0.5		1.0		2.5	mV		T = 25°C to +125°C
g_{fs1}/g_{fs2}	Transconductance Ratio	0.97	1.0	0.97	1.0	0.95	1.0			
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.25		0.25		0.25	μmhos		f = 1 kHz

INTERSIL

2N5515 thru 2N5524

Monolithic Dual Matched N-Channel Silicon Planar Epitaxial JFETS (Pair)

GENERAL DESCRIPTION

Matched FET pairs for differential amplifiers.

ABSOLUTE MAXIMUM RATINGS (Note 1)

@25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +200°C

Maximum Power Dissipation	ONE SIDE	BOTH SIDES
Device Dissipation	250 mW	500 mW
@ Free Air Temperature	85°C	85°C
Linear Derating	3.85 mW/°C	7.7 mW/°C

Maximum Voltages & Current

V_{GS}	Gate to Source Voltage	-40 V
V_{GD}	Gate to Drain Voltage	-40 V
I_G	Gate Current	50 mA

FEATURES

- Tight Temperature Tracking – $\Delta V_{GS} < 5\ \mu V/°C$
- Tight Matching –
  - $V_{GS} < 5$ mV
  - $I_G < 10$ nA @ 125°C
  - $g_{fs} < 3\%$
  - $g_{oss} < .1\ \mu$mho
- High Common Mode-Rejection – CMRR < 100 db
- Low Noise – $e_n < 15$ nV / $\sqrt{Hz}$ @10 Hz

ORDERING INFORMATION

TO71	WAFER	CHIP
2N5515	2N5515/W	2N5515/D
2N5516	2N5516/W	2N5516/D
2N5517	2N5517/W	2N5517/D
2N5518	2N5518/W	2N5518/D
2N5519	2N5519/W	2N5519/D
2N5520	2N5520/W	2N5520/D
2N5521	2N5521/W	2N5521/D
2N5522	2N5522/W	2N5522/D
2N5523	2N5523/W	2N5523/D
2N5524	2N5524/W	2N5524/D

PACKAGE DIMENSIONS

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
I_{GSS}	Gate Reverse Current (+ 25°C) (+150°C)		-250 -250	pA nA	V_{GS} = -30 V, V_{DS} = 0
BV_{GSS}	Gate-Source Breakdown Voltage	-40		V	I_G = 1 μA, V_{DS} = 0
V_P	Gate-Source Pinch-Off Voltage	-0.7	-4	V	V_{DS} = 20 V, I_D = 1 nA
I_{DSS}	Drain Current at Zero Gate Voltage (Note 2)	0.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0
g_{fs}	Common-Source Forward Transconductance (Note 2)	1000	4000	μmho	V_{DS} = 20 V, V_{GS} = 0 f = 1 kHz
g_{oss}	Common-Source Output Conductance		10	μmho	V_{DS} = 20 V, V_{GS} = 0 f = 1 kHz
C_{rss}	Common-Source Reverse Transfer Capacitance		5	pF	V_{DS} = 20 V, V_{GS} = 0 f = 1 MHz
C_{iss}	Common-Source Input Capacitance		25	pF	V_{DS} = 20 V, V_{GS} = 0 f = 1 MHz
$\bar{e}_n$	Equivalent Input Noise Voltage 2N5515-19 2N5520-24 2N5515-24		30 15 10	nV/√Hz nV/√Hz nV/√Hz	V_{DG} = 20 V, I_D = 200 μA f = 10 Hz V_{DG} = 20 V, I_D = 200 μA f = 10 Hz V_{DG} = 20 V, I_D = 200 μA f = 1 kHz
I_G	Gate Current (+ 25°C) (+125°C)		-100 -100	pA nA	V_{DG} = 20 V, I_D = 200 μA
V_{GS}	Gate Source Voltage	-0.2	-3.8	V	V_{DG} = 20 V, I_D = 200 μA
g_{fs}	Common-Source Forward Transconductance (Note 2)	500	1000	μmho	V_{DG} = 20 V, I_D = 200 μA f = 1 kHz
g_{oss}	Common-Source Output Conductance		1	μmho	V_{DG} = 20 V, I_D = 200 μA

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5515,20		2N5516,21		2N5517,22		2N5518,23		2N5519,24		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
I_{DSS1}	Drain Current Ratio at	0.95	1	0.95	1	0.95	1	0.95	1	0.90	1		V_{DS} = 20 V, V_{GS} = 0
I_{DSS2}	Zero Gate Voltage (Note 2)												
$\lvert I_{G1} - I_{G2}\rvert$	Differential Gate Current (+125°C)		10		10		10		10		10	nA	V_{DG} = 20 V, I_D = 200 μA
g_{fs1}	Transconductance Ratio	0.97	1	0.97	1	0.95	1	0.95	1	0.90	1		V_{DG} = 20 V, I_D = 200 μA
g_{fs2}	(Note 2)												f = 1 KHz
$\lvert g_{oss1} - g_{oss2}\rvert$	Differential Output Conductance		0.1		0.1		0.1		0.1		0.1	μmho	V_{DG} = 20 V, I_D = 200 μA f = 1 KHz
$\lvert V_{GS1} - V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15		15	mV	V_{DG} = 20 V, I_D = 200 μA
$\frac{\Delta\lvert V_{GS1} - V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (T_A = +25°C to +125°C)		5		10		20		40		80	μV/°C	V_{DG} = 20 V, I_D = 200 μA
$\frac{\Delta\lvert V_{GS1} - V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (T_A = +25 to -55°C)		5		10		20		40		80	μV/°C	V_{DG} = 20 V, I_D = 200 μA
CMRR	Common Mode Rejection Ratio (Note 3)	100		100		90						dB	V_{DD} = 10 to 20 V, I_D = 200 μA

NOTES:

1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
2. Pulse duration of 28mS used during test.
3. CMRR = $20\text{Log}_{10}\Delta V_{DD}/\Delta\lvert V_{GS1} - V_{GS2}\rvert$, ($\Delta V_{DD}$ = 10V)

INTERSIL

2N5902 thru 2N5909

Dual Monolithic Matched N-Channel JFETs (PAIR)

GENERAL DESCRIPTION

Matched FET pairs for differential amplifiers.

FEATURES

- Tracking < 5 μV/°C
- I_G < 1 pa
- Matched V_{GS}, $\Delta V_{GS}/\Delta T$, g_{fs}, & g_{oss}

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Gate-Drain or Gate-Source Voltage	−40 V
Gate Current	10 mA
Device Dissipation (Each Side), T_A = 25°C (Derate 3 mW/°C)	367 mW
Total Device Dissipation, T_A = 25°C (Derate 4 mW/°C)	500 mW
Storage Temperature Range	−65°C to +150°C

ORDERING INFORMATION

TO99	WAFER	CHIP
2N5902	2N5902/W	2N5902/D
2N5903	2N5903/W	2N5903/D
2N5904	2N5904/W	2N5904/D
2N5905	2N5905/W	2N5905/D

TO99	WAFER	CHIP
2N5906	2N5906/W	2N5906/D
2N5907	2N5907/W	2N5907/D
2N5908	2N5908/W	2N5908/D
2N5909	2N5909/W	2N5909/D

PACKAGE DIMENSIONS

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5902-5 MIN	2N5902-5 MAX	2N5906-9 MIN	2N5906-9 MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−5		−2	pA	V_{GS} = −20 V, V_{DS} = 0	
			−10		−5	nA		125°C
BV_{GSS}	Gate-Source Breakdown Voltage	−40		−40		V	I_G = −1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.6	−4.5	−0.6	−4.5		V_{DS} = 10 V, I_D = 1 nA	
V_{GS}	Gate Source Voltage		−4		−4			
I_G	Gate Operating Current		−3		−1	pA	V_{DG} = 10 V, I_D = 30 μA	
			−3		−1	nA		125°C
I_{DSS}	Saturation Drain Current	30	500	30	500	μA	V_{DS} = 10 V, V_{GS} = 0	
g_{fs}	Common-Source Forward Transconductance	70	250	70	250	μmho		f = 1 kHz
g_{os}	Common-Source Output Conductance		5		5			
C_{iss}	Common-Source Input Capacitance		3		3	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.5		1.5			
g_{fs}	Common-Source Forward Transconductance	50	150	50	150	μmho	V_{DG} = 10 V, I_D = 30 μA	f = 1 kHz
g_{os}	Common-Source Output Conductance		1		1			
$\overline{e_n}$	Equivalent Short Circuit Input Noise Voltage		0.2		0.1	$\frac{\mu V}{\sqrt{Hz}}$	V_{DS} = 10 V, V_{GS} = 0	
NF	Spot Noise Figure		3		1	dB		f = 100 Hz, R_G = 10 M

PARAMETER		2N5902-6 MIN	2N5902-6 MAX	2N5903-7 MIN	2N5903-7 MAX	2N5904-8 MIN	2N5904-8 MAX	2N5905-9 MIN	2N5905-9 MAX	UNIT	TEST CONDITIONS	
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		2.0		2.0		2.0		2.0	nA	V_{DG} = 10 V, I_D = 30 μA, T_A = 125°C	2N5902-5
			0.2		0.2		0.2		0.2			2N5906-9
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.95	1	0.95	1	0.95	1	0.95	1	—	V_{DS} = 10 V, V_{GS} = 0	
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.97	1	0.97	1	0.95	1	0.95	1		V_{DG} = 10 V, I_D = 30 μA	f = 1 kHz
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15	mV		
$\frac{\Delta\lvert V_{BS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Measured at end points T_A and T_B)		5		10		20		40	μV/°C		T_A = 25°C, T_B = 125°C
			5		10		20		40			T_A = −55°C, T_B = 25°C
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		0.2		0.2		0.2		0.2	μmho		f = 1 kHz

INTERSIL

2N5911 2N5912
Dual Monolithic Matched N-Channel JFETs (PAIR)

FEATURES

- Tracking < 20 μV/°C
- g_{fs} < 5000 μmho, 0 –100 MHz
- Matched V_{GS}, $\Delta V_{GS}/\Delta T$, I_G, g_{fs},

GENERAL DESCRIPTION

Matched FET pairs for wideband differential amplifiers.

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Gate-Drain or Gate-Source Voltage	-25V
Gate Current	50 mA
Device Dissipation (Each Side),	367 mW
Linear Derating	3 mW/°C
Total Device Dissipation,	500 mW
Linear Derating	4 mW/°C
Storage Temperature Range	-65°C to +200°C

ORDERING INFORMATION

TO99	WAFER	CHIP
2N5911	2N5911/W	2N5911/D
2N5912	2N5912/W	2N5912/D

PACKAGE DIMENSIONS

PIN	1	2	3	4	5	6	7	8
OUT	S_1	D_1	G_1	CASE	S_2	D_2	G_2	NO

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		–100	pA	V_{GS} = –15 V, V_{DS} = 0	
			–250	nA		150°C
BV_{GSS}	Gate Reverse Breakdown Voltage	–25		V	I_G = –1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	–1	–5	V	V_{DS} = 10 V, I_D = 1 nA	
V_{GS}	Gate-Source Voltage	–0.3	–4	V	V_{DG} = 10 V, I_D = 5 mA	
I_G	Gate Operating Current		–100	pA		
			–100	nA		125°C
I_{DSS}	Saturation Drain Current (Pulsewidth 300 μs, duty cycle ≤ 3%)	7	40	mA	V_{DS} = 10 V, V_{GS} = 0 V	
g_{fs}	Common-Source Forward Transconductance	5000	10,000	μmho	V_{DG} = 10 V, I_D = 5 mA	f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	5000	10,000	μmho		f = 100 MHz
g_{os}	Common-Source Output Conductance		100	μmho		f = 1 kHz
g_{oss}	Common-Source Output Conductance		150	μmho		f = 100 MHz
C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2	pF		
$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		20	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
NF	Spot Noise Figure		1	dB		f = 10 kHz, R_G = 100KΩ

	PARAMETER	2N5911 MIN	2N5911 MAX	2N5912 MIN	2N5912 MAX	UNIT	TEST CONDITIONS	
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		20		20	nA	V_{DG} = 10 V, I_D = 5 mA	125°C
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.95	1	0.95	1		V_{DS} = 10 V, V_{GS} = 0 (Pulsewidth 300 μs, duty cycle ≤ 3%)	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		10		15	mV	V_{DG} = 10 V, I_D = 5 mA	
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Measured at end points, T_A and T_B)		20		40	μV/°C		T_A = 25°C, T_B = 125°C
			20		40	μV/°C		T_A = –55°C, T_B = 25°C
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.95	1	0.95	1			f = 1 kHz

INTERSIL

2N6483, 2N6484, 2N6485
Low Noise Dual Monolithic Matched N-Channel JFETS

FEATURES

- Ultra Low Noise
  $\bar{e}_n < 10\ nV/\sqrt{Hz}$ at 10 Hz
- High CMRR > 100 dB
- Low Offset
  $\Delta\ |V_{GS1} - V_{GS2}| < 5\ mV$
- Tight Tracking
  $\Delta\ |V_{GS1} - V_{GS2}|/\Delta T < 5\ \mu V/°C$

GENERAL DESCRIPTION

These N-Channel Junction FETs are characterized for ultra low noise applications requiring tightly controlled and specified noise parameters at 10 Hz and 1000 Hz. Tight matching specifications make these devices ideal as the input stage for low frequency differential, instrumentation amplifiers.

ABSOLUTE MAXIMUM RATINGS (Note 1)
(@ 25°C unless otherwise noted)

Maximum Temperatures	
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	+150°C
Lead Temperature (soldering, 10 sec. time limit)	+300°C
Maximum Power Dissipation	
Device Dissipation @ 85°C Free Air Temperature	
One Side	250 mW
Both Sides	500 mW
Linear Derating	
One Side	3.85 mW/°C
Both Sides	7.7 mW/°C
Maximum Voltages & Currents	
V_{GS} Gate to Source Voltage	-50 V
V_{GD} Gate to Drain Voltage	-50 V
$V_{G1\,G2}$ Gate to Gate Voltage	±50 V
I_G Gate Current	50 mA

PACKAGE DIMENSIONS

NOTE: FOR DIE STRUCTURE, REFER TO 2N5515 FAMILY.

5019

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise specified)

SYMBOL	CHARACTERISTICS	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{GSS}	Gate Reverse Current		200	pA	$V_{GS} = -30\ V,\ V_{DS} = 0,\ T_A = +25°C$
			200	nA	$V_{GS} = -30\ V,\ V_{DS} = 0,\ T_A = +150°C$
BV_{GSS}	Gate Source Breakdown Voltage	50		V	$I_G = 1\ \mu A,\ V_{DS} = 0$
V_p	Gate Source Pinch Off Voltage	0.7	4.0	V	$V_{DS} = 20\ V,\ I_D = 1\ nA$
I_{DSS}	Drain Current at Zero Gate Voltage	0.5	7.5	mA	$V_{DS} = 20\ V,\ V_{GS} = 0$ (Note 2)
g_{fs}	Common Source Forward Transconductance	1000	4000	μmho	$V_{DS} = 20\ V,\ V_{GS} = 0,\ f = 1\ KHz$ (Note 2)
g_{oss}	Common Source Output Conductance		10	μmho	$V_{DS} = 20\ V,\ V_{GS} = 0,\ f = 1\ KHz$
C_{iss}	Common Source Input Capacitance		20	pF	$V_{DS} = 20\ V,\ V_{GS} = 0,\ f = 1\ MHz$
C_{rss}	Common Source Reverse Transfer Capacitance		3.5	pF	$V_{DS} = 20\ V,\ V_{GS} = 0,\ f = 1\ MHz$
I_G	Gate Current		100	pA	$V_{GD} = 20\ V,\ I_D = 200\ \mu A,\ T_A = +25°C$
			100	nA	$V_{DG} = 20\ V,\ I_D = 200\ \mu A,\ T_A = +150°C$
V_{GS}	Gate Source Voltage	0.2	3.8	V	$V_{DG} = 20\ V,\ I_D = 200\ \mu A$
g_{fs}	Common Source Forward Transconductance	500	1500	μmho	$V_{DG} = 20\ V,\ I_D = 200\ \mu A,\ f = 1\ KHz$ (Note 2)
g_{os}	Common Source Output Conductance		1	μmho	$V_{DG} = 20\ V,\ I_D = 200\ \mu A$
$\bar{e}_n$	Equivalent Input Noise Voltage		10	$nV/\sqrt{Hz}$	$V_{DS} = 20\ V,\ I_D = 200\ \mu A,\ f = 10\ Hz$
			5	$nV/\sqrt{Hz}$	$V_{DS} = 20\ V,\ I_D = 200\ \mu A,\ f = 1\ KHz$

MATCHING CHARACTERISTICS (@ 25°C unless otherwise noted)

SYMBOL	CHARACTERISTIC	2N6483		2N6484		2N6485		UNIT	CONDITIONS
		MIN.	MAX.	MIN.	MAX.	MIN.	MAX.		
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage	0.95	1	0.95	1	0.95	1	–	V_{DS} = 20 V, V_{GS} = 0 (Note 2)
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current		10		10		10	nA	V_{DG} = 20 V, I_D = 200 μA T_A = +125°C
$\frac{g_{fs1}}{g_{gs2}}$	Transconductance Ratio	0.97	1	0.97	1	0.95	1	–	V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz (Note 2)
$\lvert g_{os1} - g_{os2} \rvert$	Differential Output Conductance		0.1		0.1		0.1	μmho	V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		5		10		15	mV	V_{DG} = 20 V, I_D = 200 μA
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift		5		10		25	μV/°C	V_{DG} = 20 V, I_D = 200 μA T_A = +25°C to +125°C
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift		5		10		25	μV/°C	V_{DG} = 20 V, I_D = 200 μA T_A = -55°C to + 25°C
CMRR	Common Mode Rejection Ratio	100		100		90		dB	V_{DD} = 10 to 20 V, I_D = 200 μA (Note 3)

NOTES: 1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
2. Pulse duration of 2 ms used during test.
3. CMRR = $20\text{Log}_{10}\Delta V_{DD}/\Delta\lvert V_{GS1} - V_{GS2}\rvert$, ($\Delta V_{DD}$ = 10 V), not included in JEDEC registration

TYPICAL CHARACTERISTICS OF 2N6483, 2N6484, 2N6485

$\bar{e}_n$ vs. FREQUENCY

$\bar{e}_n$ vs. FREQUENCY

GATE CURRENT vs. V_{DG}

TYPICAL CAPACITANCE vs. V_{DS}

INTERSIL

IMF5911/IMF5912

Dielectrically Isolated Dual Monolithic Matched N-Channel JFETS (Pair)

FEATURES

- **Tracking < 25 μV/°C**
- **g_{fs} > 5000 μmho, 0-100 MHz**
- **Matched V_{GS}, $\Delta V_{GS}/\Delta T$, I_G, g_{fs}**
- **High Adjacent Signal Isolation**

GENERAL DESCRIPTION

The IMF 5911, 5912 are dielectrically isolated matched n-channel JFETS ideally suited for wideband differential amplifiers. The dielectric isolation virtually eliminates parasitic leakage currents and capacitance between the matched pair which are present in conventional junction isolated pairs. The electrical characteristics of the 5911, 5912 are the same as the popular 2N5911, 5912 type JFET's, with the exception of superior inter-device leakages and capacitance. The thermal matching of these devices is maintained by the common polysilicon substrate.

DIE DIMENSIONS

NOTE: Dimensions in parenthesis are metric.

PACKAGE DIMENSIONS

TO-99

NOTE: Dimensions in parenthesis are metric.

PIN	1	2	3	4	5	6	7	8
OUT	S_1	D_1	G_1	CASE	S_2	D_2	G_2	NO

ORDERING INFORMATION

TO99	CHIP
IMF5911	IMF5911/D
IMF5912	IMF5912/D

ABSOLUTE MAXIMUM RATINGS @ 25°C (unless otherwise noted)

Gate-Drain or Gate-Source Voltage ..... −25V
Gate Current ..... 50 mA
Device Dissipation (Each Side) ..... 367 mW
Linear Derating ..... 3 mW/°C
Total Device Dissipation ..... 500 mW
Linear Derating ..... 4 mW/°C
Storage Temperature Range ..... −65°C to +200°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

	PARAMETER	MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−100	pA	V_{GS} = −15 V, V_{DS} = 0	
			−250	nA		150°C
BV_{GSS}	Gate Reverse Breakdown Voltage	−25		V	I_G = −1 μA, V_{DS} = 0	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−1	−5		V_{DS} = 10 V, I_D = 1 nA	
V_{GS}	Gate-Source Voltage	−0.3	−4		V_{DG} = 10 V, I_D = 5 mA	
I_G	Gate Operating Current		−100	pA		
			−100	nA		125°C
I_{DSS}	Saturation Drain Current (Pulsewidth 300 μs, duty cycle ≤ 3%)	7	40	mA	V_{DS} = 10 V, V_{GS} = 0V	
g_{fs}	Common-Source Forward Transconductance	5000	10,000	μmho	V_{DG} = 10 V, I_D = 5mA	f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	5000	10,000			f = 100 MHz
g_{os}	Common-Source Output Conductance		100			f = 1 kHz
g_{oss}	Common-Source Output Conductance		150			f = 100 MHz
C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		10	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
NF	Spot Noise Figure		1	dB		f = 10 kHz, R_G = 100KΩ
I_{G1G2}	Gate to Gate Leakage		2	pA	V_{DG} = 50 V	

	PARAMETER	IMF5911 MIN	IMF5911 MAX	IMF5912 MIN	IMF5912 MAX	UNIT	TEST CONDITIONS	
$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		20		20	nA	V_{DG} = 10 V, I_D = 5mA	125°C
$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio	0.95	1	0.95	1		V_{DS} = 10 V, V_{GS} = 0 (Pulsewidth 300 μs, duty cycle ≤ 3%)	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		25		50	mV	V_{DG} = 10 V, I_D = 5 mA	
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Measured at end points, T_A and T_B)		25		50	μV/°C		T_A = 25°C, T_B = 125°C
			25		50			T_A = −55°C, T_B = 25°C
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.95	1	0.95	1			f = 1 kHz

INTERSIL

IMF6485

Low Noise Dual Monolithic Matched N-Channel JFETS

FEATURES

- $\bar{e}_n < 10\,nV/\sqrt{Hz}$ at 10 Hz
- CMRR > 90 dB
- $\Delta |V_{GS1} - V_{GS2}| < 25$ mV
- $\Delta |V_{GS1} - V_{GS2}| < 40\ \mu V/^\circ C$

ABSOLUTE MAXIMUM RATINGS (Note 1)

(@ 25°C unless otherwise noted)

Maximum Temperatures	
Storage Temperature	-65°C to +150°C
Operating Junction Temperature	+150°C
Lead Temperature (soldering, 10 sec. time limit)	+300°C
Maximum Power Dissipation	
Device Dissipation @ 85°C Free Air Temperature	
One Side	250 mW
Both Sides	500 mW
Linear Derating	
One Side	3.85 mW/°C
Both Sides	7.7 mW/°C
Maximum Voltages & Currents	
V_{GS} Gate to Source Voltage	-50 V
V_{GD} Gate to Drain Voltage	-50 V
$V_{G1\,G2}$ Gate to Gate Voltage	±50 V
I_G Gate Current	50 mA

GENERAL DESCRIPTION

This N-Channel Junction FET is characterized for ultra low noise applications requiring tightly controlled and specified noise parameters at 10 Hz and 1000 Hz. Tight matching specifications make this device ideal as the input stage for low frequency differential instrumentation amplifiers.

PACKAGE DIMENSIONS

NOTE: FOR DIE STRUCTURE, REFER TO 2N5515 FAMILY.

6019

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise specified)

SYMBOL	CHARACTERISTICS	MIN.	MAX.	UNIT	TEST CONDITIONS
I_{GSS}	Gate Reverse Current		-200	pA	V_{GS} = -30 V, V_{DS} = 0, T_A = +25°C
			-200	nA	V_{GS} = -30 V, V_{DS} = 0, T_A = +150°C
BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 μA, V_{DS} = 0
V_p	Gate-Source Pinch-Off Voltage	-0.7	-4.0	V	V_{DS} = 20 V, I_D = 1 nA
I_{DSS}	Drain Current at Zero Gate Voltage	0.5	7.5	mA	V_{DS} = 20 V, V_{GS} = 0 (Note 2)
g_{fs}	Common-Source Forward Transconductance	1000	4000	μmho	V_{DS} = 20 V, V_{GS} = 0, f = 1 KHz (Note 2)
g_{oss}	Common-Source Output Conductance		10	μmho	V_{DS} = 20 V, V_{GS} = 0, f = 1 KHz
C_{iss}	Common-Source Input Capacitance		20	pF	V_{DS} = 20 V, V_{GS} = 0, f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		3.5	pF	V_{DS} = 20 V, V_{GS} = 0, f = 1 MHz
I_G	Gate Current		-100	pA	V_{GD} = 20 V, I_D = 200 μA, T_A = +25°C
			-100	nA	V_{DG} = 20 V, I_D = 200 μA, T_A = +150°C
V_{GS}	Gate-Source Voltage	-0.2	-3.8	V	V_{DG} = 20 V, I_D = 200 μA
g_{fs}	Common-Source Forward Transconductance	500	1500	μmho	V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz (Note 2)
g_{os}	Common-Source Output Conductance		1	μmho	V_{DG} = 20 V, I_D = 200 μA
$\bar{e}_n$	Equivalent Input Noise Voltage		15	$nV/\sqrt{Hz}$	V_{DS} = 20 V, I_D = 200 μA, f = 10 Hz
			10	$nV/\sqrt{Hz}$	V_{DS} = 20 V, I_D = 200 μA, f = 1 KHz

MATCHING CHARACTERISTICS (@ 25° C unless otherwise noted)

SYMBOL	CHARACTERISTIC	MIN.	MAX.	UNIT	CONDITIONS
$\frac{I_{DSS1}}{I_{CSS2}}$	Drain Current Ration at Zero Gate Voltage	0.95	1	–	V_{DS} = 20 V, V_{GS} = 0 (Note 2)
$\lvert I_{G1} - I_{G2} \rvert$	Differential Gate Current		10	nA	V_{DG} = 20 V, I_D = 200 μA T_A = +125° C
$\frac{g_{fs1}}{g_{gs2}}$	Transconductance Ratio	0.95	1	–	V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz (Note 2)
$\lvert g_{os1} - g_{os2} \rvert$	Differential Output Conductance		0.1	μmho	V_{DG} = 20 V, I_D = 200 μA, f = 1 KHz
$\lvert V_{GS1} - V_{GS2} \rvert$	Differential Gate-Source Voltage		25	mV	V_{DG} = 20 V, I_D = 200 μA
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift		40	μV/° C	V_{CG} = 20 V, I_D = 200 μA T_A = +25° C to +125° C
$\frac{\Delta \lvert V_{GS1} - V_{GS2} \rvert}{\Delta T}$	Gate-Source Voltage Differential Drift		40	μV/° C	V_{DG} = 20 V, I_D = 200 μA T_A = -55° C to +25° C
CMRR	Common Mode Rejection Ratio	90		dB	V_{DD} = 10 to 20 V, I_D = 200 μA (Note 3)

NOTES: 1. These ratings are limiting values above which the serviceability of any individual semiconductor device may be impaired.
2. Pulse duration of 2 ms used during test.
3. CMRR = $20\text{Log}_{10}\Delta V_{DD}/\Delta\lvert V_{GS1} - V_{GS2}\rvert$, ($\Delta V_{DD}$ = 10 V)

TYPICAL CHARACTERISTICS

$\bar{e}_n$ vs. FREQUENCY

$\bar{e}_n$ vs. FREQUENCY

GATE CURRENT vs. V_{DG}

TYPICAL CAPACITANCE vs. V_{DS}

INTERSIL

IT500, IT501, IT502, IT503

Dual Monolithic N-Channel JFET

FEATURES

- $C_{MRR} > 120$ dB
- $I_G < 5$ pA @ $50V_{DG}$
- Low Miller Capacitance (C_{rss})
- Low $g_{os} < .025$ μmhos

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ABSOLUTE MAXIMUM RATINGS

(@ 25°C unless otherwise noted)

Maximum Temperatures

Storage Temperature . . . . . –65°C to +150°C
Operating Temperature. . . . . +150°C
Lead Temperature (soldering, 10 sec time limit). +300°C

Maximum Power Dissipation

Device Dissipation @ 85°C Free Air Temperature

One Side . . . . . 250 mW
Both Sides . . . . . 500 mW

Linear Derating

One Side . . . . . 3.85 mW/°C
Both Sides . . . . . 7.7 mW/°C

Maximum Voltages & Currents

V_{DS} Drain to Source Voltage 60V
V_{GS} Gate to Source Voltage 60V
V_{GD} Gate to Drain Voltage. 60V
$V_{G1\ G2}$ Gate to Gate Voltage 60V
I_G Gate Current . . . . . 50 mA

NOTE: Due to the non-symetrical structure of these devices, the drain and source ARE NOT interchangeable.

GENERAL DESCRIPTION

A low noise, low leakage FET that employs a cascode structure to accomplish very low Ig at high voltage levels, while giving high transconductance and very high common mode rejection ratio.

PACKAGE DIMENSIONS

TO52

BONDING PAD DETAIL

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise specified)

	Symbol	Characteristics	Min	Max	Unit	Test Conditions	
STATIC	I_{GSS}	Gate Reverse Current		-100	pA	V_{GS} = -20V, V_{DS} = 0	
				-5	nA		+125°C
	BV_{GSS}	Gate-Source Breakdown Voltage	-50		V	I_G = -1 μA, V_{DS} = 0	
	$V_{GS\ (off)}$	Gate-Source Cutoff Voltage	-0.7	-4		V_{DS} = 20V, I_D = 1 nA	
	V_{GS}	Gate-Source Voltage	-0.2	-3.8			
	I_G	Gate Operating Current		-5	pA	V_{DG} = 50V, I_D = 200 μA	
				-5	nA		125°C
	I_{DSS}	Saturation Drain Current (Note 1)	0.7	7	mA	V_{DS} = 20V, V_{GS} = 0	
DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	4000	μmho	V_{DS} = 20V, V_{GS} = 0	f = 1 kHz
	g_{fs}	Common-Source Forward Transconductance (Note 1)	700	1600		V_{DG} = 20V, I_D = 200 μA	
	g_{os}	Common-Source Output Conductance		1		V_{DS} = 20V*, V_{GS} = 0	
	g_{os}	Common-Source Output Conductance		0.025		V_{DS} = 20V, I_D = 200 μA	
	C_{g1g2}	Gate to Gate Capacitance		3.5	pF	V_{g1} = V_{g2} = 10V	f = 1 MHz
	C_{iss}	Common-Source Input Capacitance		7	pF	V_{DS} = 20V, V_{GS} = 0	
	C_{rss}	Common-Source Reverse Transfer Capacitance (Note 3)		0.5			
	NF	Spot Noise Figure		0.5	dB		f = 100 Hz, R_G = 10 MΩ
	$\bar{e}_n$	Equivalent Input Noise Voltage		0.035 0.010	$\frac{\mu V}{\sqrt{Hz}}$		f = 10 Hz f = 1 kHz

	Symbol	Characteristics	IT500 Min	IT500 Max	IT501 Min	IT501 Max	IT502 Min	IT502 Max	IT503 Min	IT503 Max	Unit	Test Conditions	
MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current		5		5		5		5	nA	V_{DG} = 20V, I_D = 200 μA	+125°C
	$\frac{I_{DSS1}}{I_{DSS2}}$	Saturation Drain Current Ratio (Note 1)	0.95	1	0.95	1	0.95	1	0.95	1	—	V_{DS} = 20V, V_{GS} = 0V	
	$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio (Note 1)	0.97	1	0.97	1	0.95	1	0.95	1	—	V_{DG} = 20V I_D = 200 μA	f = 1 kHz
	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		5		10		15	mV		
	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Differential Voltage Change with Temp. (Note 2)		5		10		20		40	μV/°C		T_A = 25°C T_B = 125°C
				5		10		20		40			T_A = -55°C T_B = 25°C
	C_{MRR}**	Common Mode Rejection Ratio	120		120		120		120		dB	ΔV_{DD} = 10V, I_D = 200 μA	

* JEDEC registered data

** $C_{MRR} = 20 \log_{10} \Delta V_{DD} / \Delta [V_{gs1} - V_{gs2}]$, ΔV_{DD} = 10/ - 20V

NOTES: 1. Pulse test required, pulsewidth = 300 μs, duty cycle ≤3%. 2. Measured at end points, T_A and T_B.
3. With case guarded C_{RSS} is typically <.15 pf

TYPICAL PERFORMANCE CURVES

GATE LEAKAGE

OUTPUT CHARACTERISTICS

TYPICAL CAPACITANCE VS. GATE-SOURCE VOLTAGE

INTERSIL

SU2365/A SU2366/A SU2367/A SU2368/A SU2369/A

Dual Monolithic Matched N-Channel JFETS (Pair)

FEATURES

- High CMRR
- Low Input Current
- Low Leakage
- Low Noise
- Offset Differential Independent of Operating Current
- Low Offset Differential
- Low Offset Differential With Change in Temp.

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +150°C
Operating Junction Temperature	+150°C
Lead Temperature (Soldering, 10 sec. time limit)	+300°C

Maximum Power Dissipation

Device Dissipation @ 85°C Free Air Temperature	
One Side	250 mW
Both Sides	500 mW
Linear Derating	
One Side	2.56 mW/°C
Both Sides	4.3 mW/°C

Maximum Voltages & Currents

V_{GS} Gate to Source Voltage	−30 V
V_{GD} Gate to Drain Voltage	−30 V
I_G Gate Current	50 mA

PACKAGE DIMENSIONS

TO-71

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		SU2365/A		SU2366/A		SU2367/A		SU2368/A		SU2369/A		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
$V_{(BR)GSS}$	V_{DS} = 0, I_G = −1.0 μA	−30		−30		−30		−30		−30		V
$V_{GS(OFF)}$	V_{DS} = 15 V, I_D = 1.0 nA		−3.5		−3.5		−3.5		−3.5		−3.5	V
V_{GS}	V_{DS} = 15 V, I_D = 200 μA		−2.5		−2.5		−2.5		−2.5		−2.5	V
I_{GSS}	V_{DS} = 0, V_{GS} = −20 V		−50		−50		−50		−50		−50	pA
I_G	V_{DS} = 15 V, I_D = 200 μA, T_A = 25°C		−20		−20		−20		−20		−20	pA
	V_{DS} = 15 V, I_D = 200 μA, T_A = 125°C		−15		−15		−15		−15		−15	nA
I_{DSS}	V_{DS} = 10 V, V_{GS} = 0	0.5	10	0.5	10	0.5	10	0.5	10	0.5	10	mA
g_{fs}	V_{DG} = 15 V, I_D = 200 μA, f = 1.0 KHz	1000	2000	1000	2000	1000	2000	1000	2000	1000	2000	μmhos
g_{fs}	V_{DS} = 10 V, V_{GS} = 0, f = 1.0 KHz	1500		1500		1500		1500		1500		μmhos
g_{os}	V_{DG} = 15 V, I_D = 200 μA		2.0		2.0		2.0		2.0		2.0	μmhos
C_{iss}	V_{DG} = 15 V, I_D = 200 μA, f = 0.14 MHz		16		16		16		16		16	pF
C_{rss}	V_{DG} = 15 V, I_D = 200 μA, f = 0.14 MHz		4.0		4.0		4.0		4.0		4.0	pF
$\bar{e}_n$	V_{DS} = 15 V, V_{GS} = 0, f = 1.0 KHz*		15		15		15		15		15	$nV/\sqrt{Hz}$
ΔV_{GS}	ΔV_{DG} = 10-20 V, I_D = 200 μA		0.3		0.3		0.4		0.5		1.0	mV
CMRR	ΔV_{DG} = 10-20 V, I_D = 200 μA		90		90		88		86		80	dB
$\lvert I_{G1}-I_{G2}\rvert$	V_{DG} = 15 V, I_D = 200 μA, T_A = 100°C		0.5		0.5		0.5		0.5		5.0	nA
$\frac{g_{fs1}}{g_{fs2}}$	V_{DG} = 15 V, I_D = 200 μA, f = 1.0 KHz	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	0.95	1.0	
$\lvert V_{GS1}-V_{GS2}\rvert$	V_{DG} = 10 V, I_D = 200 μA		5.0		10		10		15		20	mV
$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T_A}$	V_{DG} = 10 V, I_D = 200 μA, T_A = 0°C to 100°C		10		10		25		25		40	μV/°C
$V_{(BR)G1G2}$	V_{DS} = 0, V_{GS} = 0, I_D = ±1 μA	±30		±30		±30		±30		±30		V

*Figures for A versions only. Other $\bar{e}_n$ = 50 $nV/\sqrt{Hz}$.

INTERSIL

U231, U232, U233, U234, U235

Monolithic Dual N-Channel

DESIGNED FOR USE IN

- Differential Amplifiers
- Low and Maximum Frequency Amplifiers

FEATURES

- Good Matching Characteristics

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage ..... −50V
Gate Current ..... 50 mA
Total Device Dissipation at 25°C
(Derate 1.7 mW/°C to 200°C) ..... 300 mW
Storage Temperature Range ..... −65 to +200°C
Lead Temperature
(1/16" from case for 10 seconds) ..... 300°C

PACKAGE DIMENSIONS

TO-71

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted.

		Characteristic		Min	Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		−100	pA	V_{GS} = −30V, V_{DS} = 0	
2					−500	nA		150°C
3		BV_{GSS}	Gate-Source Breakdown Voltage	−50		V	I_G = 1μA, V_{DS} = 0	
4		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.5	−4.5		V_{DS} = 20V, I_D = 1 nA	
5		V_{GS}	Gate-Source Voltage	−0.3	−4.0			
6		I_G	Gate Operating Current		−50	pA	V_{DG} = 20V, I_D = 200μA	
					−250	nA		125°C
7		I_{DSS}	Saturation Drain Current (Note 1)	0.5	5.0	mA	V_{DS} = 20V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 1)	1000	3000	μmho	V_{DS} = 20V, V_{GS} = 0	f = 1 kHz
				1000				f = 100 MHz
9		g_{fs}	Common-Source Forward Transconductance (Note 1)	600	1600		V_{DG} = 20V, I_D = 200μA	f = 1 kHz
10		g_{os}	Common-Source Output Capacitance		35		V_{DS} = 20V, V_{GS} = 0	
11		g_{os}	Common-Source Output Conductance		10		V_{DG} = 20V, I_D = 200μA	
12		C_{iss}	Common-Source Input Capacitance		.6	pF	V_{DS} = 20V, V_{GS} = 0	f = 1 MHz
13		C_{rss}	Common-Source Reverse Transfer Capacitance		2			
14		$\bar{e}_n$	Equivalent Short Circuit Input Noise Voltage		80	$\frac{nV}{\sqrt{Hz}}$		f = 100 Hz

		Characteristic		U231 Max	U232 Max	U233 Max	U234 Max	U235 Max	Unit	Test Conditions	
15	MATCHING	$\lvert I_{G1}-I_{G2}\rvert$	Differential Gate Current	10	10	10	10	10	nA	V_{DG} = 20V, I_D = 200μA	125°C
16		$\frac{(I_{DSS1}-I_{DSS2})}{I_{DSS1}}$	Saturation Drain Current Match (Note 1)	5	5	5	10	15	%	V_{DS} = 20V, V_{GS} = 0	
17		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage	5	10	15	20	25	mV	V_{DG} = 20V, I_D = 200μA	
18		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 2)	10	25	50	75	100	μV/°C		T_A = 25°C T_B = 125°C
19				10	25	50	75	100			T_A = −55°C T_B = 25°C
20		$\frac{(g_{fs1}-g_{fs2})}{g_{fs1}}$	Transconductance Match (Note 1)	3	5	5	10	15	%		f = 1 kHz
21		$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance	5	5	5	5	5	μmho		

NOTES:
1. Pulse test required, pulsewidth = 300 μs, duty cycle ≤ 3%.
2. Measured at end points, T_A and T_B.

INTERSIL

U257

Dual Monolithic Matched N-Channel JFETS (PAIR)

GENERAL DESCRIPTION

Matched FET pairs for wideband differential amplifiers.

FEATURES

- $g_{fs} > 5000\ \mu mho$ from dc to 100 MHz
- Matched V_{GS}, g_{fs} and g_{os}

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Gate-Drain or Gate-Source Voltage	−25 V
Gate Current	50 mA
Device Dissipation (Each Side), $T_A = 85°C$ (Derate 3.85 mW/°C)	250 mW
Total Device Dissipation, $T_A = 85°C$ (Derate 7.7 mW/°C)	500 mW
Storage Temperature Range	−65°C to +150°C

ORDERING INFORMATION

TO99	WAFER	CHIP
U257	U257/W	U257/D

PACKAGE DIMENSIONS

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
I_{GSS}	Gate Reverse Current		−100	pA	$V_{GS} = 15\ V$, $V_{DS} = 0$	
			−250	nA		150°C
BV_{GSS}	Gate-Source Breakdown Voltage	−25		V	$I_G = -1\ \mu A$, $V_{DS} = 0$	
$V_{GS(off)}$	Gate-Source Cutoff Voltage	−1	−5		$V_{DS} = 10\ V$, $I_D = 1\ nA$	
I_{DSS}	Saturation Drain Current (Note 1)	5	40	mA	$V_{DS} = 10\ V$, $V_{GS} = 0$	
g_{fs}	Common-Source Forward Transconductance	5000	10,000	μmho	$V_{DS} = 10\ V$, $I_D = 5\ mA$	f = 1 kHz
g_{fs}	Common-Source Forward Transconductance	5000	10,000		$V_{DG} = 10\ V$, $I_D = 5\ mA$	f = 100 MHz
g_{os}	Common-Source Output Conductance		150		$V_{DS} = 10\ V$, $I_D = 5\ mA$	f = 1 kHz
g_{oss}	Common-Source Output Conductance		150		$V_{DG} = 10\ V$, $I_D = 5\ mA$	f = 100 MHz
C_{iss}	Common-Source Input Capacitance		5	pF		f = 1 MHz
C_{rss}	Common-Source Reverse Transfer Capacitance		1.2			
$\overline{e_n}$	Equivalent Input Noise Voltage		30	$\frac{nV}{\sqrt{Hz}}$		f = 10 kHz
$\frac{I_{DSS1}}{I_{DSS2}}$	Drain Current Ratio at Zero Gate Voltage (Note 1)	0.85	1		$V_{DS} = 10\ V$, $V_{GS} = 0$	
$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		100	mV	$V_{DG} = 10\ V$, $I_D = 5\ mA$	f = 1 kHz
$\frac{g_{fs1}}{g_{fs2}}$	Transconductance Ratio	0.85	1			
$\lvert g_{os1}-g_{os2}\rvert$	Differential Output Conductance		20	μmho		

NOTE:
1. Pulse test required, pulse width = 300 μs, duty cycle ≤ 30%.

INTERSIL

U401, U402, U403, U404, U405, U406

Monolithic Dual N-Channel

FEATURES

- **Minimum System Error and Calibration — 5mV Offset Maximum (U401), 95dB Minimum CMRR (U401-04)**
- **Low Drift with Temperature — 10μV/°C Maximum (401, 02)**
- **Operates from Low Power Supply Voltages — $V_{GS(off)}$ <2.5V**
- **Simplifies Amplifier Design — Output Impedance >500KΩ**

DESIGNED FOR USE AS

- **Low Noise FET Input Amplifiers**
- **Impedance Converters**
- **Precision Instrumentation Amplifiers**
- **Comparators**

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-Drain or Gate-Source Voltage 50V
Forward Gate Current .....10 mA
Device Dissipation (each side)
@ T_A = 85°C derate 2.6 mW/°C ..... 300 mW
Total Device Dissipation
@ T_A = 85°C (derate 5 mW/°C) ..... 500 mW
Storage Temperature Range .....–65 to 200°C

PACKAGE DIMENSIONS

TO-71

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25° unless otherwise noted.

		Characteristic		U401		U402		U403		U404		U405		U406		Unit	Test Conditions	
				Min	Max	Min	Max	Min	Max	Min	Max	Min	Max	Min	Max			
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	-50		-50		-50		-50		-50		-50		V	V_{DS} = o, I_G = -1μA	
2		I_{GSS}	Gate Reverse Current (Note 1)		-25		-25		-25		-25		-25		-25	pA	V_{DS} = 0, V_{GS} = -30V	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	-5	-2.5	-.5	-2.5	-.5	-2.5	-.5	-2.5	-.5	-2.5	-.5	-2.5	V	V_{DS} = 15V, I_D = 1 nA	
4		$V_{GS(on)}$	Gate-Source Voltage (on)		-2.3		-2.3		-2.3		-2.3		-2.3		-2.3		V_{DG} = 15V, I_D = 200μA	
5		I_{DSS}	Saturation Drain Current (Note 2)	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	0.5	10.0	mA	V_{DS} = 10V, V_{GS} = 0	
6					-15		-15		-15		-15		-15		-15	pA	V_{DG} = 15V,	
7		I_G	Gate Current (Note 1)		-10		-10		-10		-10		-10		-10	nA	I_D = 200μA	T_A = 125°C
8		BV_{G1-G2}	Gate-Gate Breakdown Voltage	±50		±50		±50		±50		±50		±50		V	V_{DS} = 0, V_{GS} = 0, I_G = ±1μA	
9	DYNAMIC	g_{fs}	Common-Source Forward Transconductance (Note 2)	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	2000	7000	μmho	V_{DS} = 10V, V_{GS} = 0	f = 1 kHz
10		g_{os}	Common-Source Output Conductance		20		20		20		20		20		20			
11		g_{fs}	Common-Source Forward Transconductance	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600	1000	1600		V_{DG} = 15V, I_D = 200μA	f = 1 kHz
12		g_{os}	Common-Source Output Conductance		2.0		2.0		2.0		2.0		2.0		2.0			
13		C_{iss}	Common-Source Input Capacitance		8.0		8.0		8.0		8.0		8.0		8.0	pF		f = 1 MHz
14		C_{rss}	Common-Source Reverse Transfer Capacitance		3.0		3.0		3.0		3.0		3.0		3.0			
15		e_N	Equivalent Short-Circuit Input Noise Voltage		20		20		20		20		20		20	$\frac{nV}{\sqrt{Hz}}$	V_{DS} = 15V, V_{GS} = 0	f = 10 Hz
16	MATCHING	CMRR	Common-Mode Rejection Ratio (Note 3)	95		95		95		95		90				dB	V_{DG} = 10 to 20V, I_D = 200μA	
17		$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage		5		10		10		15		20		40	mV	V_{DG} = 10V, I_D = 200μA	
18		$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Gate-Source Voltage Differential Drift (Note 4)		10		10		25		25		40		80	μV/°C	V_{DG} = 10V, I_D = 200μA	T_A = -55°C, T_B = +25°C, I_D = 200μA T_C = +125°C

NOTES:
1. Approximately doubles for every 10°C increase in T_A. 2. Pulse test duration = 300μs, duty cycle ≤ 3%. 3. CMRR = $20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right]$ ΔV_{DD} = 10V. 4. Measured at end points, T_A, T_B and T_C.

INTERSIL

Monolithic Dual Matched N-Channel JFET U421, U422, U423, U424, U425, U426

DESIGNED FOR . . .

- Very High Input Impedance
  Differential Amplifiers
  Electrometers
- Impedance Converters

FEATURES

- High Input Impedance
  I_G = 0.1 pA Maximum (U421-3)
- High Gain g_{fs} = 140 μmho Minimum @ I_D = 30 μA (U421-3)
- Low Power Supply Operation
  $V_{GS(off)}$ = 2V Maximum (U421-3)
- Minimum System Error and Calibration
  10 mV Maximum Offset
  90 dB Minimum CMRR (U421, U424)

PACKAGE DIMENSIONS

TO-99

PIN	1	2	3	4	5	6	7	8
OUT	S_1	D_1	G_1	CASE	S_2	D_2	G_2	NO

ABSOLUTE MAXIMUM RATINGS (25°C)

Gate-to-Gate Voltage ..... ±40V
Gate-Drain or Gate-Source Voltage ..... −40V
Gate Current ..... 10 mA
Device Dissipation (Each Side), T_A = 25°C
(Derate 3.2 mW/°C to 150°C) ..... 400 mW
Total Device Dissipation, T_A = 25°C
(Derate 6.0 mW/°C to 150°C) ..... 750 mW
Storage Temperature Range ..... −65 to +150°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C unless otherwise noted

		Characteristic		U421-3 Min	U421-3 Typ	U421-3 Max	U424-6 Min	U424-6 Typ	U424-6 Max	Unit	Test Conditions	
1	STATIC	BV_{GSS}	Gate-Source Breakdown Voltage	−40	−60		−40	−60		V	I_G = −1μA, V_{DS} = 0	
2	STATIC	BV_{G1G2}	Gate-Gate Breakdown Voltage	±40			±40			V	I_G = −1μA, I_D = 0, I_S = 0	
3	STATIC	I_{GSS}	Gate Reverse Current (Note 1)			0.2			1.0	pA	T = +25°C; V_{GS} = −20V, V_{DS} = 0	
						0.5			1.0	nA	T = +125°C	
4	STATIC	I_G	Gate Operating Current (Note 1)			0.1			0.5	pA	T = +25°C; V_{DG} = 10V, I_D = 30μA	
						−100			−500		T = +125°C	
5	STATIC	$V_{GS(off)}$	Gate-Source Cutoff Voltage	−0.4		−2.0	−0.4		−3.0	V	V_{DS} = 10V, I_D = 1 nA	
6	STATIC	V_{GS}	Gate-Source Voltage			−1.8			−2.9	V	V_{DG} = 10V, I_D = 30μA	
7	STATIC	I_{DSS}	Saturation Drain Current	60		1000	60		1800	μA	V_{DS} = 10V, V_{GS} = 0	
8	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	300		800	300		1000	μ℧	V_{DS} = 10V, V_{GS} = 0	f = 1 kHz
9	DYNAMIC	g_{os}	Common-Source Output Conductance			3.0			5.0			
10	DYNAMIC	C_{iss}	Common-Source Input Capacitance			3.0			3.0	pF		f = 1 MHz
11	DYNAMIC	C_{rss}	Common-Source Reverse Transfer Capacitance			1.5			1.5			
12	DYNAMIC	g_{fs}	Common-Source Forward Transconductance	140		250	135		300	μ℧	V_{DG} = 10V, I_D = 30μA	f = 1 kHz
13	DYNAMIC	g_{os}	Common-Source Output Conductance			0.5			1.0			
14	DYNAMIC	e_n	Equivalent Short Circuit Input Noise Voltage		20	50		20	70	nV/√Hz		f = 10 Hz
					10			10	50			f = 1 kHz
15	DYNAMIC	NF	Noise Figure			1.0			1.0	dB	f = 10 Hz	R_G = 10M Ω

		Characteristic		U421,4 Min	U421,4 Typ	U421,4 Max	U422,5 Min	U422,5 Typ	U422,5 Max	U423,6 Min	U423,6 Typ	U423,6 Max	Unit	Test Conditions
16	MATCH	$\lvert V_{GS1}-V_{GS2}\rvert$	Differential Gate-Source Voltage			10			15			25	mV	V_{DG} = 10V, I_D = 30μA
17	MATCH	$\frac{\Delta\lvert V_{GS1}-V_{GS2}\rvert}{\Delta T}$	Differential Gate-Source Voltage Change With Temperature (Note 2)			10			25			40	μV/°C	V_{DG} = 10V, I_D = 30μA, T_A = −55°C, T_B = 25°C, T_C = 125°C
18	MATCH	CMRR	Common Mode Rejection Ratio (Note 3)	90	95		80	90		80	90		dB	I_D = 30μA, V_{DG} = 10 to 20V

NOTES: 1. Approximately doubles for every 10°C increase in T_A.
2. Measured at end points T_A, T_B and T_C.
3. $CMRR = 20\log_{10}\left[\frac{\Delta V_{DD}}{\Delta\lvert V_{GS1}-V_{GS2}\rvert}\right]$ ΔV_{DD} = 10V

INTERSIL

2N4351

N-Channel Enhancement

FEATURES

- Low On-Resistance – 50Ω
- Low Capacitance – 1.7 pF
- High Gain – 3,000 μmhos
- High Gate Breakdown Voltage – ±125 V
- Low Threshold Voltage – 3 V

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures

Operating Junction Temperature –55°C to +150°C

Maximum Power Dissipation

Total Dissipation at 25°C Ambient Temp 0.375 W

Linear Derating Factor at 25°C Ambient Temp. 3 mW/°C

Maximum Voltages and Current

V_{DSS} Drain to Source and Body Voltage 25 V

V_{GSS} Transient Gate to Source Voltage ±125 V

$I_{D(on)}$ Drain Current 100 mA

ORDERING INFORMATION

TO72	WAFER	CHIP
2N4351	2N4351/W	2N4351/D

PACKAGE DIMENSIONS

TO-72

1003

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Substrate connected to source.

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
OFF CHARACTERISTICS					
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	25		Vdc	I_D = 10 μA, V_{GS} = 0
I_{GSS}	Gate Leakage Current		10	pAdc	V_{GS} = ±30 Vdc, V_{DS} = 0
I_{DSS}	Zero-Gate-Voltage Drain Current		10	nAdc	V_{DS} = 10 V, V_{GS} = 0
ON CHARACTERISTICS					
$V_{GS(TH)}$	Gate-Source Threshold Voltage	1.0	5	Vdc	V_{DS} = 10 V, I_D = 10 μA
$I_{D(on)}$	"ON" Drain Current	3		mAdc	V_{GS} = 10 V, V_{DS} = 10 V
$V_{DS(on)}$	Drain-Source "ON" Voltage		1.0	Vdc	I_D = 2 mA, V_{GS} = 10 V
SMALL SIGNAL CHARACTERISTICS					
$r_{ds(on)}$	Drain-Source Resistance		300	ohms	V_{GS} = 10 V, I_D = 0, f = 1 kHz
$\|y_{fs}\|$	Forward Transfer Admittance	1000		μmho	V_{DS} = 10 V, I_D = 2 mA, f = 1 kHz
C_{rss}	Reverse Transfer Capacitance		1.3	pF	V_{DS} = 0, V_{GS} = 0, f = 140 kHz
C_{iss}	Input Capacitance		5.0	pF	V_{DS} = 10 V, V_{GS} = 0, f = 140 kHz
$C_{d(sub)}$	Drain-Substrate Capacitance		5.0	pF	$V_{D(SUB)}$ = 10 V, f = 140 kHz
SWITCHING CHARACTERISTICS					
t_{d1}	Turn-On Delay		45	ns	FIGURE 1 – SWITCHING CIRCUIT and WAVEFORMS
t_r	Rise Time		65	ns	
t_{d2}	Turn-Off Delay		60	ns	
t_f	Fall Time		100	ns	

INTERSIL

3N169 3N170 3N171

N-Channel Enhancement Mode MOS FET

FEATURES

- Low Switching Voltages – $V_{GS(th)} \leq 3.0$ Vdc
- Fast Switching Times – $t_r \leq 10$ ns
- Low Drain-Source Resistance $r_{ds(on)}$ = 200 Ohms (Max)
- Low Reverse Transfer Capacitance C_{rss} = 1.3 pF (Max)
- Manufactured Using the New Silicon Nitride Process Resulting in a Stable $V_{GS(th)}$ and Gate Oxide Breakdown Protection to Typical Transients of ±150 Volts Peak

HANDLING PRECAUTIONS

MOS field-effect transistors have extremely high input resistance. They can be damaged by the accumulation of excess static charge. Avoid possible damage to the devices while wiring, testing, or in actual operation, by following the procedures outlined below:

1. To avoid the build-up of static charge, the leads of the devices should remain shorted together with a metal ring except when being tested or used.
2. Avoid unnecessary handling. Pick up devices by the case instead of the leads.
3. Do not insert or remove devices from circuits with the power on because transient voltages may cause permanent damage to the devices.

GENERAL DESCRIPTION

Enhancement Mode (Type C) transistors designed for low-power switching applications.

MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

RATING	SYMBOL	VALUE	UNIT
Drain-Source Voltage	V_{DS}	25	Vdc
Drain-Gate Voltage	V_{DG}	±35	Vdc
Gate-Source Voltage	V_{GS}	±35	Vdc
Drain Current	I_D	30	mAdc
Power Dissipation @ T_A = 25°C	P_D	300	mW
Derate above 25°C		1.7	mW/°C
Power Dissipation @ T_C = 25°C	P_D	800	mW
Derate above 25°C		4.56	mW/°C
Operating Junction Temperature	T_J	175	°C
Storage Temperature Range	T_{stg}	−65 to +200	°C

TO-72

PACKAGE DIMENSIONS

1003

PIN	OUT
1	S
2	G
3	D
4	B-C

ORDERING INFORMATION

TO72	WAFER	CHIP
3N169	3N169/W	3N169/D
3N170	3N170/W	3N170/D
3N171	3N171/W	3N171/D

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted) Substrate connected to source.

PARAMETER		MIN	MAX	UNITS	TEST CONDITIONS
OFF CHARACTERISTICS					
$V_{(BR)DSS}$	Drain-Source Breakdown Voltage	25		Vdc	I_D = 10 μAdc, V_{GS} = 0
I_{GSS}	*Gate Leakage Current		10	pAdc	V_{GS} = −35 Vdc, V_{DS} = 0
			100		V_{GS} = −35 Vdc, V_{DS} = 0, T_A = 125°C
I_{DSS}	*Zero-Gate-Voltage Drain Current		10	nAdc	V_{DS} = 10 Vdc, V_{GS} = 0
			1.0	μAdc	V_{DS} = 10 Vdc, V_{GS} = 0, T_A = 125°C
***ON CHARACTERISTICS**					
$V_{GS(th)}$	Gate-Source Threshold Voltage	0.5	1.5	Vdc	V_{DS} = 10 Vdc, I_D = 10 μAdc 3N169
		1.0	2.0		3N170
		1.5	3.0		3N171
$I_{D(on)}$	"ON" Drain Current	10		mAdc	V_{GS} = 10 Vdc, V_{DS} = 10 Vdc
$V_{DS(on)}$	Drain-Source "ON" Voltage		2.0	Vdc	I_D = 10 mAdc, V_{GS} = 10 Vdc
SMALL SIGNAL CHARACTERISTICS					
$r_{ds(on)}$	*Drain-Source Resistance		200	Ohms	V_{GS} = 10 Vdc, I_D = 0, f = 1.0 kHz
$\|Y_{fs}\|$	Forward Transfer Admittance	1000		μmhos	V_{DS} = 10 Vdc, I_D = 2.0 mAdc, f = 1.0 kHz
C_{rss}	*Reverse Transfer Capacitance		1.3	pF	V_{DS} = 0, V_{GS} = 0, f = 1.0 MHz
C_{iss}	*Input Capacitance		5.0	pF	V_{DS} = 10 Vdc, V_{GS} = 0, f = 1.0 MHz
$C_{d(sub)}$	*Drain-Substrate Capacitance		5.0	pF	$V_{D(SUB)}$ = 10 Vdc, f = 1.0 MHz
***SWITCHING CHARACTERISTICS**					
$t_{d(on)}$	Turn-On Delay Time		3.0	ns	V_{DD} = 10 Vdc, $I_{D(on)}$ = 10 mAdc, $V_{GS(on)}$ = 10 Vdc, $V_{GS(off)}$ = 0, R_G = 50 Ohms
t_r	Rise Time		10	ns	
$t_{d(off)}$	Turn-Off Delay Time		3.0	ns	
t_f	Fall Time		15	ns	

*Indicates JEDEC Registered Data.

INTERSIL

IT1750

N-Channel Enhancement Mode MOS FET

FEATURES

- Low On-Resistance – 50Ω
- Low Capacitance – 1.7 pF
- High Gain – 3,000 μmhos
- High Gate Breakdown Voltage – ±125V
- Low Threshold Voltage – 3 V

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Operating Junction Temperature –55°C to +150°C

Maximum Power Dissipation

Total Dissipation at 25°C Ambient Temp. 0.375 W

Linear Derating Factor at 25°C Ambient Temp. 3 mW/°C

Maximum Voltages and Current

V_{DSS} Drain to Source and Body Voltage 25 V

V_{GSS} Transient Gate to Source Voltage ±125 V

$I_{D(on)}$ Drain Current 100 mA

ORDERING INFORMATION

TO72	WAFER	CHIP
IT1750	IT1750/W	IT1750/D

PACKAGE DIMENSIONS

TO-72

1003

ELECTRICAL CHARACTERISTICS (T_A = 25°C, Body connected to Source unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNITS	TEST CONDITIONS
$V_{GS(TH)}$	Gate to Source Threshold Voltage	0.50	1.5	3.0	V	$V_{DS} = V_{GS}$, I_D = 10 μA, V_{BS} = 0
I_{DSS}	Drain Leakage Current		0.1	10	nA	V_{DS} = 10 V, $V_{GS} = V_{BS}$ = 0
I_{GSS}	Gate Leakage Current					(See Note 2)
BV_{DSS}	Drain Breakdown Voltage	25			V	I_D = 10 μA, $V_{GS} = V_{BS}$ = 0
$r_{DS(on)}$	Drain To Source on Resistance		25	50	ohms	V_{GS} = 20 V, V_{BS} = 0
$I_{D(on)}$	Drain Current	10	50		mA	$V_{DS} = V_{GS}$ = 10 V, V_{BS} = 0
Y_{fs}	Forward Transadmittance	3,000			μmhos	V_{DS} = 10 V, I_D = 10 mA, f = 1 KHz, V_{BS} = 0
C_{iss}	Total Gate Input Capacitance		5.0	6.0	pF	I_D = 10 mA, V_{DS} = 10 V, f = 1 MHz, V_{BS} = 0
C_{dg}	Gate to Drain Capacitance		1.3	1.6	pF	V_{DG} = 10 V, V_{BS} = 0

INTERSIL

M116

Diode Protected N-Channel Enhancement Mode MOS FET

GENERAL DESCRIPTION

- Low I_{GSS}
- Integrated Zener Clamp Protects the Gate

PRODUCT CONDITIONING

Units receive the following treatment before final electrical tests:

High Temp Storage: 24 Hours at 150°C

25,000 Acceleration/Impact in the Y_1 Plane

Thermal Shock: +100 to 0°C for 5 Cycles

Helium and/or Gross Leak Tests for Hermeticity

ABSOLUTE MAXIMUM RATINGS (25°C)

Drain-to-Source Voltage	30 V
Gate-to-Drain Voltage	30V
Drain Current	50 mA
Gate Zener Current	±0.1 mA
Storage Temperature	-65 to 150°C
Operating Junction Temperature	-55 to 125°C
Total Device Dissipation (Derate 2.25 mW/°C to 125°C)	225 mW

ORDERING INFORMATION

TO72	WAFER	CHIP
M116	M116/W	M116/D

PACKAGE DIMENSIONS

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		M116 MIN	M116 MAX	UNITS	TEST CONDITIONS
$r_{DS(on)}$	Drain Source ON Resistance		100 200	Ω	V_{GS} = 20 V, I_D = 100 μA, V_{BS} = 0 V_{GS} = 10 V, I_D = 100 μA, V_{BS} = 0
$V_{GS(th)}$	Gate Threshold Voltage	1	5	V	V_{GS} = V_{DS}, I_D = 10 μA, V_{BS} = 0
BV_{DSS}	Drain-Source Breakdown Voltage	30		V	I_D = 1 μA, V_{GS} = V_{BS} = 0
BV_{SDS}	Source-Drain Breakdown Voltage	30		V	I_S = 1 μA, V_{GD} = V_{BD} = 0
BV_{GBS}	Gate-Body Breakdown Voltage	30	60	V	I_G = 10 μA, V_{SB} = V_{DB} = 0
$I_{D(OFF)}$	Drain Cutoff Current		10	NA	V_{DS} = 20 V, V_{GS} = V_{BS} = 0
$I_{S(OFF)}$	Source Cutoff Current		10	NA	V_{SD} = 20 V, V_{GD} = V_{BD} = 0
I_{GSS}	Gate-Body Leakage		100	PA	V_{GS} = 20 V, V_{DS} = V_{BS} = 0
C_{gs} or C_{gd}	Gate-Source or Gate-Drain Capacitance		2.5	pF	V_{GB} = V_{DB} = V_{SB} = 0, f = 1 MHz Body Guarded
C_{db}	Drain-Body Capacitance		7	pF	V_{GB} = 0, V_{DB} = 10 V, f = 1 MHz
C_{iss}	Input Capacitance		10	pF	V_{GB} = 0, V_{DB} = 10 V, V_{BS} = 0 f = 1 MHz

INTERSIL

3N160
P-Channel Enhancement Mode MOS FET

GENERAL DESCRIPTION

ENHANCEMENT-TYPE METAL-OXIDE SEMICONDUCTOR TRANSISITOR

For applications requiring very high input impedance, such as series and shunt choppers, multiplexers, and commutators.

- Channel Cut Off with Zero Gate Voltage
- Square-Law Transfer Characteristic Reduces Distortion
- Independent Substrate Connection Provides Flexibility in Biasing

ABSOLUTE MAXIMUM RATINGS

@25°C free-air temperature (unless otherwise noted)

Drain-Gate Voltage	−25 V
Drain-Source Voltage	−25 V
Forward Gate-Source Voltage	−25 V
Reverse Gate-Source Voltage	+25 V
Continuous Drain Current	−125 mA
Continuous Device Dissipation at (or below) 25°C Free-Air Temperature	360 mW
Continuous Device Dissipation at (or below) 25°C Case Temperature	1.8 W
Storage Temperature Range	−65°C to 200°C
Lead Temperature 1/16 Inch from Case for 10 Seconds	300°C

HANDLING PRECAUTIONS

Curve-tracer testing and static-charge buildup are common causes of damage to insulated-gate devices. Permanent damage may result if either gate-voltage rating is exceeded even for extremely short time periods. Each transistor is protected during shipment by a gate-shorting device, which should be removed only during testing and after permanent mounting of the transistor. Personnel and equipment, including soldering irons, should be grounded.

PACKAGE DIMENSIONS

NOTE: FOR DIE STRUCTURE, REFER TO 3N163

1503X2

ELECTRICAL CHARACTERISTICS (25°C free-air temperature unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT	TEST CONDITIONS	
I_{GSSF}	Forward Gate-Terminal Current		<−1	−50	pA	V_{GS} = −25 V, V_{DS} = 0	
			−10	−50	pA	V_{GS} = −25 V, V_{DS} = 0, T_A = 100°C	
I_{GSSR}	Reverse Gate-Terminal Current		<1	10	pA	V_{GS} = 25 V, V_{DS} = 0	
I_{DSS}	Zero-Gate-Voltage Drain Current		<1	−10	nA	V_{DS} = −15 V, V_{GS} = 0	
				−10	μA	V_{DS} = −25 V, V_{GS} = 0	
$V_{GS(th)}$	Gate-Source Threshold Voltage	−1.5		−5	V	V_{DS} = −15 V, I_D = −10 μA	
V_{GS}	Gate-Source Voltage	−4.5		−8	V	V_{DS} = −15 V, I_D = −8 mA	
$I_{D(on)}$	On-State Drain Current	−40		−120	mA	V_{DS} = −15 V, V_{GS} = −15 V,	
$\lvert y_{fs} \rvert$	Small-Signal Common-Source Forward Transfer Admittance	3.5		6.5	mmho	V_{DS} = −15 V I_D = −8 mA	f = 1 kHz
$\lvert y_{os} \rvert$	Small-Signal Common-Source Output Admittance			0.25	mmho		
C_{iss}	Common-Source Short-Circuit Input Capacitance			10	pF		f = 1 MHz
C_{rss}	Common-Source Short-Circuit Reverse Transfer Capacitance			4	pF		

INTERSIL

3N161

Diode Protected P-Channel Enhancement Mode MOS FET

GENERAL DESCRIPTION

DIODE-PROTECTED ENHANCEMENT-TYPE METAL-OXIDE-SEMICONDUCTOR TRANSISTOR

For applications requiring very high input impedance, such as series and shunt choppers, multiplexers, and commutators.

FEATURES

- Channel Cut Off with Zero Gate Voltage
- Square-Law Transfer Characteristic Reduces Distortion
- Independent Substrate Connection Provides Flexibility in Biasing
- Internally Connected Diode Protects Gate from Damage due to Overvoltage

1

DESCRIPTION

These devices are designed for applications requiring very high input impedance, such as choppers, commutators, and logic switches. Each device is protected from excessive input voltage by a shunting diode connected from the gate to the substrate. This eliminates the need for most precautionary handling procedures associated with unprotected MOS devices.

PACKAGE DIMENSIONS

TO-72

PIN	OUT
1	D
2	G
3	B C
4	S

NOTE: FOR DIE STRUCTURE, REFER TO 3N172

1503ZX2

ELECTRICAL CHARACTERISTICS (25°C free-air temperature unless otherwise noted)

PARAMETER		MIN	TYP	MAX	UNIT	TEST CONDITIONS	
I_{GSSF}	Forward Gate-Terminal Current			-0.1	nA	V_{GS} = -25 V, V_{DS} = 0	
				-1	nA	V_{GS} = -25 V, V_{DS} = 0,	T_A = 100°C
$V_{(BR)GSSF}$	Forward Gate-Source Breakdown Voltage	-25			V	I_G -0.1 mA, V_{DS} = 0,	
I_{DSS}	Zero-Gate-Voltage Drain Current			-10	nA	V_{DS} = -15 V, V_{GS} = 0	
				-10	μA	V_{DS} = -25 V, V_{GS} = 0	
$V_{GS(th)}$	Gate-Source Threshold Voltage	-1.5		-5	V	V_{DS} = -15 V, I_D = 10 μA	
V_{GS}	Gate-Source Voltage	-4.5		-8	V	V_{DS} = -15 V, I_D = -8 mA	
$I_{D(on)}$	On-State Drain Current	-40		-120	mA	V_{DS} = -15 V, V_{GS} = -15 V, See Note 4	
$\|y_{fs}\|$	Small-Signal Common-Source Forward Transfer Admittance	3500		6500	μmho	V_{DS} = -15 V, I_D = -8 mA	f = 1 kHz
$\|y_{os}\|$	Small-Signal Common-Source Output Admittance			250	μmho		
C_{iss}	Common-Source Short-Circuit Input Capacitance			10	pF		f = 1 MHz
C_{rss}	Common-Source Short-Circuit Reverse Transfer Capacitance			4	pF		

INTERSIL

3N163, 3N164

P-Channel Enhancement Mode MOS FET

FEATURES

- Very High Input Impedance
- High Gate Breakdown
- Fast Switching
- Low Capacitance

MAXIMUM RATINGS (@ 25°C ambient unless noted)

		3N163	3N164
V_{GSS}	Static Gate to Source Voltage	±40V	±30V
V_{GSS}(1)	Transmit Gate to Source Voltage	±125V	±125V
V_{DSS}	Drain to Source Voltage	-40V	-30V
V_{SDS}	Source to Drain Voltage	-40V	-30V
V_{DGO}	Drain to Gate Voltage	-40V	-30V
I_D	Drain Current	-50 mA	-50 mA
P_D	Power Dissipation	375 mW	
	Derating Factor	3.0 mW/°C	
T_j	Operating Junction Temperature	-55 to +150°C	
T_{sto}	Storage Temperature	-65 to +200°C	
T_l	Lead Temperature 1/16" from Case for 10 sec max	+265°C	

(1) Devices must not be tested at ±125V more than once or for longer than 300 ms.

PACKAGE DIMENSIONS TO-72

ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

		3N163 MIN	3N163 MAX	3N164 MIN	3N164 MAX	UNITS	TEST CONDITIONS
I_{GSS}	Gate Reverse Leakage Current		10①		10②	pA	①V_{GS} = 40V, ②V_{GS} = 30V
$I_{G(f)}$	Gate Forward Current		-10①		-10②	pA	①V_{GS} = -40V, ②V_{GS} = -30V
$I_{G(f)}$	Gate Forward Current @ 125°C		-25①		-25②	pA	①V_{GS} = -40V, ②V_{GS} = -30V
BV_{DSS}	Drain-Source Breakdown Voltage	-40		-30		V	I_D = -10 μA, V_{GS} = 0
BV_{SDS}	Source Drain Breakdown Voltage	-40		-30		V	I_S = -10 μA, V_{GD} = 0, V_{DB} = 0
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0	V	V_{DS} = V_{GS}, I_D = -10 μA
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0	V	V_{DS} = -15V, I_D = -10 μA
V_{GS}	Gate Source Voltage	-3.0	-6.5	-3.0	-6.5	V	V_{DS} = -15V, I_D = 0.5 mA
I_{DSS}	Zero Gate Voltage Drain Current		200		400	pA	V_{DS} = -15V, V_{GS} = 0
I_{SDS}	Source Drain Current		400		800	pA	V_{SD} = 15V, V_{GS} = V_{DB} = 0
$r_{ds(on)}$	Drain-Source on Resistance		250		300	ohms	V_{GS} = -20V, I_D = -100 μA
$I_{D(on)}$	On Drain Current	-5.0	-30.0	-3.0	-30.0	mA	V_{DS} = -15V, V_{GS} = -10V
Y_{fs}	Forward Transconductance @ 1 kHz	2000	4000	1000	4000	μmhos	V_{DS} = -15V, I_D = -10 mA
Y_{OS}	Output Admittance @ 1 kHz		250		250	μmhos	V_{DS} = -15V, I_D = -10 mA
C_{iss}	Input Capacitance – Output Shorted		2.5		2.5	pF	V_{DS} = -15V, I_D = -10 mA, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance		0.7		0.7	pF	V_{DS} = -15V, I_D = -10 mA, f = 1 MHz
C_{oss}	Output Capacitance Input Shorted		3.0		3.0	pF	V_{DS} = -15V, I_D = -10 mA, f = 1 MHz

SWITCHING CHARACTERISTICS (@ 25°C and V_{BS} = 0)

t_{on}	Turn-On Delay Time	12	12	ns	V_{DD} = -15V
t_r	Rise Time	24	24	ns	$I_{D(on)}$ = 10 mA
t_{off}	Turn-Off Time	50	50	ns	R_G = R_L = 1.4 kΩ

SWITCHING TIME CIRCUIT

SWITCHING WAVEFORM

1

INTERSIL

3N172, 3N173

P-Channel Enhancement Mode MOS FET

FEATURES

- High Input Impedance
- Diode Protected Gate

PACKAGE DIMENSIONS TO-72

MAXIMUM RATINGS (@ 25°C ambient unless noted)

		3N172	3N173
V_{GSS}	Gate to Source Voltage	-40V	-30V
V_{DSS}	Drain to Source Voltage	-40V	-30V
V_{SDS}	Source to Drain Voltage	-40V	-30V
V_{DGO}	Drain to Gate Voltage	-40V	-30V
I_D	Drain Current	-50 mA	-50 mA
$I_{G(f)}$	Gate Forward Current	10 μA	10 μA
$I_{G(r)}$	Gate Reverse Current	1.0 mA	1.0 mA
P_D	Power Dissipation	375 mW	
	Derating Factor	3.0 mW/°C	
T_j	Operating Junction Temperature	-55 to +150°C	
T_{stg}	Storage Temperature	-65 to +200°C	
T_l	Lead Temperature 1/16" from Case for 10 sec max	+256°C	

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ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

		3N172		3N173		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX		
I_{GSS}	Gate Reverse Current		-200		-500	pA	V_{GS} = -20V
I_{GSS}	Gate Reverse Current (+125°C)		-0.5		-1.0	μA	V_{GS} = -20V
BV_{GSS}	Gate Breakdown Voltage	-40	-125	-30	-125	V	I_D = -10 μA
BV_{DSS}	Drain-Source Breakdown Voltage	-40		-30		V	I_D = -10 μA
BV_{SDS}	Source-Drain Breakdown Voltage	-40		-30		V	I_S = -10 μA, V_{DB} = 0
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0	V	V_{DS} = V_{GS}, I_D = -10 μA
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0	V	V_{DS} = -15V, I_D = -10 μA
V_{GS}	Gate Source Voltage	-3.0	-6.5	-2.5	-6.5	V	V_{DS} = -15V, I_D = -500 μA
I_{DSS}	Zero Gate Voltage Drain Current		-0.4		-10	nA	V_{DS} = -15V
I_{SDS}	Zero Gate Voltage Source Current		-0.4		-10	nA	V_{SD} = -15V, V_{DB} = 0
$r_{ds(on)}$	Drain Source On Resistance		250		350	ohms	V_{GS} = -20V, I_D = -100 μA
$I_{D(th)}$	On Drain Current	-5.0	-30	-5.0	-30	mA	V_{DS} = -15V, V_{GS} = -10V

INTERSIL

IT1700

P-Channel Enhancement Mode MOS FET

FEATURES

- Low On-Resistance – $r_{DS(on)} \leq 400$ ohms
- High Input Impedance – 10^{15} ohms
- High Gate Breakdown Voltage – $V_{GSS} \pm 125$ V
- Low Leakage – $I_{DSS} \leq 200$ pA
- High Gain – $g_{fs} > 2000$ μmhos
- Low Noise Voltage – e_n 150 nV/√Hz typical @ 100 Hz

ORDERING INFORMATION

TO72	WAFER	CHIP
IT1700	IT1700/W	IT1700/D

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures	
Storage Temperature	-65°C to +200°C
Operating Junction Temperature	-55°C to +150°C
Lead Temperature (soldering, 10 second time limit)	+300°C
Maximum Power Dissipation	
Total Dissipation at 25°C Ambient Temperature	0.375 W
Linear Derating Factor at 25°C Ambient Temperature	3 mW/°C
Total Dissipation at 25°C Case Temperature	1.25 W
Linear Derating Factor at 25°C Case Temperature	10 mW/°C
Maximum Voltages and Current	
V_{DSS} Drain to Source and Body Voltage	-40 V
V_{SDS} Source to Drain and Body Voltage	-40 V
V_{GSS} Transient Gate to Source Voltage (Note 2)	±125 V
V_{GSS} Gate to Source Voltage	-40 V
$I_{D(on)}$ Drain Current	50 mA

PACKAGE DIMENSIONS

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

	PARAMETER	MIN	MAX	UNITS	TEST CONDITIONS
BV_{DSS}	Drain to Source Breakdown Voltage	-40		V	$V_{GS} = 0$, $I_D = -10$ μA
BV_{SDS}	Source to Drain Breakdown Voltage	-40		V	$V_{GS} = 0$, $I_D = -10$ μA
I_{GSS}	Gate Leakage Current				(See Note 2)
I_{DSS}	Drain to Source Leakage Current		200	pA	$V_{GS} = 0$, $V_{DS} = -20$ V
I_{DSS} (150°C)	Drain to Source Leakage Current		0.4	μA	$V_{GS} = 0$, $V_{DS} = -20$ V
I_{SDS}	Source to Drain Leakage Current		400	pA	$V_{GS} = 0$, $V_{DS} = -20$ V
I_{SDS} (150°C)	Source to Drain Leakage Current		0.8	μA	$V_{GS} = 0$, $V_{DS} = -20$ V
$V_{GS(th)}$	Gate Threshold Voltage	-2	-5	V	$V_{GS} = V_{DS}$, $I_D = -10$ μA

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

	PARAMETER	MIN	TYP	MAX	UNITS	TEST CONDITIONS
r_{DS} (on)	Static Drain to Source "on" Resistance			400	ohms	$V_{GS} = -10$ V, $V_{DS} = 0$
I_{DS} (on)	Drain to Source "on" Current	2			mA	$V_{GS} = -10$ V, $V_{DS} = -15$ V
g_{fs}	Forward Transconductance Common Source	2000		4000	μmhos	$V_{DS} = -15$ V, $I_D = -10$ mA f = 1 kHz
C_{iss}	Small Signal, Short Circuit, Common Source, Input Capacitance			5	pF	$V_{DS} = -15$ V, $I_D = -10$ mA f = 1 MHz
C_{rss}	Small Signal, Short Circuit, Common Source, Reverse Transfer Capacitance			1.2	pF	$V_{DG} = -15$ V, $I_D = 0$ f = 1 MHz
C_{oss}	Small Signal, Short Circuit, Common Source, Output Capacitance			3.5	pF	$V_{DS} = -15$ V, $I_D = -10$ mA f = 1 MHz
$\overline{e_n}$	Equivalent Input Noise Voltage		150		nV/√Hz	$V_{DS} = -15$ V, $I_D = -1$ mA f = 100 Hz; BW = Hz

NOTE: 1. These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.

2. Actual gate current is immeasurable. Package suppliers are required to guarantee a package leakage of < 10 pA. External package leakage is the dominant mode which is sensitive to both transient and storage environment, which cannot be guaranteed.

INTERSIL

3N165 3N166

Dual Matched P-Channel Enhancement Mode MOS FETS

FEATURES

- Very High Input Impedance
- High Gate Breakdown
- Low Capacitance

MAXIMUM RATINGS (@ 25°C ambient unless noted)

V_{GSS}	Static Gate to Source Voltage	±40V
V_{GSS} (1)	Transient Gate to Source Voltage	±125V
V_{DSS}	Drain to Source Voltage	-40V
V_{GDS}	Source to Drain Voltage	-40V
V_{GG}	Gate to Gate	±80V
V_G	Any Lead to Case	±40V
I_D	Drain Current	50 mA
P_D	Power Dissipation (each side)	300 mW
	(both sides)	525 mW
	Total Derating Factor	4.2 mW/°C
T_j	Operating Junction Temperature	-55 to +150°C
T_{stg}	Storage Temperature	-65 to +200°C
T_l	Lead Temperature 1/16" from Case for 10 sec max	+300°C

(1) Devices must not be tested at ±125V more than once or for longer than 300 ms.

PACKAGE DIMENSIONS

ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

		3N165 MIN	3N165 MAX	3N166 MIN	3N166 MAX	UNITS	TEST CONDITIONS
I_{GSS}	Gate Reverse Leakage Current		10		10	pA	V_{GS} = 40V
$I_{G(f)}$	Gate Forward Leakage Current		-10		-10	pA	V_{GS} = -40V
$I_{G(f)}$	Gate Forward Leakage Current (+125°C)		-25		-25	pA	V_{GS} = -40V
I_{DSS}	Drain to Source Leakage Current		-200		-200	pA	V_{DS} = -20V
I_{SDS}	Source to Drain Leakage Current		-400		-400	pA	V_{SD} = -20V, V_{DB} = 0
$I_{D(on)}$	On Drain Current	-5	-30	-5	-30	mA	V_{DS} = -15V, V_{GS} = -10V
$V_{GS(th)}$	Gate Source Threshold Voltage	-2	-5	-2	-5	V	V_{DS} = -15V, I_D = -10 μA
$V_{GS(th)}$	Gate Source Threshold Voltage	-2	-5	-2	-5	V	V_{DS} = V_{GS}, I_D = -10 μA
$r_{ds(on)}$	Drain Source On Resistance		300		300	ohms	V_{GS} = -20V, I_D = -100 μA
g_{fs}	Forward Transconductance	1500	3000	1500	3000	μmhos	V_{DS} = -15V, I_D = -10 mA, f = 1 kHz
g_{os}	Output Admittance		300		300	μmhos	V_{DS} = -15V, I_D = -10 mA, f = 1 kHz
C_{iss}	Input Capacitance		3.0		3.0	pF	V_{DS} = -15V, I_D = -10 mA, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance		0.7		0.7	pF	V_{DS} = -15V, I_D = -10 mA, f = 1 MHz
C_{oss}	Output Capacitance Input Shorted		3.0		3.0	pF	V_{DS} = -15V, I_D = -10 mA, f = 1 MHz
$R_E(Y_{fs})$	Real Part Forward Transconductance	1200			1200	μmhos	V_{DS} = -15V, I_D = -10 mA, f = 100 MHz

MATCHING CHARACTERISTICS 3N165

		MIN	MAX	UNITS	TEST CONDITIONS
Y_{fs1}/Y_{fs2}	Forward Transconductance Ratio	0.90	1.0		V_{DS} = -15V, I_D = -500 μA, f = 1 kHz
$V_{GS1\,2}$	Gate-Source Threshold Voltage Differential		100	mV	V_{DS} = -15V, I_D = -500 μA
$\Delta V_{GS1\,2}$	Gate-Source Threshold Voltage Differential Change with Temperature		8	mV	V_{DS} = -15V, I_D = -500 μA T = -55°C to +25°C
$\Delta V_{GS1\,2}$	Gate-Source Threshold Voltage Differential Change with Temperature		10	mV	V_{DS} = -15V, I_D = -500 μA T = +25°C to +125°C

INTERSIL

3N188 3N189 3N190 3N191

Dual Matched P-Channel Enhancement Mode MOS FETS

FEATURES

- Very High Input Impedance
- Low Capacitance
- High Gate Breakdown 3N190-3N191
- V_g & (TH) Matched
- Zener Protected gate 3N188-3N189
- V_g & (TH) Tracking

MAXIMUM RATINGS (@25°C ambient unless noted)

		3N188 3N189	3N190 3N191
V_{GSS}	Static Gate to Source Voltage	±40V	-40V
V_{GSS}(1)	Transient Gate to Source Voltage	±40V	±125V
V_{DSS}	Drain to Source Voltage	-40V	-40V
V_{SDS}	Source to Drain Voltage	-40V	-40V
I_D	Drain Current	50 mA	50 mA
P_D	Power Dissipation (each side)	300 mW	
	(both sides)	525 mW	
	Total Derating Factor	4.2 mW/°C	
T_j	Operating Junction Temperature	-55 to +150°C	
T_{stg}	Storage Temperature	-65 to +200°C	
T_l	Lead Temperature 1/16" from Case for 10 sec max	+300°C	

(1) Device must not be tested at b125V more than once or for longer than 300 ms.

PACKAGE DIMENSIONS

TO-99

LEAD 1	DRAIN 1
LEAD 2	SOURCE 1
LEAD 3	GATE 1
LEAD 4	BODY
LEAD 5	GATE 2
LEAD 6	SOURCE 2
LEAD 7	DRAIN 2
LEAD 8	(NOT CONNECTED)

2506C

ORDERING INFORMATION

TO99	WAFER	CHIP
3N188		
3N189		
3N190	3N190/W	3N190/D
3N191	3N191/W	3N191/D

ALL DIMENSIONS IN INCHES UNLESS OTHERWISE NOTED
BODY (SUBSTRATE) INTERNALLY CONNECTED TO METAL CASE

ELECTRICAL CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

		3N188 3N189 MIN	3N188 3N189 MAX	3N190 3N191 MIN	3N190 3N191 MAX	UNITS	TEST CONDITIONS
I_{GSS}	Gate Reverse Current				10	pA	V_{GS} = 40V
$I_{G(f)}$	Gate Forward Current		-200		-10	pA	V_{GS} = -40V
$I_{G(f)}$	Gate Forward Current @ 125°C		-200		-25	pA	V_{GS} = -40V
BV_{DSS}	Drain-Source Breakdown Voltage	-40		-40		V	I_D = -10μA
BV_{SDS}	Source-Drain Breakdown Voltage	-40		-40		V	I_S = -10μA, V_{BD} = 0
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0	V	V_{DS} = -15V, I_D = -10 μA
$V_{GS(th)}$	Threshold Voltage	-2.0	-5.0	-2.0	-5.0	V	V_{DS} = V_{GS}, I_D = -10 μA
V_{GS}	Gate Source Voltage	-3.0	-6.5	-3.0	-6.5	V	V_{DS} = -15V I_D = -500 μA
I_{DSS}	Zero Gate Voltage Drain Current		-200		-200	pA	V_{DS} = -15V
I_{SDS}	Source Drain Current		-400		-400	pA	V_{SD} = -15V, V_{DB} = 0
$r_{ds(on)}$	Drain-Source on Resistance		300		300	ohms	V_{DS} = -20V, I_D = -100 μA
$I_{D(on)}$	On Drain Current	-5.0	-30.0	-5.0	-30.0	mA	V_{DS} = -15V, V_{GS} = -10V
g_{fs}	Forward Transconductance	1500	4000	1500	4000	μmhos	V_{DS} = -15V, I_D = -5 mA, f = 1 kHz
Y_{OS}	Output Admittance		300		300	μmhos	V_{DS} = -15V, I_D = -5 mA, f = 1 kHz
C_{iss}	Input Capacitance Output Shorted		4.5		4.5	pF	V_{DS} = -15V, I_D = -5 mA, f = 1 MHz
C_{rss}	Reverse Transfer Capacitance		1.5		1.0	pF	V_{DS} = -15V, I_D = -5 mA, f = 1 MHz
C_{oss}	Output Capacitance Input Shorted		3.0		3.0	pF	V_{DS} = -15V, I_D = -5 mA, f = 1 MHz

SWITCHING CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted)

		MIN	MAX	UNITS	TEST CONDITIONS
$t_{D(on)}$	Turn On Delay Time		15	ns	V_{DD} = -15V, I_D = -5 mA
t_r	Rise Time		30	ns	R_G = R_L = 1.4 kΩ
t_{off}	Turn Off Time		50	ns	

MATCHING CHARACTERISTICS (@ 25°C and V_{BS} = 0 unless noted) 3N188 and 3N190

		MIN	MAX	UNITS	
Y_{fs1}/Y_{fs2}	Forward Transconductance Ratio	0.85	1.0		V_{DS} = -15V, I_D = -500 μA, f = 1 kHz
V_{GS1-2}	Gate Source Threshold Voltage Differential		100	mV	V_{DS} = -15V, I_D = -500 μA
ΔV_{GS1-2}	Gate Source Threshold Voltage Differential Change with Temperature		8	mV	V_{DS} = -15V, I_D = -500 μA, T = -55°C to +25°C
$\frac{\Delta V_{GS1-2}}{\Delta T}$	Gate Source Threshold Voltage Differential Change with Temperature		10	mV	V_{DS} = -15V, I_B = -500 μA, T = +25°C to +125°C

INTERSIL

2N2453 2N2453A
Monolithic Dual Matched NPN Transistor

MAXIMUM RATINGS

CHARACTERISTIC	SYMBOL	RATING		UNIT
Collector-Base Voltage 2N2453 2N2453A	V_{CBO}	60 80		Volts
Collector-Emitter Voltage 2N2453 2N2453A	V_{CEO}	30 50		Volts
Emitter-Base Voltage	V_{EBO}	7.0		Volts
		Each Side	Both Sides	
Total Device Dissipation @ $T_A = 25°C$ @ $T_C = 100°C$ @ $T_C = 25°C$	P_D	0.2 0.35 0.6	0.3 0.7 1.2	Watts
Storage Temperature	T_{stg}	−65 to +200		°C
Junction Temperature	T_J	+200		°C
Derating Factor above 25°C 2N2453 2N2453A		1.14 1.71		mW/°C

FEATURES

- Closely Matched Current Gain
- Very Closely Matched, V_{BE}
- Low Differential Drift

PACKAGE DIMENSIONS

TO-78

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

	PARAMETER		MIN	MAX	UNIT	TEST CONDITIONS	
BV_{CBO}	Collector-Base Breakdown Voltage	2N2453 2N2453A	60 80		V	$I_C = 10\ \mu A$, $I_E = 0$	
BV_{EBO}	Emitter-Base Breakdown Voltage		7.0		V	$I_C = 0$, $I_E = 0.1\ \mu A$	
$V_{CEO(sus)}$**	Collector-Emitter Sustaining Voltage	2N2453 2N2453A	30 60		V	$I_C = 10$ mA, $I_B = 0$	
$V_{CE(sat)}$	Collector Saturation Voltage			1.0	V	$I_C = 5.0$ mA, $I_B = 0.5$ mA	
$V_{BE(sat)}$	Base Saturation Voltage			0.9	V	$I_C = 5.0$ mA, $I_B = 0.5$ mA	
I_{CBO}	Collector-Base Cutoff Current	2N2453 2N2453A 2N2453 2N2453A		5.0 5.0 10 10	nA nA μA μA	$I_E = 0$, $V_{CB} = 50$ V $I_E = 0$, $V_{CB} = 60$ V $I_E = 0$, $V_{CB} = 50$ V $I_E = 0$, $V_{CB} = 60$ V	 $T_A = 150°C$ $T_A = 150°C$
I_{EBO}	Emitter-Base Cutoff Current			2.0	nA	$I_C = 0$, $V_{EB} = 5.0$ V	
h_{FE}	DC Current Gain		80 40 150 75	600		$I_C = 10\ \mu A$, $V_{CE} = 5.0$ V $I_C = 10\ \mu A$, $V_{CE} = 5.0$ V $I_C = 1.0$ mA, $V_{CE} = 5.0$ V $I_C = 1.0$ mA, $V_{CE} = 5.0$ V	 $T_A = -55°C$ $T_A = -55°C$
h_{FE1}/h_{FE2}*	DC Current Gain Ratio	2N2453A only Both Types Both Types	0.9 0.9 0.85	1.0 1.0 1.0		$I_C = 100\ \mu A$, $V_{CE} = 5.0$ V $I_C = 1.0$ mA, $V_{CE} = 5.0$ V $I_C = 1.0$ mA, $V_{CE} = 5.0$ V	 $T_A = -55°C$ to $+125°C$
$V_{BE1}-V_{BE2}$	Base Voltage Differential			5.0 3.0	mV	$I_C = 1.0$ mA, $V_{CE} = 5.0$ V $I_C = 10\ \mu A$, $V_{CE} = 5.0$ V	
$\Delta(V_{BE1}-V_{BE2})/\Delta T$	Base Voltage Differential Drift	2N2453 2N2453A		10 5.0	μV/°C	$I_C = 10\ \mu A$, $V_{CE} = 5.0$ V	$T_A = -55°C$ to $+125°C$
h_{fe}	Small Signal Current Gain		150	600		$I_C = 1.0$ mA, $V_{CE} = 5.0$ V	f = 1 kHz
$\lvert h_{fe} \rvert$	High Frequency Current Gain		2.0			$I_C = 5.0$ mA, $V_{CE} = 10$ V	f = 30 MHz
C_{ob}	Output Capacitance	2N2453 2N2453A		8.0 4.0	pF	$I_E = 0$, $V_{CB} = 10$ V	f = 140 kHz
C_{ib}	Input Capacitance			10	pF	$I_C = 0$, $V_{BE} = 0.5$ V	f = 140 kHz
h_{rb}	Voltage Feedback Ratio			5.0	$\times 10^{-4}$	$I_C = 1.0$ mA, $V_{CE} = 5.0$ V	f = 1 kHz
h_{re}	Reverse Voltage Feedback Ratio			6.0	$\times 10^{-4}$	$I_C = 1.0$ mA, $V_{CE} = 5.0$ V	f = 1 kHz
h_{ib}	Input Resistance		20	30	ohms	$I_C = 1.0$ mA, $V_{CB} = 5.0$ V	f = 1 kHz
h_{ie}	Input Resistance			5.0	kΩ	$I_C = 1.0$ mA, $V_{CE} = 5.0$ V	f = 1 kHz
h_{ob}	Output Conductance			0.2	μmhos	$I_C = 1.0$ mA, $V_{CB} = 5.0$ V	f = 1 kHz
h_{oe}	Output Conductance		5.0	30	μmhos	$I_C = 1.0$ mA, $V_{CB} = 5.0$ V	f = 1 kHz
NF	Low Frequency Noise Figure	2N2453 2N2453A		7.0 4.0	dB	f = 1 kHz Source resistance = 10 kΩ Equivalent noise power bandwidth = 200 Hz $I_C = 10\ \mu A$, $V_{CE} = 5.0$ V	

*The lower of the h_{FE} readings is taken as h_{FE1}. **Pulse Test: Pulse Width = 300 μsec; Duty Cycle = 1%.

INTERSIL

2N4044, 2N4045, 2N4100, 2N4878, 2N4879, 2N4880

Dual Monolithic Matched NPN Silicon Planar Transistors

FEATURES

- High Gain At Low Current $h_{FE} \geqslant 200$ @ 10 μA
- Low Output Capacitance $C_{obo} \leqslant 0.8$ pF
- h_{FE} Match $h_{FE_1} / h_{FE_2} \leqslant 10\%$
- Tight V_{BE} Tracking
  $\Delta (V_{BE_1} - V_{BE_2}) \leqslant 3\ \mu V/^\circ C$ $-55^\circ C$ to $+125^\circ C$
- Dielectrically isolated matched pairs for differential amplifiers.

GENERAL DESCRIPTION

Dual monolithic matched NPN silicon planar transistors used for differential amplifier applications.

ABSOLUTE MAXIMUM RATINGS

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C

Maximum Power Dissipation

	TO-71		TO-78	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Total Dissipation at 25°C Case Temperature	0.3 Watt	0.5 Watt	0.4 Watt	0.75 Watt
Derating Factor	1.7mW/°	2.9mW/°C	2.3mW/°C	4.3mW/°C

		2N4044 2N4878	2N4100 2N4879	2N4045 2N4880
V_{CBO}	Collector to Base Voltage	60 V	55 V	45 V
V_{CEO}	Collector to Emitter Voltage	60 V	55 V	45 V
V_{EBO}	Emitter to Base Voltage (Note 2)	7 V	7 V	7 V
V_{CCO}	Collector to Collector Voltage	100 V	100 V	100 V
I_C	Collector Current	10mA	10mA	10mA

ORDERING INFORMATION

TO78	TO71	WAFER	CHIP
2N4044		2N4044/W	2N4044/D
2N4045		2N4045/W	2N4045/D
2N4100		2N4100/W	2N4100/D
	2N4878		
	2N4879		
	2N4880		

PACKAGE DIMENSIONS

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N4044 2N4878		2N4100 2N4879		2N4045 2N4880		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	200	600	150	600	80	800		I_C = 10 μA, V_{CE} = 5V
h_{FE}	DC Current Gain	225		175		100			I_C = 1.0 mA, V_{CE} = 5 V
$h_{FE}(-55^\circ C)$	DC Current Gain	75		50		30			I_C = 10 μA, V_{CE} = 5 V
$V_{BE(on)}$	Emitter-Base On Voltage		0.7		0.7		0.7	V	I_C = 10 μA, V_{CE} = 5 V
$V_{CE(sat)}$	Collector Saturation Voltage		0.35		0.35		0.35	V	I_C = 1.0 mA, I_B = 0.1 mA
I_{CBO}	Collector Cutoff Current		0.1		0.1		0.1*	nA	I_E = 0, V_{CB} = 45 V, 30 V*
$I_{CBO}(+150^\circ C)$	Collector Cutoff Current		0.1		0.1		0.1*	μA	I_E = 0, V_{CB} = 45 V, 30 V*
I_{EBO}	Emitter Cutoff Current		0.1		0.1		0.1	nA	I_C = 0, V_{EB} = 5 V
C_{obo}	Output Capacitance		0.8		0.8		0.8	pF	I_E = 0, V_{CB} = 5 V

INTERSIL

IT120 IT120A IT121 IT122
Dual Monolithic Matched NPN Silicon Planar Transistors

FEATURES

- High h_{FE} at Low Current >200 @ 10 μA
- Low Output Capacitance <2.0 pf
- $I_{B_1} - I_{B_2}$ <2.5 nA
- Tight V_{BE} Tracking $<3.0\ \mu V/^\circ C$

GENERAL DESCRIPTION

Matched pairs for differential amplifiers.

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C

Maximum Power Dissipation

	TO-78		TO-71	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Total Dissipation at 25°C Case Temperature	0.4 Watt	0.75 Watt	0.3 Watt	0.5 Watt
Derating Factor	2.3mW/°C	4.3mW/°C	1.7mW/°C	4.3mW/°C

Maximum Voltage & Current for Each Transistor

V_{CBO}	Collector to Base Voltage	45 V
V_{CEO}	Collector to Emitter Voltage	45 V
V_{EBO}	Emitter to Base Voltage	7.0 V
V_{CCO}	Collector to Collector Voltage	60 V
I_C	Collector Current	50mA

ORDERING INFORMATION

TO78	TO71	WAFER	CHIP
IT120A	IT120A-TO71	IT120A/W	IT120A/D
IT120	IT120-TO71	IT120/W	IT120/D
IT121	IT121-TO71	IT121/W	IT121/D
IT122	IT122-TO71	IT122/W	IT122/D

PACKAGE DIMENSIONS

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		IT120A MIN	IT120A MAX	IT120 MIN	IT120 MAX	IT121 MIN	IT121 MAX	IT122 MIN	IT122 MAX	UNIT	TEST CONDITIONS
h_{FE}	DC Current Gain	200		200		80		80			$I_C = 10\ \mu A$, $V_{CE} = 5.0$ V
h_{FE}	DC Current Gain	225		225		100		100			$I_C = 1.0$ mA, $V_{CE} = 5.0$ V
$h_{FE}(-55°C)$	DC Current Gain	75		75		30		30			$I_C = 10\ \mu A$, $V_{CE} = 5.0$ V
$V_{BE}(ON)$	Emitter-Base On Voltage		0.7		0.7		0.7		0.7	V	$I_C = 10\ \mu A$, $V_{CE} = 5.0$ V
$V_{CE}(SAT)$	Collector Saturation Voltage		0.5		0.5		0.5		0.5	V	$I_C = 0.5$ mA, $I_B = 0.05$ mA
I_{CBO}	Collector Cutoff Current		1.0		1.0		1.0		1.0	nA	$I_E = 0$, $V_{CB} = 45$ V
$I_{CBO}(+150°C)$	Collector Cutoff Current		10		10		10		10	μA	$I_E = 0$, $V_{CB} = 45$ V
I_{EBO}	Emitter Cutoff Current		1.0		1.0		1.0		1.0	nA	$I_C = 0$, $V_{EB} = 5.0$ V
C_{OB}	Output Capacitance		2.0		2.0		2.0		2.0	pF	$I_E = 0$, $V_{CB} = 5.0$ V
C_{TE}	Emitter Transition Capacitance		2.5		2.5		2.5		2.5	pF	$I_C = 0$, $V_{EB} = 0.5$ V
$C_{C_1 \cdot C_2}$	Collector to Collector Capacitance		4.0		4.0		4.0		4.0	pF	$V_{CC} = 0$
$I_{C_1 \cdot C_2}$	Collector to Collector Leakage Current		10		10		10		10	nA	$V_{CC} = \pm 60$ V
$V_{CEO}(SUST)$	Collector to Emitter Sustaining Voltage	45		45		45		45		V	$I_C = 1.0$ mA, $I_B = 0$
f_T	Current Gain Bandwidth Product	10 220		10 220		7 180		7 180		MHz MHz	$I_C = 10\ \mu A$, $V_{CE} = 5$ V $I_C = 1$ mA, $V_{CE} = 5$ V
$\lvert V_{BE_1} - V_{BE_2} \rvert$	Base Emitter Voltage Differential		1		2		3		5	mV	$I_C = 10\ \mu A$, $V_{CE} = 5.0$ V
$\lvert I_{B_1} - I_{B_2} \rvert$	Base Current Differential		2.5		5		25		25	nA	$I_C = 10\ \mu A$, $V_{CE} = 5.0$ V
$\lvert \Delta(V_{BE_1} - V_{BE_2}) \rvert$	Base-Emitter Voltage Differential Change with Temperature		3		5		10		20	$\mu V/°C$	$T_A = -55°C$ to $+125°C$ $I_C = 10\ \mu A$, $V_{CE} = 5.0$ V

NOTES: (1) These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
(2) The lowest of two h_{FE} readings is taken as h_{FE_1} for purposes of this ratio.

INTERSIL

IT124

Super-Beta Dual Monolithic NPN Silicon Planar Transistors

FEATURES

- **Very High Gain — $h_{FE} \geq 1500$ @ 1 and 10μA**
- **Low Output Capacitance — $C_{obo} \leq 0.8$ pF**
- **Tight V_{BE} Matching — $|V_{BE1} - V_{BE2}|$ — 2 mV TYP.**
- **High f_T — 100 MHz**

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted).

Maximum Temperatures
- Storage Temperature ..... −65°C to +200°C
- Operating Junction Temperature ..... +200°C
- Lead Temperature (soldering, 10 second time limit) ..... +260°C

Maximum Power Dissipation — ONE SIDE / BOTH SIDES
- Device Dissipation @ Free Air — 400 mW / 750 mW
- Linear Derating Factor ..... 2.3 mW/°C / 4.3 mW/°C

Maximum Voltage and Current for Each Transistor
- V_{CBO} Collector to Base Voltage 2V
- V_{CEO} Collector to Emitter Voltage 2V
- V_{EBO} Emitter to Base Voltage (Note 2) 7V
- V_{CCO} Collector to Collector Voltage 100V
- I_C Collector Current 10mA

PACKAGE DIMENSIONS

TO-78

NOTES:
All dimensions in inches
Leads are gold-plated KOVAR
Package weight is 1.08 grams

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN	MAX	UNITS	CONDITIONS
h_{FE}	DC Current Gain	1500			$I_C = 1\mu A$, $V_{CE} = 1V$
h_{FE}	DC Current Gain	1500			$I_C = 10\mu A$, $V_{CE} = 1V$
h_{FE}(−55°C)	DC Current Gain	600			$I_C = 10\mu A$, $V_{CE} = 1V$
V_{BE}(ON)	Emitter-Base "ON" Voltage		0.7	V	$I_C = 10\mu A$, $V_{CE} = 1V$
V_{CE}(SAT)	Collector Saturation Voltage		0.5	V	$I_C = 1mA$, $I_B = 0.1mA$
I_{CBO}	Collector Cutoff Current		100	pA	$I_E = 0$, $V_{CB} = 1V$
I_{CBO}(+150°C)	Collector Cutoff Current		100	nA	$I_E = 0$, $V_{CB} = 1V$
I_{EBO}	Emitter Cutoff Current		100	pA	$I_C = 0$, $V_{EB} = 5V$
C_{OBO}	Output Capacitance		0.8	pF	$I_E = 0$, $V_{CB} = 1V$
C_{TE}	Emitter Transition Capacitance		1.0	pF	$I_C = 0$, $V_{EB} = 0.5V$
C_{C1C2}	Collector to Collector Capacitance		0.8	pF	$V_{CC} = 0$
I_{C1C2}	Collector to Collector Leakage Current		250	pA	$V_{CC} = \pm 50V$
f_T	Current Gain Bandwidth Product	10		MHz	$I_C = 10\mu A$, $V_{CE} = 1V$
f_T	Current Gain Bandwidth Product	100		MHz	$I_C = 100\mu A$, $V_{CE} = 1V$
NF	Narrow Band Noise Figure		3	dB	$I_C = 10\mu A$, $V_{CE} = 3V$, f = 1 KHz, $R_G = 10$ Kohms, BW = 200 Hz
BV_{CBO}	Collector-Base Breakdown Voltage	2		V	$I_C = 10\mu A$, $I_E = 0$
BV_{EBO}	Emitter-Base Breakdown Voltage	7		V	$I_E = 10\mu A$, $I_C = 0$
V_{CEO}(SUST)	Collector-Emitter Sustaining Voltage	2		V	$I_C = 1mA$, $I_B = 0$

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	TYP	MAX	UNITS	CONDITIONS
$\|V_{BE1}-V_{BE2}\|$	Base Emitter Voltage Differential	2	5	mV	$I_C = 10\mu A$, $V_{CE} = 1V$
$\|(V_{BE1}-V_{BE2})\|/°C$	Base Emitter Voltage Differential Change with Temperature	5	15	μV/°C	$I_C = 10\mu A$, $V_{CE} = 1V$ T = −55°C to +125°C
$\|I_{B1}-I_{B2}\|$	Base Current Differential		.6	nA	$T_C = 10\mu A$, $V_{CE} = 1V$

NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10μAmps.

INTERSIL

IT124A

Super-Beta Dual Monolithic NPN Silicon Planar Transistors

FEATURES

- **Very High Gain — $h_{FE} \geq 1500$ @ 1 and 10μA**
- **Low Output Capacitance — $C_{obo} \leq 0.8$ pF**
- **Tight V_{BE} Matching — $|V_{BE1} - V_{BE2}|$ — 2 mV TYP.**
- **High f_T — 100 MHz**

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures
- Storage Temperature ..... −65°C to +200°C
- Operating Junction Temperature ..... +200°C
- Lead Temperature (soldering, 10 second time limit) ..... +260°C

Maximum Power Dissipation — ONE SIDE / BOTH SIDES
- Device Dissipation @ Free Air — 400 mW / 750 mW
- Linear Derating Factor ..... 2.3 mW/°C / 4.3 mW/°C

Maximum Voltage and Current for Each Transistor
- V_{CBO} Collector to Base Voltage 2V
- V_{CEO} Collector to Emitter Voltage 2V
- V_{EBO} Emitter to Base Voltage (Note 2) 7V
- V_{CCO} Collector to Collector Voltage 100V
- I_C Collector Current 10mA

PACKAGE DIMENSIONS

TO-78

NOTES:
All dimensions in inches
Leads are gold-plated KOVAR
Package weight is 1.08 grams

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN	MAX	UNITS	CONDITIONS
h_{FE}	DC Current Gain	1500			$I_C = 1\mu A$, $V_{CE} = 1V$
h_{FE}	DC Current Gain	1500			$I_C = 10\mu A$, $V_{CE} = 1V$
h_{FE}(−55°C)	DC Current Gain	600			$I_C = 10\mu A$, $V_{CE} = 1V$
V_{BE}(ON)	Emitter-Base "ON" Voltage		0.7	V	$I_C = 10\mu A$, $V_{CE} = 1V$
V_{CE}(SAT)	Collector Saturation Voltage		0.5	V	$I_C = 1mA$, $I_B = 0.1mA$
I_{CBO}	Collector Cutoff Current		100	pA	$I_E = 0$, $V_{CB} = 1V$
I_{CBO}(+150°C)	Collector Cutoff Current		100	nA	$I_E = 0$, $V_{CB} = 1V$
I_{EBO}	Emitter Cutoff Current		100	pA	$I_C = 0$, $V_{EB} = 5V$
C_{OBO}	Output Capacitance		0.8	pF	$I_E = 0$, $V_{CB} = 1V$
C_{TE}	Emitter Transition Capacitance		1.0	pF	$I_C = 0$, $V_{EB} = 0.5V$
C_{C1C2}	Collector to Collector Capacitance		0.8	pF	$V_{CC} = 0$
I_{C1C2}	Collector to Collector Leakage Current		1.0	nA	$V_{CC} = \pm 30V$
f_T	Current Gain Bandwidth Product	10		MHz	$I_C = 10\mu A$, $V_{CE} = 1V$
f_T	Current Gain Bandwidth Product	100		MHz	$I_C = 100\mu A$, $V_{CE} = 1V$
NF	Narrow Band Noise Figure		3	dB	$I_C = 10\mu A$, $V_{CE} = 3V$, f = 1 KHz, R_G = 10 Kohms, BW = 200 Hz
BV_{CBO}	Collector-Base Breakdown Voltage	2		V	$I_C = 10\mu A$, $I_E = 0$
BV_{EBO}	Emitter-Base Breakdown Voltage	7		V	$I_E = 10\mu A$, $I_C = 0$
V_{CEO}(SUST)	Collector-Emitter Sustaining Voltage	2		V	$I_C = 1mA$, $I_B = 0$

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	TYP	MAX	UNITS	CONDITIONS
$\|V_{BE1}-V_{BE2}\|$	Base Emitter Voltage Differential	2	3.2	mV	$I_C = 10\mu A$, $V_{CE} = 1V$
$\|(V_{BE1}-V_{BE2})\|$/°C	Base Emitter Voltage Differential Change with Temperature	5	15	μV/°C	$I_C = 10\mu A$, $V_{CE} = 1V$ T = −55°C to +125°C
$\|I_{B1}-I_{B2}\|$	Base Current Differential		.6	nA	$T_C = 10\mu A$, $V_{CE} = 1V$

NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10μAmps.

INTERSIL

IT124B

Super-Beta Dual Monolithic NPN Silicon Planar Transistors

FEATURES

- **Very High Gain — $h_{FE} \geq 4000$ @ 1 and 10μA**
- **Low Output Capacitance — $C_{obo} \leq 0.8$ pF**
- **Tight V_{BE} Matching — $|V_{BE1} - V_{BE2}|$ — 2 mV TYP.**
- **High f_T — 100 MHz**

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	−65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (soldering, 10 second time limit)	+260°C

Maximum Power Dissipation	ONE SIDE	BOTH SIDES
Device Dissipation @ Free Air	400 mW	750 mW
Linear Derating Factor	2.3 mW/°C	4.3 mW/°C

Maximum Voltage and Current for Each Transistor

V_{CBO}	Collector to Base Voltage	2V
V_{CEO}	Collector to Emitter Voltage	2V
V_{EBO}	Emitter to Base Voltage (Note 2)	7V
V_{CCO}	Collector to Collector Voltage	100V
I_C	Collector Current	10mA

PACKAGE DIMENSIONS

TO-78

NOTES:
All dimensions in inches
Leads are gold-plated KOVAR
Package weight is 1.08 grams

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN	MAX	UNITS	CONDITIONS
h_{FE}	DC Current Gain	4000			$I_C = 1\mu A$, $V_{CE} = 1V$
h_{FE}	DC Current Gain	4000			$I_C = 10\mu A$, $V_{CE} = 1V$
$h_{FE}(-55°C)$	DC Current Gain	600			$I_C = 10\mu A$, $V_{CE} = 1V$
$V_{BE}(ON)$	Emitter-Base "ON" Voltage		0.7	V	$I_C = 10\mu A$, $V_{CE} = 1V$
$V_{CE}(SAT)$	Collector Saturation Voltage		0.5	V	$I_C = 1mA$, $I_B = 0.1mA$
I_{CBO}	Collector Cutoff Current		100	pA	$I_E = 0$, $V_{CB} = 1V$
$I_{CBO}(+150°C)$	Collector Cutoff Current		100	nA	$I_E = 0$, $V_{CB} = 1V$
I_{EBO}	Emitter Cutoff Current		100	pA	$I_C = 0$, $V_{EB} = 5V$
C_{OBO}	Output Capacitance		0.8	pF	$I_E = 0$, $V_{CB} = 1V$
C_{TE}	Emitter Transition Capacitance		1.0	pF	$I_C = 0$, $V_{EB} = 0.5V$
C_{C1C2}	Collector to Collector Capacitance		0.8	pF	$V_{CC} = 0$
I_{C1C2}	Collector to Collector Leakage Current		250	pA	$V_{CC} = \pm 50V$
f_T	Current Gain Bandwidth Product	10		MHz	$I_C = 10\mu A$, $V_{CE} = 1V$
f_T	Current Gain Bandwidth Product	100		MHz	$I_C = 100\mu A$, $V_{CE} = 1V$
NF	Narrow Band Noise Figure		3	dB	$I_C = 10\mu A$, $V_{CE} = 3V$, f = 1 KHz, $R_G = 10$ Kohms, BW = 200 Hz
BV_{CBO}	Collector-Base Breakdown Voltage	2		V	$I_C = 10\mu A$, $I_E = 0$
BV_{EBO}	Emitter-Base Breakdown Voltage	7		V	$I_E = 10\mu A$, $I_C = 0$
$V_{CEO}(SUST)$	Collector-Emitter Sustaining Voltage	2		V	$I_C = 1mA$, $I_B = 0$

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	TYP	MAX	UNITS	CONDITIONS
$\|V_{BE1}-V_{BE2}\|$	Base Emitter Voltage Differential	2	5	mV	$I_C = 10\mu A$, $V_{CE} = 1V$
$\|(V_{BE1}-V_{BE2})\|/°C$	Base Emitter Voltage Differential Change with Temperature	5	15	μV/°C	$I_C = 10\mu A$, $V_{CE} = 1V$, T = −55°C to +125°C
$\|I_{B1}-I_{B2}\|$	Base Current Differential		6	nA	$T_C = 10\mu A$, $V_{CE} = 1V$

NOTES:

1. These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10μAmps.

INTERSIL

IT125

Super-Beta Dual Monolithic NPN Silicon Planar Transistors

FEATURES

- **Very High Gain — $h_{FE} \geq 1000$ @ 1 and 10μA**
- **Low Output Capacitance — $C_{obo} \leq 0.8$ pF**
- **Tight V_{BE} Matching — $|V_{BE1} - V_{BE2}|$ — 2 mV TYP.**
- **High f_T — 100 MHz**

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures
- Storage Temperature ..... −65°C to +200°C
- Operating Junction Temperature ..... +200°C
- Lead Temperature (soldering, 10 second time limit) ..... +260°C

Maximum Power Dissipation — ONE SIDE / BOTH SIDES
- Device Dissipation @ Free Air — 400 mW / 750 mW
- Linear Derating Factor ..... 2.3 mW/°C / 4.3 mW/°C

Maximum Voltage and Current for Each Transistor
- V_{CBO} Collector to Base Voltage 2V
- V_{CEO} Collector to Emitter Voltage 2V
- V_{EBO} Emitter to Base Voltage (Note 2) 7V
- V_{CCO} Collector to Collector Voltage 100V
- I_C Collector Current 10mA

PACKAGE DIMENSIONS

TO-78

NOTES:
All dimensions in inches
Leads are gold-plated KOVAR
Package weight is 1.08 grams

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	MIN	MAX	UNITS	CONDITIONS
h_{FE}	DC Current Gain	1000			$I_C = 1\mu A$, $V_{CE} = 1V$
h_{FE}	DC Current Gain	1000			$I_C = 10\mu A$, $V_{CE} = 1V$
$V_{BE}(ON)$	Emitter-Base "ON" Voltage		0.7	V	$I_C = 10\mu A$, $V_{CE} = 1V$
$V_{CE}(SAT)$	Collector Saturation Voltage		0.5	V	$I_C = 1mA$, $I_B = 0.1mA$
I_{CBO}	Collector Cutoff Current		100	pA	$I_E = 0$, $V_{CB} = 1V$
$I_{CBO}(+150°C)$	Collector Cutoff Current		100	nA	$I_E = 0$, $V_{CB} = 1V$
I_{EBO}	Emitter Cutoff Current		100	pA	$I_C = 0$, $V_{EB} = 5V$
C_{OBO}	Output Capacitance		0.8	pF	$I_E = 0$, $V_{CB} = 1V$
C_{TE}	Emitter Transition Capacitance		1.0	pF	$I_C = 0$, $V_{EB} = 0.5V$
C_{C1C2}	Collector to Collector Capacitance		0.8	pF	$V_{CC} = 0$
I_{C1C2}	Collector to Collector Leakage Current		250	pA	$V_{CC} = \pm 50V$
f_T	Current Gain Bandwidth Product	10		MHz	$I_C = 10\mu A$, $V_{CE} = 1V$
f_T	Current Gain Bandwidth Product	100		MHz	$I_C = 100\mu A$, $V_{CE} = 1V$
NF	Narrow Band Noise Figure		3	dB	$I_C = 10\mu A$, $V_{CE} = 3V$, f = 1 KHz, $R_G = 10$ Kohms, BW = 200 Hz
BV_{CBO}	Collector-Base Breakdown Voltage	2		V	$I_C = 10\mu A$, $I_E = 0$
BV_{EBO}	Emitter-Base Breakdown Voltage	7		V	$I_E = 10\mu A$, $I_C = 0$
$V_{CEO}(SUST)$	Collector-Emitter Sustaining Voltage	2		V	$I_C = 1mA$, $I_B = 0$

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

SYMBOL	CHARACTERISTICS	TYP	MAX	UNITS	CONDITIONS
$\lvert I_{B1}-I_{B2}\rvert$	Base Current Differential		.6	nA	$T_C = 10\mu A$, $V_{CE} = 1V$

INTERSIL

IT126, IT127, IT128, IT129
Dual Monolithic NPN Silicon Planar Transistors

FEATURES

- High Gain at Low Current – $h_{FE} \geqslant 230$ at 10 mA –5V
- Low Output Capacitance – $C_{obo} \leqslant 3$ pF
- Tight I_B Match – $I_{B1-2} < .25\ \mu A$ at 1 mA –5V
- Tight V_{BE} Tracking – $\Delta(V_{BE1} - V_{BE2}) \leqslant 3\ \mu V/°C$ –55°C to +125°C
- Dielectrically isolated matched pairs for differential amplifiers.

ORDERING INFORMATION

TO78	TO71	WAFER	CHIP
IT126	IT126-TO71	IT126/W	IT126/D
IT127	IT127-TO71	IT127/W	IT127/D
IT128	IT128-TO71	IT128/W	IT128/D
IT129	IT129-TO71	IT128/W	IT128/D

GENERAL DESCRIPTION

Dual monolithic NPN Silicon planar transistors used for differential amplifier applications.

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	–65°C to +200°C
Operating Junction Temperature	+200°C

	TO71		TO78	
Maximum Power Dissipation	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Total Dissipation at 25°C Case Temperature	0.3 Watt	0.5 Watt	0.4 Watt	0.75 Watt
Derating Factor	1.7 mW/°C	2.9 mW/°C	2.3 mW/°C	4.3 mW/°C

Maximum Voltage and Current for Each Transistor		IT126,7	IT128	IT129
V_{CBO}	Collector to Base Voltage	60V	55V	45V
V_{CEO}	Collector to Emitter Voltage	60V	55V	45V
V_{EBO}	Emitter to Base Voltage (Note 2)	7V	7V	7V
V_{CCO}	Collector to Collector Voltage	70V	70V	70V
I_C	Collector Current	100 mA	100 mA	100 mA

PACKAGE DIMENSIONS

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER		IT126		IT127		IT128		IT129		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	150		150		100		70			$I_C = 10\ \mu A$, $V_{CE} = 5V$
h_{FE}	DC Current Gain	200	800	200	800	150	800	100			$I_C = 1.0$ mA, $V_{CE} = 5V$
h_{FE}	DC Current Gain	230		230		170		115			$I_C = 10$ mA, $V_{CE} = 5V$
h_{FE}	DC Current Gain	100		100		75		50			$I_C = 50$ mA, $V_{CE} = 5V$
$h_{FE}(-55°C)$	DC Current Gain	75		75		60		40			$I_C = 1$ mA, $V_{CE} = 5V$
$V_{BE(on)}$	Emitter-Base On Voltage		.9		.9		.9		.9	V	$I_C = 10$ mA, $V_{CE} = 5V$
			1.0		1.0		1.0		1.0	V	$I_C = 50$ mA, $V_{CE} = 5V$
$V_{CE(sat)}$	Collector Saturation Voltage		.3		.3		.3		.3	V	$I_C = 10$ mA, $I_B = 1$ mA
			.6		.6		.6		.6	V	$I_C = 50$ mA, $I_B = 5$ mA
I_{CBO}	Collector Cutoff Current		0.1		0.1		0.1		0.1*	nA	$I_E = 0$, $V_{CB} = 45V, 30V$*
$I_{CBO}(+150°C)$	Collector Cutoff Current		0.1		0.1		0.1		0.1*	μA	$I_E = 0$, $V_{CB} = 45V, 30V$*
I_{EBO}	Emitter Cutoff Current		0.1		0.1		0.1		0.1	nA	$I_C = 0$, $V_{EB} = 5V$
C_{obo}	Output Capacitance		3		3		3		3	pF	$I_E = 0$, $V_{CB} = 20V$

INTERSIL

LM194, LM394
Monolithic NPN Transistor Pairs

FEATURES

- Emitter-base voltage matched to 50μV
- Offset voltage drift less than 0.1μV/°C
- Current gain (h_{FE}) matched to 2%
- Common-mode rejection ratio greater than 120dB
- Parameters guaranteed over 1μA to 1mA collector current
- Extremely low noise
- Superior logging characteristics compared to conventional pairs
- Plug-in replacement for presently available devices

1

CONNECTION DIAGRAM

METAL CAN PACKAGE

GENERAL DESCRIPTION

The LM194 and LM394 are junction isolated ultra well-matched monolithic NPN transistor pairs with an order of magnitude improvement in matching over conventional transistor pairs. This is accomplished by advanced linear processing and a unique new device structure.

Electrical characteristics of these devices such as drift versus initial offset voltage, noise, and the exponential relationship of base-emitter voltage to collector current closely approach those of a theoretical transistor. Extrinsic emitter and base resistances are much lower than presently available pairs, either monolithic or discrete, giving extremely low noise and theoretical operation over a wide current range. Most parameters are guaranteed over a current range of 1μA to 1mA and 0 to 40V collector-base voltage, ensuring superior performance in nearly all applications.

To guarantee long-term stability of matching parameters, internal clamp diodes have been added across the emitter-base junction of each transistor. These prevent degradation due to reverse biased emitter current — the most common cause of field failures in matched devices. The parasitic isolation junction formed by the diodes also clamps the substrate region to the most negative emitter to ensure complete isolation between devices.

The LM194 and LM394 will provide a considerable improvement in performance in most applications requiring a closely matched transistor pair. In many cases, trimming can be eliminated entirely, improving reliability and decreasing costs. Additionally, the low noise and high gain make this device attractive even where matching is not critical.

The LM194 and LM394 are available in an isolated header 6-lead TO-5. The LM194 is identical to the LM394 except for tighter electrical specifications and wider temperature range.

ABSOLUTE MAXIMUM RATINGS

Collector Current	20mA
Collector-Emitter Voltage	40V
Collector-Base Voltage	40V
Collector-Substrate Voltage	40V
Collector-Collector Voltage	40V
Base-Emitter Current	±10mA
Power Dissipation	500mW
Junction Temperature	
LM194	−55°C to +135°C
LM394	−25°C to +85°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C

ELECTRICAL CHARACTERISTICS (T_J = +25°C)

PARAMETER	CONDITIONS	LM194 MIN	LM194 TYP	LM194 MAX	LM394 MIN	LM394 TYP	LM394 MAX	UNITS
Current Gain (h_{FE})(Note 1)	V_{CB} = 0V to 40V							
	I_C = 1mA	500	700		300	700		
	I_C = 100μA	400	550		250	550		
	I_C = 10μA	300	450		200	450		
	I_C = 1μA	200	300		150	300		
Current Gain Match (h_{FE} Match)	V_{CB} = 0V to 40V							
	I_C = 10μA to 1mA		0.5	2		0.5	4	%
	I_C = 1μA		1.0			1.0		%
Emitter-Base Offset Voltage	V_{CB} = 0, I_C = 1μA to 1mA		25	50		25	150	μV
Change in Emitter-Base Offset	(Note 1)		10	24		10	50	μV
Voltage vs. Collector-Base Voltage (CMRR)	I_C = 1μA to 1mA, V_{CB} = 0V to 40V							
Change in Emitter-Base Offset Voltage vs. Collector Current	V_{CB} = 0V, I_C = 1μA to 0.3mA		5	25		5	50	μV
Emitter-Base Offset Voltage Temperature Drift (Note 2)	I_C = 10μA to 1mA							
	I_{C1} = I_{C2}		0.08	0.3		0.08	0.8	μV/°C
	V_{OS} trimmed to 0 at +25°C		0.03	0.1		0.03	0.3	μV/°C
Logging Conformity (Note 3)	I_C = 3nA to 300μA, V_{CB} = 0		150			150		μV
Collector-Base Leakage	V_{CB} = 40V		50			50		pA
Collector-Collector Leakage	V_{CC} = 40V		70			70		pA
Input Voltage Noise	I_C = 100μA, V_{CB} = 0V, f = 100Hz to 100kHz		1.8			1.8		nV/√Hz
Collector to Emitter Saturation Voltage	I_C = 1mA, I_B - 10μA		0.2			0.2		V
	I_C = 1mA, I_B = 100μA		0.1			0.1		V

Note 1: Collector base voltage is swept from 0 to 40V at a collector current of 1μA, 10μA, 100μA and 1mA.
Note 2: Offset voltage drift with V_{OS} = 0 at T_A = +25°C is valid only when the ratio of I_{C1} to I_{C2} is adjusted to give the initial zero offset. This ratio must be held to within 0.003% over the entire temperature range. Measurements taken at +25°C and temperature extremes.
Note 3: Logging conformity is measured by computing the best fit to a true exponential and expressing the error as a base-emitter voltage deviation.

TYPICAL APPLICATIONS

FAST, ACCURATE LOGGING AMPLIFIER, V_{IN} = 10V to 0.1mV or I_{IN} = 1mA to 10nA

INTERSIL

Monolithic Dual Matched PNP Silicon Planar Transistors - 2N3810, 2N3810A, 2N3811, 2N3811A

ABSOLUTE MAXIMUM RATINGS

Maximum Temperatures
- Storage Temperature ..... −65°C to +200°C
- Operating Temperature ..... 200°C
- Lead Temperature (10 seconds) ..... 230°C

Maximum Power Dissipation

Total Dissipation at	One Side	Both Sides
25°C Ambient Temperature	500 mW	600 mW
Linear Derating Factor	2.9 mW/°C	3.4 mW/°C

Maximum Voltage and Current (One side)
- V_{EBO} Emitter to Base Voltage ..... −5.0V
- V_{CBO} Collector to Base Voltage ..... −60V
- V_{CEO} Collector to Emitter Voltage ..... −60V
- I_C DC Collector Current ..... 50 mA

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: 25°C Ambient Temperature unless otherwise noted

SYMBOL	CHARACTERISTIC	2N3810 MIN.	2N3810 MAX.	2N3811 MIN.	2N3811 MAX.	UNITS	TEST CONDITIONS
I_{CBO}	Collector Cutoff Current		10		10	nA	V_{CB} = −50V, I_C = 0
			10		10	μA	V_{CB} = −50V, I_E = 0, T_A = 150°C
I_{EBO}	Emitter Cutoff Current		20		20	nA	V_{EB} = −4.0V
BV_{EBO}	Emitter to Base Breakdown Voltage	−5.0		−5.0		V	I_C = 0, I_E = 10μA
BV_{CBO}	Collector to Base Breakdown Voltage	−60		−60		V	I_E = 0, I_C = 10μA
BV_{CEO}	Collector to Emitter Breakdown Voltage	−60		−60		V	I_C = 10 mA
h_{FE}	DC Current Gain	100		225			I_C = 10 μA, V_{CE} = −5.0V
		150	450	300	900		I_C = 100μA, V_{CE} = −5.0V
		150	450	300	900		I_C = 500μA, V_{CE} = −5.0V
		150	450	300	900		I_C = 1.0 mA, V_{CE} = −5.0V
		125		250			I_C = 10 mA, V_{CE} = −5.0V
		75		150			I_C = 100μA, V_{CE} = −5.0V, T_A = −55°C
$V_{BE(ON)}$	Base to Emitter "On" Voltage		−0.7		−0.7	V	I_C = 100μA, V_{CE} = −5.0V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage		−0.2		−0.2	V	I_C = 100μA, I_B = 10μA
			−0.25		−0.25	V	I_C = 1.0 mA, I_B = 100μA
$V_{BE(sat)}$	Base to Emitter Saturation Voltage		−0.7		−0.7	V	I_C = 100μA, I_B = 10μA
			−0.8		−0.8	V	I_C = 1.0 mA, I_B = 100μA
$\frac{h_{FE1}}{h_{FE2}}$	DC Current Gain Ratio	0.9	1.0	0.9	1.0		V_{CE} = −5.0V, I_C = 0.1 mA
$\lvert V_{BE1}-V_{BE2}\rvert$	Base to Emitter Voltage Differential		−5.0		−5.0	mV	V_{CE} = −5.0V, I_C = 10μA to 10 mA
			−3.0		−3.0	mV	V_{CE} = −5.0V, I_C = 100μA
$\lvert\Delta(V_{BE1}-V_{BE2})\rvert$	Base to Emitter Voltage Differential Gradient		−1.0		−1.0	mV	V_{CE} = −5.0V, I_C = 0.1 mA
							T_A = 25°C to 125°C
			−0.8		−0.8	mV	V_{CE} = −5.0V, I_C = 0.1 mA
							T_A = −55°C to +25°C
C_{ob}	Output Capacitance		4.0		4.0	pF	V_{CB} = −5.0V, I_E = 0, f = 100 kHz
C_{ib}	Input Capacitance		8.0		8.0	pF	V_{EB} = 0.5V, I_C = 0, f = 100 kHz
$\lvert h_{fe}\rvert$	Magnitude of Common Emitter Small Signal Current Gain	1.0		1.0			I_C = 500μA, V_{CE} = −5.0V, f = 30 MHz
		1.0	5.0	1.0	5.0		I_C = 1.0 mA, V_{CE} = −5.0V, f = 100 MHz
h_{ie}	Input Impedance	3.0	30	10	40	kΩ	V_{CE} = −10V, I_C = 1.0 mA, f = 1.0 kHz
h_{re}	Reverse Voltage Feedback Ratio		25		25	x 10−4	V_{CE} = −10V, I_C = 1.0 mA, f = 1.0 kHz
h_{oe}	Output Conductance	5.0	60	5.0	60	μmho	V_{CE} = −10V, I_C = 1.0 mA, f = 1.0 kHz
h_{fe}	Small Signal Current Gain	150	600	300	900		V_{CE} = −10V, I_C = 1.0 mA, f = 1.0 kHz
$RE(h_{ie})$	Real Part of Common Emitter Small Signal Input Impedance	3.0	30	10	40	kΩ	V_{CE} = −10V, I_C = 1.0 mA, f = 1.0 kHz
NF	Noise Figure		3.0		1.5	dB	I_C = 100μA, V_{CE} = −10V, f = 1.0 kHz, PBW = 200 Hz, R_G = 3.0 kΩ
			2.5		1.5	dB	I_C = 100μA, V_{CE} = −10V, f = 10 kHz, PBW = 2.0 kHz, R_G = 3.0 kΩ
			7.0		4.0	dB	I_C = 100μA, V_{CE} = − 10V, f = 100 Hz, PBW = 20 Hz, R_G = 3.0 kΩ
			3.5		2.5	dB	I_C = 100μA, V_{CE} = −10V, R_G = 3.0 kΩ 3.0 dB down at 10 Hz and 10 kHz PBW = 15.7 kHz

INTERSIL

PACKAGE DIMENSIONS

TO-78

PIN	OUT
1	C_1
2	B_1
3	E_1
4	E_2
5	B_2
7	C_2

ELECTRICAL CONDITIONS

TEST CONDITIONS: 25°C Ambient Temperature unless otherwise noted

SYMBOL	CHARACTERISTIC	2N3810A MIN.	2N3810A MAX.	2N3811A MIN.	2N3811A MAX.	UNITS	TEST CONDITIONS
I_{CBO}	Collector Cutoff Current		10		10	nA	V_{CB} = −50V, I_C = 0
			10		10	μA	V_{CB} = −50V, I_E = 0, T_A = 150°C
I_{EBO}	Emitter Cutoff Current		20		20	nA	V_{EB} = −4.0V
BV_{EBO}	Emitter to Base Breakdown Voltage	−5.0		−5.0		V	I_C = 0, I_E = 10μA
BV_{CBO}	Collector to Base Breakdown Voltage	−60		−60		V	I_E = 0, I_C = 10μA
BV_{CEO}	Collector to Emitter Breakdown Voltage	−60		−60		V	I_C = 10 mA
h_{FE}	DC Current Gain	100		225			I_C = 10μA, V_{CE} = −5.0V
		150	450	300	900		I_C = 100μA, V_{CE} = −5.0V
		150	450	300	900		I_C = 500μA, V_{CE} = −5.0V
		150	450	300	900		I_C = 1.0 mA, V_{CE} = −5.0V
		125		250			I_C = 10 mA, V_{CE} = −5.0V
		75		150			I_C = 100μA, V_{CE} = −5.0V, T_A = −55°C
$V_{BE(ON)}$	Base to Emitter "On" Voltage		−0.7		−0.7	V	I_C = 100μA, V_{CE} = −5.0V
$V_{CE(sat)}$	Collector to Emitter Saturation Voltage		−0.2		−0.2	V	I_C = 100μA, I_B = 10μA
			−0.25		−0.25	V	I_C = 1.0 mA, I_B = 100μA
$V_{BE(sat)}$	Base to Emitter Saturation Voltage		−0.7		−0.7	V	I_C = 100μA, I_B = 10 μA
			−0.8		−0.8	V	I_C = 1.0 mA, I_B = 100μA
h_{FE1} / h_{FE2}	DC Current Gain Ratio	0.95	1.0	0.95	1.0		V_{CE} = −5.0V, I_C = 0.1 mA
		0.85	1.0	0.85	1.0		V_{CE} = −5.0V, I_C = 0.1 mA,
							T_A = −55°C to +125°C
$\|V_{BE1}-V_{BE2}\|$	Base to Emitter Voltage Differential		−5.0		−5.0	mV	V_{CE} = −5.0V, I_C = 10μA to 10 mA
			−1.5		−1.5	mV	V_{CE} = −5.0V, I_C = 100μA
$\|\Delta(V_{BE1}-V_{BE2})\|$	Base to Emitter Voltage Differential Gradient		−0.5		−0.5	mV	V_{CE} = −5.0V, I_C = 0.1 mA
							T_A = 25°C to 125°C
			−0.4		−0.4	mV	V_{CE} = −5.0V, I_C = 0.1 mA
							T_A = −55°C to +25°C
C_{ob}	Output Capacitance		4.0		4.0	pF	V_{CB} = −5.0V, I_E = 0, f = 100 kHz
C_{ib}	Input Capacitance		8.0		8.0	pF	V_{EB} = 0.5V, I_C = 0, f = 100 kHz
$\|h_{fe}\|$	Magnitude of Common Emitter Small Signal Current Gain	1.0		1.0			I_C = 500μA, V_{CE} = −5.0V, f = 30 mHz
		1.0	5.0	1.0	5.0		I_C = 1.0 mA, V_{CE} = 5.0V, f = 100 MHz
h_{ie}	Input Impedance	3.0	30	10	40	kΩ	V_{CE} = −10V, I_C = 1.0 mA, f = 1.0 kHz
h_{re}	Reverse Voltage Feedback Ratio		25		25	x 10^{-4}	V_{CE} = −10V, I_C = 1.0 mA, f = 1.0 kHz
h_{oe}	Output Conductance	5.0	60	5.0	60	μmho	V_{CE} = −10V, I_C = 1.0 mA, f = 1.0 kHz
h_{fe}	Small Signal Current Gain	150	600	300	900		V_{CE} = −10V, I_C = 1.0 mA, f = 1.0 kHz
$RE(h_{ie})$	Real Part of Common Emitter Small Signal Input Impedance	3.0	30	10	40	kΩ	V_{CE} = −10V, I_C = 1.0 mA, f = 1.0 kHz
NF	Noise Figure		3.0		1.5	dB	I_C = 100μA, V_{CE} = −10V, f = 1.0 kHz, PBW = 200 Hz, R_G = 3.0 kΩ
			2.5		1.5	dB	I_C = 10μA, V_{CE} = −10V, f = 10 kHz, PBW = 2.0 kHz, R_G = 3.0 kΩ
			7.0		4.0	dB	I_C = 100μA, V_{CE} = −10V, f = 100 Hz, PBW = 20 Hz, R_G = 3.0 kΩ
			3.5		2.5	dB	I_C = 100μA, V_{CE} = −10V, R_G = 3.0 kΩ, 3 dB down at 10 Hz and 10 kHz PBW = 15.7 kHz

1

INTERSIL

2N5117 2N5118 2N5119
Dual Monolithic Matched PNP Silicon Planar Transistors

GENERAL DESCRIPTION

Dielectrically isolated matched pairs for differential amplifiers.

ORDERING INFORMATION

TO78	WAFER	CHIP
2N5117	2N5117/W	2N5117/D
2N5118	2N5118/W	2N5118/D
2N5119	2N5119/W	2N5119/D

MAXIMUM RATINGS (25°C unless otherwise noted) (Note 1)

CHARACTERISTICS	SYMBOL	2N5117 2N5118 2N5119	UNITS
Dissipation at 25°C Case Temperature			
Each side (Note 1)	P_D	0.4	Watt
Both sides	P_D	0.75	Watt
Derating Factor			
Each side		2.3	mW/°C
Both sides		4.3	mW/°C
Voltage			
Collector to Base	V_{CBO}	45	Volts
Collector to Emitter	V_{CEO}	45	Volts
Emitter to Base (Note 2)	V_{EBO}	7.0	Volts
Collector to Collector	V_{CCO}	100	Volts
Collector Current	I_C	10	mA
Storage Temperature	T_S	-65 to +200	°C
Lead Temperature for 10 Seconds		+300	°C

PACKAGE DIMENSIONS

PIN	OUT
1	C_1
2	B_1
3	E_1
5	E_2
6	B_2
7	C_2

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5117 2N5118 MIN	2N5117 2N5118 MAX	2N5119 MIN	2N5119 MAX	UNIT	TEST CONDITIONS	
h_{FE}	DC Current Gain	100	300	50			I_C = 10 μA, V_{CE} = 5.0 V	
h_{FE}	DC Current Gain	100		50			I_C = 500 μA, V_{CE} = 5.0 V	
h_{FE}	DC Current Gain (-55°C)	30		20			I_C = 10 μA, V_{CE} = 5.0 V	
I_{CBO}	Collector Cutoff Current		0.1		0.1	nA	I_E = 0, V_{CB} = 30 V	
I_{CBO}	Collector Cutoff Current (150°C)		0.1		0.1	μA	I_E = 0, V_{CB} = 30 V	
I_{EBO}	Emitter Cutoff Current		0.1		0.1	nA	I_C = 0, V_{EB} = 5.0 V	
$I_{C1, C2}$	Collector-Collector Leakage		5.0		5.0	pA	V_{CC} = 100 V	
f_T	Current Gain Bandwith Product	100		100		MHz	I_C = 500 μA, V_{CE} = 10 V	
C_{ob}	Output Capacitance		0.8		0.8	pF	I_E = 0, V_{CB} = 5.0 V	
C_{TE}	Emitter Transition Capacitance		1.0		1.0	pF	I_C = 0, V_{EB} = 0.5 V	
$C_{C1, C2}$	Collector-Collector Capacitance		0.8		0.8	pF	V_{CC} = 0	
$V_{CEO(sust)}$	Collector-Emitter Sustaining Voltage	45		45		V	I_C = 1.0 mA, I_B = 0	
NF	Narrow Band Noise Figure		4.0		4.0	dB	I_C = 10 μA, V_{CE} = 5.0 V BW = 200 cps	f = 1 KHz, R_G = 10 KΩ
$V_{(BR)CBO}$	Collector Base Breakdown Voltage	45		45		V	I_C = 10 μA, I_E = 0	
$V_{(BR)EBO}$	Emitter Base Breakdown Voltage	7.0		7.0		V	I_E = 10 μA, I_C = 0	

MATCHING CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		2N5117 MIN	2N5117 MAX	2N5118 MIN	2N5118 MAX	2N5119 MIN	2N5119 MAX	UNIT	TEST CONDITIONS	
h_{FE_1}/h_{FE_2}	DC Current Gain Ratio (Note 3)	0.9	1.0	0.85	1.0	0.8	1.0		I_C = 10 μA to 500 μA, V_{CE} = 5 V I_C = 10 μA, V_{CE} = 5.0 V	
$V_{BE_1}-V_{BE_2}$	Base-Emitter Voltage Differential		3.0		5.0		5.0	mV	I_C = 10 μA to 500 μA, V_{CE} = 5 V I_C = 10 μA, V_{CE} = 5.0 V	
$I_{B_1}-I_{B_2}$	Base Current Differential		10.0		15		40	nA	I_C = 10 μA, V_{CE} = 5.0 V	
$\Delta(V_{BE_1}-V_{BE_2})$	Base Voltage Differential Change with Temperature		3.0		5.0		10	μV/°C	I_C = 10 μA, V_{CE} = 5.0 V	T_A = -55°C to +125°C
$\Delta(I_{B_1}-I_{B_2})$	Base-Current Differential Change with Temperature		0.3		0.5		1.0	nA/°C	I_C = 10 μA, V_{CE} = 5.0 V	T_A = -55°C to +125°C

1. Maximum ratings are limiting values above which devices may be damaged. These ratings give a maximum junction temperature of 200 C.
2. The reverse base-to-emitter voltage must never exceed 7.0 volts and the reverse base-to-emitter current must never exceed 10 μA.
3. Lower of two h_{FE} readings is defined as h_{FE_1}.

INTERSIL

IT130/A, IT131, IT132
Dual Monolithic Matched PNP Silicon Planar Transistors

FEATURES

- High h_{FE} at Low Current >200 @ 10 μA
- Low Output Capacitance <2.0 pf
- $I_{B_1} - I_{B_2}$ <2.5 nA
- Tight V_{BE} Tracking $<3.0\ \mu V/^\circ C$

GENERAL DESCRIPTION

Matched pairs for differential amplifiers.

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	-65°C to +200°C
Operating Junction Temperature	+200°C

Maximum Power Dissipation

	TO-78		TO-71	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Total Dissipation at 25°C Case Temperature	0.4 Watt	0.75 Watt	0.3 Watt	0.5 Watt
Derating Factor	2.3mW/°C	4.3mW/°C	1.7mW/°C	2.9mW/°C

Maximum Voltage & Current for Each Transistor

V_{CBO}	Collector to Base Voltage	45 V
V_{CEO}	Collector to Emitter Voltage	45 V
V_{EBO}	Emitter to Base Voltage	7.0 V
V_{CCO}	Collector to Collector Voltage	60 V
I_C	Collector Current	50 mA

ORDERING INFORMATION

TO78	TO71	WAFER	CHIP
IT130A	IT130A-TO71	IT130A/W	IT130A/D
IT130	IT130-TO71	IT130/W	IT130/D
IT131	IT131-TO71	IT131/W	IT131/D
IT132	IT132-TO71	IT132/W	IT132/D

PACKAGE DIMENSIONS

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

PARAMETER		IT130A		IT130		IT131		IT132		UNIT	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	200		200		80		80			$I_C = 10\ \mu A$, $V_{CE} = 5.0$ V
h_{FE}	DC Current Gain	225		225		100		100			$I_C = 1.0$ mA, $V_{CE} = 5.0$ V
$h_{FE}(-55^\circ C)$	DC Current Gain	75		75		30		30			$I_C = 10\ \mu A$, $V_{CE} = 5.0$ V
$V_{BE}(ON)$	Emitter-Base On Voltage		0.7		0.7		0.7		0.7	V	$I_C = 10\ \mu A$, $V_{CE} = 5.0$ V
$V_{CE}(SAT)$	Collector Saturation Voltage		0.5		0.5		0.5		0.5	V	$I_C = 0.5$ mA, $I_B = 0.05$ mA
I_{CBO}	Collector Cutoff Current		-1.0		-1.0		-1.0		-1.0	nA	$I_E = 0$, $V_{CB} = 45$ V
$I_{CBO}(+150^\circ C)$	Collector Cutoff Current		-10		-10		-10		-10	μA	$I_E = 0$, $V_{CB} = 45$ V
I_{EBO}	Emitter Cutoff Current		-1.0		-1.0		-1.0		-1.0	nA	$I_C = 0$, $V_{EB} = 5.0$ V
C_{OB}	Output Capacitance		2.0		2.0		2.0		2.0	pF	$I_E = 0$, $V_{CB} = 5.0$ V
C_{TE}	Emitter Transition Capacitance		2.5		2.5		2.5		2.5	pF	$I_C = 0$, $V_{EB} = 0.5$ V
C_{C_1, C_2}	Collector to Collector Capacitance		4.0		4.0		4.0		4.0	pF	$V_{CC} = 0$
I_{C_1, C_2}	Collector to Collector Leakage Current		10		10		10		10	nA	$V_{CC} = \pm 60$ V
$V_{CEO}(SUST)$	Collector to Emitter Sustaining Voltage	-45		-45		-45		-45		V	$I_C = 1.0$ mA, $I_B = 0$
f_T	Current Gain	5		5		4		4		MHz	$I_C = 10\ \mu A$, $V_{CE} = 5$ V
	Bandwidth Product	110		110		90		90		MHz	$I_C = 1$ mA, $V_{CE} = 5$ V
$\lvert V_{BE_1} - V_{BE_2} \rvert$	Base Emitter Voltage Differential		1		2		3		5	mV	$I_C = 10\ \mu A$, $V_{CE} = 5.0$ V
$\lvert I_{B_1} - I_{B_2} \rvert$	Base Current Differential		2.5		5		25		25	nA	$I_C = 10\ \mu A$, $V_{CE} = 5.0$ V
$\lvert \Delta(V_{BE_1} - V_{BE_2}) \rvert$	Base-Emitter Voltage Differential Change with Temperature		3		5		10		20	$\mu V/^\circ C$	$T_A = -55^\circ C$ to $+125^\circ C$, $I_C = 10\ \mu A$, $V_{CE} = 5.0$ V

NOTES: (1) These ratings are limiting values above which the serviceability of any semiconductor device may be impaired.
(2) The lowest of two h_{FE} readings is taken as h_{FE_1} for purposes of this ratio.

INTERSIL

IT136, IT137
IT138, IT139

Dual Monolithic PNP Silicon Planar Transistors

FEATURES

- High Gain at Low Current – $h_{FE} \geq 200$ @ 1mA
- Low Output Capacitance – $C_{obo} < 3$ pf
- Tight I_B Match – $I_{B_{1-2}} < .25\ \mu A$ @ 1 mA – 5V
- Tight V_{BE} Tracking – $\Delta(V_{BE_1} - V_{BE_2}) \leq 3\ \mu V/°C$ –55°C to + 125°C
- Dielectrically isolated matched pairs for differential amplifiers.

GENERAL DESCRIPTION

Dual monolithic PNP silicon planar transistors used for differential amplifier applications.

1

ABSOLUTE MAXIMUM RATINGS (Note 1)

@ 25°C (unless otherwise noted)

Maximum Temperatures

Storage Temperature	–65°C to +200°C
Operating Junction Temperature	+200°C

Maximum Power Dissipation

	TO71		TO78	
	ONE SIDE	BOTH SIDES	ONE SIDE	BOTH SIDES
Total Dissipation @ 25°C Case Temperature	0.3 Watt	0.5 Watt	0.4 Watt	0.75 Watt
Derating Factor	1.7mW/°C	2.9mW/°C	2.3mW/°C	4.3mW/°C

Maximum Voltage and Current for Each Transistor

		IT136,7	IT138	IT139
V_{CBO}	Collector to Base Voltage	60V	55V	45V
V_{CEO}	Collector to Emitter Voltage	60V	55V	45V
V_{EBO}	Emitter to Base Voltage (Note 2)	7V	7V	7V
V_{CCO}	Collector to Collector Voltage	70V	70V	70V
I_C	Collector Current	100mA	100mA	100mA

ORDERING INFORMATION

TO78	TO71	WAFER	CHIP
IT136	IT136-TO71	IT136/W	IT136/D
IT137	IT137-TO71	IT137/W	IT137/D
IT138	IT138-TO71	IT138/W	IT138/D
IT139	IT139-TO71	IT139/W	IT139/D

PACKAGE DIMENSIONS

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER		IT136		IT137		IT138		IT139		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
h_{FE}	DC Current Gain	150		150		100		70			$I_C = 10\,\mu A$, $V_{CE} = 5V$
h_{FE}	DC Current Gain	150	800	150	800	100	800	70	800		$I_C = 1.0$ mA, $V_{CE} = 5V$
h_{FE}	DC Current Gain	125	230	125		80		50			$I_C = 10$ mA, $V_{CE} = 5V$
h_{FE}	DC Current Gain	65		60		40		25			$I_C = 50$ mA, $V_{CE} = 5V$
$h_{FE}(-55°C)$	DC Current Gain	75		75		60		40			$I_C = 1$ mA, $V_{CE} = 5V$
$V_{BE(on)}$	Emitter - Base On Voltage		.9		.9		.9		.9	V	$I_C = 10$ mA, $V_{CE} = 5V$
			1.0		1.0		1.0		1.0	V	$I_C = 50$ mA, $V_{CE} = 5V$
$V_{CE(sat)}$	Collector Saturation Voltage		.3		.3		.3		.3	V	$I_C = 1$ mA, $I_B = .1$ mA
			.6		.6		.6		.6	V	$I_C = 10$ mA, $I_B = 1$ mA
I_{CBO}	Collector Cutoff Current		0.1		0.1		0.1		0.1*	nA	$I_E = 0$, $V_{CB} = 45V, 30V$*
$I_{CBO}(+150°C)$	Collector Cutoff Current		0.1		0.1		0.1		0.1*	μA	$I_E = 0$, $V_{CB} = 45V, 30V$*
I_{EBO}	Emitter Cutoff Current		0.1		0.1		0.1		0.1	nA	$I_C = 0$, $V_{EB} = 5V$
C_{obo}	Output Capacitance		3		3		3		3	pF	$I_E = 0$, $V_{CB} = 20V$

ELECTRICAL CHARACTERISTICS @ 25°C (unless otherwise noted)

PARAMETERS		IT136		IT137		IT138		IT139		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$BV_{C_1C_2}$	Collector to Collector Breakdown Voltage	100		100		100		100		V	$I_C = \pm 1\,\mu A$
$V_{CEO(sust)}$	Collector to Emitter Sustaining Voltage	60		60		55		45		V	$I_C = 1$ mA, $I_B = 0$
BV_{CBO}	Collector Base Breakdown Voltage	60		60		55		45		V	$I_C = 10\,\mu A$, $I_E = 0$
BV_{EBO}	Emitter Base Breakdown Voltage	7		7		7		7		V	$I_E = 10\,\mu A$, $I_C = 0$

MATCHING CHARACTERISTICS @ 25°C (unless otherwise noted)

PARAMETERS		IT136		IT137		IT138		IT139		UNITS	CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
$\lvert V_{BE_1} - V_{BE_2}\rvert$	Base Emitter Voltage Differential		1		2		3		5	mV	$I_C = 1$ ma, $V_{CE} = 5V$
$\lvert\Delta(V_{BE_1} - V_{BE_2})\rvert/°C$	Base Emitter Voltage Differential Change with Temperature		3		5		10		20	$\mu V/°C$	$I_C = 1$ mA, $V_{CE} = 5V$ $T_A = -55°C$ to $+125°C$
$\lvert I_{B_1} - I_{B_2}\rvert$	Base Current Differential		2.5		5		10		20	nA	$I_C = 10\,\mu A$, $V_{CE} = 5V$
			.25		.5		1.0		2.0	μA	$I_C = 1$ mA, $V_{CE} = 5V$

INTERSIL

ID100, ID101
Low Leakage Monolithic Dual Diode

FEATURES

- I_R = 0.1 pA (typical)
- $BV_R > 30$ V
- C_{TR} = 0.75 pF (typical)

GENERAL DESCRIPTION

The ID100 and ID101 are monolithic dual diodes intended for use in applications requiring extremely low leakage currents. Applications include interstage coupling with reverse isolation, signal clipping and clamping and protection of ultra low leakage FET differential dual and operational amplifiers.

1

ABSOLUTE MAXIMUM RATINGS
(@ 25°C unless otherwise noted)

Maximum Temperatures	
Storage Temperature	-65°C to +200°C
Operating Junction Temperature	+200°C
Lead Temperature (soldering, 10 sec. time limit)	+300°C
Maximum Power Dissipation	
Device Dissipation @ Free Air Temperature	300 mW
Linear Derating	1.7 mW/°C
Maximum Voltages & Currents	
V_R Reverse Voltage	30 V
$V_{D_1D_2}$ Diode to Diode Voltage	±50 V
I_F Forward Current	20 mA
I_R Reverse Current	100 μA

ORDERING INFORMATION

TO78	TO71	WAFER	CHIP
ID100		ID100/W	ID101/D
	ID101		

PACKAGE DIMENSIONS

1. Cathode 1 5. Not Used*
2. Anode 1 6. Anode 2
3. Not Used* 7. Cathode 2

1. Cathode 1 5. Not Used*
2. Anode 1 6. Anode 2
3. Not Used* 7. Cathode 2

*These leads are not to be connected together nor connected to the circuit in any way.

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

PARAMETER		ID100, ID101 MIN.	TYP.	MAX.	UNITS	TEST CONDITIONS
V_F	Forward Voltage Drop	0.8		1.1	V	I_F = 10 mA
BV_R	Reverse Breakdown Voltage	30			V	I_R = 1 μA
I_R	Reverse Leakage Current		0.1		pA	V_R = 1 V, T_A = 25°C
			2.0	10	pA	V_R = 10 V, T_A = 25°C
				10	nA	V_R = 10 V, T_A = 125°C
$\lvert I_{R_1} - I_{R_2} \rvert$	Differential Leakage Current			3	pA	V_R = 10 V
C_{TR}	Total Reverse Capacitance		0.75	1	pF	V_R = 10 V, f = 1 MHz

TYPICAL CHARACTERISTICS OF ID100/ID101

INTERSIL

IT404
Log/Antilog Transistor Array

FEATURES

Excellent log conformance over 5 decadades, 100nA-1mA.

DESCRIPTION

Four closely matched NPN transistors for multipliers, dividers, and other non-linear applications.

ABSOLUTE MAXIMUM RATINGS
(T_A = +25°C unless otherwise noted)

Temperature
- Storage Temperature . . . . . -65°C to +200°C
- Operating Junction Temperature . . . . . +200°C

Power Dissipation
- Total Dissipation 0.6W
- Derating Factor . . . . . 3.4mW/°C

Voltage and Current
- V_{CBO} Collector to Base Voltage 20V
- V_{CEO} Collector to Emitter Voltage 20V
- V_{EBO} Emitter to Base Voltage 5.0V
- V_{CC} Collector to Collector Voltage 50V
- I_C Collector Current 20mA

ELECTRICAL CHARACTERISTICS (T_A = +25°C unless otherwise noted)

CHARACTERISTIC	TEST CONDITION	MIN	MAX	UNIT
h_{FE} DC Current Gain	I_C = 10μA, V_{CE} = 5.0V	100		
h_{FE} DC Current Gain	I_C = 1mA, V_{CE} = 5.0V	100		
I_{CBO} Collector Cutoff Current	V_{CB} = 10V		100	pA
I_{EBO} Emitter Cutoff Current	V_{EB} = 4V		100	pA
BV_{CBO} Collector Base Breakdown	I_C = 10μA, I_E = 0	20		V
BV_{EBO} Emitter Base Breakdown	I_E = 10μA, I_C = 0	5		V
BV_{CEO} Sustaining Voltage	I_C = 100μA	20		V
r_e (Note 1)	I_C = 500μA	1.2	1.4	Ω

MATCHING CHARACTERISTICS (T_A = +25°C)

CHARACTERISTIC	TEST CONDITION	MIN	MAX	UNIT
Δr_e (Note 2)	I_C = 500μA		0.05	Ω
$\frac{I_{S1} \cdot I_{S2}^2}{I_{S3} \cdot I_{S4}}$	$I_{S1} = I_{S2} = I_{S3}$ = 10μA to 1mA	0.097	1.03	

Note 1: r_e is defined by $V_{BE} = \frac{KT}{q} \log \frac{I_C}{I_O} + I_C r_e$.

Note 2: $\Delta r_e = r_{e1} + r_{e2} - r_{e3} - r_{e4}$.

INTERSIL

Voltage-Controlled Resistors VCR2N, VCR3P, VCR4N, VCR5P, VCR7N

FEATURES

- Small Signal Attenuators
- Filters
- Amplifier Gain Control
- Oscillator Amplitude Control

PACKAGE DIMENSIONS

VCR2N
VCR4N

PIN	OUT
1	S
2	D
3	G-C

VCR3P
VCR5P

PIN	OUT
1	S
2	G
3	D
4	C

VCR7N

PIN	OUT
1	S
2	D
3	G
4	CASE

ABSOLUTE MAXIMUM RATING (25°C)

Gate-Drain or Gate-Source Voltage 15V
Gate Current ..... 10 mA
Total Device Dissipation at T_A = 25°C
(Derate at 2.0 mW/°C to 175°C) ..... 300 mW
Storage Temperature Range ..... −55 to +175°C

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

N-Channel VCR FETs

		Characteristic		VCR2N Min	VCR2N Max	VCR4N Min	VCR4N Max	VCR7N Min	VCR7N Max	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		−5		−0.2		−0.1	nA	V_{GS} = −15V, V_{DS} = 0	
2		BV_{GSS}	Gate-Source Breakdown Voltage	−15		−15		−15		V	I_G = −1 μA, V_{DS} = 0	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	−3.5	−7	−3.5	−7	−2.5	−5		I_D = 1 μA, V_{DS} = 10V	
4		$r_{ds(on)}$	Drain Source ON Resistance	20	60	200	600	4,000	8,000	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	DYNAMIC	C_{dgo}	Drain-Gate Capacitance		7.5		3		1.5	pF	V_{GD} = −10V, I_S = 0	f = 1 MHz
6		C_{sgo}	Source-Gate Capacitance		7.5		3		1.5		V_{GS} = −10V, I_D = 0	

P-Channel VCR FETs

		Characteristic		VCR3P	VCR5P	Unit	Test Conditions	
1	STATIC	I_{GSS}	Gate Reverse Current		20		10	nA	V_{GS} = 15V, V_{DS} = 0	
2		BV_{GSS}	Gate-Source Breakdown Voltage	15		15		V	I_G = 1μA, V_{DS} = 0	
3		$V_{GS(off)}$	Gate-Source Cutoff Voltage	3.5	7	3.5	7		I_D = −1μA, V_{DS} = −10V	
4		$r_{ds(on)}$	Drain-Source ON Resistance	70	200	300	900	Ω	V_{GS} = 0, I_D = 0	f = 1 kHz
5	DYNAMIC	C_{dgo}	Drain-Gate Capacitance		6		3	pF	V_{GD} = 10V, I_S = 0	f = 1 MHz
6		C_{sgo}	Source-Gate Capacitance		6		3		V_{GS} = 10V, I_D = 0	

VMOS

$r_{DS\ (on)}$ = 2 ohms

IVN6657/IVN6658 2-3
VN30AA/35AA/67AA/89AA/90AA 2-5
VN35AJ/66AJ/67AJ/98AJ/99AJ 2-7
IVN6660/IVN6661 2-9
VN30AB/35AB/67AB/89AB/90AB 2-11
VN35AK/66AK/67AK/98AK/99AK 2-13
VN40AF/67AF/89AF 2-15
VN46AF/66AF/88AF 2-17
IVN5000/5001S series 2-19
IVN5000/5001A series 2-23

$r_{DS\ (on)}$ = 0.4 ohm

IVN5200/5201K series 2-27
IVN5200/5201T series 2-31
IVN5200/5201H series 2-35
IVN5201C series 2-39

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V-MOS

(N-Channel Enhancement)

PRELIMINARY
Final specification. Some parameters are subject to change.

$r_{DS(on)}$ (ohms)	$I_{D(on)}$ (Amps)		$V_{GS(th)}$ (Volts)		B V_{DSS}—DRAIN-SOURCE BREAKDOWN VOLTAGE										PKG
					35 V_{min}		40 V_{min}		60 V_{min}		80 V_{min}		90 V_{min}		
max	min	peak	min	max	Zener	Non-Zener	Zener	Non-Zener	Zener	Non-Zener	Zener	Non-Zener	Zener	Non-Zener	
0.5	5.0	12	0.8	2.0				IVN5200KND		IVN5200KNE		IVN5200KNF			TO-3
0.5	5.0	12	0.8	3.6				IVN5201KND		IVN5201KNE		IVN5201KNF			
2.5	1.0	3.0	0.8	2.0		VN35AJ									
2.5	1.0	3.0	0.8	—	VN35AA										
3.0	1.0	3.0	0.8	2.0					IVN6657	VN66AJ					
3.5	1.0	3.0	0.8	—					VN67AA						
3.5	1.0	3.0	0.8	2.0						VN67AJ					
4.0	1.0	3.0	0.8	2.0									IVN6658	VN98AJ	
4.5	1.0	3.0	0.8	—							VN89AA				
4.5	1.0	3.0	0.8	2.0										VN99AJ	
5.0	1.0	3.0	0.8	—	VN30AA								VN90AA		
0.5	5.0	10	0.8	2.0				IVN5200TND		IVN5200TNE		IVN5200TNF			TO-39
0.5	5.0	10	0.8	3.6				IVN5201TND		IVN5201TNE		IVN5201TNF			
2.5	1.0	3.0	0.8	—	VN35AB										
2.5	1.0	3.0	0.8	2.0		VN35AK									
3.0	1.0	3.0	0.8	2.0					IVN6660	VN66AK					
3.5	1.0	3.0	0.8	2.0						VN67AK					
3.5	1.0	3.0	0.8	—					VN67AB						
4.0	1.0	3.0	0.8	2.0									IVN6661	VN98AK	
4.5	1.0	3.0	0.8	—							VN89AB				
4.5	1.0	3.0	0.8	2.0										VN99AK	
5.0	1.0	3.0	0.8	—	VN30AB								VN90AB		
2.5	1.0	3.0	0.8	2.0				IVN5000SND		IVN5000SNE		IVN5000SNF			TO-52
2.5	1.0	3.0	0.8	3.6				IVN5001SND		IVN5001SNE		IVN5001SNF			
0.5	5.0	12	0.8	2.0				IVN5200HND		IVN5200HNE		IVN5200HNF			TO-66
0.5	5.0	12	0.8	3.6				IVN5201HND		IVN5201HNE		IVN5201HNF			
3.0	1.0	3.0	0.8	—			VN46AF		VN66AF						TO-202
3.5	1.0	3.0	0.8	—					VN67AF						
4.0	1.0	3.0	0.8	—							VN88AF				
4.5	1.0	3.0	0.8	—							VN89AF				
5.0	1.0	3.0	0.8	—			VN40AF								
0.5	5.0	12	0.8	3.6				IVN5201CND		IVN5201CNE		IVN5201CNF			TO-220
2.5	1.0	2.0	0.8	2.0				IVN5000AND		IVN5000ANE		IVN5000ANF			TO-237
2.5	1.0	2.0	0.8	3.6				IVN5001AND		IVN5001ANE		IVN5001ANF			

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INTERSIL

IVN6657, IVN6658
n-Channel Enhancement-mode VMOS Power FETs

REPLACEMENTS FOR 2N6657,2N6658

PRELIMINARY

FEATURES

- High speed, high current switching
- Current sharing capability when paralleled
- Directly interface to CMOS, DTL, TTL logic
- DC biasing relatively simple
- Extended safe operating area
- Inherently temperature stable

APPLICATIONS

- Switching power supplies
- DC to DC inverters
- CMOS and TTL to high current interface
- Line drivers
- Logic buffers
- Pulse amplifiers

ABSOLUTE MAXIMUM RATINGS
(25°C unless otherwise noted)

Drain-source Voltage
- IVN6657 ..... 60V
- IVN6658 ..... 90V

Drain-gate Voltage
- IVN6657 ..... 60V
- IVN6658 ..... 90V

Continuous Drain Current (see note 1) 2.4A
Peak Drain Current (see note 2) 3.0A
Continuous Forward Gate Current 2.0mA
Peak-gate Forward Current 100mA
Peak-gate Reverse Current 100mA
Gate-source Forward (Zener) Voltage ..... +15V
Gate-source Reverse (Zener) Voltage ..... –0.3V
Thermal Resistance, Junction to Case ..... 5.0°C/W
Continuous Device Dissipation at (or below) 25°C Case Temperature 25W
Linear Derating Factor ..... 200mW/°C
Operating Junction Temperature Range ..... –55 to +150°C
Storage Temperature Range ..... –55 to +150°C
Lead Temperature (1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $R_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

SCHEMATIC DIAGRAM

Body internally connected to source.
Drain common to case.

PACKAGE DIMENSIONS

PKG: JEDEC TO-3

Dimensions shown in inches and *(mm)*.

OBSOLETE PART — Since this device is no longer in production, Some parameters may be subject to change.

*ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		CHARACTERISTIC		IVN6657 MIN	IVN6657 TYP	IVN6657 MAX	IVN6658 MIN	IVN6658 TYP	IVN6658 MAX	UNIT	TEST CONDITIONS	
1	STATIC	BV_{DSS}	Drain Source Breakdown	60			90			V	V_{GS} = 0, I_D = 10μA	
2				60			90				V_{GS} = 0, I_D = 2.5mA	
3		$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1mA	
4		I_{GSS}	Gate-Body Leakage		0.5	100		0.5	100	nA	V_{GS} = 15V, V_{DS} = 0	
5						500			500		V_{GS} = 15V, V_{DS} = 0, T_A = 125°C (Note 2)	
6		I_{DSS}	Zero Gate Voltage Drain Current			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0	
7						500			500		V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)	
8					100			100		nA	V_{DS} = 25V, V_{GS} = 0	
9		$I_{D(on)}$	ON-State Drain Current	1.0	2		1.0	2		A	V_{DS} = 25V, V_{GS} = 10V	(Note 1)
10		$V_{DS(on)}$	Drain-Source Saturation Voltage		0.3			0.4		V	V_{GS} = 5V, I_D = 0.1 Amp	
11					1.0	1.5		1.1	1.6		V_{GS} = 5V, I_D = 0.3 Amp	
12					0.9			1.3			V_{GS} = 10V, I_D = 0.5 Amp	
13					2.2	3.0		2.2	4.0		V_{GS} = 10V, I_D = 1.0 Amp	
14		$r_{DS(on)}$	Static Drain-Source ON-State Resistance		2.2	3.0		2.2	4.0	Ω	V_{GS} = 10V, I_D = 1.0 Amp	
15	DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON-State Resistance		2.2	3.0		2.2	4.0		V_{GS} = 10V, I_D = 1.0, f = 1kHz	
16		g_{fs}	Forward Transconductance	170	250		170	250		m℧	V_{DS} = 24V, I_D = 0.5 Amp	
17		C_{iss}	Input Capacitance			50			50	pF	V_{GS} = 0, V_{DS} = 24V, f = 1.0MHz	(Note 2)
18		C_{ds}	Drain-Source Capacitance			40			40			
19		C_{rss}	Reverse Transfer Capacitance			10			10		V_{GS} = 0, V_{DS} = 24V, f = 1.0MHz	
20						35			35		V_{GS} = 0, V_{DS} = 0, f = 1.0MHz	
21		$t_{d(on)}$	Turn-ON Delay Time		2	5		2	5	ns		
22		t_r	Rise Time		2	5		2	5			
23		$t_{d(off)}$	Turn-OFF Delay Time		2	5		2	5			
24		t_f	Fall Time		2	5		2	5			

Note 1. Pulse test — 80μsec pulse, 1% duty cycle.
Note 2. Sample test.

THERMAL RESPONSE

POWER DISSIPATION vs CASE TEMPERATURE

DC SAFE OPERATING REGION TC = 25°C

INTERSIL

VN30AA, VN35AA, VN67AA, VN89AA, VN90AA n-Channel Enhancement-mode VMOS Power FETs

PRELIMINARY

Notice: This is not a final specification. Some parametric limits are subject to change.

FEATURES

- High speed, high current switching
- Current sharing capability when paralleled
- Directly interface to CMOS, DTL, TTL logic
- DC biasing relatively simple
- Extended safe operating area
- Inherently temperature stable

APPLICATIONS

- Switching power supplies
- DC to DC inverters
- CMOS and TTL to high current interface
- Line drivers
- Logic buffers
- Pulse amplifiers

2

ABSOLUTE MAXIMUM RATINGS

(25°C unless otherwise noted)

Drain-source Voltage
- VN30AA, VN35AA 35V
- VN67AA 60V
- VN89AA 80V
- VN90AA 90V

Drain-gate Voltage
- VN30AA, VN35AA 35V
- VN67AA 60V
- VN89AA 80V
- VN90AA 90V

Continuous Drain Current (see note 1) 2.4A
Peak Drain Current (see note 2) 3.0A
Continuous Forward Gate Current 2.0mA
Peak-gate Forward Current 100mA
Peak-gate Reverse Current 100mA
Gate-source Forward (Zener) Voltage ..... +15V
Gate-source Reverse (Zener) Voltage ..... −0.3V
Thermal Resistance, Junction to Case ..... 5.0°C/W
Continuous Device Dissipation at (or below)
25°C Case Temperature 25W
Linear Derating Factor ..... 200mW/°C
Operating Junction
Temperature Range ..... −55 to +150°C
Storage Temperature Range ..... −55 to +150°C
Lead Temperature
(1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $R_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

SCHEMATIC DIAGRAM

Body internally connected to source
Drain common to case

PACKAGE DIMENSIONS

PKG: JEDEC TO-3

Dimensions shown in inches and *(mm)*.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		CHARACTERISTIC		VN30AA			VN35AA			VN67AA			VN89AA			VN90AA			UNIT	TEST CONDITIONS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
1	STATIC	BV_{DSS}	Drain Source Breakdown	35			35			60			80			90			V	$I_D = 10\mu A$, $V_{GS} = 0$
2	STATIC	$V_{GS(th)}$	Gate Threshold Voltage	0.8	1.2		0.8	1.2		0.8	1.2		0.8	1.2		0.8	1.2		V	$I_D = 1.0mA$, $V_{DS} = V_{GS}$
3	STATIC	I_{GSS}	Gate-Body Leakage		0.01	0.5		0.01	0.5		0.01	0.5		0.01	0.5		0.01	0.5	μA	$V_{GS} = 10V$, $V_{DS} = 0$
4	STATIC	I_{DSS}	Zero Gate Voltage Drain Current			10			10			10			10			10	μA	$V_{DS} = 25V$, $V_{GS} = 0$
5	STATIC	$R_{DS(on)}$	Drain-Source ON-State Resistance (Note 1)			6.0			4.5			5.1			5.1			6.0	Ω	$V_{GS} = 5V$, $I_D = 300mA$
					2.2	5.0		2.2	2.5		2.2	3.5		2.2	4.5		2.2	5.0		$V_{GS} = 10V$, $I_D = 1.0A$
6	STATIC	$I_{D(on)}$	ON-State Drain Current (Note 1)	1.0	2.0		1.0	2.0		1.0	2.0		1.0	2.0		1.0	2.0		A	$V_{DS} = 25V$, $V_{GS} = 10V$
7	DYNAMIC	g_{fs}	Forward Transconductance (Note 1)	150	250		150	250		150	250		150	250		150	250		m℧	$V_{DS} = 25V$, $I_D = 0.5A$
8	DYNAMIC	C_{iss}	Input Capacitance (Note 2)			50			50			50			50			50	pF	$V_{GS} = 0$, $V_{DS} = 24V$, f = 1.0MHz
9	DYNAMIC	C_{rss}	Reverse Transfer Capacitance (Note 2)			10			10			10			10			10	pF	
10	DYNAMIC	C_{oss}	Common Source Output Capacitance (Note 2)			40			40			40			40			40	pF	
11	DYNAMIC	t_{on}	Turn-ON Time (Note 2)			10			10			10			10			10	ns	
12	DYNAMIC	t_{off}	Turn-OFF Time (Note 2)			10			10			10			10			10	ns	

Note 1. Pulse Test — 80μs, 1% duty cycle.

Note 2. Sample Test.

2

THERMAL RESPONSE

POWER DISSIPATION vs CASE TEMPERATURE

DC SAFE OPERATING REGION T_C = 25°C

INTERSIL

VN35AJ, VN66AJ, VN67AJ, VN98AJ, VN99AJ
n-Channel Enhancement-mode VMOS Power FETs

PRELIMINARY

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

FEATURES

- High speed, high current switching
- High gain-bandwidth product
- Inherently temperature stable
- Extended safe operating area
- DC biasing relatively simple
- Requires almost zero current drive

APPLICATIONS

- High current analog switches
- RF power amplifiers
- Laser diode pulsers
- Line drivers
- Logic buffers
- Pulse amplifiers

2

ABSOLUTE MAXIMUM RATINGS
(25°C unless otherwise noted)

Drain-source Voltage
- VN35AJ 35V
- VN66AJ, VN67AJ 60V
- VN98AJ, VN99AJ 90V

Drain-gate Voltage
- VN35AJ 35V
- VN66AJ, VN67AJ 60V
- VN98AJ, VN99AJ 90V

Continuous Drain Current (see note 1) 2.4A
Peak Drain Current (see note 2) 3.0A
Gate-source Forward Voltage ..... +30V
Gate-source Reverse Voltage ..... −30V
Thermal Resistance, Junction to Case ..... 5.0°C/W
Continuous Device Dissipation at (or below)
- 25°C Case Temperature 25W

Linear Derating Factor ..... 200mW/°C
Operating Junction
- Temperature Range ..... −55 to +150°C

Storage Temperature Range ..... −55 to +150°C
Lead Temperature
- (1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $R_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

SCHEMATIC DIAGRAM

Body internally connected to source.
Drain common to case.

PACKAGE DIMENSIONS

PKG: JEDEC TO-3

Dimensions shown in inches and *(mm)*.

VN35AJ, VN66AJ, VN67AJ, VN98AJ, VN99AJ

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		CHARACTERISTIC			VN35AJ MIN	VN35AJ TYP	VN35AJ MAX	VN66AJ VN67AJ MIN	VN66AJ VN67AJ TYP	VN66AJ VN67AJ MAX	VN98AJ VN99AJ MIN	VN98AJ VN99AJ TYP	VN98AJ VN99AJ MAX	UNIT	TEST CONDITIONS	
1	STATIC	BV_{DSS}	Drain-Source Breakdown		35			60			90			V	V_{GS} = 0, I_D = 10μA	
2	STATIC	$V_{GS(th)}$	Gate-Threshold Voltage		0.8		2.0	0.8		2.0	0.8		2.0	V	V_{DS} = V_{GS}, I_D = 1mA	
3	STATIC	I_{GSS}	Gate-Body Leakage			0.5	100		0.5	100		0.5	100	nA	V_{GS} = 15V, V_{DS} = 0	
4	STATIC	I_{GSS}	Gate-Body Leakage				500			500			500	nA	V_{GS} = 15V, V_{DS} = 0, T_A = 125°C (Note 2)	
5	STATIC	I_{DSS}	Zero Gate Voltage Drain Current				10			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0	
6	STATIC	I_{DSS}	Zero Gate Voltage Drain Current				500			500			500	μA	V_{DS} = 0.8 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)	
7	STATIC	I_{DSS}	Zero Gate Voltage Drain Current			100			100			100		nA	V_{DS} = 25V, V_{GS} = 0	
8	STATIC	$I_{D(on)}$	ON-State Drain Current		1.0	2.0		1.0	2.0		1.0	2.0		A	V_{DS} = 25V, V_{GS} = 10V	
9	STATIC	$V_{DS(on)}$	Drain-Source Saturation Voltage	VN66AJ					1.0			1.1		V	V_{GS} = 5V, I_D = 0.3A	(Note 1)
10	STATIC	$V_{DS(on)}$	Drain-Source Saturation Voltage	VN98AJ					2.2	3.0		2.2	4.0	V	V_{GS} = 10V, I_D = 1.0A	(Note 1)
11	STATIC	$V_{DS(on)}$	Drain-Source Saturation Voltage	VN35AJ		1.0			1.1			1.2		V	V_{GS} = 5V, I_D = 0.3A	(Note 1)
12	STATIC	$V_{DS(on)}$	Drain-Source Saturation Voltage	VN67AJ VN99AJ		2.2	2.5		2.2	3.5		2.2	4.5	V	V_{GS} = 10V, I_D = 1.0A	(Note 1)
13	DYNAMIC	g_{fs}	Forward Transconductance		170	250		170	250		170	250		m℧	V_{DS} = 24V, I_D = 0.5A	(Note 1)
14	DYNAMIC	C_{iss}	Input Capacitance			40	50		40	50		40	50	pF	V_{GS} = 0, V_{DS} = 24V, f = 1MHz	(Note 2)
15	DYNAMIC	C_{oss}	Common Source Output Capacitance			38	45		35	40		32	40	pF	V_{GS} = 0, V_{DS} = 24V, f = 1MHz	(Note 2)
16	DYNAMIC	C_{rss}	Reverse Transfer Capacitance			7	10		6	10		5	10	pF	V_{GS} = 0, V_{DS} = 24V, f = 1MHz	(Note 2)
17	DYNAMIC	t_{on}	Turn ON Time			3	8		3	8		3	8	ns		(Note 2)
18	DYNAMIC	t_{off}	Turn OFF Time			3	8		3	8		3	8	ns		(Note 2)

Note 1. Pulse test — 80μs pulse, 1% duty cycle.
Note 2. Sample test.

2

THERMAL RESPONSE

POWER DISSIPATION vs CASE TEMPERATURE

DC SAFE OPERATING REGION T_C = 25°C

INTERSIL

IVN6660, IVN6661 n-Channel Enhancement-mode VMOS Power FETs

REPLACEMENTS FOR 2N6660, 2N6661
PRELIMINARY

PRELIMINARY DATA
Notice: This is not a final specification. Some parametric limits are subject to change.

FEATURES

- High speed, high current switching
- Current sharing capability when paralleled
- Directly interface to CMOS, DTL, TTL logic
- DC biasing relatively simple
- Extended safe operating area
- Inherently temperature stable

APPLICATIONS

- Switching power supplies
- DC to DC inverters
- CMOS and TTL to high current interface
- Line drivers
- Logic buffers
- Pulse amplifiers

ABSOLUTE MAXIMUM RATINGS
(25°C unless otherwise noted)

Drain-source Voltage
IVN6660 ..... 60V
IVN6661 ..... 90V
Drain-gate Voltage
IVN6660 ..... 60V
IVN6661 ..... 90V
Continuous Drain Current (see note 1) 1.2A
Peak Drain Current (see note 2) 3.0A
Continuous Forward Gate Current 2.0mA
Peak-gate Forward Current 100mA
Peak-gate Reverse Current 100mA
Gate-source Forward (Zener) Voltage ..... +15V
Gate-source Reverse (Zener) Voltage ..... −0.3V
Thermal Resistance, Junction to Case ..... 20°C/W
Continuous Device Dissipation at (or below)
25°C Case Temperature 6.25W
Linear Derating Factor ..... 50mW/°C
Operating Junction
Temperature Range ..... −55 to +150°C
Storage Temperature Range ..... −55 to +150°C
Lead Temperature
(1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $R_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

SCHEMATIC DIAGRAM

Body internally connected to source.
Drain common to case.

PACKAGE DIMENSIONS

PKG: JEDEC TO-39

Dimensions shown in inches and *(mm)*.

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		CHARACTERISTIC		IVN6660 MIN	IVN6660 TYP	IVN6660 MAX	IVN6661 MIN	IVN6661 TYP	IVN6661 MAX	UNIT	TEST CONDITIONS	
1	STATIC	BV_{DSS}	Drain Source Breakdown	60			90			V	V_{GS} = 0, I_D = 10μA	
2				60			90				V_{GS} = 0, I_D = 2.5mA	
3		$V_{GS(th)}$	Gate Threshold Voltage	0.8		2.0	0.8		2.0		V_{DS} = V_{GS}, I_D = 1mA	
4		I_{GSS}	Gate-Body Leakage		0.5	100		0.5	100	nA	V_{GS} = 15V, V_{DS} = 0	
5						500			500		V_{GS} = 15V, V_{DS} = 0, T_A = 125°C	(Note 2)
6		I_{DSS}	Zero Gate Voltage Drain Current			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0	
7						500			500		V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)	
8					100			100		nA	V_{DS} = 25V, V_{GS} = 0	
9		$I_{D(on)}$	ON-State Drain Current	1.0	2		1.0	2		A	V_{DS} = 25V, V_{GS} = 10V	(Note 1)
10		$V_{DS(on)}$	Drain-Source Saturation Voltage		0.3			0.4		V	V_{GS} = 5V, I_D = 0.1 Amp	
11					1.0	1.5		1.1	1.6		V_{GS} = 5V, I_D = 0.3 Amp	
12					0.9			1.3			V_{GS} = 10V, I_D = 0.5 Amp	
13					2.2	3.0		2.2	4.0		V_{GS} = 10V, I_D = 1.0 Amp	
14		$r_{DS(on)}$	Static Drain-Source ON-State Resistance		2.2	3.0		2.2	4.0	Ω	V_{GS} = 10V, I_D = 1.0 Amp	
15	DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON-State Resistance		2.2	3.0		2.2	4.0		V_{GS} = 10V, I_D = 1.0, f = 1kHz	
16		g_{fs}	Forward Transconductance	170	250		170	250		m℧	V_{DS} = 24V, I_D = 0.5 Amp	
17		C_{iss}	Input Capacitance			50			50	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0MHz	(Note 2)
18		C_{ds}	Drain-Source Capacitance			40			40			
19		C_{rss}	Reverse Transfer Capacitance			10			10		V_{GS} = 0, V_{DS} = 24V, f = 1.0MHz	
20						35			35		V_{GS} = 0, V_{DS} = 0, f = 1.0MHz	
21		$t_{d(on)}$	Turn-ON Delay Time		2	5		2	5	ns		
22		t_r	Rise Time		2	5		2	5			
23		$t_{d(off)}$	Turn-OFF Delay Time		2	5		2	5			
24		t_f	Fall Time		2	5		2	5			

Note 1. Pulse test — 80μsec pulse, 1% duty cycle. **Note 2.** Sample test.

THERMAL RESPONSE

POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE

DC SAFE OPERATING REGION Tc = 25°C

INTERSIL

VN30AB, VN35AB, VN67AB, VN89AB, VN90AB n-Channel Enhancement-mode VMOS Power FETs

PRELIMINARY

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

FEATURES

- High speed, high current switching
- Current sharing capability when paralleled
- Directly interface to CMOS, DTL, TTL logic
- DC biasing relatively simple
- Extended safe operating area
- Inherently temperature stable

APPLICATIONS

- Switching power supplies
- DC to DC inverters
- CMOS and TTL to high current interface
- Line drivers
- Logic buffers
- Pulse amplifiers

ABSOLUTE MAXIMUM RATINGS
(25°C unless otherwise noted)

Drain-source Voltage
- VN30AB, VN35AB 35V
- VN67AB 60V
- VN89AB 80V
- VN90AB 90V

Drain-gate Voltage
- VN30AB, VN35AB 25V
- VN67AB 60V
- VN89AB 80V
- VN90AB 90V

Continuous Drain Current (see note 1) 1.2A
Peak Drain Current (see note 2) 3.0A
Continuous Forward Gate Current 2.0mA
Peak-gate Forward Current 100mA
Peak-gate Reverse Current 100mA
Gate-source Forward (Zener) Voltage ..... +15V
Gate-source Reverse (Zener) Voltage ..... –0.3V
Thermal Resistance, Junction to Case ..... 20°C/W
Continuous Device Dissipation at (or below) 25°C Case Temperature 6.25W
Linear Derating Factor ..... 50mW/°C
Operating Junction Temperature Range ..... –55 to +150°C
Storage Temperature Range ..... –55 to +150°C
Lead Temperature (1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $R_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

SCHEMATIC DIAGRAM

Body internally connected to source.
Drain common to tab.

PACKAGE DIMENSIONS

PKG: JEDEC TO-39

Dimensions shown in inches and *(mm)*.

2

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		CHARACTERISTIC		VN30AB			VN35AB			VN67AB			VN89AB			VN90AB			UNIT	TEST CONDITIONS
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX		
1		BV_{DSS}	Drain Source Breakdown	35			35			60			80			90			V	I_D = 10μA, V_{GS} = 0
2		$V_{GS(th)}$	Gate Threshold Voltage	0.8	1.2		0.8	1.2		0.8	1.2		0.8	1.2		0.8	1.2			I_D = 1.0mA, V_{DS} = V_{GS}
3	STATIC	I_{GSS}	Gate-Body Leakage		0.01	0.5		0.01	0.5		0.01	0.5		0.01	0.5		0.01	0.5	μA	V_{GS} = 10V, V_{DS} = 0
4	STATIC	I_{DSS}	Zero Gate Voltage Drain Current			10			10			10			10			10	μA	V_{DS} = 25V, V_{GS} = 0
5	STATIC	$R_{DS(on)}$	Drain-Source ON-State Resistance (Note 1)		6.0				4.5			5.1			5.1			6.0	Ω	V_{GS} = 5V, I_D = 300mA
					2.2	5.0		2.2	2.5		2.2	3.5		2.2	4.5		2.2	5.0		V_{GS} = 10V, I_D = 1.0A
6	STATIC	$I_{D(on)}$	ON-State Drain Current (Note 1)	1.0	2.0		1.0	2.0		1.0	2.0		1.0	2.0		1.0	2.0		A	V_{DS} = 25V, V_{GS} = 10V
7	DYNAMIC	g_{fs}	Forward Transconductance		250			250			250			250			250		m℧	V_{DS} = 25V, I_D = 0.5A
8	DYNAMIC	C_{iss}	Input Capacitance (Note 2)			50			50			50			50			50	pF	V_{GS} = 0, V_{DS} = 24V, f = 1.0MHz
9	DYNAMIC	C_{rss}	Reverse Transfer Capacitance (Note 2)			10			10			10			10			10	pF	V_{GS} = 0, V_{DS} = 24V, f = 1.0MHz
10	DYNAMIC	C_{oss}	Common Source Output Capacitance (Note 2)			40			40			40			40			40	pF	V_{GS} = 0, V_{DS} = 24V, f = 1.0MHz
11	DYNAMIC	t_{on}	Turn-ON Time (Note 2)			10			10			10			10			10	ns	
12	DYNAMIC	t_{off}	Turn-OFF Time (Note 2)			10			10			10			10			10	ns	

Note 1. Pulse Test — 80μs, 1% duty cycle.

Note 2. Sample Test.

THERMAL RESPONSE

POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE

DC SAFE OPERATING REGION Tc = 25°C

INTERSIL

VN35AK, VN66AK, VN67AK, VN98AK, VN99AK n-Channel Enhancement-mode VMOS Power FETs

PRELIMINARY

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

FEATURES

- High speed, high current switching
- High gain-bandwidth product
- Inherently temperature stable
- Extended safe operating area
- DC biasing relatively simple
- Requires almost zero current drive

APPLICATIONS

- High current analog switches
- RF power amplifiers
- Laser diode pulsers
- Line drivers
- Logic buffers
- Pulse amplifiers

ABSOLUTE MAXIMUM RATINGS
(25°C unless otherwise noted)

Drain-source Voltage
- VN35AK 35V
- VN66AK, VN67AK 60V
- VN98AK, VN99AK 90V

Drain-gate Voltage
- VN35AK 35V
- VN66AK, VN67AK 60V
- VN98AK, VN99AK 90V

Continuous Drain Current (see note 1) 1.2A
Peak Drain Current (see note 2) 3.0A
Gate-source Forward Voltage ..... +30V
Gate-source Reverse Voltage ..... −30V
Thermal Resistance, Junction to Case ..... 20°C/W
Continuous Device Dissipation at (or below)
- 25°C Case Temperature 6.25W

Linear Derating Factor ..... 50mW/°C
Operating Junction
- Temperature Range ..... −55 to +150°C

Storage Temperature Range ..... −55 to +150°C
Lead Temperature
- (1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $R_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

SCHEMATIC DIAGRAM

Body internally connected to source.
Drain common to case.

PACKAGE DIMENSIONS

PKG: JEDEC TO-39

Dimensions shown in inches and *(mm)*.

2

VN35AK, VN66AK, VN67AK, VN98AK, VN99AK

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		CHARACTERISTIC			VN35AK			VN66AK VN67AK			VN98AK VN99AK			UNIT	TEST CONDITIONS	
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS}	Drain-Source Breakdown		35			60			90			V	V_{GS} = 0, I_D = 10μA	
2	STATIC	$V_{GS(th)}$	Gate-Threshold Voltage		0.8		2.0	0.8		2.0	0.8		2.0	V	V_{DS} = V_{GS}, I_D = 1mA	
3	STATIC	I_{GSS}	Gate-Body Leakage			0.5	100		0.5	100		0.5	100	nA	V_{GS} = 15V, V_{DS} = 0	
4	STATIC	I_{GSS}	Gate-Body Leakage				500			500			500	nA	V_{GS} = 15V, V_{DS} = 0, T_A = 125°C (Note 2)	
5	STATIC	I_{DSS}	Zero Gate Voltage Drain Current				10			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0	
6	STATIC	I_{DSS}	Zero Gate Voltage Drain Current				500			500			500	μA	V_{DS} = 0.8 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)	
7	STATIC	I_{DSS}	Zero Gate Voltage Drain Current			100			100			100		nA	V_{DS} = 25V, V_{GS} = 0	
8	STATIC	$I_{D(on)}$	ON-State Drain Current		1.0	2.0		1.0	2.0		1.0	2.0		A	V_{DS} = 25V, V_{GS} = 10V	
9	STATIC	$V_{DS(on)}$	Drain-Source Saturation Voltage	VN66AK					1.0			1.1		V	V_{GS} = 5V, I_D = 0.3A	(Note 1)
10	STATIC	$V_{DS(on)}$	Drain-Source Saturation Voltage	VN98AK					2.2	3.0		2.2	4.0	V	V_{GS} = 10V, I_D = 1.0A	(Note 1)
11	STATIC	$V_{DS(on)}$	Drain-Source Saturation Voltage	VN35AK VN67AK VN99AK		1.0			1.1			1.2		V	V_{GS} = 5V, I_D = 0.3A	(Note 1)
12	STATIC	$V_{DS(on)}$	Drain-Source Saturation Voltage	VN35AK VN67AK VN99AK		2.2	2.5		2.2	3.5		2.2	4.5	V	V_{GS} = 10V, I_D = 1.0A	(Note 1)
13	STATIC	g_{fs}	Forward Transconductance		170	250		170	250		170	250		m℧	V_{DS} = 24V, I_D = 0.5A	(Note 1)
14	DYNAMIC	C_{iss}	Input Capacitance			40	50		40	50		40	50	pF	V_{GS} = 0, V_{DS} = 24V, f = 1MHz	(Note 2)
15	DYNAMIC	C_{oss}	Common Source Output Capacitance			38	45		35	40		32	40	pF	V_{GS} = 0, V_{DS} = 24V, f = 1MHz	(Note 2)
16	DYNAMIC	C_{rss}	Reverse Transfer Capacitance			7	10		6	10		5	10	pF	V_{GS} = 0, V_{DS} = 24V, f = 1MHz	(Note 2)
17	DYNAMIC	t_{on}	Turn ON Time			3	8		3	8		3	8	ns		(Note 2)
18	DYNAMIC	t_{off}	Turn OFF Time			3	8		3	8		3	8	ns		(Note 2)

Note 1. Pulse test — 80μs pulse, 1% duty cycle. **Note 2.** Sample test.

2

THERMAL RESPONSE

POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE

DC SAFE OPERATING REGION Tc = 25°C

INTERSIL

VN40AF, VN67AF, VN89AF
n-Channel Enhancement-mode VMOS Power FETs

PRELIMINARY

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

FEATURES

- High speed, high current switching
- Current sharing capability when paralleled
- Directly interface to CMOS, DTL, TTL logic
- DC biasing relatively simple
- Extended safe operating area
- Inherently temperature stable

APPLICATIONS

- Switching power supplies
- DC to DC inverters
- CMOS and TTL to high current interface
- Line drivers
- Logic buffers
- Pulse amplifiers

ABSOLUTE MAXIMUM RATINGS
(25°C unless otherwise noted)

Drain-source Voltage
- VN40AF 40V
- VN67AF 60V
- VN89AF 80V

Drain-gate Voltage
- VN40AF 40V
- VN67AF 60V
- VN89AF 80V

Continuous Drain Current (see note 1) 1.7A
Peak Drain Current (see note 2) 3.0A
Continuous Forward Gate Current 2.0mA
Peak-gate Forward Current 100mA
Peak-gate Reverse Current 100mA
Gate-source Forward (Zener) Voltage ..... +15V
Gate-source Reverse (Zener) Voltage ..... –0.3V
Thermal Resistance, Junction to Case ..... 10.4°C/W
Continuous Device Dissipation at (or below)
25°C Case Temperature 12W
Linear Derating Factor ..... 96mW/°C
Operating Junction
Temperature Range ..... –40 to +150°C
Storage Temperature Range ..... –40 to +150°C
Lead Temperature
(1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $R_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

SCHEMATIC DIAGRAM

Body internally connected to source.
Drain common to tab.

PACKAGE DIMENSIONS

PKG: JEDEC TO-202

Dimensions shown in inches and *(mm)*.

2

INTERSIL

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		CHARACTERISTIC		VN40AF MIN	VN40AF TYP	VN40AF MAX	VN67AF MIN	VN67AF TYP	VN67AF MAX	VN89AF MIN	VN89AF TYP	VN89AF MAX	UNIT	TEST CONDITIONS	
1	STATIC	BV_{DSS}	Drain-Source Breakdown	40			60			80			V	V_{GS} = 0, I_D = 10μA	
2				40			60			80				V_{GS} = 0, I_D = 2.5mA	
3		$V_{GS(th)}$	Gate-Threshold Voltage	0.6	1.2		0.8	1.2		0.8	1.2			V_{DS} = V_{GS}, I_D = 1mA	
4		I_{GSS}	Gate-Body Leakage		0.01	10		0.01	10		0.01	10	μA	V_{GS} = 10V, V_{DS} = 0	
5						100			100			100		V_{GS} = 10V, V_{DS} = 0, T_A = 125°C (Note 2)	
6		I_{DSS}	Zero Gate Voltage Drain Current			10			10			10		V_{DS} = Max. Rating, V_{GS} = 0	
7						100			100			100		V_{DS} = 0.8 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)	
8					100			100			100		nA	V_{DS} = 25V, V_{GS} = 0	
9		$I_{D(on)}$	ON-State Drain Current	1.0	2		1.0	2		1.0	2		A	V_{DS} = 25V, V_{GS} = 10V	
10		$V_{DS(on)}$	Drain-Source Saturation Voltage		0.3			0.3			0.4		V	V_{GS} = 5V, I_D = 0.1A	(Note 1)
11					1.0	2.0		1.0	1.7		1.4	1.9		V_{GS} = 5V, I_D = 0.3A	
12					1.0			1.0			1.3			V_{GS} = 10V, I_D = 0.5A	
13					2.2	5.0		2.2	3.5		2.2	4.5		V_{GS} = 10V, I_D = 1.0A	
14	DYNAMIC	g_m	Forward Transconductance		250			250			250		m℧	V_{DS} = 24V, I_D = 0.5A	
15		C_{iss}	Input Capacitance			50			50			50	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0 MHz	(Note 2)
16		C_{rss}	Reverse Transfer Capacitance			10			10			10			
17		C_{oss}	Common-Source Output Capacitance			50			50			50			
18		$t_{d(on)}$	Turn-ON Delay Time		2	5		2	5		2	5	ns		
19		t_r	Rise Time		2	5		2	5		2	5			
20		$t_{d(off)}$	Turn-OFF Delay Time		2	5		2	5		2	5			
21		t_f	Fall Time		2	5		2	5		2	5			

Note 1. Pulse test — 80μs pulse, 1% duty cycle.
Note 2. Sample test.

2

THERMAL RESPONSE

POWER DISSIPATION vs CASE TEMPERATURE

DC SAFE OPERATING REGION Tc = 25°C

INTERSIL

VN46AF, VN66AF, VN88AF
n-Channel Enhancement-mode VMOS Power FETs

PRELIMINARY

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject to change.

FEATURES

- High speed, high current switching
- Current sharing capability when paralleled
- Directly interface to CMOS, DTL, TTL logic
- DC biasing relatively simple
- Extended safe operating area
- Inherently temperature stable

APPLICATIONS

- Switching power supplies
- DC to DC inverters
- CMOS and TTL to high current interface
- Line drivers
- Logic buffers
- Pulse amplifiers

ABSOLUTE MAXIMUM RATINGS
(25°C unless otherwise noted)

Drain-source Voltage
- VN46AF 40V
- VN66AF 60V
- VN88AF 80V

Drain-gate Voltage
- VN46AF 40V
- VN66AF 60V
- VN88AF 80V

Continuous Drain Current (see note 1) 1.7A
Peak Drain Current (see note 2) 3.0A
Continuous Forward Gate Current 2.0mA
Peak-gate Forward Current 100mA
Peak-gate Reverse Current 100mA
Gate-source Forward (Zener) Voltage ..... +15V
Gate-source Reverse (Zener) Voltage ..... –0.3V
Thermal Resistance, Junction to Case ..... 10.4°C/W
Continuous Device Dissipation at (or below) 25°C Case Temperature 12W
Linear Derating Factor ..... 96mW/°C
Operating Junction Temperature Range ..... –40 to +150°C
Storage Temperature Range ..... –40 to +150°C
Lead Temperature (1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $R_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

SCHEMATIC DIAGRAM

Body internally connected to source. Drain common to tab.

PACKAGE DIMENSIONS

PKG: JEDEC TO-202

Dimensions shown in inches and *(mm)*.

2

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted)

		CHARACTERISTIC		VN46AF			VN66AF			VN88AF			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS}	Drain-Source Breakdown	40			60			80			V	V_{GS} = 0, I_D = 10μA	
2				40			60			80				V_{GS} = 0, I_D = 2.5mA	
3		$V_{GS(th)}$	Gate-Threshold Voltage	0.8	1.7		0.8	1.7		0.8	1.7			V_{DS} = V_{GS}, I_D = 1mA	
4		I_{GSS}	Gate-Body Leakage		0.01	10		0.01	10		0.01	10	μA	V_{GS} = 10V, V_{DS} = 0	
5						100			100			100		V_{GS} = 10V, V_{DS} = 0, T_A = 125°C (Note 2)	
6		I_{DSS}	Zero Gate Voltage Drain Current			10			10			10		V_{DS} = Max. Rating, V_{GS} = 0	
7						100			100			100		V_{DS} = 0.8 Max. Rating, V_{GS} = 0, T_A = 125°C (Note 2)	
8					100			100			100		nA	V_{DS} = 25V, V_{GS} = 0	
9		$I_{D(on)}$	ON-State Drain Current	1.0	2		1.0	2		1.0	2		A	V_{DS} = 25V, V_{GS} = 10V	(Note 1)
10		$V_{DS(on)}$	Drain-Source Saturation Voltage		0.3			0.3			0.4		V	V_{GS} = 5V, I_D = 0.1A	
11					1.0	1.5		1.0	1.5		1.4	1.7		V_{GS} = 5V, I_D = 0.3A	
12					1.0			1.0			1.3			V_{GS} = 10V, I_D = 0.5A	
13					2.2	3.0		2.2	3.0		2.2	4.0		V_{GS} = 10V, I_D = 1.0A	
14	DYNAMIC	g_{fs}	Forward Transconductance	150	250		150	250		150	250		m℧	V_{DS} = 24V, I_D = 0.5A	
15		C_{iss}	Input Capacitance			50			50			50	pF	V_{GS} = 0, V_{DS} = 25V, f = 1.0MHz	(Note 2)
16		C_{rss}	Reverse Transfer Capacitance			10			10			10			
17		C_{oss}	Common-Source Output Capacitance			50			50			50			
18		$t_{d(on)}$	Turn-ON Delay Time		2	5		2	5		2	5	ns		
19		t_r	Rise Time		2	5		2	5		2	5			
20		$t_{d(off)}$	Turn-OFF Delay Time		2	5		2	5		2	5			
21		t_f	Fall Time		2	5		2	5		2	5			

Note 1. Pulse test — 80μs pulse, 1% duty cycle. **Note 2.** Sample test.

2

THERMAL RESPONSE

POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE

DC SAFE OPERATING REGION
Tc = 25°C

INTERSIL

IVN5000SND, IVN5000SNE, IVN5000SNF, IVN5001SND, IVN5001SNE, IVN5001SNF n-Channel Enhancement-mode VMOS Power FETs

PRELIMINARY

FEATURES

- High speed, high current switching
- High gain-bandwidth product
- Inherently temperature stable
- Extended Safe Operating Area
- DC biasing relatively simple
- Requires almost zero current drive

APPLICATIONS

- Switching power supplies
- DC to DC inverters
- High gain, broad-band VHF/UHF Amplifiers
- Line drivers
- Logic buffers
- Pulse amplifiers

ABSOLUTE MAXIMUM RATINGS

(25°C unless otherwise noted)

Drain-source Voltage
- IVN5000SND, IVN5001SND 40V
- IVN5000SNE, IVN5000SNE 60V
- IVN5000SNF, IVN5001SNF 80V

Drain-gate Voltage
- IVN5000SND, IVN5001SND 40V
- IVN5000SNE, IVN5001SNE 60V
- IVN5000SNF, IVN5001SNF 80V

Continuous Drain Current (see note 1) 0.9A
Peak Drain Current (see note 2) 3.0A
Gate-source Forward Voltage ..... +30V
Gate-source Reverse Voltage ..... −30V
Thermal Resistance, Junction to Case ..... 40°C/W
Continuous Device Dissipation at (or below)
- 25°C Case Temperature 3.13W

Linear Derating Factor ..... 25mW/°C
Operating Junction
- Temperature Range ..... −55 to +150°C

Storage Temperature Range ..... −55 to +150°C
Lead Temperature
- (1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $R_{DS(on)}$ and maximum power dissipation.

Note 2. Maximum pulse width 80μsec, maximum duty cycle 1.0%.

SCHEMATIC DIAGRAM

Body internally connected to source
Drain common to case

PACKAGE DIMENSIONS

PKG: JEDEC TO-52

Dimensions shown in inches and *(mm)*.

IVN5000SND, IVN5000SNE, IVN5000SNF, IVN50001SND, IVN5001SNE, IVN50001SNF

INTERSIL

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), V_{BS} = 0

		CHARACTERISTICS			IVN5000SND IVN5001SND			IVN5000SNE IVN5001SNE			IVN5000SNF INV5001SNF			UNIT	TEST CONDITIONS	
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage		40			60			80			V	V_{GS} = 0, I_D = 10μA	
2	STATIC	$V_{GS(th)}$	Gate Threshold Voltage	IVN5000 Series	0.8		2.0	0.8		2.0	0.8		2.0	V	V_{DS} = V_{GS}, I_D = 1mA	
3	STATIC	$V_{GS(th)}$	Gate Threshold Voltage	IVN5001 Series	0.8		3.6	0.8		3.6	0.8		3.6	V	V_{DS} = V_{GS}, I_D = 1mA	
4	STATIC	I_{GSS}	Gate-Body Leakage			0.1	10		0.1	10		0.1	10	nA	V_{GS} = 15V, V_{DS} = 0	
5	STATIC	I_{GSS}	Gate-Body Leakage				50			50			50	nA	V_{GS} = 15V, V_{DS} = 0, T_A = +125°C	
6	STATIC	I_{DSS}	Zero Gate Voltage Drain Current				10			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0	
7	STATIC	I_{DSS}	Zero Gate Voltage Drain Current				500			500			500	μA	V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = +125°C	
8	STATIC	I_{DSS}	Zero Gate Voltage Drain Current			20			20			20		nA	V_{DS} = 24V, V_{GS} = 0	
9	STATIC	$I_{D(on)}$	ON-State Drain Current	IVN5000 Series	1.0	1.9		1.0	1.9		1.0	1.9		A	V_{DS} = 24V, V_{GS} = 10V	
10	STATIC	$I_{D(on)}$	ON-State Drain Current	IVN5001 Series	1.0	1.9		1.0	1.9		1.0	1.9		A	V_{DS} = 24V, V_{GS} = 12V	
11	STATIC	$V_{DS(on)}$	Drain-Source Saturation Voltage	IVN5000SND IVN5000SNE IVN5000SNF		1.5			1.5			1.5		V	V_{GS} = 5V, I_D = 0.3A	
12	STATIC	$V_{DS(on)}$	Drain-Source Saturation Voltage	IVN5000SND IVN5000SNE IVN5000SNF		2.0	2.5		2.0	2.5		2.0	2.5	V	V_{GS} = 10V, I_D = 1.0A	
13	STATIC	$V_{DS(on)}$	Drain-Source Saturation Voltage	IVN5001SND INV5001SNE IVN5001SNF		1.2			1.2			1.2		V	V_{GS} = 7V, I_D = 0.3A	
14	STATIC	$V_{DS(on)}$	Drain-Source Saturation Voltage	IVN5001SND INV5001SNE IVN5001SNF		1.9	2.5		1.9	2.5		1.9	2.5	V	V_{GS} = 12V, I_D = 1.0A	
15	STATIC	$r_{DS(on)}$	Static Drain-Source ON Resistance	IVN5000 Series		2.0	2.5		2.0	2.5		2.0	2.5	Ω	V_{GS} = 10V	I_D = 1.0A (Note 1)
16	STATIC	$r_{DS(on)}$	Static Drain-Source ON Resistance	IVN5001 Series		1.9	2.5		1.9	2.5		1.9	2.5	Ω	V_{GS} = 12V	I_D = 1.0A (Note 1)
17	DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance	IVN5000 Series		2.0	2.5		2.0	2.5		2.0	2.5	Ω	V_{GS} = 10V	I_D = 1.0A, f = 1KHz (Note 1)
18	DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance	IVN5001 Series		1.9	2.5		1.9	2.5		1.9	2.5	Ω	V_{GS} = 12V	I_D = 1.0A, f = 1KHz (Note 1)
19	DYNAMIC	g_{fs}	Forward Transconductance		170		280	170	280		170	280		m℧	V_{DS} = 24V, I_D = 0.5A, f = 1KHz	(Note 1)
20	DYNAMIC	C_{iss}	Input Capacitance			40	50		40	50		40	50	pF	V_{DS} = 24V, V_{GS} = 0 f = 1MHz	(Note 2)
21	DYNAMIC	C_{oss}	Output Capacitance			27	40		27	40		27	40	pF	V_{DS} = 24V, V_{GS} = 0 f = 1MHz	(Note 2)
22	DYNAMIC	C_{rss}	Reverse Transfer Capacitance			6	10		6	10		6	10	pF	V_{DS} = 24V, V_{GS} = 0 f = 1MHz	(Note 2)
23	DYNAMIC	$t_{d(on)}$	Turn-ON Delay Time				5			5			5	ns	See Switching Times Test Circuit	(Note 2)
24	DYNAMIC	t_r	Rise Time				5			5			5	ns	See Switching Times Test Circuit	(Note 2)
25	DYNAMIC	$t_{d(off)}$	Turn-OFF Delay Time				5			5			5	ns	See Switching Times Test Circuit	(Note 2)
26	DYNAMIC	t_f	Fall Time				5			5			5	ns	See Switching Times Test Circuit	(Note 2)

Note 1. Pulse test — 80μsec, 1% duty cycle.
Note 2. Sample test.

THERMAL RESPONSE

DC SAFE OPERATING REGION
T_C = 25°C

POWER DISSIPATION DERATING

PRELIMINARY
Notice: This is not a final specification. Parametric limits are subject to change.

TYPICAL PERFORMANCE CURVES (25°C unless otherwise noted)

OUTPUT CHARACTERISTICS

SATURATION CHARACTERISTICS

TRANSFER CHARACTERISTIC

NORMALIZED DRAIN-SOURCE ON RESISTANCE vs TEMPERATURE

CAPACITANCE vs DRAIN-SOURCE VOLTAGE

OUTPUT CONDUCTANCE vs DRAIN CURRENT

2

IVN5000SND, IVN5000SNE, IVN5000SNF, IVN50001SND, IVN5001SNE, IVN50001SNF

PRELIMINARY This is not a final specification. Some parameters and limits are subject to change.

DRAIN-SOURCE ON RESISTANCE vs GATE-SOURCE VOLTAGE

TRANSCONDUCTANCE vs DRAIN CURRENT

TRANSCONDUCTANCE vs GATE-SOURCE VOLTAGE

2

SWITCHING TIME TEST CIRCUIT

SWITCHING TIME TEST WAVEFORMS

INTERSIL

IVN5000AND, IVN5000ANE, IVN5000ANF, IVN5001AND, IVN5001ANE, IVN5001ANF n-Channel Enhancement-mode VMOS Power FETs

PRELIMINARY

PRELIMINARY Notice: This is not a final specification. Some parametric limits are subject to change.

FEATURES

- High speed, high peak current switching
- Inherent current sharing capability when paralleled
- Directly interfaces to CMOS, DTL, TTL logic
- Simple, straight-forward DC biasing
- Inherent protection from thermal runaway
- Reliable, low cost plastic package

APPLICATIONS

- LED and lamp drivers
- High gain, wide-band amplifiers
- High speed switches
- Line drivers
- Logic buffers
- Pulse amplifiers

ABSOLUTE MAXIMUM RATINGS

(25°C unless otherwise noted)

Drain-source Voltage	
IVN5000AND, IVN5001AND	40V
IVN5000ANE, IVN5000ANE	60V
IVN5000ANF, IVN5001ANF	80V
Drain-gate Voltage	
IVN5000AND, IVN5001AND	40V
IVN5000ANE, IVN5001ANE	60V
IVN5000ANF, IVN5001ANF	80V
Continuous Drain Current (see note 1)	0.7A
Peak Drain Current (see note 2)	2.0A
Gate-source Forward Voltage	+30V
Gate-source Reverse Voltage	−30V
Thermal Resistance, Junction to Case	62.5°C/W
Continuous Device Dissipation at (or below) 25°C Case Temperature	2.0W
Linear Derating Factor	16mW/°C
Operating Junction Temperature Range	−40 to +150°C
Storage Temperature Range	−40 to +150°C
Lead Temperature (1/16 in. from case for 10 sec)	+300°C

Note 1. T_C = 25°C; controlled by typical $R_{DS(on)}$ and maximum power dissipation.

Note 2. Maximum pulse width 80μsec, maximum duty cycle 1.0%.

SCHEMATIC DIAGRAM

Body internally connected to source
Drain common to tab

PACKAGE DIMENSIONS

PKG: JEDEC TO-237

NOTE 1: Leads solder dipped or tin plated.
Dimensions shown in inches and *(mm)*.

2

IVN5000AND, IVN5000ANE, IVN5000ANF, IVN50001AND, IVN5001ANE, IVN50001ANF

INTERSIL

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), V_{BS} = 0

		CHARACTERISTICS		IVN5000AND IVN5001AND			IVN5000ANE IVN5001ANE			IVN5000ANF INV5001ANF			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS} Drain-Source Breakdown Voltage		40			60			80			V	V_{GS} = 0, I_D = 10μA	
2	STATIC	$V_{GS(th)}$ Gate Threshold Voltage	IVN5000 Series	0.8		2.0	0.8		2.0	0.8		2.0	V	V_{DS} = V_{GS}, I_D = 1mA	
3	STATIC	$V_{GS(th)}$ Gate Threshold Voltage	IVN5001 Series	0.8		3.6	0.8		3.6	0.8		3.6	V	V_{DS} = V_{GS}, I_D = 1mA	
4	STATIC	I_{GSS} Gate-Body Leakage			0.1	10		0.1	10		0.1	10	nA	V_{GS} = 15V, V_{DS} = 0	
5	STATIC	I_{GSS} Gate-Body Leakage				50			50			50	nA	V_{GS} = 15V, V_{DS} = 0, T_A = +125°C	
6	STATIC	I_{DSS} Zero Gate Voltage Drain Current				10			10			10	μA	V_{DS} = Max. Rating, V_{GS} = 0	
7	STATIC	I_{DSS} Zero Gate Voltage Drain Current				500			500			500	μA	V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = +125°C	
8	STATIC	I_{DSS} Zero Gate Voltage Drain Current			20			20			20		nA	V_{DS} = 24V, V_{GS} = 0	
9	STATIC	$I_{D(on)}$ ON-State Drain Current	IVN5000 Series	1.0	1.9		1.0	1.9		1.0	1.9		A	V_{DS} = 24V, V_{GS} = 10V	
10	STATIC	$I_{D(on)}$ ON-State Drain Current	IVN5001 Series	1.0	1.9		1.0	1.9		1.0	1.9		A	V_{DS} = 24V, V_{GS} = 12V	
11	STATIC	$V_{DS(on)}$ Drain-Source Saturation Voltage	IVN5000AND IVN5000ANE IVN5000ANF		1.5			1.5			1.5		V	V_{GS} = 5V, I_D = 0.3A	
12	STATIC	$V_{DS(on)}$ Drain-Source Saturation Voltage	IVN5000AND IVN5000ANE IVN5000ANF		2.0	2.5		2.0	2.5		2.0	2.5	V	V_{GS} = 10V, I_D = 1.0A	
13	STATIC	$V_{DS(on)}$ Drain-Source Saturation Voltage	IVN5001AND INV5001ANE IVN5001ANF		1.2			1.2			1.2		V	V_{GS} = 7V, I_D = 0.3A	
14	STATIC	$V_{DS(on)}$ Drain-Source Saturation Voltage	IVN5001AND INV5001ANE IVN5001ANF		1.9	2.5		1.9	2.5		1.9	2.5	V	V_{GS} = 12V, I_D = 1.0A	
15	STATIC	$r_{DS(on)}$ Static Drain-Source ON Resistance	IVN5000 Series		2.0	2.5		2.0	2.5		2.0	2.5	Ω	V_{GS} = 10V	I_D = 1.0A
16	STATIC	$r_{DS(on)}$ Static Drain-Source ON Resistance	IVN5001 Series		1.9	2.5		1.9	2.5		1.9	2.5	Ω	V_{GS} = 12V	I_D = 1.0A
17	DYNAMIC	$r_{ds(on)}$ Small-Signal Drain-Source ON Resistance	IVN5000 Series		2.0	2.5		2.0	2.5		2.0	2.5	Ω	V_{GS} = 10V	I_D = 1.0A, f = 1KHz
18	DYNAMIC	$r_{ds(on)}$ Small-Signal Drain-Source ON Resistance	IVN5001 Series		1.9	2.5		1.9	2.5		1.9	2.5	Ω	V_{GS} = 12V	I_D = 1.0A, f = 1KHz
19	DYNAMIC	g_{fs} Forward Transconductance		170		280	170	280		170	280		m℧	V_{DS} = 24V, I_D = 0.5A, f = 1KHz	
20	DYNAMIC	C_{iss} Input Capacitance			40	50		40	50		40	50	pF	V_{DS} = 24V, V_{GS} = 0 f = 1MHz	(Note 2)
21	DYNAMIC	C_{oss} Output Capacitance			27	40		27	40		27	40	pF	V_{DS} = 24V, V_{GS} = 0 f = 1MHz	(Note 2)
22	DYNAMIC	C_{rss} Reverse Transfer Capacitance			6	10		6	10		6	10	pF	V_{DS} = 24V, V_{GS} = 0 f = 1MHz	(Note 2)
23	DYNAMIC	$t_{d(on)}$ Turn-ON Delay Time				5			5			5	ns	See Switching Times Test Circuit	(Note 2)
24	DYNAMIC	t_r Rise Time				5			5			5	ns	See Switching Times Test Circuit	(Note 2)
25	DYNAMIC	$t_{d(off)}$ Turn-OFF Delay Time				5			5			5	ns	See Switching Times Test Circuit	(Note 2)
26	DYNAMIC	t_f Fall Time				5			5			5	ns	See Switching Times Test Circuit	(Note 2)

Note 1. Pulse test — 80μsec, 1% duty cycle.
Note 2. Sample test.

THERMAL RESPONSE

DC SAFE OPERATING REGION

T_C = 25°C

POWER DISSIPATION DERATING

IVN5000AND, IVN5000ANE, IVN5000ANF, IVN50001AND, IVN5001ANE, IVN50001ANF

INTERSIL

TYPICAL PERFORMANCE CURVES (25°C unless otherwise noted)

OUTPUT CHARACTERISTICS

SATURATION CHARACTERISTICS

TRANSFER CHARACTERISTIC

NORMALIZED DRAIN-SOURCE ON RESISTANCE vs TEMPERATURE

CAPACITANCE vs DRAIN-SOURCE VOLTAGE

OUTPUT CONDUCTANCE vs DRAIN CURRENT

2

INTERSIL

DRAIN-SOURCE ON RESISTANCE vs GATE-SOURCE VOLTAGE

TRANSCONDUCTANCE vs DRAIN CURRENT

TRANSCONDUCTANCE vs GATE-SOURCE VOLTAGE

2

SWITCHING TIME TEST CIRCUIT

SWITCHING TIME TEST WAVEFORMS

INTERSIL

IVN5200KND, IVN5201KND, IVN5200KNE, IVN5201KNE, IVN5200KNF, IVN5201KNF n-Channel Enhancement-mode VMOS Power FETs

PRELIMINARY

FEATURES

- High speed, high current switching
- Inherent current sharing capability when paralleled
- Extremely low drive currents
- Simple, straight-forward DC biasing
- Extended safe operating area
- Inherently temperature stable

APPLICATIONS

- Switching power supplies
- DC to DC inverters
- CMOS and TTL to high current logic
- High current line drivers
- Motor controllers
- Power amplifiers

ABSOLUTE MAXIMUM RATINGS
(25°C unless otherwise noted)

Drain-source Voltage
- IVN5200KND, IVN5201KND 40V
- IVN5200KNE, IVN5201KNE 60V
- IVN5200KNF, IVN5201KNF 80V

Drain-gate Voltage
- IVN5200KND, IVN5201KND 40V
- IVN5200KNE, IVN5201KNE 60V
- IVN5200KNF, IVN5201KNF 80V

Continuous Drain Current 5.0A
Peak Drain Current (see note 1) 12A
Gate-source Forward Voltage ..... +30V
Gate-source Reverse Voltage ..... −30V
Thermal Resistance, Junction to Case ..... 2.5°C/W
Continuous Device Dissipation at (or below)
- 25°C Case Temperature 50W

Linear Derating Factor ..... 400mW/°C
Operating Junction
- Temperature Range ..... −55 to +150°C

Storage Temperature Range ..... −55 to +150°C
Lead Temperature
- (1/16 in. from case for 10 sec) ..... +300°C

Note 1. Maximum pulse width 80μsec, maximum duty cycle 1.0%.

SCHEMATIC DIAGRAM

Body internally connected to source
Drain common to case

PACKAGE DIMENSIONS

PKG: JEDEC TO-3

Dimensions shown in inches and *(mm)*.

2

IVN5200KND, IVN5201KND, IVN5200KNE, IVN5201KNE, IVN5200KNF, IVN5201KNF

INTERSIL

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), V_{BS} = 0

		CHARACTERISTICS		IVN5200KND IVN5201KND			IVN5200KNE IVN5201KNE			IVN5200KNF INV5201KNF			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS} Drain-Source Breakdown Voltage		40			60			80			V	V_{GS} = 0, I_D = 100μA	
2		$V_{GS(th)}$ Gate Threshold Voltage	IVN5200 Series	0.8		2.0	0.8		2.0	0.8		2.0	V	V_{DS} = V_{GS}, I_D = 5mA	
3			IVN5201 Series	0.8		3.6	0.8		3.6	0.8		3.6	V		
4		I_{GSS} Gate-Body Leakage			0.2	20		0.2	20		0.2	20	nA	V_{GS} = 12V, V_{DS} = 0	
5						100			100			100	nA	V_{GS} = 12V, V_{DS} = 0, T_A = +125°C	
6		I_{DSS} Zero Gate Voltage Drain Current				100			100			100	μA	V_{DS} = Max. Rating, V_{GS} = 0	
7						5.0			5.0			5.0	mA	V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = +125°C	
8					100			100			100		nA	V_{DS} = 24V, V_{GS} = 0	
9		$I_{D(on)}$ ON-State Drain Current	IVN5200 Series	5.0	10		5.0	10		5.0	10		A	V_{DS} = 24V, V_{GS} = 10V	
10			IVN5201 Series	5.0	10		5.0	10		5.0	10		A	V_{DS} = 24V, V_{GS} = 12V	
11		$V_{DS(on)}$ Drain-Source Saturation Voltage	IVN5200KND IVN5200KNE IVN5200KNF		1.5			1.5			1.5		V	V_{GS} = 5V, I_D = 2.0A	
12					1.9	2.5		1.9	2.5		1.9	2.5	V	V_{GS} = 10V, I_D = 5.0A	
13			IVN5201KND INV5201KNE IVN5201KNF		1.2			1.2			1.2		V	V_{GS} = 7V, I_D = 2.0A	
14					1.8	2.5		1.8	2.5		1.8	2.5	V	V_{GS} = 12V, I_D = 5.0A	(Note 1)
15		$r_{DS(on)}$ Static Drain-Source ON Resistance	IVN5200 Series		0.38	0.50		0.38	0.50		0.38	0.50	Ω	V_{GS} = 10V, I_D = 5.0A	
16			IVN5201 Series		0.36	0.50		0.36	0.50		0.36	0.50	Ω	V_{GS} = 12V, I_D = 5.0A	
17	DYNAMIC	$r_{ds(on)}$ Small-Signal Drain-Source ON Resistance	IVN5200 Series		0.38	0.50		0.38	0.50		0.38	0.50	Ω	V_{GS} = 10V, I_D = 5.0A, f = 1KHz	
18			IVN5201 Series		0.36	0.50		0.36	0.50		0.36	0.50	Ω	V_{GS} = 12V, I_D = 5.0A, f = 1KHz	
19		g_{fs} Forward Transconductance		1.0	1.8		1.0	1.8		1.0	1.8		mho	V_{DS} = 24V, I_D = 5.0A, f = 1KHz	
20		C_{iss} Input Capacitance			210	250		210	250		210	250	pF	V_{DS} = 24V, V_{GS} = 0, f = 1MHz	(Note 2)
21		C_{oss} Output Capacitance			160	200		160	200		160	200	pF		
22		C_{rss} Reverse Transfer Capacitance			45	60		45	60		45	60	pF		
23		$t_{d(on)}$ Turn-ON Delay Time				20			20			20	ns	See Switching Times Test Circuit I_D = 4.0A	(Note 2)
24		t_r Rise Time				20			20			20	ns		
25		$t_{d(off)}$ Turn-OFF Delay Time				20			20			20	ns		
26		t_f Fall Time				20			20			20	ns		

Note 1. Pulse test — 80μsec, 1% duty cycle.
Note 2. Sample test.

THERMAL RESPONSE

POWER DISSIPATION vs CASE TEMPERATURE

DC SAFE OPERATING REGION T_C = 25°C

IVN5200KND, IVN5201KND, IVN5200KNE, IVN5201KNE, IVN5200KNF, IVN5201KNF

INTERSIL

TYPICAL PERFORMANCE CURVES (25°C unless otherwise noted)

OUTPUT CHARACTERISTICS

SATURATION CHARACTERISTICS

TRANSFER CHARACTERISTIC

NORMALIZED DRAIN-SOURCE ON RESISTANCE vs TEMPERATURE

CAPACITANCE vs DRAIN-SOURCE VOLTAGE

OUTPUT CONDUCTANCE vs DRAIN CURRENT

2

PRELIMINARY DATA Intersil reserves the right to make changes in specifications at any time without notice. The data sheet is not a final specification. Some parameters are subject to change.

DRAIN-SOURCE ON RESISTANCE vs GATE-SOURCE VOLTAGE

TRANSCONDUCTANCE vs DRAIN CURRENT

TRANSCONDUCTANCE vs GATE-SOURCE VOLTAGE

2

SWITCHING TIME TEST CIRCUIT

SWITCHING TIME TEST WAVEFORMS

INTERSIL

IVN5200TND, IVN5201TND, IVN5200TNE, IVN5201TNE, IVN5200TNF, IVN5201TNF n-Channel Enhancement-mode VMOS Power FETs

PRELIMINARY

FEATURES

- High speed, high current switching
- Inherent current sharing capability when paralleled
- Directly interfaces to CMOS, DTL, TTL logic
- Simple, straight-forward DC biasing
- Extended safe operating area
- Inherently temperature stable

APPLICATIONS

- High efficiency switching power supplies
- Off-line switching regulators
- High speed, high current switches
- Line drivers
- Logic buffers
- High peak current pulse amplifiers

ABSOLUTE MAXIMUM RATINGS
(25°C unless otherwise noted)

Drain-source Voltage
- IVN5200TND, IVN5201TND 40V
- IVN5200TNE, IVN5201TNE 60V
- IVN5200TNF, IVN5201TNF 80V

Drain-gate Voltage
- IVN5200TND, IVN5201TND 40V
- IVN5200TNE, IVN5201TNE 60V
- IVN5200TNF, IVN5201TNF 80V

Continuous Drain Current (see note 1) 4.0A
Peak Drain Current (see note 2) 10A
Gate-source Forward Voltage ..... +30V
Gate-source Reverse Voltage ..... −30V
Thermal Resistance, Junction to Case ..... 10°C/W
Continuous Device Dissipation at (or below)
- 25°C Case Temperature 12.5W

Linear Derating Factor ..... 100mW/°C
Operating Junction
- Temperature Range ..... −55 to +150°C

Storage Temperature Range ..... −55 to +150°C
Lead Temperature
- (1/16 in. from case for 10 sec) ..... +300°C

Note 1. T_C = 25°C; controlled by typical $R_{DS(on)}$ and maximum power dissipation.

Note 2. Pulse width 80μsec, duty cycle 1.0%.

SCHEMATIC DIAGRAM

Body internally connected to source
Drain common to case

PACKAGE DIMENSIONS

PKG: JEDEC TO-39

Dimensions shown in inches and *(mm)*.

IVN5200TND, IVN5201TND, IVN5200TNE, IVN5201TNE, IVN5200TNF, IVN5201TNF

INTERSIL

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), V_{BS} = 0

		CHARACTERISTICS		IVN5200TND IVN5201TND MIN	TYP	MAX	IVN5200TNE IVN5201TNE MIN	TYP	MAX	IVN5200TNF INV5201TNF MIN	TYP	MAX	UNIT	TEST CONDITIONS	
1	STATIC	BV_{DSS} Drain-Source Breakdown Voltage		40			60			80			V	V_{GS} = 0, I_D = 100μA	
2	STATIC	$V_{GS(th)}$ Gate Threshold Voltage	IVN5200 Series	0.8		2.0	0.8		2.0	0.8		2.0	V	V_{DS} = V_{GS}, I_D = 5mA	
3	STATIC	$V_{GS(th)}$ Gate Threshold Voltage	IVN5201 Series	0.8		3.6	0.8		3.6	0.8		3.6	V	V_{DS} = V_{GS}, I_D = 5mA	
4	STATIC	I_{GSS} Gate-Body Leakage			0.2	20		0.2	20		0.2	20	nA	V_{GS} = 12V, V_{DS} = 0	
5	STATIC	I_{GSS} Gate-Body Leakage				100			100			100	nA	V_{GS} = 12V, V_{DS} = 0, T_A = +125°C	
6	STATIC	I_{DSS} Zero Gate Voltage Drain Current				100			100			100	μA	V_{DS} = Max. Rating, V_{GS} = 0	
7	STATIC	I_{DSS} Zero Gate Voltage Drain Current				5.0			5.0			5.0	mA	V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = +125°C	
8	STATIC	I_{DSS} Zero Gate Voltage Drain Current			100			100			100		nA	V_{DS} = 24V, V_{GS} = 0	
9	STATIC	$I_{D(on)}$ ON-State Drain Current	IVN5200 Series	5.0	10		5.0	10		5.0	10		A	V_{DS} = 24V, V_{GS} = 10V	
10	STATIC	$I_{D(on)}$ ON-State Drain Current	IVN5201 Series	5.0	10		5.0	10		5.0	10		A	V_{DS} = 24V, V_{GS} = 12V	
11	STATIC	$V_{DS(on)}$ Drain-Source Saturation Voltage	IVN5200TND IVN5200TNE IVN5200TNF		1.5			1.5			1.5		V	V_{GS} = 5V, I_D = 2.0A	
12	STATIC	$V_{DS(on)}$ Drain-Source Saturation Voltage	IVN5200TND IVN5200TNE IVN5200TNF		1.9	2.5		1.9	2.5		1.9	2.5	V	V_{GS} = 10V, I_D = 5.0A	
13	STATIC	$V_{DS(on)}$ Drain-Source Saturation Voltage	IVN5201TND INV5201TNE IVN5201TNF		1.2			1.2			1.2		V	V_{GS} = 7V, I_D = 2.0A	
14	STATIC	$V_{DS(on)}$ Drain-Source Saturation Voltage	IVN5201TND INV5201TNE IVN5201TNF		1.8	2.5		1.8	2.5		1.8	2.5	V	V_{GS} = 12V, I_D = 5.0A	(Note 1)
15	STATIC	$r_{DS(on)}$ Static Drain-Source ON Resistance	IVN5200 Series		0.38	0.50		0.38	0.50		0.38	0.50	Ω	V_{GS} = 10V	I_D = 5.0A
16	STATIC	$r_{DS(on)}$ Static Drain-Source ON Resistance	IVN5201 Series		0.36	0.50		0.36	0.50		0.36	0.50	Ω	V_{GS} = 12V	I_D = 5.0A
17	DYNAMIC	$r_{ds(on)}$ Small-Signal Drain-Source ON Resistance	IVN5200 Series		0.38	0.50		0.38	0.50		0.38	0.50	Ω	V_{GS} = 10V	I_D = 5.0A, f = 1KHz
18	DYNAMIC	$r_{ds(on)}$ Small-Signal Drain-Source ON Resistance	IVN5201 Series		0.36	0.50		0.36	0.50		0.36	0.50	Ω	V_{GS} = 12V	I_D = 5.0A, f = 1KHz
19	DYNAMIC	g_{fs} Forward Transconductance		1.0	1.8		1.0	1.8		1.0	1.8		mho	V_{DS} = 24V, I_D = 5.0A, f = 1KHz	
20	DYNAMIC	C_{iss} Input Capacitance			210	250		210	250		210	250	pF	V_{DS} = 24V, V_{GS} = 0, f = 1MHz	(Note 2)
21	DYNAMIC	C_{oss} Output Capacitance			160	200		160	200		160	200	pF	V_{DS} = 24V, V_{GS} = 0, f = 1MHz	(Note 2)
22	DYNAMIC	C_{rss} Reverse Transfer Capacitance			45	60		45	60		45	60	pF	V_{DS} = 24V, V_{GS} = 0, f = 1MHz	(Note 2)
23	DYNAMIC	$t_{d(on)}$ Turn-ON Delay Time				20			20			20	ns	See Switching Times Test Circuit I_D = 4.0A	(Note 2)
24	DYNAMIC	t_r Rise Time				20			20			20	ns	See Switching Times Test Circuit I_D = 4.0A	(Note 2)
25	DYNAMIC	$t_{d(off)}$ Turn-OFF Delay Time				20			20			20	ns	See Switching Times Test Circuit I_D = 4.0A	(Note 2)
26	DYNAMIC	t_f Fall Time				20			20			20	ns	See Switching Times Test Circuit I_D = 4.0A	(Note 2)

Note 1. Pulse test — 80μsec, 1% duty cycle.
Note 2. Sample test.

THERMAL RESPONSE

POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE

DC SAFE OPERATING REGION Tc = 25°C

IVN5200TND, IVN5201TND, IVN5200TNE, IVN5201TNE, IVN5200TNF, IVN5201TNF

INTERSIL

TYPICAL PERFORMANCE CURVES (25°C unless otherwise noted)

OUTPUT CHARACTERISTICS

SATURATION CHARACTERISTICS

TRANSFER CHARACTERISTIC

NORMALIZED DRAIN-SOURCE ON RESISTANCE vs TEMPERATURE

CAPACITANCE vs DRAIN-SOURCE VOLTAGE

OUTPUT CONDUCTANCE vs DRAIN CURRENT

2

PRELIMINARY Information Only This product is not a standard product. Specifications are subject to change without notice.

DRAIN-SOURCE ON RESISTANCE vs GATE-SOURCE VOLTAGE

TRANSCONDUCTANCE vs DRAIN CURRENT

TRANSCONDUCTANCE vs GATE-SOURCE VOLTAGE

SWITCHING TIME TEST CIRCUIT

SWITCHING TIME TEST WAVEFORMS

INTERSIL

IVN5200HND, IVN5201HND, IVN5200HNE, IVN5201HNE, IVN5200HNF, IVN5201HNF n-Channel Enhancement-mode VMOS Power FETs

PRELIMINARY

FEATURES

- High speed, high current switching
- Inherent current sharing capability when paralleled
- Directly interfaces to CMOS, DTL, TTL logic
- Simple, straight-forward DC biasing
- Extended safe operating area
- Inherently temperature stable

APPLICATIONS

- Switching power supplies
- DC to DC inverters
- Logic buffers
- Line drivers
- Motor controllers
- Power amplifiers

ABSOLUTE MAXIMUM RATINGS

(25°C unless otherwise noted)

Drain-source Voltage
- IVN5200HND, IVN5201HND 40V
- IVN5200HNE, IVN5201HNE 60V
- IVN5200HNF, IVN5201HNF 80V

Drain-gate Voltage
- IVN5200HND, IVN5201HND 40V
- IVN5200HNE, IVN5201HNE 60V
- IVN5200HNF, IVN5201HNF 80V

Continuous Drain Current 5.0A
Peak Drain Current (see note 1) 12A
Gate-source Forward Voltage ..... +30V
Gate-source Reverse Voltage ..... −30V
Thermal Resistance, Junction to Case ..... 4.17°C/W
Continuous Device Dissipation at (or below)
25°C Case Temperature 30W
Linear Derating Factor ..... 240mW/°C
Operating Junction
Temperature Range ..... −55 to +150°C
Storage Temperature Range ..... −55 to +150°C
Lead Temperature
(1/16 in. from case for 10 sec) ..... +300°C

Note Maximum pulse width 80μsec, maximum duty cycle 1.0%.

SCHEMATIC DIAGRAM

Body internally connected to source.
Drain common to case.

PACKAGE DIMENSIONS

PKG: JEDEC TO-66

Dimensions shown in inches and *(mm)*.

IVN5200HND, IVN5201HND, IVN5200HNE, IVN5201HNE, IVN5200HNF, IVN5201HNF

INTERSIL

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), V_{BS} = 0

		CHARACTERISTICS			IVN5200HND IVN5201HND			IVN5200HNE IVN5201HNE			IVN5200HNF INV5201HNF			UNIT	TEST CONDITIONS	
					MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage		40			60			80			V	V_{GS} = 0, I_D = 100μA	
2	STATIC	$V_{GS(th)}$	Gate Threshold Voltage	IVN5200 Series	0.8		2.0	0.8		2.0	0.8		2.0	V	V_{DS} = V_{GS}, I_D = 5mA	
3	STATIC	$V_{GS(th)}$	Gate Threshold Voltage	IVN5201 Series	0.8		3.6	0.8		3.6	0.8		3.6	V	V_{DS} = V_{GS}, I_D = 5mA	
4	STATIC	I_{GSS}	Gate-Body Leakage			0.2	20		0.2	20		0.2	20	nA	V_{GS} = 12V, V_{DS} = 0	
5	STATIC	I_{GSS}	Gate-Body Leakage				100			100			100	nA	V_{GS} = 12V, V_{DS} = 0, T_A = +125°C	
6	STATIC	I_{DSS}	Zero Gate Voltage Drain Current				100			100			100	μA	V_{DS} = Max. Rating, V_{GS} = 0	
7	STATIC	I_{DSS}	Zero Gate Voltage Drain Current				5.0			5.0			5.0	mA	V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = +125°C	
8	STATIC	I_{DSS}	Zero Gate Voltage Drain Current			100			100			100		nA	V_{DS} = 24V, V_{GS} = 0	
9	STATIC	$I_{D(on)}$	ON-State Drain Current	IVN5200 Series	5.0	10		5.0	10		5.0	10		A	V_{DS} = 24V, V_{GS} = 10V	
10	STATIC	$I_{D(on)}$	ON-State Drain Current	IVN5201 Series	5.0	10		5.0	10		5.0	10		A	V_{DS} = 24V, V_{GS} = 12V	
11	STATIC	$V_{DS(on)}$	Drain-Source Saturation Voltage	IVN5200HND IVN5200HNE IVN5200HNF		1.5			1.5			1.5		V	V_{GS} = 5V, I_D = 2.0A	(Note 1)
12	STATIC	$V_{DS(on)}$	Drain-Source Saturation Voltage	IVN5200HND IVN5200HNE IVN5200HNF		1.9	2.5		1.9	2.5		1.9	2.5	V	V_{GS} = 10V, I_D = 5.0A	(Note 1)
13	STATIC	$V_{DS(on)}$	Drain-Source Saturation Voltage	IVN5201HND INV5201HNE IVN5201HNF		1.2			1.2			1.2		V	V_{GS} = 7V, I_D = 2.0A	(Note 1)
14	STATIC	$V_{DS(on)}$	Drain-Source Saturation Voltage	IVN5201HND INV5201HNE IVN5201HNF		1.8	2.5		1.8	2.5		1.8	2.5	V	V_{GS} = 12V, I_D = 5.0A	(Note 1)
15	STATIC	$r_{DS(on)}$	Static Drain-Source ON Resistance	IVN5200 Series		0.38	0.50		0.38	0.50		0.38	0.50	Ω	V_{GS} = 10V, I_D = 5.0A	(Note 1)
16	STATIC	$r_{DS(on)}$	Static Drain-Source ON Resistance	IVN5201 Series		0.36	0.50		0.36	0.50		0.36	0.50	Ω	V_{GS} = 12V, I_D = 5.0A	(Note 1)
17	DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance	IVN5200 Series		0.38	0.50		0.38	0.50		0.38	0.50	Ω	V_{GS} = 10V, I_D = 5.0A, f = 1KHz	(Note 1)
18	DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance	IVN5201 Series		0.36	0.50		0.36	0.50		0.36	0.50	Ω	V_{GS} = 12V, I_D = 5.0A, f = 1KHz	(Note 1)
19	DYNAMIC	g_{fs}	Forward Transconductance		1.0	1.8		1.0	1.8		1.0	1.8		mho	V_{DS} = 24V, I_D = 5.0A, f = 1KHz	(Note 1)
20	DYNAMIC	C_{iss}	Input Capacitance			210	250		210	250		210	250	pF	V_{DS} = 24V, V_{GS} = 0 f = 1MHz	(Note 2)
21	DYNAMIC	C_{oss}	Output Capacitance			160	200		160	200		160	200	pF	V_{DS} = 24V, V_{GS} = 0 f = 1MHz	(Note 2)
22	DYNAMIC	C_{rss}	Reverse Transfer Capacitance			45	60		45	60		45	60	pF	V_{DS} = 24V, V_{GS} = 0 f = 1MHz	(Note 2)
23	DYNAMIC	$t_{d(on)}$	Turn-ON Delay Time				20			20			20	ns	See Switching Times Test Circuit I_D = 4.0A	(Note 2)
24	DYNAMIC	t_r	Rise Time				20			20			20	ns	See Switching Times Test Circuit I_D = 4.0A	(Note 2)
25	DYNAMIC	$t_{d(off)}$	Turn-OFF Delay Time				20			20			20	ns	See Switching Times Test Circuit I_D = 4.0A	(Note 2)
26	DYNAMIC	t_f	Fall Time				20			20			20	ns	See Switching Times Test Circuit I_D = 4.0A	(Note 2)

Note 1. Pulse test — 80μsec, 1% duty cycle.
Note 2. Sample test.

POWER DISSIPATION vs CASE TEMPERATURE

THERMAL RESPONSE

DC SAFE OPERATING REGION Tc = 25°C

PRELIMINARY
Note: This is not a final specification. Electric limits are subject to change.

TYPICAL PERFORMANCE CURVES (25°C unless otherwise noted)

OUTPUT CHARACTERISTICS

SATURATION CHARACTERISTICS

TRANSFER CHARACTERISTIC

NORMALIZED DRAIN-SOURCE ON RESISTANCE vs TEMPERATURE

CAPACITANCE vs DRAIN-SOURCE VOLTAGE

OUTPUT CONDUCTANCE vs DRAIN CURRENT

2

PRELIMINARY
Information contained herein is not a final specification. Intersil reserves the right to change specifications and products without notice.

DRAIN-SOURCE ON RESISTANCE vs GATE-SOURCE VOLTAGE

TRANSCONDUCTANCE vs DRAIN CURRENT

TRANSCONDUCTANCE vs GATE-SOURCE VOLTAGE

2

SWITCHING TIME TEST CIRCUIT

SWITCHING TIME TEST WAVEFORMS

INTERSIL

IVN5201CND, IVN5201CNE, IVN5201CNF n-Channel Enhancement-mode VMOS Power FETs

PRELIMINARY

PRELIMINARY
Notice: This is not a final specification. Some parameters are subject to change.

FEATURES

- High speed, high current switching
- Inherent current sharing capability when paralleled
- Directly interfaces to CMOS, DTL, TTL logic
- Simple, straight-forward DC biasing
- Extended safe operating area
- Reliable, low cost plastic package

APPLICATIONS

- Deflection coil drivers
- Off-line switching regulators
- Power amplifiers
- DC to DC inverters
- Motor controllers
- High current line drivers

ABSOLUTE MAXIMUM RATINGS

(25°C unless otherwise noted)

Drain-source Voltage
- IVN5201CND 40V
- IVN5201CNE 60V
- IVN5201CNF 80V

Drain-gate Voltage
- IVN5201CND 40V
- IVN5201CNE 60V
- IVN5201CNF 80V

Continuous Drain Current 5.0A
Peak Drain Current (see note 1) 12A
Gate-source Forward Voltage ..... +30V
Gate-source Reverse Voltage ..... −30V
Thermal Resistance, Junction to Case ..... 4.17°C/W
Continuous Device Dissipation at (or below)
25°C Case Temperature 30W
Linear Derating Factor ..... 240mW/°C
Operating Junction
Temperature Range ..... −40 to +150°C
Storage Temperature Range ..... −40 to +150°C
Lead Temperature
(1/16 in. from case for 10 sec) ..... +300°C

Note 1. Maximum pulse width 80μsec, maximum duty cycle 1.0%.

SCHEMATIC DIAGRAM

Body internally connected to source.
Drain common to tab.

PACKAGE DIMENSIONS

PKG: JEDEC TO-220

Dimensions shown in inches and *(mm)*.

2

ELECTRICAL CHARACTERISTICS (25°C unless otherwise noted), V_{BS} = 0

		CHARACTERISTICS		IVN5201CND			IVN5201CNE			IVN5201CNF			UNIT	TEST CONDITIONS	
				MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX			
1	STATIC	BV_{DSS}	Drain-Source Breakdown Voltage	40			60			80			V	V_{GS} = 0, I_D = 100μA	
2	STATIC	$V_{GS(th)}$	Gate Threshold Voltage	0.8		3.6	0.8		3.6	0.8		3.6		V_{DS} = V_{GS}, I_D = 5mA	
3	STATIC	I_{GSS}	Gate-Body Leakage		0.2	20		0.2	20		0.2	20	nA	V_{GS} = 12V, V_{DS} = 0	
4	STATIC	I_{GSS}	Gate-Body Leakage			100			100			100	nA	V_{GS} = 12V, V_{DS} = 0, T_A = +125°C	
5	STATIC	I_{DSS}	Zero Gate Voltage Drain Current			100			100			100	μA	V_{DS} = Max. Rating, V_{GS} = 0	
6	STATIC	I_{DSS}	Zero Gate Voltage Drain Current			5.0			5.0			5.0	mA	V_{DS} = 0.80 Max. Rating, V_{GS} = 0, T_A = +125°C	
7	STATIC	I_{DSS}	Zero Gate Voltage Drain Current		100			100			100		nA	V_{DS} = 24V, V_{GS} = 0	
8	STATIC	$I_{D(on)}$	ON-State Drain Current	5.0	10		5.0	10		5.0	10		A	V_{DS} = 24V, V_{GS} = 12V	
9	STATIC	$V_{DS(on)}$	Drain-Source Saturation Voltage		1.2			1.2			1.2		V	V_{GS} = 7V, I_D = 2.0A	
10	STATIC	$V_{DS(on)}$	Drain-Source Saturation Voltage		1.8	2.5		1.8	2.5		1.8	2.5	V	V_{GS} = 12V, I_D = 5.0A	
11	STATIC	$r_{DS(on)}$	Static Drain-Source ON Resistance		0.36	0.50		0.36	0.50		0.36	0.50	Ω	V_{GS} = 12V, I_D = 5.0A	(Note 1)
12	DYNAMIC	$r_{ds(on)}$	Small-Signal Drain-Source ON Resistance		0.36	0.50		0.36	0.50		0.36	0.50	Ω	V_{GS} = 12V, I_D = 5.0A f = 1KHz	(Note 1)
13	DYNAMIC	g_{fs}	Forward Transconductance	1.0	1.8		1.0	1.8		1.0	1.8		mho	V_{DS} = 24V, I_D = 5.0A, f = 1KHz	(Note 1)
14	DYNAMIC	C_{iss}	Input Capacitance		210	250		210	250		210	250	pF	V_{DS} = 24V, V_{GS} = 0, f = 1MHz	(Note 2)
15	DYNAMIC	C_{oss}	Output Capacitance		160	200		160	200		160	200	pF	V_{DS} = 24V, V_{GS} = 0, f = 1MHz	(Note 2)
16	DYNAMIC	C_{rss}	Reverse Transfer Capacitance		45	60		45	60		45	60	pF	V_{DS} = 24V, V_{GS} = 0, f = 1MHz	(Note 2)
17	DYNAMIC	$t_{d(on)}$	Turn-ON Delay Time			20			20			20	ns	See Switching Times Test Circuit I_D = 4.0A	(Note 2)
18	DYNAMIC	t_r	Rise Time			20			20			20	ns	See Switching Times Test Circuit I_D = 4.0A	(Note 2)
19	DYNAMIC	$t_{d(off)}$	Turn-OFF Delay Time			20			20			20	ns	See Switching Times Test Circuit I_D = 4.0A	(Note 2)
20	DYNAMIC	t_f	Fall Time			20			20			20	ns	See Switching Times Test Circuit I_D = 4.0A	(Note 2)

Note 1. Pulse test — 80μsec, 1% duty cycle.
Note 2. Sample test.

2

THERMAL RESPONSE

POWER DISSIPATION vs CASE OR AMBIENT TEMPERATURE

DC SAFE OPERATING REGION T_C = 25°C

PRELIMINARY Note: This is not a final specification. Some parametric limits are subject to change.

TYPICAL PERFORMANCE CURVES (25°C unless otherwise noted)

OUTPUT CHARACTERISTICS

SATURATION CHARACTERISTICS

TRANSFER CHARACTERISTIC

NORMALIZED DRAIN-SOURCE ON RESISTANCE vs TEMPERATURE

CAPACITANCE vs DRAIN-SOURCE VOLTAGE

OUTPUT CONDUCTANCE vs DRAIN CURRENT

PRELIMINARY
Note: This is not a final specification. Some parametric limits are subject to change.

DRAIN-SOURCE ON RESISTANCE vs GATE-SOURCE VOLTAGE

TRANSCONDUCTANCE vs DRAIN CURRENT

TRANSCONDUCTANCE vs GATE-SOURCE VOLTAGE

SWITCHING TIME TEST CIRCUIT

SWITCHING TIME TEST WAVEFORMS

Analog Switches and Gates

Multiplexers

IH6108 3-6
IH6116 3-12
IH6208 3-18
IH6216 3-24

Analog Switch Drivers

D112/113/120/121 3-30
D123, D125 3-34
D129 3-38

Analog Switches with Drivers

DG111/112 3-40
DG116/118/123/125 3-44
DG120/121 3-48
DG126A Family 3-52
DG139A Family 3-56
DG180-191 3-60
DG426A Family 3-64
DG439A Family 3-68
IH181-185, 187-191 3-72
IH200 3-78
IH201/202 3-81
IH5001/2 3-84
IH5003/4 3-86
IH5005-7 3-88
IH5009-24 3-92
IH5025-38 3-98
IH5040-51 3-104
IH5052/3 3-114
IH5140-45 3-122
IH401/401A 3-130

Analog Switches without Drivers

G115/123 3-135
G116-119 3-139
G125-132, G1330/40/50/60 3-143
MM450/550, MM451/551, MM452/552, MM455/555 3-145

(CMOS or TTL to higher levels)

Digital Translatcr/Analog Driver

IH6201 3-147

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Analog Switches with Driver

Electrical Characteristics @ +25°C—Military Temperature Devices

Type	No. of Channels	Intersil Device No.	Switch Technology	$r_{DS(on)}$ Ω max(1)	$I_{D(off)}$ nA max	t_{on} μs max	t_{off} μs max	Logic Input: Logic Level	Logic Input: Input Typ(2)	Power Consumption mW
SPST	1	IH5001	N-JFET	30	5.0	0.5	1.0	DTL, TTL, RTL	lo	175
		IH5002	N-JFET	50	5.0	0.5	1.0	DTL, TTL, RTL	lo	175
		IH5021	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5022	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
		IH5023	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5024	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
		IH5037	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5038	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5040	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.350
		IH5140	CMOS	75	1.0	0.08	0.05	TTL, CMOS	hi	450
	2	DG111	PMOS FET	450	−1.0	0.3	1.0	DTL, TTL, RTL	lo	330
		DG112	PMOS FET	450	−1.0	0.3	1.0	DTL, TTL, RTL	lo	300
		DG133A	N-JFET	30	1.0	0.3	0.8	DTL, TTL, RTL	hi	175
		DG134A	N-JFET	80	1.0	0.3	0.8	DTL, TTL, RTL	hi	175
		DG141A	N-JFET	10	10.0	0.5	1.25	DTL, TTL, RTL	hi	175
		DG151A	N-JFET	15	10.0	0.5	1.25	DTL, TTL, RTL	hi	175
		DG152A	N-JFET	50	2.0	0.3	0.8	DTL, TTL, RTL	hi	175
		DG180	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	lo	150
		DG181	N-JFET	30	1.0	0.15	0.13	DTL, TTL, RTL	lo	150
		DG182	N-JFET	75	1.0	0.25	0.13	DTL, TTL, RTL	lo	150
		DG433A	N-JFET	35	5.0	0.5	1.0	DTL, TTL, RTL	hi	175
		DG434A	N-JFET	80	5.0	0.5	1.0	DTL, TTL, RTL	hi	175
		DG441A	N-JFET	15	15.0	0.75	1.25	DTL, TTL, RTL	hi	175
		DG451A	N-JFET	20	15.0	0.75	1.25	DTL, TTL, RTL	hi	175
		DG452A	N-JFET	100	5.0	0.5	1.0	DTL, TTL, RTL	hi	175
		IH181	Vara FET	30	0.1	0.25	0.13	DTL, TTL, RTL, CMOS, TTL High Level	lo	.350
		IH182	Vara FET	75	0.1	0.25	0.13	DTL, TTL, RTL, CMOS, TTL High Level	lo	.350
		IH200	CMOS	75	1.0	1.0	0.5	DTL, TTL, RTL, CMOS, TTL High Level	lo	.350
		IH5003	N-JFET	30	1.0	0.3	0.8	DTL, TTL, RTL	hi	175
		IH5004	N-JFET	50	1.0	0.3	0.8	DTL, TTL, RTL	hi	175
		IH5005	N-JFET	10	10.0	1.0	2.5	DTL, TTL, RTL	hi	175
		IH5006	N-JFET	30	1.0	0.5	1.0	DTL, TTL, RTL	hi	175
		IH5007	N-JFET	80	1.0	0.5	1.0	DTL, TTL, RTL	hi	175
		IH5017	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5018	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
		IH5019	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5020	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
		IH5033	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5034	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5035	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5036	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5041	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.350
		IH5048	CMOS	35	1.0	0.25	0.15	DTL, TTL, RTL, CMOS, PMOS	hi	.350
		IH5141	CMOS	75	1.0	0.08	0.05	TTL, CMOS	hi	450
	3	IH5013	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5014	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
		IH5015	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5016	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
		IH5029	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5030	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5031	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5032	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
	4	DG116	P-MOSFET	450	−4.0	0.3	1.0	DTL, TTL, RTL	lo	600
		DG118	P-MOSFET	450	−4.0	0.3	1.0	DTL, TTL, RTL	lo	660
		IH201	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS	lo	.350
		IH202	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS	hi	.350
		IH5009	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5010	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
		IH5011	P-JFET	100	0.2	0.5	0.5	TTL High Level	lo	
		IH5012	P-JFET	150	0.2	0.5	0.5	TTL Low Level	lo	
		IH5025	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5026	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5027	P-JFET	100	0.5	0.2	0.2	TTL High Level	lo	
		IH5028	P-JFET	150	0.5	0.2	0.2	TTL High Level	lo	
		IH5052	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	lo	.350
		IH5053	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.350
	5	DG123	P-MOSFET	450	−4.0	0.3	1.0	DTL, TTL, RTL	hi	750
		DG125	P-MOSFET	450	−4.0	0.3	1.0	DTL, TTL, RTL	lo	825
		DG143A	N-JFET	80	1.0	0.4	0.8	DTL, TTL, RTL	(3)	175
		DG144A	N-JFET	30	1.0	0.4	0.8	DTL, TTL, RTL	(3)	175
		DG146A	N-JFET	10	10.0	0.5	1.25	DTL, TTL, RTL	(3)	175
		DG161A	N-JFET	15	10.0	0.5	1.25	DTL, TTL, RTL	(3)	175
		DG162A	N-JFET	50	2.0	0.4	0.8	DTL, TTL, RTL	(3)	175
		DG186	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	(3)	80
		DG187	N-JFET	30	0.1	0.15	0.13	DTL, TTL, RTL	(3)	80

3

Type	No. of Channels	Device No.	Switch Technology	$r_{DS(on)}$ Ω max(1)	$I_{D(off)}$ nA max	t_{on} μs max	t_{off} μs max	Logic Input: Logic Level	Logic Input: Input Typ(2)	Power Consumption mW
SPDT	1	DG188	N-JFET	75	0.1	0.25	0.13	DTL, TTL, RTL	(3)	80
		DG443A	N-JFET	80	5.0	0.5	1.0	DTL, TTL, RTL	(3)	175
		DG444A	N-JFET	35	5.0	0.5	1.0	DTL, TTL, RTL	(3)	175
		DG446A	N-JFET	15	15.0	0.75	1.25	DTL, TTL, RTL	(3)	175
		DG461A	N-JFET	20	15.0	0.75	1.25	DTL, TTL, RTL	(3)	175
		DG462A	N-JFET	100	5.0	0.5	1.0	DTL, TTL, RTL	(3)	175
		IH187	Vara FET	30	0.1	0.25	0.13	DTL, TTL, RTL, CMOS, PMOS, TTL High Level	(3)	.350
		IH188	Vara FET	75	0.1	0.25	0.13	DTL, TTL, RTL, CMOS, PMOS, TTL High Level	(3)	.350
		IH5042	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, PMOS, CMOS	(3)	.350
		IH5050	CMOS	35	1.0	0.25	0.15	DTL, TTL, RTL, PMOS, CMOS	(3)	.350
	2	IH5142	CMOS	75	1.0	0.08	0.05	TTL, CMOS	(3)	450
		DG189	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	(3)	150
		DG1910	N-JFET	30	1.0	0.15	0.13	DTL, TTL, RTL	(3)	150
		DG191	N-JFET	75	1.0	0.25	0.13	DTL, TTL, RTL	(3)	150
		IH5043	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, PMOS, CMOS	(3)	.350
		IH5051	CMOS	35	1.0	0.25	0.15	DTL, TTL, RTL, PMOS, CMOS	(3)	.350
		IH190	CMOS	30	0.1	0.25	0.13	TTL, CMOS, PMOS, TTL High Level	(3)	.350
		IH191	CMOS	75	0.1	0.25	0.13	TTL, CMOS, PMOS, TTL High Level	(3)	.350
		IH5143	CMOS	75	1.0	0.08	0.05	TTL, CMOS	(3)	450
DPST	1	IH5044	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.350
		IH5144	CMOS	75	1.0	0.8	0.5	TTL, CMOS	hi	450
	2	DG126A	N-JFET	80	1.0	0.3	0.8	DTL, TTL, RTL	hi	175
		DG129A	N-JFET	30	1.0	0.3	0.8	DTL, TTL, RTL	hi	175
		DG140A	N-JFET	10	10.0	0.5	1.25	DTL, TTL, RTL	hi	175
		DG153A	N-JFET	15	10.0	0.5	1.25	DTL, TTL RTL	hi	175
		DG154A	N-JFET	50	2.0	0.3	0.8	DTL, TTL, RTL	hi	175
		DG183	N-JFET	10	10.0	0.3	0.25	DTL, TTL, RTL	hi	150
		DG184	N-JFET	30	1.0	0.15	0.13	DTL, TTL, RTL	hi	150
		DG185	N-JFET	75	1.0	0.25	0.13	DTL, TTL, RTL	hi	150
		DG426A	N-JFET	80	5.0	0.5	1.0	DTL, TTL, RTL	hi	175
		DG429A	N-JFET	35	5.0	0.5	1.0	DTL, TTL, RTL	hi	175
		DG440A	N-JFET	15	15.0	0.75	1.25	DTL, TTL, RTL	hi	175
		DG453A	N-JFET	20	15.0	0.75	1.25	DTL, TTL, RTL	hi	175
		DG454A	N-JFET	100	5.0	0.5	1.0	DTL, TTL, RTL	hi	175
		IH184	Vara FET	30	0.1	0.25	0.13	DTL, TTL, RTL, CMOS, PMOS	hi	.350
		IH185	Vara FET	75	0.1	0.25	0.13	DTL, TTL, RTL, CMOS, PMOS	hi	.350
		IH5045	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, PMOS, CMOS	hi	.350
		IH5049	CMOS	35	1.0	0.25	0.15	DTL, TTL, RTL, PMOS, CMOS	hi	.350
		IH5145	CMOS	75	1.0	0.08	0.05	TTL, CMOS	hi	450
	3	DG120	P-MOS FET	450	−3.0	0.3	2.0	DTL, TTL, RTL	hi	150
		DG121	P-MOS FET	450	−3.0	0.3	2.0	DTL, TTL, RTL	lo	165
DPDT	1	DG139A	N-JFET	30	1.0	0.4	0.8	DTL, TTL, RTL	(3)	175
		DG142A	N-JFET	80	1.0	0.4	0.8	DTL, TTL, RTL	(3)	175
		DG145A	N-JFET	10	10.0	0.5	1.25	DTL, TTL, RTL	(3)	175
		DG163A	N-JFET	15	10.0	0.5	1.25	DTL, TTL, RTL	(3)	175
		DG164A	N-JFET	50	2.0	0.4	0.8	DTL, TTL, RTL	(3)	175
		DG439A	N-JFET	35	5.0	0.5	1.0	DTL, TTL, RTL	(3)	175
		DG442A	N-JFET	80	5.0	0.5	1.0	DTL, TTL, RTL	(3)	175
		DG445A	N-JFET	15	15.0	0.75	1.25	DTL, TTLQ, RTL	(3)	175
		DG463A	N-JFET	20	15.0	0.75	1.25	DTL, TTL, RTL	(3)	175
		DG464A	N-JFET	100	5.0	0.5	1.0	DTL, TTL, RTL	(3)	175
		IH5046	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	(3)	.350
4PST	1	IH5047	CMOS	75	1.0	0.5	0.25	DTL, TTL, RTL, CMOS, PMOS	hi	.350
	1 of 8	IH6108	CMOS	400	10.0	1.5	1.0	DTL, TTL, RTL, CMOS	hi	5
MUX	1 of 16	IH6116	CMOS	400	10.0	1.5	1.0	DTL, TTL, RTL, CMOS	hi	5
	2 of 8	IH6208	CMOS	400	5.0	1.5	1.0	DTL, TTL, RTL, CMOS	hi	5
	2 of 16	IH6216	CMOS	400	5.0	1.5	1.0	DTL, TTL, RTL, CMOS	hi	5

3

Multi-Channel FET Switches

Electrical Characteristics @ +25°C—Military Temperature Devices

Type	No. of Channels	Device No.	Switch Technology	$r_{DS(on)}$ ohms max(4)	$r_{DS(on)}$ ohms max(1)	$I_{D(off)}$ na max	t_{on} ns max*	t_{off} ns max*	Logic Input Logic Level	Logic Input type
	3	MM-455	P-MOS	200	600	0.2	50	50	P-MOS	lo
		MM-555	P-MOS	200	600	20.0	50	50	P-MOS	lo
		G-124	P-MOS	100	450	2.0	100	100	P-MOS	hi
		G-125	N-JFET	500	500	0.05	30	50	−5V PMOS	hi
		G-126	N-JFET	250	250	0.05	30	50	−10V PMOS	hi
		G-127	N-JFET	90	90	0.1	30	50	−5V PMOS	hi
		G-128	N-JFET	45	45	0.1	30	50	−10V PMOS	hi
		G-129	N-JFET	500	500	0.05	30	50	−5V PMOS	hi
		G-130	N-JFET	250	250	0.05	30	50	−10V PMOS	hi
		G-131	N-JFET	90	90	0.1	30	50	−5V PMOS	hi
	4	G-132	N-JFET	45	45	0.1	30	50	−10V PMOS	hi
SPST		G-1330	N-JFET	20	20	0.5	30	50	−5V PMOS	hi
		G-1340	N-JFET	10	10	0.5	30	50	−10V PMOS	hi
		G-1350	N-JFET	20	20	0.5	30	50	−5V PMOS	hi
		G-1360	N-JFET	10	10	0.5	30	50	−10V PMOS	hi
		MM-451	P-MOS	200	600	0.2	50	50	P-MOS	lo
		MM-452	P-MOS	200	600	0.2	50	50	P-MOS	lo
		MM-551	P-MOS	200	600	20.0	50	50	P-MOS	lo
		MM-552	P-MOS	200	600	20.0	50	50	P-MOS	lo
	5	G-116	P-MOS	100	450	−2.5	100	100	P-MOS	lo
		G-117	P-MOS	100	450	−0.5	100	100	P-MOS	lo
	6	G-115	P-MOS	100	450	−10.0	100	100	P-MOS	lo
		G-118	P-MOS	100	450	−3.0	100	100	P-MOS	lo
		G-123	P-MOS	125	500	−10.0	100	100	P-MOS	lo
Diff	2	MM-450	P-MOS	200	600	0.2	50	50	P-MOS	lo
		MM-550	P-MOS	200	600	20.0	50	50	P-MOS	lo
SPST	3	G-119	P-MOS	100	450	−1.5	100	100	P-MOS	lo

*These times are dependent on the driver used.

3 Drivers for FET Switches

Electrical Characteristics @ +25°C—Military Temperature Devices

No. of Channels	Device No.	V_{OUT} Positive volts	V_{OUT} Negative volts	t_{on} ns max	t_{off} ns max	I_{in} Lo mA (Max)	I_{in} Hi μA (Max)	Logic Input Level	Power Consumption (mW)
	D112	+9.9	−19.2	250	1500	0.7	1.0	TTL	200
	D113	+9.9	−19.2	250	1500	1.0	1.0	TTL	200
2	D120	+9.9	−19.2	250	600	0.7	1.0	TTL	200
	D121	+9.9	−19.2	250	600	1.0	1.0	TTL	200
	IH6201	+14.0	−14.0	200	300	1.0 μA	1.0	TTL	350
4	D129	V_{CC}	−19.3	250	1000	−0.2	0.25	TTL/DTL	100
6	D123	V_{CC}	−19.7	250	600	1.0	1.0	TTL/DTL	125
	D125	V_{CC}	−19.7	250	600	0.7	1.0	TTL	300

NOTES:
1. Switch Resistance under worst case analog voltage.
2. Positive logic lo ("O") or hi ("I") voltage at driver input necessary to turn switch on.
3. Logic "O" or "I" can be arbitrarily assigned for double-throw switches.
4. Switch resistance under best case analog voltage.

VARAFET

Type	$r_{DS(on)}$ Ω max	V_p V max	$I_{s(off)}$ pA max	I_{DSS} mA min	t_{on} ns max	t_{off} ns max	Package 4 FETS/Pkg	V_{analog} V_{p-p} min	V_{inject} V_{p-p} max
IH401	30	7.5	200	45 min	50	150	16 Pin Dip	15	10
IH401A	50	5.	200	35 min	50	150	16 Pin Dip	20	10

LOWEST QUIESCENT CURRENT — HIGHEST SPEED — LOWEST $r_{DS\ (on)}$

IH5040 FAMILY and IH200 FAMILY
Monolithic CMOS driver gate combination.

Features
1. Very low quiescent current resulting in very low power consumption.
2. Low cost.
3. Good speed with moderate $r_{DS\ (on)}$ and leakage.
4. Overvoltage protection to ±25V.
5. Can switch up to ±13V signals with ±15V supplies.

Notes
1. TTL, DTL, CMOS and PMOS compatible.
2. 5048 through 5053 and the IH200 family are 2-chip hybrid devices with 35Ω $r_{DS\ (on)}$ max @ 25°C.
3. 5040 through 5047 have 75Ω $r_{DS\ (on)}$ max @ 25°C

5040	SPST
5041,5048	Dual SPST
5042,5050	SPDT
5043,5051	Dual SPDT
5044	DPST
5045,5049	Dual DPST
5046	DPDT
5047	4PST
5052,5053	Quad SPST
200	Dual SPST
201,202	Quad SPST

IH5140 FAMILY
Monolithic CMOS driver gate combination.

Features
1. High speed switch.
2. Low quiescent current resulting in low power consumption.
3. Low leakage resulting in low error term.
4. Lower cost than the comparable speed DG180 Family.
5. Can switch signals almost to the supply rails.

Notes
1. TTL and CMOS compatible.
2. Pin compatible with the more popular members of the DG180 Family.

5140	SPST
5141	Dual SPST
5142	SPDT
5143	Dual SPDT
5144	DPST
5145	Dual DPST

IH181 FAMILY
CMOS driver and Varafet gate.

Features
1. Low charge injection.
2. Almost as fast as 5140 and DG180 Families.
3. Very low quiescent current resulting in low power consumption.
4. Ultra low leakage.

Notes
1. TTL, HTL, CMOS and PMOS compatible.
2. Pin for pin compatible with DG180 Family.

IH181,182	Dual SPST
IH184,185	Dual DPST
IH187,188	SPDT
IH190,191	Dual SPDT

DG180 FAMILY
Bipolar/MOS driver with N-JFet gate.

Features
1. Low $r_{DS\ (on)}$
2. As fast as the IH5140 Family.
3. Moderate leakage

Notes
1. DTL, TTL, RTL compatible
2. DG180,183,185 and 189 have 10 Ω max on resistance but have higher leakage than others in the family.
3. DG181,184,187 and 190 have 30Ω max $r_{DS\ (on)}$.
4. DG182,185,188 and 191 have 75Ω max $r_{DS\ (on)}$.

DG180,181,182	Dual SPST
DG183,184,185	Dual DPST
DG186,187,188	SPDT
DG189,190,191	Dual SPDT

DG126, DG126A FAMILY and IH5001 FAMILY
Bipolar driver with N-JFet gate.

Features
1. Low $r_{DS\ (on)}$
2. Only switch with true chip enable pin.
3. Low cost
4. Moderate leakage & quiescent current specifications.

Notes
1. "A" selection devices have higher speeds.
2. DG426/A family is a slightly downgraded version of the DG126/A series. See spec tables for comparison.

DG133,134,141, 151,152	Dual SPST
DG126,129,140, 153,154	Dual DPST
DG143,144,146, 161,162	Diff. Input SPDT
DG139,142,145, 163,164	Diff. Input DPDT
IH5001,5002	SPST
IH5003,5004,5005 5006,5007	Dual SPST

3

Notes:
1. Intersil continues to produce the older DG111 family of switches (DG111 through (DG125). The most significant feature of this family is that it has the maximum number of switches per package.
2. Intersil also markets devices that consist of drivers only (D112 through D129 and the IH6201) and gates only (G115 through G135, MM450 through MM555 and the IH401).

For switches whose outputs go into the input of an Op Amp:	For switching positive signals only:
5009 FAMILY VIRTUAL GROUND SWITCH	**5025 FAMILY** POSITIVE SIGNAL SWITCH
Output of switch must go into the virtual ground point of an Op Amp (unless signal is <0.7V).	Can switch positive signals only unless a translator driver is used.
Features 1. Very low quiescent current 2. Does not need driver, can be driven directly by TTL. 3. Low cost.	**Features** 1. Very low quiescent current 2. Does not need driver, can be driven directly by TTL. 3. Low Cost
Notes 1. All switches in 5009 family are SPST. 2. Odd numbered devices are driven by TTL open collector logic. 3. Even numbered devices are driven by TTL low level logic. 4. Commonly used for signals going into the inverting input of Op-Amps.	**Notes** 1. All switches in 5025 family are SPST. 2. All devices can be driven by TTL open collector logic. All devices can be driven by low level TTL logic if input signal is less than 1V. 3. Commonly used for signals going into the non-inverting input of Op-Amps. 4. Odd numbered devices have 100Ω max $r_{DS\ (on)}$ @ 25°C. 5. Even numbered devices have 150 max $r_{DS\ (on)}$ @ 25°C.
5009,5010 quad, compensated 5011,5012 quad, uncompensated 5013,5014 triple, compensated 5015,5016 triple, uncompensated 5017,5018 dual, compensated 5019,5020 dual, uncompensated 5021,5022 single, compensated 5023,5024 single, uncompensated	5025,5026 quad, common drain 5027,5028 quad. 5029,5030 triple, common drain 5031,5032 triple. 5033,5034 dual, common drain 5035,5036 dual. 5037,5038 single.

INTERSIL

IH6108
CMOS 8 Channel Analog Multiplexer

FEATURES

- Ultra Low Leakage ≤ 100pA (Total I_{Doff})
- r_{on} <400 ohms over full signal and temperature range
- Power supply quiescent current less than 100μA
- ±14V analog signal range
- No Latch up or "S.C.R." action
- Break before make switching
- Binary strobe control (3 strobe inputs control 8 channels)
- TTL and CMOS compatible strobe control
- Pin — Pin with DG508 HI-508 & AD7508

GENERAL DESCRIPTION

The IH6108 is a CMOS monolithic, one-out-of-8 multiplexer. The part is a plug-in replacement for the DG508. Three line binary decoding is used so that the 8 channels can be controlled by 3 strobe inputs; additionally a fourth input is provided to use as a system enable; if the enable input is 0V, none of the channels can be turned on. When the enable input is high (5V) the channels are sequenced by the 3 line strobe inputs. The 3 strobe inputs are controlled by TTL logic or CMOS logic elements; a "0" corresponds to any voltage less than 0.8V and a "1" corresponds to any voltage greater than 2.4V; however the enable input En *must* be taken to 5V to enable the system and less than 0.8V to disable the system.

FUNCTIONAL DIAGRAM

3 LINE BINARY STROBE INPUTS
(1 0 1) AND En @ 5V
ABOVE EXAMPLE SHOWS CHANNEL 6 TURNED ON.

DECODE TRUTH TABLE

A_2	A_1	A_0	En	ON SWITCH
x	x	x	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

A_0, A_1, A_2
Logic "1" = $V_{AH} \geq 2.4V$
Logic "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6108MDE	−55°C to +125°C	16 pin DIP
IH6108CDE	0°C to 70°C	16 pin DIP
IH6108CPE	0°C to 70°C	16 pin plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, En) to Ground ..... −15V to 15V
V_S or V_D to V_{CC} ..... 0, −32V
V_S or V_D −V_{CC} 0, 32V
+V_{CC} to Ground 16V
−V_{CC} to Ground ..... −16V
Current (Any Terminal) ..... 30 mA
Current (Analog Drain) ..... 20 mA
Current (Analog Source) ..... 20 mA
Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Power Dissipation (Package)* ..... 1200 mW

*All leads soldered or welded to PC board. Derate 10 mW/°C above 70°C.

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT	TEST CONDITIONS (UNLESS OTHERWISE NOTED) +V_{CC} = 15V, −V_{CC} = −15V, Ground = 0V V_{En} = +5V (Note 1)	
SWITCH	$r_{DS(ON)}$	S to D	8	180	300	300	400	350	350	450	Ω	V_D = 10V, I_S = −1.0mA	Sequence each switch on
			8	150	300	300	400	350	350	450		V_D = −10V, I_S = −1.0mA	$V_{A(L)}$ = 0.8V, $V_{A(H)}$ = 2.4V
	$\Delta r_{DS(ON)}$			20							%	$\Delta r_{DS(ON)} = \frac{r_{DS(ON)MAX} - r_{DS(ON)MIN}}{r_{DS(ON)AVG.}}$ −10V ≤ V_S 10V	
	$I_{S(OFF)}$	S	8	0.002		0.05	50		0.1	50	NA	V_S = 10V, V_D = −10V	
			8	0.002		0.05	50		0.1	50		V_S = −10V, V_D = 10V	
	$I_{D(OFF)}$	D	1	0.03		0.1	100		0.2	100		V_D = 10V, V_S = −10V	V_{En} = 0
			1	0.03		0.1	100		0.2	100		V_D = −10V, V_S = 10V	
	$I_{D(ON)}$	D	8	0.1		0.2	100		0.4	100		$V_{S(All)}$ = V_D = 10V	Sequence each switch on
			8	0.1		0.2	100		0.4	100		$V_{S(All)}$ = V_D = −10V	$V_{A(L)}$ = 0.8V, $V_{A(H)}$ = 2.4V
INPUT	$I_{AN(ON)}$ or	A_0, A_1 or A_2	3	.01		−10	−30		−10	−30	μA	V_A = 2.4V or 0V	
	$I_{AN(OFF)}$	Inputs	3	.01		10	30		10	30		V_A = 15V or 0V	
	I_{2n}	A_0 A_1 A_2	3			−10	−30		−10	−30		V_{En} 5V	All V_A = 0 (Strobe pins)
		En	1			−10	−30		−10	−30		V_{En} 0	
DYNAMIC	$t_{transition}$	D		0.3		1					μs	See Fig. 1	
	t_{open}	D		0.2								See Fig. 2	
	$t_{on(En)}$	D		0.6		1.5						See Fig. 3	
	$t_{off(En)}$	D		0.4		1							
	"OFF" Isolation	D		60							dB	V_{En} = 0, R_L = 200Ω, C_L = 3pF, V_S = 3 VRMS, f = 500 kHz	
	$C_{S(OFF)}$			5							pF	V_S = 0	
	$C_{D(OFF)}$			25								V_D = 0	V_{En} = 0V, f = 140 kHz to 1 MHz
	$C_{DS(OFF)}$			1								V_S = 0, V_D = 0	
SUPPLY	$I_{13}(+V_{CC})$	+V_{CC}	1	40		200			1000		μA		
	$I_3(-V_{CC})$	−V_{CC}	1	2		100			1000			V_{En} 5V	
	I_{13} Standby	+V_{CC}	1	1		100			1000				All V_A 0 OR 5V
	I_3 Standby	−V_{CC}	1	1		100			1000			V_{En} 0	

NOTE 1: See Section I. Enable Input Strobing Levels.

Figure 1. $t_{transition}$ Switching Test

3

Figure 2. t_{open} Break-Before-Make Switching Test

Figure 3. t_{on} and t_{off} Switching Test

3

IH6108 APPLICATION INFORMATION

I. Enable Input Strobing Levels

The chip enable input on the IH6108 requires a minimum of +4.5V to trigger it into the "1" state and a maximum of +0.8V to trigger it into the "0" state. If the chip enable input is being driven from TTL logic, a pull-up resistor is required from the gate output to +5V supply. The value of this resistor is not critical and can be in the 1K to 3KΩ range (See Figure 4).

Figure 4. Enable Input Strobing from TTL Logic

IH6108 APPLICATION INFORMATION (CONT.)

When the En input is driven from CMOS logic, no pullup is necessary. Fig. 5 shows the CD4009 driving the En input.

Figure 5. Enable Input Strobing from CMOS Logic

The Supply Voltage of the CD4009 does affect the switching speed of the IH6108. same is true for TTL Supply Voltage Levels. The chart below shows the effect, on $t_{transition}$ times, of supply varying from +4.5V to +5.5V.

CMOS OR TTL SUPPLY VOLTAGE	TYPICAL $t_{transition}$ @ 25°C
+4.5V	400ns
+4.75V	300ns
+5.00V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the Enable Strobe Logic.

The cases shown in Figures 4 and 5 deal with enable strobing when expandability to more than eight channels is required. In these cases the En terminal acts as a fourth binary input. If eight channels or less are being multiplexed, the En terminal can be directly connected to +5V logic supply which would "enable" the IH6108 at all times.

IH6108 APPLICATION INFORMATION (CONT.)

APPLICATIONS

II. Using the IH6108 with supplies other than ±15V

The IH6108 can be used with power supplies ranging from ±6V to ±16V. The switch $r_{DS(ON)}$ will increase as the supply voltages decrease. However, the multiplexer error term (the product of leakage times $r_{DS(ON)}$) will remain approximately constant since leakage decreases as the supply voltages are reduced.

Caution must be taken to ensure that the chip enable (En) voltage is at least 0.7V below V_{CC} at all times. If this is not done the binary input strobing levels will not function properly. This may be achieved quite simply by connecting En (pin 2) to $+V_{CC}$ (pin 13) via a silicon diode as shown in Figure 6. If the IH6108 is hooked up in this type of a configuration a further requirement must be met — the strobe levels at A_0 and A_1 must be within 2.5V of the En voltage to define a binary "1" state. For the case shown in Figure 6 the En voltage is 11.3V which means that logic high at A_0 and A_1 is = +8.8V (logic low continues to be = 0.8V). In this configuration the IH6108 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the IH6108 have common supplies the En pin should again be connected to the supply through a silicon diode. In this case tying En to the logic supply directly will not work since it will violate the 0.7V differential voltage required between $+V_{CC}$ and En on the IH6108 (See Figure 7). A 1μf capacitor can be placed across the diode to minimize switching glitches.

Figure 6. IH6108 Connection Diagram for less than ±15V Supply Operation.

IH6108 APPLICATION INFORMATION (CONT.)

Figure 7. IH6108 Connection Diagram with Enable Input Strobing for less than ±15V Supply Operation.

III. Peak-to-Peak Signal Handling Capability

The IH6108 can handle input signals up to ±14V actually -15V to +14.3V when it has ±15V supplies. The input protection diode prevents the handling of signals up to +15V.

The electrical specifications of the IH6108 are guaranteed for ±10V signals but the specifications have very minor changes for ±14V signals. The notable changes would be slightly lower $r_{DS(on)}$ and slightly higher leakages.

PACKAGE DIMENSIONS

16 Pin Ceramic Dual-In-Line Package (DE)

16 Pin Plastic Dual-In-Line Package (PE)

INTERSIL

IH6116
CMOS 16-Channel Analog Multiplexer (One out of 16)

FEATURES

- Pin Compatible with DG506, HI-506 & AD7506
- Ultra Low Leakage ≤100pA
- ±11V analog signal range
- r_{on} <700 ohms over full signal and temperature range
- Break before make switching
- TTL and CMOS compatible strobe control
- Binary strobe control (4 strobe inputs control 16 channels)
- Two tier submultiplexing to facilitate expandability
- Power supply quiescent current less than 100μA
- No Latch up or "S.C.R." action

GENERAL DESCRIPTION

The IH6116 is a CMOS monolithic, one-out-of 16 multiplexer, and is a plug-in replacement for the DG506. Four line binary decoding is used so that the 16 channels can be controlled by 4 strobe inputs; additionally a fifth input is provided to use as a system enable; if the enable input is 0V, none of the channels can be turned on. When the enable input is high (5V) the channels are sequenced by the 4 line strobe inputs. The 4 strobe inputs are controlled by TTL logic or CMOS logic elements; a "0" corresponds to any voltage less than 0.8V and a "1" corresponds to any voltage greater than 3V; however the enable input (EN) *must* be taken to 5V to enable the system and less than 0.8V to disable the system.

FUNCTIONAL DIAGRAM

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	EN	ON SWITCH
x	x	x	x	0	NONE
0	0	0	0	1	1
0	0	0	1	1	2
0	0	1	0	1	3
0	0	1	1	1	4
0	1	0	0	1	5
0	1	0	1	1	6
0	1	1	0	1	7
0	1	1	1	1	8
1	0	0	0	1	9
1	0	0	1	1	10
1	0	1	0	1	11
1	0	1	1	1	12
1	1	0	0	1	13
1	1	0	1	1	14
1	1	1	0	1	15
1	1	1	1	1	16

Logic "1" = $V_{AH} \geq 3.0V$
Logic "0" = $V_{AL} \leq 0.8V$

PIN CONFIGURATION

TOP VIEW
V_1 COMMON TO SUBSTRATE

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6116MDI	-55°C to +125°C	28 pin DIP
IH6116CDI	0°C to 70°C	28 pin DIP
IH6116CPI	0°C to 70°C	28 pin Plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V to 15V
V_S or V_D to V_1 ..... 0, −32V
V_S or V_D to V_2 ..... 0, 32V
V_1 to Ground 16V
V_2 to Ground ..... −16V
Current (Any Terminal) ..... 30 mA
Current (Analog Drain) ..... 20 mA
Current (Analog Source) ..... 20 mA
Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Power Dissipation (Package)* ..... 1200 mW

*All leads soldered or welded to PC board. Derate 10 mW/°C above 70°C.

ELECTRICAL CHARACTERISTICS

	CHARACTERISTIC	MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX −55°C	MAX LIMITS M SUFFIX 25°C	MAX LIMITS M SUFFIX 125°C	MAX LIMITS C SUFFIX 0°C	MAX LIMITS C SUFFIX 25°C	MAX LIMITS C SUFFIX 70°C	UNIT	TEST CONDITIONS (UNLESS OTHERWISE NOTED) V_1 = 15V, V_2 = −15V, Ground = 0 V_{EN} = +5V (Note 1)	
SWITCH	$r_{DS(ON)}$	S to D	16	480	600	600	700	650	650	750	Ω	V_D = 10V, I_S = −1.0mA	Sequence each switch on
			16	300	600	600	700	650	650	750		V_D = −10V, I_S = −1.0mA	$V_{A(L)}$ = 0.8V, $V_{A(H)}$ = 3V
	$\Delta r_{DS(ON)}$			20							%	$\Delta r_{DS(ON)} = \frac{r_{DS(ON)MAX} - r_{DS(ON)MIN}}{r_{DS(ON)AVG.}}$ −10V ≤ V_S 10V	
	$I_{S(OFF)}$	S	16	0.01		0.1	50		0.2	50	NA	V_S = 10V, V_D = −10V	V_{EN} = 0
			16	0.01		0.1	50		0.2	50		V_S = −10V, V_D = 10V	
	$I_{D(OFF)}$	D	1	0.1		0.2	100		0.4	100		V_D = 10V, V_S = −10V	
			1	0.1		0.2	100		0.4	100		V_D = −10V, V_S = 10V	
	$I_{D(ON)}$	D	16	0.1		0.2	100		0.4	100		$V_{S(All)}$ = V_D = 10V	Sequence each switch on
			16	0.1		0.2	100		0.4	100		$V_{S(All)}$ = V_D = −10V	$V_{A(L)}$ = 0.8V, $V_{A(H)}$ = 3V
INPUT	$I_{AN(ON)}$ or $I_{AN(OFF)}$		4	.01		−10	−30		−10	−30	μA	V_A = 3.0V	
			4	.01		10	30		10	30		V_A = 15V	
	I_A	A_0 A_1 A_2 A_3	4			−10	−30		−10	−30		V_{EN} = 5V	All V_A = 0
		EN	1			−10	−30		−10	−30		V_{EN} = 0	
DYNAMIC	$t_{transition}$	D		0.6		1					μs	See Fig. 1	
	t_{open}	D		0.2								See Fig. 2	
	$t_{on(En)}$	D		0.8		1.5						See Fig. 3	
	$t_{off(En)}$	D		0.3		1							
	"OFF" Isolation	D		60							dB	V_{EN} = 0, R_L = 200Ω, C_L = 3pF, V_S = 3 VRMS, f = 500 kHz	
	$C_{S(OFF)}$			5							pF	V_S = 0	V_{EN} = 0, f = 140 kHz to 1 MHz
	$C_{D(OFF)}$			40								V_D = 0	
	$C_{DS(OFF)}$			1								V_S = 0, V_D = 0	
SUPPLY	I_1	V_1	1	55		200			1000		μA	V_{EN} = 5V	All V_A = 0 OR 3V
	I_2	V_2	1	2		100			1000				
	I_1 Standby	V_1	1	1		100			1000			V_{EN} = 0	
	I_2 Standby	V_2	1	1		100			1000				

NOTE 1: See Section V. Enable Input Strobing Levels.

Figure 1

Figure 2

Figure 3

IH6116 APPLICATIONS

I. 1 out of 32 channel multiplexer using 2 IH6116s.

Figure 4

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

IH6116 APPLICATIONS

II. 1 out of 32 channel multiplexer using 2 IH6116s; using an IH5041 for submultiplexing.

Figure 5

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
0	0	0	0	0	S1
0	0	0	0	1	S2
0	0	0	1	0	S3
0	0	0	1	1	S4
0	0	1	0	0	S5
0	0	1	0	1	S6
0	0	1	1	0	S7
0	0	1	1	1	S8
0	1	0	0	0	S9
0	1	0	0	1	S10
0	1	0	1	0	S11
0	1	0	1	1	S12
0	1	1	0	0	S13
0	1	1	0	1	S14
0	1	1	1	0	S15
0	1	1	1	1	S16

DECODE TRUTH TABLE

A_4	A_3	A_2	A_1	A_0	ON SWITCH
1	0	0	0	0	S17
1	0	0	0	1	S18
1	0	0	1	0	S19
1	0	0	1	1	S20
1	0	1	0	0	S21
1	0	1	0	1	S22
1	0	1	1	0	S23
1	0	1	1	1	S24
1	1	0	0	0	S25
1	1	0	0	1	S26
1	1	0	1	0	S27
1	1	0	1	1	S28
1	1	1	0	0	S29
1	1	1	0	1	S30
1	1	1	1	0	S31
1	1	1	1	1	S32

IH6116 APPLICATIONS

III. 1 out of 64 multiplexer using 4 1/16s and IH5053 as submultiplexer.

Figure 6

IV. GENERAL NOTE ON EXPANDABILITY OF IH6116

The IH6116 is a two tier multiplexer wherein sixteen input channels are routed to a common output in blocks of 4 channels at a time. Each block of 4 input channels is routed to one common output channel; thus the submultiplexed system looks like 4 blocks of 4 inputs routed to 4 different outputs, and the 4 outputs are all tied together. Thus 20 switches are needed to handle the 16 channels of information. The advantage of this scheme is lower output capacity and lower leakage than a system with all 16 channels tied to one common output. Also the expandability into 32, 64, 128, etc. is facilitated. Figures 4, 5, and 6 show how the IH6116 is expanded.

Figure 4 shows a 1 out of 32 multiplexer using 2 of the IH6116s. Since the 6116 is itself a 2 tier system. Now the four output channels of each 6116 are tied together so that 8 channels are tied for the V_{out} common point. Since only one channel of information is on at a time, the common output will consist of 7 off channels and 1 on channel. Thus the output leakage will correspond to 7 $I_{D(offs)}$ and 1 $I_{D(on)}$; this should result in about 1.0 nA of typical leakage at room temperature. Thruput speed will be typically 0.8μs for t_{on} and 0.3μs for t_{off}. Thruput channel resistance will be in the 500 ohm area.

Figure 5 shows the same 1 out of 32 mux as Figure 4, except that a third tier of submultiplexing is added to further reduce leakage and output capacity. The IH5041 has typical on resistances of 50 ohms (max. is 75 ohms) so it only increases thruput channel resistance from the 500 ohms of Figure 4 to about 550 ohms for Figure 5. Thruput channel speed is a little slower by about 0.5μs for both on and off time. Output leakage is about 0.2 nA typical.

Figure 6 shows a 1 out of 64 mux using 3 tier muxing (similar to Figure 5 application). The Intersil IH5053 is used to get the third tier of muxing. The V_{out} point will see 3 off channels and 1 on channel at any time so that the typical leakages will be about 0.4 nA. Thruput channels resistance will be in the 550 ohm area and thruput switching speeds will be about 1.3μs for on time and 0.8μs for off time.

The IH5053 was chosen as the third tier of the mux because it will switch the same AC signals as the IH6116 (typically plus and minus 11V) and break before make switching is guaranteed so that the muxing system remains a break-before-make. Also power supply quiescent currents are typically 1μA from any supply, so that no excessive system power is generated. Also the logic of the 5053 is such that it can be tied directly to the enable input (as shown in the figures) with no extra logic being required.

V. ENABLE INPUT STROBING LEVELS

The enable input (EN) acts as an enabling or disabling pin for the IH6116, when used as a 16 channel mux; however, when expanding the mux to more than 16 channels, the EN pin acts as another address input. As an example, we see in Figures 4 and 5 that the EN pin acts as the A_4 input.

For the system to function properly the EN input (pin 18) must go to 5V ±5% for the high state and less than 0.8V for the low state. When using TTL logic, a pull-up resistor should be used to pull the output voltage up to 5V; this resistor should be 1k ohm or less. When using CMOS logic, the high state goes up to the power supply so no pull-up is required.

3

PACKAGE DIMENSIONS

28 Pin Ceramic Package

28 Pin Plastic Package

28 Pin CerDIP Package

NOTE: This multiplexer does not require external resistors and/or diodes to eliminate what is commonly known as a latch up or SCR action. Because of the elimination of external resistors in each channel the $r_{DS(ON)}$ of the switch is maintained at specified values.

INTERSIL

IH6208 CMOS 4-Channel Differential Analog Multiplexer

FEATURES

- **Ultra low leakage ≤ 100pA (Total I_{Doff})**
- **r_{on} < 400 ohms over full signal and temperature range**
- **Power supply quiescent current less than 100μA**
- **±14V analog signal range**
- **No latch up or "S.C.R." action**
- **Break before make switching**
- **Binary strobe control (2 strobe inputs controls 2 out of 8 channels).**
- **TTL and CMOS compatible strobe control**
- **Pin — Pin with HI509, DG509 & AD7509**

GENERAL DESCRIPTION

The IH6208 is a 2 out of 8 CMOS monolithic multiplexer. The part is a plug-in replacement for the DG509. Two line binary decoding is used so that the 8 channels can be controlled in pairs by the binary inputs; additionally a third input is provided to use as a system enable; if the enable input is 0V, none of the channels can be turned on. When the enable input is high (5V) the channels are sequenced by the 2 line binary inputs. The 2 strobe inputs are controlled by TTL logic or CMOS logic elements; a "0" corresponds to any voltage less than 0.8V and a "1" corresponds to any voltage greater than 2.4V; however the enable input (En) *must* be taken to 5V to enable the system and less than 0.8V to disable the system.

FUNCTIONAL DIAGRAM

2 LINE BINARY STROBE INPUTS
(0 0) AND En = 5V (En = "1" FOR +5V, "0" FOR 0V)
ABOVE EXAMPLE SHOWS CHANNELS 1a & 1b ON.

DECODE TRUTH TABLE

A_1	A_0	En	ON SWITCH PAIR
X	X	0	NONE
0	0	1	1a, 1b
0	1	1	2a, 2b
1	0	1	3a, 3b
1	1	1	4a, 4b

A_0, A_1

LOGIC "1" = V_{AH} > 2.4V
LOGIC "0" = V_{AL} < 0.8V

PIN CONFIGURATION

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6208MDE	-55°C to +125°C	16 pin DIP
IH6208CDE	0°C to 70°C	16 pin DIP
IH6208CPE	0°C to 70°C	16 pin Plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, En) to Ground ..... −15V, V_1
V_S or V_D to V_{CC} ..... 0, −32V
V_S or V_D to V_{CC} 0, 32V
+V_{CC} to Ground 16V
−V_{CC} to Ground ..... −16V
Current (Any Terminal) ..... 30 mA
Current (Analog Drain) ..... 20 mA
Current (Analog Source) ..... 20 mA
Operating Temperature ..... −55 to 125°C
Storage Temperature ..... −65 to 150°C
Power Dissipation (Package)* ..... 1200 mW

*All leads soldered or welded to PC board. Derate 10 mW/°C above 70°C.

ELECTRICAL CHARACTERISTICS

	CHARACTERISTIC	MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25°C	MAX LIMITS M SUFFIX −55°C	M SUFFIX 25°C	M SUFFIX 125°C	C SUFFIX 0°C	C SUFFIX 25°C	C SUFFIX 70°C	UNIT	TEST CONDITIONS (UNLESS OTHERWISE NOTED) +V_{CC} = 15V, −V_{CC} = −15V, Ground = 0V V_{En} = +5V (Note 1)	
SWITCH	$r_{DS(ON)}$	S to D	8	180	300	300	400	350	350	450	Ω	V_D = 10V, I_S = −1.0 mA	Sequence each switch on
			8	150	300	300	400	350	350	450		V_D = −10V, I_S = −1.0 mA	$V_{A(L)}$=0.8V, $V_{A(H)}$=2.4V
	$\Delta r_{DS(ON)}$			20							%	$\Delta r_{DS(ON)} = \frac{r_{DS(ON)MAX} - r_{DS(ON)MIN}}{r_{DS(ON)}\ AVG.}$ −10V ≤ V_S 10V	
	$I_{S(OFF)}$	S	8	0.002		0.05	50		0.1	50	NA	V_S = 10V, V_D = −10V	V_{En} = 0
			8	0.002		0.05	50		0.1	50		V_S = −10V, V_D = 10V	
	$I_{D(OFF)}$	D	2	0.03		0.1	50		0.2	100		V_D = 10V, V_S = −10V	
			2	0.03		0.1	50		0.2	100		V_D = −10V, V_S = 10V	
	$I_{D(ON)}$	D	8	0.1		0.2	50		0.4	100		$V_{S(All)}$= V_D = 10V	Sequence each switch on
			8	0.1		0.2	50		0.4	100		$V_{S(All)}$ = V_D = −10V	$V_{A(L)}$=0.8V, $V_{A(H)}$=2.4V
INPUT	$I_{AN(ON)}$ or		2	.01		−10	−30		−10	−30	μA	V_A = 2.4V or 0V	
	$I_{AN(OFF)}$		2	.01		10	30		10	30		V_A = 15V or 0V	
	I_{2n}	A_0 A_1	2			−10	−30		−10	−30		V_{En} = 5V	All V_A = 0
		En	1			−10	−30		−10	−30		V_{En} = 0	(Strobe Pins)
DYNAMIC	$t_{transition}$	D		0.3		1					μs	See Fig. 1	
	t_{open}	D		0.2								See Fig. 2	
	$t_{on(En)}$	D		0.6		1.5						See Fig. 3	
	$t_{off(En)}$	D		0.4		1							
	"OFF" Isolation	D		60							dB	V_{En} = 0, R_L = 200Ω, C_L = 3 pF, V_S = 3 VRMS, f = 500 kHz	
	$C_{S(OFF)}$			5							pF	V_S = 0	V_{En} = 0, f = 140 kHz to 1 MHz
	$C_{D(OFF)}$			12								V_D = 0	
	$C_{DS(OFF)}$			1								V_S = 0, V_D = 0	
SUPPLY	I_{14} (+V_{CC})	+V_{CC}	1	40		200			1000		μA	V_{En} = 5V	All V_A = 0 OR 5V
	I_3 (−V_{CC})	−V_{CC}	1	2		100			1000				
	I_{14} Standby	+V_{CC}	1	1		100			1000			V_{En} = 0	
	I_3 Standby	−V_{CC}	1	1		100			1000				

NOTE 1: See Section I Enable Input Strobing Levels.

SWITCHING INFORMATION

Figure 1. $t_{transition}$ Switching Test

Figure 2. t_{open} (Break-Before-Make) Switching Test

Figure 3. t_{on} and t_{off} Switching Test

3

IH6208 APPLICATION INFORMATION

I. Enable Input Strobing Levels

The chip enable input on the IH6208 requires a minimum of +4.5V to trigger it into the "1" state and a maximum of +0.8V to trigger it into the "0" state. If the chip enable input is being driven from TTL logic, a pull-up resistor is required from the gate output to +5V supply. The value of this resistor is not critical and can be in the 1K to 3KΩ range (See Figure 4).

Figure 4. Enable Input Strobing from TTL Logic

IH6208 APPLICATION INFORMATION (CONT.)

When the En input is driven from CMOS logic, no pullup is necessary. Fig. 5 shows the CD4009 driving the En input.

Figure 5

The Supply Voltage of the CD4009 does affect the switching speed of the IH6208 (with the same being true for Supply Voltage Levels). The chart below shows the effect, on $t_{transition}$ times, of supply varying from +4.5V to +5.5V.

CMOS OR TTL SUPPLY	TYPICAL $t_{transition}$ @ 25°C
+4.5V	400ns
+4.75V	300ns
+5.0V	250ns
+5.25V	200ns
+5.50V	175ns

The throughput rate can therefore be maximized by using a +5V to +5.5V supply for the Enable Strobe Logic.

The cases shown in Figures 4 and 5 deal with enable strobing when expandability to more than four differential channels is required. In these cases the En terminal acts as a third binary input. If four channel pairs or less are being multiplexed, the En terminal can be directly connected to +5V logic supply which would "enable" the IH6208 at all times.

IH6208 APPLICATION INFORMATION (CONT.)

APPLICATIONS

II. Using the IH6208 with supplies other than ±15V

The IH6208 can be used with power supplies ranging from ±6V to ±16V. The switch $r_{DS(ON)}$ will increase as the supply voltages decrease. However, the multiplexer error term (the product of leakage times $r_{DS(ON)}$ will remain approximately constant since leakage decreases as the supply voltages are reduced.

Caution must be taken to ensure that the chip enable (En) voltage is at least 0.7V below V_{CC} at all times. If this is not done the binary input strobing levels will not function properly. This may be achieved quite simply by connecting En (pin 2) to $+V_{CC}$ (pin 14) via a silicon diode as shown in Figure 6. If the IH6208 is hooked up in this type of a configuration a further requirement must be met — the strobe levels at A_0 and A_1 must be within 2.5V of the En voltage to define a binary "1" state. For the case shown in Figure 6 the En voltage is 11.3V which means that logic high at A_0 and A_1 is = +8.8V (logic low continues to be = 0.8V). In this configuration the IH6208 cannot be driven by TTL (+5V) or CMOS (+5V) logic. It can be driven by TTL open collector logic or CMOS logic with +12V supplies.

If the logic and the IH6208 have common supplies the En pin should again be connected to the supply through a silicon diode. In this case tying En to the logic supply directly will not work since it will violate the 0.7V differential voltage required between $+V_{CC}$ and En on the IH6208 (See Figure 7). A 1μf capacitor can be placed across the diode to minimize switching glitches.

Figure 6. IH6208 Connection Diagram for less than ±15V Supply Operation.

IH6208 APPLICATION INFORMATION

Figure 7. IH6208 Connection Diagram with Enable Input Strobing for less than ±15V Supply Operation.

III. Peak-to-Peak Signal Handling Capability

The IH6208 can handle input signals up to ±14V (actually -15V to +14.3V) when it has ±15V supplies. The input protection diode prevents the handling of signals up to +15V.

The electrical specifications of the IH6208 are guaranteed for ±10V signals but the specifications have very minor changes for ±14V signals. The notable changes would be slightly lower $r_{DS(on)}$ and slightly higher leakages.

PACKAGE DIMENSIONS

16 Pin Ceramic Dual-In-Line Package (DE)

16 Pin Plastic Dual-In-Line Package (PE)

INTERSIL

IH6216
CMOS 8-Channel Differential Analog Multiplexer

FEATURES

- **Pin Compatible with HI507, DG507 & AD7507**
- **±11V analog signal range**
- **r_{on} < 700 ohms over full signal and temperature range**
- **Break before make switching**
- **TTL and CMOS compatible strobe control**
- **Binary strobe control (3 strobe inputs controls 2 out of 16 channels).**
- **Two tier submultiplexing to facilitate expandability**
- **Power supply quiescent current less than 100μA**
- **No latch up or "S.C.R." action**
- **Very low leakage ≤ 100pA**

GENERAL DESCRIPTION

The IH6216 is a 2 out of 16 CMOS monolithic multiplexer. The part is a plug-in replacement for the DG507. Three line binary decoding is used so that the 16 channels can be controlled in pairs by the binary inputs; additionally a fourth input is provided to use as a system enable; if the enable input is 0V, none of the channels can be turned on. When the enable input is high (5V) the channels are sequenced by the 3 line binary inputs. The 3 strobe inputs are controlled by TTL logic or CMOS logic elements; a "0" corresponds to any voltage less than 0.8V and a "1" corresponds to any voltage greater than 3.0V; however the enable input (EN) *must* be taken to 5V to enable the system and less than 0.8V to disable the system.

FUNCTIONAL DIAGRAM

DECODE TRUTH TABLE

A_2	A_1	A_0	EN	ON SWITCH PAIR
X	X	X	0	NONE
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

LOGIC "1" = V_{AH} > 3V
LOGIC "0" = V_{AL} < 0.8V

PIN CONFIGURATION

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
IH6216MDI	-55°C to +125°C	28 pin DIP
IH6216CDI	0°C to 70°C	28 pin DIP
IH6216CPI	0°C to 70°C	28 pin Plastic DIP

ABSOLUTE MAXIMUM RATINGS

V_{IN} (A, EN) to Ground ..... −15V, V_1
V_S or V_D to V_1 ..... 0, −32V
V_S or V_D to V_2 ..... 0, 32V
V_1 to Ground 16V
V_2 to Ground ..... −16V
Current (Any Terminal) ..... 30 mA
Current (Analog Drain) ..... 20 mA
Current (Analog Source) ..... 20 mA
Operating Temperature ..... −55 to 125° C
Storage Temperature ..... −65 to 150° C
Power Dissipation (Package)* 1200mW
Lead Temperature (Soldering 10 sec) ..... 300 °C

*All leads soldered or welded to PC board. Derate 10 mW/° C above 70° C

ELECTRICAL CHARACTERISTICS

CHARACTERISTIC		MEASURED TERMINAL	NO TESTS PER TEMP	TYP 25° C	MAX LIMITS M SUFFIX −55° C	M SUFFIX 25° C	M SUFFIX 125° C	C SUFFIX 0° C	C SUFFIX 25° C	C SUFFIX 70° C	UNIT	TEST CONDITIONS (UNLESS OTHERWISE NOTED) V_1 = 15V, V_2 = −15V, Ground = 0 V_{EN} = +5V (Note 1)	
SWITCH	$r_{DS(ON)}$	S to D	16	480	600	600	700	650	650	750	Ω	V_D = 10V, I_S = −1.0mA	Sequence each switch on
			16	300	600	600	700	650	650	750		V_D = −10V, I_S = −1.0mA	$V_{A(L)}$=0.8V, $V_{A(H)}$=3V
	$\Delta r_{DS(ON)}$			20							%	$\Delta r_{DS(ON)} = \frac{r_{DS(ON)MAX} - r_{DS(ON)MIN}}{r_{DS(ON)}\ AVG.}$ −10V ≤ V_S 10V	
	$I_{S(OFF)}$	S	16	0.01		0.1	50		0.2	50	nA	V_S = 10V, V_D = −10V	V_{EN} = 0
			16	0.01		0.1	50		0.2	50		V_S = −10V, V_D = 10V	
	$I_{D(OFF)}$	D	2	0.1		0.2	100		0.4	100		V_D = 10V, V_S = −10V	
			2	0.1		0.2	100		0.4	100		V_D = −10V, V_S = 10V	
	$I_{D(ON)}$	D	16	0.1		0.2	100		0.4	100		$V_{S(All)}$ = V_D = 10V	Sequence each switch on
			16	0.1		0.2	100		0.4	100		$V_{S(All)}$ = V_D = −10V	$V_{A(L)}$=0.8V, $V_{A(H)}$=3V
INPUT	$I_{AN(ON)}$ or		3	.01		−10	−30		−10	−30	μA	V_A = 3.0V	
	$I_{AN(OFF)}$		3	.01		10	30		10	30		V_A = 15V	
	I_A	A_0 A_1 A_2 A_3	3			−10	−30		−10	−30		V_{EN} = 5V	All V_A = 0
		EN	1			−10	−30		−10	−30		V_{EN} = 0	
DYNAMIC	$t_{transition}$	D		0.6		1					μs	See Fig. 1	
	t_{open}	D		0.2								See Fig. 2	
	$t_{on(En)}$	D		0.8		1.5						See Fig. 3	
	$t_{off(En)}$	D		0.3		1							
	"OFF" Isolation	D		60							dB	V_{EN} = 0, R_L = 200Ω, C_L = 3 pF, V_S = 3 VRMS, f = 500 kHz	
	$C_{S(OFF)}$			5							pF	V_S = 0	V_{EN} = 0, f = 140 kHz to 1 MHz
	$C_{D(OFF)}$			20								V_D = 0	
	$C_{DS(OFF)}$			1								V_S = 0, V_D = 0	
SUPPLY	I_1	V_1	1	55		200			1000		μA	V_{EN} = 5V	All V_A = 0 OR 3V
	I_2	V_2	1	2		100			1000				
	I_1 Standby	V_1	1	1		100			1000			V_{EN} = 0	
	I_2 Standby	V_2	1	1		100			1000				

NOTE 1: See Section V. Enable Input Strobing Levels.

SWITCHING INFORMATION

Figure 2

Figure 3

IH6216 APPLICATIONS

I. 2 out of 32 channel multiplexer using 2 IH6216s.

Figure 4

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1a	
0	0	0	1	S2a	
0	0	1	0	S3a	
0	0	1	1	S4a	
0	1	0	0	S5a	
0	1	0	1	S6a	
0	1	1	0	S7a	
0	1	1	1	S8a	V_{OUT1}
1	0	0	0	S9a	
1	0	0	1	S10a	
1	0	1	0	S11a	
1	0	1	1	S12a	
1	1	0	0	S13a	
1	1	0	1	S14a	
1	1	1	0	S15a	
1	1	1	1	S16a	

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1b	
0	0	0	1	S2b	
0	0	1	0	S3b	
0	0	1	1	S4b	
0	1	0	0	S5b	
0	1	0	1	S6b	
0	1	1	0	S7b	
0	1	1	1	S8b	V_{OUT2}
1	0	0	0	S9b	
1	0	0	1	S10b	
1	0	1	0	S11b	
1	0	1	1	S12b	
1	1	0	0	S13b	
1	1	0	1	S14b	
1	1	1	0	S15b	
1	1	1	1	S16b	

IH6216 APPLICATIONS

II. 2 out of 32 channel multiplexer using 2 IH6216s; using an IH5043 for submultiplexing.

Figure 5

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1a	
0	0	0	1	S2a	
0	0	1	0	S3a	
0	0	1	1	S4a	
0	1	0	0	S5a	
0	1	0	1	S6a	
0	1	1	0	S7a	
0	1	1	1	S8a	V_{OUT1}
1	0	0	0	S9a	
1	0	0	1	S10a	
1	0	1	0	S11a	
1	0	1	1	S12a	
1	1	0	0	S13a	
1	1	0	1	S14a	
1	1	1	0	S15a	
1	1	1	1	S16a	

DECODE TRUTH TABLE

A_3	A_2	A_1	A_0	ON SWITCH	
0	0	0	0	S1b	
0	0	0	1	S2b	
0	0	1	0	S3b	
0	0	1	1	S4b	
0	1	0	0	S5b	
0	1	0	1	S6b	
0	1	1	0	S7b	
0	1	1	1	S8b	V_{OUT2}
1	0	0	0	S9b	
1	0	0	1	S10b	
1	0	1	0	S11b	
1	0	1	1	S12b	
1	1	0	0	S13b	
1	1	0	1	S14b	
1	1	1	0	S15b	
1	1	1	1	S16b	

IH6216 APPLICATIONS

III. 2 out of 64, using 4 IH6216s and 2 IH5043s as submultiplexers.

Figure 6

IV. GENERAL NOTE ON EXPANDABILITY OF IH6216

The IH6216 is a two tier multiplexer wherein 8 pairs of input channels are routed to a pair of outputs in blocks of 4 channels at a time. Each block of 4 input channels is routed to one common output channel; thus the submultiplexed system looks like 4 bloks of 4 inputs routed to 4 different outputs, and the 4 outputs are tied in pairs. Thus 20 switches are needed to handle the 16 channels of information. The advantage of this scheme is lower output capacity and lower leakage than a system with all 8 channels tied to one common output. Also the expandability into 2 out of 32, 64, 128, etc. is facilitated. Figures 4, 5, and 6 show how the IH6216 is expanded.

Figure 4 shows a 2 out of 32 multiplexer using 2 of the IH6216s. Since the 6216 is itself a 2 tier mux, the system as shown is basically a 2 tier system. Corresponding output points of each of the 6216 are connected together, and the enable input strobe is used as the A_3 input. Since each output (pins 2 and 28) corresponds to an "on" fet and an "off" fet, the overall system looks like 1 "on" fet and 3 "off" fets for each of the V_{out1} and V_{out2} outputs. Thus the output leakage will be 1 $I_{D(on)}$ plus 3 $I_{D(off)}$s or about 0.4 nA typical, at room temperature. Thruput speed will be typically 0.8μs for t_{on} and 0.3μs for t_{off}. Thruput channel resistance will be in the 500 ohm area.

Figure 5 shows the same 2 out of 32 mux as Figure 4, except that a third tier of submultiplexing is added to further reduce leakage and output capacity. The IH5043 has typical on resistance of 50 ohms (max. is 75 ohms) so it only increases thruput channel resistance from the 500 ohms of Figure 4 to about 550 ohms for Figure 5. Thruput channel speed is a little slower by about 0.5μs for both on and off time. Output leakage is about 0.2 nA typical.

Figure 6 shows a 2 out of 64 mux using 3 tier muxing (similar to Figure 5 application). Again the Intersil IH5043 is used to get the third tier of muxing. Each V_{out} point will see 3 off channels and 1 on channel at any time so that the typical leakages will be about 0.4 nA. Thruput channel resistance will be in the 550 ohm area and thruput switching speeds will be about 1.3μs for on time and 0.8μs for off time.

The IH5043 was chosen as the third tier of the mux because it will switch the same AC signals as the IH6216 (typically plus and minus 15V) and break before make switching is guaranteed so that the muxing system remains a break-before-make. Also power supply quiescent currents are typically 1μA from any supply, so that no excessive system power is generated. Also the logic of the 5043 is such that it can be tied directly to the enable input (as shown in the figures) with no extra logic being required.

V. ENABLE INPUT STROBING LEVELS

The enable input (EN) acts as an enabling or disabling pin for the IH6216 when used as a 2 out of 16 channel mux; however, when expanding the mux to more than 16 channels, the EN pin acts as another address input. As an example, we see in Figures 4 and 5 that the EN pin acts as the A_3 input.

For the system to function properly the EN input (pin 18) must go to 5V ±5% for the high state and less than 0.8V for the low state. When using TTL logic, a pull-up resistor should be used to pull the output voltage up to 5V; this resistor should be 1k ohm or less. When using CMOS logic, the high state goes up to the power supply so no pull-up is required.

3

PACKAGE DIMENSIONS

28 Pin Ceramic Package

28 Pin Plastic Package

28 Pin CerDIP Package

NOTE: This multiplexer does not require external resistors and/or diodes to eliminate what is commonly known as a latch up or SCR action. Because of the elimination of external resistors in each channel the $r_{DS(ON)}$ of the switch is maintained at specified values.

INTERSIL

D112/D113/D120/D121
2-Channel FET Switch Drivers
Military Series −55°C to +125°C

- Two separate channels
- J-FET Collector Pull-up
- Interfaces 5V Logic
- Two switching speeds to choose from

GENERAL DESCRIPTION

This series contains 2 separate channels each with J-FET collector pull-up, in one package. Two switching speeds are provided for speed-power ratio selection.

ABSOLUTE MAXIMUM RATINGS

Pos. Supply to Emitter ($V_{CC} - V_{EE}$)	33V
Output to Emitter ($V_{OUT} - V_{EE}$)	33V
Logic Supply to Emitter ($V_L - V_{EE}$)	30V
Ref. to Emitter ($V_R - V_{EE}$)	31V
Input to Ref. ($V_{IN} - V_R$)	2V
Ref. to Input ($V_R - V_{IN}$)	6V
Logic Supply to Input ($V_L - V_{IN}$)	±6V
Current (any pin)	30 mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Dissipation (Note)	**750mW**
Lead Temperature (soldering, 10 sec.)	**300°C**

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10 mW/°C.

SCHEMATIC AND LOGIC DIAGRAMS

D112 & D120

D113 & D121

ORDERING INFORMATION

D 113 M FD

- Package: FD – 14 Pin Flat Pack ¼" x ¼"
  DD – 14 Pin Hermetic Dip
- Temperature Range:
  M – −55°C to +125°C
  I – −20°C to +85°C
  C – 0°C to +70°C
- Device Chip Type
- Analog Switch Driver

PACKAGE OUTLINES

14-Pin Ceramic Package

Flat Package

PRODUCT CONDITIONING

The following processes are preformed 100% in accordance with MIL-STD-883.

Precap Visual – Method 2010, Cond. B.
Stabilization Bake – Method 1008
Temperature Cycle – Method 1010
Centrifuge – Method 2001, Cond. E
Hermeticity – Method 1014, Cond. A, C.
(Leak Rate $< 5 \times 10^{-8}$ atm cc/s)

ELECTRICAL CHARACTERISTICS (per channel)

Test conditions unless otherwise specified are as follows: V_{EE} = −20V, V_{CC} = +10V, I_{OUT} = 0, V_L = 4.5 V, V_R = 0. Output and power supply measurements based on specified input conditions.

		PARAMETER (NOTE)	LIMIT					CONDITION
			−55°C	25°C	125°C	MAX/MIN	UNITS	
INPUT	D112 D120	$I_{IN(ON)}$	1.5	1.5	1.2	MAX	mA	V_{IN} = 0.4V
		$I_{IN(OFF)}$	1.0	1.0	20		μA	V_{IN} = 4.1V
	D113 D121	$V_{IN(ON)}$	1.3	1.0	0.8		V	I_{IN} = 1 mA
		$I_{IN(OFF)}$	1.0	1.0	100		μA	V_{IN} = 0.4V
OUTPUT	D112 D113	$I_{DSS(OFF)}$	−2.2	−1.8	−1.8	MAX	mA	V_{OUT} = −20V, V_{EE} = −20V
		$I_{DSS(OFF)}$	−0.6	−0.4	−0.4	MIN		
	D120 D121	$I_{DSS(OFF)}$	−7.5	−5.7	−5.1	MAX		
		$I_{DSS(OFF)}$	−3.2	−3.0	−2.0	MIN		
	ALL	$V_{OUT(OFF)}$	9.9	9.9	9.8	MIN	V	I_{OUT} = −10 μA
		$V_{OUT(ON)}$	−19.2	−19.2	−19.0	MIN	V	I_{OUT} = 1 mA
POWER SUPPLY	D112	$I_{L(ON)}$		2.0		MAX	mA	One channel ON
		$I_{CC(ON)}$		1.8				
		$I_{EE(ON)}$		3.8				
	D120	$I_{L(ON)}$		2.0				
		$I_{CC(ON)}$		5.7				
		$I_{EE(ON)}$		7.7				
	D113	$I_{R(ON)}$		0.5				
		$I_{CC(ON)}$		1.8				
		$I_{EE(ON)}$		2.8				
	D121	$I_{R(ON)}$		0.5				
		$I_{CC(ON)}$		5.7				
		$I_{EE(ON)}$		6.7				
	ALL	$I_{L(OFF)}$		250		MAX	μA	All channels OFF
		$I_{R(OFF)}$		150				
		$I_{CC(OFF)}$		50				
		$I_{EE(OFF)}$		250				
SWITCHING TIMES	D112 D113	t_{OFF}		1.5		MAX	μs	(See Switching Times)
		t_{ON}		0.25				
	D120 D121	t_{OFF}		0.60				
		t_{ON}		0.25				

NOTE: (OFF) and (ON) subscripts refer to the conduction state of the driver.

3

TYPICAL PERFORMANCE CURVES

OUTPUT RISE TIME VS TEMPERATURE AND LOAD CAPACITANCE (D112, D113)

OUTPUT RISE TIME VS TEMPERATURE AND LO. CAPACITANCE (D120, D12.

SWITCHING TIMES VS TEMPERATURE

$I_{DSS(OFF)}$ VS TEMPERATURE

$I_{OUT(OFF)}$ VS TEMPERATURE

R_{SAT} VS TEMPERATURE

3

APPLICATION TIPS

The recommended resistors for interfacing with RTL, DTL, and T^2L Logic is shown in figures 1 and 2.

Figure 1. D112 and D120 Interface

Figure 2. D113 and D121 Interface

Enable Control

The V_R and V_L pins can be used as a STROBE or an ENABLE control. The requirements for the enable driver are as follows: I_L (ON) X no. of channels used for the D112 & D120 and I_R (ON) X no. of channels used for the D113 & D121. The voltage at V_L must be greater than the voltage at V_{IN} by at least +4V.

3

SWITCHING TIMES

Circuit Diagrams

INTERSIL

D123/D125
6-Channel FET Switch Drivers
Military Series −55°C to +125°C

FEATURES

- Provides dc level shifting between low-level Logic and MOS-FET or J-FET switches
- External Collector Pull-ups required
- Direct interface with G116, G117, G119, G115, and G123 MOS-FET switches

GENERAL DESCRIPTION

The D123 and D125 monolithic bi-polar drivers convert low-level positive signals (0 & +5V) to the high level positive and negative voltages necessary to drive FET switches. One lead can be used to provide an enabling capability.

ABSOLUTE MAXIMUM RATINGS

Input-to-Emitter Voltage ($V_{IN} - V_{EE}$)	33V
Output-to-Emitter Voltage ($V_O - V_{EE}$)	33V
Logic Supply-to-Emitter Voltage ($V_L - V_{EE}$)	27V
Input-to-Reference Voltage ($V_{IN} - V_R$)	2V
Input-to-Logic Supply Voltage ($V_{IN} - V_L$)	+6V
Reference-to-Emitter Voltage ($V_R - V_{EE}$)	31V
Maximum Dissipation (Note)	750 mW
Current (any pin)	30 mA
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature of 70°C. Derate 10 mW/°C for higher ambient temperature.

SCHEMATIC AND LOGIC DIAGRAMS

D123

D125

ORDERING INFORMATION

D 123 M FD

- FD — Package: FD – 14 Pin Flat Pack ¼" x ¼"; DD – 14 Pin Hermetic Dip
- M — Temperature Range: M – −55°C to +125°C; I – −20°C to +85°C; C – 0°C to +70°C
- 123 — Device Chip Type
- D — Analog Switch Driver

PACKAGE OUTLINES

NOTE: All dimensions in inches.

Flat Package

FD Package
TO-86

Ceramic Dual-In-Line Package

DD Package
TO 116

PRODUCT CONDITIONING

Units receive the following treatment before final electrical test:

Thermal Shock
+100 to 0°C for 5 cycles
Centrifuge
20,000g centrifuge in the Y. plane.
Hermeticity
Helium and gross leak tests.

ELECTRICAL CHARACTERISTICS

Test conditions unless otherwise specified are as follows: V_{EE} = −20V, V_L = 4.5V, I_{OUT} = 0, V_R = 0. Output and power supply measurements based on specified input conditions.

		PARAMETER	MAX LIMIT				CONDITIONS
			−55°C	25°C	125°C	UNITS	
INPUT	D123	$I_{IN(OFF)}$	1	1	100	μA	V_{IN} = 0.4V
		$V_{IN(ON)}$	1.3	1	0.8	V	I_{IN} = 1 mA
	D125	$I_{IN(OFF)}$	1	1	20	μA	V_{IN} = 4.1V
		$I_{IN(ON)}$	1.5	1.5	1.2	mA	V_{IN} = 0.5V
OUTPUT	D125 & D123	$I_{OUT(OFF)}$	0.1	0.1	10	μA	V_{OUT} = +10V
		$V_{OUT(ON)}$	−19.7	−19.7	−19.5	V	I_{OUT} = 1 mA
		$V_{OUT(ON)}$	−19.2	−19.2	−19.0	V	I_{OUT} = 4 mA
POWER SUPPLY	D123	$I_{R(ON)}$ (1)	0.5	0.5	0.5	mA	I_{OUT} = 0 for ON measurements. V_{OUT} = +10V for OFF measurements.
		$I_{R(OFF)}$ (2)	1	1	150	μA	
		$I_{EE(ON)}$ (1)	1	1	1	mA	
		$I_{EE(OFF)}$ (2)	2	2	200	μA	
	D125	$I_{L(ON)}$ (1)	2	2	1.9	mA	
		$I_{L(OFF)}$ (2)	1	1	100	μA	
		$I_{EE(ON)}$ (1)	2	2	1.9	μA	
		$I_{EE(OFF)}$ (2)	2	2	200	μA	
SWITCHING TIMES	D125 & D123	$t_{(on)}$		250		ns	I_{OUT} = 1 mA C_{OUT} (3) = 10 pF
		$t_{(off)}$ (4)		800		ns	(See Switching Times)
	D125 & D123	$t_{(on)}$		250		ns	I_{OUT} = 4 mA C_{OUT} (3) = 10 pF
		$t_{(off)}$ (5)		600		ns	(See Switching Times)

NOTES: (1) One channel ON, 5 channels OFF.
(2) All channels OFF.
(3) Add 30 ns per pF for 1 mA and add 8 ns per pF for 4 mA for additional capacitive loading.
(4) For Dual-In-Line package add 120 ns to $t_{(off)}$.
(5) For Dual-In-Line package add 30 ns to $t_{(off)}$.

SWITCHING TIMES

Circuit Diagrams

TYPICAL CHARACTERISTICS

$t_{off(delay)}$ VS $I_{IN(PEAK)}$ D123

SWITCHING TIMES VS TEMPERATURE D123 AND D125 (SEE NOTES 4 AND 5)

$V_{IN(ON)}$ VS TEMPERATURE D123

I_{IN} VS V_{IN} D123

V_{SAT} VS TEMPERATURE D123 AND D125

$I_{OUT(OFF)}$ VS TEMPERATURE D123 AND D125

APPLICATION TIPS

Interfacing the D123 and D125

In order to meet all the specifications on this data sheet, certain requirements must be met by the drive circuitry.

The D125 can be turned ON easily, but care must be exercised to insure turn-off. Keeping $V_L - V_{IN} \leq 0.4V$ is a must to insure turn-off. To accomplish this a shunt resistor must be added to supply the leakage current (I_{CES}) for DTL devices. Since I_{CES} = 50 μA, a 0.4V/0.05 mA = 8k or less should be used. For T^2L devices using a 2k resister will insure turn-off with up to 200 μA of leakage current.

Using the ENABLE Control

Device pins V_R or V_L, can be used to enable the D123 or D125 drivers. For the D123 the enabling driver must sink $I_{R(ON)}$ X no. of channels used. For the D125, $I_{L(ON)}$ X no. of channels used must be sourced with a voltage at least +4V greater than V_{IN}.

APPLICATIONS

Using INTERSIL'S MOS-FET SWITCH G117 with either the D123 or D125 drivers provides a reliable means of providing up to 5 channels with a series block for multiplexing applications.

5-Channel Multiplexer

INTERSIL

D129
4-Channel MOS FET Switch Driver with Decode

FEATURES

- Quad Three-Input Gates Decode Binary Counter to Four Lines
- Inputs Compatible with Low Power TTL and DTL, I_F = 200μA Max
- Output Current Sinking Capability 10mA
- External Pull-Up Elements Required
- Compatible with G115 and G123 Series Multichannel MOS FET Switches which include Current-Limiter Pull-Up FETs

ORDERING INFORMATION

D 129 M DD

- Package:
  - FD 14 pin flat (¼" x ¼")
  - DD 14 pin DIL Ceramic
- Temperature Range:
  - M – -55°C to +125°C
  - I – -20°C to + 85°C
- Device Chip Type
- Analog Switch Driver

GENERAL DESCRIPTION

The D129 is a 4-channel driver with binary decode input. It has been designed to provide the DC level-shifting required to interface low-level logic outputs (0.7 to 2.2V) to field-effect transistor inputs (up to 50V peak-to-peak). For a 5V input logic supply, the V_{EE} terminal can be set at any voltage between -5V and -30V. The output transistor is capable of sinking 10mA and will stand-off up to 50V above V_{EE} in the off-state.

The ON state of the driver is controlled by a logic "1" (open) on all three input logic lines, while the OFF state of the driver is achieved by pulling any one of the three inputs to a logic "0" (ground).

The 4-channel driver is internally connected such that each one can be controlled independently or decoded from a binary counter.

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SCHEMATIC AND LOGIC DIAGRAMS

PACKAGE OUTLINES

14-PIN CERAMIC DUAL-IN-LINE PACKAGE

FLAT PACKAGE

ABSOLUTE MAXIMUM RATINGS

$V_O - V_{EE}$	50V
$V_R - V_{EE}$	33V
$V_L - V_R$	8V
$V_{IN} - V_R$	±6V
Current (any terminal)	30mA
Storage Temperature	-65°C to +150°C
Operating Temperature	-55°C to +125°C
Power Dissipation (note)	750mW
Lead Temperature (Soldering, 10 sec)	300°C

Note: Dissipation rating assumes device mounted with all leads welded or soldered to pc board in ambient temperature of 70°C. Derate 10mW/°C for higher ambient termperatures.

ELECTRICAL CHARACTERISTICS

Test conditions unless otherwise specified $V_{EE} = -20V$, $V_R = 0V$, $V_L = 5V$

	PARAMETER		CONDITIONS		MAX LIMITS D129M -55°C	D129M 25°C	D129M 125°C	D129I -20°C	D129I 25°C	D129I 85°C	UNIT
OUT	V_{OL}	Output Voltage, Low	$I_O = 10mA$	$V_{IN} = 2.2V$, $V_L = 4.5V$	-19.3	-19.3	-19	-19.25	-19.25	-19	V
OUT	V_{OL}	Output Voltage, Low	$I_O = 1mA$	$V_{IN} = 2.2V$, $V_L = 4.5V$	-19.8	-19.8	-19.75				V
OUT	I_{OH}	Output Current, High	$V_O = 10V$, $V_{IN} = 0.7V$		0.1	0.1	20	0.2	0.2	10	μA
IN	I_{INH} *	Input Current Input Voltage High	$V_{IN} = 5V$ Input Under Test, $V_{IN} = 0$ All Other Inputs		0.25	0.25	5	1	1	5	μA
IN	I_{INL} *	Input Current, Input Voltage Low	$V_{IN} = 0$, $V_L = 5.5V$		-250	-200	-160	-250	-225	-200	μA
TIME	t_{on}	Turn-ON Time	See Switching Time Test Circuit			0.25			0.3		μs
TIME	t_{off}	Turn-OFF Time	See Switching Time Test Circuit			1.0			1.5		μs
SUPPLY	I_{EE}	Negative Supply Current	$V_{EE} = -20V$, $V_L = 5.5V$	One Channel "ON"		- 2			- 2.25		mA
SUPPLY	I_L	Logic Supply Current	$V_{EE} = -20V$, $V_L = 5.5V$	One Channel "ON"		3			3.3		mA
SUPPLY	I_{EE}	Negative Supply Current	$V_{EE} = -20V$, $V_L = 5.5V$	All $V_{IN} = 0$, All Channels "OFF"		-10			-25		μA
SUPPLY	I_L	Logic Supply Current	$V_{EE} = -20V$, $V_L = 5.5V$	All $V_{IN} = 0$, All Channels "OFF"		0.75			1		mA

* Per gate Input

SWITCHING TIME AND TEST CIRCUIT

$t_f = 100ns$
$t_r = 100ns$
$t_{pw} = 1\mu s$
$f = 100K$ Hz

INTERSIL

DG111/DG112
2-Channel Drivers with MOS-FET Switches Military Series
−55°C to +125°C

FEATURES

- Each Channel Completely Isolated
- 20V P-P Switching Capability
- Zener Diode Protected Gates
- MOS-FET Current-Source Pull-Up

GENERAL DESCRIPTION

This driver-switch series provides two completely isolated switches per package. The collector supply (V_{CC}) may be operated at different voltages for each switch. Two driver input configurations are available for inverting and non-inverting applications. For minimum propagation delay as well as optimum speed and power, a terminal is supplied for biasing the constant-current MOS-FET pull-up.

ABSOLUTE MAXIMUM RATINGS

Collector to Emitter ($V_{CC} - V_{EE}$)	33V
Collector to Pull-up ($V_{CC} - V_P$)	33V
Drain to Emitter ($V_D - V_{EE}$)	32V
Drain to Source ($V_D - V_S$)	28V
Source to Drain ($V_S - V_D$)	28V
Source to Emitter ($V_S - V_{EE}$)	32V
Logic to Emitter ($V_L - V_{EE}$)	33V
Ref. to Emitter ($V_R - V_{EE}$)	31V
Ref. to Input ($V_R - V_{IN}$)	+6V
Logic to Input ($V_L - V_{IN}$)	±6V
Current (Any Terminal)	30 mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Dissipation (Note)	750mW
Lead Temperature (soldering, 10 sec.)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature of +70°C. Derate 10 mW/°C for higher ambient temperature.

ORDERING INFORMATION

DG 111 M FD

- FD — Package
  - FD – 14 pin Flat Package
  - DD – 14 pin Hermetic DIP
- M — Temperature Range
  - M – Military (−55°C to +125°C)
  - I – Industrial (−20°C to +85°C)
  - C – Commercial (0°C to +70°C)
- 111 — Device Chip Type
- DG — Analog Driver Switch Combination

TRUTH TABLE

DG112		DG111		Switch Cond.
V_{IN}	V_R	V_{IN}	V_L	
L	L	L	L	OFF
H	L	L	H	ON
L	H	H	L	OFF
H	H	H	H	OFF

L = 0V, H = +V

PRODUCT CONDITIONING

The following processes are performed 100% in accordance with MIL-STD-883.

Precap Visual—Method 2010, Cond. B
Stabilization Bake—Method 1008
Temperature Cycle—Method 1010
Centrifuge—Method 2001, Cond. E
Hermeticity—Method 1014, Cond. A, C
(Leak Rate $< 5 \times 10^{-8}$ atm cc/s)

ELECTRICAL CHARACTERISTICS

Test conditions unless otherwise specified are as follows: $V_R = 0$, $V_L = 4.5V$, $V_{CC} = 10V$, $V_{EE} = -20V$, and $P = -20V$. Input ON and OFF test conditions are used for output and power supply specifications.

		PARAMETER (NOTE)	MAX LIMIT -55°C	MAX LIMIT 25°C	MAX LIMIT 125°C	UNITS	CONDITIONS	
INPUT	DG111	$I_{IN(OFF)}$	10	10	20	μA	$V_{IN} = 4.1V$	
		$I_{IN(ON)}$	-0.7	-0.7	-0.7	mA	$V_{IN} = 0.5V$	
	DG112	$I_{IN(OFF)}$	1	1	100	μA	$V_{IN} = 0.4V$	
		$V_{IN(ON)}$	1.3	1.0	0.8	V	$I_{IN} = 1mA$	
OUTPUT	DG111 DG112	$r_{DS(ON)}$	100	100	125	Ω	$V_D = 10V$	$I_S = -100\ \mu A$
			200	200	250	Ω	$V_D = 0$	
			450	450	600	Ω	$V_D = -10V$	
		$I_{D(ON)}$		1	1000	nA	$V_D = 10V$, $I_S = 0$	
		$I_{D(OFF)}$		-1	-1000	nA	$V_S = 10V$, $V_D = 10V$	
		$I_{S(OFF)}$		-1	-1000	nA	$V_D = 10V$, $V_S = -10V$	
POWER SUPPLY	DG111	$I_{L(ON)}$		3		mA	One Channel ON	
	DG112	$I_{R(ON)}$		-0.5				
	DG111	$I_{CC(ON)}$		3				
	DG112	$I_{EE(ON)}$		-6				
	DG111 DG112	$I_{CC(OFF)}$		10		μA	All Channels OFF	
		$I_{L(OFF)}$		10				
		$I_{R(OFF)}$		-15				
		$I_{EE(OFF)}$		-20				
SWITCHING TIMES	DG111 DG112	t_{ON}		300		ns	See Switching Times	
		t_{OFF}		1		μs		

NOTE: (OFF) and (ON) subscripts refer to the conduction state of the MOS-FET switch.

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APPLICATION TIPS

The recommended resistor values for interfacing with RTL, DTL, and T^2L Logic is shown in figs. 1 and 2.

Figure 1. DG111 Interface

Figure 2. DG112 Interface

Enable Control

The V_R and V_L terminals can be used as a strobe or an enable control. The requirements for sinking current at V_R or sourcing current at V_L are: $I_{L(ON)}$ x no. of channels used, for DG111, and $I_{R(ON)}$ x no. of channels used, for the DG112. The voltage at V_L must be greater than V_{IN} for $V_{IN} < 4V$. V_L must be at least +4V for $V_{IN} > 4V$.

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SWITCHING TIMES

TYPICAL CHARACTERISTICS

r_{DS} vs V_D OR V_S

SWITCHING TIMES vs TEMPERATURE (DG111, DG112)

I_{IN} vs V_{IN} (DG112)

PACKAGE OUTLINES

3

Flat Package

NOTE: All dimensions in inches.

FD Package

Ceramic Dual-In-Line Package

NOTE: All dimensions in inches.

DD Package

INTERSIL

DG116/DG118/DG123/DG125 4 and 5-Channel Driver-MOS-FET Switch Combinations Military Series −55°C to +125°C

FEATURES

- Available With and Without Programmable Constant Current pull-up
- Zener Protection on All Gates
- P-Channel Enhancement-Type MOS-FET Switches
- Each Switch Summed to One Common Point

GENERAL DESCRIPTION

This series includes devices with four and five channel switching capability. Each channel is composed of a driver and a MOS-FET switch. Two driver versions are supplied for inverting and noninverting applications. A MOS-FET, used as a current source provides an active pull-up for faster switching.

An external biasing connection is brought out for biasing the current source for optimization of speed and power.

ABSOLUTE MAXIMUM RATINGS

Collector to Emitter ($V_{CC} - V_{EE}$)	33V
Collector to pull-up ($V_{CC} - V_P$)	33V
Drain to Emitter ($V_D - V_{EE}$)	32V
Source to Emitter ($V_S - V_{EE}$)	32V
Drain to Source ($V_D - V_S$)	28V
Source to Drain ($V_S - V_D$)	28V
Logic to Emitter ($V_L - V_{EE}$)	33V
Reference to Emitter ($V_R - V_{EE}$)	31V
Reference to Input ($V_R - V_{IN}$)	6V
Logic to Input ($V_L - V_{IN}$)	±6V
Input to Emitter ($V_{IN} - V_{EE}$)	33V
Current (any terminal)	30 mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Dissipation (Note)	750mW
Lead Tempertature (soldering, 10 sec.)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature of 70°C. Derate 10mW/°C for higher ambient temperature.

ORDERING INFORMATION

DG 116 M FD

- Package
  - FD – 14 pin Flat Package
  - DD – 14 pin Hermetic DIP
- Temperature Range
  - M – Military (−55°C to +125°C)
  - I – Industrial (−20°C to +85°C)
  - C – Commercial (0°C to +70°C)
- Device Chip Type
- Analog Driver Switch Combination

TRUTH TABLE

DG116, DG123		DG118, DG125		Switch Cond.
V_{IN}	V_R	V_{IN}	V_L	
L	L	L	L	OFF
H	L	L	H	ON
L	H	H	L	OFF
H	H	H	H	OFF

L = 0V, H = +V

PRODUCT CONDITIONING

The following processes are performed 100% in accordance with MIL-STD-883.

Precap Visual-Method 2010, Cond. B.
Hermeticity-Method 1014, Cond. A,C.
Stabilization Bake-Method 1008.
Temperature Cycle-Method 1010.
Centrifuge-Method 2001, Cond. E.
(Leak $< 5 \times 10^{-8}$ atm. cc/s)

ELECTRICAL CHARACTERISTICS

Test conditions unless specified otherwise are as follows: V_L = 4.5V, V_R = O, V_{EE} = −20V, and P = −20V. Input ON and OFF test conditions used for output and power supply specifications.

		PARAMETER (NOTE)	MAX LIMITS				CONDITIONS
			−55°C	+25°C	+125°C	UNITS	
INPUT	DG116 DG123	$I_{IN(OFF)}$	1	1	100	μA	V_{IN} = 0.4V
		$V_{IN(ON)}$	1.3	1.0	0.8	V	I_{IN} = 1 mA
	DG118 DG125	$I_{IN(OFF)}$	1	1	20	μA	V_{IN} = 4.1V
		$I_{IN(ON)}$	-0.7	-0.7	-0.7	mA	V_{IN} = 0.5V
OUTPUT	All circuits	$r_{DS(ON)}$	100	100	125	Ω	V_D = 10V, I_S = -1mA
			200	200	250	Ω	V_D = 0, I_S = −100 μA
			450	450	600	Ω	V_D = −10V, I_S = −100 μA
		$I_{D(ON)}$		4	4000	nA	V_D = 10V, $I_{S(all)}$ = 0
		$I_{D(OFF)}$		−4	−4000	nA	$V_{S(all)}$ = 10V, V_D = −10V
		$I_{S(OFF)}$		−1	−1000	nA	V_D = 10V, V_S = −10V
POWER SUPPLY	All circuits	$I_{CC(ON)}$		3		mA	One Channel (ON)
		$I_{L(ON)}$		3		mA	
		$I_{R(ON)}$		−0.5		mA	
		$I_{EE(ON)}$		−6		mA	
	All circuits	$I_{CC(OFF)}$		10		μA	All Channels (OFF)
		$I_{L(OFF)}$		10		μA	
		$I_{R(OFF)}$		−15		μA	
		$I_{EE(OFF)}$		−20		μA	
SWITCHING TIMES	All circuits	$t_{(ON)}$		0.3		μs	See Switching Times
		$t_{(OFF)}$		1		μs	

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the MOS-FET switch for the given test condition.

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APPLICATION TIPS

The recommended resistor values for interfacing RTL, DTL, and T^2L Logic are shown in Figures 1 and 2.

Figure 1. DG118 and DG125 Interface

Figure 2. DG116 and DG123 Interface

Enable Control

The V_R and V_L terminals can be used as either a Strobe or an Enable control. The requirements for sinking current at V_R or sourcing current at V_L are: $I_{L(ON)}$ x No. of channels used, for DG118 and DG125, and $I_{R(ON)}$ x No. of channels used, for the DG116 and DG123 devices. The voltage at V_L must be greater than the voltage at V_{IN} by at least +4V.

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SWITCHING TIMES

DG116, 123

DG118, 125

TYPICAL CHARACTERISTICS

I_{IN} vs V_{IN} (DG116, DG123)

SWITCHING TIMES vs TEMPERATURE

r_{DS} vs V_D or V_S

PACKAGE OUTLINES

3

Flat Package

NOTE: All dimensions in inches.
FD Package

Ceramic Dual-In-Line Package

NOTE: All dimensions in inches.
DD Package

INTERSIL

DG120/DG121
3-Channel Drivers with Differential Switches
Military Series −55°C to +125°C

FEATURES

- 3-Channel With Normally-Off MOS-FET Switches in One Package
- $\Delta r_{DS(ON)}$ Matched to Better Than 30Ω.

GENERAL DESCRIPTION

This series is composed of three channels in one package. Each channel is composed of two matched MOS-FET switches for differential input requirements. Two driver configurations are available for inverting and noninverting applications. A MOS-FET used as a current source provides an active pull-up load for faster switching.

ABSOLUTE MAXIMUM RATINGS

Collector to Emitter ($V_{CC} - V_{EE}$)	33V
Collector to pull-up ($V_{CC} - V_P$)	33V
Drain to Emitter ($V_D - V_{EE}$)	32V
Source to Emitter ($V_S - V_{EE}$)	32V
Drain to Source ($V_D - V_S$)	28V
Source to Drain ($V_S - V_D$)	28V
Logic to Emitter ($V_L - V_{EE}$)	33V
Ref. to Emitter ($V_R - V_{EE}$)	31V
Ref. to Input ($V_R - V_{IN}$)	+6V
Logic to Input ($V_L - V_{IN}$)	±6V
Current (any terminal)	30 mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Dissipation (Note)	750mW
Lead Tempertature (soldering, 10 sec.)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature of 70°C. Derate 10mW/°C for higher ambient temperature.

DG120 (One Channel)

DG121 (One Channel)

ORDERING INFORMATION

DG 120 M FD

- FD — Package
  - FD – 14 pin Flat Package
  - DD – 14 pin Hermetic DIP
- M — Temperature Range
  - M – Military (−55°C to +125°C)
  - I – Industrial (−20°C to +85°C)
  - C – Commercial (0°C to +70°C)
- 120 — Device Chip Type
- DG — Analog Driver Switch Combination

TRUTH TABLE

DG120		DG121		Switch Cond.
V_{IN}	V_R	V_{IN}	V_L	
L	L	L	L	OFF
H	L	L	H	ON
L	H	H	L	OFF
H	H	H	H	OFF

L = 0V, H = +V

PRODUCT CONDITIONING

The following processes are performed 100% in accordance with MIL-STD-883.

Precap Visual—Method 2010, Cond. B.
Stabilization Bake—Method 1008.
Temperature Cycle—Method 1010.
Centrifuge—Method 2001, Cond. E.
Hermeticity—Method 1014, Cond. A,C
(Leak Rate $< 5 \times 10^{-8}$ atm. cc/s)

ELECTRICAL CHARACTERISTICS

Test conditions unless otherwise specified are as follows: $V_R = 0$, $V_L = 4.5V$, $V_{CC} = 10V$, $V_{EE} = -20V$. Input ON and OFF test conditions are used for output and power supply specifications.

		PARAMETER (NOTE 1)	MAX LIMIT -55°C	MAX LIMIT +25°C	MAX LIMIT +125°C	UNITS	CONDITIONS	
INPUT	DG120	$I_{IN(OFF)}$	1	1	100	μA	$V_{IN} = 0.4V$	
		$V_{IN(ON)}$	1.3	1.0	0.8	V	$I_{IN} = 1$ mA	
	DG121	$I_{IN(OFF)}$	10	10	20	μA	$V_{IN} = 4.1V$	
		$I_{IN(ON)}$	-0.7	-0.7	-0.7	mA	$V_{IN} = 0.5V$	
OUTPUT	Both	$r_{DS(ON)}$	100	100	125	Ω	$V_D = 10V$	$I_S = -1$mA
			200	200	250	Ω	$V_D = 0$	
			450	450	600	Ω	$V_D = -10V$	
		$\Delta r_{DS(ON)}$ (Note 2)		30		Ω	$V_D = -10V$, $I_S = -100\mu A$	
		$I_{D(ON)}$		3	3000	nA	$V_D = 10V$, $I_S = 0$	
		$I_{D(OFF)}$		-3	-3000		$V_{S(all)} = 10V$, $V_D = -10V$	
		$I_{S(OFF)}$		-1	-1000		$V_D = 10V$, $V_S = -10V$	
POWER SUPPLY	DG120	$I_{R(ON)}$		-0.5		mA	One Channel ON	
	DG121	$I_{L(ON)}$		3				
	Both	$I_{CC(ON)}$		3				
		$I_{EE(ON)}$		-6				
		$I_{CC(OFF)}$		10		μA	All Channels OFF	
		$I_{L(OFF)}$		10				
		$I_{R(OFF)}$		-15				
		$I_{EE(OFF)}$		-20				
SWITCHING TIMES	Both	t_{ON}		300		ns	See Switching Times	
		t_{OFF}		2		μs		

NOTE 1: (OFF) and (ON) subscripts refer to the conduction state of the MOS-FET switch.
NOTE 2: $\Delta r_{DS(ON)}$ is the resistance difference between differential switches.

3

APPLICATION TIPS

The recommended resistor values for interfacing RTL, DTL, and T^2L Logic are shown in Figures 1 and 2.

Figure 1. DG121 Interface

Figure 2. DG120 Interface

Enable Control

The V_R and V_L terminals can be used as a strobe or an enable control. The requirements for sinking current at V_R or sourcing current at V_L are: $I_{L(ON)}$ x No. of channels used, for DG121 and $I_{R(ON)}$ x No. of channels used, for DG120. The voltage at V_L must be greater than V_{IN} for $V_{IN} < 4V$. V_L must be at least +4V for $V_{IN} > 4V$.

3

APPLICATIONS

3-Channel Differential Multiplexer

SWITCHING TIMES

DG120

DG121

TYPICAL CHARACTERISTICS

r_{DS} vs V_D or V_S

SWITCHING TIMES vs TEMPERATURE

I_{IN} vs V_{IN} (DG120)

PACKAGE OUTLINES

Flat Package

NOTE: All dimensions in inches.
FD Package

Ceramic Dual-In-Line Package

NOTE: All dimensions in inches.
DD Package

INTERSIL

DG126/A, DG129/A, DG133/A, DG134/A, DG140/A, DG141/A, DG151/A, DG152/A, DG153/A, DG154A

2-Channel Drivers with SPST and DPST FET Switches

FEATURES

- Each channel complete—interfaces with most integrated logic
- Low OFF power dissipation, 1 mW
- Switches analog signals up to 20 volts peak-to-peak
- Low $r_{DS(ON)}$, 10 ohms max on DG140/A and DG141/A
- Switching times improved 100% – 'A' Versions.

GENERAL DESCRIPTION

These switching circuits contain two channels in one package, each channel consisting of a driver circuit controlling a SPST or DPST junction FET switch. The driver interfaces DTL, TTL or RTL logic signals for multiplexing, commutating, and D/A converter applications, which permits logic design directly with the switch function. Logic "1" at the input turns the FET switch ON, and logic "0" turns it OFF.

ABSOLUTE MAXIMUM RATINGS

Analog Signal Voltage ($V_A - V_2$ or $V_1 - V_A$)	30V
Total Supply Voltage ($V_1 - V_2$)	36V
Pos. Supply Voltage to Ref. Voltage ($V_1 - V_R$)	25V
Ref. Voltage to Neg. Supply Voltage ($V_R - V_2$)	22V
Power Dissipation (Note)	750 mW
Current (any terminal)	30 mA
Storage Temperature	-65 to +150°C
Operating Temperature	-55 to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10 mW/°C.

DUAL SPST

DG133/A($r_{DS(ON)}$ = 30 Ω)
DG134/A($r_{DS(ON)}$ = 80 Ω)
DG141/A($r_{DS(ON)}$ = 10 Ω)
DG151/A($r_{DS(ON)}$ = 15 Ω)
DG152/A($r_{DS(ON)}$ = 50 Ω)

DUAL DPST

DG126/A($r_{DS(ON)}$ = 80 Ω)
DG129/A($r_{DS(ON)}$ = 30 Ω)
DG140/A($r_{DS(ON)}$ = 10 Ω)
DG153/A($r_{DS(ON)}$ = 15 Ω)
DG154/A($r_{DS(ON)}$ = 50 Ω)

ORDERING INFORMATION

DG 1 26A DD

- DD — Package (See Outline Drawings)
- 26A — Device Chip Type
- 1 — Military Temperature Range (-55°C to 125°C)
- DG — Analog Gate

PACKAGE DIMENSIONS

Flat Package

FD Package

Ceramic Dual-In-Line Package

DD Package

PRODUCT CONDITIONING

The following processes are performed 100% in accordance with MIL-STD-883.

Precap Visual—Meth. 2010, Cond. B
Stabilization Bake—Meth. 1008
Temp. Cycle—Meth. 1010
Centrifuge—Meth. 2001, Cond. D
Hermeticity—Meth. 1014, Cond. A, C
(Leak Rate $<5 \times 10^{-8}$ atm cc/s)

ELECTRICAL CHARACTERISTICS PER CHANNEL

Applied voltages for all tests: DG126/A, DG129/A, DG133/A, DG134/A, DG140/A, DG141/A (V_1 = +12V, V_2 = −18V, V_R = 0) and DG151/A, DG152/A, DG153/A, DG154/A (V_1 = +15V, V_2 = −15V, V_R = 0). Input test condition which guarantees FET switch ON and OFF as specified is used for output and power supply specifications.

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT −55°	25°	125°	UNITS	TEST CONDITIONS
INPUT	$V_{IN(ON)}$	Input Voltage—On	All Circuits	2.9 min	2.5 min	2.0 min	Volts	V_2 = −12V
	$V_{IN(OFF)}$	Input Voltage—Off		1.4	1.0	0.6	Volts	V_2 = −12V
	$I_{IN(ON)}$	Input Current		120	60	60	μA	V_{IN} = 2.5V
	$I_{IN(OFF)}$	Input Leakage Current		0.1	0.1	2	μA	V_{IN} = 0.8V
SWITCH OUTPUT	$r_{DS(ON)}$	Drain-Source On Resistance	DG126/A DG134/A	80	80	150	Ω	
			DG129/A DG133/A	30	30	50	Ω	V_D = 10V, I_S = 1 mA
			DG140/A DG141/A	10	10	20	Ω	V_D = 10V, I_S = −10 mA
			DG151/A DG153/A	15	15	30	Ω	V_D = 7.5V, I_S = 1 mA
			DG152/A DG154/A	50	50	100	Ω	
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG126/A DG129/A DG133/A DG134/A		2	100	nA	$V_D = V_S$ = −10V
	$I_{S(OFF)}$	Source Leakage Current			1	100	nA	V_S = 10V, V_D = −10V
	$I_{D(OFF)}$	Drain Leakage Current			1	100	nA	V_D = 10V, V_S = −10V
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG140/A DG141/A		2	100	nA	$V_D = V_S$ = −10V
	$I_{S(OFF)}$	Source Leakage Current			10	1000	nA	V_S = 10V, V_D = −10V
	$I_{D(OFF)}$	Drain Leakage Current			10	1000	nA	V_D = 10V, V_S = −10V
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG151/A DG153/A		2	500	nA	$V_D = V_S$ = −7.5V
	$I_{S(OFF)}$	Source Leakage Current			10	1000	nA	V_S = 7.5V, V_D = −7.5V
	$I_{D(OFF)}$	Drain Leakage Current			10	1000	nA	V_D = 7.5V, V_S = −7.5V
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG152/A DG154/A		2	500	nA	$V_D = V_S$ = −7.5V
	$I_{S(OFF)}$	Source Leakage Current			2	200	nA	V_S = 7.5V, V_D = −7.5V
	$I_{D(OFF)}$	Drain Leakage Current			2	200	nA	V_D = 7.5V, V_S = −7.5V
POWER SUPPLY	$I_{1(ON)}$	Positive Power Supply Drain Current	All Circuits		3		mA	One Driver ON, V_{IN} = 2.5V
	$I_{2(ON)}$	Negative Power Supply Drain Current			−1.8		mA	
	$I_{R(ON)}$	Reference Power Supply Drain Current			−1.4		mA	
	$I_{1(OFF)}$	Positive Power Supply Leakage Current			25		μA	Both Drivers OFF, V_{IN} = 0.8V
	$I_{2(OFF)}$	Negative Power Supply Leakage Current			−25		μA	
	$I_{R(OFF)}$	Reference Power Supply Leakage Current			−25		μA	

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

3

ELECTRICAL CHARACTERISTICS PER CHANNEL (cont.)

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT -55°	25°	125°	UNITS	TEST CONDITIONS
SWITCHING	t_{ON}	Turn-On Time	DG126, DG129 DG133, DG134 DG152, DG154		600		ns	See Below
			DG126A, DG129A DG133A, DG134A DG152A, DG154A		300	500	ns	
	t_{OFF}	Turn-Off Time	DG126, DG129 DG133, DG134 DG152, DG154		1.6		µs	See Below
			DG126A, DG129A DG133A, DG134A DG152A, DG154A		0.8	1.2	µs	
	t_{ON}	Turn-On Time	DG140, DG141 DG151, DG153		1.0		µs	See Below
			DG140A, DG141A DG151A, DG153A		0.5	0.8	µs	
	t_{OFF}	Turn-Off Time	DG140, DG141 DG151, DG153		2.5		µs	See Below
			DG140A, DG141A DG151A, DG153A		1.25	1.8	µs	
POWER	P_{ON}	ON Driver Power	All Circuits		175		mW	Both Inputs V_{IN} = 2.5V
	P_{OFF}	OFF Driver Power			1		mW	Both Inputs V_{IN} = 1V

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

SWITCHING TIMES (at 25°C)

DG126/A, 129/A, 133/A, 134/A, 140/A, 141/A

DG151/A, 152/A, 153/A, 154/A

OFF MODEL

OFF MODEL

ON MODEL

ON MODEL

TYPICAL CHARACTERISTICS (per channel)

DG126/A, 129/A, 133/A, 134/A, 140/A, 141/A

V_{IN} THRESHOLD vs TEMPERATURE

DG151/A, 152/A, 153/A, 154/A

V_{IN} THRESHOLD vs TEMPERATURE

$r_{DS(ON)}$ vs TEMPERATURE (Normalized to 25°C Value)

$r_{DS(ON)}$ vs TEMPERATURE

ALL CIRCUITS

ON SUPPLY CURRENT vs TEMPERATURE

$I_{D(OFF)}$ vs TEMPERATURE

OFF SUPPLY CURRENT vs TEMPERATURE

3

INTERSIL

DG139/A, DG142/A — DG146/A, DG161/A — DG164/A
Drivers with Differentially Driven N.O. and N.C. FET Switches

FEATURES

- Each channel complete-interfaces with most integrated logic
- Low OFF power dissipation, 1 mW
- Switches analog signals up to 20 volts peak-to-peak
- Low $r_{DS(ON)}$, 10 ohms max on DG145/A and DG146/A
- Switching times improved 100%—"A" circuits, 125°C guarantee

GENERAL DESCRIPTION

Each package contains a monolithic driver with differential input and 2 or 4 discrete FET switches. The driver may be treated as a special purpose differential amplifier which controls the conduction state of the FET switches. The differential output of the driver sets the switches in opposition, one pair open and the other pair closed. All switches may be opened by applying a positive control signal to the V_R terminal.

ABSOLUTE MAXIMUM RATINGS

$V_1 - V_2$	36V	$V_1 - V_R$	17V
$V_S - V_2$	30V	$V_1 - V_{IN1}$ or V_{IN2}	14V
$V_1 - V_S$	30V	$V_{IN1} - V_{IN2}$	±6V
$V_S - V_D$	±22V	$V_{IN1} - V_R$	±6V
$V_R - V_2$	21V	$V_{IN2} - V_R$	±6V

Power Dissipation (Note) . . . . . 750 mW
Current (any terminal) . . . . . 30 mA
Storage Temperature . . . . . -65 to +150°C
Operating Temperature . . . . . -55 to +125°C
Lead Temperature (soldering, 10 sec) . . . . . 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10 mW/°C.

3

SPDT

DG143/A($r_{DS(ON)}$ = 80Ω)
DG144/A($r_{DS(ON)}$ = 30Ω)
DG146/A($r_{DS(ON)}$ = 10Ω)
DG161/A($r_{DS(ON)}$ = 15Ω)
DG162/A($r_{DS(ON)}$ = 50Ω)

DPDT

DG139/A($r_{DS(ON)}$ = 30Ω)
DG142/A($r_{DS(ON)}$ = 80Ω)
DG145/A($r_{DS(ON)}$ = 10Ω)
DG163/A($r_{DS(ON)}$ = 15Ω)
DG164/A($r_{DS(ON)}$ = 50Ω)

ORDERING INFORMATION

PACKAGE DIMENSIONS

Flat Package

FD Package

Ceramic Dual-In-Line Package

PRODUCT CONDITIONING

The following processes are performed 100% in accordance with MIL-STD-883.

Precap Visual—Meth. 2010, Cond. B
Stabilization Bake—Meth. 1008
Temp. Cycle—Meth. 1010
Centrifuge—Meth. 2001, Cond. D
Hermeticity—Meth. 1014, Cond. A, C
(Leak Rate $< 5 \times 10^{-8}$ atm cc/s)

ELECTRICAL CHARACTERISTICS PER CHANNEL

Applied voltages for all tests: DG139/A, DG142/A, DG143/A, DG144/A, DG145/A, DG146/A (V_1 = 12V, V_2 = −18V, V_R = 0, V_{IN2} = 2.5V) and DG161/A, DG162/A, DG163/A, DG164/A (V_1 = 15V, V_2 = −15V, V_R = 0, V_{IN2} = 2.5V). Input test condition that guarantees FET switch ON or OFF as specified is used for output specifications.

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT -55°	25°	125°	UNITS	TEST CONDITIONS
INPUT	$V_{IN(ON)}$	Input Voltage—On	All Circuits	2.9 min	2.5 min	2.0 min	Volts	At Pin 9 and 13 See Figure 1 and 2, Pg. 4
	$V_{IN(OFF)}$	Input Voltage—Off		1.4	1.0	0.6	Volts	At Pin 9 and 13 See Figure 1 and 2, Pg. 4
	$\lvert V_9 - V_{13}\rvert$	Differential Voltage		0.5 min	0.5 min	0.5 min	Volts	See Note 1, Pg. 4
	$I_{IN1(ON)}$	Input Current		120	60	60	μA	V_{IN1} = 3.0V
	$I_{IN2(ON)}$			120	60	60	μA	V_{IN2} = 2.0V
	$I_{IN1(OFF)}$	Input Leakage Current		0.1	0.1	2	μA	V_{IN1} = 2.0V
	$I_{IN2(OFF)}$			0.1	0.1	2	μA	V_{IN2} = 3.0V
SWITCH OUTPUT	$r_{DS(ON)}$	Drain-Source On Resistance	DG142/A DG143/A	80	80	150	Ω	V_D = 10V, I_S = −1mA
			DG139/A DG144/A	30	30	60	Ω	
			DG145/A DG146/A	10	10	20	Ω	V_D = 10V, I_S = −1mA
			DG161A DG163/A	15	15	30	Ω	V_D = 7.5V, I_S = 1 mA
			DG162/A DG164/A	50	50	100	Ω	
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG139/A DG142/A DG143/A DG144/A		2	100	nA	$V_D = V_S$ = −10V
	$I_{S(OFF)}$	Source Leakage Current			1	100	nA	V_S = 10V, V_D = −10V
	$I_{D(OFF)}$	Drain Leakage Current			1	100	nA	V_D = 10V, V_S = −10V
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG145/A DG146/A		2	100	nA	$V_D = V_S$ = −10V
	$I_{S(OFF)}$	Source Leakage Current			10	1000	nA	V_S = 10V, V_D = −10V
	$I_{D(OFF)}$	Drain Leakage Current			10	1000	nA	V_D = 10V, V_S = −10V
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG161/A DG163/A		2	500	nA	$V_D = V_S$ = −7.5V
	$I_{S(OFF)}$	Source Leakage Current			10	1000	nA	V_S = 7.5V, V_D = −7.5V
	$I_{D(OFF)}$	Drain Leakage Current			10	1000	nA	V_D = 7.5V, V_S = −7.5V
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG162/A DG164/A		2	500	nA	$V_D = V_S$ = −7.5V
	$I_{S(OFF)}$	Source Leakage Current			2	200	nA	V_S = 7.5V, V_D = −7.5V
	$I_{D(OFF)}$	Drain Leakage Current			2	200	nA	V_D = 7.5V, V_S = −7.5V
POWER SUPPLY	$I_{1(ON)}$	Positive Power Supply Drain Current	All Circuits		4.0		mA	V_{IN1} = 3V or V_{IN1} = 2V
	$I_{2(ON)}$	Negative Power Supply Drain Current			−2.0		mA	
	$I_{R(ON)}$	Reference Power Supply Drain Current			−2.0		mA	
	$I_{1(OFF)}$	Positive Power Supply Leakage Current			25		μA	$V_{IN1} = V_{IN2}$ = 0.8V
	$I_{2(OFF)}$	Negative Power Supply Leakage Current			−25		μA	
	$I_{R(OFF)}$	Reference Power Supply Leakage Current			−25		μA	

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

3

ELECTRICAL CHARACTERISTICS PER CHANNEL (cont.)

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT -55°C	25°	125°	UNITS	TEST CONDITIONS
SWITCHING	t_{ON}	Turn-On Time	DG139, DG142 DG143, DG144 DG162, DG164		0.8		μs	See Below
			DG139A, DG142A DG143A, DG144A DG162A, DG164A		0.4	0.7	μs	
	t_{OFF}	Turn-Off Time	DG139, DG142 DG143, DG144 DG162, DG164		1.6		μs	See Below
			DG139A, DG142A DG143A, DG144A DG162A, DG164A		0.8	1.2	μs	
	t_{ON}	Turn-On Time	DG145, DG146 DG161, DG163		1.0		μs	See Below
			DG145A, DG146A DG161A, DG163A		0.5	0.8	μs	
	t_{OFF}	Turn-Off Time	DG145, DG146 DG161, DG163		2.5		μs	See Below
			DG145A, DG146A DG161A, DG163A		1.25	1.8	μs	
POWER	P_{ON}	ON Driver Power	All Circuits		175		mW	Both Inputs V_{IN} = 2.5V
	P_{OFF}	OFF Driver Power			1		mW	Both Inputs V_{IN} = 1.0V

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

SWITCHING TIMES (25°C)

DG139/A, 142/A, 143/A, 144/A, 145/A, 146/A

DG161/A, 162/A, 163/A, 164/A

OFF MODEL

OFF MODEL

ON MODEL

ON MODEL

FIGURE 1

FIGURE 2

NOTE1: An example of Absolute Minimum Differential Voltage, $|V_9 - V_{13}|$, is when V_9 = 3V and V_{13} = 2.5V, the V_9 side of the switch is ON and the V_{13} side of the switch is OFF at 25°C. Conversely, when V_9 = 2V and V_{13} = 2.5V, the V_9 side of the switch is OFF and the V_{13} side of the switch is ON at 25°C.

TYPICAL CHARACTERISTICS (per channel)

DG139/A, 142/A, 144/A, 145/A, 146/A

V_{IN1} THRESHOLD vs TEMPERATURE

$r_{DS(ON)}$ vs TEMPERATURE

$I_{D(OFF)}$ vs TEMPERATURE

DG161/A, 162/A, 163/A, 164/A

V_{IN1} THRESHOLD vs TEMPERATURE

$R_{DS(ON)}$ vs TEMPERATURE

$I_{S(OFF)}$ vs TEMPERATURE

INTERSIL

DG180 — DG191
High-Speed Driver with Junction FET Switches

FEATURES

- Constant ON-resistance: 75Ω max. for ±10V signals, 10Ω max. for ±7.5 signals.
- ±15V power supplies
- < 2nA leakage from signal channel in both ON and OFF states
- TTL, DTL, RTL direct drive compatibility
- t_{on}, t_{off} < 150ns, break-before-make action
- Cross-talk and open switch isolation, > 50dB at 10 MHz (75Ω load)

FUNCTIONAL DESCRIPTION

PART NUMBER	TYPE	R_{ON} (MAX)
DG 180	Dual SPST	10
DG 181	Dual SPST	30
DG 182	Dual SPST	75
DG 183	Dual DPST	10
DG 184	Dual DPST	30
DG 185	Dual DPST	75
DG 186	SPDT	10
DG 187	SPDT	30
DG 188	SPDT	75
DG 189	Dual SPDT	10
DG 190	Dual SPDT	30
DG 191	Dual SPDT	75

GENERAL DESCRIPTION

The DG180 thru DG191 series of analog gates consists of 2 or 4 N-channel junction-type field-effect transistors (J-FET) designed to function as electronic switches. Level-shifting drivers enable low-level inputs (0.8 to 2V) to control the ON-OFF state of each switch. The driver is designed to provide a turn-off speed which is faster than turn-on speed, so that break-before-make action is achieved when switching from one channel to another. In the ON state each switch conducts current equally well in either direction. In the OFF condition the switches will block voltages up to 20V peak-to-peak. Switch-OFF input-output feedthrough is > 50dB at 10MHz, because of the low output impedance of the FET-gate driving circuit.

ANALOG GATE PRODUCT CONDITIONING

The following processes are performed 100% in accordance with MIL-STD-883.

Precap Visual – Method 2010, Condition B.
Stabilization Bake – Method 1008.
Temperature Cycle – Method 1010.
Centrifuge – Method 2001, Condition E.
Hermeticity – Method 1014, Condition A,C.
(Leak Rate < 5 x 10^{-7} atm cc/s)

SCHEMATIC DIAGRAM (Typical Channel)

ONE AND TWO CHANNEL SPDT AND SPST CIRCUIT CONFIGURATION

DG186/187/188 SHOWN

TWO CHANNEL DPST CIRCUIT CONFIGURATION

DG183/184/185 SHOWN

MAXIMUM RATINGS

$V_{CC}-V_{EE}$	36V	V_L-V_{IN}	8V
$V_{CC}-V_D$	33V	V_L-V_R	8V
V_D-V_{EE}	33V	$V_{IN}-V_R$	8V
V_D-V_S	±22V	V_R-V_{EE}	27V
V_L-V_{EE}	36V	V_R-V_{IN}	2V

Current (Any Terminal except S or D) See Note 3 30mA

Current (S or D) See Note 3 200 mA

Storage Temperature −65°C to +150°C

Operating Temperature −55°C to +125°C

Power Dissipation* 450 (TW), 750 (FLAT), 825 (DIP) mW

*Device mounted with all leads welded or soldered to PC board. Derate 6mW/°C (TW); 10mW/°C (FLAT); 11mW/°C (DIP) above 75°C.

Lead Temperature (Soldering, 10 sec) 300°C

MAXIMUM ELECTRICAL CHARACTERISTICS (V_{CC} = +15V, V_{EE} = -15V, V_L = +5V, V_R = 0, Unless Otherwise Noted)

	PARAMETER	DEVICE	A SERIES -55°C	A SERIES +25°C	A SERIES +125°C	B SERIES -20°C	B SERIES +25°C	B SERIES +85°C	UNITS	TEST CONDITIONS (Note 1)
SWITCH	I_S (off)	DG181, 182, 184, 185 187, 188, 190, 191 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	V_S = 10V, V_D = -10V, V_{CC} = 10V V_{EE} = -20V, V_{IN} = "off"
		DG181, 184, 187, 190 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	V_S = 7.5V, V_D = -7.5V V_{IN} = "off"
		DG182, 185, 188, 191		1	100		5	100	nA	V_S = 10V, V_D = −10V V_{IN} = "off"
	I_D (off)	DG181, 182, 184, 185 187, 188, 190, 191 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	V_S = 10V, V_D = -10V, V_{CC} = 10V V_{EE} = -20V, V_{IN} = "off"
		DG181, 184, 187, 190 (DG180, 183, 186, 189)		1 (10)	100 (1000)		5 (15)	100 (300)	nA	V_S = 7.5V, V_D = -7.5V V_{IN} = "off"
		DG182, 185, 188, 191		1	100		5	100	nA	V_S = 10V, V_D = -10V V_{IN} = "off"
	I_D (on) + I_S (on)	DG180, 181, 183, 184, 186, 187, 189, 190		-2	-200		-10	-200	nA	V_D = V_S = -7.5V, V_{IN} = "on"
		DG182, 183, 188, 191		-2	-200		-10	-200	nA	V_D = V_S = -10V, V_{IN} = "on"
IN	I_{INL}	ALL	-250	-250	-250	-250	-250	-250	μA	V_{IN} = 0V
	I_{INH}	ALL		10	20		10	20	μA	V_{IN} = 5V
DYNAMIC	t_{on}	10Ω Switches		300			350		ns	See switching time test circuit
		30Ω Switches		150			180			
		75Ω Switches		250			300			
	t_{off}	10Ω Switches		250			300			
		30Ω and 75Ω Switches		130			150			
	C_S (off)	DG181, 182, 184, 185, 187, 188, 190, 191 (DG180, 183, 186, 189)	9 typical (21 typical)						pF	V_S = -5V, I_D = 0, f = 1MHz
	C_D (off)		6 typical (17 typical)							V_D = +5V, I_S = 0, f = 1MHz
	$C_{D(on)}$ + $C_{S(on)}$		14 typical (17 typical)							V_D = V_S = 0, f = 1MHz
	Off Isolation		Typically > 50dB at 10MHz (See Note 2)							R_L = 75Ω, C_L = 3pF
SUPPLY	I_{CC}	DG180, 181, 182, 189 190, 191		1.5			1.5		mA	V_{IN} = 5V
		DG183, 184, 185		0.1			0.1			
		DG186, 187, 188		0.8			0.8			
	I_{EE}	DG180, 181, 182, 189 190, 191		-5.0			-5.0			
		DG183, 184, 185		-4.0			-4.0			
		DG186, 187, 188		-3.0			-3.0			
	I_L	DG180, 181, 182, 183 184, 185, 189, 190, 191		4.5			4.5			
		DG186, 187, 188		3.2			3.2			
	I_R	ALL		-2.0			-2.0			
	I_{CC}	DG180, 181, 182, 189, 190, 191		1.5			1.5			V_{IN} = 0V
		DG183, 184, 185		3.0			3.0			
		DG186, 187, 188		0.8			0.8			
	I_{EE}	DG180, 181, 182, 189, 190, 191		-5.0			-5.0			
		DG183, 184, 185		-5.5			-5.5			
		DG186, 187, 188		-3.0			-3.0			
	I_L	DG180, 181, 182, 183 184, 185, 189, 190, 191		4.5			4.5			
		DG186, 187, 188		3.2			3.2			
	I_R	ALL		-2.0			-2.0			

Note 1: See Switching State Diagrams for V_{IN} "ON" and V_{IN} "OFF" Test Conditons.

Note 2: Off Isolation typically >55dB at 1MHz for DG 180, 183, 186, 189.

Note 3: Saturation Drain Current for DG180, 183, 186, 189 only, typically 300mA (2msec Pulse Duration.) Maximum Current on all other devices (any terminal) 30mA.

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ELECTRICAL CHARACTERISTICS (CONT'D)
MAXIMUM ON RESISTANCES ($R_{DS(ON)}$ MAX)

DEVICE NUMBER	A SERIES			B SERIES			UNITS	CONDITIONS (Note 1) V_{CC} = 15V, V_{EE} = -15V, V_L = 5V, V_R = 0V	
	-55°C	+25°C	+125°C	-20°C	+25°C	+85°C			
DG 180	10	10	20	15	15	25	Ω	V_D = -7.5V	
DG 181	30	30	60	50	50	75	Ω	V_D = -7.5V	
DG 182	75	75	100	100	100	150	Ω	V_D = -10V	
DG 183	10	10	20	15	15	25	Ω	V_D = -7.5V	
DG 184	30	30	60	50	50	75	Ω	V_D = -7.5V	
DG 185	75	75	150	100	100	150	Ω	V_D = -10V	I_S = -10 mA
DG 186	10	10	20	15	15	25	Ω	V_D = -7.5V	
DG 187	30	30	60	50	50	75	Ω	V_D = -7.5V	V_{IN} = "ON"
DG 188	75	75	150	100	100	150	Ω	V_D = -10V	
DG 189	10	10	20	15	15	25	Ω	V_D = -7.5V	
DG 190	30	30	60	50	50	50	Ω	V_D = -7.5V	
DG 191	75	75	150	100	100	150	Ω	V_D = -10V	

APPLICATION HINT (for design only): Normally the minimum signal handling capability of the DG180 through DG191 family is 20V peak-to-peak for the 75Ω switches and 15V peak-to-peak for the 10Ω and 30Ω switches (refer I_D and I_S tests above). For other Analog Signals, the following guidelines can be used: proper switch turn-off requires that $V_{EE} \leq V_{ANALOG}$ (-peak) -Vp ≤ 7.5V for the 10Ω and 30Ω switches and Vp ≤ 5.0V for 75Ω switches, i.e., A -10V minimum (-peak) analog signal and a 75Ω switch (Vp ≤ 5V), requires that $V_{EE} \leq$ -10V -5V = -15V.

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or – as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

LOGIC INPUT FOR "OFF" TO "ON" CONDITION (DG180/181/182 SHOWN)

SWITCHING STATE DIAGRAMS

DUAL SPST
DG180/181/182

TEST CONDITIONS

DG180/181/182	
V_{IN} "ON" = 0.8V	All Channels
V_{IN} "OFF" = 2.0V	All Channels

SWITCH STATES ARE FOR LOGIC "1" INPUT = 2.0V

Metal Can Package

TOP VIEW

ORDER NUMBERS:
DG180AA OR DG180BA
DG181AA OR DG181BA
DG182AA OR DG182BA

Flat Package

TOP VIEW

ORDER NUMBERS:
DG180AL OR DG180BL
DG181AL OR DG181BL
DG182AL OR DG182BL

Dual-In-Line Package

TOP VIEW

ORDER NUMBERS:
DG180AP OR DG181BP
DG181AP OR DG181BP
DG182AP OR DG182BP

DUAL DPST
DG183/184/185

TEST CONDITIONS

DG183/184/185	
V_{IN} "ON" = 2.0V	All Channels
V_{IN} "OFF" = 0.8V	All Channels

SWITCH STATES ARE FOR LOGIC "0" INPUT = 0.8V

Flat Package

TOP VIEW

ORDER NUMBERS:
DG183AL OR DG183BL
DG184AL OR DG184BL
DG185AL OR DG185BL

Dual-In-Line Package

TOP VIEW

ORDER NUMBERS:
DL183AP OR DG183BP
DG184AP OR DG184BP
DG185AP OR DG185BP

INTERSIL

SPDT
DG186/187/188

TEST CONDITIONS

DG186/187/188	
V_{IN} "ON" = 2.0V	Channel 1
V_{IN} "ON" = 0.8V	Channel 2
V_{IN} "OFF" = 2.0V	Channel 2
V_{IN} "OFF" - 0.8V	Channel 1

SWITCH STATES ARE
FOR LOGIC "1" INPUT = 2.0V

Metal Can Package

ORDER NUMBERS:
DG186AA OR DG186BA
DG187AA OR DG187BA
DG188AA OR DG188BA

Flat Package

ORDER NUMBERS:
DG186AL OR DG186BL
DG187AL OR DG187BL
DG188AL OR DG188BL

Dual-In-Line Package

ORDER NUMBERS:
DG186AP OR DG186BP
DG187AP OR DG187BP
DG188AP OR DG188BP

DUAL SPDT
DG189/190/191

TEST CONDITIONS

DG189/190/191	
V_{IN} "ON" = 2.0V	Channels 1 & 2
V_{IN} "ON" = 0.8V	Channels 3 & 4
V_{IN} "OFF" = 2.0V	Channels 3 & 4
V_{IN} "OFF" = 0.8V	Channels 1 & 2

SWITCH STATES ARE
FOR LOGIC "1" INPUT = 2.0V

Flat Package

ORDER NUMBERS:
DG189AL OR DG189BL
DG190AL OR DG190BL
DG191AL OR DG191BL

Dual-In-Line Package

ORDER NUMBERS:
DG189AP OR DG189BP
DG190AP OR DG190BP
DG191AP OR DG191BP

PACKAGE DIMENSIONS

16 PIN CERAMIC PACKAGE

14 PIN CERAMIC PACKAGE

FLAT PACKAGE

TO-100 PACKAGE

NOTE: ALL DIMENSIONS IN INCHES.

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INTERSIL

DG426/A, DG429/A, DG433/A, DG434/A, DG440/A, DG441/A, DG451/A, DG452/A, DG453/A, DG454/A

2-Channel Drivers with SPST and DPST FET Switches

FEATURES

- Each channel complete–interfaces with most integrated logic
- Low OFF power dissipation, – 1mW
- Switches analog signals up to 16 volts peak-to-peak
- Low $r_{DS(ON)}$, 15 ohms max on DG440/A and DG441/A
- Switching times improved 100%–"A" versions

GENERAL DESCRIPTION

These switching circuits contain two channels in one package, each channel consisting of a driver circuit controlling a SPST or DPST junction FET switch. The driver interfaces DTL, TTL or RTL logic signals for multiplexing, commutating, and D/A converter applications, which permits logic design directly with the switch function. Logic "1" at the input turns the FET switch ON, and logic "0" turns it OFF.

ABSOLUTE MAXIMUM RATINGS

Analog Signal Voltage ($V_A - V_2$ or $V_1 - V_A$) 28V
Total Supply Voltage ($V_1 - V_2$) 32V
Pos. Supply Voltage to Ref. Voltage ($V_1 - V_R$) . . . 18V
Ref. Voltage to Neg. Supply Voltage ($V_R - V_2$) . . . 21V
Power Dissipation (Note) . . . . . 750 mW
Current (any terminal) . . . . . 30 mA
Storage Temperature . . . . . –65 to +150°C
Operating Temperature . . . . . –65 to +150°C
Lead Temperature (soldering, 10 sec.) . . . . . 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C.

DUAL SPST

DG433/A($r_{DS(ON)}$ = 35Ω)
DG434/A($r_{DS(ON)}$ = 80Ω)
DG441/A($r_{DS(ON)}$ = 15Ω)
DG451/A($r_{DS(ON)}$ = 20Ω)
DG452/A($r_{DS(ON)}$ = 100Ω)

DUAL DPST

DG426/A($r_{DS(ON)}$ = 80Ω)
DG429/A($r_{DS(ON)}$ = 35Ω)
DG440/A($r_{DS(ON)}$ = 15Ω)
DG453/A($r_{DS(ON)}$ = 20Ω)
DG454/A($r_{DS(ON)}$ = 100Ω)

ORDERING INFORMATION

DG 4 26A DD

- DD — Package (See Outline Drawings)
- 26A — Device Chip Type
- 4 — Commercial Temperature Range (0°C to 70°C)
- DG — Analog Gate

PACKAGE DIMENSIONS

Flat Package

FD Package

Ceramic Dual-In-Line Package

DD Package

ELECTRICAL CHARACTERISTICS PER CHANNEL

Applied voltages for all tests; DG426/A, DG429/A, DG433/A, DG434/A, DG440/A, DG441/A, (V_1 = +12V, V_2 = −18V, V_R = 0) and DG451/A, DG452/A, DG453/A, DG454/A (V_1 = +15V, V_2 = −15V, V_R = 0). Input test condition which guarantees FET switch ON and OFF as specified is used for output and power supply specifications.

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT 0°	25°	70°	UNITS	TEST CONDITIONS
INPUT	$V_{IN(ON)}$	Input Voltage–On	All Circuits	2.9 min	2.5 min	2.0 min	Volts	V_2 = −12V
	$V_{IN(OFF)}$	Input Voltage–Off		1.4	1.0	0.8	Volts	V_2 = −12V
	$I_{IN(ON)}$	Input Current		150	100	100	μA	V_{IN} = 2.5V
	$I_{IN(OFF)}$	Input Leakage Current		4	4	10	μA	V_{IN} = 0.8V
SWITCH OUTPUT	$r_{DS(ON)}$	Drain-Source On Resistance	DG426/A DG434/A	80	80	130	Ω	V_D = 8V, I_S = 1 mA
			DG429/A DG433/A	35	35	50	Ω	
			DG440/A DG441/A	15	15	25	Ω	
			DG451/A DG453/A	20	20	30	Ω	V_D = 5.5V, I_S = 1 mA
			DG452/A DG454/A	100	100	140	Ω	
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG426/A DG429/A DG433/A DG434/A		5	160	nA	$V_D = V_S$ = −8V
	$I_{S(OFF)}$	Source Leakage Current			5	160	nA	V_S = 8V, V_D = −8V
	$I_{D(OFF)}$	Drain Leakage Current			5	160	nA	V_D = 8V, V_S = −8V
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG440/A DG441/A		5	160	nA	$V_D = V_S$ = −8V
	$I_{S(OFF)}$	Source Leakage Current			15	500	nA	V_S = 8V, V_D = −8V
	$I_{D(OFF)}$	Drain Leakage Current			15	500	nA	V_D = 8V, V_S = −8V
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG451/A DG453/A		5	100	nA	$V_D = V_S$ = −5.5V
	$I_{S(OFF)}$	Source Leakage Current			15	300	nA	V_S = 5.5V, V_D = −5.5V
	$I_{D(OFF)}$	Drain Leakage Current			15	300	nA	V_D = 5.5V, V_S = −5.5V
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG452/A DG454/A		5	100	nA	$V_D = V_S$ = −5.5V
	$I_{S(OFF)}$	Source Leakage Current			5	100	nA	V_S = 5.5V, V_D = −5.5V
	$I_{D(OFF)}$	Drain Leakage Current			5	100	nA	V_D = 5.5V, V_S = −5.5V
POWER SUPPLY	$I_{1(ON)}$	Positive Power Supply Drain Current	All Circuits		3.5		mA	One Driver ON, V_{IN} = 2.5V
	$I_{2(ON)}$	Negative Power Supply Drain Current			−2.0		mA	
	$I_{R(ON)}$	Reference Power Supply Drain Current			−1.5		mA	
	$I_{1(OFF)}$	Positive Power Supply Leakage Current			25		μA	Both Drivers OFF, V_{IN} = 0.8V
	$I_{2(OFF)}$	Negative Power Supply Leakage Current			−25		μA	
	$I_{R(OFF)}$	Reference Power Supply Leakage Current			−25		μA	

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

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ELECTRICAL CHARACTERISTICS PER CHANNEL (cont.)

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT 0°	25°	70°	UNITS	TEST CONDITIONS
SWITCHING	t_{ON}	Turn-On Time	DG426, DG429 DG433, DG434 DG452, DG454		1.0		µs	See Below
			DG426A, DG429A DG433A, DG434A DG452A, DG454A		0.5	0.7	µs	
	t_{OFF}	Turn-Off Time	DG426, DG429 DG433, DG434 DG452, DG454		2.0		µs	See Below
			DG426A, DG429A DG433A, DG434A DG452A, DG454A		1.0	1.3	µs	
	t_{ON}	Turn-On Time	DG440, DG441 DG451, DG453		1.5		µs	See Below
			DG440A, DG441A DG451A, DG453A		.75	1.3	µs	
	t_{OFF}	Turn-Off Time	DG440, DG441 DG451, DG453		2.5		µs	See Below
			DG440A, DG441A DG451A, DG453A		1.25	1.8	µs	
POWER	P_{ON}	ON Drive Power	All Circuits		175		mW	Both Inputs V_{IN} = 2.5V
	P_{OFF}	OFF Driver Power			1		mW	Both Inputs V_{IN} = 1.0V

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

SWITCHING TIMES (at 25°C)

DG426/A, 429/A, 433/A, 434/A, 440/A, 441/A

DG451/A, 452/A, 453/A, 454/A

OFF MODEL

OFF MODEL

ON MODEL

ON MODEL

TYPICAL CHARACTERISTICS (per channel)

DG426/A, 429/A, 433/A, 434/A, 440/A, 441/A

V_{IN} THRESHOLD vs TEMPERATURE

DG451/A, 452/A, 453/A, 454/A

V_{IN} THRESHOLD vs TEMPERATURE

$r_{DS(ON)}$ vs TEMPERATURE (Normalized to 25°C Value)

$I_{D(OFF)}$ vs TEMPERATURE

ALL CIRCUITS

ON SUPPLY CURRENT vs TEMPERATURE

$r_{DS(ON)}$ vs TEMPERATURE

OFF SUPPLY CURRENT vs TEMPERATURE

3

INTERSIL

DG439/A, DG442/A — DG446/A, DG461/A — DG464/A
Drivers with Differentially Driven N.O. and N.C. FET Switches

FEATURES

- Each channel complete—interfaces with most integrated logic
- Low OFF power dissipation,—1mW
- Switches analog signals up to 16 volts peak-to-peak
- Low $r_{DS(ON)}$, 15 ohms max on DG445/A and DG446/A
- Switching times improved 100%—"A" circuits

GENERAL DESCRIPTION

Each package contains a monolithic driver with differential input and 2 or 4 discrete FET switches. The driver may be treated as a special purpose differential amplifier which controls the conduction state of the FET switches. The differential output of the driver sets the switches in opposition, one pair open and the other pair closed. All switches may be opened by applying a positive control signal to the V_R terminal.

ABSOLUTE MAXIMUM RATINGS

$V_1 - V_2$	32V	$V_1 - V_R$	16V
$V_S - V_2$	28V	$V_1 - V_{IN1}$ or V_{IN2}	14V
$V_1 - V_S$	28V	$V_{IN1} - V_{IN2}$	±5V
$V_S - V_D$	±21V	$V_{IN1} - V_R$	±5V
$V_R - V_2$	20V	$V_{IN2} - V_R$	±5V

Power Dissipation (Note) . . . . . 750 mW
Current (any terminal) . . . . . 30 mA
Operating Temperature . . . . . -55 to +125°C
Lead Temperature (soldering, 10 sec) . . . . . 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10 mW/°C.

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SPDT

DG443/A($r_{DS(ON)}$ = 80Ω)
DG444/A($r_{DS(ON)}$ = 35Ω)
DG446/A($r_{DS(ON)}$ = 15Ω)
DG461/A($r_{DS(ON)}$ = 20Ω)
DG462/A($r_{DS(ON)}$ = 100Ω)

DPDT

DG439/A($r_{DS(ON)}$ = 35Ω)
DG442/A($r_{DS(ON)}$ = 80Ω)
DG445/A($r_{DS(ON)}$ = 15Ω)
DG463/A($r_{DS(ON)}$ = 20Ω)
DG464/A($r_{DS(ON)}$ = 100Ω)

ORDERING INFORMATION

DG 4 39A DD

- DD — Package (See Outline Drawings)
- 39A — Device Chip Type
- 4 — Commercial Temperature Range (0°C to 70°C)
- DG — Analog Gate

PACKAGE DIMENSIONS

Flat Package

FD Package

Ceramic Dual-In-Line Package

DD Package

PRODUCT CONDITIONING

The following processes are performed 100% in accordance with MIL-STD-883.

Precap Visual—Meth. 2010, Cond. B
Stabilization Bake—Meth. 1008
Temp. Cycle—Meth. 1010
Centrifuge—Meth. 2001, Cond. D
Hermeticity—Meth. 1014, Cond. A, C
(Leak Rate $< 5 \times 10^{-8}$ atm cc/s)

ELECTRICAL CHARACTERISTICS PER CHANNEL

Applied voltages for all tests: DG439/A, DG442/A, DG443/A, DG444/A, DG445/A, DG446/A, (V_1 = 12V, V_2 = -18V, V_R = 0, V_{IN2} = 2.5V) and DG461A, DG462/A, DG463/A, DG464/A (V_1 = 15V, V_2 = -15V, V_R = 0, V_{IN2} = 2.5V). Input test condition that guarantees FET switch ON or OFF as specified is used for output specifications.

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT -55°	25°	125°	UNITS	TEST CONDITIONS
INPUT	$V_{IN(ON)}$	Input Voltage—On	All Circuits	2.9 min	2.5 min	2.0 min	Volts	At Pin 9 and 13 See Figure 1 and 2, Pg. 4
	$V_{IN(OFF)}$	Input Voltage—Off		1.4	1.0	0.8	Volts	At Pin 9 and 13 See Figure 1 and 2, Pg. 4
	$\lvert V_9 - V_{13}\rvert$	Differential Voltage		0.5 min	0.5 min	0.5 min	Volts	See Note 1, Pg. 4
	$I_{IN1(ON)}$	Input Current		150	100	100	μA	V_{IN1} = 3.0V
	$I_{IN2(ON)}$			150	100	100	μA	V_{IN2} = 2.0V
	$I_{IN1(OFF)}$	Input Leakage Current		4	4	10	μA	V_{IN1} = 2.0V
	$I_{IN2(OFF)}$			4	4	10	μA	V_{IN2} = 3.0V
SWITCH OUTPUT	$r_{DS(ON)}$	Drain-Source On Resistance	DG442/A DG443/A	80	80	130	Ω	V_D = 10V, I_S = 1 mA
			DG439/A DG444/A	35	35	50	Ω	
			DG445/A DG446/A	15	15	25	Ω	
			DG461/A DG463/A	20	20	30	Ω	V_D = 7.5V, I_S = 1 mA
			DG462/A DG464/A	100	100	140	Ω	
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG439/A DG442/A DG443/A DG444/A		5	160	nA	$V_D = V_S$ = -8V
	$I_{S(OFF)}$	Source Leakage Current			5	160	nA	V_S = 8V, V_D = -8V
	$I_{D(OFF)}$	Drain Leakage Current			5	160	nA	V_D = 8V, V_S = -8V
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG445/A DG446/A		5	160	nA	$V_D = V_S$ = -8V
	$I_{S(OFF)}$	Source Leakage Current			15	500	nA	V_S = 8V, V_D = -8V
	$I_{D(OFF)}$	Drain Leakage Current			15	500	nA	V_D = 8V, V_S = -8V
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG461/A DG463/A		5	100	nA	$V_D = V_S$ = -5.5V
	$I_{S(OFF)}$	Source Leakage Current			15	300	nA	V_S = 5.5V, V_D = -5.5V
	$I_{D(OFF)}$	Drain Leakage Current			15	300	nA	V_D = 5.5V, V_S = -5.5V
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	DG462/A DG464/A		5	100	nA	$V_D = V_S$ = -5.5V
	$I_{S(OFF)}$	Source Leakage Current			5	100	nA	V_D = 5.5V, V_S = -5.5V
	$I_{D(OFF)}$	Drain Leakage Current			5	100	nA	V_D = 5.5V, V_S = -5.5V
POWER SUPPLY	$I_{1(ON)}$	Positive Power Supply Drain Current	All Circuits		3.5		mA	V_{IN1} = 3V or V_{IN1} = 2V
	$I_{2(ON)}$	Negative Power Supply Drain Current			-2.0		mA	
	$I_{R(ON)}$	Reference Power Supply Drain Current			-1.5		mA	
	$I_{1(OFF)}$	Positive Power Supply Leakage Current			25		μA	$V_{IN1} = V_{IN2}$ = 0.8V
	$I_{2(OFF)}$	Negative Power Supply Leakage Current			-25		μA	
	$I_{R(OFF)}$	Reference Power Supply Leakage Current			-25		μA	

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

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ELECTRICAL CHARACTERISTICS PER CHANNEL (cont.)

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT -55°C	25°	125°	UNITS	TEST CONDITIONS
SWITCHING	t_{ON}	Turn-On Time	DG439, DG442 DG443, DG444 DG462, DG464		1.0		µs	See Below
			DG439A, DG442A DG443A, DG444A DG462A, DG464A		0.5	0.7	µs	
	t_{OFF}	Turn-Off Time	DG439, DG442 DG443, DG444 DG462, DG464		2.0		µs	See Below
			DG439A, DG442A DG443A, DG444A DG462A, DG464A		1.0	1.3	µs	
	t_{ON}	Turn-On Time	DG445, DG446 DG461, DG463		1.5		µs	See Below
			DG445A, DG446A DG461A, DG463A		.75	1.3	µs	
	t_{OFF}	Turn-Off Time	DG445, DG446 DG461, DG463		2.5		µs	See Below
			DG445A, DG446A DG461A, DG463A		1.25	1.8	µs	
POWER	P_{ON}	ON Driver Power	All Circuits		175		mW	Both Inputs V_{IN} = 2.5V
	P_{OFF}	OFF Driver Power			1		mW	Both Inputs V_{IN} = 1.0V

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

SWITCHING TIMES (25°C)

DG439/A, 442/A, 443/A, 444/A, 445/A, 446/A

DG461/A, 462/A, 463/A, 464/A

OFF MODEL

OFF MODEL

ON MODEL

ON MODEL

FIGURE 1

FIGURE 2

NOTE1: An example of Absolute Minimum Differential Voltage, $|V_9 - V_{13}|$, is when V_9 = 3V and V_{13} = 2.5V, the V_9 side of the switch is ON and the V_{13} side of the switch is OFF at 25°C. Conversely, when V_9 = 2V and V_{13} = 2.5V, the V_9 side of the switch is OFF and the V_{13} side of the switch is ON at 25°C.

TYPICAL CHARACTERISTICS (per channel)

DG439/A, 442/A, 443/A, 444/A, 445/A, 446/A

V_{IN1} THRESHOLD vs TEMPERATURE

$r_{DS(ON)}$ vs TEMPERATURE

$I_{D(OFF)}$ vs TEMPERATURE

DG461/A, 462/A, 463/A, 464/A

V_{IN1} THRESHOLD vs TEMPERATURE

$R_{DS(ON)}$ vs TEMPERATURE

$I_{S(OFF)}$ vs TEMPERATURE

INTERSIL

IH181/IH182/IH184/IH185/ IH187/IH188/IH190/IH191 Low-Power, High-Level Analog Gates*

FEATURES

- Switches 20 Vpp Signals
- Quiescent Current Less than 100 μA
- Overvoltage Protection to ±25V
- Break-Before-Make Switching; t_{OFF} 130 ns Max, t_{ON} 250 nsec Max.
- T^2L, HTL, CMOS, PMOS Compatible
- Low r_{DS} (ON) – 30Ω
- Construction includes CMOS high level driver circuitry combined with unique "VARAFET" switches.

GENERAL DESCRIPTION

This family of solid state analog gates is designed using both CMOS technology and a unique new J-FET technology. CMOS processing is used to make a driver or translator chip, which translates the TTL strobing logic into plus and minus 15V. This driver chip draws extremely low quiescent current from the power supplies; thus system power dissipation is reduced to nW typical.

The actual switching element is a unique new Intersil design, called the Varafet. The Varafet is a monolithic combination of a varactor J-FET diode driving a conventional J-FET. Strobing the solid state switch is accomplished by the TTL levels of a "1" being 2.4V or greater; a "0" is 0.8V or lower. The translator input circuitry will draw virtually no source or sinking current (typical pa of input current) from the TTL logic output element, and the effective fanout, if one were to drive only solid state switches, approaches millions.

The family of analog gates is guaranteed to be "break-before-make" switching; The "off" time is faster than the "on" time. Typical turn-off times are 80 ns and typical turn-on times are 200 ns.

3

*** Note:** The INTERSIL IH181/191 series is a low power version of the standard DG181/191 series. They meet or exceed the standard DG181/191 series specifications with the following exceptions:

1.) V_{INH} = 2.4 volts minimum.

2.) Break-before-make switching requires t_{ON} to be 250 nsec maximum.

See also IH5040, IH5140 series.

SCHEMATIC DIAGRAM (Typical Channel)

FUNCTIONAL DESCRIPTION

PART NUMBER	TYPE	R_{ON}
IH 181	Dual SPST	30
IH 182	Dual SPST	75
IH 184	Dual DPST	30
IH 185	Dual DPST	75
IH 187	SPDT	30
IH 188	SPDT	75
IH 190	Dual SPDT	30
IH 191	Dual SPDT	75

CMOS ANALOG GATE PRODUCT CONDITIONING

The following processes are performed 100% in accordance with MIL-STD-883.

Precap Visual – Method 2010, Cond. B.
Stabilization Bake – Method 1008.
Temperature Cycle – Method 1010
Centrifuge – Method 2001, Cond. E.
Hermeticity – Method 1014, Cond. A, C.
(Leak Rate $< 5 \times 10^{-7}$ atm cc/s)

MAXIMUM RATINGS

$V_1 - V_2$	36 V	$V_L - V_{IN}$	8 V
$V_1 - V_D$	33 V	$V_L - V_R$	8 V
$V_D - V_2$	33 V	$V_{IN} - V_R$	8 V
$V_D - V_S$	±22 V	$V_R - V_2$	36 V
$V_L - V_2$	36 V	$V_R - V_{IN}$	2 V

Current (Any Terminal)	30 mA
Storage Temperature	−65°C to 150°C
Operating Temperature	−55°C to 125°C
Power Dissipation*	450 mW
Lead Temperature (soldering, 10 sec.)	300°C

*Device mounted with all leads welded or soldered to PC board. Derate 6 mW/°C above 75°C

ELECTRICAL CHARACTERISTICS – IH 181 THRU IH 191

(V_1 = 15 V, V_2 = −15 V, V_L = 5 V, V_R = 0, Unless Noted)

PARAMETER Note (1)	DEVICE	MAX LIMITS (Note 1) −55°C +25°C +125°C	MAX LIMITS (Note 1) −20°C +25°C +85°C	UNITS	TEST CONDITIONS
SWITCH	ALL	0.1 50	5 100	nA	V_S = 10V, V_D = −10V V_1 = 10V V_2 = −20V V_{IN} = 2.4V
	IH 181 IH 184 IH 187 IH 190	0.1 50	5 100	nA	V_S = 7.5V, V_D = −7.5V V_{IN} = 2.4V
I_S (OFF)	IH 182 IH 185 IH 188 IH 191	0.1 50	5 100	nA	V_S = 10V, V_D = −10V V_{IN} = 2.4V
	ALL	0.1 50	5 100	nA	V_S = 10V V_D = −10V V_1 = 10V V_2 = −20V V_{IN} = 2.4V
	IH 181 IH 184 IH 187 IH 190	0.1 50	5 100	nA	V_S = 7.5V V_D = −7.5V V_{IN} = 2.4V
I_D (OFF)	IH 182 IH 185 IH 188 IH 191	0.1 50	5 100	nA	V_S = 10V V_D = −10V V_{IN} = 2.4V
	IH 181 IH 184 IH 187 IH 190	-0.2 100	-10 -200	nA	$V_D = V_S$ = −7.5V V_{IN} = 0.8V
I_D (ON) + I_S (ON)	IH 182 IH 185 IH 188 IH 191	-0.2 100	-10 -200	nA	$V_D = V_S$ = −10V V_{IN} = 0.8V
IN I_{INL}	ALL	1 1 1	1 1 1	μA	V_{IN} = 0V
I_{INH}	ALL	1 1 1	1 1 1	μA	V_{IN} = 5V
DYNAMIC t_{on}	ALL	250	300	ns	See switching time test circuit Fig. 10
t_{off}	ALL	130	150	ns	
$C_{S(off)}$	ALL	9 typical		pf	V_S = −5V, I_D = 0, f = 1MHZ
C_D (off)		6 typical		pf	V_S = −5V, I_D = 0, f = 1MHZ
$C_{D(on)}$ + C_S (on)		14 typical		pf	$V_D = V_S$ = 0 f = 1MHZ
Off Isolation		Typ > 50 dB at 10 MHZ		pf	R_L = 100Ω, C_L = 3pf
Supply I_{CC}	ALL	100 10 100	100	μA	Both V_{IN} = 0V
I_{EE}		100 10 100	100	μA	
I_L		10	100	μA	
I_R		10	100	μA	
I_{CC}		100 10 100	100	μA	Both V_{IN} = 5 V
I_{EE}		100 10 100	100	μA	
I_L		10	100	μA	
I_R		10	100	μA	

APPLICATION HINT (for design only): The minimum signal handling capability of the IH181 through IH191 family is 20V peak to peak for the 75Ω switches and 15V peak to peak for the 30Ω switches (refer I_D and I_S tests above. Proper switch turn off requires that $V_{ee} \leq V_{ANALOG}$ (−peak) − V_P where $V_P \leq$ 7.5V for 30Ω switches and $V_P \leq$ 5.0V for 75Ω switches i.e., A −10V minimum (−peak) analog signal and a 75Ω switch ($V_P \leq$ 5V), requires that $V_{ee} \leq$ −10V −5V = −15V.

MAXIMUM ON RESISTANCES – $r_{DS(ON)}$ MAX

(V_1 = 15 V, V_2 = −15 V, V_L = 5 V, V_R = 0, I_S = 10 mA, V_{INL} = 0.8 V, V_{INH} = 2.4V)

DEVICE NUMBER	MILITARY TEMPERATURE −55°C	25°C	125°C	INDUSTRIAL TEMPERATURE −20°C	25°C	85°C	UNITS	CONDITIONS
IH 181	30	30	60	50	50	75	Ω	V_D = −7.5V
IH 182	75	75	100	100	100	150	Ω	V_D = −10V
IH 184	30	30	60	50	50	75	Ω	V_D = −7.5 V
IH 185	75	75	150	100	100	150	Ω	V_D = −10V
IH 187	30	30	60	50	50	75	Ω	V_D = −7.5V
IH 188	75	75	150	100	100	150	Ω	V_D = −10V
IH 190	30	30	60	50	50	75	Ω	V_D = −7.5V
IH 191	75	75	150	100	100	150	Ω	V_D = −10V

LOGIC COMPATIBILITY

The IH 181/191 series has been designed to directly interface with the popular TTL, HTL, and CMOS families, but almost any logic family can be used. The fact that the solid state switch input current approaches zero (specification has 1 μA maximum for either high or low input states) means that one is operating along the zero load current, or zero source current line for the TTL output voltage vs. I_{load} or I_{source} current. Thus the maximum output is obtained from the TTL gate. Figures 1 and 2 show the expected (typical) output of a TTL gate vs. load and source currents and plotted as a function of temperature and power supply.

FIGURE 1. CIRCUIT ANALYSIS AND CHARACTERISTICS OF SERIES 54/74

FIGURE 2.

FIGURE 3. FOR INTERFACING WITH TTL LOGIC

FIGURE 4. FOR INTERFACING WITH HTL OPEN COLLECTOR LOGIC

FIGURE 5. FOR USE WITH CMOS LOGIC

Note: When using HTL or CMOS logic, a zener diode should be added between the V_L supply (normally plus 5V) and the V_1 supply (normally plus 15V). This zener is not critical. Any value between 2V and 10V will work fine, and no biasing resistor is needed to establish a current through the zener. In cases where the TTL logic level may go below 2.4V, a pull-up resistor should be added between the TTL output and the plus 5V power supply.

THEORY OF OPERATION

Voltage Translator or Driver Circuit

The translator part of the IH181 family takes the low level strobe input and converts it to a plus and minus 15V swing. These voltage swings are necessary to drive the output Varafets so they can switch the maximum analog input signal. As shown in Figures 6 and 7, this translation is performed without drawing any power supply quiescent current. Typical quiescent current is only the $I_{D(off)}$ leakage of the FET – this is usually less than 1 nA. Whether the input strobe logic is in the "1" state or the "0" state makes no difference; the quiescent current remains leakage of FET in the off condition.

The currents previously discussed are dc currents and the obvious result is low circuit power consumption. For example, with plus and minus 15V power supplies, the specified maximum power consumption is 3 mW. The typical power consumption will be 30 nW. When strobing from a particular duty cycle square wave, ac currents will be drawn and the magnitude of these are dependent upon the duty cycle and the plus repetition rate. Figure 8 shows typical ac current draw as a function of pulse repetition rate.

FIGURE 6. DRIVER STATES WITH T^2L "1" INPUT

FIGURE 7. DRIVER STATES WITH T^2L "0" INPUT

FIGURE 8. POWER SUPPLY QUIESCENT CURRENT VS. LOGIC FREQUENCY RATE

FIGURE 9. OUTPUT VARAFET

THEORY OF OPERATION (CONTINUED)

Output J-FET or Varafet

The output J-FET is the actual solid state switch. The translator circuit is merely a means to interface the low level TTL strobing logic into higher levels to drive the output FET. The varafet is a monolithically constructed combination of a varactor diode in series with the gate of an N-channel J-FET. The driver diode (varactor diode) is needed to prevent forward biasing the output FET during normal switching applications. Figure 9 shows a schematic of the complete varafet.

Notice that the polarity of the driver diode is such that it forms a back-to-back diode combination with the source-to-gate or drain-to-gate junctions of the FET. This makes it impossible to forward bias a source-to-gate junction during switching. The driver diode is a voltage variable capacitor whose C (capacity) vs. V (voltage across diode) plot is much greater than the C vs. V plot for either the source-to-gate or drain-to-gate FET iunctions. In fact, the criteria for proper operation of the varafet is that the integral of the diode's C vs. V plot is at least equal to the sum of the C vs. V plots for the source-to-gate and drain-to-gate FET junctions. The integral of C vs. V is charge Q. C = Q/V and Q = C X V. Thus the varafet is really a charge transfer device.

SWITCHING STATE DIAGRAMS

DUAL SPST
IH181/IH182

SWITCH STATES ARE FOR LOGIC "1" INPUT

Metal Can Package

ORDER NUMBERS:
IH181MTW OR IH181CTW
IH182MTW OR IH182CTW

Flat Package

ORDER NUMBERS:
IH181MFD OR IH181CFD
IH182MFD OR IH182CFD

Dual-In-Line Package

ORDER NUMBERS:
IH181MDD OR IH181CDD
IH182MDD OR IH182CDD

DUAL DPST
IH184/IH185

Flat Package

ORDER NUMBERS:
IH184MFD OR IH184CFD
IH185MFD OR IH185CFD

Dual-In-Line Package

ORDER NUMBERS:
IH184MDE OR IH184CDE
IH185MDE OR IH185CDE

SPDT
IH187/IH188

Metal Can Package

ORDER NUMBERS:
IH187MTW OR IH187CTW
IH188MTW OR IH188CTW

Flat Package

ORDER NUMBERS:
IH187MFD OR IH187CFD
IH188MFD OR IH188CFD

Dual-In-Line Package

ORDER NUMBERS:
IH187MDD OR IH187CDD
IH188MDD OR IH188CDD

DUAL SPDT
IH190/IH191

Flat Package

ORDER NUMBERS:
IH190MFD OR IH190CFD
IH191MFD OR IH191CFD

Dual-In-Line Package

ORDER NUMBERS:
IH190MDE OR IH190CDE
IH191MDE OR IH191CDE

SWITCHING TIME TEST CIRCUIT

Switch output waveform shown for V_S = constant with logic input waveform as shown. Note that V_S may be + or − as per switching time test circuit. V_O is the steady state output with switch on. Feedthrough via gate capacitance may result in spikes at leading and trailing edge of output waveform.

	SWITCH INPUT	
	75Ω SERIES	30Ω SERIES
t_{on}	V_S = +10V	V_S = +7.5V
t_{off}	V_S = −10V	V_S = −7.5V

FIGURE 10

PACKAGE DIMENSIONS

16 PIN CERAMIC PACKAGE

14 PIN CERAMIC PACKAGE

FLAT PACKAGE

TO–100 PACKAGE

NOTE: All dimensions in inches.

IH200
CMOS Analog Gate

FEATURES

- **Switches Greater Than 20Vpp Signals With ±15V Supplies**
- **Quiescent Current Less Than 10μA**
- **Overvoltage Protection to ±25V**
- **Break-Before-Make Switching: t_{OFF} 200 nsec, t_{ON} 400nsec Typical**
- **T²L, DTL, CMOS, PMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **Complete Monolithic Construction**

GENERAL DESCRIPTION

The IH200 solid state analog gate is designed using an improved, high voltage CMOS monolithic technology. This improved CMOS technology provides input overvoltage capability to ±25 volts without damage to the device, and destructive latch-up of solid state analog gates has been eliminated. Early CMOS gates were destroyed when power supplies were removed with an input signal present. The INTERSIL CMOS technology has eliminated this serious systems problem.

Key performance advantages of the IH200 are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 10μA. Also designed into the IH200 is guaranteed Break-Before-Make switching. This is logically accomplished by extending the t_{ON} time (400 nsec TYP.) such that it exceeds t_{OFF} time (200 nsec TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. This eliminates the need for external logic required to avoid channel to channel shorting during switching.

3

FUNCTIONAL DIAGRAM

PIN CONFIGURATIONS

DUAL-IN-LINE PACKAGE

ORDER NUMBERS:
IH200AP
IH200BP

DUAL-IN-LINE PACKAGE

ORDER NUMBERS:
IH200MDE
IH200CDE

FLAT PACKAGE

SWITCH STATES ARE FOR LOGIC "1" INPUT (POSITIVE LOGIC)

ORDER NUMBERS:
IH200AL
IH200BL

METAL CAN PACKAGE

ORDER NUMBERS:
IH200AA
IH200BA

MAXIMUM RATINGS

Current (Any Terminal)	<30 mA
Storage Temperature	−65°C to +150°C
Operating Temperature	−55°C to +125°C
Power Dissipation	450mW
(All Leads Soldered to a P.C. Board)	
Derate 6 mW/°C Above 70°C	
Lead Temperature (Soldering, 10 sec)	300°C

V_1-V_2	<33V
V_1-V_D	<30V
V_D-V_2	<30V
V_D-V_S	<±22V
V_L-V_2	<33V
V_L-V_{IN}	<30V
V_L-V_R	<20V
V_{IN}-V_R	<20V

ELECTRICAL CHARACTERISTICS (@ 25°C, V_1 = +15V, V_2 = −15V, V_L = +5V, V_R = 0.V)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				TEST
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 0.8 V
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 2.4 V
$r_{DS(ON)}$	Drain-Source On Resistance	75	75	100	80	80	100	Ω	I_S = 1mA, V_{ANALOG} = −10 V to ±10 V
$r_{DS(ON)}$	Channel to Channel R_{DS}(ON) Match	25	25	25	30	30	30	Ω	I_S (Each Channel) = 1 mA
V_{ANALOG}	Min. Analog Signal Handling Capability	±11	±11	±11	±10	±10	±10	V	I_S = 10 mA
$I_{D(OFF)}$	Switch OFF Leakage Current	1	1	100	5	5	250	nA	V_{ANALOG} = −10 V to +10 V
$I_{D(ON)}$ +$I_{S(ON)}$	Switch On Leakage Current	2	2	200	10	10	250	nA	V_D = V_S = −10 V to +10 V
t_{ON}	Switch "ON" Time		1.0			1.0		μs	R_L = 1 kΩ, V_{ANALOG} = −10 V to +10 V See Fig. A
t_{OFF}	Switch "OFF" Time		0.5			0.5		μs	R_L = 1 kΩ, V_{ANALOG} = −10 V to +10 V See Fig. A
$Q_{(INJ.)}$	Charge Injection		15			20		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R_L = 100Ω, C_L ≤5pF See Fig. C
I_{V1}	+ Power Supply Quiescent Current	10	10	100	10	10	100	μA	V_1 = +15 V, V_2 = −15 V, V_L = +5V V_L = +5 V, V_R = 0 Switch Duty Cycle < 10%
I_{V2}	−Power Supply Quiescent Current	10	10	100	10	10	100	μA	
I_{VL}	+5 V Supply Quiescent Current	10	10	100	10	10	100	μA	
I_{VR}	Gnd Supply Quiescent Current	10	10	100	10	10	100	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off

3

TEST CIRCUITS

Figure A

Figure B

Figure C

PACKAGE DIMENSIONS

16 PIN CERAMIC PACKAGE (DE)

16 PIN DIP PACKAGE (PE)

3

TO-100 PACKAGE

14 PIN CERDIP (JD)

FLAT PACKAGE (FD)

NOTE: Dimensions in inches (millimeters)

INTERSIL

IH201/IH202
CMOS Analog Gate

FEATURES

- **Switches Greater Than 20Vpp Signals With ±15V Supplies**
- **Quiescent Current Less Than 10μA**
- **Overvoltage Protection to ±25V**
- **Break-Before-Make Switching t_{OFF} 200 nsec, t_{ON} 400nsec Typical**
- **T²L, DTL, CMOS, PMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **IH201 4 Normally Closed Switches**
- **IH202 4 Normally Open Switches**
- **Low Leakage Typical <100pA**

GENERAL DESCRIPTION

The IH201/2 solid state analog gate is designed using an improved, high voltage CMOS technology. This improved CMOS technology provides input overvoltage capability to ±25 volts without damage to the device and the destructive latch-up of solid state analog gates has been eliminated. Early CMOS gates were destroyed when power supplies were removed with an input signal present. The INTERSIL CMOS technology has eliminated this serious systems problem.

Key performance of the IH201 are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 10μA. Also designed into the IH201/2 is guaranteed Break-Before-Make switching. This is logically accomplished by extending the t_{ON} time (400 nsec TYP.) such that it exceeds t_{OFF} time (200nsec TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. This eliminates the need for external logic required to avoid channel to channel shorting during switching.

3

FUNCTIONAL DIAGRAM

PIN CONFIGURATIONS

DUAL-IN-LINE PACKAGE

ORDER NUMBERS:
IH201MDE OR IH201CDE

SWITCH STATES ARE FOR LOGIC "1" INPUT

ORDER NUMBERS:
IH202MDE OR IH202CDE

MAXIMUM RATINGS

Current (Any Terminal)	<30 mA
Storage Temperature	−65° C to +150° C
Operating Temperature	−55° C to +125° C
Power Dissipation	450mW
(All Leads Soldered to a P.C. Board)	
Derate 6 mW/°C Above 70 °C	
Lead Temperature (Soldering, 10 sec)	300 °C

V_I-V_2	<33V
V_I-V_D	<30V
V_D-V_2	<30V
V_D-V_S	<±22V
V_L-V_2	<33V
V_L-V_{IN}	<30V
V_L-V_R	<20V
V_{IN}-V_R	<20V

ELECTRICAL CHARACTERISTICS (@25° C, V_1 = +15V, V_2 = −15V, V_L = +5 V, V_R = 0 V)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				TEST
SYMBOL	CHARACTERISTIC	−55° C	+25° C	+125° C	0	+25° C	+70° C	UNITS	CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 0.8 V (IH201), V_{IN} = 2.4V (IH202)
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 2.4 V (IH201), V_{IN} = 0.8V (IH202)
$r_{DS(ON)}$	Drain-Source On Resistance	100	100	200	150	150	200	Ω	I_S = 1mA, V_{ANALOG} = ±10 V
$r_{DS(ON)}$	Channel to Channel R_{DS}(ON) Match	25	25	25	30	30	30	Ω	I_S (Each Channel) = 1 mA
V_{ANALOG}	Min. Analog Signal Handling Capability	±11	±11	±11	±10	±10	±10	V	I_S = 10 mA
$I_{D(OFF)}$	Switch OFF Leakage Current	1	1	200	2	2	250	nA	V_{ANALOG} = −10 V to +10 V
$I_{D(ON)}$ +$I_{S(ON)}$	Switch On Leakage Current	2	2	200	2	2	250	nA	V_D = V_S = −10 V to +10 V
t_{ON}	Switch "ON" Time		1.0			1.0		μs	R_L = 1 kΩ, V_{ANALOG} = −10 V to +10 V See Fig. A
t_{OFF}	Switch "OFF" Time		0.5			0.5		μs	R_L = 1 kΩ, V_{ANALOG} = −10 V to +10 V See Fig. A
$Q_{(INJ.)}$	Charge Injection		15			20		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R_L = 100Ω, C_L ≤5pF See Fig. C
I_{V1}	+ Power Supply Quiescent Current	20	20	100	30	30	100	μA	V_1 = +15 V, V_2 = −15 V, V_L = +5V V_R = 0 Switch Duty Cycle < 10%
I_{V2}	−Power Supply Quiescent Current	20	20	100	30	30	100	μA	
I_{VL}	+5 V Supply Quiescent Current	20	20	100	30	30	100	μA	
I_{VR}	Gnd Supply Quiescent Current	20	20	100	20	20	100	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off

3

TEST CIRCUITS

Figure A

Figure B

Figure C

PACKAGE DIMENSIONS

16 PIN CERAMIC PACKAGE (DE)

16 PIN DIP PACKAGE

16-PIN FLAT PAK (FE)

NOTE: Dimensions in inches (millimeters)

***Not available in plastic at this time.**

INTERSIL

IH5001/IH5002 1-Channel Driver with SPST FET Switch AND Gate Available

FEATURES

- Gate Lead Available for Nulling Charge Injection Voltage
- Channel Complete—Interfaces With Most Integrated Logic
- Low OFF Power Dissipation, –1 mW
- Low $r_{DS(ON)}$, 30Ω Max on IH5001
- Switches Analog Signals up to 16 Volts Peak-to-Peak

GENERAL DESCRIPTION

These switching circuits contain one channel in one package, the channel consisting of a driver circuit controlling a SPST junction FET switch. The driver interfaces DTL, TTL, or RTL logic signals for multiplexing, commutating, and D/A converter applications, which permits logic design directly with the switch function. Logic "1" at the input turns the FET switch ON, and logic "0" turns it OFF. The gate lead of the FET has been brought out to enable the application of a referral resistor for nulling offset voltage due to charge injection.

ABSOLUTE MAXIMUM RATINGS

Analog Signal Voltage ($V_A - V_2$ or $V_1 - V_A$)	28V
Total Supply Voltage ($V_1 - V_2$)	32V
Pos. Supply Voltage to Ref. Voltage ($V_1 - V_R$)	18V
Ref. Voltage to Neg. Supply Voltage ($V_R - V_1$)	21V
Power Dissipation (Note)	500 mW
Current (Any Terminal)	30 mA
Storage Temperature	–65 to +150°C
Operating Temperature	0 to +70°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C.

SPST

IH5001($r_{DS(ON)}$ = 30Ω)
IH5002($r_{DS(ON)}$ = 50Ω)

PACKAGE OUTLINES

Plastic DIP

PA Package

ORDERING INFORMATION

IH 5 0 01 C PA

- PA — Package (See Outline Drawing)
- C — Commercial Temperature Range (0 to +70°C)
- 01 — Type
- 0 — Gate
- 5 — Analog
- IH — Intersil Hybrid

ELECTRICAL CHARACTERISTICS

Applied voltages for all tests: $V_1 = +12V$, $V_2 = -18V$, $V_R = 0$. Input test condition which guarantees FET switch ON or OFF as specified is used for output and power supply specifications.

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX LIMIT 0°	25°	70°	UNITS	TEST CONDITIONS
INPUT	$V_{IN(ON)}$	**Input Voltage-ON**	Both Circuits	**2.9 min**	**2.5 min**	**2.0 min**	Volts	$V_2 = -12V$
	$V_{IN(OFF)}$	**Input Voltage-OFF**		**1.4**	**1.0**	**0.8**	Volts	$V_2 = -12V$
	$I_{IN(ON)}$	Input Current		150	100	100	μA	$V_{IN} = 2.5V$
	$I_{IN(OFF)}$	Input Leakage Current		4	4	10	μA	$V_{IN} = 0.8V$
SWITCHING OUTPUT	$V_{DS(ON)}$	**Drain-Source ON Resistance**	IH5001	**30**	**30**	**50**	Ω	$V_D = 8V$, $I_S = 1$ mA
			IH5002	**50**	**50**	**85**	Ω	
	$I_{D(ON)}+I_{S(ON)}$	Drive Leakage Current	Both Circuits		5	160	nA	$V_D = V_S = -8V$
	$I_{S(OFF)}$	Source Leakage Current			5	160	nA	$V_S = 8V$, $V_D = -8V$
	$I_{D(OFF)}$	**Drain Leakage Current**			**5**	**160**	nA	$V_D = 8V$, $V_S = -8V$
POWER SUPPLY	$I_{1(ON)}$	Positive Power Supply Drain Current	Both Circuits		3.5		mA	Driver ON, $V_{IN} = 2.5V$
	$I_{2(ON)}$	Negative Power Supply Drain Current			−2.0		mA	
	$I_{R(ON)}$	Reference Power Supply Drain Current			−1.5		mA	
	$I_{1(OFF)}$	Positive Power Supply Leakage Current			25		μA	Driver OFF, $V_{IN} = 0.8V$
	$I_{2(OFF)}$	Negative Power Supply Leakage Current			−25		μA	
	$I_{R(OFF)}$	Reference Power Supply Leakage Current			−25		μA	
SWITCH	t_{ON}	**Turn-On Time**	Both Circuits		**0.5**	**0.7**	μs	See Below
	t_{OFF}	**Turn-Off Time**			**1.0**	**1.3**	μs	
POWER	P_{ON}	ON Driver Power	Both Circuits		175		mW	$V_{IN} = 2.5V$
	P_{OFF}	OFF Driver Power			1		mW	$V_{IN} = 1.0V$
FET	$V_{GS(f)}$	Gate Source Forward Voltage	Both Circuits		1.5		Volts	$I_G = 1.0$ mA, $V_{DS} = 0$

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

SWITCHING TIMES (at 25°C)

OFF MODEL

ON MODEL

3

INTERSIL

IH5003/IH5004 2-Channel Drivers with SPST FET Switches AND Gate Available

FEATURES

- Gate Lead Available for Nulling Charge Injection Voltage
- Each Channel Complete—Interfaces With Most Integrated Logic
- Low OFF Power Dissipation, –1 mW
- Switches Analog Signals up to 20 Volts Peak-to-Peak
- Low $r_{DS(ON)}$, 30Ω Max on IH5003

GENERAL DESCRIPTION

These switching circuits contain two channels in one package, each channel consisting of a driver circuit controlling a SPST junction FET switch. The driver interfaces DTL, TTL, or RTL logic signals for multiplexing, commutating, and D/A converter applications, which permits logic design directly with the switch function. Logic "1" at the input turns the FET switch ON, and logic "0" turns it OFF. The gate lead of the FETs has been brought out to enable the application of a referral resistor for nulling out offset voltage due to charge injection.

ABSOLUTE MAXIMUM RATINGS

Analog Signal Voltage ($V_A - V_2$ or $V_1 - V_A$)	30V
Total Supply Voltage ($V_1 - V_2$)	36V
Pos. Supply Voltage to Ref. Voltage ($V_1 - V_R$)	25V
Ref. Voltage to Neg. Supply Voltage ($V_R - V_2$)	22V
Power Dissipation (Note)	750 mW
Current (Any Terminal)	30 mA
Storage Temperature	-65 to +150°C
Operating Temperature	-55 to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10 mW/°C.

DUAL SPST

IH5003 ($r_{DS(ON)}$ = 30Ω)
IH5004 ($r_{DS(ON)}$ = 50Ω)

PACKAGE OUTLINES

FD Package

DD Package

ORDERING INFORMATION

IH 5 0 03 M FD

- FD — Package (See Outline Drawing)
- M — Military Temperature Range (-55°C to +125°C)
- 03 — Type
- 0 — Gate
- 5 — Analog
- IH — Intersil Hybrid

ELECTRICAL CHARACTERISTICS

Applied Voltages for all tests: V_1 = +12V, V_2 = −18V, V_R = 0. Input test condition which guarantees FET switch ON or OFF as specified is used for output and power supply specifications.

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX LIMIT −55°	25°	125°	UNITS	TEST CONDITIONS
INPUT	$V_{IN(ON)}$	**Input Voltage-ON**	Both Circuits	**2.9 min**	**2.5 min**	**2.0 min**	Volts	V_2 = −12V
	$V_{IN(OFF)}$	**Input Voltage-OFF**		**1.4**	**1.0**	**0.6**	Volts	V_2 = −12V
	$I_{IN(ON)}$	Input Current		120	60	60	μA	V_{IN} = 2.5V
	$I_{IN(OFF)}$	Input Leakage Current		0.1	0.1	2	μA	V_{IN} = 0.8V
SWITCHING OUTPUT	$r_{DS(ON)}$	**Drain-Source ON Resistance**	IH5003	**30**	**30**	**50**	Ω	V_D = 10V, I_S = 1 mA
			IH5004	**50**	**50**	**85**	Ω	
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	Both Circuits		2	100	nA	$V_D = V_S$ = −10V
	$I_{S(OFF)}$	Source Leakage Current			1	100	nA	V_S = 10V, V_D = −10V
	$I_{D(OFF)}$	Drain Leakage Current			1	100	nA	V_D = 10V, V_S = −10V
POWER SUPPLY	$I_{1(ON)}$	Positive Power Supply Drain Current	Both Circuits		3		mA	One Driver ON, V_{IN} = 2.5V
	$I_{2(ON)}$	Negative Power Supply Drain Current			−1.8		mA	
	$I_{R(ON)}$	Reference Power Supply Drain Current			−1.4		mA	
	$I_{1(OFF)}$	Positive Power Supply Leakage Current			25		μA	Both Drivers OFF V_{IN} = 0.8V
	$I_{2(OFF)}$	Negative Power Supply Leakage Current			−25		μA	
	$I_{R(OFF)}$	Reference Power Supply Leakage Current			−25		μA	
SWITCH	t_{ON}	**Turn-ON Time**	Both Circuits		**0.3**	**0.5**	μs	See Below
	t_{OFF}	**Turn-OFF Time**			**0.8**	**1.2**	μs	
POWER	P_{ON}	ON Driver Power	Both Circuits		175		mW	Both Inputs V_{IN} = 2.5
	P_{OFF}	OFF Driver Power			1		mW	Both Inputs V_{IN} = 1V
FET	$V_{GS(f)}$	Gate Source Forward Voltage	Both Circuits		1.5		Volts	I_G = 1.0 mA, V_{DS} = 0

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

SWITCHING TIMES (at 25°C)

OFF MODEL

ON MODEL

INTERSIL

IH5005 — IH5007 2-Channel Drivers with SPST FET Switches Gate Available AND

FEATURES

- Gate Lead Available for Nulling Charge Injection Voltage
- Expansion Capability Available
- Each Channel Complete—Interfaces With Most Integrated Logic
- Low OFF power dissipation, 1 mW
- Low $r_{DS(ON)}$, 10Ω Max on IH5005

GENERAL DESCRIPTION

These switching circuits contain two channels in one package, each channel consisting of a driver circuit controlling a SPST junction FET switch. The driver interfaces DTL, TTL, or RTL logic signals for multiplexing, commutating, and D/A converter applications, which permits logic design directly with the switch function. Logic "1" at the input turns the FET switch ON, and Logic "0" turns it OFF. The gate lead of the FETs has been brought out to enable the application of a referral resistor for nulling offset voltage due to charge injection. Driver points are brought out to provide for the addition of external FETs for expansion capability.

ABSOLUTE MAXIMUM RATINGS

Analog Signal Voltage ($V_A - V_2$ or $V_1 - V_A$)	30V
Total Supply Voltage ($V_1 - V_2$)	36V
Pos. Supply Voltage to Ref. Voltage ($V_1 - V_R$)	25V
Ref. Voltage to Neg. Supply Voltage ($V_R - V_2$)	22V
Power Dissipation (Note)	750 mW
Current (Any Terminal)	30 mA
Storage Temperature	-65°C to +150°C
Operating Temperature	-65°C to +125°C
Lead Temperature (soldering, 10 sec.)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10 mW/°C.

3

DUAL SPST

IH5005 ($r_{DS(ON)}$ = 10Ω)
IH5006 ($r_{DS(ON)}$ = 30Ω)
IH5007 ($r_{DS(ON)}$ = 80Ω)

PACKAGE OUTLINES

NOTE: All dimensions in inches.

FD Package DD Package

ORDERING INFORMATION

IH 5 0 05 M FD

- FD — Package (See Outline Drawing)
- M — Temperature Range
  - M – Military (-55°C to +125°C)
  - I – Industrial (-20°C to +85°C)
  - C – Commercial (0°C to +70°C)
- 05 — Type
- 0 — Gate
- 5 — Analog
- IH — Intersil Hybrid

PRODUCT CONDITIONING

The following processes are performed 100% in accordance with MIL-STD-883.

Precap Visual—Meth. 2010, Cond. B
Stabilization Bake—Meth. 1008
Temp. Cycle—Meth. 1010
Centrifuge—Meth. 2001, Cond. D
Hermeticity—Meth. 1014, Cond. A, C
(Leak Rate $< 5 \times 10^{-8}$ atm cc/s)

ELECTRICAL CHARACTERISTICS

Applied Voltages for all tests: V_1 = +12V, V_2 = −18V, V_R = 0. Input test condition which guarantees FET switch ON or OFF as specified is used for output and power supply specifications.

	SYMBOL (NOTE)	CHARACTERISTIC	TYPE	ABSOLUTE MAX. LIMIT −55°	25°	125°	UNITS	TEST CONDITIONS
INPUT	$V_{IN(ON)}$	Input Voltage—ON	All Circuits	2.9 min	2.5 min	2.0 min	Volts	V_2 = −12V
	$V_{IN(OFF)}$	Input Voltage—OFF		1.4	1.0	0.6	Volts	V_2 = −12V
	$I_{IN(ON)}$	Input Current		120	60	60	μA	V_{IN} = 2.5V
	$I_{IN(OFF)}$	Input Leakage Current		0.1	0.1	2	μA	V_{IN} = 0.8V
SWITCH OUTPUT	$r_{DS(ON)}$	Drain-Source On Resistance	IH5007	80	80	150	Ω	V_D = 10V, I_S = 1 mA
			IH5006	30	30	50	Ω	
			IH5005	10	10	20	Ω	
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	IH5006 IH5007		2	100	nA	$V_D = V_S$ = −10V
	$I_{S(OFF)}$	Source Leakage Current			1	100	nA	V_S = 10V, V_D = −10V
	$I_{D(OFF)}$	Drain Leakage Current			1	100	nA	V_D = 10V, V_S = −10V
	$I_{D(ON)} + I_{S(ON)}$	Drive Leakage Current	IH5005		2	100	nA	$V_D = V_S$ = −10V
	$I_{S(OFF)}$	Source Leakage Current			10	1000	nA	V_S = 10V, V_D = −10V
	$I_{D(OFF)}$	Drain Leakage Current			10	1000	nA	V_D = 10V, V_S = −10V
POWER SUPPLY	$I_{1(ON)}$	Positive Power Supply Drain Current	All Circuits		3		mA	One Driver ON, V_{IN} = 2.5V
	$I_{2(ON)}$	Negative Power Supply Drain Current			−1.8		mA	
	$I_{R(ON)}$	Reference Power Supply Drain Current			−1.4		mA	
	$I_{1(OFF)}$	Positive Power Supply Leakage Current			25		μA	Both Drivers OFF, V_{IN} = 0.8V
	$I_{2(OFF)}$	Negative Power Supply Leakage Current			−25		μA	
	$I_{R(OFF)}$	Reference Power Supply Leakage Current			−25		μA	
SWITCHING	t_{ON}	Turn-ON Time	IH5005		1.0	1.5	μs	See Page 3
	t_{OFF}	Turn-OFF Time			2.5	3.7	μs	
	t_{ON}	Turn-ON Time	IH5006 IH5007		0.5	0.8	μs	
	t_{OFF}	Turn-OFF Time			1.0	1.5	μs	
POWER	P_{ON}	ON Driver Power	All Circuits		175		mW	Both Inputs V_{IN} = 2.5
	P_{OFF}	OFF Driver Power			1		mW	Both Inputs V_{IN} = 1.0
FET	$V_{GS(f)}$	Gate Source Forward Voltage	All Circuits		1.5		Volts	I_G = 1.0 mA, V_{DS} = 0
EXPAND	V_{P-P}	Peak-Peak Voltage at Expansion Outputs	All Circuits		30		Volts	V_{IN} = 0V / +3V; V_1 = +18V, V_2 = −18V, $R_L \geq 10\Omega$

NOTE: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

3

SWITCHING TIMES (at 25°C)

OFF MODEL

ON MODEL

TYPICAL CHARACTERISTICS (per channel)

APPLICATION

Expansion Capability IH5005

IH5009 — IH5024 Positive Signal Analog Switches

FEATURES

- **Switches Analog Signals up to 20 Volts Peak-to-Peak**
- **Each Channel Complete — Interfaces with Most Integrated Logic**
- **Switching Speeds Less than 0.5μs**
- **$I_{D(OFF)}$ Less than 500pA Typical at 70°C**
- **Effective $r_{ds(ON)}$ — 5Ω to 50Ω**
- **Commercial and Military Temperature Range Operation**

PACKAGE DIMENSIONS (Note 1)

8-Pin Plastic Package (PA)

14-Pin Plastic Package (PD)

16-Pin Plastic Package (PE)

14-Pin Ceramic Package (DD)

NOTE 1. Board drilling dimensions will equal standard practices for .020 diameter lead.

GENERAL DESCRIPTION

The IH5009 series of analog switches were designed to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost is a primary design objective (less than $1/switch in volume), performance and versatility have not been sacrificed.

Each package contains up to four channels of analog gating and is designed to eliminate the need for an external driver. The odd numbered devices are designed to be driven directly from T^2L open collector logic (15 volts) while the even numbered devices are driven directly from low level T^2L logic (5 volts). Each channel simulates a SPDT switch. SPST switch action is obtained by leaving the diode cathode unconnected; for SPDT action, the cathode should be grounded (0V). The parts are intended for high performance multiplexing and commutating usage. A logic "0" turns the channel ON and a logic "1" turns the channel OFF.

ABSOLUTE MAXIMUM RATINGS

Positive Analog Signal Voltage	30V
Negative Analog Signal Voltage	−15V
Diode Current	10mA
Power Dissipation (Note)	500mW
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C
Operating Temperature	
5009C Series	0°C to +70°C
5009M Series	−55°C to +125°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperature, derate at rate of 5mW/°C.

FUNCTIONAL DIAGRAM (Four Channel Switch)

Figure 1

ELECTRICAL CHARACTERISTICS (per channel)

SYMBOL (Note 1)	CHARACTERISTIC	TYPE	SPECIFICATION LIMIT −55°C (M) 0°C (C) MIN/MAX	25°C TYP.	25°C MIN/MAX	+125°C (M) +70°C (C) MIN/MAX	UNITS	TEST CONDITIONS (Note 2)
$I_{IN(ON)}$	Input Current-ON	All	0.1	.01	0.1	100	μA	$V_{IN}=0V$, $I_D=2mA$
$I_{IN(OFF)}$	Input Current-OFF	5V Logic Ckts	0.2	.04	0.1	10	nA	$V_{IN}=+4.5V$, $V_A=\pm10V$
$I_{IN(OFF)}$	Input Current-OFF	15V Logic Ckts	0.2	.04	0.2	10	nA	$V_{IN}=+11V$, $V_A=\pm10V$
$V_{IN(ON)}$	Channel Control Voltage-ON	5V Logic Ckts	0.5		0.5	0.5	V	See Figure 6, Note 3
$V_{IN(ON)}$	Channel Control Voltage-ON	15V Logic Ckts	1.5		1.5	1.5	V	See Figure 7, Note 3
$V_{IN(OFF)}$	Channel Control Voltage-OFF	5V Logic Ckts	4.5		4.5	4.5	V	See Figure 6, Note 3
$V_{IN(OFF)}$	Channel Control Voltage-OFF	15V Logic Ckts	11.0		11.0	11.0	V	See Figure 7, Note 3
$I_{D(OFF)}$	Leakage Current-OFF	5V Logic Ckts	0.2	.02	0.2	10	nA	$V_{IN}=+4.5V$, $V_A=\pm10V$
$I_{D(OFF)}$	Leakage Current-OFF	15V Logic Ckts	0.2	.02	0.2	10	nA	$V_{IN}=+11V$, $V_A=\pm10V$
$I_{D(ON)}$	Leakage Current-OFF	5V Logic Ckts	1.0	0.30	1.0	1000 (M) 200 (C)	nA	$V_{IN}=0V$, $I_S=1mA$
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	0.5	0.10	0.5	500 (M) 100 (C)	nA	$V_{IN}=0V$, $I_S=1mA$
$I_{D(ON)}$	Leakage Current-ON	5V Logic Ckts	1.0		1.0	10	nA	$V_{IN}=0V$, $I_S=2mA$
$I_{D(ON)}$	Leakage Current-ON	15V Logic Ckts	2.0		2.0	1000	nA	$V_{IN}=0V$, $I_S=2mA$
$r_{DS(ON)}$	Drain-Source ON-Resistance	5V Logic Ckts	150.0	90.00	150.0	385 (M) 240 (C)	Ω	$I_D=2mA$, $V_{IN}=0.5V$
$r_{DS(ON)}$	Drain-Source ON-Resistance	15V Logic Ckts	100.0	60.00	100.0	250 (M) 160 (C)	Ω	$I_D=2mA$, $V_{IN}=1.5V$
$t_{(ON)}$	Turn-ON Time	All		150.00	500.0		ns	See Figures 4 & 5
$t_{(OFF)}$	Turn-OFF Time	All		300.00	500.0		ns	See Figures 4 & 5
CT	Cross Talk	All		120.00			dB	f = 100Hz

NOTE 1: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

NOTE 2: Refer to Figure 3 for definition of terms.

NOTE 3: $V_{IN(ON)}$ and $V_{IN(OFF)}$ are test conditions guaranteed by the following test respectively $r_{DS(ON)}$ and $I_{D(OFF)}$.

3

THEORY OF OPERATION

The signals seen at the drain of a junction FET type analog switch can be arbitrarily divided into two categories: Those which are less than ±200mV, and those which are greater than ±200mV. The former category includes all those circuits where switching is performed at the virtual ground point of an op-amp, and it is primarily towards these applications that the IH5009 family of circuits is directed.

By limiting the analog signal at the switching point to ±200mV, no external driver is required and the need for additional power supplies is eliminated.

Devices are available with both common drains and with uncommitted drains.

Those devices which feature common drains have another FET in addition to the channel switches. This FET, which has gate and source connected such that $V_{GS}=0$, is intended to compensate for the on-resistance of the switch. When placed in series with the feedback resistor (Figure 2) the gain is given by

$$\text{GAIN} = \frac{10k\Omega + r_{DS(ON)}\,(\text{compensator})}{10k\Omega + r_{DS}\,(\text{switch})}$$

Figure 2. Use of Compensation FET

Clearly, the gain error caused by the switch is dependent on the match between the FETs rather than the absolute value of the FET on-resistance. For the standard product, all the FETs in a given package are guaranteed to match within 50Ω. Selections down to 5Ω are available however. The part numbers are shown in Table II. Since the absolute value of $r_{DS(ON)}$ is only guaranteed to be less than 100Ω or 150Ω, a substantial improvement in gain accuracy can be obtained by using the compensating FET.

DEFINITION OF TERMS

Figure 3.

NOISE IMMUNITY

The advantage of SPDT switching is high noise immunity when the series element is OFF. For example, if a +10 volt analog input is being swiched by T²L open collector logic, the series switch is OFF when the logic level is at +15 volts. At this time the diode conducts and holds the source at approximately +0.7 volts with an AC impedance to ground of 25 ohms. Thus random noise superimposed on the +10 volt analog input will not falsely trigger the FET since the noise voltage will be shunted to ground.

When switching a negative voltage, the input further increase the OFF voltage beyond pinch-off, so there is no danger of the FET turning on.

SWITCHING CHARACTERISTICS

Figure 4. High Level Logic

Figure 5. Standard DTL, TTL, RTL

LOGIC INTERFACE CIRCUITS

Figure 6. Interfacing with ±5V Logic

Figure 7. Interfacing with +15V Open Collector Logic

TYPICAL ELECTRICAL CHARACTERISTICS (per channel)

CROSSTALK MEASUREMENT CIRCUIT

3

APPLICATIONS (Note)

GAIN PROGRAMMABLE AMPLIFIER

3-CHANNEL MULTIPLEXER WITH SAMPLE & HOLD

NOTE: Additional applications information is given in Application Bulletin A004 "The 5009 Series of Low Cost Analog Switches".

DEVICE SCHEMATICS AND PIN CONNECTIONS

TABLE I

FOUR CHANNEL

IH5009 ($r_{DS(ON)} \leq 100\Omega$)
IH5010 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

IH5011 ($r_{DS(ON)} \leq 100\Omega$)
IH5012 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

THREE CHANNEL

IH5013 ($r_{DS(ON)} \leq 100\Omega$)
IH5014 ($r_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

IH5015 ($r_{DS(ON)} \leq 100\Omega$)
IH5016 ($r_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

TWO CHANNEL

IH5021 ($r_{DS(ON)} \leq 100\Omega$)
IH5022 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

IH5017 ($r_{DS(ON)} \leq 100\Omega$)
IH5018 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

SINGLE CHANNEL

IH5023 ($r_{DS(ON)} \leq 100\Omega$)
IH5023 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

IH5019 ($r_{DS(ON)} \leq 100\Omega$)
IH5020 ($r_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

ORDERING INFORMATION

1. BASIC PART NUMBERS: Table II shows part numbers corresponding to control logic levels, number of channels, and ON-resistance requirements.

TABLE II

BASIC PART NUMBER	PACKAGE CODE	INPUT LOGIC DRIVE	DESCRIPTION	EFFECTIVE $r_{DS(ON)}$ (OHMS) MAX.	$r_{DS(ON)}$ (OHMS) MAX. (25°C)
IH5009	XD	High Level	4-Channel, 15V Logic	50	100
IH5010	XD	DTL, TTL, RTL	4-Channel, 5V Logic	50	150
ITS7318	XD	High Level	4-Channel, 15V Logic	25	100
ITS7319	XD	DTL, TTL, RTL	4-Channel, 5V Logic	25	150
ITS7320	XD	High Level	4-Channel, 15V Logic	10	100
ITS7321	XD	DTL, TTL, RTL	4-Channel, 5V Logic	10	150
ITS7322	XD	High Level	4-Channel, 15V Logic	5	100
ITS7323	XD	DTL, TTL, RTL	4-Channel, 5V Logic	5	150
IH5011	XE	High Level	4-Channel, 15V Logic	Not Available	100
IH5012	XE	DTL, TTL, RTL	4-Channel, 5V Logic	Not Available	150
IH5013	XD	High Level	3-Channel, 15V Logic	50	100
IH5014	XD	DTL, TTL, RTL	3-Channel, 5V Logic	50	150
ITS7324	XD	High Level	3-Channel, 15V Logic	25	100
ITS7325	XD	DTL, TTL, RTL	3-Channel, 5V Logic	25	150
ITS7326	XD	High Level	3-Channel, 15V Logic	10	100
ITS7327	XD	DTL, TTL, RTL	3-Channel, 5V Logic	10	150
ITS7328	XD	High Level	3-Channel, 15V Logic	5	100
ITS7329	XD	DTL, TTL, RTL	3-Channel, 5V Logic	5	150
IH5015	XE	High Level	3-Channel, 15V Logic	Not Available	100
IH5016	XE	DTL, TTL, RTL	3-Channel, 5V Logic	Not Available	150
IH5017	XA	High Level	2-Channel, 15V Logic	50	100
IH5018	XA	DTL, TTL, RTL	2-Channel, 5V Logic	50	150
ITS7330	XA	High Level	2-Channel, 15V Logic	25	100
ITS7331	XA	DTL, TTL, RTL	2-Channel, 5V Logic	25	150
ITS7332	XA	High Level	2-Channel, 15V Logic	10	100
ITS7333	XA	DTL, TTL, RTL	2-Channel, 5V Logic	10	150
ITS7334	XA	High Level	2-Channel, 15V Logic	5	100
ITS7335	XA	DTL, TTL, RTL	2-Channel, 5V Logic	5	150
IH5019	XA	High Level	2-Channel, 15V Logic	Not Available	100
IH5020	XA	DTL, TTL, RTL	2-Channel, 5V Logic	Not Available	150
IH5021	XA	High Level	1-Channel, 15V Logic	50	100
IH5022	XA	DTL, TTL, RTL	1-Channel, 5V Logic	50	150
ITS7336	XA	High Level	1-Channel, 15V Logic	25	100
ITS7337	XA	DTL, TTL, RTL	1-Channel, 5V Logic	25	150
ITS7338	XA	High Level	1-Channel, 15V Logic	10	100
ITS7339	XA	DTL, TTL, RTL	1-Channel, 5V Logic	10	150
ITS7340	XA	High Level	1-Channel, 15V Logic	5	100
ITS7341	XA	DTL, TTL, RTL	1-Channel, 5V Logic	5	150
IH5023	XA	High Level	1-Channel, 15V Logic	Not Available	100
IH5024	XA	DTL, TTL, RTL	1-Channel, 5V Logic	Not Available	150

2. ORDER NUMBER FORMAT

BASIC PART NUMBER — C — PD

- PD: PACKAGE (SEE OUTLINE DRAWING)
- C: TEMPERATURE RANGE (C = COMMERCIAL, 0°C to +70°C) (M = MILITARY, -55°C to +125°C)
- BASIC PART NUMBER: 4 OR 5 DIGIT NUMBER FROM TABLE II

3. PACKAGES

PA – 8 PIN PLASTIC
DA – 8 PIN CERAMIC
PD – 14 PIN PLASTIC
DD – 14 PIN CERAMIC
PE – 16 PIN PLASTIC
DE – 16 PIN CERAMIC

4. ORDERING EXAMPLE

ITS 7232 — M — DD

- DD: PACKAGE 14 PIN CERAMIC DIP
- M: -55 C to 125 C OPERATING TEMPERATURE RANGE
- ITS 7232: 4 CHANNEL, 5V LOGIC CONTROL WITH $R_{DS(ON)}$ EFFECTIVE <5V

3

IH5025 — IH5038 Positive Signal Analog Switches

FEATURES

- **Switches up to +20V into High Impedance Loads (i.e. Non-Inverting Input of Operational Amp.)**
- **Driven from TTL Open Collector Logic**
- **$I_{D(OFF)} < 50pA$**
- **$r_{DS(ON)} < 150\Omega$**
- **$r_{DS(ON)}$ Match $< 50\Omega$ Channel to Channel**
- **Switching Speeds < 100ns**

ORDERING INFORMATION

GENERAL DESCRIPTION

The IH5025 series of analog switches were designed to fill the need for an easy-to-use, inexpensive switch for both industrial and military applications. Although low cost is a primary design objective (less than $1/switch in volume), performance and versatility have not been sacrificed.

Each package contains up to four channels of analog gating and is designed to eliminate the need for an external driver.

The entire family is designed to be driven from TTL open collector logic (15V), but can be driven from 5V logic if signal input is less than 1V. Alternatively, 20V switching is readily obtainable if TTL supply voltage is +25V. Normally, only positive signals can be switched; however, up to ±10V can be handled by the addition of a PNP stage (Figure 11) or by capacitor isolation (Figure 10). Each channel is a SPST switch. A logic "0" turns the channel ON and a logic "1" turns the channel OFF.

3

PACKAGE DIMENSIONS (NOTE 1)

Note 1: Board drilling requirements will equal standard practices for .020 diameter lead.

ABSOLUTE MAXIMUM RATINGS

Positive Analog Signal Voltage 25V
Negative Analog Signal Voltage ..... −0.5VDC
Drain Current 25mA
Power Dissipation (Note) 500mW
Storage Temperature ..... −65°C to +150°C

Operating Temperature
5025C Series ..... 0°C to +70°C
5025M Series ..... −55°C to +125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperature, derate at rate of 5mW/°C.

ELECTRICAL CHARACTERISTICS (per channel)

SYMBOL (Note 1)	CHARACTERISTIC	TYPE	SPECIFICATION LIMIT −55°C (M) 0°C (C)	25°C TYP.	25°C MIN/MAX	+125°C (M) +70°C (C)	UNITS MIN/MAX	TEST CONDITIONS
$I_{IN(ON)}$	Input Current-ON	All		0.30	1.0	100 (M) 25 (C)	nA (max)	$V_{IN} = 0V$
$I_{IN(OFF)}$	Input Current-OFF	All		0.20	1.0	50 (M) 10 (C)	nA (max)	$V_{IN} = 15V$
$V_{IN(ON)}$	Channel Control Voltage-ON	All	1.5		1.5	1.5	V (max)	See Figure 1
$V_{IN(OFF)}$	Channel Control Voltage-OFF	All	14.0		14.0	14.0	V (min)	See Figure 1
$I_{D(OFF)}$	Leakage Current-OFF	All		0.06	0.5	100 (M) 10 (C)	nA (max)	$V_{IN} = 15V$
$I_{D(ON)}$	Leakage Current-ON	Odd Nos.		1.00	10.0	5000 (M) 250 (C)	nA (max)	$V_{IN} = 0V$
$I_{D(ON)}$	Leakage Current-ON	Even Nos.		0.10	1.0	500 (M) 25 (C)	nA (max)	$V_{IN} = 0V$
$r_{DS(ON)}$	Drain-Source ON-Resistance	Odd Nos.		60.00	100.0	250 (M) 150 (C)	Ω (max)	$V_{IN} = 0.5V$, $I_D = 1mA$
$r_{DS(ON)}$	Drain-Source ON-Resistance	Even Nos.		90.00	150.0	385 (M) 240 (C)	Ω (max)	$V_{IN} = 0.5V$, $I_D = 1mA$
$r_{DS(ON)}$	Drain-Source ON-Resistance	Odd Nos.		85.00	160.0	420 (M) 250 (C)	Ω (max)	$V_{IN} = 1.0V$, $I_D = 1mA$
$r_{DS(ON)}$	Drain-Source ON-Resistance	Even Nos.		110.00	200.0	400 (M) 250 (C)	Ω (max)	$V_{IN} = 1.0V$, $I_D = 1mA$
$t_{(ON)}$	Turn-ON Time	All		0.10	0.2	0.4	μs (max)	See Figure 2
$t_{(OFF)}$	Turn-OFF Time	All		0.10	0.2	0.4	μs (max)	See Figure 2
$Q_{(INJ)}$	Charge Injection	All		7.00	20.0		mV_{p-p} (max)	See Figure 3
$V_{A(OFF)}$	Cross Coupling Rejection	All		0.10	1.0		mV_{p-p} (max)	See Figure 4
$\Delta r_{DS(ON)}$	Channel to Channel $r_{DS(ON)}$ Match	All		25.00	50.0	50	Ω (max)	$V_{IN} = 0.5V$, $I_D = 1mA$

NOTE 1: (OFF) and (ON) subscript notation refers to the conduction state of the FET switch for the given test.

TEST CIRCUITS

Figure 1

Figure 2

Figure 3

Figure 4

THEORY OF OPERATION

The IH5025 series differs from the IH5009 series in that floating outputs can be driven by the IH5025 series. This family is generally used when operating into a non-inverting input of an operational amplifier, while the IH5009 series is used in operations where it feeds into the inverting (virtual ground) input of an operational amplifier.

The IH5025 model is a basic charge area switching device, in that proper gating action depends upon the capacity vs. voltage relationship for the diode junctions. This C vs. V, when integrated out, produces total charge Q. It is Q total which is switched between the series diode and the gate to source and gate to drain junctions. The charge area (C vs. V) for the diode has been chosen to be a minimum of four (4) times the area of the gate to source junction, thus providing adequate safety margins to insure proper switching action.

If normal logical voltage levels of ground to +15V (open collector TTL) are used, only signals which are between 0V and +10V can be switched. The pinch-off range of the P-Channel FET has been selected between 2.0V and 3.9V; thus with +15V at the logical input, and a +10V signal input, 1.1V of margin exists for turn-off. When the IH5025 is used with 5V TTL logic, a maximum of +1V can be switched.

The gate of each FET has been brought out so that a "referral resistor" can be placed between gate and source. This is used to minimize charge injection effects. The connection is shown below:

For switching levels > +10V, the +15V power supply must be increased so that there is a minimum of 5V of difference between supply and signal. For example, to switch +15V level, +20V TTL supply is required. Up to +20V levels can be gated.

LOGIC INTERFACE CIRCUITS

When operating with TTL logic it is necessary to use pull-up resistors as shown in Figures 6 and 7. This ensures the necessary positive voltages for proper gating action.

Figure 5. Interfacing with +5V Logic

Figure 6. Interfacing with +15V Open Collector Logic

TYPICAL ELECTRICAL CHARACTERISTICS (per channel)

APPLICATIONS

Figure 7. Multiplexer from Positive Output Transducers

Figure 8. Sample and Hold Switch

Figure 9. Switching up to +20V Signals with T2L Logic

Figure 10. Switching Bipolar Signals with T2L Logic

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APPLICATIONS (Cont.)

ADVANTAGES OVER FIGURE NO. 10 METHOD
A. DC LEVELS OF UP TO ±10V CAN BE SWITCHED, AS WELL AS AC SIGNALS UP TO 100 KC; NO. 10 METHOD SWITCHES ONLY AC RANGE OF 10 Hz TO 10 kHz.
B. CKT IS NOW BREAK BEFORE MAKE

DISADVANTAGES:
A. PNP CKT DRAWS 3 mA, WHEN ON; THUS ADDS 3 mA X 30V = 90 mW POWER DISS.
B. t_{ON} TIME WILL BE CONSIDERABLY SLOWED DOWN FROM 100 ns (BEFORE IN FIGURE NO. 10) TO 1 → 2 μs NOW.

Figure 11. Switching Bipolar Signals with T²L Logic (Alternate Method)

Figure 12. Using the IH5028 as a Dual SPDT to Drive Ladder Networks for Bipolar Switching (up to ±10V)

Figure 13. Gain Control with High Input Impedance

DEVICE SCHEMATICS AND PIN CONNECTIONS

IH5025 ($R_{DS(ON)} \leq 100\Omega$)
IH5026 ($R_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

IH5027 ($R_{DS(ON)} \leq 100\Omega$)
IH5028 ($R_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

IH5029 ($R_{DS(ON)} \leq 100\Omega$)
IH5030 ($R_{DS(ON)} \leq 150\Omega$)
14 PIN DIP

IH5031 ($R_{DS(ON)} \leq 100\Omega$)
IH5032 ($R_{DS(ON)} \leq 150\Omega$)
16 PIN DIP

IH5033 ($R_{DS(ON)} \leq 100\Omega$)
IH5034 ($R_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

IH5035 ($R_{DS(ON)} \leq 100\Omega$)
IH5036 ($R_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

IH5037 ($R_{DS(ON)} \leq 100\Omega$)
IH5038 ($R_{DS(ON)} \leq 150\Omega$)
8 PIN DIP

3

INTERSIL

IH5040-IH5051 Family High Level CMOS Analog Gates

FEATURES

- Switches Greater Than 20Vpp Signals With ±15V Supplies
- Quiescent Current Less Than 1μA
- Overvoltage Protection to ±25V
- Break-Before-Make Switching t_{OFF} 200nsec, t_{ON} 300nsec Typical
- T²L, DTL, CMOS, PMOS Compatible
- Non-Latching With Supply Turn-Off
- Low r_{DS} (ON) – 35Ω
- New DPDT & 4PST Configurations
- Complete Monolithic Construction IH5040 through IH5047

CMOS ANALOG GATE PRODUCT CONDITIONING

The following processes are performed 100% in accordance with MIL-STD-883.

Precap Visual – Method 2010, Cond. B.
Stabilization Bake – Method 1008
Temperature Cycle – Method 1010
Centrifuge – Method 2001, Cond. E
Hermeticity – Method 1014, Cond. A, C.
(Leak Rate $< 5 \times 10^{-7}$ atm cc/s)

GENERAL DESCRIPTION

The IH5040 family of solid state analog gates are designed using an improved, high voltage CMOS monolithic technology. These devices provide ease-of-use and performance advantages not previously available from solid state switches. This improved CMOS technology provides input overvoltage capability to ±25 volts without damage to the device, and destructive latch-up of solid state analog gates has been eliminated. Early CMOS gates were destroyed when power supplies were removed with an input signal present. The IH5040 CMOS technology has eliminated this serious systems problem.

Key performance advantages of the 5040 series are TTL compatibility and ultra low-power operation. The quiescent current requirement is less than 1μA. Also designed into the 5040 is guaranteed Break-Before-Make switching, which is accomplished by extending the t_{ON} time (300 nsec TYP.) so that it exceeds t_{OFF} time (200 nsec TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON. This eliminates the need for external logic required to avoid channel to channel shorting during switching.

Many of the 5040 series improve upon and are pin-for-pin and electrical replacements for other solid state switches.

FUNCTIONAL DIAGRAM

FIGURE 1. TYPICAL DRIVER, GATE – IH5042

FUNCTIONAL DESCRIPTION

INTERSIL PART NO.	TYPE		R_{ON}	PIN/FUNCTIONAL EQUIVALENT (Note 1)
IH5040		SPST	75Ω	
IH5041	Dual	SPST	75Ω	
IH5042		SPDT	75Ω	DG 188AA/BA
IH5043	Dual	SPDT	75Ω	DG 191AP/BP
IH5044		DPST	75Ω	
IH5045	Dual	DPST	75Ω	DG 185AP/BP
IH5046		DPDT	75Ω	
IH5047		4PST	75Ω	
IH5048 (hybrid)	Dual	SPST	35Ω	
IH5049 (hybrid)	Dual	DPST	35Ω	DG 184AP/BP
IH5050 (hybrid)		SPDT	35Ω	DG 187AA/BA
IH5051 (hybrid)	Dual	SPDT	35Ω	DG 190AP/BP

NOTE 1. See Switching State diagrams for applicable package equivalency.

Pin and functional equivalent monolithic versions of the DG181, DG182, DG187 and DG188 are available. See data sheet for this and also IH181 to IH191.

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MAXIMUM RATINGS

Current (Any Terminal)	< 30mA
Storage Temperature	–65°C to +150°C
Operating Temperature	–55°C to +125°C
Power Dissipation	450mW
(All Leads Soldered to a P. C. Board) Derate 6mW/°C Above 70°C	
Lead Temperature (Soldering, 10 sec)	300°C

$V_I - V_2$	< 33V
$V_I - V_D$	< 30V
$V_D - V_2$	< 30V
$V_D - V_S$	< ±22V
$V_L - V_2$	< 33V
$V_L - V_{IN}$	< 30V
$V_L - V_R$	< 20V
$V_{IN} - V_R$	< 20V

ELECTRICAL CHARACTERISTICS (@ 25°C, V_1 = +15 V, V_2 = –15 V, V_L = +5 V, V_R = 0 V)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	-55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	TEST CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 2.4 V Note 1
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 0.8 V Note 1
$r_{DS(ON)}$	Drain–Source On Resistance	75(35)	75(35)	150(60)	80 (45)	80 (45)	130 (45)	Ω	(IH5048 Thru IH5051) I_S = 1mA, V_{ANALOG} = -10 V to +10 V
$\Delta r_{DS(ON)}$	Channel to Channel $R_{DS(ON)}$ Match	25(15)	25 (15)	25(15)	30(15)	30(15)	30(15)	Ω	(IH5048 thru IH5051) I_S (Each Channel) = 1 mA,
V_{ANALOG}	Min. Analog Signal Handling Capability	±11(±10)	±11(±10)	±11(±10)	±10(±10)	±10(±10)	±10(±10)	V	I_S = 10 mA (IH5048 thru IH5051)
$I_{D(OFF)}$	Switch OFF Leakage Current	1(1)	1(1)	100(100)	5(5)	5(5)	100(100)	nA	V_{ANALOG} = -10 V to +10 V (IH5048 thru IH5051
$I_{D(ON)}$ $+I_{S(ON)}$	Switch On Leakage Current	2(2)	2(2)	200(200)	10(10)	10 (10)	100(200)	nA	$V_D = V_S$ = -10 V to + 10 V (IH5048 thru IH5051)
t_{ON}	Switch "ON" Time		500(250)			500(300)		ns	R_L = 1 kΩ, V_{ANALOG} = -10 V to +10 V See Fig. A
t_{OFF}	Switch "OFF" Time		250(150)			250(150)		ns	R_L = 1 kΩ, V_{ANALOG} = -10 V to +10 V See Fig. A (IH5048 thru IH5051)
$Q_{(INJ.)}$	Charge Injection		15 (10)			20 (10)		mV	See Fig. B (IH5048 thru IH5051)
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R_L = 100Ω, C_L ≤ 5 pF See Fig. C
I_{V1}	+ Power Supply Quiescent Current	1	1	10	10	10	100	μA	
I_{V2}	– Power Supply Quiescent Current	1	1	10	10	10	100	μA	V_1 = +15 V, V_2 = -15 V, V_L = +5 V V_L = +5 V, V_R = 0
I_{VL}	+5 V Supply Quiescent Current	1	1	10	10	10	100	μA	Switch Duty Cycle ≤ 10%
I_{VR}	Gnd Supply Quiescent Current	1	1	10	10	10	100	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off; Any Other Channel Switches as per Fig. E

TEST CIRCUITS

FIG. A

FIG. B

FIG. C

NOTE 1: Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.

3

TYPICAL ELECTRICAL CHARACTERISTICS (Per Channel)

R_{DS} (ON) vs V_{ANALOG} SIGNAL

R_{DS} (ON) vs POWER SUPPLY VOLTAGE

CHARGE INJECTION vs V_{ANALOG} (SEE FIG. B) C_L = 10,000pF

FIGURE D

CROSS COUPLING REJECTION vs FREQUENCY

FIGURE E

OFF ISOLATION vs FREQUENCY

FIGURE F

POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE

FIGURE G

SWITCHING STATE DIAGRAMS

SWITCH STATES
ARE FOR LOGIC "1" INPUT

FLAT PACKAGE (FD) | DIP (DE) PACKAGE | (TW) PACKAGE

SPST
IH5040 (r_{DS} (ON) <75Ω)

DUAL SPST
IH5041 (r_{DS} (ON) <75Ω)

SPDT
IH5042 (r_{DS} (ON) <75Ω)

(DG188 EQUIVALENT)

DUAL SPDT
IH5043 (r_{DS}(ON) <75Ω)

(DG191 EQUIVALENT)

DPST
IH5044 (r_{DS} (ON) <75Ω)

DUAL DPST
IH5045 (r_{DS} (ON) <75Ω)

(DG185 EQUIVALENT)

3

SWITCHING STATE DIAGRAMS (Cont.)

SWITCH STATES
ARE FOR LOGIC "1" INPUT

FLAT PACKAGE | DIP (DE) PACKAGE | (TW) PACKAGE

DPDT
IH5046 (r_{DS} (ON) <75Ω)

4PST
IH5047 (r_{DS} (ON) <75Ω)

DUAL SPST
IH5048 (r_{DS} (ON) <35Ω)

DUAL DPST
IH5049 (r_{DS} (ON) <35Ω)

(DG184 EQUIVALENT)

SPDT
IH5050 (r_{DS} (ON) <35Ω)

(DG187 EQUIVALENT)

DUAL SPDT
IH5051 (r_{DS} (ON) <35Ω)

(DG190 EQUIVALENT)

3

APPLICATIONS

IMPROVED SAMPLE & HOLD
USING IH5043

FIGURE H

USING THE CMOS SWITCH TO DRIVE
AN R/2R LADDER NETWORK (2 LEGS)

FIGURE I

EXAMPLE: If $-V_{ANALOG} = -10VDC$ and $+V_{ANALOG} = +10VDC$ then Ladder Legs are switched between ±10VDC, depending upon state of Logic Strobe.

3

THEORY OF OPERATION

A. FLOATING BODY CMOS STRUCTURE

In a conventional C-MOS structure, the body of the "n" channel device is tied to the negative supply, thus forming a reverse biased diode between the drain/source and the body (Fig. J). Under certain conditions this diode can become forward biased; for example, if the supplies are off (at ground) and a negative input is applied to the drain. This can have serious consequences for two reasons. Firstly, the diode has no current limiting and if excessive current flows, the circuit may be permanently damaged. Secondly, this diode forms part of a parasitic SCR in the conventional C-MOS structure. Forward biasing the diode causes the SCR to turn on, giving rise to a "latch-up" condition.

Intersil's improved C-MOS process incorporates an additional diode in series with the body (Fig. K). The cathode of this diode is then tied to V+, thus effectively floating the body. The inclusion of this diode not only blocks the excessive current path, but also prevents the SCR from turning on.

FIGURE J

FIGURE K

B. OVERVOLTAGE PROTECTION

The floating body construction inherently provides overvoltage protection. In the conventional C-MOS process, the body of all N-channel FETs is tied to the most negative power supply and the body of all P-channel devices to the most positive supply (i. e., ±15V). Thus, for an overvoltage spike of > ±15V, a forward bias condition exists between drain and body of the MOSFET. For example, in Fig. J if the analog signal input is more negative than −15V, the drain to body of the N-channel FET is forward biased and destruction of the device can result. Now by floating the body, using diode D1, the drain to body of the MOSFET is still forward biased, but D1 is reversed biased so no current flows (up to the breakdown of D1 which is ⩾ 40V). Thus, negative excursions of the analog signal can go up to a maximum of -25V. When the signal goes positive (⩾ +15V, D1 is forward biased, but now the drain to body junction is reversed for the N-channel FET; this allows the signal to go to a maximum of +25V with no appreciable current flow. While the explanation above has been restricted to N-channel devices, the same applies to P-channel FETs and the construction is as shown in Fig. L. Fig. L describes an output stage showing the paralleling of an N and P channel to linearize the $r_{DS(ON)}$ with signal input. The presence of diodes D1 and D2 effectively floats the bodies and provides over voltage protection to a maximum of ±25V.

FIGURE L

DIGITALLY TUNED
LOW POWER ACTIVE FILTER

Constant gain, constant Q, variable frequency filter which provides simultaneous Lowpass, Bandpass, and Highpass outputs. With the component values shown, center frequency will be 235Hz and 23.5Hz for high and low logic inputs respectively, Q = 100, and Gain = 100.

$$f_n = \text{Center Frequency} = \frac{1}{2\pi RC}$$

LOGIC INTERFACING

FOR INTERFACING WITH T^2L OPEN COLLECTOR LOGIC.

TYP. EXAMPLE FOR +15V CASE SHOWN

3

FOR USE WITH CMOS LOGIC.

$15V \geq V_{DD} \geq 5V$
$0V \geq V_{SS} \geq -15V$

ORDERING INFORMATION

TYPE	ORDER PART NUMBER	PACKAGE	TEMPERATURE RANGE	FUNCTION
IH 5040	IH 5040 MDE	16 Pin Hermetic DIP	-55°C to 125°C	SPST
	IH 5040 CDE	16 Pin Hermetic DIP	0°C to 70°C	SPST
	IH 5040 CPE	16 Pin Plastic DIP	0°C to 70°C	SPST
	IH 5040 MFD	14 Pin Flat Pak	-55°C to 125°C	SPST
IH 5041	IH 5041 MDE	16 Pin Hermetic DIP	-55°C to 125°C	Dual SPST
	IH 5041 CDE	16 Pin Hermetic DIP	0°C to 70°C	Dual SPST
	IH 5041 CPE	16 Pin Plastic DIP	0°C to 70°C	Dual SPST
	IH 5041 MFD	14 Pin Flat Pak	-55°C to 125°C	Dual SPST
	IH 5041 CTW	TO-100	0°C to 70°C	Dual SPST
	IH 5041 MTW	TO-100	-55°C to 125°C	Dual SPST
IH 5042	IH 5042 MDE	16 Pin Hermetic DIP	-55°C to 125°C	SPDT
	IH 5042 CDE	16 Pin Hermetic DIP	0°C to 70°C	SPDT
	IH 5042 CPE	16 Pin Plastic DIP	0°C to 70°C	SPDT
	IH 5042 MFD	14 Pin Flat Pak	-55°C to 125°C	SPDT
	IH 5042 CTW	TO-100	0°C to 70°C	SPDT
	IH 5042 MTW	TO-100	-55°C to 125°C	SPDT
IH 5043	IH 5043 MDE	16 Pin Hermetic DIP	-55°C to 125°C	Dual SPDT
	IH 5043 CDE	16 Pin Hermetic DIP	0°C to 70°C	Dual SPDT
	IH 5043 CPE	16 Pin Plastic DIP	0°C to 70°C	Dual SPDT
	IH 5043 MFD	14 Pin Flat Pak	-55°C to 125°C	Dual SPDT
IH 5044	IH 5044 MDE	16 Pin Hermetic DIP	-55°C to 125°C	DPST
	IH 5044 CDE	16 Pin Hermetic DIP	0°C to 70°C	DPST
	IH 5044 CPE	16 Pin Plastic DIP	0°C to 70°C	DPST
	IH 5044 MFD	14 Pin Flat Pak	-55°C to 125°C	DPST
	IH 5044 CTW	TO-100	0°C to 70°C	DPST
	IH 5044 MTW	TO-100	-55°C to 125°C	DPST
IH 5045	IH 5045 MDE	16 Pin Hermetic DIP	-55°C to 125°C	Dual DPST
	IH 5045 CDE	16 Pin Hermetic DIP	0°C to 70°C	Dual DPST
	IH 5045 CPE	16 Pin Plastic DIP	0°C to 70°C	Dual DPST
	IH 5045 MFD	14 Pin Flat Pak	-55°C to 125°C	Dual DPST
IH 5046	IH 5046 MDE	16 Pin Hermetic DIP	-55°C to 125°C	DPDT
	IH 5046 CDE	16 Pin Hermetic DIP	0°C to 70°C	DPDT
	IH 5046 CPE	16 Pin Plastic DIP	0°C to 70°C	DPDT
	IH 5046 MFD	14 Pin Flat Pak	-55°C to 125°C	DPDT
IH 5047	IH 5047 MDE	16 Pin Hermetic DIP	-55°C to 125°C	4PST
	IH 5047 CDE	16 Pin Hermetic DIP	0°C to 70°C	4PST
	IH 5047 CPE	16 Pin Plastic DIP	0°C to 70°C	4PST
	IH 5047 MFD	14 Pin Flat Pak	-55°C to 125°C	4PST
IH 5048	IH 5048 MDE	16 Pin Hermetic DIP	-55°C to 125°C	Dual SPST
	IH 5048 CDE	16 Pin Hermetic DIP	0°C to 70°C	Dual SPST
	IH 5048 MFD	14 Pin Flat Pak	-55°C to 125°C	Dual SPST
	IH 5048 CTW	TO-100	0°C to 70°C	Dual SPST
	IH 5048 MTW	TO-100	-55°C to 125°C	Dual SPST
IH 5049	IH 5049 MDE	16 Pin Hermetic DIP	-55°C to 125°C	Dual DPST
	IH 5049 CDE	16 Pin Hermetic DIP	0°C to 70°C	Dual DPST
	IH 5049 MFD	14 Pin Flat Pak	-55°C to 125°C	Dual DPST
IH 5050	IH 5050 MDE	16 Pin Hermetic DIP	-55°C to 125°C	SPDT
	IH 5050 CDE	16 Pin Hermetic DIP	0°C to 70°C	SPDT
	IH 5050 MFD	14 Pin Flat Pak	-55°C to 125°C	SPDT
	IH 5050 MTW	TO-100	-55°C to 125°C	SPDT
	IH 5050 CTW	TO-100	0°C to 70°C	SPDT
IH 5051	IH 5051 MDE	16 Pin Hermetic DIP	-55°C to 125°C	Dual SPDT
	IH 5051 CDE	16 Pin Hermetic DIP	0°C to 70°C	Dual SPDT
	IH 5051 MFD	14 Pin Flat Pak	-55°C to 125°	Dual SPDT

PACKAGE DIMENSIONS

16 LEAD CERAMIC (DE)

16 LEAD PLASTIC

14 LEAD FLATPACK (FD)

TO–100 (TW) PACKAGE

NOTE: All dimensions in inches and (millimeters).

3

INTERSIL

IH5052/IH5053 CMOS Analog Gates

FEATURES

- **Switches Greater Than 20Vpp Signals With ±15V Supplies**
- **Quiescent Current Less Than 10μa**
- **Overvoltage Protection to ±25V**
- **Break-Before-Make Switching t_{OFF} 100nsec, t_{ON} 250nsec Typical**
- **T²L, DTL, CMOS, PMOS Compatible**
- **Non-Latching With Supply Turn-Off**
- **IH5052 4 Normally Closed Switches**
- **IH5053 4 Normally Open Switches**

GENERAL DESCRIPTION

The IH5052/3 solid state analog gates are designed using an improved, high voltage CMOS technology. This provides ease-of-use and performance advantages not previously available from solid state switches. This improved CMOS technology provides input overvoltage capability to ±25 volts without damage to the device, and the destructive latch-up of solid state analog gates has been eliminated. Early CMOS gates were destroyed when power supplies were removed with an input signal present. The INTERSIL CMOS technology has eliminated this serious systems problem. Key performance advantages are TTL compatible and ultra low-power operation. The quiescent current requirement is less than 10μA. Also designed into the IH5052/3 is guaranteed Break-Before-Make switching. This is logically accomplished by extending the t_{ON} time (400nsec TYP.) such that it exceeds t_{OFF} time (200nsec TYP.). This insures that an ON channel will be turned OFF before an OFF channel can turn ON and eliminates the need for external logic required to avoid channel to channel shorting during switching. The IH5052 is designed to have switch closure with Logic "0" (0.8V or less) and the IH5053 is designed to close switches with a Logical "1" (2.4V or more).

3

FUNCTIONAL DIAGRAM

PIN CONFIGURATIONS

DUAL-IN-LINE PACKAGE

ORDER NUMBERS:
IH5052MDE OR IH5052CDE

SWITCH STATES ARE FOR LOGIC "1" INPUT

ORDER NUMBERS:
IH5053MDE OR IH5053CDE

MAXIMUM RATINGS

Current (Any Terminal) ..... <30mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature ..... −55°C to +125°C
Power Dissipation 450mW
(All Leads Soldered to a P.C. Board)
Derate 6 mW/°C Above 70°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

$V_I—V_2$	<33V
$V_I—V_D$	<30V
$V_D—V_2$	<30V
$V_D—V_S$	<±22V
$V_L—V_2$	<33V
$V_L—V_{IN}$	<30V
$V_L—V_R$	<20V
$V_{IN}—V_R$	<20V

ELECTRICAL CHARACTERISTICS (@ 25°C, V_1 = +15V, V_2 = −15V, V_L = +5V, V_R = 0V)

PER CHANNEL		MIN./MAX. LIMITS							TEST CONDITIONS
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	−55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 2.4V (IH5053) = 0.8V (IH5052)
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 0.8V (IH5053) = 2.4V (IH5052)
$r_{DS(ON)}$	Drain-Source On Resistance	75	75	100	80	80	100	Ω	I_S = 1mA, V_{analog} = −10V to +10V
$\Delta r_{DS(ON)}$	Channel to Channel $R_{DS(ON)}$ Match	25	25	25	30	30	30	Ω	I_S (Each Channel) = 1 mA
V_{ANALOG}	Min. Analog Signal Handling Capability	±11	±11	±11	±10	±10	±10	V	I_S = 10mA
$I_{D(OFF)}$	Switch OFF Leakage Current	1	1	100	5	5	100	nA	V_{ANALOG} = −10V to +10V
$I_{D(ON)}$ + $I_{S(ON)}$	Switch On Leakage Current	2	2	200	10	10	100	nA	V_D = V_S = −10V to +10V
t_{ON}	Switch "ON" Time		500			500		ns	R_L = 1kΩ, V_{analog} = −10V to +10V See Fig. A
t_{OFF}	Switch "OFF" Time		250			250		ns	R_L = 1kΩ, V_{analog} = −10V to +10V See Fig. A
$Q_{(INJ.)}$	Charge Injection		15			20		mV	See Fig. B
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R_L = 100Ω, C_L ≤ 5pF See Fig. C
I_{V1}	+ Power Supply Quiescent Curent	10	10	100	10	10	100	μA	
I_{V2}	− Power Supply Quiescent Current	10	10	100	10	10	100	μA	V_1 = +15V, V_2 = −15V, V_L = +5V V_L = +5V, V_R = 0
I_{VL}	+5V Supply Quiescent Current	10	10	100	10	10	100	μA	Switch Duty Cycle ≤ 10%
I_{VR}	Gnd Supply Quiescent Current	10	10	100	10	10	100	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off; Any Other Channel Switches as per Fig. E

TEST CIRCUITS

FIG. A

FIG. B

FIG. C

TYPICAL ELECTRICAL CHARACTERISTICS (Per Channel)

r_{DS}(ON) vs V_{ANALOG} SIGNAL

r_{DS}(ON) vs POWER SUPPLY VOLTAGE

CHARGE INJECTION vs V_{ANALOG} (SEE FIG. B) C_L = 10,000pF

FIGURE D

CROSS COUPLING REJECTION vs FREQUENCY

FIGURE E

OFF ISOLATION vs FREQUENCY

FIGURE F

POWER SUPPLY QUIESCENT CURRENT vs LOGIC FREQUENCY RATE

FIGURE G

THEORY OF OPERATION

A. Floating Body CMOS Structure

In a conventional C-MOS structure, the body of the "n" channel device is tied to the negative supply, thus forming a reverse biased diode between the drain/source and the body (Fig. H). Under certain conditions this diode can become forward biased; for example, if the supplies are off (at ground) and a negative input is applied to the drain. This can have serious consequences for two reasons. Firstly, the diode has no current limiting and if excessive current flows, the circuit may be permanently damaged. Secondly, this diode forms part of a parasitic SCR in the conventional C-MOS structure. Forward biasing the diode causes the SCR to turn on, giving rise to a "latch-up" condition.

Intersil's improved C-MOS process incorporates an additional diode in series with the body (Fig. I). The cathode of this diode is then tied to V+, thus effectively floating the body. The inclusion of this diode not only blocks the excessive current path, but also prevents the SCR from turning on.

FIGURE H

FIGURE I

B. Overvoltage Protection

The floating body construction inherently provides overvoltage protection. In the conventional C-MOS process, the body of all N-channel FETs is tied to the most negative power supply and the body of all P-channel devices to the most positive supply (i.e., ±15V). Thus, for an overvoltage spike of > ±15V, a forward bias condition exists between drain and body of the MOSFET. For example, in Fig. H if the analog signal input is more negative than −15V, the drain to body of the N-channel FET is forward biased and destruction of the device can result. Now by floating the body, using diode D1, the drain to body of the MOSFET is still forward biased, but D1 is reversed biased so no current flows (up to the breakdown of D1 which is ≥ 40V). Thus, negative excursions of the analog signal can go up to a maximum of −25V. When the signal goes positive (≥ +15V, D1 is forward biased, but now the drain to body junction is reversed for the N-channel FET; this allows the signal to go to a maximum of +25V with no appreciable current flow. While the explanation above has been restricted to N-channel devices, the same applies to P-channel FETs and the construction is as shown in Fig. J. Fig. J describes an output stage showing the paralleling of an N and P-channel to linearize the $r_{DS(on)}$ with signal input. The presence of diodes D1 and D2 effectively floats the bodies and provides overvoltage protection to a maximum of ±25V.

FIGURE J

LOGIC INTERFACING

FOR INTERFACING WITH T2L OPEN COLLECTOR LOGIC.

TYP. EXAMPLE FOR +15V CASE SHOWN

FOR USE WITH CMOS LOGIC.

3

APPLICATIONS

PROGRAMMABLE GAIN NON-INVERTING AMPLIFIER WITH SELECTABLE INPUTS

ACTIVE LOW PASS FILTER WITH DIGITALLY SELECTED BREAK FREQUENCY

APPLICATIONS (Continued)

4-CHANNEL SEQUENCING MUX

Truth Table (IH5052)

ENABLE	MUX SEQUENCE RATE	SEQUENCER OUTPUT		SWITCH STATES (– DENOTES OFF)			
		2^0	2^1	SW1	SW2	SW3	SW4
0	0	0	0	—	—	—	—
1	0	0	0	ON	—	—	—
1	1 pulse	1	0	—	ON	—	—
1	2 pulses	0	1	—	—	—	—
1	3 pulses	1	1	—	—	—	ON
1	4 pulses	0	0	ON	—	—	—

3

A Latching DPDT

The latch feature insures positive switching action in response to non-repetitive or erratic commands. The A_1 and A_2 inputs are normally low. A HIGH input to A_2 turns S_1 and S_2 ON, a HIGH to A_1 turns S_3 and S_4 ON. Desirable for use with limit detectors, peak detectors, or mechanical contact closures.

Truth Table (IH5052)

COMMAND		STATE OF SWITCHES AFTER COMMAND	
A_2	A_1	S_3 & S_4	S_1 & S_2
0	0	same	same
0	1	on	off
1	0	off	on
1	1	INDETERMINATE	

PACKAGE DIMENSIONS

16 PIN CERAMIC PACKAGE (DE)

16-PIN FLAT PAK (FE)

NOTE: Dimensions in inches (millimeters)

3

INTERSIL

IH5140-IH5145 Family High Level CMOS Analog Gates

FEATURES

- **Super fast break before make switching t_{on} 80ns typ, t_{off} 50ns typ (SPST switches)**
- **Power supply currents less than 1μA**
- **"OFF" leakages less than 100pA @ 25°C guaranteed**
- **Non-latching with supply turn-off**
- **Single monolithic CMOS chip**
- **Plug-in replacements for IH5040 family and part of the DG180 family to upgrade speed and leakage**
- **Greater than 1MHz toggle rate**
- **Switches greater than 20Vp-p signals with ±15V supplies**
- **T^2L, CMOS direct compatibility**

CMOS ANALOG GATE PRODUCT CONDITIONING

The following processes are performed 100% in accordance with MIL-STD-883.
Precap Visual — Method 2010, Cond. B
Stabilization Bake — Method 1008
Temperature Cycle — Method 1010
Centrifuge — Method 2001, Cond. E
Hermeticity — Method 1014, Cond. A, C
(Leak Rate < 5 x 10^{-7} atm cc/s)

3

GENERAL DESCRIPTION

The IH5140 Family of CMOS monolithic switches utilizes Intersil's latch-free junction isolated processing to build the fastest switches now available. "OFF" leakages are guaranteed to be less than 100pA at 25°C. These switches can be toggled at a rate of greater than 1MHz with super fast t_{on} times (80ns typical) and faster t_{off} times (50ns typical) guaranteeing break before make switching. This family of switches therefore combines the speed of the hybrid FET DG180 Family with the reliability and low power consumption of a monolithic CMOS construction.

No quiescent power is dissipated in either the "ON" or the "OFF" state of the switch. Maximum power supply current is 1μA from any supply and typical quiescent currents are in the 10nA range which makes these devices ideal for portable equipment and military applications.

The IH5140 Family is completely compatible with TTL (5V) logic, TTL open collector logic and CMOS logic gates. It is pin compatible with Intersil's IH5040 Family and part of the DG180/190 Family as shown in the switching state diagrams on page 8.

FUNCTIONAL DIAGRAM

FIGURE 1. Typical Driver/Gate — IH5142

ORDERING INFORMATION

Order Part Number	Function	Package	Temperature Range
IH5140 MDE	SPST	16 Pin Hermetic DIP	-55°C to 125°C
IH5140 CDE	SPST	16 Pin Hermetic DIP	0°C to 70°C
IH5140 CPE	SPST	16 Pin Plastic DIP	0°C to 70°C
IH5140 MFD	SPST	14 Pin Flat Pack	-55°C to 125°C
IH5141 MDE	Dual SPST	16 Pin Hermetic DIP	-55°C to 125°C
IH5141 CDE	Dual SPST	16 Pin Hermetic DIP	0°C to 70°C
IH5141 CPE	Dual SPST	16 Pin Plastic DIP	0°C to 70°C
IH5141 MFD	Dual SPST	14 Pin Flat Pack	-55°C to 125°C
IH5141 CTW	Dual SPST	TO-100	0°C to 70°C
IH5141 MTW	Dual SPST	TO-100	-55°C to 125°C
IH5142 MDE	SPDT	16 Pin Hermetic DIP	-55°C to 125°C
IH5142 CDE	SPDT	16 Pin Hermetic DIP	0°C to 70°C
IH5142 CPE	SPDT	16 Pin Plastic DIP	0°C to 70°C
IH5142 MFD	SPDT	14 Pin Flat Pack	-55°C to 125°C
IH5142 CTW	SPDT	TO-100	0°C to 70°C
IH5142 MTW	SPDT	TO-100	-55°C to 125°C
IH5143 MDE	Dual SPDT	16 Pin Hermetic DIP	-55°C to 125°C
IH5143 CDE	Dual SPDT	16 Pin Hermetic DIP	0°C to 70°C
IH5143 CPE	Dual SPDT	14 Pin Plastic DIP	0°C to 70°C
IH5143 MFD	Dual SPDT	14 Pin Flat Pack	-55°C to 125°C
IH5144 MDE	DPST	16 Pin Hermetic DIP	-55°C to 125°C
IH5144 CDE	DPST	16 Pin Hermetic DIP	0°C to 70°C
IH5144 CPE	DPST	16 Pin Plastic DIP	0°C to 70°C
IH5144 MFD	DPST	14 Pin Flat Pack	-55°C to 125°C
IH5144 CTW	DPST	TO-100	0°C to 70°C
IH5144 MTW	DPST	TO-100	-55°C to 125°C
IH5145 MDE	Dual DPST	16 Pin Hermetic DIP	-55°C to 125°C
IH5145 CDE	Dual DPST	16 Pin Hermetic DIP	0°C to 70°C
IH5145 CPE	Dual DPST	16 Pin Plastic DIP	0°C to 70°C
IH5145 MFD	Dual DPST	14 Pin Flat Pack	-55°C to 125°C

MAXIMUM RATINGS

Current (Any Terminal) ..... < 30 mA
Storage Temperature ..... -65°C to +150°C
Operating Temperature ..... -55°C to +125°C
Power Dissipation ..... 450 mW
(All Leads Soldered to a P.C. Board)
Derate 6 mW/°C Above 70°C
Soldering Temperature

$V_I—V_2$ <33V
$V_I—V_D$ <30V
$V_D—V_2$ <30V
$V_D—V_S$ <±22V
$V_L—V_2$ <33V
$V_L—V_{IN}$ <30V
$V_L—V_R$ <20V
$V_{IN}—V_R$ <20V

ELECTRICAL CHARACTERISTICS (@ 25°C, V_1 = +15V, V_2 = -15V, V_L = +5V, V_R = 0 V)

PER CHANNEL		MIN./MAX. LIMITS							
		MILITARY			COMMERCIAL				
SYMBOL	CHARACTERISTIC	-55°C	+25°C	+125°C	0	+25°C	+70°C	UNITS	TEST CONDITIONS
$I_{IN(ON)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 2.4 V Note 1
$I_{IN(OFF)}$	Input Logic Current	1	1	1	1	1	1	μA	V_{IN} = 0.8 V Note 1
$R_{DS(ON)}$	Drain—Source On Resistance	50	50	75	75	75	100	Ω	I_S = -10 mA V_{ANALOG} = -10 V to +10 V
$\Delta R_{DS(ON)}$	Channel to Channel $R_{DS(ON)}$ Match	25	25	25	30	30	30	Ω	I_S (Each Channel) = -10 mA
V_{ANALOG}	Min. Analog Signal Handling Capability	±11	±11	±11	±10	±10	±10	V	I_S = 10 mA
$I_{D(OFF)}$ $I_{S(OFF)}$	Switch OFF Leakage Current	0.1 0.1	0.1 0.1	20 20	0.5 0.5	0.5 0.5	20 20	nA	V_D = +10 V, V_S = -10 V V_D = -10V, V_S = +10 V
$I_{D(ON)}$ $+I_{S(ON)}$	Switch On Leakage Current	0.2	0.2	40	1	1	40	nA	V_D = V_S = -10 V to +10 V
t_{ON} t_{OFF}	Switch "ON" Time Switch "OFF" Time	See pages 4 & 5 for switching time specifications and timing diagrams.							
$Q_{(INJ.)}$	Charge Injection		10			15		mVPP	See Fig. 4, Note 2
OIRR	Min. Off Isolation Rejection Ratio		54			50		dB	f = 1 MHz, R_L = 100Ω, C_L ≤ 5 pF See Fig. 5, Note 2
I_{V1}	+ Power Supply Quiescent Current	1.0	1.0	10.0	10	10	100	μA	
I_{V2}	- Power Supply Quiescent Current	1.0	1.0	10.0	10	10		μA	V_1 = +15 V, V_2 = -15 V, V_L = +5 V, V_R = 0
I_{VL}	+5 V Supply Quiescent Current	1.0	1.0	10.0	10	10	100	μA	Switch Duty Cycle < 10% See Fig. 6
I_{VR}	Gnd Supply Quiescent Current	1.0	1.0	10.0	10	10	100	μA	
CCRR	Min. Channel to Channel Cross Coupling Rejection Ratio		54			50		dB	One Channel Off; Any Other Channel Switches See Fig. 7, Note 2

Note: 1. Some channels are turned on by high "1" logic inputs and other channels are turned on by low "0" inputs; however 0.8V to 2.4V describes the min. range for switching properly. Refer to logic diagrams to see absolute value of logic input required to produce "ON" or "OFF" state.
2. Charge injection, OFF isolation, and Channel to Channel isolation are only sample tested in production.

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FIGURE 2. $R_{DS(ON)}$ vs. Temp., @ ±15V, +5V Supplies.

FIGURE 3. $R_{DS(ON)}$ vs. Power Supplies.

FIGURE 4. Charge Injection vs. Analog Signal.

FIGURE 5. "OFF" Isolation vs. Frequency.

FIGURE 6. Power Supply Current Draws vs. Logic Strobe Rate.

FIGURE 7. Channel to Channel Cross Coupling Rejection vs. Frequency.

SWITCHING TIME SPECIFICATIONS

(t_{ON}, t_{OFF} are maximum specifications and t_{ON}-t_{OFF} is minimum specifications)

Part Number	Symbol	Characteristics	MILITARY -55°C	MILITARY +25°C	MILITARY +125°C	COMMERCIAL 0°C	COMMERCIAL +25°C	COMMERCIAL +70°C	Units	Test Conditions
IH5140-5141	t_{ON}	Switch "ON" time		100			150		ns	Figure 8
	t_{OFF}	Switch "OFF" time		75			125			
	t_{ON}-t_{OFF}	Break-before-make		10			5			
	t_{ON}	Switch "ON" time		150			175		ns	Figure 9
	t_{OFF}	Switch "OFF" time		125			150			
	t_{ON}-t_{OFF}	Break-before-make		10			5			
IH5142-5143	t_{ON}	Switch "ON" time		175			250		ns	Figure 8
	t_{OFF}	Switch "OFF" time		125			150			
	t_{ON}-t_{OFF}	Break-before-make		10			5			
	t_{ON}	Switch "ON" time		200			300		ns	Figure 9
	t_{OFF}	Switch "OFF" time		125			150			
	t_{ON}-t_{OFF}	Break-before-make		10			5			
	t_{ON}	Switch "ON" time		175			250		ns	Figure 10
	t_{OFF}	Switch "OFF" time		125			150			
	t_{ON}-t_{OFF}	Break-before-make		10			5			
	t_{ON}	Switch "ON" time		200			300		ns	Figure 11
	t_{OFF}	Switch "OFF" time		125			150			
	t_{ON}-t_{OFF}	Break-before-make		10			5			
IH5144-5145	t_{ON}	Switch "ON" time		175			250		ns	Figure 8
	t_{OFF}	Switch "OFF" time		125			150			
	t_{ON}-t_{OFF}	Break-before-make		10			5			
	t_{ON}	Switch "ON" time		200			300		ns	Figure 9
	t_{OFF}	Switch "OFF" time		125			150			
	t_{ON}-t_{OFF}	Break-before-make		10			5			

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NOTE: SWITCHING TIMES ARE MEASURED @ 90% PTS.

FIGURE 8.

FIGURE 9.

FIGURE 10.

FIGURE 11.

TYPICAL SWITCHING APPLICATIONS

SCALE: VERT. = 5V/DIV.
HORIZ. = 100ns/DIV.

TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 8)

-55°C

+25°C

+125°C

TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 9)

-55°C

+25°C

+125°C

TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 10)

+25°C

TTL OPEN COLLECTOR LOGIC DRIVE (Corresponds to Figure 11)

+25°C

APPLICATIONS

FIGURE 12. Improved Sample and Hold Using IH5143

EXAMPLE: If $-V_{ANALOG} = -10VDC$ and $+V_{ANALOG} = +10VDC$ then Ladder Legs are switched between ±10VDC, depending upon state of Logic Strobe.

FIGURE 13. Using the CMOS Switch to Drive an R/2R Ladder Network (2 Legs)

CONSTANT GAIN, CONSTANT Q, VARIABLE FREQUENCY FILTER WHICH PROVIDES SIMULTANEOUS LOWPASS, BANDPASS, AND HIGHPASS OUTPUTS. WITH THE COMPONENT VALUES SHOWN, CENTER FREQUENCY WILL BE 235Hz AND 23.5Hz FOR HIGH AND LOW LOGIC INPUTS RESPECTIVELY, Q = 100, AND GAIN = 100.

$$f_n = \text{CENTER FREQUENCY} = \frac{1}{2\pi RC}$$

FIGURE 14. Digitally Tuned Low Power Active Filter.

APPLICATION NOTE

To maximize switching speed on the IH5140 family use TTL open collector logic (15V with a 1K or less collector resistor). For SPST switches, typical $t_{on} \approx 80ns$ and typical $t_{off} \approx 50ns$ for signals in range of -10V to +10V with this high level drive configuration. The SPDT and DPST switches are approximately 30ns slower in both t_{on} and t_{off} with the same drive configuration. 15V CMOS logic levels can be used (0V to +15V), but propagation delays in the CMOS logic will slow down the switching (typical 50ns → 100ns delays).

When driving the IH5140 Family from either +5V TTL or CMOS logic, switching times run 20ns slower than if they were driven from +15V logic levels. Thus $t_{on} \approx$ 105ns typical, and $t_{off} \approx$ 75ns typical for SPST switches and 135ns typical and 105ns typical (t_{on}, t_{off}) for SPDT or DPST switches. The low level drive can be made as fast as the high level drive if ±5V strobe levels are used instead of the usual 0V→+3.0V drive. Pin 13 is taken to -5V instead of the usual GND and strobe input is taken from +5V to -5V levels as shown in Figure 15.

The typical channel of the IH5140 family consists of an N-channel MOS-FET. The N-channel MOS-FET uses a "Body Puller" FET to drive the body to -15V (±15V supplies) to get good breakdown voltages when the switch is in the off state (See Fig. 16). This "Body Puller" FET also allows the N-channel body to electrically float when the switch is in the on state producing a fairly constant $R_{DS}(ON)$ with different signal voltages. While this "Body Puller" FET improves switch performance, it can cause a problem when analog input signals are present (negative signals only) and power supplies are off. This fault condition is shown in Figure 17.

Current will flow from -10V analog voltage through the drain to body junction of Q1, then through the drain to body junction of Q3 to GND. This means that there is 10V across two forward-biased silicon diodes and current will go to whatever value the input signal source is capable of supplying. If the analog input signal is derived from the same supplies as the switch this fault condition cannot occur. Turning off the supplies would turn off the analog signal at the same time.

This fault situation can also be eliminated by placing a diode in series with the negative supply line (pin 14) as shown in Figure 18. Now when the power supplies are off and a negative input signal is present this diode is reverse biased and no current can flow.

FIGURE 15.

FIGURE 16.

FIGURE 17.

FIGURE 18.

INTERSIL

SWITCHING STATE DIAGRAMS

SWITCH STATES ARE FOR LOGIC "1" INPUT

SPST
IH5140 (R_{DS} (ON) <75Ω)

DUAL SPST
IH5141 (R_{DS} (ON) <75Ω)

SPDT
IH5142 (R_{DS}(ON) < 75Ω)

DUAL SPDT
IH5143 (R_{DS} (ON) <75Ω)

DPST
IH5144 (R_{DS} (ON) <75Ω)

DUAL DPST
IH5145 (R_{DS} (ON) <75Ω)

PACKAGE DIMENSIONS

16 LEAD CERAMIC (DE)

16 LEAD PLASTIC

14 LEAD FLATPACK (FD)

TO-100 (TW) PACKAGE

NOTE: All dimensions in inches and (millimeters).

3

IH401/IH401A VARAFET Switch

FEATURES

- $r_{DS(on)}$ = 25 ohms Typical (IH401)
- $I_{D(off)}$ of 10pA Typical
- Switching Times of 25ns for t_{on} and 75ns for t_{off} (R_L=1kΩ)
- Built-In Overvoltage Protection to Plus or Minus 25V
- Charge Injection of 3mV Typical into 0.01μF Capacitor
- $C_{ISS(on)}$ <1pF Typical
- Can Be Used for Hybrid Construction

SCHEMATIC/CONNECTION DIAGRAM

GENERAL DESCRIPTION

The IH401 is made up of 4 monolithically constructed combinations of a varactor type diode and an N-channel Junction FET. The FET itself is very similar to the popular 2N4391, and the driver diode is a specially designed diode, such that its capacity is a strong function of the voltage across it. The driver diode is electrically in series with the gate of the N-channel FET and simulates a back to back diode structure; this structure is needed to prevent forward biasing the source to gate or drain to gate junctions of the FET when used in switching applications.

Previous applications of Junction FETs required the addition of diodes, in series with the gate, and then perhaps a gate to source referral resistor or a capacitor in parallel with the diode; therefore, at least 3 components were required to perform the switch function. The IH401 does this same job in one component (with a great deal better performance characteristics).

Like a standard FET, to practically perform a solid state switch function a translator should be added to drive the diode. This translator takes the T^2L levels and converts them to voltages required to drive the diode/FET system (typically a 0V to -15V translation and a 3V to +15V shift). With ±15V power supplies, the IH401 will typically switch 18Vp-p at any frequency from dc to 20MHz, with less than 30 ohms $r_{DS(on)}$. The IH401A will typically switch 22Vp-p with less than 50 ohms $r_{DS(on)}$.

ORDERING INFORMATION

DIP Package: IH401JE
IH401AJE

PACKAGE DIMENSIONS/PAD LAYOUT

16 LEAD CER-DIP

Note: All dimensions in inches, ±.010 unless otherwise shown.

ABSOLUTE MAXIMUM RATINGS

V^+ to V^- 35V
V^+ 35V
V^- 35V
V^+ to V_{IN} 40V

Operating Temperature ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... 300°C

ELECTRICAL CHARACTERISTICS AT 25°C (unless otherwise specified)

SYMBOL	CHARACTERISTIC	CONDITIONS	IH401 MIN	IH401 TYP	IH401 MAX	UNIT
$R_{DS(on)}$	Switch "on" Resistance	V_{DRIVE} = 15V, V_{DRAIN} = −7.5V, I_D = 10mA		20	30	Ω
V_P	Pinch-Off Voltage	I_D = 1 nA, V_{DS} = 10V	4	6	7.5	V
$I_{D(off)}$	Switch "off" Current or "off" Leakage	V_{DRIVE} = −15V, V_{SOURCE} = −7.5V, V_{DRAIN} = +7.5V		10	200	pa
$I_{D(off)}$	Switch "off" Leakage at 125°C	Same as Above		0.25	50	na
$I_{S(off)}$	Switch "off" Current	V_{DRIVE} = −15V, V_{DRAIN} = −7.5V, V_{SOURCE} = +7.5V		10	200	pa
$I_{S(off)}$	Switch "off" Leakage at 125°C	Same as Above		0.3	50	na
$I_{D(on)}$ + $I_{S(on)}$	Switch Leakage when Turned "on"	V_D = V_S = −7.5V, V_{DRIVE} = +15V		0.02	2	na
V_{analog}	AC Input Voltage Range without Distortion	See Figure B	15	18		V_{p-p}
V_{inject}	Charge Injection Amplitude	See Figure C		3	10	mV_{p-p}
BV_{diode}	Diode Reverse Breakdown Voltage. This Correlates to Overvoltage Protection	V_D = V_S = −V, I_{DRIVE} = 1 μA, V_{DRIVE} = 0V	−30	−45		V
BV_{gss}	Gate to Source or Gate to Drain Reverse Breakdown Voltage	V_{DRIVE} = −V, V_D = V_S = 0V, I_{DRIVE} = 1 μA	30	41		V
I_{DSS}	Maximum Current Switch can Deliver (Pulsed)	V_{DRIVE} = 15V, V_S = 0V, V_D = +10V	45	70		mA
t_{on}	Switch "on" time (Note 1)	See Figure A		25	50	ns
t_{off}	Switch "off" time (Note 1)	See Figure A		75	150	ns

NOTE 1: Driving waveform must be >100ns rise and fall time.

FIGURE A

FIGURE B

FIGURE C

ELECTRICAL CHARACTERISTICS AT 25°C (unless otherwise specified)

SYMBOL	CHARACTERISTIC	CONDITIONS	IH401A MIN	IH401A TYP	IH401A MAX	UNIT
$r_{DS(on)}$	Switch "on" Resistance	V_{DRIVE} = 15V, V_{DRAIN} = −10V, I_D = 10mA		35	50	Ω
V_P	Pinch-Off Voltage	I_D = 1 nA, V_{DS} = 10V	3	4	5	V
$I_{D(off)}$	Switch "off" Current or "off" Leakage	V_{DRIVE} = −15V, V_{SOURCE} = −10V, V_{DRAIN} = +10V		10	200	pa
$I_{D(off)}$	Switch "off" Leakage at 125°C	Same as Above		0.25	50	na
$I_{S(off)}$	Switch "off" Current	V_{DRIVE} = −15V, V_{DRAIN} = −10V, V_{SOURCE} = +10V		10	200	pa
$I_{S(off)}$	Switch "off" Leakage at 125°C	Same as Above		0.3	50	na
$I_{D(on)}$ + $I_{S(on)}$	Switch Leakage when Turned "on"	V_D = V_S = −10V, V_{DRIVE} = +15V		0.02	2	na
V_{analog}	AC Input Voltage Range without Distortion	See Figure B	20	22		V_{p-p}
V_{inject}	Charge Injection Amplitude	See Figure C		3	10	mV_{p-p}
BV_{diode}	Diode Reverse Breakdown Voltage. This Correlates to Overvoltage Protection	V_D = V_S = −V, I_{DRIVE} = 1 μA, V_{DRIVE} = 0V	−30	−45		V
BV_{gss}	Gate to Source or Gate to Drain Reverse Breakdown Voltage	V_{DRIVE} = −V, V_D = V_S = 0V, I_{DRIVE} = 1 μA	30	41		V
I_{DSS}	Maximum Current Switch can Deliver (Pulsed)	V_{DRIVE} = 15V, V_S = 0V, V_D = +10V	35	55		mA
t_{on}	Switch "on" time (Note 1)	See Figure A		25	50	ns
t_{off}	Switch "off" time (Note 1)	See Figure A		75	150	ns

NOTE: Driving waveform must be >100ns rise and fall time.

APPLICATIONS

IH401 FAMILY

In general, the IH401 family can be used in any application formally using a JFET/isolation diode combination (2N4391 or similar). Like standard FET circuits, the IH401 requires a translator for normal analog switch function. The translator is used to boost the TTL input signals to the ±15V analog supply levels which allow the IH401 to handle ±7.5V analog signals (or IH401A to handle ±10V analog signals). A typical simple PNP translator is shown in Figure 1.

FIGURE 1

Although this simple PNP circuit represents a minimum of components, it requires open collector TTL input and $t_{(off)}$ is limited by the collector load resistor (approximately 1.5μs for 10kΩ). Improved switching speed can be obtained by increasing the complexity of the translator stage.

A translator which overcomes the problems of the simple PNP stage is the Intersil IH6201.* This translator driving an IH401 varafet produces the following typical features:

- t_{on} time of approx. 200ns } break before make
- t_{off} time of approx. 80ns } switch
- TTL compatible strobing levels of

- $I_{D(on)}$ + $I_{S(on)}$ typically 20pA up to ±10V analog signals
- $I_{D(off)}$ or $I_{S(off)}$ typically 20pA
- Quiescent current drain of approx. 100nA in either "on" or "off" case

APPLICATIONS (Cont.)

*The IH6201 is a dual translator (two independent translators per package) constructed from monolithic CMOS technology. The schematic of one-half IH6201, driving one-fourth of an IH401, is shown in Figure 2.

NOTE: Each translator output has a θ and $\bar{\theta}$ output. $\bar{\theta}$ is just the inverse of θ, i.e., ($\bar{\theta}$ output is 180° out of phase with respect to θ output).

FIGURE 2

A very useful feature of this system is that one-half of an IH6201 and one-half of an IH401 can combine to make a SPDT switch, or an IH6201 plus an IH401 can make a dual SPDT analog switch. (See III.)

I. DUAL SPST ANALOG SWITCH

NOTE: Either switch is turned on when strobe input goes high.

APPLICATIONS (Cont.)

II. DPDT ANALOG SWITCH

III. DUAL SPDT

IV. DUAL DPST

INTERSIL

G115/G123
4 and 6-Channel MOS FET Switches Industrial Series
−20°C to +85°C

FEATURES

- Integrated MOS-FET Constant-Current Sources for tive Driver-Collector Pull-up
- Integrated Zener Diode Protection for Both Positive and Negative Spike Protection
- P-Channel Enhancement-Type Switches

GENERAL DESCRIPTION

These switches may be connected directly to the INTERSIL switch-driver D123 series without the need of any interfacing components, and are internally protected by a Zener diode integrated on the silicon chip. A MOS-FET used as a current source provides an active pull-up for faster switching capability. The active pull-up FET can be disabled without sacrificing the Zener protection of the gates.

ABSOLUTE MAXIMUM RATINGS (25°C)

Source Current (I_S)	100 mA
Drain Current (I_D)	100 mA
Gate Current (I_G)	5 mA
Pull-up Control Current (I_P)	100 μA
Body to Source ($V_B - V_S$)	−2V to +25V
Body to Drain ($V_B - V_D$)	−2V to +25V
Body to Gate ($V_B - V_G$)	+35V
Body to Pull-up ($V_B - V_P$)	+35V
Power Dissipation (derate 10mW/°C above 70°C)	750mW
Lead Temperature (soldering, 10 sec.)	300°C

ORDERING INFORMATION

3

PRODUCT CONDITIONING

Units receive the following processing before final electrical test:

Temperature Cycle – −65°C to +150°C, 5 cycles

Hermeticity–Fluorocarbon Gross Leak, 100%
Helium Fine Leak, 2% AQL

ELECTRICAL CHARACTERISTICS (per channel unless noted)

	PARAMETER	LIMITS					CONDITIONS	
		−20°C	25°C	85°C	MIN/ MAX	UNITS		
G115 and G123	$r_{DS(ON)}$	125	125	150	Max	Ω	V_{BD} = 0, V_{GD} = −30V	I_S = 1 mA
		250	250	300			V_{BD} = +10V, V_{GD} = −20V	
		500	500	600			V_{BD} = +20V, V_{GD} = −10V	
	$I_{D(OFF)}$		−10	−500	Max	nA	V_{DS} = −20V, V_{BS} = V_{GS} = V_{PS} = 0	
	$I_{S(OFF)}$		−5	−100	Max	nA	V_{SD} = −20V, V_{BD} = V_{GD} = V_{PD} = 0	
	I_{GBS}		−5	−100	Max	nA	V_{GB} = −20V, V_{DB} = V_{SB} = V_{PB} = 0	
	$I_{G(ON)}$		−0.8		Min	mA	V_{GB} = −30V, V_{PB} = −30V, V_{DB} = 0	
			−2.4		Max			
	$V_{GS(th)}$	−2	−2	−2	Min	V	I_S = −10 μA, V_{DG} = 0, V_{BS} = V_{PS} = 0	
		−6	−6	−6	Max			
	BV_{DSS}	−25	−25	−25	Min	V	I_D = −10 μA, V_{GB} = V_{BS} = V_{PS} = 0	
	BV_{SDS}	−25	−25	−25	Min	V	I_S = −10 μA, V_{GD} = V_{BD} = V_{PD} = 0	
	BV_{GBS}	−35	−35	−35	Min	V	I_G = −10 μA, V_{DB} = V_{SB} = V_{PB} = 0	
		−90	−90	−90	Max	V		
	BV_{PBS}	−35	−35	−35	Min	V	I_P = −10 μA, V_{DB} = V_{SB} = V_{GB} = 0	
		−90	−90	−90	Max	V		
	C_{GS}, C_{GD}		3(TYP)		Typ	pF	V_{GB} = 0, V_{SB} = 0, V_{DB} = 0, V_{PB} = 0 f = 1 mHz, Body Guarded	
	C_{DS}		0.4(TYP)		Typ	pF		
G115	C_{DB}		18 (TYP)		Typ	pF	V_{DB} = −5V, V_{SB} = V_{GB} = V_{PB} = 0 f = 1 MHz	
G123			9 (TYP)		Typ	pF		
Both	C_{SB}		3.5(TYP)		Typ	pF	V_{SB} = −5V, V_{DB} = 0, V_{GB} = V_{PB} = 0 f = 1 MHz	

3

APPLICATION TIPS

Description of Analog Switch

Single Channel

G-Terminal – This is the control terminal of the switch. The voltage at this terminal determines the conduction state of Q_2. To insure conduction of Q_2 when voltages between ±10V are switched, the gate voltage (V_G) should be at least 10V more negative than the most negative voltage to be switched (–10V). Therefore, V_G should go to –20V. To insure turn-off V_G should not be less than the most positive voltage to be switched, +10V. For convenience the same potential as the body could be used.

B-Terminal – This terminal is connected to the body (substrate) of the chip and must be maintained at a voltage that is equal to or greater than the most positive voltage to be switched. This is to insure that the drain-to-body or the source-to-body junctions do not become forward biased.

P-Terminal – The potential, with respect to the body, at this terminal determines the gate-to-source voltage of Q_1 which determines the amount of drain current available for driver-collector pull-up. Shorting terminal P to B prevents Q_1 and Q_3 from conducting, but still allows the body-to-drain junction of Q_1 to act as a forward biased diode for positive gate voltages, and to act as a Zener diode for negative voltages which exceed BV_{DSS} (–30 to –90V) for protecting the gate of Q_2.

D-Terminal – The common point of the MOS-FET switches (summing point).

S-Terminal – This is the normally-open terminal of the MOS-FET switch and is normally used as the input.

3

APPLICATIONS

6-Channel Multiplexer

Dual Current-to-Voltage Converter With Range Programming

TYPICAL CHARACTERISTICS

PACKAGE OUTLINES

G115

16-Pin Ceramic Dual-In-Line Package

NOTES: 1. Index to be visible from bottom and/or top.

2. Installed position of lead centers.

3. All dimensions in inches.

Flat Package

G123

NOTE: All dimensions in inches.

FD Package

TO-86

Ceramic Dual-In-Line Package

G123

NOTE: All dimensions in inches

DD Package

TO-116

INTERSIL

G116 — G119
5 and 6-Channel MOS-FET Switches
Military Series −55°C to +125°C

FEATURES

- P-Channel Enhancement-type MOS-FET Switches
- Zener Protection on All Gates
- With and Without Constant Current Source Pull-up

GENERAL DESCRIPTION

These switches may be connected directly to the INTERSIL switch-driver D123 series without need of any interfacing components. These MOS-FET switches are internally protected by a Zener diode integrated on the silicon chip. A MOS-FET used as a current source provides an active pull-up for faster switching. The active pull-up FET can be disabled without sacrificing the Zener protection of the gates.

ABSOLUTE MAXIMUM RATINGS (25°C)

Source Current (I_S)	100 mA
Drain Current (I_D)	100 mA
Control Gate Current I_G	5 mA
Pull-Up Gate Current I_P	100 μA
Body Voltage (V_B) to Any Terminal	−2 to +30V
Power Dissipation (Note)	750 mW
Storage Temperature	−55°C to +150°C
Operating Temperature	−50°C to +125°C
Lead Temperature (soldering, 10 sec.)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10 mW/°C.

G116

G117

G118

G119

ORDERING INFORMATION

G 116 M FD

- FD — Package: FD – 14 pin Flat Package; DD – 14 pin Hermetic DIP
- M — Temperature Range: M – Military (−55°C to +125°C); I – Industrial (−20°C to +85°C); C – Commercial (0°C to +70°C)
- 116 — Device Chip Type
- G — Analog Switch

3

ELECTRICAL CHARACTERISTICS (per channel unless noted)

References to pull-up gate P do not apply to G118.

PARAMETER	LIMITS G116M Series 25°C	G116M Series 125°C	G116C Series 25°C	G116C Series 125°C	MIN/MAX	UNITS	CONDITIONS	
$r_{DS(ON)}$ (Note 1)	100	125	125		Max	Ω	$V_{BD} = 0, V_{GD} = -30V, V_{PB} = 0$	$I_S = -1mA$
	200	250	250				$V_{BD} = +10V, V_{GD} = -20V, V_{PB} = 0$	
	450	600	600				$V_{BD} = +20V, V_{GD} = -10V, V_{PB} = 0$	
$I_{S(OFF)}$	-0.5	-500	-1		Max	nA	$V_{SD} = -20V, V_{BD} = V_{GD} = V_{PD} = 0$	
$I_{D(OFF)}$	-2.5	-2500	-5		Max	nA	$V_{DS} = -20V$	G116
	-3.0	-3000	-6				$V_{BD} = V_{GD} = V_{PD} = 0$	G118
	-1.5	-1500	-3					G119
	-0.5	-500	-1		Max	nA	V_{G1B} to $V_{G5B} = 0, V_{G6B} = -30V$, $V_{DB} = -20V, V_{SB} = V_{PB} = 0$	G117
BV_{DSS}	-30		-30		Min	V	$I_D = -10\ \mu A, V_{GS} = V_{BS} = V_{PS} = 0$	
BV_{SDS}	-30		-30		Min		$I_S = -10\ \mu A, V_{GD} = V_{BD} = V_{PD} = 0$	
BV_{GBS}	-30		-30		Min		$I_G = -10\ \mu A, V_{PB} = V_{SB} = V_{DB} = 0$	
	-90		-90		Max			
BV_{PBS}	-30		-30		Min		$I_P = -10\ \mu A, V_{GB} = V_{SB} = V_{DB} = 0$	
	-90		-90		Max			
$V_{GD(th)}$	-2		-2		Min		$I_S = -10\ \mu A, V_{DS} = -10V, V_{SB} = 0$	
	-6		-6		Max			
$I_{G(ON)}$ (Note 2)	-0.5		-0.3		Min	mA	$V_{GB} = -30V, V_{PB} = -30V, V_{SB} = V_{DB} = 0$	
	-2		-2.5		Max			
I_{GSS}	-0.5	-500	-1		Max	nA	$V_{GB} = -20V, V_{DS} = V_{BS} = V_{PS} = 0$	
C_{GD} or C_{GS}	3		3		Max	pF	$V_{PB} = 0, V_{BS} = 0$, or $V_{BD} = 0$	
C_{SD}	0.4		0.4		Max	pF	Body Guarded, f = 1 mHz	
C_{SB}	3.5		3.5		Max	pF	$V_{PB} = V_{GB} = V_{DB} = 0, V_{SB} = -5V$, f = 1 mHz	
C_{DB}	18		18		Max	pF	$V_{PB} = V_{GB} = V_{SB} = 0$, $V_{DB} = -5V$, f = 1 mHz	G116
	18		18					G118
	10		10					G119
	20		20		Max	pF	$V_{G6B} = -30V, V_{PB} = V_{SB} = 0$, V_{G1B} to $V_{G5B} = 0, V_{DB} = -5V$, f = 1 mHz	G117

NOTE 1: For the G117 this is the resistance from each of the source terminals (5 terminals) and the one drain terminal to the internal junction of the output MOS-FETs.

NOTE 2: Not applicable to G118.

3

APPLICATION TIPS

Description of Analog Switch

Single Channel

G-Terminal – This is the control terminal of the switch; the voltage at this terminal determines the conduction state of Q_2. To insure conduction of Q_2 when voltages between ±10V are switched, the gate voltage (V_G) should be at least 10V more negative than the most negative voltage to be switched (–10V). Therefore, V_G should go to –20V. To insure turn-off V_G should not be less than the most positive voltage to be switched, +10V. For convenience the same potential as the body could be used.

B-Terminal – This terminal is connected to the body (substrate) of the chip and must be maintained at a voltage that is equal to or greater than the most positive voltage to be switched. This is to insure that the drain-to-body or the source-to-body junctions do not become forward biased.

P-Terminal – The potential, with respect to the body, at this terminal determines the gate-to-source voltage of Q_1 which determines the amount of drain current available for driver-collector pull-up. Shorting terminal P to B prevents Q_1 and Q_3 from conducting, but still allows the body-to-drain junction of Q_1 to act as a forward biased diode for positive gate voltages, and to act as a Zener diode for negative voltages which exceed BV_{DSS} (–30 to –90V) for protecting the gate of Q_2.

D-Terminal – The common point of the MOS-FET switches (summing point).

S-Terminal – This is the normally-open terminal of the MOS-FET switch and is normally used as the input.

3

APPLICATIONS

5-Channel Multiplexer With Series Switch

3-Channel Differential Multiplexer

TYPICAL CHARACTERISTICS

PACKAGE OUTLINES

Flat Package

NOTE: All dimensions in inches.

FD Package

TO-86

Ceramic Dual-In-Line Package

DD Package

TO-116

INTERSIL

G125 — G132
G1330/40/50/60
4-Channel Junction FET Switches

FEATURES

- $r_{DS(ON)} < 10$ ohms: G1340 and G1360
- $I_{D(OFF)} < 50$ pA: G125, G126, G129 and G130
- C_{DG}, $C_{SG} < 2$ pF: G125, G126, G129 and G130

GENERAL DESCRIPTION

These switches consist of four N-Channel Junction FETS in a single package. In the G129, G130, G131, G132, G1350 and G1360 the drains are common to assist the designer in applications such as multiplexing.

ABSOLUTE MAXIMUM RATINGS

Gate-Drain or Gate-Source Voltage	-40V
Gate Current	50 mA
Total Device Dissipation Free Air (Note)	500 mW
Storage Temperature Range	-65 to +150°C
Operating Temperature	-65 to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 75°C. For higher temperatures, derate the device at the rate of 6.7 mW/°C.

ELECTRICAL CHARACTERISTICS per channel (25°C unless otherwise noted)

CHARACTERISTIC		TEST CONDITIONS		G125 G129	G126 G130	G127 G131	G128 G132	G1330 G1350	G1340 G1360	UNIT	LIMIT
I_{GSS}	Gate Reverse Current	V_{GS} = -20V, V_{DS} = 0	25°C	-0.1	-0.1	-0.2	-0.2	-5.0	-5.0	nA	Max
			125°C	-0.1	-0.1	-0.2	-0.2	-5.0	-5.0	μA	
BV_{GSS}	Gate-Source Breakdown Voltage	I_G = -1 μA, V_{DS} = 0		-40	-40	-40	-40	-30	-30	V	Min
V_P	Gate-Source Pinch-Off Voltage	V_{DS} = 10V, I_D = 0.1 μA		-5	-10	-5	-10	-5	-10	V	Max
$I_{D(OFF)}$	Drain Cutoff Current	V_{DS} = 10V, V_{GS} = -10V	25°C	0.05	0.05	0.1	0.1	0.5	0.5	nA	Max
			125°C	0.05	0.05	0.1	0.1	0.5	0.5	μA	
$I_{S(OFF)}$	Source Cutoff Current	V_{SD} = 10V, V_{GD} = -10V	25°C	0.05	0.05	0.1	0.1	0.5	0.5	nA	Max
			125°C	0.05	0.05	0.1	0.1	0.5	0.5	μA	
I_{DSS}	Drain Current at Zero Gate Voltage	V_{DS} = 10V, V_{GS} = 0 (Pulsed)		0.5	2	5	10	15	30	mA	Min
r_{DS}	Drain-Source ON Resistance	V_{GS} = 0, I_D = 0, f = 1 kHz		500	250	90	45	20	10	Ω	Max
$C_{DG} + C_{SG}$	Gate-Source plus Gate-Drain ON Capacitance	V_{GS} = 0, V_{DS} = 0, f = 1 MHz		10	10	40	40	300	300	pF	Max
C_{DG}	Drain-Gate OFF Capacitance	V_{GS} = -10V, V_{DS} = 0, f = 1 MHz		2	2	7	7	16	16	pF	Max
C_{SG}	Source-Gate OFF Capacitance			2	2	7	7	16	16	pF	Max

3

PRODUCT CONDITIONING

The following processes are performed 100% in accordance with MIL-STD-883.

Precap Visual—Meth. 2010, Cond. B
Stabilization Bake—Meth. 1008
Temp. Cycle—Meth. 1010
Centrifuge—Meth, 2001, Cond. D
Hermeticity—Meth. 1014, Cond. A, C
(Leak Rate $< 5 \times 10^{-8}$ atm cc/s)

TYPICAL CHARACTERISTICS

APPLICATION

4-Channel Commutator Circuit

INPUT RANGE: -10 to +10V
GATE: LOGIC "1" FOR SWITCH ON
LOGIC "0" FOR SWITCH OFF

PACKAGE OUTLINE

Flat Package

NOTE: All dimensions in inches.

FD Package

ORDERING INFORMATION

G 125 I FD

- FD — Package: FD — 14 Pin Flat Pack ¼" x ¼"
- I — Temperature Range: M — -55°C to +125°C; I — -20°C to +85°C
- 125 — Device Chip Type
- G — Analog Switch

INTERSIL

MM450/MM550, MM451/MM551 MM452/MM552, MM455/MM555 MOS-FET Switches

FEATURES

- Large Analog Input—±10V
- Low Supply Voltage—V_{BULK} = +10V
  V_{GG} = -20V
- Typical ON Resistance—V_{IN} = -10V, 150Ω
  V_{IN} = +10V, 75Ω
- Low Leakage Current—200 pA @ 25°C
- Input Gate Protection

GENERAL DESCRIPTION

The MM450, and MM550 series each contain p channel MOS enhancement mode transistors. These devices are useful in airborne and ground support systems requiring multiplexing, analog transmission, and numerous signal routing applications. The use of low threshold transistors (V_{TH} = 2 volts) permits operations with large analog input swings (±10 volts) at low gate voltages (-20 volts).

Each gate input is protected from static charge build-up by the incorporation of zener diode protective devices connected between the gate input and device bulk.

ABSOLUTE MAXIMUM RATINGS (Note 1)

Gate Voltage (V_{GG})	+14.5V to -30V
Bulk Voltage (V_{BULK})	+14V
Analog Input (V_{IN})	+14V to -20V
Power Dissipation	200 mW
Operating Temperature	
MM450, MM451, MM452, MM455	-55°C to +125°C
MM550, MM551, MM552, MM555	-25°C to 70°C
Storage Temperature	-65°C to +150°C
Lead Tempertature (soldering, 10 sec.)	300°C

NOTE 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10 mW/°C for FD package and 6.5 mW/°C for TW package.

CONNECTION DIAGRAMS

MM450, MM550 Dual Differential Switch

TW Package

MM451, MM551 Four Channel Switch

TW Package

MM452, MM552 Four MOS Transistor Package

FD Package

MM455, MM555 Three MOS Transistor Package

TW Package

ORDERING INFORMATION

PACKAGE DIMENSIONS

Flat Package

FD Package

10 Lead Metal Can Package

TW Package

3

ELECTRICAL CHARACTERISTICS (per channel unless noted)

SYMBOL	CHARACTERISTICS	TYPE	LIMITS 25°	70°	85°	125°	MIN/MAX	UNITS	CONDITIONS
V_{IN}	Analog Input Voltage	All	±10				Max	V	
$V_{GS(TH)}$	Threshold Voltage	All	1.5				Min	V	$V_{DG} = 0$, $I_D = 10\,\mu A$
			3.0				Max		
$r_{DS(ON)}$	Drain-Source On Resistance	All	600		600		Max	Ω	$V_{IN} = -10V$; $I_D = 1$ mA, $V_B = 10V$, $V_{GS} = -20V$
			200		200		Max	Ω	$V_{IN} = +10V$
I_{GBS}	Gate Leakage Current	All	5			100	Max	nA	$V_{GS} = -25V$, $V_{BS} = V_{DS} = 0$
$I_{D(OFF)}$	Drain Leakage Current	MM450, MM451 MM452, MM455	0.2		40	200	Max	nA	$V_{DB} = -25V$, $V_{GB} = V_{SB} = 0$
		MM550, MM551 MM552, MM555	20	100			Max	nA	
$I_{S(OFF)}$	Source Leakage Current	MM450, MM451 MM452, MM455	0.4		40	400	Max	nA	$V_{SB} = -25V$, $V_{DB} = V_{GB} = 0$
		MM550, MM551 MM552, MM555		100			Max	nA	
C_{DB}	Drain-Body Capacitance	All	10				pF	Max	$V_{DB} = V_{GB} = V_{SB} = 0$, f = 1 MHz
C_{SB}	Source-Body Capacitance	MM450, MM550	14				pF	Max	
		MM451, MM551	24				pF	Max	
		MM452, MM552	11				pF	Max	
		MM455, MM555	11				pF	Max	
C_{GB}	Gate-Body Capacitance	MM450, MM550	13				pF	Max	
		MM451, MM551	8				pF	Max	
		MM452, MM552	9				pF	Max	
		MM455, MM555	9				pF	Max	
C_{GS}	Gate-Source Capacitance	All	5				pF	Max	

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TYPICAL PERFORMANCE CURVES

INTERSIL

IH6201
Dual CMOS Driver/ Voltage Translator

FEATURES

- **Driven direct from TTL or CMOS logic**
- **Translates logic levels up to 30V levels**
- **Switches 20V$_{ACPP}$ signals when used in conjunction with Intersil IH401A Varafet (as an analog gate)**
- **$t_{ON} \leq$ 300nS & $t_{OFF} \leq$ 200nS for 30V level shifts**
- **Quiescent supply current $\leq$ 100μa for any state (d.c.)**
- **Provides both normal & inverted outputs**

GENERAL DESCRIPTION

The IH6201 is a CMOS, Monolithic, Dual Voltage Translator; it takes the low level TTL or CMOS logic level and converts them to higher levels (i.e. to ±15V swings). This translator is typically used in making solid state switches, or analog gates.

When used in conjunction with the Intersil IH401 family Varafets, the combination makes a complete solid state switch capable of switching signals up to 22Vpp and up to 20MHz in frequency. This switch is a "break-before-make" type (i.e. t_{off} time < t_{on} time). The combination has typical t_{off} ≈ 80nS and typ. t_{on} ≈ 200nS for signals up to 20Vpp in amplitude.

A TTL "1" input strobe will force the θ driver output up to V^+ level; the $\bar{\theta}$ output will be driven down to the V^- level. When the TTL input goes to "0", the θ output goes to V^- and $\bar{\theta}$ goes to V^+; thus θ and $\bar{\theta}$ are 180° out of phase with each other. These complementary outputs can be used to create a wide variety of functions such as SPDT and DPDT switches, etc.; alternatively the complementary outputs can be used to drive an N and P channel Mosfet, to make a complete Mosfet analog gate.

The driver typically uses +5V and ±15V power supplies; however a wide range of V^+ and V^- is possible, however V^+ > 5V is necessary for the driver to work properly.

BLOCK DIAGRAM

PIN CONFIGURATION

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE
IH6201CDE	0°C to 70°C
IH6201MDE	-55°C → +125°C
IH6201CJE	0°C to 70°C
IH6201MJE	-55°C to 125°C
IH6201CPE	0°C to 70°C

SCHEMATIC DIAGRAM (ONE CHANNEL)

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ABSOLUTE MAXIMUM RATINGS

V^+ to V^- 35V
V^+ 35V
V^- 35V
V^+ to V_{IN} 40V

Operating Temperature ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (Soldering 10 sec) ..... 300°C

ELECTRICAL SPECIFICATIONS $V^+ = +15V$, $V^- = -15V$, $V_L = +5V$, $V_R = 0V$

ITEM	CONDITIONS	IH6201CDE			IH6201MDE			UNITS
		−25°C	+25°C	+85°C	−55°C	+25°C	+125°C	
θ or $\bar{\theta}$ driver output swing	$V_{IN}=0V$ +3V fig. 2B	28	28	28	28	28	28	Vpp
V_{IN} strobe level ("1") for proper translation	$\theta \geq 14V$ $\bar{\theta} \geq -14V$	3.0	3.0	3.0	2.4	2.4	2.4	$V_{D.C.}$
V_{IN} strobe level ("0") for proper translation	$\theta \geq -14V$ $\bar{\theta} \geq 14V$	0.4	0.4	0.4	0.8	0.8	0.8	$V_{D.C.}$
I_{IN} input strobe current draw (for 0V → 5V range)	$V_{IN} = 0V$ or +5V	1	1	1	1	1	1	μA
t_{ON} time	$V_{IN}=0V$ 3V 4μs $C_L = 30pf$ switching turn-on time fig. 2B	400	400	400	300	300	300	nS
t_{OFF} time	$V_{IN}=0V$ +3V 4μs $C_L = 30pf$ switching turn-off time fig. 2B	300	300	300	200	200	200	nS
I^+ (V+) power supply quiescent current	$V_{IN} = 0V$ or +5V	100	100	100	100	100	100	μA
I^- (V−) power supply quiescent current	$V_{IN} = 0V$ or +5V	100	100	100	100	100	100	μA
I_L (V_L) power supply quiescent current	$V_{IN} = 0V$ or +5V	100	100	100	100	100	100	μA

3

APPLICATIONS

I. INPUT DRIVE CAPABILITY

The strobe input lines are designed to be driven from TTL logic levels; this means 0.8V → 2.4V levels max. and min. respectively. For those users who require 0.8V to 2.0V operation, a pull-up resistor is recommended from the TTL output to +5V line. This resistor is not critical and can be in the 1kΩ to 10kΩ range.

When using 4000 series CMOS logic, the input strobe is connected direct to the 4000 series gate output and no pull up resistors, or any other interface, is necessary.

When the input strobe voltage level goes below Gnd (i.e. to −15V) circuit is unaffected as long as V^+ to V_{IN} does not exceed absolute maximum rating.

II. OUTPUT DRIVE CAPABILITY

The translator output is designed to drive the Intersil IH401 family of Varafets; these are N-channel J-FETS with built-in driver diodes. Driver diodes are necessary to isolate the signal source from the driver/translator output; this prevents forward biasing between the signal input and the $+V_{CC}$ supply. The IH6201 will drive any J-FET provided some sort of isolation is added i.e.

Figure 1

You will notice in Figure 1 that a "referral" resistor has been added from 2N4391 gate to its source. This resistor is needed to compensate for inadequate charge area curve for isolation diode (i.e. if C vs. V plot for diode ≤ 2 [C vs. V plot for output J-FET] switch won't function; then adding this resistor overcomes this condition. The "referral" resistor is normally in the 100kΩ to 1MΩ range and is not too critical.

III. MAKING A COMPLETE SOLID STATE SWITCH THAT CAN HANDLE 20Vpp SIGNALS

The limitation on signal handling capability comes from the output gating device. When a J-FET is used, it's the pinch-off of the J-FET acting with the V^- supply that does the

APPLICATIONS, CONTINUED

limiting. In fact max. signal handling capability = 2 (Vp + (V^-)) Vpp where Vp = pinch-off voltage of J-FET chosen. i.e. Vp = 7V, V^- = −15V ∴ max. signal handling = 2 (7V + (−15V)) Vpp = 2(7V−15)pp=2(−8Vpp)=16Vpp. Obviously to get ≥ 20Vpp, Vp ≥ 5V with V^- = −15V. Another simple way to get 20Vpp with Vp = 7V, is to increase V^- to −17V. In fact using V^+ = +12V or +15V and setting V^- = −18V allows one to switch 20Vpp with any member of IH401 family. The advantage of using the Vp = 7V pinch-off (along with unsymmetrical supplies) over the Vp = 5V pinch-off (and ±15V supplies) is that you will have a much lower $R_{DS(ON)}$ resistance for the Vp = 7V fet.(i.e. for the 2N4391 fet $R_{DS(ON)} \approx 22\Omega$, $R_{DS(ON)} \approx 35\Omega$)
Vp = 7V Vp = 5V

The IH6201 is a dual translator, each containing 4 CMOS FETs. The schematic of one-half IH6201, driving one-fourth of an IH401, is shown in Figure 2A.

Figure 2A

Figure 2B

NOTE: Each translator output has a θ and $\bar{\theta}$ output. θ is just the inverse of $\bar{\theta}$.

A very useful feature of this system is that one-half of an IH6201 and one-half of an IH401 can combine to make a SPDT switch, or an IH6201 plus an IH401 can make a dual SPDT analog switch. (See III.)

I. Dual SPST Analog Switch

II. DPDT Analog Switch

NOTE: Either switch is turned on when strobe input goes high.

APPLICATIONS, CONTINUED

III. Dual SPDT

IV. Dual DPST

PACKAGE DIMENSIONS

16 Pin Ceramic Dual-In-Line Package (DE)

16 Pin Plastic Dual-In-Line Package (PE)

16-Pin CERDIP (JE)

Data Acquisition

A/D Converters

ICL7104/8052A/8068 4-4
ICL7109 4-20
ICL8052/3 4-36
LD110/111/114 4-45

D/A Converters

AD7520/21/30/31 4-51
AD7523 4-57
AD7533 4-61
AD7541 4-65
ICL7112 4-71
ICL7113 4-77

DVM Circuits

ICL7101/8052 4-81
ICL7103/8052 4-89
ICL7103/8068 4-97
ICL7106/7 4-105
ICL7116/7 4-115

Successive Approximation Registers

AM2502/3/4 4-123

Switches; Current Switches for D/A

ICL8018/19/20 4-129

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Integrating Analog-to-Digital Converters for Display

Maximum Electrical Specification at 25°C unless otherwise noted.

	Single Chip		Two Chip System				
Model	**New ICL7106/ICL7116**	**New ICL7102/ICL7117**	**ICL8052/ ICL8053**	**ICL8052/ ICL7101**	**ICL8068A/ ICL7103B**	**ICL8052A/ ICL7103A**	**LD110/LD114/ LD111-12**
Resolution	±3½ digit	±3½ digit	Depends on counter used	±3½ digit	±4½ digit	±4½ digit	±3½ digit
Accuracy							
Nonlinearity	±1 count	±1 count	±0.002%	±1 count	±1 count	±1 count	±1 count
Zero Input Reading	±0.000	±0.000	±0.0000	±0.000	±0.000	±0.0000	±0.0000
Ratiometric Reading	+1.000.	+1.000.	+1.0000.	+1.000.	+1.000.	+1.0000.	+1.000.
(Ratiometric)	±1 count	±1 count	±1 count	±1 count	±1 count	±1 count	±1 count
Rollover Error	±1 count	±1 count	±1 count	±1 count	±1 count	±1 count	±1 count
Stability							
Offset vs Temperature	1 μV/°C	1 μV/°C	5 μV/°C	5 μV/°C	2 μV/°C	2 μV/°C	—
Gain vs Temperature	5 ppm/°C	5 ppm/°C	15 ppm/°C	15 ppm/°C	5 ppm/°C	5 ppm/°C	—
Conversion Rate	0.1 to 15 conv/sec	0.1 to 15 conv/sec	0.1 to 30 conv/sec	0.1 to 30 conv/sec	0.1 to 30 conv/sec	0.1 to 30 conv/sec	0.3 to 12 conv/sec
Analog Input							
Voltage Range	±200 mV to ±2V	±200 mV to ±2V	±2V	±200 mV to ±2V	±200 mV to ±2V	±2V	±2V
Impedance	$10^{12}\Omega$	$10^{12}\Omega$	$10^{9}\Omega$	$10^{9}\Omega$	$10^{9}\Omega$	$10^{9}\Omega$	$10^{9}\Omega$
Leakage Current	2pA	3pA	30pA	30pA	200pA	10pA	40pA typ
Noise (peak-to-peak)	15μV typ	15μV typ	20μV typ	20μV typ	2μV typ	20μV typ	—
Digital Input	Display Hold	Display Hold					
Digital Outputs							
Format	7 segment LCD display	7 segment LED display	Depends on counter used	Latched Parallel BCD	Multiplex BCD	Multiplex BCD	Multiplex BCD
Logic Level	AC: 4.5V down from V+	11. Comm Anode DTL TTL CMOS	Depends on counter used	TTL/CMOS	TTL/CMOS	TTL/CMOS	TTL/CMOS
Power Supply							
Voltage	+9V	±5V	±15V; +5V	±15V; +5V	±15V; +5V	±15V; +5V	±15; +5V
Current	1.8mA	1.8mA	12mA	17mA; 25mA	20mA; 30mA	18mA; 30mA	27mA; 24mA
Package	40 pin DIP	40 pin DIP	(2) 14 pin DIP	16 pin DIP 40 pin DIP	16 pin DIP 24 pin DIP	16 pin DIP 24 pin DIP	(2) 16 pin DIP

Integrating Analog-to-Digital Converters for Data Acquisition

4

Maximum Electrical Specifications at +25°C unless otherwise noted

Type	Single-Chip	Two-Chip						
Model	**New ICL7109**	**ICL8068/ ICL7104-12**	**ICL8068/ ICL7104-14**	**ICL8068/ ICL7104-16**	**ICL8052/ ICL7101**	**ICL8068A/ ICL7103B**	**ICL8052A/ ICL7103A**	**ICL8052/ ICL8053**
Resolution	±12-Bit Binary	±12-Bit Binary	±14-Bit Binary	±16-Bit Binary	3½-Digit BCD	4½-Digit BCD	4½-Digit BCD	±12-Bit Binary
μP Compatible	yes	yes	yes	yes	yes	yes	yes	yes
Output	Programmable: 1. Latched parallel 3 state Binary 2. Controlled 2-8 bit byte	Programmable: 1. Latched parallel 3 state binary 2. Controlled 3 2-8 Bit byte for ICL7104-12/14, 3-8 bit byte for ICL7104-16			Latched parallel BCD	Multiplexed BCD	Multiplexed BCD	Interface to MOS, TTL, μP
Control Lines	Start/Convert, Busy, Byte Enable, Mode, Load, Send Enable, Out of Range				Start/Convert. Busy, Out of Range	Start/Convert, Busy, Strobe Out of Range Underrange	Start/Convert Busy, Strobe Out of Range Underrange	Auto-zero, Signal Interpret Two Reference, Integrate, and Comparator Output
UART Compatible	yes	yes	yes	yes	no	yes	yes	no

Digital-to-Analog Converters*

Maximum Electrical Specifications at +25°C unless otherwise noted

Model	New AD7523	New AD7533	AD7520 (7530)	New ICL7113	AD7521 (7531)	New AD7541	New ICL7112
Resolution	8 bit	10 bit	10 bit	3 digit	12 bit	12 bit	12 bit
Accuracy	J/K/L	J/K/L	J/K/L	B/A	J/K/L	J/K/L	J/K
Linearity	0.2%/0.1%/0.05%	0.2%/0.1%/0.05%	0.2%/0.1%/0.05%	0.2%/0.05%	0.2%/0.1%/0.05%	0.02%/0.01%/0.01%	0.02%/0.01%
Zero Offset	50 μA	200 nA	200 nA (300 nA)	200 nA	200 nA (300 nA)	50 nA	200 nA
Full Scale Reading	1.5% max	1.4%	0.3% typ	0.3% typ	0.3% typ	0.3%	0.3%
Stability							
Gain vs. Temp	10 ppm/°C	10 ppm/°C	10 ppm/°C	10 ppm-°C	10 ppm/°C	10 ppm/°C	5 ppm/°C
Linearity vs. Temp	2 ppm/°C	2 ppm/°C	2 ppm/°C	2 ppm/°C	2 ppm/°C	0.2 ppm/°C	0.2 ppm/°C
Setting Time to ±0.05% F.S.	150 ns	600 ns typ	500 ns typ	500 ns typ	500 ns typ	1 μs	500 ns typ
Input Code	DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS	DTL/TTL/CMOS
Logic Compatibility option	Binary Offset Binary	Binary Offset Binary	Binary Offset Binary	BCD	Binary Offset Binary	Binary Offset Binary	Binary Offset Binary
Power Supply							
Voltage	+5 to +16V	+5 to +15V	+5 to +15V	+5 to +15V	+5 to +15V	+5 to +16V	+5 to +15V
Current	100 μA	2 mA	2 mA	2 mA	2 mA	2 mA	2 mA
Package	16 pin DIP	16 pin DIP	16 pin DIP	18 pin DIP	18 pin DIP	18 pin DIP	18 pin DIP

*R2R Ladder Multiplying Type

Successive Approximation Registers AM2502/2503/2504

8 (2502/2503) and 12 bit (2504) successive approximation registers can be used as serial to parallel counter or ring counter. Contains storage and control for SAR A to D converters.

Quad Current Switches ICL8018/8019/8020

High speed precision current switches for use in current summing D/A converters. Can be purchased individually or in matched sets with accuracies of 0.01% (ICL8018), 0.1% (ICL8019), or 1.0% (ICL8020)

4

INTERSIL

ICL8052/ICL7104 Pair
ICL8068/ICL7104 Pair
16/14/12 Bit Binary A/D Converters for μProcessors

FEATURES

- 16 bit binary three-state latched outputs plus polarity and overrange. Also 14 and 12 bit versions.
- Ideally suited for interface to UARTs, microprocessors, or other complex circuitry.
- Conversion on demand or continuously.
- Handshake byte-serial transmission synchronously or on demand.
- Guaranteed zero reading for zero volts input.
- True polarity at zero count for precise null detection.
- Single reference voltage for true ratiometric operation.
- Onboard clock and reference.
- Auto-Zero; Auto-Polarity
- Accuracy guaranteed to 1 count.
- All outputs TTL compatible.
- ±10V analog input range
- Status signal available for external sync, A/Z in preamp, etc.

GENERAL DESCRIPTION

The ICL7104, combined with the ICL8052 or ICL8068, forms a member of Intersil's high performance A/D converter family. The 16-bit version, the ICL7104-16, performs the analog switching and digital function for a 16-bit binary A/D converter, with full three-state output, UART handshake capability, and other outputs for a wide range of output interfacing. The ICL7014-14 and ICL7104-12 are 14 and 12-bit versions. The analog section, as with all Intersil's integrating converters, provides fully precise Auto-Zero, Auto-Polarity (including ±0 null indication), single reference operation, very high input impedance, true input integration over a constant period for maximum EMI rejection, fully ratiometric operation, over-range indication, and a medium quality built-in reference. The chip pair also offers optional input buffer gain for high sensitivity applications, a built-in clock oscillator, and output signals for providing an external Auto-Zero capability in preconditioning circuitry, synchronizing external multiplexers, etc. The basic schematic connections are shown in Figure 1.

Figure 1: 8052A (8068A)/7104 16/14/12 Bit A/D Converter Functional Block Diagram

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
8052	0°C to 70°C	14 pin plastic DIP	ICL8052CPD
8052	0°C to 70°C	14 pin ceramic DIP	ICL8052CDD
8052A	0°C to 70°C	14 pin plastic DIP	ICL8052ACPD
8052A	0°C to 70°C	14 pin ceramic DIP	ICL8052ACDD
8068	0°C to 70°C	14 pin plastic DIP	ICL8068CJD
8068A	0°C to 70°C	14 pin plastic DIP	ICL8068ACJD

Part	Temp. Range	Package	Order Number
7104 12 bit	0°C to 70°C	40 pin plastic DIP	ICL7104-12 CPL
7104 12 bit	0°C to 70°C	40 pin ceramic DIP	ICL7104-12 CDL
7104 14 bit	0°C to 70°C	40 pin plastic DIP	ICL7104-14 CPL
7104 14 bit	0°C to 70°C	40 pin ceramic DIP	ICL7104-14 CDL
7104 16 bit	0°C to 70°C	40 pin plastic DIP	ICL7104-16 CPL
7104 16 bit	0°C to 70°C	40 pin ceramic DIP	ICL7104-16 CDL

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 500 mW
Storage Temperature ..... −65°C to +150°C

8052, 8068

Supply Voltage ..... ±18V
Differential Input Voltage(8068) ..... ±30V
(8052) ..... ±6V
Input Voltage (Note 2) ..... ±15V
Output Short Circuit Duration,
All Outputs (Note 3) ..... Indefinite
Operating Temperature ..... 0°C to +70°C
Lead Temperature (Soldering, 60 Sec.)

7104

V+ Supply (GND to V+) 12
V++ to V− 32
Positive Supply Voltage (GND to V++) 17
Negative Supply Voltage (GND to V−) 17
Analog Input Voltage (Pin 32-39) (Note 4) ..... V+ to V−
Digital Input Voltage ..... V+ +0.3V
(Pins 2-30) (Note 5) ..... GND −0.3V

Note 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.
Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
Note 3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.
Note 4: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.
Note 5: Connecting any digital inputs or outputs to voltages greater than V+ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources not on the same power supply be applied to the ICL7104 before its power supply is established.

*COMMENT: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent damage to the devices. This is a stress rating only and functional operation of the devices at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

7104 ELECTRICAL CHARACTERISTICS (V+ = +5V, V++ = +15V, V− = −15V, Ta = 25°C)

CHARACTERISTICS		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Clock Input	CLOCK 1	I_{IN}	Vin = +5V to 0V	±2	±7	±30	μA
Comparator I/P	COMP IN (Note 1)	I_{IN}	Vin = 0V to +5V	−10	±0.001	+10	μA
Inputs with Pulldown	MODE	I_{IH}	Vin = +5V	+1	+5	+30	μA
		I_{IL}	Vin = 0V	−10	±0.01	+10	μA
Inputs with Pullups	SEN, R/$\overline{H}$	I_{IH}	Vin = +5V	−10	±0.01	+10	μA
	$\overline{LBEN}$, $\overline{MBEN}$, $\overline{HBEN}$, $\overline{CE/LD}$ (Note 2)	I_{IL}	Vin = 0V	−30	−5	−1	μA
Input High Voltage	All Digital Inputs	V_{IH}		2.5	2.0	—	V
Input Low Voltage	All Digital Inputs	V_{IL}			1.5	1.0	V
Digital Outputs Three-Stated On	$\overline{LB}$ $\overline{EN}$, $\overline{MB}$ $\overline{EN}$ (16 only), $\overline{HB}$ $\overline{EN}$, $\overline{CE/LD}$ (Note 3)	V_{OL}	I_{OL} = 1.6 mA	—	.27	.4	V
		V_{OH}	I_{OH} = −10μA		4.5	—	V
		V_{OH}	I_{OH} = −240μA	2.4	3.5	—	V
	BIT n, POL, OR						
Digital Outputs Three-Stated Off	BIT n, POL, OR	I_{LO}	0 ≤ Vout ≤ V+	−10	±.001	+10	μA
Non-Three-State Digital Output	STTS	V_{OL}	I_{OL} = 3.2 mA	—	.3	.4	V
		V_{OH}	I_{OH} = −400μA	2.4	3.3	—	V
	CLOCK 2	V_{OL}	I_{OL} = 320μA		0.5		V
		V_{OH}	I_{OH} = −320μA		4.5		V
	CLOCK 3 (-12, -14 ONLY)	V_{OL}	I_{OL} = 1.6 mA		.27	.4	V
		V_{OH}	I_{OH} = −320μA	2.4	3.5		V
Switch	Switch 1	$R_{DS}ON$		—	25k		Ω
	Switches 2,3	$R_{DS}ON$		—	4k	20k	Ω
	Switches 4,5,6,7,8,9	$R_{DS}ON$		—	2k	10k	Ω
	Switch Leakage	$I_{D}OFF$		—	15		pA
Clock	Clock Freq. (Note 4)			DC	200	400	kHz
Supply Currents	+5V Supply Current All outputs high impedance	I+	Freq. = 200 kHz		200	600	μA
	+15V Supply Current	I++	Freq. = 200 kHz		.3	1.0	mA
	−15V Supply Current	I−	Freq. = 200 kHz		25	100	μA
Supply Voltage Range	Logic Supply	V+	Note 5	4.0		+11.0	V
	Positive Supply	V++		+10.0		+16.0	V
	Negative Supply	V−		−16.0		−10.0	V

Note 1: This spec applies when not in Auto-Zero phase.
Note 2: These specs apply when these pins are inputs i.e. the mode pin is low, and the 7104 is not in handshake mode.
Note 3: These specs apply when these pins are outputs, i.e. the mode pin is high or the 7104 is in handshake mode.
Note 4: Clock circuit shown in Fig. 12 or 13.
Note 5: V+ must not be more positive than V++.

8068 ELECTRICAL CHARACTERISTICS (V_S = ±15V unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8068 MIN	8068 TYP	8068 MAX	8068A MIN	8068A TYP	8068A MAX	UNITS
EACH OPERATIONAL AMPLIFIER								
Input Offset Voltage	V_{CM} = 0V		20	65		20	65	mV
Input Current (either input) (Note 1)	V_{CM} = 0V		175	250		80	150	pA
Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V_{CM} = ±2V		110			110		
Large Signal Voltage Gain	R_L = 50kΩ	20,000			20,000			V/V
Slew Rate			6			6		V/μs
Unity Gain Bandwidth			2			2		MHz
Output Short-Circuit Current			5	10		5	10	mA
COMPARATOR AMPLIFIER								
Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
Positive Output Voltage Swing		+12	+13		+12	+13		V
Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
VOLTAGE REFERENCE								
Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
Output Resistance			5			5		ohms
Temperature Coefficient			50			40		ppm/°C
Supply Voltage Range		±10		±16	±10		±16	V
Supply Current Total				14		8	14	mA

8052 ELECTRICAL CHARACTERISTICS (V_S = ±15V unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8052 MIN	8052 TYP	8052 MAX	8052A MIN	8052A TYP	8052A MAX	UNITS
EACH OPERATIONAL AMPLIFIER								
Input Offset Voltage	V_{CM} = 0V		20	50		20	50	mV
Input Current (either input) (Note 1)	V_{CM} = 0V		5	50		2	10	pA
Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
Non-Linear Component of Common-Mode Rejection Ratio (Note 2)	V_{CM} = ±2V		110			110		
Large Signal Voltage Gain	R_L = 10kΩ	20,000			20,000			V/V
Slew Rate			6			6		V/μs
Unity Gain Bandwidth			1			1		MHz
Output Short-Circuit Current			20	100		20	100	mA
COMPARATOR AMPLIFIER								
Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
Positive Output Voltage Swing		+12	+13		+12	+13		V
Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
VOLTAGE REFERENCE								
Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
Output Resistance			5			5		ohms
Temperature Coefficient			50			40		ppm/°C
Supply Voltage Range		±10		±16	±10		±16	V
Supply Current Total			6	12		6	12	mA

Note 1: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta jA$ Pd where θjA is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

Note 2: This is the only component that causes error in dual-slope converter.

SYSTEM ELECTRICAL CHARACTERISTICS: 8068/7104

(V_{++} = +15V, V_+ = +5V, V_- = −15V Clock Frequency = 200KHz

CHARACTERISTICS	CONDITIONS	8068A/7104-12			8068A/7104-14			8068A/7104-16			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	V_{in} = 0.0V Full Scale = 4.000V	−.000	±.000	+.000	−0.0000	±0.0000	+0.0000	−0.0000	±0.0000	+0.0000	Hexadecimal Reading
Ratiometric Reading (1)	V_{in} = $V_{Ref.}$ Full Scale = 4.000V	7FF	800	801	1FFF	2000	2001	7FFF	8000	8001	Hexadecimal Reading
Linearity over ± Full Scale (error of reading from best straight line)	$-4V \le V_{in} \le +4V$		0.2	1		0.5	1		0.5	1	LSB
Differential Linearity (difference between worse case step of adjacent counts and ideal step	$-4V \le V_{in} \le +4V$		.01			.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \equiv +V_{in} \approx 4V$		0.2	1		0.5	1		0.5	1	LSB
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 4.000V		3			2			2		μV
Leakage Current at Input (2)	V_{in} = 0V		200	265		100	165		100	165	pA
Zero Reading Drift	V_{in} = 0V 0°C ≤ T_A ≤ 70°C		1	5		0.5	2		0.5	2	μV/°C
Scale Factor Temperature (3) Coefficient	V_{in} = +4V 0 ≤ T_A ≤ 50°C (ext. ref. 0 ppm/°C)		2	5		2	5		2	5	ppm/°C

SYSTEM ELECTRICAL CHARACTERISTICS: 8052/7104

(V_{++} = +15V, V_+ = +5V, V_- = −15V Clock Frequency = 200KHz

CHARACTERISTICS	CONDITIONS	8052/7104-12			8052A/7104-14			8052A/7104-16			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	V_{in} = 0.0V Full Scale = 4.000V	−.000	±.000	+.000	−0.0000	±0.0000	+0.0000	−0.0000	±0.0000	+0.0000	Hexadecimal Reading
Ratiometric Reading (3)	V_{in} = $V_{Ref.}$ Full Scale = 4.000V	7FF	800	801	1FFF	2000	2001	7FFF	8000	8001	Hexadecimal Reading
Linearity over ± Full Scale (error of reading from best straight line)	$-4V \le V_{in} \le +4V$		0.2	1		0.5	1		0.5	1	LSB
Differential Linearity (difference between worse case step of adjacent counts and ideal step)	$-4V \le V_{in} \le +4V$		.01			.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \equiv +V_{in} \approx 4V$		0.2	1		0.5	1		0.5	1	LSB
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 4.000V		20 50			30			30		μV
Leakage Current at Input (2)	V_{in} = 0V		30	80		20	30		20	30	pA
Zero Reading Drift	V_{in} = 0V 0° ≤ T_A ≤ 70°C		1	5		0.5	2		0.5	2	μV/°C
Scale Factor Temperature Coefficient	V_{in} = +4V 0 ≤ T_A ≤ 70°C (ext. ref. 0 ppm/°C)		3	15		2	5		2	5	ppm/°C

Note 1: Tested with low dielectric absorption integrating capacitor.

Note 2: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents are measured with junctions at ambient temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \theta jA\,Pd$ where θjA is the thermal resistance from junction to ambient. A heat sink can be used to reduce temperature rise.

Note 3: The temperature range can be extended to 70°C and beyond if the Auto-Zero and Reference capacitors are increased to absorb the high temperature leakage of the 8068. See note 2 above.

Full 18 Bit Three State Output

Various Combinations of Byte Disables

AC CHARACTERISTICS (V++ = +15V, V+ = +5V, V− = −15V)

Figure 2: Direct Mode Output Timing

TABLE 1: Direct Mode Timing Requirements

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{BEA}	$\overline{XBEN}$ Min. Pulse Width		500		ns
t_{DAB}	Data Access Time from $\overline{XBEN}$		200		ns
t_{DHB}	Data Hold Time from $\overline{XBEN}$		200		ns
t_{CEA}	$\overline{CE/LD}$ Min. Pulse Width		500		ns
t_{DAC}	Data Access Time from $\overline{CE/LD}$		200		ns
t_{DHC}	Data Hold Time from $\overline{CE/LD}$		200		ns

TABLE 2: Handshake Timing Requirements

NAME	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{MW}	MODE Pulse (minimum)		20		ns
t_{SM}	MODE pin set-up time		–150		ns
t_{ME}	MODE pin high to low Z $\overline{CE/LD}$ high delay		200		ns
t_{MB}	MODE pin high to $\overline{XBEN}$ low Z (high) delay		200		ns
t_{CEL}	CLOCK 1 high to $\overline{CE/LD}$ low delay		700		ns
t_{CEH}	CLOCK 1 high to $\overline{CE/LD}$ high delay		600		ns
t_{CBL}	CLOCK 1 high to $\overline{XBEN}$ low delay		900		ns
t_{CBH}	CLOCK 1 high to $\overline{XBEN}$ high delay		700		ns
t_{CDH}	CLOCK 1 high to data enabled delay		1100		ns
t_{CDL}	CLOCK 1 low to data disabled delay		1100		ns
t_{SS}	Send ENable set-up time		–350		ns
t_{CBZ}	CLOCK 1 high to $\overline{XBEN}$ disabled delay		2000		ns
t_{CEZ}	CLOCK 1 high to $\overline{CE/LD}$ disabled delay		2000		ns

FIGURE 3: Timing Relationships In Handshake Mode

PIN ASSIGNMENTS

TABLE 3: Pin Assignment and Function Description

PIN	SYMBOL	OPTION	DESCRIPTION
1	V(++)		Positive Supply Voltage Nominally +15V
2	GND		Digital Ground .0V, ground return
3	STTS		STaTuS output .HI during Integrate and Deintegrate until data is latched .LO when analog section is in Auto-Zero configuration.
4	POL		POLarity. Three-state output. HI for positive input.
5	OR		OverRange. Three-state output.
6	BIT 16 BIT 14 BIT 12	−16 −14 −12	(Most significant bit)
7	BIT 15 BIT 13 BIT 11	−16 −14 −12	Data Bits, Three-state outputs. See Table 4 for format of $\overline{\text{EN}}$ables and bytes.
8	BIT 14 BIT 12 BIT 10	−16 −14 −12	
9	BIT 13 BIT 11 BIT 9	−16 −14 −12	
10	BIT 12 BIT 10 nc	−16 −14 −12	
11	BIT 11 BIT 9 nc	−16 −14 −12	
12	BIT 10 nc nc	−16 −14 −12	
13	BIT 9 nc nc	−16 −14 −12	
14	BIT 8		
15	BIT 7		
16	BIT 6		
17	BIT 5		
18	BIT 4		
19	BIT 3		
20	BIT 2		
21	BIT 1		Least significant bit
22	$\overline{\text{LBEN}}$		Low Byte $\overline{\text{EN}}$able. If not in handshake mode (see pin 27) when LO (with $\overline{\text{CE}}/\overline{\text{LD}}$, pin 30) activates low-order byte outputs, BITS 1-8 When in handshake mode (see pin 27), serves as a low-byte flag output. See Figures 8, 9 and 10.
23	$\overline{\text{MBEN}}$ $\overline{\text{HBEN}}$	−16 −14 −12	Mid Byte $\overline{\text{EN}}$able. Activates BITS 9-16, see $\overline{\text{LBEN}}$ (pin 22) High Byte $\overline{\text{EN}}$able. Activates BITS 9-14, POL, OR, see $\overline{\text{LBEN}}$ (pin 22)
24	$\overline{\text{HBEN}}$ CLOCK3	−16 14 −12	High Byte $\overline{\text{EN}}$able. Activates POL, OR, see $\overline{\text{LBEN}}$ (pin 22). RC oscillator pin. Can be used as clock output.

PIN	SYMBOL	DESCRIPTION
25	CLOCK1	Clock input. External clock or oscillator.
26	CLOCK2	Clock output. Crystal or RC oscillator.
27	MODE	Input LO;Direct output mode where $\overline{\text{CE}}/\overline{\text{LD}}$, $\overline{\text{HBEN}}$, $\overline{\text{MBEN}}$, and $\overline{\text{LBEN}}$ act as inputs directly controlling byte outputs. If pulsed HI causes immediate entry into handshake mode (see Figure 9). If HI, enables $\overline{\text{CE}}/\overline{\text{LD}}$, $\overline{\text{HBEN}}$, $\overline{\text{MBEN}}$, and $\overline{\text{LBEN}}$ as outputs. Handshake mode will be entered and data output as in Figures 7 & 8 at conversion completion.
28	R/$\overline{\text{H}}$	Run/$\overline{\text{Hold}}$; Input HI-conversions continuously performed every 2^{17} (−16) 2^{15} (−14) or 2^{13} (−12) clock pulses. Input LO-conversion in progress completed, converter will stop in Auto-Zero 7 counts before input integrate.
29	SEN	Send-ENable: Input controls timing of byte transmission in handshake mode. HI indicates 'send'.'
30	$\overline{\text{CE}}/\overline{\text{LD}}$	Chip-$\overline{\text{E}}$nable/$\overline{\text{L}}$oa$\overline{\text{D}}$. With MODE (pin 27) LO, $\overline{\text{CE}}/\overline{\text{LD}}$ serves as a master output enable; when HI, the bit outputs and POL, OR are disabled. With MODE HI, pin serves as a $\overline{\text{L}}$oa$\overline{\text{D}}$ strobe (-ve going) used in handshake mode. See Figures 7 & 8.
31	V(+)	Positive Logic Supply Voltage. Nominally +5V.
32	AN.IN	ANalog INput. High side.
33	BUF IN	BUFfer INput to analog chip (ICL8052 or ICL8068)
34	REFCAP2	REFerence CAPacitor (negative side)
35	AN.GND.	ANalog GrouND. Input low side and reference low side.
36	A-Z	Auto-Zero node.
37	VREF	Voltage REFerence input (positive side)
38	REFCAP1	REFerence CAPacitor (positive side)
39	COMP-IN	COMParator INput from 8052/8068
40	V(−)	Negative Supply Voltage. Nominally −15V.

	CE/LD																
	HBEN		MBEN								LBEN						
7104-16	POL	O/R	B16	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

	HBEN								LBEN							
7104-14	POL	O/R	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1
7104-12	POL	O/R			B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

TABLE 4: Three-State Byte Formats and $\overline{\text{EN}}$able Pins.

DETAILED DESCRIPTION

Analog Section

Figure 4 shows the equivalent Circuit of the Analog Section of both the ICL7104/8052 and the ICL7104/8068 in the 3 different phases of operation. If the Run/$\overline{\text{H}}$old pin is left open or tied to V+, the system will perform conversions at a rate determined by the clock frequency: 131,072 for −16; 32,368 for −14; and 8092 for −12 clock periods per cycle (see Figure 5 conversion timing).

Figure 4A: Phase I Auto-Zero

Figure 4B: Phase II Integrate Input

Figure 4C: Phase III + Deintegrate

Figure 4D: Phase III - Deintegrate

Figure 4: Analog Section of Either ICL8052 or ICL8068 with ICL7104

1. **Auto-Zero Phase I** Fig. 4A.

   During Auto-Zero, the input of the buffer is shorted to analog ground thru switch 2, and switch 1 closes a loop around the integrator and comparator. The purpose of the loop is to charge the Auto-Zero capacitor until the integrator output does not change with time. Also switches 4 and 9 recharge the reference capacitor to Vref.

2. **Input Integrate Phase II** Fig. 4B.

   During input integrate the Auto-Zero loop is opened and the analog input is connected to the buffer input thru switch 3. (The reference capacitor is still being charged to V_{ref} during this time.) If the input signal is zero, the buffer, integrator and comparator will see the same voltage that existed in the previous state (Auto-Zero). Thus the integrator output will not change but will remain stationary during the entire Input Integrate cycle. If V_{in} is not equal to zero, an unbalanced condition exists compared to the Auto-Zero phase, and the integrator will generate a ramp whose slope is proportional to V_{in}. At the end of this phase, the sign of the ramp is latched into the polarity F/F.

Deintegrate Phase III Fig. 4 C&D

During the Deintegrate phase, the switch drive logic uses the output of the polarity F/F in determining whether to close switches 6 and 9 or 7 and 8. If the input signal was positive, switches 7 and 8 are closed and a voltage which is V_{ref} more negative than during Auto-Zero is impressed on the buffer input. Negative inputs will cause $+V_{ref}$ to be applied to the buffer input via switches 6 and 9. Thus, the reference capacitor generates the equivalent of a (+) reference or a (−) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to the zero-crossing point established in Phase I. The time, or number of counts, required to do this is proportional to the input voltage. Since the Deintegrate phase can be twice as long as the Input integrate phase, the input voltage required to give a full scale reading = $2V_{ref}$.

Note: Once a zero crossing is detected, the system automatically reverts to Auto-Zero phase for the leftover Deintegrate time (unless Run/$\overline{\text{Hold}}$ is manipulated, see Run/$\overline{\text{Hold}}$ Input in detailed description, digital section).

COUNTS			
	Phase I	Phase II	Phase III
-16	32768	32768	65536
-14	8192	8192	16384
-12	2048	2048	4096

Figure 5: Conversion Timing

Table 5: Some Typical Component Values

V++ = +15V, V+ = 5V, V− = −15V, Clock Freq = 200 kHz

ICL8052/8068 with	ICL7104-16			ICL7104-14		ICL7104-12		UNITS
Full scale V_{IN}	200	800	4000	100	4000	50	4000	mV
Buffer Gain	10	1	1	10	1	10	1	
R_{INT}	100	43	200	47	180	27	200	kΩ
C_{INT}	.33	.33	.33	0.1	0.1	.022	.022	μF
C_{AZ}	1.0	1.0	1.0	1.0	1.0	.47	.47	μF
C_{ref}	10	1.0	1.0	10	1.0	4.7	4.7	μF
V_{ref}	100	400	2000	50	2000	25	200	mV
Resolution	3.1	12	61	6.1	244	12	980	μV

Component Value Selection

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

Integrating Resistor

The integrating resistor is determined by the full scale input voltage and the output current of the buffer used to charge the integrator capacitor. This current should be small compared to the output short circuit current such that thermal effects are kept to a minimum and linearity is not affected. Values of 5 to 40 μA give good results with a nominal of 20 μA. The exact value may be chosen by

$$R_{INT} = \frac{\text{full scale voltage*}}{20\mu A}$$

*Note: If gain is used in the buffer amplifier then -

$$R_{INT} = \frac{\text{(Buffer gain) (full scale voltage)}}{20\mu A}$$

Integrating Capacitor

The product of integrating resistor and capacitor is selected to give 9 volt swing for full scale inputs. This is a compromise between possibly saturating the integrator (at +14 volts) due to tolerance build-up between the resistor, capacitor and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. In general, the value of C_{INT} is give by

$$C_{INT} = \frac{\left[\begin{array}{l}\text{(32768 for -16}\\ \text{(8192 for -14 X clock period)}\\ \text{(2048 for -12}\end{array}\right] \text{X } (20\mu A)}{\text{Integrator output voltage swing}}$$

A very important characteristic of the integrating capacitor is that it have low dielectric absorption to prevent roll-over or ratiometric errors. A good test for dielectric absorption is to use the capacitor with the input tied to the reference.

This ratiometric condition should read half scale 100 . . . 000 and any deviation is probably due to dielectric absorption. Polypropylene capacitors give undetectable errors at reasonable cost. Polystyrene and polycarbonate capacitors may also be used in less critical applications.

Auto-Zero and Reference Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system, a large capacitor giving less noise. The reference capacitor should be large enough such that stray capacitance to ground from its nodes is negligible.

Note: When gain is used in the buffer amplifier the reference capacitor should be substantially larger than the auto-zero capacitor. As a rule of thumb, the reference capacitor should be approximately the gain times the value of the auto-zero capacitor. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Reference Voltage

The analog input required to generate a full scale output is $V_{IN} = 2\ V_{REF}$.

The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7104 at 16 bits is one part in 65536, or 15.26ppm. Thus, if the reference has a temperature coefficient of 50ppm/°C (on board reference) a temperature change of 1/3°C will introduce a one-bit absolute error. For this reason, it is recommended that an external high quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

Buffer Gain

At the end of the auto-zero interval, the instantaneous noise voltage on the auto-zero capacitor is stored, and subtracts from the input voltage while adding to the reference voltage during the next cycle. The result is that this noise voltage effectively is somewhat greater than the input noise voltage of the buffer itself during integration. By introducing some voltage gain into the buffer, the effect of the auto-zero noise (referred to the input) can be reduced to the level of the inherent buffer noise. This generally occurs with a buffer gain of between 3 and 10. Further increase in buffer gain merely increases the total offset to be handled by the auto-zero loop, and reduces the available buffer and integrator swings, without improving the noise performance of the system. The circuit recommended for doing this with the ICL8068/ICL7104 is shown in Figure 6. With careful layout, the circuit shown can achieve effective input noise voltages on the order of 1-2μV, allowing full 16-bit use with full scale inputs of as low as 150mV. Note that at this level, thermo-electric EMFs between PC boards, IC pins, etc., due to local temperature changes can be very troublesome. For further discussion, see App. Note A030.

Figure 6: Adding Buffer Gain to ICL8068

ICL8052 vs ICL8068

The ICL8052 offers significantly lower input leakage currents than the ICL8068, and may be found preferable in systems with high input impedances. However, the ICL8068 has substantially lower noise voltage, and for systems where system noise is a limiting factor, particularly in low signal level conditions, will give better performance.

DETAILED DESCRIPTION

Digital Section

The digital section includes the clock oscillator circuit, a 16, 14 or 12 bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic and UART handshake logic, as shown in the Block Diagram Figure 7 (16 bit version shown).

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined under "ICL7104 Electrical Characteristics". For minimum power consumption, all inputs should swing from GND (low) to V+ (high). Inputs driven from TTL gates should have 3-5kΩ pullup resistors added for maximum noise immunity.

Mode Input

The MODE input is used to control the output mode of the converter. When the MODE pin is connected to GND or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in three bytes for the 7104-16 or two bytes for the 7104-14 and 7104-12, then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

STaTuS Output

During a conversion cycle, the STaTuS output goes high at the beginning of Input Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 5 for details of this timing. This signal may be used as a "data valid" flag (data never changes while STaTuS is low) to drive interrupts, or for monitoring the status of the converter.

Run/$\overline{\text{H}}$old Input

When the Run/$\overline{\text{H}}$old input is connected to V+ or left open (this input has a pullup resistor to ensure a high level when the pin is left open), the circuit will continuously perform conversion cycles, updating the output latches at the end of every Deintegrate (Phase III) portion of the conversion cycle (See Figure 5). (See under "Handshake Mode" for exception.) In this mode of operation, the conversion cycle will be performed in 131,072 for 7104-16, 32768 for 7104-14 and 8192 for 7104-2 clock periods, regardless of the resulting value.

If Run/$\overline{\text{H}}$old goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to eliminate the time spent in Deintegrate after the zero-crossing. If Run/$\overline{\text{H}}$old stays or goes low, the converter will ensure a minimum Auto-Zero time, and then wait in Auto-Zero until the Run/$\overline{\text{H}}$old input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STaTuS output will go high) seven clock periods after the high level is detected at Run/$\overline{\text{H}}$old. See Figure 8 for details.

Using the Run/$\overline{\text{H}}$old input in this manner allows an easy "convert on demand" interface to be used. The converter may be held at idle in Auto-Zero with Run/$\overline{\text{H}}$old low. When Run/$\overline{\text{H}}$old goes high the conversion is started, and when the STaTuS output goes low the new data is valid (or transferred to the UART - see Handshake Mode). Run/$\overline{\text{H}}$old may now go low terminating Deintegrate and ensuring a minimum Auto-Zero time before stopping to wait for the next conversion. Alternately, Run/$\overline{\text{H}}$old can be used to minimize conversion time by ensuring that it goes low during Deintegrate, after zero crossing, and goes high after the hold point is reached. The required activity on the Run/$\overline{\text{H}}$old input can be provided by connecting it to the CLOCK3 (-12, -14), CLOCK2 (-16) Output. In this mode the conversion time is dependent on the input value measured. Also refer to Intersil Application Bulletin A030 for a discussion of the effects this will have on Auto-Zero performance.

Figure 7: Digital Section

Figure 8: Run/Hold Operation

If the Run/Hold input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for Run/Hold to go high. As above, Integrate (Phase II) begins seven clock periods after the high level is detected.

Direct Mode

When the MODE pin is left at a low level, the data outputs[bits 1 through 8 low order byte, see Table 4 for format of middle (-16) and high order bytes]are accessible under control of the byte and chip ENable terminals as inputs. These ENable inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip ENable input is low, taking a byte ENable input low will allow the outputs of that byte to become active (three-stated on). This allows a variety of parallel data accessing techniques to be used, as shown in Figure 2. The timing requirements for these outputs are shown in Figure 2 and Table 1.

It should be noted that these control inputs are asynchronous with respect to the converter clock - the data may be accessed at any time. Thus it is possible to access the data while it is being updated, which could lead to scrambled data. Synchronizing the access of data with the conversion cycle by monitoring the STaTuS output will prevent this. Data is never updated while STaTuS is low. Also note the potential bus conflict described under "Initial Clear Circuitry".

Figure 9: Handshake With SEN Held Positive

Handshake Mode

The handshake output mode is provided as an alternative means of interfacing the ICL7104 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte ENable inputs. This mode is specifically designed to allow a direct interface between the ICL7104 and industry-standard UARTs (such as the Intersil CMOS UARTs, IM6402/3) with no external logic required. When triggered into the handshake mode, the ICL7104 provides all the control and flag signals necessary to sequence the three (ICL7106-16) or two (ICL7104-14, -12) bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission to minimize the number of lines to the central controlling processor.

Entry into the handshake mode will occur if either of two conditions are fulfilled; first, if new data is latched (i.e. a conversion is completed) while MODE pin (pin 27) is high, in which case entry occurs at the end of the latch cycle; or secondly, if the MODE pin goes from low to high, when entry will occur immediately (if new data is being latched, entry is delayed to the end of the latch cycle). While in the handshake mode, data latching is inhibited, and the MODE pin is ignored. (Note that conversion cycles will continue in the normal manner). This allows versatile initiation of handshake operation without danger of false data generation; if the MODE pin is held high, every conversion (other than those completed during handshake operations) will start a new handshake operation, while if the MODE pin is pulsed high, handshake operations can be obtained "on demand."

When the converter enters the handshake mode, or when the MODE input is high, the chip and byte ENable terminals become TTL-compatible outputs which provide the control signals for the output cycle. The Send ENable pin (SEN) (pin 29) is used as an indication of the ability of the external device to receive data. The condition of the line is sensed once every clock pulse, and if it is high; the next (or first) byte is enabled on the next rising CLOCK 1 (pin 25) clock edge, the corresponding byte ENable line goes low, and the Chip ENable/LoaD line (pin 30) (CE/LD) goes low for one full clock pulse only, returning high.

On the next falling CLOCK 1 clock pulse edge, if SEN remains high, or after it goes high again, the byte output lines will be put in the high impedance state (or three-stated off). One half pulse later, the byte ENable pin will be cleared high, and (unless finished) the CE/LD and the next byte ENable pin will go low. This will continue until all three (2 in the case of 12 and 14 bit devices) bytes have been sent. The bytes are individually put into the low impedance state i.e.: three-stated on during most of the time that their byte ENable pin is (active) low. When receipt of the last byte has been acknowledged by a high SEN, the handshake mode will be cleared, re-enabling data latching from conversions, and recognizing the condition of the MODE pin again. The byte and chip ENable will be three-stated off, if MODE is low, but held high by their (weak) pullups. These timing relationships are illustrated in Figure 9, 10, and 11, and Table 2.

Figure 10: Handshake - Typical UART Interface Timing

Figure 9 shows the sequence of the output cycle with SEN held high. The handshake mode (Internal MODE high) is entered after the data latch pulse (since MODE remains high the $\overline{CE}/\overline{LD}$, $\overline{LBEN}$, $\overline{MBEN}$ and $\overline{HBEN}$ terminals are active as outputs). The high level at the SEN input is sensed on the same high to low internal clock edge. On the next low to high internal clock edge, the $\overline{CE}/\overline{LD}$ and the $\overline{HBEN}$ outputs assume a low level and the high-order byte (POL and OR, and except for -16, Bis 9-14) outputs are enabled. The $\overline{CE}/\overline{LD}$ output remains low for one full internal clock period only, the data outputs remain active for 1-1/2 internal clock periods, and the high byte $\overline{EN}$able remains low for two clock periods. Thus the $\overline{CE}/\overline{LD}$ output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte $\overline{EN}$able as an output may be used as a byte identification flag. With SEN remaining high the converter completes the output cycle using $\overline{CE}/\overline{LD}$, $\overline{MBEN}$ and $\overline{LBEN}$ while the remaining byte outputs (see Table 4) are activated. The handshake mode is terminated when all bytes are sent (3 for -16, 2 for -14, -12).

Figure10shows an output sequence where the SEN input is used to delay portions of the sequence, or handshake, to ensure correct data transfer. This timing diagram shows the relationships that occur using an industry-standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEN input to the ICL7104 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{CE}/\overline{LD}$ terminal of the ICL7104 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

Assuming the UART Transmitter Buffer Register is empty, the SEN input will be high when the handshake mode is entered after new data is stored. The $\overline{CE}/\overline{LD}$ and $\overline{HBEN}$ terminals will go low after SEN is sensed, and the high order byte outputs become active. When $\overline{CE}/\overline{LD}$ goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the $\overline{HBEN}$ output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next ICL7104 internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the $\overline{HBEN}$ output returns high. At the same time, the $\overline{CE}/\overline{LD}$ and $\overline{MBEN}$ (-16) or $\overline{LBEN}$ outputs go low, and the corresponding byte outputs become active. Similarly, when the $\overline{CE}/\overline{LD}$ returns high at the end of one clock period, the enabled data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7104 internal clock high to low edge, disabling the data outputs. For the 16 bit device, the sequence is repeated for $\overline{LBEN}$. One-half internal clock later, the handshake mode will be cleared, and the chip and byte $\overline{EN}$able terminals return high and stay active (as long as MODE stays high).

With the MODE input remaining high as in these examples, the converter will output the results of every conversion

Figure 11: Handshake Triggered By Mode

except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 11 shows a handshake output sequence triggered by such an edge. In addition, the SEN input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEN input, and the sequence for the first (high order) byte is similar to the sequence for the other bytes. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STaTuS output and Run/$\overline{\text{Hold}}$ input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

Initial Clear Circuitry

The internal logic of the 7104 is supplied by an internal regulator between V++ and Digital Ground. The regulator includes a low-voltage detector that will clear various registers. This is intended to ensure that on initial power-up, the control logic comes up in Auto-Zero, with the 2nd, 3rd, and 4th MSB bits cleared, and the "mode" FF cleared (i.e. in "direct" mode). This, however, will also clear these registers if the supply voltage "glitches" to a low enough value. Additionally, if the supply voltage comes up too fast, this clear pulse may be too narrow for reliable clearing. In general, this is not a problem, but if the UART internal "MODE" FF should come up set, the byte and chip ENable lines will become active outputs. In many systems this could lead to buss conflicts, especially in non-handshake systems. In any case, SEN should be high (held high for non-handshake systems) to ensure that the MODE FF will be cleared as fast as possible (see Fig. 9 for timing). For these and other reasons, adequate supply bypass is recommended.

4

Oscillator

The ICL7104-14 and -12 are provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated as an RC or crystal oscillator.

Figure 12 shows the oscillator configured for RC operation. The internal clock will be of the same frequency and phase as the voltage on the CLOCK 3 pin. The resistor and capacitor should be connected as shown. The circuit will oscillate at a frequency given by f = .45/RC. An 100kΩ resistor is recommended for useful ranges of frequency. For optimum 60Hz line rejection, the capacitor value should be chosen such that 32768 (-16), 8192 (-14), 2048 (-12) clock periods is close to an integral multiple of the 60Hz period.

Figure 12: RC Oscillator

Note that CLOCK 3 has the same output drive as the bit outputs.

As a result of pin count limitations, the ICL7104-16 has only CLOCK 1 and CLOCK 2 available, and cannot be used as an RC oscillator. The internal clock will correspond to the inverse of the signal on CLOCK 2. Figure 13 shows a crystal oscillator circuit, which can be used with all 7104 versions. If an external clock is to be used, it should be applied to CLOCK 1. The internal clock will correspond to the signal applied to this pin.

Figure 13: Crystal Oscillator

POWER SUPPLY SEQUENCING

Because of the nature of the CMOS process used to fabricate the ICL7104, and the multiple power supplies used, there are certain conditions of these supplies under which a disabling and potentially damaging SCR action can occur. All of these conditions involve the V+ supply (nom. +5V) being more positive than the V++ supply. If there is any possibility of this occuring during start-up, shut down, under transient conditions during operation, or when inserting a PC board into a "hot" socket, etc., a diode should be placed between V- and V++ to prevent it. A germanium or Schottky rectifier diode would be best, but in most cases a silicon rectifier diode is adequate.

ANALOG AND DIGITAL GROUNDS

Extreme care must be taken to avoid ground loops in the layout of 8068 or 8052/7104 circuits, especially in 16-bit and high sensitivity circuits. It is most important that return currents from digital loads are not fed into the analog ground line. A recommended connection sequence for the ground lines is shown in Figure 14.

Some applications bulletins that may be found useful are listed here:

A016 "Selecting A/D Converters", by Dave Fullagar
A017 "The Integrating A/D Converter", by Lee Evans
A018 "Do's and Dont's of Applying A/D Converters", by Peter Bradshaw and Skip Osgood
A025 "Building a Remote Data Logging Station", by Peter Bradshaw
A030 "The ICL7104 - A Binary Output A/D Converter for Microprocessors", by Peter Bradshaw
R005 "Interfacing Data Converters & Microprocessors", by Peter Bradshaw et al, Electronics, Dec. 9, 1976.

Figure 14: Grounding Sequence

PACKAGE DIMENSIONS

14 Pin Plastic Dual-In-Line Package

14 Pin Ceramic Dual-In-Line Package

14 Pin CERDIP

40 Pin Plastic Dual-In-Line Package

40 Pin Ceramic Dual-In-Line Package

INTERSIL

ICL7109
12 Bit Binary A/D Converter for Microprocessor Interfaces

FEATURES

- **12 bit binary (plus polarity and overrange) dual slope integrating analog-to-digital converter.**
- **Byte-organized TTL-compatible three-state outputs and UART handshake mode for simple parallel or serial interfacing to microprocessor systems.**
- **RUN/$\overline{\text{HOLD}}$ input and STATUS output can be used to monitor and control conversion timing.**
- **True differential input and differential reference.**
- **Low noise-typically 15μV peak-to-peak.**
- **1pA typical input current.**
- **Operates at up to 30 conversions per second.**
- **On-chip oscillator operates with inexpensive 3.58MHz TV crystal giving 7.5 conversions per second for 60Hz rejection, or may be operated as an RC oscillator for other clock frequencies.**
- **Fabricated using MAX-CMOS™ technology combining analog and digital functions on a single low power LSI CMOS chip.**
- **All inputs fully protected against static discharge; no special handling precautions necessary.**

GENERAL DESCRIPTION

The ICL7109 is a high performance, low power integrating A/D converter designed to easily interface to microprocessors.

The output data (12 bits, polarity and overrange) may be directly accessed under control of two byte enable inputs and a chip select input for a simple parallel bus interface. A UART handshake mode is provided which allows the ICL7109 to work with industry-standard UARTs to provide serial data transmission, ideal for remote data logging applications. The RUN/$\overline{\text{HOLD}}$ input and STATUS output allow monitoring and control of conversion timing.

The ICL7109 provides the user the high accuracy, low noise, low drift, versatility and economy of the dual-slope integrating A/D converter. Features like true differential input and reference, zero drift of less than 1μV/°C max., input bias current of 10pA max., and typical power consumption of 20mW make the ICL7109 an attractive per-channel alternative to analog multiplexing for many data acquisition applications.

Note: A MIL-STD (883 processing) version of the ICL7109 will be available July 1979.

PIN CONFIGURATION AND TEST CIRCUIT:

(See Figure 1 for typical connection to a UART or Microcomputer)

PACKAGE DIMENSIONS

40 Pin Plastic Dual-in-Line Package

40 Pin Ceramic Dual-in-Line Package

ORDERING INFORMATION

Part	Package	Temp. Range	Order Part #
7109	40 pin ceramic DIP	-25°C to +85°C	ICL7109IDL
7109	40 pin plastic DIP	0°C to +70°C	ICL7109CPL

ABSOLUTE MAXIMUM RATINGS

Positive Supply Voltage (GND to V^+) ..... +6.2V
Negative Supply Voltage (GND to V^-) ..... −9V
Analog Input Voltage (Lo or Hi) (Note 1) ..... V^+ to V^-
Reference Input Voltage (Lo or Hi) (Note 1) ..... V^+ to V^-
Digital Input Voltage (Pins 2-27) (Note 2) ..... $V^+ + 0.3V$ / GND − 0.3V
Power Dissipation (Note 3)
  Ceramic or Cerdip Package ..... 1W @ 85° C
  Plastic Package ..... 500mW @ 70° C
Operating Temperature
  Ceramic or Cerdip Package ..... −25° C ≤ T_A ≤ 85° C
  Plastic Package ..... 0° C ≤ T_A ≤ 70° C
Storage Temperature ..... −55° C ≤ T_A ≤ 125° C
Lead Temperature (soldering, 60 sec) ..... 300° C

Absolute maximum ratings define stress limitations which if exceeded may permanently damage the device. These ratings are not continuous duty ratings. For continuous operation these devices must be operated under the conditions defined under "Operating Characteristics."

TABLE I OPERATING CHARACTERISTICS

All parameters with V^+ = +5V, V^- = −5V, GND = 0V, T_A = 25°C, unless otherwise indicated.
Test circuit as shown on page 1.

ANALOG SECTION

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading		V_{IN} = 0.0V Full scale = 409.6mV	0000_8	$\pm 0000_8$	$+0000_8$	Octal Reading
Ratiometric Reading		$V_{IN} = V_{REF}$ V_{REF} = 204.8mV	3777_8	3777_8 4000_8	4000_8	Octal Reading
Non-Linearity (Max deviation from best straight line fit)		Full scale = 409.6mV or 4.096V	−1	±.2	+1	Counts
Roll-over Error (difference in reading for equal pos. and neg. inputs near full scale.			−1	±.2	+1	Counts
Common Mode Rejection Ratio		V_{CM} ± 1V V_{IN} = 0V Full Scale = 409.6mV		50		μV/V
Noise (p-p value not exceeded 95% of time)		V_{IN} = 0V Full Scale = 409.6mV		15		μV
Leakage Current at Input		V_{IN} = 0V		1	10	pA
Zero Reading Drift		V_{IN} = 0V		0.2	1	μV/°C
Scale Factor Temperature Coefficient		V_{IN} = 408.9mV => 7770_8 reading Ext. Ref. 0 ppm/°C		1	5	ppm/°C
Supply Current V^+ to GND	I_{DL}	V_{IN} = 0, Crystal Osc. 3.58MHz test circuit Pins 2-21, 25, 26, 27, 29, open		700	1500	μA
Supply Current V^+ to V^-	I_{DA}			700	1500	μA
Ref Out Voltage		Referred to V^+, 25kΩ between V^+ and REF OUT	−2.4	−2.8	−3.2	V
Ref Out Temp. Coefficient		25kΩ between V^+ and REF OUT		80		ppm/°C

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DIGITAL SECTION

PARAMETER		SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Output High Voltage		V_{OH}	I_{OUT} = 100μA Pins 2-16, 18, 19, 20	3.5	4.3		V
Output Low Voltage		V_{OL}	I_{OUT} = 1.6mA		0.2	0.4	V
Output Leakage Current			Pins 3-16 high impedance		±.01	±1	μA
Control I/O Pullup Current			Pins 18, 19, 20 V_{OUT} = V⁺ −3V MODE input at GND		5		μA
Control I/O Loading			$\overline{HBEN}$ Pin 19 $\overline{LBEN}$ Pin 18			50	pF
Input High Voltage		V_{IH}	Pins 18-21, 26, 27 referred to GND	2.5			V
Input Low Voltage		V_{IL}	Pins 18-21, 26, 27 referred to GND			1	V
Input Pull-up Current			Pins 26, 27 V_{OUT} = V⁺ −3V		5		μA
Input Pull-up Current			Pins 17, 24 V_{OUT} = V⁺ −3V		25		μA
Input Pull-down Current			Pin 21 V_{OUT} = GND +3V		5		μA
Oscillator Output Current	High	O_{OH}	V_{OUT} = 2.5V		1		mA
	Low	O_{OL}	V_{OUT} = 2.5V		1.5		mA
Buffered Oscillator Output Current	High	BO_{OH}	V_{OUT} = 2.5V		2		mA
	Low	BO_{OL}	V_{OUT} = 2.5V		5		mA
MODE Input Pulse Width				50			ns

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA

Note 2: Due to the SCR structure inherent in the process used to fabricate these devices, connecting any digital inputs or outputs to voltages greater than V⁺ or less than GND may cause destructive device latchup. For this reason it is recommended that no inputs from sources not on the same power supply be applied to the ICL7109 before its power supply is established, and that in multiple supply systems the supply to the ICL7109 be activated first.

Note 3: This limit refers to that of the package and will not be obtained during normal operation.

Figure 1A. To transmit latest result, send any word to UART.

Figure 1B. Typical Connection Diagram Parallel Interface With 8748/8048 Microcomputer

TABLE 2 - Pin Assignment and Function Description

PIN	SYMBOL	DESCRIPTION
1	GND	Digital Ground, 0V, Ground return for all digital logic
2	STATUS	Output - High during integrate and deintegrate until data is latched. - Low when analog section is in Auto-Zero configuration.
3	POL	Polarity, Three-State Output
4	OR	Over-range, Three-State Output
5	B12	Bit 12 (Most Significant Bit)
6	B11	Bit 11
7	B10	Bit 10
8	B9	Bit 9
9	B8	Bit 8
10	B7	Bit 7
11	B6	Bit 6 Data Bits, Three-State Output
12	B5	Bit 5
13	B4	Bit 4
14	B3	Bit 3
15	B2	Bit 2
16	B1	Bit 1 (Least Significant Bit)
17	TEST	Input High - Normal Operation. Input Low - Forces all bit outputs high. Note: This input is used for test purposes only.
18	$\overline{LBEN}$	Low Byte Enable - With Mode (Pin 21) low, and $\overline{CE/LOAD}$ (Pin 20) low, taking this pin low activates low order byte outputs B1-B8. - With Mode (Pin 21) high, this pin serves as a low byte flag output used in handshake mode. See Figures 7, 8, 9.
19	$\overline{HBEN}$	High Byte Enable - With Mode (Pin 21) low, and $\overline{CE/LOAD}$ (Pin 20) low, taking this pin low activates high order byte outputs B9-B12, POL, OR. - With Mode (Pin 21) high, this pin serves as a high byte flag output used in handshake mode. See Figures 7, 8, 9.
20	$\overline{CE/LOAD}$	Chip Enable Load - With Mode (Pin 21) low, $\overline{CE/LOAD}$ serves as a master output enable. When high, B1-B12, POL, OR outputs are disabled. - With Mode (Pin 21) high, this pin serves as a load strobe used in handshake mode. See Figures 7, 8, 9.
21	MODE	Input Low - Direct output mode where $\overline{CE/LOAD}$ (Pin 20), $\overline{HBEN}$ (Pin 19) and $\overline{LBEN}$ (Pin 18) act as inputs directly controlling byte outputs. Input Pulsed High - Causes immediate entry into handshake mode and output of data as in Figure 9. Input High - Enables $\overline{CE/LOAD}$ (Pin 20), $\overline{HBEN}$ (Pin 19), and $\overline{LBEN}$ (Pin 18) as outputs, handshake mode will be entered and data output as in Figures 7 and 8 at conversion completion.
22	OSC IN	Oscillator Input
23	OSC OUT	Oscillator Output
24	OSC SEL	Oscillator Select - Input high configures OSC IN, OSC OUT, BUF OSC OUT as RC oscillator - clock will be same phase and duty cycle as BUF OSC OUT. - Input low configures OSC IN, OSC OUT for crystal oscillator - clock frequency will be 1/58 of frequency at BUF OSC OUT.
25	BUF OSC OUT	Buffered Oscillator Output
26	RUN/$\overline{HOLD}$	Input High - Conversions continuously performed every 8192 clock pulses. Input Low - Conversion in progress completed, converter will stop in Auto-Zero 7 counts before integrate.
27	SEND	Input - Used in handshake mode to indicate ability of an external device to accept data.
28	V^+	Analog Negative Supply - Nominally 5V with respect to GND (Pin 1).
29	REF OUT	Reference Voltage Output - Nominally 2.8V down from V^+ (Pin 40).
30	BUFFER	Buffer Amplifier Output
31	AUTO-ZERO	Auto-Zero Node - Inside foil of C_{AZ}
32	INTEGRATOR	Integrator Output - Outside foil of C_{INT}
33	COMMON	Analog Common - System is Auto-Zeroed to COMMON
34	INPUT LO	Differential Input Low Side
35	INPUT HI	Differential Input High Side
36	REF IN	Differential Reference Input Positive
37	REF CAP	Reference Capacitor Positive
38	REF CAP	Reference Capacitor Negative
39	REF IN	Differential Reference Input Negative
40	V^+	Positive Supply Voltage - Nominally +5V with respect to GND (Pin 1).

DETAILED DESCRIPTION

Analog Section

Figure 2 shows the equivalent circuit of the Analog Section of the ICL7109. When the RUN/$\overline{HOLD}$ input is left open or connected to V^+, the circuit will perform conversions at a rate determined by the clock frequency (8192 clock periods per cycle). Each measurement cycle is divided into three phases as shown in Figure 3. They are (1) Auto-Zero (AZ), (2) Signal Integrate (INT) and (3) Deintegrate (DE).

1. **Auto-Zero Phase**

During auto-zero three things happen. First, input high and low are disconnected from their pins and internally shorted to analog common. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the AZ accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. **Signal Integrate Phase**

During signal integrate the auto-zero loop is opened, the internal short is removed and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between input high and input low for a fixed time of 2048 clock periods. At the end of this phase, the polarity of the integrated signal is determined.

Figure 2: Analog Section

Figure 3: Conversion Timing

3. **Deintegrate Phase**

   The final phase is deintegrate, or reference integrate. Input low is internally connected to analog common and input high is connected across the previously charged (during auto-zero) reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to the zero crossing (established in Auto Zero) with a fixed slope. Thus the time for the output to returr. to zero (represented by the number of clock periods counted) is proportional to the input signal.

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worst case condition would be a large positive common mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 4V full scale with some loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

The ICL7109 has, however, been optimized for operation with analog common near digital ground. With power supplies of +5V and −5V, this allows a 4V full scale integrator swing positive or negative maximizing the performance of the analog section.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to deintegrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by

selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worst case condition (see Component Values Selection below).

The roll-over error from these sources is minimized by having the reference common mode voltage near or at analog common.

Component Value Selection

For optimum performance of the analog section, care must be taken in the selection of values for the integrator capacitor and resistor, auto-zero capacitor, reference voltage, and conversion rate. These values must be chosen to suit the particular application.

The most important consideration is that the integrator output swing (for full-scale input) be as large as possible. For example, with ±5V supplies and COMMON connected to GND, the nominal integrator output swing at full scale is ±4V. Since the integrator output can go to 0.3V from either supply without significantly affecting linearity, a 4V integrator output swing allows 0.7V for variations in output swing due to component value and oscillator tolerances. With ±5V supplies and a common mode range of ±1V required, the component values should be selected to provide ±3V integrator output swing. Noise and rollover errors will be slightly worse than in the ±4V case. For larger common mode voltage ranges, the integrator output swing must be reduced further. This will increase both noise and rollover errors. To improve the performance, supplies of ±6V may be used.

1. **Integrating Resistor**

   Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 4.096 volt full scale, 200kΩ is near optimum and similarly a 20kΩ for a 409.6mV scale. For other values of full scale voltage, R_{INT} should be chosen by the relation $R_{INT} = \frac{\text{full scale voltage}}{20\mu A}$

2. **Integrating Capacitor**

   The integrating capacitor C_{INT} should be selected to give the maximum integrator output voltage swing without saturating the integrator (approximately 0.3 volt from either supply). For the ICL7109 with ±5 volt supplies and analog common connected to GND, a ±3.5 to ±4 volt integrator output swing is nominal. For 7-1/2 conversions per second (61.72KHz clock frequency) as provided by the crystal oscillator, nominal values for C_{INT} and C_{AZ} are 0.15μF and 0.33μF, respectively. If different clock frequencies are used, these values should be changed to maintain the integrator output voltage swing. In general, the value of C_{INT} is given by

   $$C_{INT} = \frac{(2048 \times \text{clock period})\,(20\mu A)}{\text{integrator output voltage swing}}$$

   An additional requirement of the integrating capacitor is that it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

3. **Auto-Zero Capacitor**

   The size of the auto-zero capacitor has some influence on the noise of the system; a big capacitor, giving less noise. However, it cannot be increased without limits since it, in parallel with the integrating capacitor forms an R-C time constant that determines the speed of recovery from overloads and more important the error that exists at the end of an auto-zero cycle. For 409.6mv full scale where noise is very important and the integrating resistor small, a value of C_{AZ} twice C_{INT} is optimum. Similarly for 4.096V full scale where recovery is more important than noise, a value of C_{AZ} equal to half of C_{INT} is recommended.

   For optimal rejection of stray pickup, the outer foil of C_{AZ} should be connected to the R-C summing junction and the inner foil to pin 31. Similarly the outer foil of C_{INT} should be connected to pin 32 and the inner foil to the R-C summing junction.

4. **Reference Capacitor**

   A 1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the reference low is not at analog common) and a 409.6mV scale is used, a larger value is required to prevent roll-over error. Generally 10μF will hold the roll-over error to 0.5 count in this instance.

5. **Reference Voltage**

   The analog input required to generate a full scale output of 4096 counts is $V_{IN} = 2V_{REF}$. Thus for a normalized scale, a reference of 2.048V should be usd for a 4.096V full scale, and 204.8mV should be used for a 0.4096V full scale. However, in many applications where the A/D is sensing the output of a transducer, there will exist a scale factor other than unity between the absolute output voltage to be measured and a desired digital output. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 409.6mV, the input voltage should be measured directly and a reference voltage of 0.341V should be used. Suitable values for integrating resistor and capacitor are 34k and 0.15μF. This avoids a divider on the input. Another advantage of this system occurs when a zero reading is desired for non-zero input. Temperature and weight measurements with an offset or tare are examples. The offset may be introduced by connecting the voltage output of the transducer between common and analog high, and the offset voltage between common and analog low, observing polarities carefully. However, in processor-based systems using the ICL7109, it may be more efficient to perform this type of scaling or tare subtraction digitally using software.

6. **Reference Sources**

   The stability of the reference voltage is a major factor in the overall absolute accuracy of the converter. The resolution of the ICL7109 at 12 bits is one part in 4096, or 244ppm. Thus if the reference has a temperature coefficient of 80ppm/°C (onboard reference) a temperature difference of 3°C will introduce a one-bit absolute error. For this reason, it is recommended that an external high-quality reference be used where the ambient temperature is not controlled or where high-accuracy absolute measurements are being made.

The ICL7109 provides a Reference Output (pin 29) which may be used with a resistive divider to generate a suitable reference voltage. This output will sink up to about 20mA without significant variation in output voltage, and is provided with a pullup bias device which sources about 10μA. The output voltage is nominally 2.8V below V^+, and has a temperature coefficient of ±80ppm/°C typ. When using the onboard reference, Ref Out (Pin 29) should be connected to Ref − (pin 39), and Ref+ should be connected to the wiper of a precision potentiometer between Ref Out and V^+. The circuit for a 204.8mV reference is shown in the test circuit. For a 2.048V reference, the fixed resistor should be removed, and a 25kΩ precision potentiometer between Ref Out and V^+ should be used.

DETAILED DESCRIPTION

Digital Section

The digital section includes the clock oscillator and scaling circuit, a 12-bit binary counter with output latches and TTL-compatible three-state output drivers, polarity, over-range and control logic, and UART handshake logic, as shown in the Block Diagram Figure 4.

Throughout this description, logic levels will be referred to as "low" or "high". The actual logic levels are defined in Table 1 "Operating Characteristics". For minimum power consumption, all inputs should swing from GND (low) to V^+ (high). Inputs driven from TTL gates should have 3-5kΩ pullup resistors added for maximum noise immunity.

MODE Input

The MODE input is used to control the output mode of the converter. When the MODE pin is connected to GND or left open (this input is provided with a pulldown resistor to ensure a low level when the pin is left open), the converter is in its "Direct" output mode, where the output data is directly accessible under the control of the chip and byte enable inputs. When the MODE input is pulsed high, the converter enters the UART handshake mode and outputs the data in two bytes, then returns to "direct" mode. When the MODE input is left high, the converter will output data in the handshake mode at the end of every conversion cycle. (See section entitled "Handshake Mode" for further details).

STATUS Output

During a conversion cycle, the STATUS output goes high at the beginning of Signal Integrate (Phase II), and goes low one-half clock period after new data from the conversion has been stored in the output latches. See Figure 3 for details of this timing. This signal may be used as a "data valid" flag (data never changes while STATUS is low) to drive interrupts, or for monitoring the status of the converter.

RUN/$\overline{\text{HOLD}}$ Input

When the RUN/$\overline{\text{HOLD}}$ input is connected to V^+ or left open (this input has a pullup resistor to ensure a high level when the pin is left open), the circuit will continuously perform conversion cycles, updating the output latches at the end of every Deintegrate (Phase III) portion of the conversion cycle (See Figure 3). In this mode of operation, the conversion cycle will be performed in 8192 clock periods, regardless of the resulting value.

If the RUN/$\overline{\text{HOLD}}$ input goes low (and stays there) during Integrate (Phase II) or Deintegrate (Phase III) before the zero crossing is detected, the converter will complete the conversion in progress, update the output latches, and then terminate Phase III, jumping to Auto-Zero (Phase I). If RUN/$\overline{\text{HOLD}}$ stays low, the converter will ensure a minimum Auto-Zero time, and wait in Auto-Zero until the RUN/$\overline{\text{HOLD}}$ input goes high. The converter will begin the Integrate (Phase II) portion of the next conversion (and the STATUS output will go high) seven clock periods after the high level is detected at RUN/$\overline{\text{HOLD}}$. See Figure 5 for details.

Figure 4: Digital Section

Figure 5: Run/$\overline{\text{Hold}}$ Operation

Using the RUN/$\overline{\text{HOLD}}$ input in this manner allows an easy "convert on demand" interface to be used. The converter may be held at idle in auto-zero with RUN/$\overline{\text{HOLD}}$ low. When RUN/$\overline{\text{HOLD}}$ goes high the conversion is started, and when the STATUS output goes low the new data is valid (or transferred to the UART - see Handshake Mode). RUN/$\overline{\text{HOLD}}$ may now go low terminating Deintegrate and ensuring a minimum Auto-Zero time before stopping to wait for the next conversion.

If RUN/$\overline{\text{HOLD}}$ goes low at any time during Deintegrate (Phase III) after the zero crossing has occurred, the circuit will immediately terminate Deintegrate and jump to Auto-Zero. This feature can be used to "short-cycle" the converter by eliminating the time spent in Deintegrate after the zero crossing. The required activity on the RUN/$\overline{\text{HOLD}}$ input can be provided by connecting it to the Buffered Oscillator Output. In this mode the conversion time is dependent on the input value measured. Also refer to Intersil Application Bulletin A030 for a discussion of the effects this will have on Auto-Zero performance.

If the RUN/$\overline{\text{HOLD}}$ input goes low and stays low during Auto-Zero (Phase I), the converter will simply stop at the end of Auto-Zero and wait for RUN/$\overline{\text{HOLD}}$ to go high. As above, Integrate (Phase II) begins seven clock periods after the high level is detected.

Direct Mode

When the MODE pin is left at a low level, the data outputs (bits 1 through 8 low order byte, bits 9 through 12, polarity and over-range high order byte) are accessible under control of the byte and chip enable terminals as inputs. These three inputs are all active low, and are provided with pullup resistors to ensure an inactive high level when left open. When the chip enable input is low, taking a byte enable input low will allow the outputs of that byte to become active (three-stated on). This allows a variety of parallel data accessing techniques to be used, as shown in the section entitled "Interfacing." The timing requirements for these outputs are shown in Figure 6 and Table 3.

Table 3 - Direct Mode Timing Requirements

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS
t_{BEA}	Byte Enable Width	200	500		ns
t_{DAB}	Data Access Time from Byte Enable		150	300	ns
t_{DHB}	Data Hold Time from Byte Enable		150	300	ns
t_{CEA}	Chip Enable Width	300	500		ns
t_{DAC}	Data Access Time from Chip Enable		200	400	ns
t_{DHC}	Data Hold Time from Chip Enable		200	400	ns

Figure 6: Direct Mode Output Timing

It should be noted that these control inputs are asynchronous with respect to the converter clock - the data may be accessed at any time. Thus it is possible to access the data while it is begin updated, which could lead to scrambled data. Synchronizing the access of data with the conversion cycle by monitoring the STATUS output will prevent this. Data is never updated while STATUS is low.

Handshake Mode

The handshake output mode is provided as an alternative means of interfacing the ICL7109 to digital systems, where the A/D converter becomes active in controlling the flow of data instead of passively responding to chip and byte enable inputs. This mode is specifically designed to allow a direct interface between the ICL7109 and industry-standard UARTs (such as the Intersil CMOS UARTs, IM6402/3) with no external logic required. When triggered into the handshake mode, the ICL7109 provides all the control and flag signals necessary to sequence the two bytes of data into the UART and initiate their transmission in serial form. This greatly eases the task and reduces the cost of designing remote data acquisition stations using serial data transmission to minimize the number of lines to the central controlling processor.

Entry into the handshake mode is controlled by the MODE pin. When the MODE terminal is held high, the ICL7109 will enter the handshake mode after new data has been stored in the output latches at the end of every conversion performed (See Figures 7 and 8). The MODE terminal may also be used to trigger entry into the handshake mode on demand. At any time during the conversion cycle, the low to high transition of a short pulse at the MODE input will cause immediate entry

Figure 7: Handshake With Send Held Positive

Figure 8: Handshake - Typical UART Interface Timing

into the handshake mode. If this pulse occurs while new data is being stored, the entry into handshake mode is delayed until the data is stable. While the converter is in the handshake mode, the MODE input is ignored, and although conversions will still be performed, data updating will be inhibited (See Figure 9) until the converter completes the output cycle and clears the handshake mode.

When the converter enters the handshake mode, or when the MODE input is high, the chip and byte enable terminals become TTL-compatible outputs which provide the control signals for the output cycle (See Figures 7, 8, and 9).

In handshake mode, the SEND input is used by the converter as an indication of the ability of the receiving device (such as a UART) to accept data.

Figure 7 shows the sequence of the output cycle with SEND held high. The handshake mode (Internal MODE high) is entered after the data latch pulse (since MODE remains high the $\overline{CE/LOAD}$, $\overline{LBEN}$ and $\overline{HBEN}$ terminals are active as outputs). The high level at the SEND input is sensed on the same high to low internal clock edge. On the next low to high internal clock edge, the $\overline{CE/LOAD}$ and the $\overline{HBEN}$ outputs assume a low level, and the high-order byte (bits 9 through 12, POL, and OR) outputs are enabled. The $\overline{CE/LOAD}$ output remains low for one full internal clock period only, the data outputs remain active for 1-1/2 internal clock periods, and the high byte enable remains low for two clock periods. Thus the $\overline{CE/LOAD}$ output low level or low to high edge may be used as a synchronizing signal to ensure valid data, and the byte enable as an output may be used as a byte identification flag. With SEND remaining high the converter completes the output cycle using $\overline{CE/LOAD}$ and $\overline{LBEN}$ while the low order byte outputs (bits 1 through 8) are activated. The handshake mode is terminated when both bytes are sent.

Figure 8 shows an output sequence where the SEND input is used to delay portions of the sequence, or handshake, to ensure correct data transfer. This timing diagram shows the relationships that occur using an industry-standard IM6402/3 CMOS UART to interface to serial data channels. In this interface, the SEND input to the ICL7109 is driven by the TBRE (Transmitter Buffer Register Empty) output of the UART, and the $\overline{CE/LOAD}$ terminal of the ICL7109 drives the TBRL (Transmitter Buffer Register Load) input to the UART. The data outputs are paralleled into the eight Transmitter Buffer Register inputs.

Assuming the UART Transmitter Buffer Register is empty, the SEND input will be high when the handshake mode is entered after new data is stored. The $\overline{CE/LOAD}$ and $\overline{HBEN}$ terminals will go low after SEND is sensed, and the high order byte outputs become active. When $\overline{CE/LOAD}$ goes high at the end of one clock period, the high order byte data is clocked into the UART Transmitter Buffer Register. The UART TBRE output will now go low, which halts the output cycle with the $\overline{HBEN}$ output low, and the high order byte outputs active. When the UART has transferred the data to the Transmitter Register and cleared the Transmitter Buffer Register, the TBRE returns high. On the next ICL7109

Figure 9: Handshake Triggered By Mode

internal clock high to low edge, the high order byte outputs are disabled, and one-half internal clock later, the $\overline{HBEN}$ output returns high. At the same time, the $\overline{CE/LOAD}$ and $\overline{LBEN}$ outputs go low, and the low order byte outputs become active. Similarly, when the $\overline{CE/LOAD}$ returns high at the end of one clock period, the low order data is clocked into the UART Transmitter Buffer Register, and TBRE again goes low. When TBRE returns to a high it will be sensed on the next ICL7109 internal clock high to low edge, disabling the data outputs. One-half internal clock later, the handshake mode will be cleared, and the $\overline{CE/LOAD}$, $\overline{HBEN}$, and $\overline{LBEN}$ terminals return high and stay active (as long as MODE stays high).

With the MODE input remaining high as in these examples, the converter will output the results of every conversion except those completed during a handshake operation. By triggering the converter into handshake mode with a low to high edge on the MODE input, handshake output sequences may be performed on demand. Figure 9 shows a handshake output sequence triggered by such an edge. In addition, the SEND input is shown as being low when the converter enters handshake mode. In this case, the whole output sequence is controlled by the SEND input, and the sequence for the first (high order) byte is similar to the sequence for the second byte. This diagram also shows the output sequence taking longer than a conversion cycle. Note that the converter still makes conversions, with the STATUS output and RUN/$\overline{HOLD}$ input functioning normally. The only difference is that new data will not be latched when in handshake mode, and is therefore lost.

Oscillator

The ICL7109 is provided with a versatile three terminal oscillator to generate the internal clock. The oscillator may be overdriven, or may be operated as an RC or crystal oscillator. The OSCILLATOR SELECT input changes the internal configuration of the oscillator to optimize it for RC or crystal operation.

When the OSCILLATOR SELECT input is high or left open (the input is provided with a pullup resistor), the oscillator is configured for RC operation, and the internal clock will be of the same frequency and phase as the signal at the BUFFERED OSCILLATOR OUTPUT. The resistor and capacitor should be connected as in Figure 10. The circuit will oscillate at a frequency given by f = .45/RC. A 100kΩ resistor is recommended for useful ranges of frequency. For optimum 60Hz line rejection, the capacitor value should be chosen such that 2048 clock periods is close to an integral multiple of the 60Hz period.

Figure 10: RC Oscillator

When the OSCILLATOR SELECT input is low a feedback device and output and input capacitors are added to the oscillator. In this configuration, as shown in Figure 11, the

Figure 11: Crystal Oscillator

oscillator will operate with most crystals in the 1 to 5MHz range with no external components. Taking the OSCILLATOR SELECT input low also inserts a fixed ÷58 divider circuit between the BUFFERED OSCILLATOR OUTPUT and the internal clock. Using an inexpensive 3.58MHz TV crystal, this division ratio provides an integration time given by:

$$T = (2048 \text{ clock periods}) \times \left(\frac{58}{3.58\text{MHz}}\right) = 33.18\text{ms}$$

This time is very close to two 60Hz periods or 33.33ms. The error is less than one percent, which will give better than 40dB 60Hz rejection. The converter will operate reliably at conversion rates of up to 30 per second, which corresponds to a clock frequency of 245.8kHz.

If at any time the oscillator is to be overdriven, the overdriving signal should be applied at the OSCILLATOR INPUT, and the OSCILLATOR OUTPUT should be left open. The internal clock will be of the same frequency, duty cycle, and phase as the input signal when OSCILLATOR SELECT is left open. When OSCILLATOR SELECT is at GND, the clock will be a factor of 58 below the input frequency.

When using the ICL7109 with the IM6403 UART, it is possible to use one 3.58MHz crystal for both devices. The BUFFERED OSCILLATOR OUTPUT of the ICL7109 may be used to drive the OSCILLATOR INPUT of the UART, saving the need for a second crystal. However, the BUFFERED OSCILLATOR OUTPUT does not have a great deal of drive, and when driving more than one slave device, external buffering should be used.

Test Input

When the TEST input is taken to a level halfway between V⁺ and GND, the counter output latches are enabled, allowing the counter contents to be examed anytime.

When the TEST input is connected to GND, the counter outputs are all forced into the high state, and the internal clock is disabled. When the input returns to the 1/2 (V⁺ −GND) voltage or to V⁺ and one clock is input, the counter outputs will all be clocked to the negative state. This allows easy testing of the counter and its outputs.

INTERFACING

Direct Mode

Figure 12 shows some of the combinations of chip enable and byte enable control signals which may be used when interfacing the ICL7109 to parallel data lines. The $\overline{CE/LOAD}$ input may be tied low, allowing either byte to be controlled by its own enable as in Figure 12A. Figure 12B shows a configuration where the two byte enables are connected together. In this configuration, the $\overline{CE/LOAD}$ serves as a chip enable, and the $\overline{HBEN}$ and $\overline{LBEN}$ may be connected to GND or serve as a second chip enable. The 14 data outputs will all be enabled simultaneously. Figure 12C shows the $\overline{HBEN}$ and $\overline{LBEN}$ as flag inputs, and $\overline{CE/LOAD}$ as a master enable, which could be the READ strobe available from most microprocessors.

Figure 12: Direct Mode Chip and Byte Enable Combinations

Figure 13 shows an approach to interfacing several ICL7109s to a bus, ganging the $\overline{HBEN}$ and $\overline{LBEN}$ signals to several converters together, and using the $\overline{CE/LOAD}$ inputs (perhaps decoded from an address) to select the desired converter.

Some practical circuits utilizing the parallel three-state output capabilities of the ICL7109 are shown in Figures 14 through 19. Figure 14 shows a straightforward application to the Intel MCS-48, -80 and -85 systems via an 8255PPI, where the ICL7109 data outputs are active at all times. The I/O ports of an 8155 may be used in the same way. This interface can be used in a read-anytime mode, although a read performed while the data latches are being updated will lead to scrambled data. This will occur very rarely, in the proportion of setup-skew times to conversion time. One way to overcome this is to read the STATUS output as well, and if it is high, read the data again after a delay of more than 1/2 converter clock period. If STATUS is now low, the second reading is correct, and if it is still high, the first reading is correct. Alternatively, this timing problem is completely avoided by using a read-after-update sequence, as shown in Figure 15. Here the high to low transition of the STATUS output drives an interrupt to the microprocessor causing it to access the data. This application also shows the RUN/$\overline{HOLD}$ input being used to initiate conversions under software control.

A similar interface to Motorola MC6800 or MOS Technology MCS650X systems is shown in Figure 16. The high to low transition of the STATUS output generates an interrupt via the Control Register B CB1 line. Note that CB2 controls the RUN/$\overline{HOLD}$ pin through Control Register B, allowing software-controlled initiation of conversions in this system also.

Figure 17 shows an interface to the Intersil IM6100 CMOS microprocessor family using the IM6101 PIE to control the data transfers. Here the data is read by the microprocessor in an 8-bit and a 6-bit word, directly from the ICL7109 to the microprocessor data bus. Again, the high to low transition of the STATUS output generates an interrupt leading to a software routine controlling the two read operations. As before, the RUN/$\overline{HOLD}$ input to the ICL7109 is shown as being under software control.

The three-state output capability of the ICL7109 allows direct interfacing to most microprocessor busses. Examples of this are shown in the Typical Connection Diagram on

Figure 13: Three-stating Several 7109's to a Small Bus

Page 3 and in Figures 18 and 19. It is necessary to carefully consider the system timing in this type of interface, to be sure that requirements for setup and hold times, and minimum pulse widths are met. Note also the drive limitations on long busses. Generally this type of interface is only favored if the memory peripheral address density is low so that simple address decoding can be used. Interrupt handling can also require many additional components, and using an interface device will usually simplify the system in this case.

Figure 14: Full-time Parallel Interface to INTEL Microcomputer Systems

Figure 15: Full-time Parallel Interface to INTEL Microcomputers With Interrupt

Figure 16: Full-time Parallel Interface to MC6800 or MCS650X Microprocessors

Figure 17: ICL7109-IM6100 Interface Using IM6101 PIE

Figure 18: Direct ICL7109 - INTEL 8080/8085 Interface

Figure 19: Direct ICL7109 - MC6800 Bus Interface

Handshake Mode

The handshake mode allows ready interface with a wide variety of external devices. For instance, external latches may be clocked by the rising edge of $\overline{CE/LOAD}$, and the byte enables may be used as byte identification flags or as load enables.

Figure 20 shows a handshake interface to Intel microprocessors again using an 8255PPI. The handshake operation with the 8255 is controlled by inverting its Input Buffer Full (IBF) flag to drive the SEND input to the ICL7109, and using the $\overline{CE/LOAD}$ to drive the 8255 strobe. The internal control register of the PPI should be set in MODE 1 for the port used. If the 7109 is in handshake mode and the 8255 IBF flag is low, the next word will be strobed into the port. The strobe will cause IBF to go high (SEND goes low), which will keep the enabled byte outputs active. The PPI will generate an interrupt which when executed will result in the data being read. When the byte is read, the IBF will be reset low, which causes the ICL7109 to sequence into the next byte. This figure shows the MODE input to the ICL7109 connected to a control line on the PPI. If this output is left high, or tied high separately, the data from every conversion (provided the data access takes less time than a conversion) will be sequenced in two bytes into the system.

If this output is made to go from low to high, the output sequence can be obtained on demand, and the interrupt may be used to reset the MODE bit. Note that the RUN/$\overline{HOLD}$ input to the ICL7109 may also be driven by a bit of the 8255 so that conversions may be obtained on command under software control. Note that one port of the 8255 is not used, and can service another peripheral device. The same arrangement can also be used with the 8155.

Figure 21 shows a similar arrangement with the MC6800 or MCS650X microprocessors, except that both MODE and RUN/$\overline{HOLD}$ are tied high to save port outputs.

The handshake mode is particularly convenient for directly interfacing to industry standard UARTs (such as the Intersil IM6402/6403 or Western Digital TR1602) providing a minimum component count means of serially transmitting converted data. A typical UART connection is shown on page 3. In this circuit, any word received by the UART causes

Figure 20: Handshake Interface - ICL7109 to INTEL MCS-48, -80, 85

Figure 21: Handshake Interface - ICL7109 to MC6800, MCS650X

the UART DR (Data Ready) output to go high. This drives the MODE input to the ICL7109 high, triggering the ICL7109 into handshake mode. The high order byte is output to the UART first, and when the UART has transferred the data to the Transmitter Register, TBRE (SEND) goes high and the second byte is output. When TBRE (SEND) goes high again, $\overline{\text{LBEN}}$ will go high, driving the UART DRR (Data Ready Reset) which will signal the end of the transfer of data from the ICL7109 to the UART.

Figure 22 shows an extension of the one converter - one UART scheme of the Typical Connection to several ICL7109s with one UART. In this circuit, the word received by the UART (available at the RBR outputs when DR is high) is used to select which converter will handshake with the UART. With no external components, this scheme will allow up to eight ICL7109s to interface with one UART. Using a few more components to decode the received word will allow up to 256 converters to be accessed on one serial line.

The applications of the ICL7109 are not limited to those shown here. The purpose of these examples is to provide a starting point for users to develop useful systems, and to show some of the variety of interfaces and uses of the ICL7109. Many of the ideas suggested here may be used in combination; in particular the uses of the STATUS, RUN/$\overline{\text{HOLD}}$, and MODE signals may be mixed.

Figure 22: Multiplexing Converters with Mode Input

INTERSIL

ICL8052/ICL8053
3½ Digit Pair
ICL 8052A/ICL8053A
4½ Digit Pair

FEATURES

- Accuracy high enough for ±40,000 count instruments
- Priced low enough to compete with 3½ digit DPM/DVM pairs
- One basic circuit for an entire family of DVMs
- Auto-Zero; Auto-Polarity
- 5pA input current typical
- Single reference voltage
- True ratiometric (scale factor of 1)

CONNECTION DIAGRAM

8053 Auto Zero Switch Network

8052 Analog Signal Conditioner

GENERAL DESCRIPTION

The 8052/8053 pair has been designed to "lock-in" the accuracy of a DVM and at the same time give the designer the freedom of using any output format his system requires. With reasonable care, the 0.001% linearity capability of the pair can be maintained in production instruments. The system uses time-proven dual-slope integration with all of its advantages: i.e., non-critical components, high rejection of noise and a-c signals, non-critical clock frequency and true ratiometric readings. At the same time it has reduced or eliminated many of the sources of error that have limited dual-slope accuracy. With the 8052/8053 pairs, critical board layout is no longer required to give low charge injection by the switches, and elaborate ground planes are not necessary to keep clock pulse transients out of the comparator circuitry. A further feature of these devices is that the DVM/DPM manufacturer can generate an entire family of instruments using only one basic p-c board with 2 or 3 jumper points. The family could include:

±200.0 mV Full Scale
±2.000 Volts
±400.0mV
±4.000 Volts
±800.0mV
±2.0000 Volts
±4.0000 Volts
±3.2768 Volts (16 bits in 0.1mV increments)

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
8052	0°C to +70°C	14 pin plastic DIP	ICL8052CPD
8052	0°C to +70°C	14 pin ceramic DIP	ICL8052CDD
8052A	0°C to +70°C	14 pin plastic DIP	ICL8052ACPD
8052A	0°C to +70°C	14 pin ceramic DIP	ICL8052ACDD
8053	0°C to +70°C	14 pin plastic DIP	ICL8053CPD
8053	0°C to +70°C	14 pin ceramic DIP	ICL8053CDD
8053A	0°C to +70°C	14 pin plastic DIP	ICL8053ACPD
8053A	0°C to +70°C	14 pin ceramic DIP	ICL8053ACDD

PACKAGE DIMENSIONS

14 Pin Plastic Dual-In-Line Package

14 Pin Ceramic Dual-In-Line Package

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1)	500 mW
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temperature (Soldering, 60 Sec.)	300°C

8052 ONLY

Supply Voltage	±18V
Differential Input Voltage	± 6V
Input Voltage (Note 2)	±15V
Output Short Circuit Duration, All Outputs (Note 3)	Indefinite

8053 ONLY

Source Current (I_S)	100 mA
Drain Current (I_D)	100 mA
Digital Inputs	5 mA
V^+ to V^-	25V
Digital Input	V^- to V^+

Note 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

8053 ELECTRICAL CHARACTERISTICS (V+ = +5V, V− = −15V unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8053 MIN	8053 TYP	8053 MAX	8053A MIN	8053A TYP	8053A MAX	UNITS
R_{on} Switch 1, 3 (each Switch)	$V_7 = +4.5V$ $V_6 = V_9 = V_{10} = +0.5V$		1000	2500		1000	2500	ohms
R_{on} Switch 2	Same as Switch 1, 2		2000	5000		2000	5000	ohms
R_{on} Switch 4	$V_9 = +4.5V$ $V_6 = V_7 = V_{10} = +0.5V$		1000	2500		1000	2500	ohms
R_{on} Switch 5	$V_{10} = +4.5V$ $V_6 = V_7 = V_9 = +0.5V$		1000	2500		1000	2500	ohms
R_{on} Switch 6	$V_6 = +4.5V$ $V_7 = V_9 = V_{10} = +0.5V$		1000	2500		1000	2500	ohms
Total Leakage Sw 1, 2, 5 & 6 $I_1 + I_3$ @ most positive Voltage	$V_6 = V_7 = V_9 = V_{10} = +0.5V$ $V_4 = -4V$, $V_2 = 0V$ $V_1 = V_3 = +4V$		10	50		5	20	pA
Total Leakage Sw 1, 2, 5 & 6 $I_1 + I_3$ @ most negative Voltage	$V_6 = V_7 = V_9 = V_{10} = +0.5V$ $V_4 = +4V$, $V_2 = 0V$ $V_1 = V_3 = -4V$		10	50		5	20	pA
Total Leakage Sw 3 & 4 $I_{12} + I_{13}$ @ most positive Volt.	$V_6 = V_7 = V_9 = V_{10} = +0.5V$ $V_1 = V_{11} = -4V$ $V_{12} = V_{13} = +4V$		10	50		5	20	pA
Total Leakage Sw 3 & 4 $I_{12} + I_{13}$ @ most negative Volt.	$V_6 = V_7 = V_9 = V_{10} = +0.5V$ $V_1 = V_{11} = +4V$ $V_{12} = V_{13} = -4V$		10	50		5	20	pA
Supply Current (V^+ or V^-)	$V_{6,7,9 \text{ or } 10} = 0.5V$ (each of 4 drivers)		150	300		150	300	μA
	$V_{6,7,9 \text{ \& } 10} = 4.5V$ (all drivers)		1	10		1	10	μA
Switching Time t_{on}	See Figure 1		75			75		nsec
t_{off}	See Figure 1		150			150		nsec

FIGURE 1. TURN-ON SWITCHING TIME.

TURN-OFF SWITCHING TIME.

8052 ELECTRICAL CHARACTERISTICS (V_s = ±15V unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8052			8052A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
EACH OPERATIONAL AMPLIFIER								
Input Offset Voltage	V_{CM} = 0V		20	50		20	50	mV
Input Current (either input)	V_{CM} = 0V		5	50		2	10	pA
Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
Non-Linear Component of Common-Mode Rejection Ratio*	V_{CM} = ±2V		110			110		dB
Large Signal Voltage Gain	R_L = 10kΩ	20,000			20,000			V/V
Slew Rate			6			6		V/μs
Unity Gain Bandwidth			1			1		MHz
Output Short-Circuit Current			20	100		20	100	mA
COMPARATOR AMPLIFIER								
Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
Positive Output Voltage Swing		+12	+13		+12	+13		V
Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
VOLTAGE REFERENCE								
Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
Output Resistance			5			5		ohms
Temperature Coefficient			50			40		ppm /°C
Supply Current Total			6	12		6	12	mA

*This is the only component that causes error in dual-slope converter.

SYSTEM ELECTRICAL CHARACTERISTICS

(V_{++} = +15V, V_+ = +5V, V_- = −15V Clock Frequency Set for 3 Reading/Sec)

CHARACTERISTICS	CONDITIONS	8052/8053(1)			8052A/8053A(2)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	V_{in} = 0.0V	−0.000	±0.000	+0.000	−0.0000	±0.0000	+0.0000	Digital Reading
Ratiometric Reading	$V_{in} \equiv V_{Ref.}$	+0.999	+1.000	+1.001	+0.9999	+1.0000	+1.0001	Digital Reading
Linearity over ± Full Scale (error of reading from best straight line)	$-2V \leqslant V_{in} \leqslant +2V$		0.2	1		0.5	1	Digital Count Error
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \equiv +V_{in} \approx 2V$		0.2	1		0.5	1	Digital Count Error
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 200.0mV		0.2					Digital Count
	Full scale = 2.000V		0.05			0.3		
Leakage Current into Input	V_{in} = 0V		5	30		3	10	pA
Zero Reading Drift	V_{in} = 0V $0° \leqslant T_A \leqslant 70°C$		1	5		0.5	2	μV/°C
Scale Factor Temperature Coefficient	V_{in} = +2V $0 \leqslant T_A \leqslant 70°C$ (ext. ref. 0 ppm/°C		3	15		2	5	ppm/°C

(1) Tested in 3½ digit (2,000 count) circuit shown in Fig. 5 clock frequency 12 kHz.

(2) Tested in 4½ digit (20,000 count) circuit shown in Fig. 5 clock frequency 120 kHz.

THEORY OF OPERATION

Figure 4 shows a function diagram for an A-D converter using the 8052/8053 pair. In this circuit, each measurement cycle is divided into four equal parts by the state F/F. The first part, state 00, is the auto-zero cycle. The switch driver decoder recognizes this state and turns on hex switches number 1, 2, and 3. Switches 1 and 2 impress a voltage equal to V_{REF} across the reference capacitor. Switch 3 closes a loop around the integrator and comparator. The purpose of this loop is to charge up the auto-zero capacitor until the integrator output does not change with time. During the second state, 01, switches 1, 2 and 3 are opened and switch 4 is closed. If the input voltage is zero, the buffer, integrator and comparator will see the same voltages that existed in the previous state. Thus, the integrator output will not change but will remain stationary during the entire signal-integrate cycle. If V_{IN} is not equal to zero, an unbalanced condition exists compared to the auto-zero cycle and the integrator will generate a ramp whose slope is proportional to V_{IN}. At the end of this cycle, the sign of the ramp is latched into the polarity F/F. The final cycle, reference integrate, includes states 10 and 11. The switch driver decoder uses the output of the polarity F/F in deciding whether to close switch 5 or 6. If the input signal was positive, switch 6 is closed and a voltage which is V_{REF} more negative than during auto-zero is impressed on the buffer input. If the input signal was negative switch 5 is closed and a voltage which is V_{REF} more positive than during auto-zero is impressed on the buffer input. Thus, the reference capacitor generates the equivalent of a (+) reference or a (−) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to zero. The time, or number of counts, required to do this is proportional to the input voltage. Since the reference cycle can be twice as long as the signal integrate cycle, the input voltage required to give a full scale reading $\equiv 2\ V_{REF}$. The circuit, as described to this point, is not new to this application. It has been used successfully for several years. However, this system makes three major contributions to the accuracy of this circuit. These are: (1) low charge injection, (2) junction FET op amp, and (3) zero-crossing flip-flop.

FIGURE 2.
INTEGRATOR OUTPUT NEAR ZERO-CROSSING.

1. **Low Charge Injection.**

   During auto-zero, there is no problem in charging the capacitors to the correct voltage. The problem is getting the switches off without changing this voltage. As the gate is driven off, the gate-to-drain capacitance of the switch injects a charge on the reference or auto-zero capacitor, changing its voltage. The designer, using discrete components, is forced into critical board layouts where charges of opposite polarity are injected to compensate or neutralize the driver injection. This balance will be upset by any unit-to-unit variation of switch capacitance so at best the final design is a compromise. In the 8052/8053 the critical layout has been done on the semiconductor chip and need not concern the user. Also, since a silicon-gate process is used for the switches, the unit-to-unit variation is extremely low. The net result is to give an error due to charge injection that is so low it is difficult to measure; but certainly less than 5μV referred to the input.

2. **Junction FET Op Amps.**

   Both the buffer and integrator use junction FET inputs in a guarded circuit that reduces the voltage across the FET to 3 or 4 volts. At this voltage level, input leakage currents of 1 pA are typical. For typical component values 2 pA leakege contributes less than 2 μV of error to the circuit. In theory, MOS FET's would contribute less leakage but their increased noise would swamp out any improvement by orders of magnitude.

3. **Zero-Crossing Flip Flop.**

   The problem that the zero-crossing flip-flop is designed to solve is shown in figure 2.

The integrator output is approaching the zero-crossing point where the clock will be stopped and the reading displayed. The clock pulse feedthrough superimposed upon this ramp will cause a false reading by stopping the count prematurely. For a 40,000 count instrument, the ramp is changing approximately 0.25mV per clock pulse (10 volt max integrator output divided by 40,000 counts). The clock pulses have to be less than 100μV peak to avoid causing significant errors. The circuit layout to achieve this can be time consuming at best and impossible at worst. The suggested circuit gets around this problem by feeding the zero-crossing information into a J-K flip-flop instead of using it directly. The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. Any false zero-crossing caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by one count in every instance. If a correction was not made, the display would always be one count too high. The correction is to change the four states of the converter one count early. In other words, instead of changing states at the beginning of count 0000, the states are changed at the beginning of count 9999. Since this pulse is always available as "carry" from a synchronous counter, no extra decoding is required. A bonus feature of this circuit is that latching the counter output becomes very simple with no potential race condition existing. The designer has one complete clock pulse to transfer the counter data to the latches and decouple them before a false reading will occur. The timing diagram for a signal ≈ 0 is shown in figure 3.

FIGURE 3.

FIGURE 4. FUNCTIONAL DIAGRAM FOR A/D CONVERTER.

Specific Circuits Using the 8052/8053

Figure 5 shows the complete circuit for a 4-1/2 digit (±2.000V full scale) A-D with LED readout and parallel BCD data lines. In addition to the 8052/8053, this circuit uses 6 low-cost CMOS packages for control and 5 TIL 306 as a combination LED readout, synchronous counter, and BCD latch. In this circuit, the clock runs continuously driving the 5 decade counters in the TIL 306's. The carry from the fourth decade is used to trigger the state F-F. Thus, each of the four states lasts for 10,000 counts. At the beginning of state 10, the 5th decade is cleared. None of the other counters need to be cleared since they automatically roll to 0000 at this point. When the zero-crossing F-F detects the end of the measurement, a latch pulse is initiated. The R-C time constant of this pulse is selected long enough (50nSec) to assure the latches turn on, but short enough (3μSec) to assure that the latches are decoupled before the next clock pulse. Selecting a typical time constant of 400nSec assures proper latching with wide variance in component value.

In order to give a visual indication of overload, the LED displays are blanked during state 00 if an overload exists. If overloaded, the instrument will blink a reading of 19999. A non-blinking reading of 19999 is a valid reading for the instrument.

By tying the clear terminals of the state flip-flop and the four decade counters to a common bus, the instrument can be synchronized to external events. If the bus is low, the instrument is held in auto-zero with the last measurement cycle at the beginning of state 00. The data valid pulse indicates the end of measurement cycle. For free-running condition, the bus is held high at +5 volts.

FIGURE 5. GENERAL CIRCUIT FOR A FAMILY OF DVM's.

Generating a Family of A-D Converters

In figure 5, the lines marked (MSB) and (MSB-1) are connected to Q_B and Q_A of the 4-bit state flip-flop respectively. This forces a change in state for each carry pulse (10,000 counts) from the decade counters. If the lines were moved to Q_C and Q_B respectively, two carry pulses (20,000 counts) would be required to change states. Since full-scale is two states long, the max count now becomes 40,000; (actually 39,999). Similarly if Q_D and Q_C are used the max count is now 7,999 (one less decade counter would be used in this case). The ability to easily change max count (full scale) is most useful where the A-D converter is measuring physical constants such as temperature, distances, weight, etc. It allows designer to match the digital reading of the instrument to the analog range of the transducer. Since the analog input required to generate full scale output is $2V_{REF}$ in every case, an almost endless variety of scale factors can be generated easily from one basic design. Table I summarizes how the family of DVM's is generated.

Full Scale	V_{REF}	Total Number Of Decade Counters	Connect MSB-1 to	Connect MSB to
±200.0mV	+.1000V	4	Q_A	Q_B
±2.000V	+1.000V	4	Q_A	Q_B
±400.0mV	+.2000V	4	Q_B	Q_C
±4.000V	−2.000V	4	Q_B	Q_C
±800.0mV	+.4000V	4	Q_C	Q_D
±2.0000V	+1.0000V	5	Q_A	Q_B
±4.0000V	−2.0000V	5	Q_B	Q_C
±3.2768V	+1.6384V	4*	Q_C	Q_D

*Number of 4-bit binary counters

TABLE I

FIGURE 6. 16-BIT BINARY CONVERTER

Specific circuits demonstrating this principle are shown in figures 5 and 6. An 800.0mV full scale A-D can be obtained from the 2.0000V instrument shown in figure 5 with the three following modifications:

1. Delete middle LED counter.
2. State decode moved to Q_D and Q_C,
3. Reference voltage adjusted to 0.4000V.

Figure 6 is the specific circuit for a 16-bit binary A-D. Here the decade counters and displays have been replaced by synchronous 4-bit counters and latches. To give a full scale reading of ±3.2768 volts the reference is adjusted to 1.6384 volts.

Figure 7 shows the circuit for a 40,000 count instrument. This circuit conforms to all of the "family" rules with the exception that it uses a −2.0000 volt reference. If a positive reference was used, pin 3 of the 8053 would have to swing to +6V (+4 volt input +2 volt reference). Since this exceeds the +5 volt supply, the switch would forward bias into the substrate. It can easily accommodate the +2 to −6 volt swing required of a negative reference. The only change required by a negative reference is that the drive to pin 6 (+ Reference driver) and pin 10 (− Reference driver) be interchanged. Also since the internal reference is not used, no connections are made to pins 3, 6, and 7 of the 8052.

FIGURE 7. 4¾ DIGIT DVM

Alternate Circuits

In a 4½ digit (20,000 count) instrument where the family generating capabilities of the four bit counter is not required, a dual D flip-flop can be substituted for this function with some reduction in parts costs. Also a "±1" LED, driven by a dual D flip-flop, can replace the fifth TIL306. Figure 8 shows a circuit with these two substitutions made.

If the Parallel BCD capabilities of the TIL306 are not required, a further reduction in parts cost can be achieved by using the circuit of figure 9. In this circuit the MM74C926 performs the counting, latch and 7 segment decode function of the TIL306 such that it can be used with any LED displays. Some modification of the clock and latch circuit is required since the 74C926 uses a ripple counter with a carry at 0000 instead of a synchronous carry at 9999. When a zero-crossing signal is detected and the latch-enable is initiated, a signal is simultaneously fed to the clock drive circuitry to delay the clock and therefore the count until the previous count can be latched. The latch time-constant is shorter than the clock-delay time-constant to assure that the latch is transferred and disabled before the clock resumes counting. A 1μS time delay in the output of the clock driver assures that the slight delay (100nS) between the clock pulse and the clock-delay pulse does not clock the counter. Blanking is provided to give a visual indication of overload. However, the display will flash .0000 instead of 1.9999 due to the nature of the ripple counter.

FIGURE 8. 4½ DIGIT DVM (PARALLEL BCD)

Component Selection

Except for the Reference Voltage, none of the component values are first-order important in determining the accuracy of the instrument. While this is undoubtedly an advantage of this approach, it does make the selection of nominal component values arbitrary at best. For instance the reference capacitor and auto-zero capacitor are each shown as 1.0μF. These relative large values are selected to give greater immunity to PC board leakage since much smaller capacitors are adequate for charge injection errors or leakage errors from the 8052/8053. The ratio of integrating resistor and capacitor is selected to give 9 volt swing for full scale inputs. This is a compromise between possibly saturating the integrator (at ±14 volts) due to tolerance build-up between the resistor, capacitor and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. Again the .22 value for integrating cap is selected for PC considerations alone since the very small leakage at the integrator input is nulled at auto-zero. A very important characteristic of the integrating cap is low dielectric absorption. A polypropylene cap (made by TRW) gave excellent results in the application. In fact a good test for dielectric absorption is to test the subject cap in this circuit with the input tied to reference. This ratiometric condition should read 1.0000 and any deviation is probably due to dielectric absorption. In this test poly-carbonate caps typically read .9992, polystyrene, .9997 and polypropylene, 1.0000. The increased temperature coefficient of polypropylene is of no consequence in this circuit. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

FIGURE 9. 4½ DIGIT DVM (20,000 COUNT MULTIPLEXED DISPLAY)

The output of the comparator is clamped to the +5 volts supply to prevent the positive swing of the comparator from forward biasing the auto-zero switch to its substrate and injecting minority carriers that would be collected as leakage currents. In addition, a voltage translation network connects the output of the comparator to the auto-zero switch. The purpose of this network is to assure that, during auto-zero, the output of the comparator is at or near the threshold of the CMOS logic (+2.5V) while the auto-zero cap is being charged to V_{REF} (+1V in the case of 2.0000 instrument). Otherwise even with zero signal in, some reference integrate period would be required to drive the comparator output to the threshold region. This would show up as an equivalent offset error. Once the divider chain has been selected, the unit-to-unit variation should contribute less than a few tenths-of-a-count error in the worse case (40,000 count instrument) and proportionately less in other instruments. For a 3½ digit instrument, the error is unmeasurable.

Finally, the back-to-back diodes are used to lower noise. In the normal operating mode they offer a high impedance and long integrating time constant to any noise pulses charging the auto-zero cap. At start-up or recovery from an overload, their impedance is low to large signals so the cap can be charged in one auto-zero cycle.

Max Clock Frequency

The maximum conversion rate of most dual-slope A-D converters is limited by the frequency response of the comparator. Even though the comparator in this circuit is all NPN with an open-loop gain-bandwidth product of 300MHz, it is no exception. The comparator output follows the integrator ramp with a 3μS delay. At a clock frequency of 160kHz (6μS period) half of the first reference integrate period is lost in delay. This means that the meter reading will change from 0 to 1 with 50μV in, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at midpoint is considered desirable by most users. However, if the clock frequency is increased appreciably above this, the instrument will flash "1" on noise peaks even when the input is shorted.

Some circuits use positive feedback or a latch to solve the delay problem. However, unless the comparator voltage swing, the comparator gain, and the integrator gain are carefully controlled, this circuit can generate *anticipation* errors that greatly exceed the 3μS *delay* error. Also it is very susceptible to noise spikes. A more controlled approach for extending the conversion rate is the use of a small resistor in the integrator feedback loop. This feeds a small pulse to the comparator to get it moving quickly, and partially compensate for its delay.

The minimum clock frequency is established by leakage on the auto-zero and reference cap. With most devices, measurement cycles as long as 10 seconds gave no measurable leakage error.

INTERSIL

LD110, LD111
3-1/2 Digit A/D Converter Set

LD114
Multiple-Option Digital Processor

FEATURES

- Accuracy 0.05% Of Reading ±1 Count
- Two Voltage Ranges – 1.999 V and 199.9 mV
- Sampling Rates up to 12 Samples/Second
- FET Input for $Z_{in} > 1000\ M\Omega$
- Auto-Zero Minimizes Effects of Offset, Drift and Temperature
- Auto-Polarity
- Multiplexed Parallel BCD or Serial BCD Output (LD114)
- Active High or Active Low Logic Outputs (LD114)
- Overrange and Underrange Signals Available for Auto-Ranging Capability.
- ÷512 Output Available for Phase Locked Loop Clock (LD114)
- TTL Compatible Outputs

GENERAL DESCRIPTION

The monolithic LD111 analog processor contains a bipolar comparator, a bipolar integrating amplifier, two MOS-FET input unity gain amplifiers, several P-channel enhancement mode analog switches and the necessary level shifting drivers to allow the analog and digital processors to be directly interfaced. A wide range of conversion rates (1/3 to 12 samples per second) as well as two voltage ranges can be accommodated using externally determined RC time constants. All amplifiers are internally compensated.

The PMOS LD110/LD114 synchronous digital processor combines the counting, storage and data multiplexing functions with the random logic necessary to control the quantized charge-balancing function of the analog processor. Seventeen static latches store the 3½ digits of BCD data as well as overrange, underrange and polarity information.

In the LD110, nine push-pull output buffers (capable of driving one standard TTL load each) provide the sign, digit strobe and multiplexed BCD data outputs, all of which are active high. The digit scan is an interlaced format of digits 1, 3, 2, and 4.

In the LD114, ten push-pull output buffers (capable of driving one standard TTL load) provide the clock frequency ÷512, sign, digit strobe and multiplexed BCD data. Four data output format options allow the user to tailor the BCD output to his circuit requirements.

LD111 ANALOG PROCESSOR

TOP VIEW

LD110 DIGITAL PROCESSOR

TOP VIEW

LD114 DIGITAL PROCESSOR

TOP VIEW

ABSOLUTE MAXIMUM RATINGS

V_{IN} . . . . . ±5.0V
$V_1 - V_2$ (LD111) 30V
V_{SS} 6V
$V_{SS} - V_2$ (LD110/LD114) 20V
Voltage on any pin relative to V_{SS} (LD114) 0.3 V to -20V
V_{REF} . . . . . V_1

Operating Temperature . . . . . 0 to 70°C
Storage Temperature . . . . . -65 to 150°C
Power Dissipation (Package, LD110/LD111*. . 750 mW
Power Dissipation (Package, LD114)* . . . . 1200 mW

*Device mounted with all leads welded or soldered to PC Board, Derate 6.3 mW/°C above 25°C.

ELECTRICAL CHARACTERISTICS V_1 = 12 V, V_2 = -12 V, V_{SS} = 5 V V_{REF} = 8.2 V. T_A = 25°C

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
INPUT	Clock Frequency	f_{IN}	50% Duty Cycle		30.7		KHz
	Input Bias Current	I_{IN}	T_A = 25° C		4		pA
			T_A = 70° C		40		
	Normal Mode Rejection	NMR	f_L = 60 Hz		40		dB
	Clock Input Current, Low	I_{CL}	V_{CLOCK} in = 0.4 V			-500	µA
	Comparator	I_{INL}	V_{INL} = -12 V			-100	
	Latch Inhibit	I_{INL}	V_{INL} = -12 V		180	-600	
	Format Option Inputs	I_{INH}	V_{INH} = V_{SS}		25	400	
OUTPUT	Measure/Zero Voltage, Low	V_{OL1}	I_{OL} = 150 µA			0.4	V
	Measure/Zero Voltage, High	V_{OH1}	I_{OH} = -200 µA	2.4			
	Up/Down Logic Voltage, Low	V_{OL2}	I_{OL} = 250 µA			0.4	
	Up/Down Logic Voltage, High	V_{OH2}	I_{OH} = -200 µA	2.4			
	Digits, Bits, Sign Voltage, ÷512*	V_{OL3}	I_{OL} = 1.6 mA			0.4	
	Analog Comparator Voltage	V_{OH3}	I_{OH} = -100 µA	2.4			
	Data Bit Voltage, High	V_{OH4}	I_{OH} = -200 µA	2.4			
	Digits, Sign Voltage, ÷512*	V_{OH5}	I_{OH} = -800 µA	2.4			
SWITCH	ON Resistance, Auto Zero Switch	$r_{DS(on)}$	$V_{AZ(in)}$ = -4.0 V, I_S = -50 µA		11	50	KΩ
	ON Resistance, Up/Down Switch	$r_{DS(on)}$	I_S = 1 mA		650	3000	Ω
	Up/Down Switch Temperature Coefficient	TC			0.20	0.50	%/°C
SUPPLY	Supply Current, LD111	I_1			2.2	3.5	mA
	Supply Current, LD111	I_{2A}			-1.8	-3.0	
	Supply Current, LD110/114	I_{2D}			-17	-23	
	Supply Current, LD110/114	I_{SS}			17.4	24	
	Power Supply Rejection Ratio, V_1	$PSRR_1$		80	85		dB
	Power Supply Rejection Ratio, V_2	$PSRR_2$		60	65		
	Reference Current Rejection Ratio		R_{REF} = R_2 = 100KΩ, V_{IN} = 2V	35	41		nA/LSB

*÷512 output applicable to LD114 only

INPUT/OUTPUT SCHEMATICS

OUTPUT BUFFERS
(Digits, Bits, Sign, 512, M/Z, U/D)

COMPARATOR, CLOCK, LATCH INHIBIT INPUTS

FORMAT OPTION INPUTS
(Bit Phase, Digit Phase, Scan, Serial Bits)

DESCRIPTION OF PIN FUNCTIONS (LD110/LD114)

V_{SS} – Positive Supply Voltage. Recommended level is +5 volts ±10%.

V_2 – Negative Supply Voltage. Recommended level is -12 volts ±10%.

CLOCK IN – This input accepts a TTL or MOS level clock to drive the synchronous digital circuitry. Acceptable duty cycles on the external clock range from 30% high, 70% low to 70% high, 30% low for clock frequencies from 2 kHz to 75 kHz. Although any clock frequency between 2 kHz and 75 kHz may be used, clock frequencies that are integer divisions of $2048F_L$($F_{IN} = 2048F_L/n$, n = 1, 2, 3, 4, 5, F_L = Line Frequency) provide measure and zero periods that are integer multiples of the line frequency period ($T_{zero} = n/F_L$, $T_{measure} = 2n/F_L$). Line frequency interference is minimized by the selection of one of these 50 frequencies.

This input has an active pull-up to V_{SS}.

M/Z – Measure/Zero Logic Output. This 0 to 5 volt logic output successively provides Autozero and Measurement intervals of 2048 and 4096 clock periods respectively. This output is compatible with CMOS logic and directly interfaces with the LD111 analog processor.

÷512 (LD114) – This TTL compatible output (1 standard load) provides the necessary clock frequency division for a phase locked loop digital clock. The line frequency rejection will be held at the maximum level (>80 dB) when locked to the line frequency.

U/D – Up/Down Logic Output. This output has logic levels of 0 to +5 volts to provide pulse-width modulation of the reference current when used with the LD111 analog processor. This output is CMOS compatible.

COMP – Analog Comparator Input. This input has an active pull-up to V_{SS} for a comparator "high" state. This pin must be pulled down to V_2 for a "low" comparator state.

An End-of-Conversion Signal can be decoded from the three interconnecting logic lines (M/Z, U/D, Comp) using the following CMOS logic.

$\overline{M/Z + U/D + Comp}$ = E.O.C.

SIGN – Sign of Analog Input Polarity. This TTL level output is a static signal which is either 0 or V_{SS} for a negative or positive input polarity respectively.

BIT PHASE (*LD114) – The bit outputs will be active high (positive) logic if this pin is left open or connected to V_2. The application of V_{SS} to this pin will give a complemented output (negative logic).

DIGIT PHASE (*LD114) – The Digit Strobe outputs will be of positive logic if this pin is left open or connected to V_2 (an active pull-down is internally connected to V_2). Applying V_{SS} to this pin will complement the outputs to give negative logic. Negative logic may simplify interfacing with Common Anode LED, Gas Discharge and Liquid Crystal Displays.

B_1, B_2, B_3, B_4 – BCD Data Bit Output. B_4 represents the most significant bit and B_1 the least significant bit of the BCD output. Bit 4 of digit 4 goes high for an underrange condition (less than 100 counts). These outputs are compatible with 1 standard TTL load.

MUX Underrange = $B_4 \cdot D_4$ (5% of full scale)

D_1, D_2, D_3, D_4 – Digit Strobe Outputs. D_4 is the most significant and D_1 the least significant digit of the 3½ digit output. The digit strobes are each selected in turn when the BCD data bits for that digit appear at the bit outputs.

MUX Overrange = $\overline{D_1 + D_2 + D_3 + D_4}$ (100% of full scale, count ≥2000).

SCAN (*LD114) – Sequential/Interlace Digit Scan. The digit strobe format will be an interlaced format of digits 1, 3, 2 and 4 if this pin is left open or is connected to V_2. This format is useful for display digits packaged two to an envelope and which require an interdigit blanking period eg. (Beckman Displays). By alternating from envelope, an interdigit blanking period is effectively provided.

The application of V_{SS} to this pin will give a sequential scan of digits 1, 2, 3 and 4. This format may be more useful in interfacing with data acquisition equipment.

LATCH INHIBIT (*LD114) – Connecting this pin to V_2 will prevent updating of the internal static latches, thus providing a "hold" function. Leaving this pin disconnected will allow the latches to be updated once each sampling period.

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DESCRIPTION OF PIN FUNCTIONS (LD110/LD114) Cont.

SERIAL BITS (*LD114)—Parallel/Serial Bit Output Format. The BCD data bits for each digit will appear simultaneously with the digit strobe if the parallel bit option is selected.

This format is useful for driving multiplexed displays. The parallel bit format is available when this pin is left open or connected to V_2.

The application of V_{SS} to this pin will put all of the BCD data bits in a serial order at the bit 4 output.

Bit outputs 1, 2, and 3 contain time markers to identify the data. The most significant bit of the last digit (D_4) is identified by a marker at the bit 2 output. The least significant bit of the first Digit (D_1) is identified by a marker at bit 3. Bit 1 shows a marker for the least significant bit of each digit.

All output format options are independent of one another (i.e., the serial bit output can have either sequential or interlace scan, Positive or Negative logic).

(*For LD110, action is described for "pin left open".)

DESCRIPTION OF PIN FUNCTIONS – LD111

BUF OUT – The output of this unity gain input buffer amplifier is applied to the integrator summing node through a scaling resistor R_2. The value of this resistor is typically 10 KΩ for a 200.0 mV full-scale and 100 KΩ for a 2.000 V full-scale. The digital output is inversely proportional to the value of this resistor,

$$\text{Count} = \frac{V_{IN}}{V_{REF}} \frac{R_1}{R_2} 8192$$

HI-QUALITY GND – This pin, typically connected to a High Quality Ground point for single ended inputs **CAN BE USED AS THE INVERTING INPUT FOR DIFFERENTIAL SIGNALS.** The digital output will be V_{IN} - V_{HI} - Q. When using this differential mode, it is important that resistor R_3 equal Resistor R_2 for proper operation.

M/Z – Measure/Zero Logic Input. Internal level shifting drivers operate the PMOS switches in response to this digital signal.

U/D – Up/Down Logic Input. The logic signal applied to this pin operates a SPDT switch to provide Quantized pulses of charge to the integrator.

COMP – This analog comparator output is an open collector configuration which goes to V_2 when "low."

V_2 – Negative Supply Voltage. Recommended level is -12 V ±10%.

GND – Analog Processor Ground.

REF_{out} – This voltage output of the SPDT U/D switch, converted to a current by resistor R_1, supplies the reference current to the integrator.

INT. IN – Integrator Summing Node.

V_{REF} – A stable positive reference voltage (5 to 11 V) applied to this pin is the standard to which the input voltage V_{IN} is measured. Ratio measurements can be made by applying a variable to this input (1.0 to 11V).

INT. OUT – The output of the integrating amplifier is made available for application to the Auto-Zero amplifier by means of resistor R_4.

AZ OUT – The output of the unity gain Auto-Zero Amplifier provides a second negative reference current to the integrator through resistor R_3.

AZ FILTER – The RC filter (R_5 and C_{STRG}) connected to this pin stores. D.C. voltage components to balance amplifier offset and drift components.

AZ IN – This input is switched into the AZ filter during the Zeroing interval.

V_{IN} – Analog Voltage Input. The A/D System digitizes the voltage appearing at this input.

V_1 – Positive Supply Voltage. The recommended level is +12 volts ±10%.

APPLICATIONS LD111/LD114

3½ Digit DVM (±200.0 mV)

APPLICATIONS LD110/LD111

3½ Digit DVM (±2.000 Volts)

ORDERING INFORMATION

PART	TEMP. RANGE	PACKAGE	ORDER NO.
LD110	0°C to 70°C	16 lead DIP ceramic	LD110 CP
LD110	0°C to 70°C	16 lead DIP plastic	LD110 CJ
LD111	0°C to 70°C	16 lead DIP ceramic	LD111 CP
LD111	0°C to 70°C	16 lead DIP plastic	LD111 CJ
LD114	0°C to 70°C	28 lead DIP ceramic	LD114 CR

PACKAGE DIMENSIONS

16 PIN CERAMIC PACKAGE

16 PIN DIP PACKAGE

28 LEAD DUAL-IN-LINE PACKAGE (SIDE BRAZE)

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INTERSIL

AD7520/AD7530
AD7521/AD7531
10 & 12 Bit Monolithic Multiplying D/A Converters

FEATURES

- **AD7520 (AD7530): 10 Bit Resolution; 8, 9 and 10 Bit Linearity**
- **AD7521 (AD7531): 12 Bit Resolution; 8, 9 and 10 Bit Linearity**
- **Low Power Dissipation: 20 mW (Max)**
- **Low Nonlinearity Tempco: 2 PPM of FSR/°C (Max)**
- **Current Settling Time: 500 nS to 0.05% of FSR**
- **Supply Voltage Range: +5V to +15V**
- **DTL/TTL/CMOS Compatible**
- **Full Input Static Protection**
- **883B Processed Versions Available**

GENERAL DESCRIPTION

The AD7520 (AD7530) and AD7521 (AD7531) are monolithic, high accuracy, low cost 10-bit and 12-bit resolution, multiplying digital-to-analog converters (DAC). INTERSIL thin-film on CMOS process enables up to 10-bit accuracy with DTL/TTL/CMOS compatible operation. Digital inputs are fully protected against static discharge by compensating diodes to ground and positive supply.

Typical applications for the AD7520 (7530) and AD7521 (7531) include: digital/analog interfacing, multiplication and division; programmable power supplies; CRT character generation; digitally controlled gain circuits, integrators and attenuators, etc.

The AD7530 and AD7531 are identical to the AD7520 and AD7521, respectively, with the exception of output leakage current and feedthrough specifications.

FUNCTIONAL DIAGRAM

(Switches shown for Digital Inputs "High")

CHIP TOPOGRAPHY

PACKAGE IDENTIFICATION

Suffix D: Cerdip package
Suffix N: Plastic DIP package

ORDERING INFORMATION

Nonlinearity	Temperature Range 0°C to +70°C	−25°C to +85°C	−55°C to +125°C
0.2% (8-Bit)	AD7520JN AD7530JN AD7521JN AD7531JN	AD7520JD AD7530JD AD7521JD AD7531JD	AD7520SD AD7521SD
0.1% (9-Bit)	AD7520KN AD7530KN AD7521KN AD7531KN	AD7520KD AD7530KD AD7521KD AD7531KD	AD7520TD AD7521TD
0.05% (10-Bit)	AD7520LN AD7530LN AD7521LN AD7531LN	AD7520LD AD7530LD AD7521LD AD7531LD	AD7520UD AD7521UD

PIN CONFIGURATION

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ABSOLUTE MAXIMUM RATINGS (T_A = 25° C unless otherwise noted)

VDD (to GND) ..... +17V
VREF (to GND) ..... ±25V
Digital Input Voltage Range ..... VDD to GND
Output Voltage Compliance ..... −100mV to VDD
Power Dissipation (package)
up to +75° C ..... 450 mW
derates above +75° C by ..... 6 mW/° C

Operating Temperatures
JN, KN, LN Versions ..... 0° C to +70° C
JD, KD, LD Versions ..... −25° C to 85° C
SD, TD, UD Versions ..... −55° C to +125° C
Storage Temperature ..... −65° C to +150° C

CAUTION: 1) The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2) Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.

SPECIFICATIONS (VDD=+15V, VREF=+10V, TA=25° C unless otherwise specified)

PARAMETER	AD7520 (AD7530)	AD7521 (AD7531)	UNITS	LIMIT	TEST CONDITIONS	FIG.
DC ACCURACY (Note 1) Resolution	10	12	Bits			
Nonlinearity J S	0.2 (8-Bit)		% of FSR	Max	S, T, U: over −55° C to +125° C	1
K T	0.1 (9-Bit)		% of FSR	Max		1
L U	0.05 (10-Bit)		% of FSR	Max	−10V≤VREF≤+10V	1
Nonlinearity Tempco	2		PPM of FSR/° C	Max		
Gain Error (Note 2)	0.3		% of FSR	Typ	−10V≤VREF≤+10V	
Gain Error Tempco (Note 2)	10		PPM of FSR/° C	Max		
Output Leakage Current (either output)	200 (300)		nA	Max	Over the specified temperature range	
Power Supply Rejection	±0.005		% of FSR/%	Typ		2
AC ACCURACY Output Current Settling Time	500		nS	Typ	To 0.05% of FSR (All digital inputs low to high and high to low)	6
Feedthrough Error	10		mV pp	Max	VREF = 20V pp, 100 KHz (50KHz) All digital inputs low	5
REFERENCE INPUT Input Resistance (Note 3)	5K		Ω	Min	All digital inputs high. I_{OUT1} at ground.	
	10K			Typ		
	20K			Max		
ANALOG OUTPUT Voltage Compliance (both outputs)	See absolute max. ratings					
Output Capacitance	I_{OUT1} 120 I_{OUT2} 37		pF pF	Typ Typ	All digital inputs high	4
	I_{OUT1} 37 I_{OUT2} 120		pF pF	Typ Typ	All digital inputs low	4
Output Noise (both outputs)	Equivalent to 10KΩ Johnson noise			Typ		3
DIGITAL INPUTS Low State Threshold	0.8		V	Max	Over the specified temp range	
High State Threshold	2.4		V	Min		
Input Current (low to high state)	1		μA	Typ		
Input Coding	Binary/Offset Binary				See Tables 1 & 2 on pages 4 and 5	
POWER REQUIREMENTS Power Supply Voltage Range	+5 to +15		V			
IDD	5		nA	Typ	All digital inputs at GND	
	2		mA	Max	All digital inputs high or low	
Total Power Dissipation (Including the ladder)	20		mW	Typ		

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Ladder and feedback resistor Tempco is approximately −150ppm/° C.

Specifications subject to change without notice.

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TEST CIRCUITS

NOTE: The following test circuits apply for the AD7520. Similar circuits can be used for the AD7530, AD7521 and AD7531.

Figure 1. Nonlinearity

Figure 2. Power Supply Rejection

Figure 3. Noise

Figure 4. Output Capacitance

Figure 5. Feedthrough Error

Figure 6. Output Current Settling Time

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of (2^{-n}) (V_{REF}). A bipolar converter of n bits has a resolution of $[2^{-(n-1)}]$ $[V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

GENERAL CIRCUIT INFORMATION

The AD7520 (AD7530) and AD7521 (AD7531) are monolithic, multiplying D/A converters. Highly stable thin film R-2R resistor ladder network and NMOS DPDT switches form the basis of the converter circuit. CMOS level shifters also enable low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 7. The NMOS DPDT switches steer the ladder leg currents between IOUT1 and IOUT2 busses which must be held at ground potential or virtual ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.

(Switches shown for Digital Inputs "High")

Figure 7. 7520 (7521) Functional Diagram

Converter errors are further eliminated by using separate metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 8). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder DPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors, resulting in accurate leg currents.

Figure 8. CMOS Switch

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APPLICATIONS

UNIPOLAR BINARY OPERATION

The circuit configuration for operating the AD7520 (AD7530) and AD7521 (AD7531) in unipolar mode is shown in Figure 9. With positive and negative VREF values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1.

Figure 9. Unipolar Binary Operation (2-Quadrant Multiplication)

Zero Offset Adjustment

1. Connect all AD7520 (AD7530) or AD7521 (AD7531) digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0 V ± 1 mV at VOUT.

Gain Adjustment

1. Connect all AD7520 (AD7530) or AD7521 (AD7531) digital inputs to VDD.
2. Monitor VOUT for a $-V_{REF}(1-2^{-n})$ reading. (n=10 for AD7520 (AD7530) and n=12 for AD7521 (AD7531)).
3. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

TABLE 1

CODE TABLE — UNIPOLAR BINARY OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}(1-2^{-n})$
1000000001	$-V_{REF}(1/2+2^{-n})$
1000000000	$-V_{REF}/2$
0111111111	$-V_{REF}(1/2-2^{-n})$
0000000001	$-V_{REF}(2^{-n})$
0000000000	0

NOTE: 1. LSB = 2^{-n} V_{REF} 2. n=10 (12) for 7520 (7521) 7530 (7531)

(APPLICATIONS, Cont'd.)

BIPOLAR (OFFSET BINARY) OPERATION

The circuit configuration for operating the AD7520 (AD7530) or AD7521 (AD7531) in the bipolar mode is given in Figure 10. Using offset binary digital input codes and positive and negative reference voltage values 4-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

Figure 10. Bipolar Operation (4-Quadant Multiplication)

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to IOUT1 bus. A "Logic 0" input forces the bit current to IOUT2 bus. For any code the IOUT1 and IOUT2 bus currents are complements of one another. The current amplifier at IOUT2 changes the polarity of IOUT2 current and the transconductance amplifier at IOUT1 output sums the two currents. This configuration doubles the output range but halves the resolution of the DAC. The difference current resulting at zero offset binary code, (MSB="Logic 1", All other bits="Logic 0), is corrected by using an external resistor, (10 Megohm), from VREF to IOUT2.

Offset Adjustment

1. Adjust VREF to approximately +10 V.
2. Connect all digital inputs to "Logic 1"
3. Adjust IOUT2 amplifier offset zero adjust trimpot for 0V±1 mV at IOUT2 amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust IOUT1 amplifier offset zero adjust trimpot for 0V±1 mV at VOUT.

Gain Adjustment

1. Connect all AD7520 (AD7530) or AD7521 (AD7531) digital inputs to VDD.
2. Monitor VOUT for a -VREF ($1-2^{-(n-1)}$ volts reading. (n=10 for AD7520 (AD7530) and n=12 for AD7521 (AD7531)).
3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

TABLE 2
CODE TABLE — BIPOLAR (OFFSET BINARY) OPERATION

DIGITAL INPUT	ANALOG OUTPUT
1111111111	$-V_{REF}(1-2^{-(n-1)})$
1000000001	$-V_{REF}(2^{-(n-1)})$
1000000000	0
0111111111	$V_{REF}(2^{-(n-1)})$
0000000001	$V_{REF}(1-2^{-(n-1)})$
0000000000	V_{REF}

NOTE: 1. LSB = $2^{-(n-1)}$ V_{REF} **2.** n = 10(12) for 7520 (7521) 7530 (7531)

POWER DAC DESIGN USING AD7520

Figure 11. The Basic Power DAC

A typical power DAC designed for 8 bit accuracy and 10 bit resolution is shown in Figure 11. INTERSIL IH8510 power amplifier (1 Amp continuous output with up to +25 V) is driven by the AD7520.

A summing amplifier between the AD7520 and the IH8510 is used to separate the gain block containing the AD7520 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise AD7520 can be directly connected to the IH8510, by using a 25 volts reference for the DAC.

An important note on the AD7520/101A interface concerns the connection of pin 1 of the DAC and pin 2 of the 101A. Since this point is the summing junction of an amplifier with an AC gain of 50,000 or better, stray capacitance should be minimized; otherwise instabilities and poor noise performance will result. Notice that the output of the 101A is fed into an inverting amplifier with a gain of -3, which can be easily changed to a non-inverting configuration. (For more information write for: INTERSIL Application Bulletin A021-Power D/A Converters Using The IH8510 by Dick Wilenken.)

(APPLICATIONS, Cont'd.)

ANALOG/DIGITAL DIVISION

With the AD7520 connected in its normal multiplying configuration as shown in figure 15, the transfer function is

$$V_O = -V_{IN}\left(\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}\right)$$

where the coefficients A_x assume a value of 1 for an ON bit and 0 for an OFF bit.

By connecting the DAC in the feedback of an operational amplifier, as shown in Figure 12, the transfer function becomes

$$V_O = \left(\frac{-V_{IN}}{\frac{A_1}{2^1} + \frac{A_2}{2^2} + \frac{A_3}{2^3} + \cdots \frac{A_n}{2^n}}\right)$$

This is division of an analog variable (V_{IN}) by a digital word. With all bits off, the amplifier saturates to its bound, since division by zero isn't defined. With the LSB (Bit-10) ON, the gain is 1023. With all bits ON, the gain is 1 (±1 LSB).

Figure 12. Analog/Digital Divider

PACKAGE DIMENSIONS

16 PIN CERDIP

16 PIN PLASTIC DIP

BONDING DIAGRAM

18 PIN CERDIP

18 PIN PLASTIC DIP

BONDING DIAGRAM

1. Lead no. 1 identified by dot or notch.
2. Dimensions in inches (millimeters).

INTERSIL

AD7523
8 Bit Monolithic Multiplying A/D Converters

FEATURES

- 8, 9 and 10 bit linearity
- Low gain and linearity Tempcos
- Full temperature range operation
- Full input static protection
- DTL/TTL/CMOS compatible
- +5 to +15 volts supply range
- Fast settling time: 100 nS
- Four quadrant multiplication
- 883B Processed versions available

GENERAL DESCRIPTION

The Intersil AD7523 is a monolithic, low cost, high performance, 10 bit accurate, multiplying digital-to-analog converter (DAC), in a 16-pin DIP.

Intersil's thin-film resistors on CMOS circuitry provide 8-bit resolution (8, 9 and 10-bit accuracy), with DTL/TTL/CMOS compatible operation.

Intersil AD7523's accurate four quadrant multiplication, full military temperature range operation, full input protection from damage due to static discharge by clamps to V+ and GND and very low power dissipation make it a very versatile converter.

Low noise audio gain control, motor speed control, digitally controlled gain and attenuators are a few of the wide number of applications of the 7523.

FUNCTIONAL DIAGRAM

(Switches shown for Digital Inputs "High")

PIN CONFIGURATION

ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0°C to +70°C	-25°C to +85°C	-55°C to +125°C
0.2% (8 Bit)	AD7523JN	AD7523AD	AD7523SD
0.1% (9 Bit)	AD7523KN	AD7523BD	AD7523TD
0.05% (10 Bit)	AD7523LN	AD7523CD	AD7523UD

PACKAGE IDENTIFICATION

SUFFIX D: CERDIP PACKAGE
SUFFIX N: PLASTIC PACKAGE

4

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

VDD (to GND) ..... +17V
VREF (to GND) ..... ±25V
Digital Input Voltage Range ..... −0.3 to VDD
Output Voltage Compliance ..... −0.3 to VDD
Power Dissipation (package)
Plastic
up to +70°C 670mW
derates above +70°C by ..... 8.3mW/°C
Ceramic
up to 75°C 450mW
derates above 75°C by ..... 6mW/°C
Operating Temperatures
JN, KN, LN Versions ..... 0°C to +70°C
AD, BD, CD Versions ..... −25°C to +85°C
SD, TD, UD Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

CAUTION: 1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2. Do not apply voltages higher than VDD and lower than GND to any terminal except VREF.

SPECIFICATIONS (VDD = +15V, VREF = +10V unless otherwise specified)

PARAMETER		TA +25°C	TA MIN-MAX	UNITS	LIMIT	TEST CONDITIONS
DC ACCURACY (Note 1)						
Resolution		8	8	Bits	Min	
Nonlinearity (Note 2)	(±1/2 LSB)	±0.2	±0.2	% of FSR	Max	
	(±1/4 LSB)	±0.1	±0.1	% of FSR	Max	−10V ≤ VREF ≤ +10V
	(±1/8 LSB)	±0.05	±0.05	% of FSR	Max	$V_{OUT1} = V_{OUT2} = 0V$
Monotonicity		Guaranteed				
Gain Error (Note 2)		±1.5	±1.8	% of FSR	Max	Digital inputs high.
Nonlinearity Tempco (Note 2 and 3)		2		PPM of FSR/°C	Max	−10V VREF +10V
Gain Error Tempco (Note 2 and 3)		10		PPM of FSR/°C	Max	
Output Leakage Current (either output)		±50	±200	nA	Max	$V_{OUT1} = V_{OUT2} = 0$
AC ACCURACY (Note 3)						
Power Supply Rejection (Note 2)		0.02	0.03	% of FSR/%	Max	V_{DD} = 14.0 to 15.0V
Output Current Settling Time		150	200	nS	Max	To 0.2% of FSR, R_L = 100Ω
Feedthrough Error		±1/2	±1	LSB	Max	VREF = 20V pp, 200KHz sine wave. All digital inputs low.
REFERENCE INPUT		5K		Ω	Min	
Input Resistance (Pin 15)		20K		Ω	Max	All digital inputs high. I_{OUT1} at ground.
Temperature Coefficient (Note 3)		−500		ppm/°C	Max	
ANALOG OUTPUT (Note 3)						Both outputs.
Voltage Compliance (Note 4)		−100mV to V_{DD}				See maximum ratings.
Output Capacitance	C_{OUT1}	100		pF	Max	All digital inputs high (VINH)
	C_{OUT2}	30		pF	Max	
	C_{OUT1}	30		pF	Max	All digital inputs low (VINL)
	C_{OUT2}	100		pF	Max	
DIGITAL INPUTS						
Low State Threshold (VINL)		0.8		V	Max	Guarantees DTL/TTL and CMOS (0.5
High State Threshold (VINH)		2.4		V	Min	max, 14.5 min) levels
Input Current (per input)		±1		μA	Max	V_{IN} = 0V or +15V
Input Coding		Binary/Offset Binary				See Tables 1 & 2
Input Capacitance (Note 3)		4		pF	Max	
POWER REQUIREMENTS						Accuracy is tested and guaranteed at
Power Supply Voltage Range		+5 to +16		V		V_{DD} = +15V, only.
IDD		100		μA	Max	All digital inputs low or high.

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

Specifications subject to change without notice.

APPLICATIONS
UNIPOLAR OPERATION

Figure 1. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
11111111	$-V_{REF}\left(\frac{255}{256}\right)$
10000001	$-V_{REF}\left(\frac{129}{256}\right)$
10000000	$-V_{REF}\left(\frac{128}{256}\right) = -\frac{V_{REF}}{2}$
01111111	$-V_{REF}\left(\frac{127}{256}\right)$
00000001	$-V_{REF}\left(\frac{1}{256}\right)$
00000000	$-V_{REF}\left(\frac{0}{256}\right) = 0$

Note: 1 LSB = $(2^{-8})(V_{REF}) = \left(\frac{1}{256}\right)(V_{REF})$

Table 1. Unipolar Binary Code Table

BIPOLAR OPERATION

NOTES:
1. R3/R4 MATCH 0.1% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. R5-R7 USED TO ADJUST V_{OUT} = 0V AT INPUT CODE 10000000.
4. CR1 & CR2 PROTECT AD7523 AGAINST NEGATIVE TRANSIENTS.

Figure 2. Bipolar (4-Quadrant) Operation

DIGITAL INPUT MSB LSB	ANALOG OUTPUT
11111111	$-V_{REF}\left(\frac{127}{128}\right)$
10000001	$-V_{REF}\left(\frac{1}{128}\right)$
10000000	0
01111111	$+V_{REF}\left(\frac{1}{128}\right)$
00000001	$+V_{REF}\left(\frac{127}{128}\right)$
00000000	$+V_{REF}\left(\frac{128}{128}\right)$

Note: 1LSB = $(2^{-7})(V_{REF}) = \left(\frac{1}{128}\right)(V_{REF})$

Table 2. Bipolar (Offset Binary) Code Table

4

POWER DAC DESIGN USING AD7523

Figure 3. The Basic Power DAC

A typical power DAC designed for 10 bit accuracy and 8 bit resolution is shown in Figure 3. INTERSIL IH8510 power amplifier (1 Amp continuous output with up to +25V) is driven by the AD7523.

A summing amplifier between the AD7523 and the IH8510 is used to separate the gain block containing the AD7520 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise AD7523 can be directly connected to the IH8510, by using a 25 volts reference for the DAC.

APPLICATIONS (continued)

DIVIDER (DIGITALLY CONTROLLED GAIN)

$V_{OUT} = -V_{IN}/D$

WHERE:

$$D = \frac{BIT1}{2^1} + \frac{BIT2}{2^2} + \dots \frac{BIT8}{2^8}$$

$$\left(0 \le D \le \frac{255}{256}\right)$$

MODIFIED SCALE FACTOR AND OFFSET

$$V_{OUT} = V_{REF}\left[\left(\frac{R_2}{R_1+R_2}\right) - \left(\frac{R_1 D}{R_1+R_2}\right)\right] \quad \text{WHERE:} \quad D = \frac{BIT\ 1}{2^1} + \frac{BIT\ 2}{2^2} + \dots \frac{BIT\ 8}{2^8}$$

$$\left(0 \le D \le \frac{255}{256}\right)$$

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

4

PACKAGE DIMENSIONS

16 PIN CERDIP

16 PIN PLASTIC DIP

1. Lead no. 1 identified by dot or notch.
2. Dimensions in inches (millimeters).

INTERSIL

AD7533
10 Bit Monolithic Multiplying D/A Converters

FEATURES

- Lowest cost 10-bit DAC
- 8, 9 and 10 bit linearity
- Low gain and linearity Tempcos
- Full temperature range operation
- Full input static protection
- DTL/TTL/CMOS direct interface
- +5 to +15 volts supply range
- Low power dissipation
- Fast settling time
- Four quadrant multiplication
- Direct AD7520 equivalent
- 883B Processed versions available

GENERAL DESCRIPTION

The Intersil AD7533 is a low cost, monolithic 10-bit, four-quadrant multiplying digital-to-analog converter (DAC).

Intersil's thin-film resistors on CMOS circuitry provide 10, 9 and 8 bit accuracy, full temperature range operation, +5V to +15V power range, full input protection from damage due to static discharge by clamps to V+ and ground and very low power dissipation.

Pin and function equivalent to Industry Standard AD7520, the AD7533 is recommended as a lower cost alternative for old or new 10-bit DAC designs.

Application of AD7533 includes programmable gain amplifiers, digitally controlled attenuators, function generators and control systems.

FUNCTIONAL DIAGRAM

(Switches shown for Digital Inputs "High")

PIN CONFIGURATION

ORDERING INFORMATION

Nonlinearity	Temperature Range		
	0°C to +70°C	-25°C to +85°C	-55°C to +125°C
±0.2% (8-bit)	AD7533JN	AD7533AD	AD7533SD
±0.1% (9-bit)	AD7533KN	AD7533BD	AD7533TD
±0.05% (10-bit)	AD7533LN	AD7533CD	AD7533UD

PACKAGE IDENTIFICATION

SUFFIX D: CERDIP PACKAGE
SUFFIX N: PLASTIC PACKAGE

4

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

VDD (to GND) ..... −0.3V, +17V
VREF (to GND) ..... ±25V
Digital Input Voltage Range ..... −0.3V to V_{DD}
Output Voltage Compliance ..... −0.3 to VDD
Power Dissipation (package)
Ceramic
up to +75°C 450mW
derates above +75°C by ..... 6mW/°C
Plastic
up to 70°C 670mW
derates above 70°C by ..... 8.3mW/°C
Operating Temperatures
JN, KN, LN Versions ..... 0°C to +70°C
AD, BD, CD Versions ..... −25°C to +85°C
SD, TD, UD Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Lead Temperature (soldering, 10 seconds) ..... +300°C

CAUTION: 1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2. Do not apply voltages lower than ground or higher than V_{DD} to any pin except V_{REF} and R_{FB}.

SPECIFICATIONS (VDD = +15V, VREF = +10V, V_{OUT1} = V_{OUT2} = 0 unless otherwise specified)

PARAMETER		TA +25°C	TA MIN-MAX	UNITS	LIMIT	TEST CONDITIONS
DC ACCURACY (Note 1)						
Resolution		10	10	Bits	Min	
Nonlinearity (Note 2)		±0.2	±0.2	% of FSR	Max	
		±0.1	±0.1	% of FSR	Max	−10V ≤ VREF ≤ +10V
		±0.05	±0.05	% of FSR	Max	V_{OUT1} = V_{OUT2} = 0V
Gain Error (Note 2 and 5)		±1.4	±1.5	% of FS	Max	Digital Inputs = VINH
Output Leakage Current (either output)		±50	±200	nA	Max	V_{REF} = ±10V
AC ACCURACY						
Power Supply Rejection (Note 2 and 3)		0.005	0.008	% of FSR/%	Max	V_{DD} = 14.0 to 17.0V
Output Current Settling Time		600 (Note 6)	800 (Note 3)	nS	Max	To 0.05% of FSR, R_L = 100Ω
Feedthrough Error (Note 3)		±0.05	±0.1	% FSR	Max	VREF = ±10V, 100KHz sine wave. Digital inputs low.
REFERENCE INPUT		5K			Min	
Input Resistance (Pin 15)		20K		Ω	Max	All digital inputs high.
Temperature Coefficient		−300		ppm/°C	Typ	
ANALOG OUTPUT						Both outputs.
Voltage Compliance (Note 4)		−100mV to V_{DD}				See maximum ratings.
Output Capacitance (Note 3)	C_{OUT1}	100		pF	Max	All digital inputs high (VINH)
	C_{OUT2}	35		pF	Max	
	C_{OUT1}	35		pF	Max	All digital inputs low (VINL)
	C_{OUT2}	100		pF	Max	
DIGITAL INPUTS						
Low State Threshold (VINL)		0.8		V	Max	
High State Threshold (VINH)		2.4		V	Min	
Input Current (I_{IN})		±1		μA	Max	V_{IN} = 0V and V_{DD}
Input Coding		Binary/Offset Binary				See Tables 1 & 2
Input Capacitance (Note 3)		5		pF	Max	
POWER REQUIREMENTS						
V_{DD}		+15 ±10%		+15 ±10%		Rated Accuracy
Power Supply Voltage Range		+5 to +16		V		
IDD		2		mA	Max	Digital Inputs = V_{INL} to V_{INH}
I_{DD}		100μA		150μA	Max	Digital Inputs = 0V or V_{DD}

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.
5. Full scale (FS) = − (V_{REF}) • (1023/1024)
6. Sample tested to ensure specification compliance.
7. 100% screened to MIL-STD-833, method 5004, para. 3.1.1. through 3.1.12 for class B device. Final electrical tests are: Nonlinearity, Gain Error, Output Leakage Current, V_{INH}, V_{INL}, I_{IN} and I_{DD} @ +25°C and +125°C (SD, TD, UD) or +25°C and +85°C (AD, BD, CD).

Specifications subject to change without notice.

GENERAL CIRCUIT INFORMATION

The Intersil AD7533 is a 10 bit, monolithic, multiplying D/A converter. Highly stable thin film R-2R resistor ladder network and NMOS DPDT switches form the basis of the converter circuit. CMOS level shifters provide low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 1. The NMOS DPDT switches steer the ladder leg currents between IOUT1 and IOUT2 busses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.

(Switches shown for Digital Inputs "High")

Figure 1

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 2). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder DPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors resulting in accurate leg currents.

Figure 2

APPLICATIONS

UNIPOLAR OPERATION (2-QUADRANT MULTIPLICATION)

NOTES:
1. R1 AND R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
2. SCHOTTKY DIODE CR1 (HP5082-2811 OR EQUIV) PROTECTS OUT1 TERMINAL AGAINST NEGATIVE TRANSIENTS.

Figure 3. Unipolar Binary Operation (2-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 3)
1111111111	$-V_{REF}\left(\frac{1023}{1024}\right)$
1000000001	$-V_{REF}\left(\frac{513}{1024}\right)$
1000000000	$-V_{REF}\left(\frac{512}{1024}\right) = -\frac{V_{REF}}{2}$
0111111111	$-V_{REF}\left(\frac{511}{1024}\right)$
0000000001	$-V_{REF}\left(\frac{1}{1024}\right)$
0000000000	$-V_{REF}\left(\frac{0}{1024}\right) = 0$

NOTES:

1. Nominal Full Scale for the circuit of Figure 3 is given by

$$FS = -V_{REF}\left(\frac{1023}{1024}\right)$$

2. Nominal LSB magnitude for the circuit of Figure 3 is given by

$$LSB = V_{REF}\left(\frac{1}{1024}\right)$$

Table 1. Unipolar Binary Code

BIPOLAR OPERATION (4-QUADRANT MULTIPLICATION)

NOTES:
1. R3/R4 MATCH 0.05% OR BETTER.
2. R1, R2 USED ONLY IF GAIN ADJUSTMENT IS REQUIRED.
3. SCHOTTKY DIODES CR1 AND CR2 (HP5082-2811 OR EQUIV) PROTECT OUT1 AND OUT2 TERMINALS FROM NEGATIVE TRANSIENTS

Figure 4. Bipolar Operation (4-Quadrant Multiplication)

DIGITAL INPUT MSB LSB	NOMINAL ANALOG OUTPUT (V_{OUT} as shown in Figure 4)
1111111111	$-V_{REF}\left(\frac{511}{512}\right)$
1000000001	$-V_{REF}\left(\frac{1}{512}\right)$
1000000000	0
0111111111	$+V_{REF}\left(\frac{1}{512}\right)$
0000000001	$+V_{REF}\left(\frac{511}{512}\right)$
0000000000	$+V_{REF}\left(\frac{512}{512}\right)$

NOTES:

1. Nominal Full Scale Range for the circuit of Figure 4 is given by

$$FSR = V_{REF}\left(\frac{1023}{512}\right)$$

2. Nominal LSB magnitude for the circuit of Figure 4 is given by

$$LSB = V_{REF}\left(\frac{1}{512}\right)$$

Table 2. Bipolar (Offset Binary) Code Table

POWER DAC DESIGN USING AD7533

Figure 5. The Basic Power DAC

A typical power DAC designed for 8 bit accuracy and 10 bit resolution is shown in Figure 5. INTERSIL IH8510 power amplifier (1 Amp continuous output with up to +25V) is driven by the AD7533.

A summing amplifier between the AD7533 and the IH8510 is used to separate the gain block containing the AD7533 on-chip resistors from the power amplifier gain stage whose gain is set only by the external resistors. This approach minimizes drift since the resistor pairs will track properly. Otherwise AD7533 can be directly connected to the IH8510, by using a 25 volts reference for the DAC. Notice that the output of the 101A is fed into an inverting amplifier with a gain of −3, which can be easily changed to a non-inverting configuration. (For more information write for: INTERSIL Application Bulletin A021-Power D/A Converters Using The IH8510 by Dick Wilenken.)

10-BIT AND SIGN MULTIPLYING DAC

PROGRAMMABLE FUNCTION GENERATOR

PACKAGE DIMENSIONS

16 PIN CERDIP

16 PIN PLASTIC DIP

1. Lead no. 1 identified by dot or notch.
2. Dimensions in inches (millimeters).

INTERSIL

AD7541
12 Bit Monolithic Multiplying D/A Converters

FEATURES

- 12 bit linearity (0.01%)
- Pretrimmed gain
- Low gain and linearity Tempcos
- Full temperature range operation
- Full input static protection
- DTL/TTL/CMOS compatible
- +5 to +15 volts supply range
- Low power dissipation (20mW)
- Current settling time: 1μs to 0.01% of FSR
- Four quadrant multiplication
- 883B Processed versions available

GENERAL DESCRIPTION

The Intersil AD7541 is a monolithic, low cost, high performance, 12-bit accurate, multiplying digital-to-analog converter (DAC).

Intersil's wafer level laser-trimmed thin-film resistors on CMOS circuitry provide true 12-bit linearity with DTL/TTL/CMOS compatible operation.

Special tabbed-resistor geometries (improving time stability), full input protection from damage due to static discharge by diode clamps to V+ and ground, large I_{OUT1} and I_{OUT2} bus lines (improving superposition errors) are some of the features offered by Intersil AD7541.

Pin compatible with AD7521, this new DAC provides accurate four quadrant multiplication over the full military temperature range.

FUNCTIONAL DIAGRAM

(Switches shown for Digital Inputs "High")

PIN CONFIGURATION

ORDERING INFORMATION

Nonlinearity	Temperature Range 0°C to +70°C	-25°C to +85°C	-55°C to +125°C
0.02% (11-bit)	AD7541JN	AD7541AD	AD7541SD
0.01% (12-bit)	AD7541KN	AD7541BD	AD7541TD
0.01% (12-bit) Guaranteed Monotonic	AD7541LN	—	—

PACKAGE IDENTIFICATION

4

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

VDD (to GND) ..... +17V
VREF (to GND) ..... ±25V
Digital Input Voltage Range ..... VDD to GND
Output Voltage Compliance ..... −100mV to VDD
Power Dissipation (package)
up to +75°C 450mW
derates above +75°C by ..... 6mW/°C

Operating Temperatures
JN, KN, LN Versions ..... 0°C to +70°C
AD, BD Versions ..... −25°C to +85°C
SD, TD Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C

CAUTION 1. The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.
2. Do not apply voltages higher than V_{DD} or less than GND potential on any terminal except V_{REF}.

SPECIFICATIONS (VDD = +15V, VREF = +10V, TA = 25°C unless otherwise specified)

PARAMETER		TA +25°C	TA MIN-MAX	UNITS	LIMIT	TEST CONDITIONS	FIG.
DC ACCURACY (Note 1) Resolution		12	12	Bits	Min		
Nonlinearity (Note 2)	S J	±0.020	±0.024	% of FSR	Max	−10V ≤ VREF ≤ +10V	1
	T K	±0.010	±0.012	% of FSR	Max	V_{OUT1} = V_{OUT2} = 0V	
	L	±0.010	±0.012	% of FSR	Max		
		Guaranteed Monotonic					
Gain Error (Note 2)		±0.3	±0.4	% of FSR	Max	−10V ≤ VREF ≤ +10V	
Output Leakage Current (either output)		±50	±200	nA	Max	V_{OUT1} = V_{OUT2} = 0	
AC ACCURACY (Note 3) Power Supply Rejection (Note 2)		±0.01	±0.02	% of FSR/%	Max	V_{DD} = 14.5 to 15.5V	2
Output Current Settling Time		1		μS	Max	To 0.01% of FSR	6
Feedthrough Error		1		mV pp	Max	VREF = 20V pp, 10 KHz. All digital inputs low.	5
REFERENCE INPUT Input Resistance		5K		Ω	Min	All digital inputs high. I_{OUT1} at ground.	
		10K			Typ		
		20K			Max		
ANALOG OUTPUT Voltage Compliance (Note 4)		−100mV to V_{DD}				Both outputs. See maximum ratings.	
Output Capacitance (Note 3)	C_{OUT1}	200		pF	Max	All digital inputs high (VINH)	4
	C_{OUT2}	60		pF	Max		
	C_{OUT1}	60		pF	Max	All digital inputs low (VINL)	4
	C_{OUT2}	200		pF	Max		
Output Noise (both outputs)		Equivalent to 10KΩ Johnson noise			Typ		3
DIGITAL INPUTS Low State Threshold (VINL)		0.8		V	Max		
High State Threshold (VINH)		2.4		V	Min		
Input Current		±1		μA	Max	V_{IN} = 0 or V_{DD}	
Input Coding		Binary/Offset Binary				See Tables 1 & 2 on pages 4 and 5.	
Input Capacitance (Note 3)		8		pF	Max		
POWER REQUIREMENTS Power Supply Voltage Range		+5 to +16		V		Accuracy is not guaranteed over this range	
IDD		2		mA	Max	All digital inputs high or low	
Total Power Dissipation (including the ladder)		20		mW	Typ		

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

Specifications subject to change without notice.

TEST CIRCUITS

Figure 1. Nonlinearity

Figure 2. Power Supply Rejection

Figure 3. Noise

Figure 4. Output Capacitance

Figure 5. Feedthrough Error

Figure 6. Output Current Settling Time

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

GENERAL CIRCUIT INFORMATION

The Intersil AD7541 is a 12 bit, monolithic, multiplying D/A converter. Highly stable thin film R-2R resistor ladder network and NMOS DPDT switches form the basis of the converter circuit. CMOS level shifters provide low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 7. The NMOS DPDT switches steer the ladder leg currents between IOUT1 and IOUT2 busses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.

Converter errors are further eliminated by using wider metal interconnections between the major bits and the outputs. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

Each circuit is laser-trimmed, at the wafer level, to better than 12 bits linearity. For the first four bits of the ladder, special trim-tabbed geometries are used to keep the body of the resistors, carrying the majority of the output current, undisturbed. The resultant time stability of the trimmed circuits is comparable to that of untrimmed units.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first (Figure 8). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder DPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors, resulting in accurate leg currents.

(Switches shown for Digital Inputs "High")

Figure 7. AD7541 Functional Diagram

Figure 8. CMOS Switch

APPLICATIONS

General Recommendations

Static performance of the AD7541 depends on I_{OUT1} and I_{OUT2} (pin 1 and pin 2) potentials being exactly equal to GND (pin 3).

The output amplifier should be selected to have a low input bias current (typically less than 75nA), and a low drift (depending on the temperature range). The voltage offset of the amplifier should be nulled (typically less than ±200μV).

The bias current compensation resistor in the amplifier's non-inverting input can cause a variable offset. Non-inverting input should be connected to GND with a low resistance wire.

Ground-loops must be avoided by taking all pins going to GND to a common point, using separate connections.

The V_{DD} (pin 18) power supply should have a low noise level and should not have any transients exceeding +17 volts.

Unused digital inputs must be connected to GND or V_{DD} for proper operation.

A high value resistor (~1MΩ) can be used to prevent static charge accumulation, when the inputs are open-circuited for any reason.

When gain adjustment is required, low tempco (approximately 50ppm/°C) resistors or trim-pots should be selected.

APPLICATIONS, Continued

UNIPOLAR BINARY OPERATION

The circuit configuration for operating the AD7541 in unipolar mode is shown in Figure 9. With positive and negative VREF values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1. Schottky diode (HP 5082-2811 or equivalent) prevents I_{OUT1} from negative excursions which could damage the device. This precaution is only necessary with certain high speed amplifiers.

Figure 9. Unipolar Binary Operation (2-Quadrant Multiplication)

Zero Offset Adjustment
1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±0.5mV (max) at VOUT.

Gain Adjustment
1. Connect all digital inputs to VDD.
2. Monitor VOUT for a $-V_{REF}(1 - 1/2^{12})$ reading.
3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

TABLE 1
Code Table — Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}(1 - 1/2^{12})$
100000000001	$-V_{REF}(1/2 + 1/2^{12})$
100000000000	$-V_{REF}/2$
011111111111	$-V_{REF}(1/2 - 1/2^{12})$
000000000001	$-V_{REF}(1/2^{12})$
000000000000	0

BIPOLAR (OFFSET BINARY) OPERATION

The circuit configuration for operating the AD7541 in the bipolar mode is given in Figure 10. Using offset binary digital input codes and positive and negative reference voltage values Four-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

Note: R1 and R2 should be 0.01%, low-TCR resistors.

Figure 10. Bipolar Operation (4-Quadrant Multiplication)

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to IOUT1 bus. A "Logic 0" input forces the bit current to IOUT2 bus. For any code the IOUT1 and IOUT2 bus currents are complements of one another. The current amplifier at IOUT2 changes the polarity of IOUT2 current and the transconductance amplifier at IOUT1 output sums the two currents. This configuration doubles the output range but halves the resolution of the DAC. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistive divider, from VREF to IOUT2.

Offset Adjustment
1. Adjust VREF to approximately +10V.
2. Connect all digital inputs to "Logic 1".
3. Adjust IOUT2 amplifier offset zero adjust trimpot for 0V ± 0.1mV at IOUT2 amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust IOUT1 amplifier offset zero adjust trimpot for 0V ± 0.1mV at IOUT1 amplifier output.
6. Adjust R4 for 0V ± 0.2mV at VOUT.

Gain Adjustment
1. Connect all digital inputs to VDD.
2. Monitor VOUT for a $-V_{REF}(1 - 1/2^{11})$ volts reading.
3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

TABLE 2
Code Table — Bipolar (Offset Binary) Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}(1 - 1/2^{11})$
100000000001	$-V_{REF}(1/2^{11})$
100000000000	0
011111111111	$V_{REF}(1/2^{11})$
000000000001	$V_{REF}(1 - 1/2^{11})$
000000000000	V_{REF}

4

Figure 11. General DAC Circuit with Compensation Capacitor, C_C.

Figure 12. AD7541 Response with: A = Intersil 741HS

Figure 13. AD7541 Response with: A = Intersil 2515
C_C = 15pF

Figure 14. AD7541 Response with: A = Intersil 2520

DYNAMIC PERFORMANCE

The dynamic performance of the DAC, also depends on the output amplifier selection. For low speed or static applications, AC specifications of the amplifier are not very critical. For high-speed applications slew-rate, settling-time, open-loop gain and gain/phase-margin specifications of the amplifier should be selected for the desired performance.

The output impedance of the AD7541 looking into I_{OUT1} varies between 10kΩ ($R_{Feedback}$ alone) and 5kΩ ($R_{Feedback}$ in parallel with the ladder resistance).

Similarly the output capacitance varies between the minimum and the maximum values depending on the input code. These variations necessitate the use of compensation capacitors, when high speed amplifiers are used.

A capacitor in parallel with the feedback resistor provides the necessary phase compensation to critically damp the output.

A small capacitor connected to the compensation pin of the amplifier may be required for unstable situations causing oscillations. Careful PC board layout, minimizing parasitic capacitances, is also vital.

Three typical circuits and the resultant waveforms are shown in Figures 11 to 14. A low-cost general purpose (Intersil 741HS), a low-cost high-speed (Intersil 2515) and a high-speed fast-settling (Intersil 2520) amplifier cover the principal application areas.

4

PACKAGE DIMENSIONS

18 PIN CERDIP

18 PIN PLASTIC DIP

1. Lead no. 1 identified by dot or notch.
2. Dimensions in inches (millimeters).

INTERSIL

ICL7112
12 Bit Monolithic Multiplying D/A Converters

FEATURES
- 12 bit linearity (0.01%)
- Low gain Tempco (5ppm/°C)
- Full temperature range operation
- Latch-up free operation
- DTL/TTL/CMOS compatible
- +5 to +15 volts supply range
- Low power dissipation (20mW)
- Current settling time: 1μs to 0.01% of FSR
- Four quadrant multiplication
- 883B Processed versions available

FUNCTIONAL DIAGRAM

(Switches shown for Digital Inputs "High")

GENERAL DESCRIPTION
The Intersil ICL7112 is a monolithic, low cost, high performance, 12-bit accurate, multiplying digital-to-analog converter (DAC).

Intersil's laser-trimmed thin-film resistors on junction-isolated CMOS circuitry provide true 12-bit absolute accuracy with DTL/TTL/CMOS compatible operation.

Special tabbed-resistor geometries (improving time stability), latch-up free operation, feed-back resistor compensation (improving gain tempco and power supply rejection ratio), large I_{OUT1} and I_{OUT2} bus lines (improving superposition errors) are some of the features offered by Intersil ICL7112.

Pin compatible with AD7521 and AD7541, this new DAC provides accurate four quadrant multiplication over the full military temperature range.

CHIP TOPOGRAPHY

PIN CONFIGURATION

ORDERING INFORMATION

Nonlinearity	Temperature Range 0°C to +70°C	-25°C to +85°C	-55°C to +125°C
0.02% (11-bit)	ICL7112JPN	ICL7112JJN	ICL7112SJN
0.01% (12-bit)	ICL7112KPN	ICL7112KJN	ICL7112TJN
0.01% (12-bit) Guaranteed Monotonic	ICL7112LPN	—	—

PACKAGE IDENTIFICATION

SUFFIX J: CERDIP PACKAGE
SUFFIX P: PLASTIC PACKAGE
SUFFIX N: 18 LEAD DIP PACKAGE

4

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

VDD (to GND) ..... +17V
VREF (to GND) ..... ±25V
Digital Input Voltage Range ..... VDD to GND
Output Voltage Compliance ..... −5 to VDD
Power Dissipation (package)
up to +75°C by 450mW
derates above +75°C by ..... 6mW/°C

Operating Temperatures
JP, KP, LP Versions ..... 0°C to +75°C
JJ, KJ Versions ..... −25°C to +85°C
SJ, TJ Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C

CAUTION: The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

SPECIFICATIONS (VDD = +15V, VREF = +10V, TA = 25°C unless otherwise specified)

PARAMETER			TA +25°C	TA MIN-MAX	UNITS	LIMIT	TEST CONDITIONS	FIG.
DC ACCURACY (Note 1)								
Resolution			12	12	Bits	Min		
Nonlinearity (Note 2)	S	J	±0.020	±0.024	% of FSR	Max	−10V ≤ VREF ≤ +10V	1
	T	K	±0.010	±0.012	% of FSR	Max	$V_{OUT1} = V_{OUT2} = 0V$	
		L	±0.010	±0.012	% of FSR	Max		
			Guaranteed Monotonic					
Gain Error (Note 2)			±0.3	0.35	% of FSR	Max	−10V ≤ VREF ≤ +10V	
Nonlinearity Tempco (Note 2 and 3)			0.2		PPM of FSR/°C	Max		
Gain Error Tempco (Note 2 and 3)			5		PPM of FSR/°C	Max		
Output Leakage Current (either output)			±50	±200	nA	Max		
AC ACCURACY (Note 3)								
Power Supply Rejection (Note 2			±50	±100	PPM of FSR/%	Max	V_{DD} = 14.0 to 16.0V	2
Output Current Settling Time			1		μS	Max	To 0.01% of FSR	6
Feedthrough Error			1		mV pp	Max	VREF = 20V pp, 10 KHz. All digital inputs low.	5
REFERENCE INPUT			5K			Min		
Input Resistance			10K		Ω	Typ	All digital inputs high.	
			20K			Max	I_{OUT1} at ground.	
ANALOG OUTPUT							Both outputs.	
Voltage Compliance (Note 4)			−100mV to V_{DD}				See maximum ratings.	
Output Capacitance (Note 3)			I_{OUT1} 550		pF	Max	All digital inputs high	4
			I_{OUT2} 250		pF	Max		
			I_{OUT1} 250		pF	Max	All digital inputs low	4
			I_{OUT2} 550		pF	Max		
Output Noise (both outputs)			Equivalent to 10KΩ Johnson noise			Typ		3
DIGITAL INPUTS								
Low State Threshold			0.8		V	Max		
High State Threshold			2.4		V	Typ		
			3.0		V	Min		
Input Current			±1		μA	Max	V_{IN} = 0 to V_{DD}	
Input Coding			Binary/Offset Binary				See Tables 1 & 2 on pages 4 and 5.	
Input Capacitance (Note 3)			8		pF	Max		
POWER REQUIREMENTS								
Power Supply Voltage Range			+5 to +16		V		Accuracy not guaranteed over this range.	
IDD			2		mA	Max	All digital inputs high or low	
Total Power Dissipation (including the ladder)			20		mW	Typ		

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

Specifications subject to change without notice.

TEST CIRCUITS

Figure 1. Nonlinearity

Figure 2. Power Supply Rejection

Figure 3. Noise

Figure 4. Output Capacitance

Figure 5. Feedthrough Error

Figure 6. Output Current Settling Time

DEFINITION OF TERMS

NONLINEARITY: Error contributed by deviation of the DAC transfer function from a best straight line function. Normally expressed as a percentage of full scale range. For a multiplying DAC, this should hold true over the entire V_{REF} range.

RESOLUTION: Value of the LSB. For example, a unipolar converter with n bits has a resolution of $(2^{-n})(V_{REF})$. A bipolar converter of n bits has a resolution of $[2^{-(n-1)}][V_{REF}]$. Resolution in no way implies linearity.

SETTLING TIME: Time required for the output function of the DAC to settle to within 1/2 LSB for a given digital input stimulus, i.e., 0 to Full Scale.

GAIN: Ratio of the DAC's operational amplifier output voltage to the nominal input voltage value.

FEEDTHROUGH ERROR: Error caused by capacitive coupling from V_{REF} to output with all switches OFF.

OUTPUT CAPACITANCE: Capacity from I_{OUT1} and I_{OUT2} terminals to ground.

OUTPUT LEAKAGE CURRENT: Current which appears on I_{OUT1} terminal with all digital inputs LOW or on I_{OUT2} terminal when all inputs are HIGH.

GENERAL CIRCUIT INFORMATION

The Intersil ICL7112 is a 12 bit, monolithic, multiplying D/A converter. Highly stable thin film R-2R resistor ladder network and NMOS DPDT switches form the basis of the converter circuit. Junction isolated CMOS level shifters provide latch-proof low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 7. The NMOS DPDT switches steer the ladder leg currents between IOUT1 and IOUT2 busses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.

Converter errors are further eliminated by using wider metal interconnections between the major bits and the outputs, and by compensating the internal feedback resistor with a series switch. Use of high threshold switches reduces the offset (leakage) errors to a negligible level.

Each circuit is laser-trimmed, at the wafer level, to better than 12 bits linearity. For the first four bits of the ladder, special trim-tabbed geometries are used to keep the body of the resistors, carrying the majority of the output current, undisturbed. The resultant time stability of the trimmed circuits is comparable to that of untrimmed units.

The level shifter circuits are comprised of three inverters with a positive feedback from the output of the second to the first, (Figure 8). This configuration results in DTL/TTL/CMOS compatible operation over the full military temperature range. With the ladder DPDT switches driven by the level shifter, each switch is binarily weighted for an "ON" resistance proportional to the respective ladder leg current. This assures a constant voltage drop across each switch, creating equipotential terminations for the 2R ladder resistors, resulting in accurate leg currents.

(Switches shown for Digital Inputs "High")

Figure 7. ICL7112 Functional Diagram

Figure 8. CMOS Switch

APPLICATIONS

General Recommendations

Static performance of the ICL7112 depends on I_{OUT1} and I_{OUT2} (pin 1 and pin 2) potentials being exactly equal to GND (pin 3).

The output amplifier should be selected to have a low input bias current (typically less than 75nA), and a low drift (depending on the temperature range). The voltage offset of the amplifier should be nulled (typically less than ±200μV).

The bias current compensation resistor in the amplifier's non-inverting input can cause a variable offset. Non-inverting input should be connected to GND with a low resistance wire.

Ground-loops must be avoided by taking all pins going to GND to a common point; using separate connections.

ICL7112 does not require any external protection diodes.

The V_{DD} (pin 18) power supply should have a low noise level and should not have any transients exceeding +17 volts.

Unused digital inputs must be connected to GND or V_{DD} for proper operation.

A high value resistor (~1MΩ) can be used to prevent static charge accumulation, when the inputs are open-circuited for any reason.

When gain adjustment is required, low tempco (approximately 50ppm/°C) resistors or trim-pots should be selected.

APPLICATIONS, Continued

UNIPOLAR BINARY OPERATION

The circuit configuration for operating the ICL7112 in unipolar mode is shown in Figure 9. With positive and negative VREF values the circuit is capable of 2-Quadrant multiplication. The "Digital Input Code/Analog Output Value" table for unipolar mode is given in Table 1.

Figure 9. Unipolar Binary Operation (2-Quadrant Multiplication)

Zero Offset Adjustment
1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±0.5mV (max) at VOUT.

Gain Adjustment
1. Connect all digital inputs to VDD.
2. Monitor VOUT for a $-V_{REF}$ $(1 - 1/2^{12})$ reading.
3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

TABLE 1
Code Table — Unipolar Binary Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}$ $(1 - 1/2^{12})$
100000000001	$-V_{REF}$ $(1/2 + 1/2^{12})$
100000000000	$-V_{REF}/2$
011111111111	$-V_{REF}$ $(1/2 - 1/2^{12})$
000000000001	$-V_{REF}$ $(1/2^{12})$
000000000000	0

BIPOLAR (OFFSET BINARY) OPERATION

The circuit configuration for operating the ICL7112 in the bipolar mode is given in Figure 10. Using offset binary digital input codes and positive and negative reference voltage values Four-Quadrant multiplication can be realized. The "Digital Input Code/Analog Output Value" table for bipolar mode is given in Table 2.

Note: R1 and R2 should be 0.01%, low-TCR resistors.

Figure 10. Bipolar Operation (4-Quadrant Multiplication)

A "Logic 1" input at any digital input forces the corresponding ladder switch to steer the bit current to IOUT1 bus. A "Logic 0" input forces the bit current to IOUT2 bus. For any code the IOUT1 and IOUT2 bus currents are complements of one another. The current amplifier at IOUT2 changes the polarity of IOUT2 current and the transconductance amplifier at IOUT1 output sums the two currents. This configuration doubles the output range but halves the resolution of the DAC. The difference current resulting at zero offset binary code, (MSB = "Logic 1", All other bits = "Logic 0"), is corrected by using an external resistive divider, from VREF to IOUT2.

Offset Adjustment
1. Adjust VREF to approximately +10V.
2. Connect all digital inputs to "Logic 1".
3. Adjust IOUT2 amplifier offset zero adjust trimpot for 0V ± 0.1mV at IOUT2 amplifier output.
4. Connect MSB (Bit 1) to "Logic 1" and all other bits to "Logic 0".
5. Adjust IOUT1 amplifier offset zero adjust trimpot for 0V ± 0.1mV at IOUT1 amplifier output.
6. Adjust R4 for 0V ± 0.2mV at VOUT.

Gain Adjustment
1. Connect all digital inputs to VDD.
2. Monitor VOUT for a $-V_{REF}$ $(1 - 1/2^{11})$ volts reading.
3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

TABLE 2
Code Table — Bipolar (Offset Binary) Operation

DIGITAL INPUT	ANALOG OUTPUT
111111111111	$-V_{REF}$ $(1 - 1/2^{11})$
100000000001	$-V_{REF}$ $(1/2^{11})$
100000000000	0
011111111111	V_{REF} $(1/2^{11})$
000000000001	V_{REF} $(1 - 1/2^{11})$
000000000000	V_{REF}

Figure 11. General DAC Circuit with Compensation Capacitor, C_C.

Figure 12. ICL7112 Response with: A = Intersil 741HS
C_C = 100pF

Figure 13. ICL7112 Response with: A = Intersil 2515
C_C = 30pF

Figure 14. ICL7112 Response with: A = Intersil 2520
C_C = 22pF

DYNAMIC PERFORMANCE

The dynamic performance of the DAC also depends on the output amplifier selection. For low speed or static applications, AC specifications of the amplifier are not very critical. For high-speed applications slew-rate, settling-time, open-loop gain and gain/phase-margin specifications of the amplifier should be selected for the desired performance.

The output impedance of the ICL7112 looking into I_{OUT1} varies between 10kΩ ($R_{Feedback}$ alone) and 5kΩ ($R_{Feedback}$ in parallel with the ladder resistance).

Similarly the output capacitance varies between the minimum and the maximum values depending on the input code. These variations necessitate the use of compensation capacitors, when high speed amplifiers are used.

A capacitor in parallel with the feedback resistor provides the necessary phase compensation to critically damp the output.

A small capacitor connected to the compensation pin of the amplifier may be required for unstable situations causing oscillations. Careful PC board layout, minimizing parasitic capacitances, is also vital.

Three typical circuits and the resultant waveforms are shown in Figures 11 to 14. A low-cost general purpose (Intersil 741HS), a low-cost high-speed (Intersil 2515) and a high-speed fast-settling (Intersil 2520) amplifier cover the principal application areas.

4

PACKAGE DIMENSIONS

18 PIN CERDIP

18 PIN PLASTIC DIP

BONDING DIAGRAM

1. Lead no. 1 identified by dot or notch.
2. Dimensions in inches (millimeters).

INTERSIL

ICL7113
3 Digit BCD Monolithic Multiplying D/A Converter

FEATURES

- .05% Linearity (ICL7113L)
- Low gain Tempco (10 ppm/°/C)
- Full temperature range operation
- Latch-up free operation
- DTL/TTL/CMOS compatible
- +5 to +15 volts supply range
- Low power dissipation (20mW)
- Current settling time: 1 μS to 0.05% of FSR
- 883B Processed versions available

GENERAL DESCRIPTION

The Intersil ICL7113 is a monolithic, low cost, high performance, 3 digit BCD, multiplying digital-to-analog converter (DAC).

Intersil's laser-trimmed thin-film resistors on junction-isolated CMOS circuitry provide .05% absolute accuracy with DTL/TTL/CMOS compatible operation.

Special tabbed-resistor geometries (improving time stability), latch-up free operation, feed-back resistor compensation (improving gain tempco and power supply rejection ratio), large I_{OUT1} and I_{OUT2} bus lines (improving superposition errors) are some of the features offered by Intersil ICL7113.

Typical applications include: Thumbwheel switch voltage dividers; digitally controlled gain circuits, attenuators, power supplies, etc.

FUNCTIONAL DIAGRAM

PIN CONFIGURATION

ORDERING INFORMATION

Nonlinearity	Temperature Range 0°C to +70°C	-25°C to +85°C	-55°C to +125°C
0.2%	ICL7113JPN	ICL7113JJN	ICL7113SJN
0.1%	ICL7113KPN	ICL7113KJN	ICL7113TJN
0.05%	ICL7113LPN	ICL7113LJN	ICL7113UJN

PACKAGE IDENTIFICATION

SUFFIX J: CERDIP PACKAGE
SUFFIX P: PLASTIC PACKAGE
SUFFIX N: 18 LEAD DIP PACKAGE

4

ABSOLUTE MAXIMUM RATINGS

(T_A = 25°C unless otherwise noted)

VDD (to GND) ..... +17V
VREF (to GND) ..... ±25V
Digital Input Voltage Range ..... VDD to GND
Output Voltage Compliance ..... −5 to VDD
Power Dissipation:
up to +75°C 450mW
derates above +75°C by ..... 6mW/°C

Operating Temperatures
JP, KP, LP Versions ..... 0°C to +70°C
JJ, KJ Versions ..... −25°C to +85°C
SJ, TJ Versions ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C

CAUTION: The digital control inputs are zener protected; however, permanent damage may occur on unconnected units under high energy electrostatic fields. Keep unused units in conductive foam at all times.

SPECIFICATIONS (VDD = +15V, VREF = +10V, TA = 25°C unless otherwise specified)

PARAMETER			TA +25°C	TA MIN-MAX	UNITS	LIMIT	TEST CONDITIONS
DC ACCURACY (Note 1)							
Resolution			3	3	Digits	Min	
Nonlinearity (Note 2)	S	J	.20	.20	% of FSR	Max	−10V ≤ VREF ≤ +10V
	T	K	.10	.10	% of FSR	Max	$V_{OUT1} = V_{OUT2} = 0V$
	U	L	.05	.05	% of FSR	Max	
Gain Error (Note 2)			±.3	±.4	% of FSR	Typ	−10V ≤ VREF ≤ +10V
Nonlinearity Tempco (Note 2 and 3)			2		PPM of FSR/°C	Max	
Gain Error Tempco (Note 2 and 3)			10		PPM of FSR/°C	Max	
Output Leakage Current (either output)			±50	±200	nA	Max	
AC ACCURACY							
Power Supply Rejection (Note 2 and 3)			±0.05	±0.1	% of FSR/%	Max	V_{DD} = 14.0 to 16.0V
Output Current Settling Time (Note 3)			1	1	μS	Max	To 0.05% of FSR
Feedthrough Error (Note 3)			1.5	2	mV pp	Max	VREF = 20V pp, 10 KHz. All digital inputs low.
REFERENCE INPUT							
Input Resistance			5K		Ω	Min	All digital inputs high. I_{OUT1} at ground.
			10K			Typ	
			20K			Max	
ANALOG OUTPUT							Both outputs. See maximum ratings.
Voltage Compliance (Note 4)			−100mV to V_{DD}				
Output Capacitance (Note 3)			I_{OUT1} 550		pF	Max	All digital inputs high
			I_{OUT2} 250		pF	Max	
			I_{OUT1} 250		pF	Max	All digital inputs low
			I_{OUT2} 550		pF	Max	
Output Noise (both outputs)			Equivalent to 10KΩ Johnson noise			Typ	
DIGITAL INPUTS							
Low State Threshold			0.8		V	Max	Over the specified temp range
High State Threshold			2.4		V	Typ	
			3.0		V	Min	
Input Current V_{IN} = 0 to V_{DD}			±1		μA	Max	
Input Coding			BCD				See Table 1
Input Capacitance (Note 3)			8		pF	Max	
POWER REQUIREMENTS							
Power Supply Voltage Range			+5 to +16		V		Accuracy not guaranteed over this range.
IDD			2		mA	Max	All digital inputs high or low
Total Power Dissipation (including the ladder)			20		mW	Typ	

NOTES: 1. Full scale range (FSR) is 10V for unipolar and ±10V for bipolar modes.
2. Using internal feedback resistor, $R_{FEEDBACK}$.
3. Guaranteed by design; not subject to test.
4. Accuracy not guaranteed unless outputs at ground potential.

Specifications subject to change without notice.

4

GENERAL CIRCUIT INFORMATION

The Intersil ICL7113 is a 3 digit BCD monolithic, multiplying D/A converter. Highly stable thin film R-2R resistor ladder network, interquad voltage dividers, and NMOS DPDT switches form the basis of the converter circuit. Junction isolated CMOS level shifters, Figure 2, provide latch-proof low power DTL/TTL/CMOS compatible operation. An external voltage or current reference and an operational amplifier are all that is required for most voltage output applications.

A simplified equivalent circuit of the DAC is shown in Figure 3. The NMOS DPDT switches steer the ladder leg currents between IOUT1 and IOUT2 busses which must be held at ground potential. This configuration maintains a constant current in each ladder leg independent of the input code.

Each circuit is laser-trimmed, at the wafer level, to better than .05% linearity. For the first MSB bits, special trim-tabbed geometries are used to keep the body of the resistors, carrying the majority of the output current, undisturbed. The resultant time stability of the trimmed circuits is comparable to that of untrimmed units.

Figure 2: CMOS Level Shifter/Switch

Figure 3: ICL7113 Circuit Diagram

APPLICATIONS

General Recommendations

To insure stability and prevent output ringing, a compensation capacitor of 10-100pF in parallel with the feed back resistor will be needed for some applications.

Unused digital inputs must be connected to GND or V_{DD} for proper operation.

ICL7113 does not require external schottky protection diodes at output.

BCD MULTIPLYING DAC

Intersil 7113 is capable of 2-quadrant multiplication with positive and negative reference values. The "Digital Input Code/Analog Output Value" table is given in Table 1. Figure 4 shows a typical circuit.

Figure 4: BCD Multiplying DAC Circuit

Zero Offset Adjustment:
1. Connect all digital inputs to GND.
2. Adjust the offset zero adjust trimpot of the output operational amplifier for 0V ±0.5mV (max) at VOUT.

Gain Adjustment:
1. Apply BCD Code .999 (1001 1001 1001)
2. Monitor VOUT for a −VREF (1 - 1/10³) reading.
3. To increase VOUT, connect a series resistor, (0 to 500 ohms), in the IOUT1 amplifier feedback loop.
4. To decrease VOUT, connect a series resistor, (0 to 500 ohms), between the reference voltage and the VREF terminal.

TABLE 1
CODE TABLE - BCD DAC

INPUT		ANALOG OUTPUT
BCD	DECIMAL	
1001 1001 1001	999	$-V_{REF}$ (1-1/10³)
0000 0000 0001	001	$-V_{REF}$ (1/10³)
0000 0000 0000	000	0

APPLICATIONS (Continued)

Figure 5: Thumbwheel Switch Attenuator

The circuit in Figure 4 shows the ICL7113 used as a low-cost precision voltage divider, similar to 10-turn potentiometers. Low parts count, increased reliability, low cost, 0.1% V_{IN} resolution and an excellent 0.05% of FSR non-linearity make ICL7113 a real advantage for the circuit designer.

The BCD coded thumbwheel assembly (available from AMP, Harrisburg, PA; CHERRY, Waukegan, IL; SAE, Santa Clara, CA) applies to BCD data to the ICL7113 inputs. A SPST assembly with pull-up or pull-down resistors can be substituted.

Resistors R1, R2 can be used to adjust the gain, R3 to limit the current if make-before-break switches are used; and R4 to adjust the offset voltage.

A voltage reference and an Intersil IH8510 power amplifier can be used with this circuit to build a ±25V, 1 Amp continuous output power source. (For more information write for Intersil Application Bulletin A021 - "Power D/A Converters Using the IH8510," by D. Wilenken.)

PACKAGE DIMENSIONS

4

18 PIN CERDIP

18 PIN PLASTIC DIP

BONDING DIAGRAM

1. Lead no. 1 identified by dot or notch.
2. Dimensions in inches (millimeters).

ICL8052/ICL7101
3½ Digit A/D Pair

FEATURES

- Guaranteed zero reading for 0 volts input
- Auto-zero; auto polarity
- 5pA input current typical
- Single reference voltage
- Latched parallel (full-time) BCD output for LCDs or data busing
- True polarity at zero count for precise null detection
- On-board clock and reference

ORDERING INFORMATION

Part	Temp. Range	Package	Order Number
8052	0°C to 70°C	14 pin plastic DIP	ICL8052CPD
8052	0°C to 70°C	14 pin ceramic DIP	ICL8052CDD
7101	0°C to 70°C	40 pin plastic DIP	ICL7101CPL
7101	0°C to 70°C	40 pin ceramic DIP	ICL7101CDL

GENERAL DESCRIPTION

The 8052/7101 A/D Pair, with its parallel BCD outputs, is ideally suited for data processing applications or interfacing with 3½-digit Liquid Crystal Displays. No external circuitry is required to demultiplex the information. In addition, it has a "start/reset" input and "busy" output that allows easy synchronization to system requirements. The 8052/7101 provides 4½-digit accuracy in a 3½-digit format with typical system performance like 5pA input leakage, auto-zero to 10μV with less than 1μV/°C drift and Linearity to 0.002%.

The 8052/7101 A/D pair also features conversion rates from 10 seconds to 30 per second, making them ideally suited for a wide variety of applications.

CONNECTION DIAGRAM

8052 Analog Signal Conditioner

CONNECTION DIAGRAM

7101 Digital Processor

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1)	500mW
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temperature (Soldering, 60 Sec.)	300°C

8052 ONLY

Supply Voltage	±18V
Differential Input Voltage	±6V
Input Voltage (Note 2)	±15V
Output Short Circuit Duration, All Outputs (Note 3)	Indefinite

7101 ONLY

Source Current (I_S)	100mA
Drain Current (I_D)	100mA
Digital Inputs	5mA
V^+ to V^-	25V
Digital Input	V^- to V^+

Note 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

7101 ELECTRICAL CHARACTERISTICS (V^+ = +5.0V, V^- = −15V, T_A = +25°C unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	7101 MIN	7101 TYP	7101 MAX	UNITS
Clock Frequency	f_{IN}	C = 1500 pF		20		kHz
External Clock In	I_{INL}	V_{IN} = 0 V		0.35	1.0	mA
External Clock In	I_{INH}	V_{IN} = +5.0 V		0.35	1.0	mA
Reset/Start	I_{INL}	V_{IN} = 0 V		0.8	2.0	mA
Internal Counter Override External Counter Input	I_{INH}	V_{IN} = +5.0 V		0.35	1.0	mA
BCD	V_{OL}	I_{OL} = 1.6 mA		0.25	0.4	V
BCD	V_{OH}	I_{OH} = −200 μA	2.4	4.5		V
Out-of-Range	V_{OL}	I_{OL} = 3.2 mA		0.25	0.4	V
Out-of-Range	V_{OH}	I_{OH} = 400 μA	2.4	4.5		V
Polarity, Apex, Busy, $\overline{1000}$	V_{OL}	I_{OL} = 0.8 mA		0.25	0.4	
Polarity, Apex, Busy, $\overline{1000}$	V_{OH}	I_{OH} = −200 μA	2.4	4.5		V
Gated Clockout	V_{OL}	I_{OL} = 0.3 mA		0.25	0.4	V
Gated Clockout	V_{OH}	I_{OH} = −200 μA	2.4	4.5		V
Switches 1, 3, 4, 5, 6	$R_{DS(ON)}$			400		Ω
Switch 2	$R_{DS(ON)}$			2500		Ω
+5.0 V Supply Current	I_{CC}^+			15	25	mA
−15 V Supply Current	I_{CC}^-			3.0	5.0	mA

Output

External Counter Input
Internal Counter Override

Start/Reset

TYPICAL INPUT/OUTPUT SCHEMATICS

8052 ELECTRICAL CHARACTERISTICS ($V_S = \pm 15V$, $T_A = +25°C$ unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8052 MIN	8052 TYP	8052 MAX	UNITS
OPERATIONAL AMPLIFIER					
Input Offset Voltage	$V_{CM} = 0V$		20	50	mV
Input Current (either input)	$V_{CM} = 0V$		5	50	pA
Common-Mode Rejection Ratio	$V_{CM} = \pm 10V$	70	90		dB
Non-Linear Component of Common-Mode Rejection Ratio*	$V_{CM} = \pm 2V$		110		dB
Large Signal Voltage Gain	$R_L = 10k\Omega$ $V_{OUT} = \pm 10V$	20,000			V/V
Slew Rate			6		V/μs
Unity Gain Bandwidth			1		MHz
Output Short-Circuit Current			20	50	mA
COMPARATOR AMPLIFIER					
Small-Signal Voltage Gain	$R_L = 30k\Omega$		4000		V/V
Positive Output Voltage Swing		+12	+13		V
Negative Output Voltage Swing		-2.0	-2.6		V
VOLTAGE REFERENCE					
Output Voltage		1.5	1.75	2.0	V
Output Resistance			5		ohms
Temperature Coefficient			40		ppm
Supply Current Total			6	12	mA

*This is the only component that causes error in dual-slope converter.

SYSTEM ELECTRICAL CHARACTERISTICS

($V_{++} = +15V$, $V_+ = +5.0V$, $V_- = -15V$, $T_A = +25°C$, Clock Frequency Set for 3 Reading/Sec)

CHARACTERISTICS	CONDITIONS	8052/7101 (1) MIN	8052/7101 (1) TYP	8052/7101 (1) MAX	UNITS
Zero Input Reading	$V_{in} = 0.0V$	-0.000	±0.000	+0.000	Digital Reading
Ratiometric Reading	$V_{in} \equiv V_{Ref.}$	+0.998	+1.000	+1.001	Digital Reading
Linearity over ± Full Scale (error off reading from best straight line)	$-2V \leqslant V_{in} \leqslant +2V$		0.1	1	Digital Count Error
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \equiv +V_{in} \approx 2V$		0.1	1	Digital Count Error
Noise (P-P value not exceeded 95% of time)	$V_{in} = 0V$ Full scale = 200.0mV		0.2		Digital
	Full scale = 2.000V		0.05		Count
Leakage Current into Input	$V_{in} = 0V$		5	30	pA
Zero Reading Drift	$V_{in} = 0V$ $0° \leqslant T_A \leqslant 70°C$		1	5	μV/°C
Scale Factor Temperature Coefficient	$V_{in} = +2V$ $0° \leqslant T_A \leqslant 70°C$ (ext. ref. 0 ppm/°C)		3	15	ppm/°C

(1) Tested in 3½ digit (2,000 count) circuit shown in Fig. 1 clock frequency 20kHz.

4

CIRCUIT DESCRIPTION

Figure 1 shows a typical circuit for a DVM. A minimum of external components is required since the chips have an on-board clock and a medium-quality (40ppm/°C) internal reference. The circuit also shows the switching required for two scale factors: 2.000V and 200.0mV full scale.

The system uses the time-proven dual-slope integration with all of its advantages; non-critical components, high rejection of noise and AC signals, non-critical clock frequency and true ratiometric readings. At the same time, it eliminates one of the basic disadvantages of dual-slope conversion: separate positive and negative reference sources. In this system, the negative reference is generated by charging the reference capacitor to the positive reference potential and then switching it into the circuit inverted when a negative reference is required. Due to the very low leakage and charge injection of the FET switches, the positive and negative references track each other to 10μV over a wide temperature range. This assures a very small error between positive and negative scale factor and, thus, excellent linearity from (+) full-scale to (–) full-scale (.002% typical).

The measurement cycle for the 8052/7101 has three phases. These are auto-zero, integrate input, and integrate reference. At the end of a measurement the system automatically reverts to the auto-zero mode until a new measurement is initiated. If an over-load has not occurred in the previous measurement, 10 milliseconds of auto-zero is sufficient to null any offsets to 10μV. At power on, or after an overload, 100 milliseconds is required to assure the auto-zero capacitor has charged to the correct value.

Start Conversion

Prior to conversion, the reset-start input must be held low to inhibit conversion (during auto-zero). Conversion is initiated by a positive transition on the start-reset line. (It must therefore return to the low state prior to completion of conversion in order to allow proper auto-zero function.) The positive transition generates a clear pulse which resets all internal logic (counters, etc.) and sets the clock enable, thus initiating the conversion sequence.

Integrate Input

During the first period, switch #4 is closed, (all others open), applying the input potential to the buffer. Since the amplifier offsets are stored on the auto-zero capacitor, the integrator's slope is determined solely by the input voltage. The input voltage is integrated for exactly 1000 counts, thus reaching an integrator output proportional to the integral of the input for a fixed time.

Integrate Reference

At the end of 1000 counts, switch #4 is opened, the polarity flip-flop is set, and the integrate reference period begins. Depending on the polarity, switch #5 or #6 is closed, connecting the buffer input to ground or $2V_{ref}$. This causes the integrator to ramp towards its quiescent (auto-zero) point with a slope proportional to $+V_{ref}$ or $-V_{ref}$. When the integrator crosses its quiescent auto-zero point, the comparator changes state, causing the zero crossing detector to generate a conversion complete signal which inhibits the clock and loads the logic information into the output latches. Switch #5 (or #6) is opened, switches #1, #2, and #3 are closed, and the system returns to a quiescent auto-zero mode, awaiting the next initiate conversion signal. If 2000 counts are received prior to zero crossing, an out-of-range signal is generated which sets the "out-of-range" output and resets the system.

Note 1: Internal reference out ≃ 1.8V, reference input = 1,000 volts for 1.999 volt scale and 100mV for 199.9mV scale.
Note 2: External components shown are suggested for 3 readings/sec.
Note 3: Parallel BCD outputs and other latched outputs are strobed at end of conversion and retain data until completion of next conversion.
Note 4: Start/Reset should remain Low during Auto-Zero. Conversion is initiated by a positive pulse on start pin.. (minimum width 100nsec).
Note 5: Component values ±20% typ.

FIGURE 1. 3½ DIGIT A/D CONVERTER FUNCTIONAL DIAGRAM

7101 Digital Processor Controls

Two pins are included on the 7101 that allow the user to externally control the gain of the converter. The first pin, "Internal Counter Override", if held high, will inhibit the carry pulse from the internal counter that switches the converter from signal integrate to reference integrate. As long as this input is high, the converter will remain in the signal integrate mode. At the same time, it enables the other pin, External Counter Input, to supply this transition pulse from external sources. One technique for changing the gain of the system would be to hold "Internal Counter Override" high through the first N carry pulses. This would increase the signal integrate time by a factor of N+1 and, thus, the sensitivity of the system by N+1. Since the number of suppressed pulses could be controlled digitally, the system could accomodate signals from ±2.000V to ±200.0mV (or lower, if time permits) without changing the external analog scale factor components. By using more complex external logic and both inputs, the user could digitally set offset (tare) and scale factor to convert voltages to physical units such as "degrees centigrade", "pounds", or "feet".

A "BUSY" pin is provided which permits interrogating the 8052/7101 to determine the status of the conversion. During the signal integrate and reference integrate periods, the "busy" line is high until the conversion is complete, at which time "busy" line goes low. This transition can be used to signal "new data available".

The "Apex" pin provides a digital signal which goes high during the reference integrate period.

"OUT-OF-RANGE" is indicated by a latched "low" on pin 23 for counts over 2000. The BCD digital values are "high" (true), except $\overline{1000}$ which is "low".

A positive polarity of the analog input signal is indicated by a "high" state at the output of the "polarity" latch on pin 22.

FIGURE 2.

The 7101 has an internal clock which requires a single capacitor between Pins 25 and 28 to operate. Figure 2 shows the typical capacitor value required to give the desired frequency.

During auto-zero, the clock is internally gated-off with Pin 28 high and Pin 25 low. When "start-reset" goes high, starting a measurement cycle, the clock starts counting with Pins 25 and 28 immediately changing phase. The counting continues until the end of the measurement cycle, at which time the clock is returned to its auto-zero condition.

In a typical application where visual readings are required, three readings per second is near the optimum speed. Faster readings make it difficult to resolve individual readings, while at slower rates the reader has to wait too long between measurements. In this application, 40% of the time (133mS) could be allocated to auto-zero and 60% (200mS) to signal and reference integrate. Since a measurement cycle consists of 3,000 clock pulses maximum, this dictates a clock frequency of 15kHz. Also, since the dual-slope technique of A/D conversion is not first-order dependent on clock frequency, the ±20% variation of clock frequency from unit-to-unit would result in no measurable error. However, in some applications, a more precise clock frequency would be desired. For instance, if precise rejection of 60Hz is required, the signal integrate phase (1,000 counts) would have to contain an integral number of 60Hz periods. For these applications, an external clock can be used by deleting the capacitor and connecting the external clock to Pin 25. However, if the clock is run asynchronously with start/reset, there will be one clock pulse of uncertainty in the integrate signal time, depending on where in the clock pulse period the start/reset went high. This will show up as one count of noise for signal near full-scale. This noise or jitter can be avoided by synchronizing the start/reset pulse to the negative-going edge of the external clock. Pin 33, Gated Clock Out, is a buffered output of the clock (internal or external) that is off (low) during auto-zero and in phase with Pin 25 during measurement.

Component Selection

Except for the reference voltage, none of the component values are first order important in determining the accuracy of the instrument. While this is undoubtedly an advantage of this approach, it does make the selection of nominal component values arbitrary at best. For instance, the reference capacitor and auto-zero capacitor are each shown as 1.0μfd. These relatively large values are selected to give greater immunity to PC board leakage since much smaller capacitors are adequate for charge injection errors or leakage errors from the 8052/7101.

The ratio of integrating resistor and capacitor is selected to give 9-volt swing for full-scale inputs. This is a compromise between possibly saturating the integrator (at ±14V) due to tolerance build-up between the resistor, capacitor, and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. Again, the .22μfd value for the integrating capacitor is selected for PC board considerations alone since the very small leakage at the integrator input is nulled at auto-zero. A very important characteristic of the integrating capacitor is low dielectric absorption. A polypropylene capacitor gave excellent results. In fact, a good test for dielectric absorption is to use the capacitor in this circuit with the input tied to reference. This ratiometric condition should read 1.000 and any deviation is probably due to dielectric absorption. In this ratiometric condition, a polycarbonate capacitor contributed an error of approximately 0.8 digit, polystyrene about 0.3 digit, and polypropylene less than 0.05 digit. The increased T.C. of polypropylene is of no consequence in this circuit. The dielectric absorption of the reference capacitor and auto-zero capacitor are only important at power on or when the circuit is recovering from an overload. Thus, smaller or cheaper capacitors can be used here if accurate readings are not required for the first few seconds of recovery.

The back-to-back diodes on the comparator output are recommended in the 200.0mV range to reduce the noise effects. In the normal operating mode, they offer a high impedance and long integrating time constant to any noise pulses charging the auto-zero capacitor. At start-up or recovery from an overload, their impedance is low to large signals so the capacitor can be charged in one auto-zero cycle. If only the 2.000V range is used, a 100k resistor in place of the back-to-back diodes is adequate for noise effects.

Maximum Clock Frequency

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. Even though the comparator in this circuit is all NPN with an open loop gain-bandwidth product of 300MHz, it is no exception. The comparator output follows the integrator ramp with a 3μS delay. At a clock frequency of 160kHz (6μS period), half of the first reference integrate period is lost in delay. This means that the meter reading will change from 0 to 1 with 50μV in, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at mid-point is considered desirable by most users. However, if the clock frequency is increased appreciably above this, the instrument will flash 1 on noise peaks even when the input is shorted.

Some circuits use positive feedback or a latch to solve the delay problem. However, unless the comparator voltage swing, the comparator gain, and the integrator gain are carefully controlled, this circuit can generate **anticipation** errors that greatly exceed the 3μS **delay** error. Also, it is very susceptible to noise spikes. A more controlled approach for extending the conversion rate is the use of a small resistor in the integrator feedback loop. This feeds a small pulse to the comparator to get it moving quickly and partially compensate for its delay.

The minimum clock frequency is established by leakage on the auto-zero and reference capacitor. With most devices, measurement cycles as long as 10 seconds gave no measurable leakage error.

APPLICATIONS

8052/7101 3½ Digit LCD DPM/DVM

Figure 3 illustrates an application where the 8052/7101 interfaces with a Liquid Crystal Display. The CD4054 and CD4055s are Liquid Crystal Display Drivers (4-segment and 7-segment, respectively) which provide the level shifting (up to $30V_{p-p}$ at $V_{DD}-V_{EE}$ = 15V) necessary to drive the LCD. Overrange is indicated by a special character. If blanking of any part of the display is required on overload, Pin 23 (7101) can be used to drive Pin 7 on those display drivers via an inverter and level shift such as CD4009 or 74C903 or another CD4054. Display applications requiring a plus sign rather than a blank indication for positive analog input levels (i.e., +1.999 versus 1.999) need to invert the "polarity" logic output level which is normally high for positive analog input signals.

FIGURE 3. 8052/7101 3½ DIGIT LCD DPM/DVM

8052/7101/6100/6101 Set

The circuit in Figure 4 interfaces the 8052/7101 A-to-D converter chip set to an IM6100* microprocessor, using the 6101* Parallel Interface Element. Hex Tri-state Buffers (e.g., MM80C95*) are used to control bus access from the 7101 during read operations.

Conversion is initiated by activating the WRITE 1 line (positive going). The converter pair will then convert the analog input to digital form, and latch the data in the 7101. The busy line will go low as the conversion ends, and this transition is sensed by the SENSE 1 line, triggering an interrupt. The interrupt routine should read the 12-line data word, and then the polarity, $\overline{1000}$ and out-of-range lines.

Sufficient time must be allowed for the auto-zero loop to settle before retriggering a conversion. Ten milliseconds of auto-zero is sufficient to null any offsets to 10 microvolts. At power-on or after an overload, 100 milliseconds is required to assure the auto-zero capacitor has charged to the correct value. This time delay may be implemented conveniently using the IM6102 (Memory Extender/Time Delay Device).

Some skeletal service routines for this connection are given on page 7 and 8.

*References:
Intersil IM6100 CMOS 12-bit Microprocessor
Intersil IM6101 Parallel Interface Element
National MM80C95 Hex CMOS Tri-State Buffers

FIGURE 4. 3½ DIGIT PARALLEL BCD DATA ACQUISITION SYSTEM

8052/7101/6100/6101 APPLICATION PROGRAM

A possible set-up and service routine for the connection is given below.

```
/ASSUME PIE SELECT IS SET TO 54, INTERRUPT VECTOR TO 2000
        (OCTAL)
/INITIALIZE ROUTINE: SET-UP FOR NO INTERRUPT

1200    7200                CLA
1201    1240                TAD SSCRA
1202    6545                WCRA 54          /SET-UP CONTROL REGISTER A
1203    7200                CLA
1204    1241                TAD SSCRB
1205    6555                WCRB 54          /SET-UP CONTROL REGISTER B
1206    7200                CLA
1207    1242                TAD SSVV
1210    6556                WVR 54           /SET-UP VECTOR REGISTER

1220    0000    CONVERT,    Ø                /INITIATE CONVERSION SUBROUTINE
1221    1243                TAD SSCRAI
```

1222	6545		WCRA 54	/SET-UP CONTROL REGISTER A
1223	6541		WRITE1 54	/THE WRITE PULSE STARTS CONVERSION
1224	5620		JMP I CONVERT	/RETURN
1240	0040	SSCRA,	0040	/WP 1 SET HI, IE1 SET LO
1241	0000	SCRRB,	0000	/SL1, SP1 SET LP, NEGATIVE EDGE SENSE
1242	2000	SSVV,	2000	/VECTOR ADDRESS
1243	0041	SSCRAI,	0041	/WPI SET HI, IE1 SET HI
0000	0000	INTRPT,	Ø	/ENTRY POINT FOR INTERRUPT
0001	6002		IOF	/DISABLE INTERRUPT, JUMP TO VECTOR ADDRESS
0140	0000	AD1,	Ø	/FIRST WORD OF DATA
0141	0000	AD2,	Ø	/SECOND WORD OF DATA
0160	0000	TEMP1,	Ø	/TEMPORARY STORAGE
2000	5210	VV,	JMP ATOD	/JUMP TO SERVICE POINT
2010	3160	ATOD,	DCA TEMP1	/SAVE AC
2011	6540		READ1 54	/READ BCD LINES
2012	3140		DCA AD1	/AND STORE
2013	6550		READ2 54	/READ POLARITY, 1000, AND OVERRANGE
2014	7040		CMA	/COMPLEMENT TO THE TRUE
2015	3141		DCA AD2	/AND STORE
/	– –	– – –	– – – –	/ANY OTHER WORK
2020	1160		TAD TEMP1	/RESTORE AC
2021	6001		ION	/RESTORE INTERRUPT
2022	5400		JMP I INTRPT	/RETURN

4

PACKAGE DIMENSIONS

14 Pin Plastic Dual-In-Line Package

14 Pin Ceramic Dual-In-Line Package

40 Pin Plastic Dual-In-Line Package

40 Pin Ceramic Dual-In-Line Package

INTERSIL

8052A/7103A 4½ Digit Pair
8052/7103 3½ Digit Pair

FEATURES

- Accuracy guaranteed to ±1 count over entire ±20,000 counts (8052A/7103A)
- Guaranteed zero reading for 0 volts input
- 5pA input current typical
- True polarity at zero count for precise null detection
- Single reference voltage required
- Over-range and under-range signals available for auto-ranging capability
- All outputs TTL compatible
- Medium quality reference (40ppm typical) on board
- Blinking display gives visual indication of over-range
- Six auxillary inputs/outputs are available for interfacing to UARTS, Microprocessors or other complex circuitry

GENERAL DESCRIPTION

The 8052A/7103A with its multiplexed BCD outputs and digit drivers is ideally suited for the visual display DVM/DPM market. Accuracy is outstanding with performance like: 5pA input leakage, auto-zero to 10μV with less than 1μV/°C drift; linearity of 0.002%; scale factor temperature coefficients of 3ppm/°C (with external reference). The system uses the time-proven dual-slope integration with all its advantages, i.e., non-critical components, high rejection of noise and a-c signals, non-critical clock frequency, almost perfect differential linearity and true ratiometric readings. At the same time it has reduced or eliminated many of the sources of error that have limited dual-slope accuracy. With the 8052A/7103A pairs, critical board layout is no longer required to give low charge injection by the switches and elaborate ground planes are not necessary to keep clock pulse transients out of the comparator circuit.

The 8052/7103 (3½ digit pair) features conversion rates from 1 measurement every 10 seconds to 30/second, making them ideally suited for a wide variety of applications.

FIGURE 1. FUNCTIONAL BLOCK DIAGRAM

ORDERING INFORMATION

3½ Digit Pair

Part	Temp. Range	Package	Order Number
8052	0°C to 70°C	14 pin plastic DIP	ICL8052CPD
8052	0°C to 70°C	14 pin ceramic DIP	ICL8052CDD
7103	0°C to 70°C	28 pin plastic DIP	ICL7103CPI
7103	0°C to 70°C	28 pin ceramic DIP	ICL7103CDI

4½ Digit Pair

Part	Temp. Range	Package	Order Number
8052A	0°C to 70°C	14 pin plastic DIP	ICL8052ACPD
8052A	0°C to 70°C	14 pin ceramic DIP	ICL8052ACDD
7103A	0°C to 70°C	28 pin plastic DIP	ICL7103ACPI
7103A	0°C to 70°C	28 pin ceramic DIP	ICL7103ACDI

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1)	500 mW
Storage Temperature	−65°C to +150°C
Operating Temperature	0°C to +70°C
Lead Temperature (Soldering, 60 Sec.)	300°C

8052, 8052A

Supply Voltage	±18V
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short Circuit Duration, All Outputs (Note 3)	Indefinite

7103, 7103A

Source Current (I_S)	100 mA
Drain Current (I_D)	100 mA
Digital Inputs	5 mA
V^+ to V^-	25V
Digital Input to V^+	V^- to V^+
Digital Input to V^-	V^+ to V^-

Note 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

SYSTEM ELECTRICAL CHARACTERISTICS

(V_{++} = +15V, V_+ = +5V, V_- = −15V Clock Frequency Set for 3 Reading/Sec)

CHARACTERISTICS	CONDITIONS	8052/7103(1)			8052A/7103A(2)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	V_{in} = 0.0V Full Scale = 2.000V	−0.000	±0.000	+0.000	−0.0000	±0.0000	+0.0000	Digital Reading
Ratiometric Reading (3)	$V_{in} \equiv V_{Ref.}$ Full Scale = 2.000V	+0.999	+1.000	+1.001	+0.9999	+1.0000	+1.0001	Digital Reading
Linearity over ± Full Scale (error of reading from best straight line)	$-2V \leqslant V_{in} \leqslant +2V$		0.2	1		0.5	1	Digital Count Error
Differential Linearity (difference between worse case step of adjacent counts and ideal step	$-2V \leqslant V_{in} \leqslant +2V$		.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \equiv +V_{in} \approx 2V$		0.2	1		0.5	1	Digital Count Error
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 200.0mV Full scale = 2.000V		20 50			 30		μV
Leakage Current at Input	V_{in} = 0V		5	30		3	10	pA
Zero Reading Drift	V_{in} = 0V $0° \leqslant T_A \leqslant 70°C$		1	5		0.5	2	μV/°C
Scale Factor Temperature Coefficient	V_{in} = +2V $0 \leqslant T_A \leqslant 70°C$ (ext. ref. 0 ppm/°C)		3	15		2	5	ppm/°C

(1) Tested in 3½ digit (2,000 count) circuit shown in Fig. 3 clock frequency 12 kHz. Pin 2 7103 connected to Gnd.

(2) Tested in 4½ digit (20,000 count) circuit shown in Fig. 3 clock frequency 120 kHz. Pin 2 7103A open.

(3) Tested with a low dielectric absorbtion integrating capacitor. See Component Selection Section.

8052 ELECTRICAL CHARACTERISTICS (V_S = ±15V unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8052			8052A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
EACH OPERATIONAL AMPLIFIER								
Input Offset Voltage	V_{CM} = 0V		20	50		20	50	mV
Input Current (either input)	V_{CM} = 0V		5	50		2	10	pA
Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
Non-Linear Component of Common-Mode Rejection Ratio*	V_{CM} = ±2V		110			110		
Large Signal Voltage Gain	R_L = 10kΩ	20,000			20,000			V/V
Slew Rate			6			6		V/μs
Unity Gain Bandwidth			1			1		MHz
Output Short-Circuit Current			20	100		20	100	mA
COMPARATOR AMPLIFIER								
Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
Positive Output Voltage Swing		+12	+13		+12	+13		V
Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
VOLTAGE REFERENCE								
Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
Output Resistance			5			5		ohms
Temperature Coefficient			50			40		ppm/°C
Supply Current Total			6	12		6	12	mA

*This is the only component that causes error in dual-slope converter.

7103 AND 7103A ELECTRICAL CHARACTERISTICS (V^+ = +5.0, V^- = −15V, Ta = 25°C)

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUTS	Clock In, Run/Hold, 4½/3½	I_{inL}	V_{in} = 0		.2	.6	mA
		I_{inH}	V_{in} = +5V		.1	10	μA
	Comp. In	I_{inL}	V_{in} = 0		.1	10	μA
		I_{inH}	V_{in} = +5V		.1	10	μA
OUTPUTS	All Outputs	V_{OL}	I_{OL} = 1.6ma		.25	.40	V
	B_1, B_2, B_4, B_8 D_1, D_2, D_3, D_4, D_5	V_{OH}	I_{OH} = −1mA	2.4	4.2		V
	Busy, Strobe, Over-range, Under-range Polarity	V_{OH}	I_{OH} = −10μA	4.9	4.99		V
SWITCH	Switches 1, 3, 4, 5, 6	$R_{DS\ ON}$			400		Ω
	Switch 2	$R_{DS\ ON}$			1200		Ω
	Switch Leakage (All)	$I_{D\ OFF}$			2		pA
SUPPLY	+5V Supply Current	I_{CC+}			20	30	mA
	−15V Supply Current	I_{CC-}			4	6	mA

4

THEORY OF OPERATION

Figure 1 shows a function diagram for an A/D converter using the 8052/7103 pair. In this circuit, each measurement cycle is divided into four equal parts. The first part, phase 1, is the auto-zero cycle. The switch driver decoder recognizes this state and turns on hex switches number 1, 2, and 3. Switches 1 and 2 impress a voltage equal to V_{REF} across the reference capacitor. Switch 3 closes a loop around the integrator and comparator. The purpose of this loop is to charge up the auto-zero capacitor until the integrator output does not change with time. During the second part, Phase 2, switches 1, 2 and 3 are opened and switch 4 is closed. If the input voltage is zero, the buffer, integrator and comparator will see the same voltages that existed in the previous state. Thus, the integrator output will not change but will remain stationary during the entire signal-integrate cycle. If V_{IN} is not equal to zero, an unbalanced condition exists compared to the auto-zero cycle and the integrator will generate a ramp whose slope is proportional to V_{IN}. At the end of this cycle, the sign of the ramp is latched into the polarity F/F. The final part, reference integrate, includes phases 3 & 4. The switch driver decoder uses the output of the polarity F/F in deciding whether to close switch 5 or 6. If the input signal was positive, switch 6 is closed and a voltage which is V_{REF} more negative than during auto-zero is impressed on the buffer input. If the input signal was negative switch 5 is closed and a voltage which is V_{REF} more positive than during auto-zero is impressed on the buffer input. Thus, the reference capacitor generates the equivalent of a (+) reference or a (−) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to zero. The time, or number of counts, required to do this is porportional to the input voltage. Since the reference cycle can be twice as long as the signal integrate cycle, the input voltage required to give a full scale reading $\equiv 2\ V_{REF}$. The circuit, as described to this point, is not new to this application. It has been used successfully for several years. However, this system makes three major contributions to the accuracy of this circuit. These are: (1) low charge injection, (2) junction FET op amp, and (3) zero-crossing flip-flop.

1. Low Charge Injection.

During auto-zero, there is no problem in charging the capacitors to the correct voltage. The problem is getting the switches off without changing this voltage. As the gate is driven off, the gate-to-drain capacitance of the switch injects a charge on the reference or auto-zero capacitor, changing its voltage. The designer, using discrete components, is forced into critical board layouts where charges of opposite polarity are injected to compensate or neutralize the driver injection. This balance will be upset by any unit-to-unit variation of switch capacitance so at best the final design is a compromise. In the 8052/7103 the critical layout has been done on the semiconductor chip and need not concern the user. Also, since a silicon-gate process is used for the switches, the unit-to-unit variation is extremely low. The net result is to give an error due to charge injection that is so low it is difficult to measure; but certainly less than 5μV referred to the input.

2. Junction FET Op Amps.

Both the buffer and integrator use junction FET inputs in a guarded circuit that reduces the voltage across the FET to 3 or 4 volts. At this voltage level, input leakage currents of 2 pA are typical. For typical component values 2 pA leakage contributes less than 2μV of error to the circuit. In theory, MOS FET's would contribute less leakage but their increased noise would more than swamp out any improvement.

3. Zero-Crossing Flip Flop.

The problem that the zero-crossing flip-flop is designed to solve is shown in figure 2.

FIGURE 2. INTEGRATOR OUTPUT NEAR ZERO-CROSSING

The integrator output is approaching the zero-crossing point where the clock will be stopped and the reading displayed. The clock pulse feedthrough superimposed upon this ramp will cause a false reading by stopping the count prematurely. For a 20,000 count instrument, the ramp is changing approximately 0.50mV per clock pulse (10 volt max integrator output divided by 20,000 counts). The clock pulses have to be less than 100μV peak to avoid causing significant errors. The circuit layout to achieve this can be time consuming at best and impossible at worst. The suggested circuit gets around this problem by feeding the zero-crossing information into a flip-flop instead of using it directly. The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. Any false zero-crossing caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by one count in every instance. If a correction was not made, the display would always be one count too high. The correction is to disable the counter for one clock pulse at the beginning of phase 3. This one count delay compensates for the delay of the zero-crossing flip-flop and allows the correct number to be latched into the display. Similarly, a one count delay at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2 so that true ratiometric readings are possible.

APPLICATIONS

Specific Circuits Using the 8052A/7103A

Figure 3 shows the complete circuit for a 4½ digit (±2.000V) full scale) A/D with LED readout using the internal reference of the 8052A. If an external reference is used, the reference supply (pin 7) should be connected to ground and the 300pF reference cap deleted. The circuit also shows a typical R-C input filter. Depending on the application, the time-constant of this filter can be made faster, slower or the filter deleted completely. The ½ digit LED is driven off of the 7 segment decoder with a zero reading blanked by connecting a D5 signal to RBI input of the decoder.

A voltage translation network is connected between the comparator output of the 8052A and the auto-zero input of the 7103A. The purpose of this network is to assure that, during auto-zero, the output of the comparator is at or near the threshold of the 7103A logic (+2.5V) while the auto-cap is being charged to V_{REF} (+1.0 volts for a 2.000V instrument). Otherwise, even with zero volts in, some reference integrate period would be required to drive the comparator output to the threshold level. This would show up as an equivalent offset error. Once the divider network has been selected, the unit-to-unit variation should contribute less than a tenth of a count error. A second feature of the network is that it holds the source of switch 3 to ≈ +4V during the integrate and deintegrate cycles of positive input voltages. During this time, the comparator output is clamped by an internal diode on the 7103A to ≈ +5.7 volts. Since the gate of switch 3 is at +5 volts for this off condition, the +1 volt Vgs of the FET assures the switch is off to the 1 or 2 pA leakage level. Finally, the back-to-back diodes are used to lower noise. In the normal operating mode they offer a high impedance and long integrating time constant to any noise pulses charging the auto-zero cap. At startup or recovery from an overload, their impedance is low to large signals so that the cap can be charged up in one auto-zero cycle.

FIGURE 3. 8052A/7103A 4½ DIGIT A-D CONVERTER

Component Selection

Except for the Reference Voltage, none of the component values are first-order important in determining the accuracy of the instrument. While this is undoubtedly an advantage of this approach, it does make the selection of nominal component values arbitrary at best. For instance the reference capacitor and auto-zero capacitor are each shown as 1.0μF. These relative large values are selected to give greater immunity to PC board leakage since smaller capacitors are adequate for charge injection errors or leakage errors from the 8052/7103. The ratio of integrating resistor and capacitor is selected to give 9 volt swing for full scale inputs. This is a compromise between possibly saturating the integrator (at ±14 volts) due to tolerance build-up between the resistor, capacitor and clock and the errors a lower voltage swing could induce due to offsets referred to the output of the comparator. Again the .22μF value for the integrating cap is selected for PC considerations alone since the very small leakage at the integrator input is nulled at auto-zero. A very important characteristic of the integrating cap is low dielectric absorption. A polypropylene cap gave excellent results in the application. In fact a good test for dielectric absorption is to test the subject cap in this circuit with the input tied to reference. This ratiometric condition should read 1.0000 and any deviation is probably due to dielectric absorption. In this test poly-carbonate caps typically read .9992, polystyrene, .9997 and polypropylene, 1.0000. The increased temperature coefficient of polypropylene is of no consequence in this circuit. The dielectric absorption of the reference cap and auto-zero cap are only important at power-on or when the circuit is recovering from an overload. Thus, smaller or cheaper caps can be used here if accurate readings are not required for the first few seconds of recovery.

Max Clock Frequency

The maximum conversion rate of most dual-slope A-D converters is limited by the frequency response of the comparator. Even though the comparator in this circuit is all NPN with an open-loop gain-bandwidth product of 300MHz, it is no exception. The comparator output follows the integrator ramp with a 3μS delay. At a clock frequency of 160kHz (6μS period) half of the first reference integrate period is lost in delay. This means that the meter reading will change from 0 to 1 with 50μV in, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at midpoint is considered desirable by most users. However, if the clock frequency is increased appreciably above this, the instrument will flash "1" on noise peaks even when the input is shorted.

For many dedicated applications where the input signal is always one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, up to 500kHz clock rate may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

The minimum clock frequency is established by leakage on the auto-zero and reference cap. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

AUXILIARY INPUTS/OUTPUTS

The 7103 and 7103A include several pins that allow them to operate conveniently in more sophisticated systems. These include:

1. 4½/3½ (Pin 2). When high (or open) the internal counter operates as a full 4½ decade counter with a complete measurement cycle requiring 40,000 counts. When held low, the least significant decade is cleared and the clock is fed directly into the next decade. A measurement cycle now requires only 4000 clock pulses. All 5 digit drivers are active in either case with each digit lasting 200 counts with pin 2 high (4½ digit) and 20 counts for pin 2 low (3½ digit). The only difference between 7103A and 7103 is that they were tested with this pin high and low respectively. Actually, most 7103 will operate satisfactorily in a 4½ digit application. They simply have not received the more complex testing required to prove it.

2. Run/Hold (Pin 4). When high (or open) the A/D will free-run with equally spaced measurement cycles every 40,000/4,000 clock pulses. If taken low, the converter will continue the full measurement cycle that it is in and then hold this reading as long as pin 4 is held low. A short positive pulse (greater than 300ns) will now initiate a new measurement cycle beginning with 10,000/1,000 counts of auto zero. Of course if the pulse occurs before the full measurement cycle (40,000/4,000 counts) is completed, it will not be recognized and the converter will simply complete the measurement it is in. An external indication that a full measurement cycle has been completed is that the first strobe pulse (see below) will occur 100/10 counts after the end of this cycle. Thus, if Run/Hold is low and has been low for at least 100/10 counts, the converter is holding and ready to start a new measurement when pulsed high.

3. $\overline{\text{Strobe}}$ (Pin 18). This is a negative going output pulse that aids in transferring the BCD data to external latches, UARTs or microprocessors. There are 5 negative going $\overline{\text{Strobe}}$ pulses that occur in the center of each of the digit drive pulses and occur once and only once for each measurement cycle starting 100/10 pulses after the end of the full measurement cycle. Digit 5 (MSD) goes high at the end of the measurement cycle and stays on for 200/20 counts. In the center of this digit pulse (to avoid race conditions between changing BCD and digit drives) the first $\overline{\text{Strobe}}$ pulse goes negative for ½ clock pulse width. Similarly, after 200/20 clock pulses, digit 4 goes high and 100/10 pulses later the $\overline{\text{Strobe}}$ goes negative for the second time. This continues through digit 1 (LSD) when the fifth and last $\overline{\text{Strobe}}$ pulse is sent. The digit drive will continue to scan (unless the previous signal was over-range) but no additional $\overline{\text{Strobe}}$ pulses will be sent until a new measurement is available.

FIGURE 4. TIMING DIAGRAM

4. Busy (Pin 28). Busy goes high at the beginning of signal integrate and stays high until the first clock pulse after zero-crossing (or after end of measurement in the case of an over-range). The internal latches are enabled (i.e., transferred during the first clock pulse after busy and are latched at the end of this clock pulse. The circuit automatically reverts to auto-zero when not BUSY so it may also be considered a $\overline{A\text{-}Z}$ signal. A very simple means for transmitting the data down a single wire pair from a remote location would be to AND BUSY with clock and subtract 10,001/1,001 counts from the number of pulses received (as mentioned previously there is one NO count pulse in each reference integrate (cycle).

5. Over-range (Pin 14). This pin goes positive when the input signal exceeds the range (20,000/2,000) of the converter. The output F-F is set at the end of Busy and is reset to zero at the beginning of Reference integrate in the next measurement cycle.

6. Under-range (Pin 13). This pin goes positive when the reading is 9% of range or less. The output F-F is set at the end of busy (if the new reading is 1800/180 or less) and is reset at the beginning of signal integrate of the next reading.

7. Polarity (Pin 3). This pin is positive for a positive input signal. It is valid even for a zero reading. In other words, +0000 means the signal is positive but less than the least significant bit. The converter can be used as a null detector by forcing equal (+) and (–) readings. The null at this point should be less than 0.1 LSB. This output becomes valid at the beginning of reference integrate and remains correct until it is re-validated for the next measurement.

8. Digit Drives (Pins 19, 24, 25, 26 and 27). The digit drives are a positive going signal that each last for 200/20 clock pulses. The scan sequence is D_5 (MSD), D_4, D_3, D_2 and D_1 (LSD). All five digits are scanned even when operating in the 3½ digit mode. The scan is continuous unless an over-range occurs. Then all digit drives are blanked from the end of the strobe sequence until the beginning of Reference Integrate when D_5 will start the scan again. This gives a blinking display as a visual indication of over-range.

9. BCD (pins 20, 21, 22 and 23). The Binary coded Decimal bits B_8, B_4, B_2 and B_1 are positive logic signals that go on simultaneously with the digit driver.

INTERFACING WITH UARTS AND MICROPROCESSORS

Figure 5 shows a very simple interface between a free-running 8052A/7103A and a UART. The five $\overline{\text{Strobe}}$ pulses start the transmission of the five data words. The digit 5 word is 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. Also the polarity is transmitted indirectly by using it to drive the Even Parity Enable Pin (EPE). If EPE of the receiver is held low, a parity flag at the receiver can be decoded as a positive signal, no flag as negative.

FIGURE 5. SIMPLE 7103/7103A TO UART INTERFACE

A more complex arrangement is shown in Fig. 6. Here the UART can instruct the A/D to begin a measurement sequence by a word on RRI. The Busy signal resets the Data Ready Reset (DRR). Again $\overline{\text{Strobe}}$ starts the transmit sequence. A quad 2 input multiplexer is used to superimpose polarity, over-range, and under-range onto the D_5 word since in this instance it is known that $B_2 = B_4 = B_8 = 0$.

FIGURE 6. COMPLEX 7103/7103A TO UART INTERFACE

Circuits for the 7103/7103A to interface directly with three popular microprocessors are shown in Figures 7, 8 and 9. The main differences in the circuits are that IM6100 with its 12 bit word capability can accept polarity, over-range, under-range, 4 bits of BCD and 5 digits simultaneously where the 8080 and the MC6800 with 8 bits words need to have polarity, over-range and under-range multiplexed onto the Digit 5 word – as in the UART circuits. In each case the microprocessor can instruct the A/D when to begin a measurement and when to hold this measurement.

FIGURE 7. IM6100 TO 7103/7103A INTERFACE

FIGURE 8. Mc6800 TO 7103/7103A INTERFACE

FIGURE 9. INTEL 8080 TO 7103/7103A INTERFACE

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PACKAGE DIMENSIONS

14 Pin Plastic Dual-In-Line Package

14 Pin Ceramic Dual-In-Line Package

28 Pin Plastic Dual-In-Line Package

28 Pin Ceramic Dual-In-Line Package

INTERSIL

ICL8068A/ICL7103B 4½ Digit
ICL8068/ICL7103 3½ Digit
Precision A/D Converter

FEATURES

- Typically less than 2μV p-p noise (200.00mv full scale)
- Accuracy guaranteed to ±1 count over entire ±20,000 counts (2.0000 volts full scale)
- Guaranteed zero reading for 0 volts input
- True polarity at zero count for precise null detection
- Single reference voltage required
- Over-range and under-range signals available for auto-ranging capability
- All outputs TTL compatible
- Medium quality reference (40ppm typical) on board
- Blinking display gives visual indication of over-range
- Six auxillary inputs/outputs are available for interfacing to UARTs, Microprocessors or other complex circuitry

GENERAL DESCRIPTION

The 8068A/7103B is the latest addition to Intersil's growing family of A/D converters. With the 8068 low noise B-FET process, is ideally suited for low voltage, low impedance applications. When used in a 200.00mV full scale configuration, it will give 10μV/count resolution with 2μV p-p noise. At the same time it has the dynamic range to handle signals as large as +3 volts or −5volts with excellent linearity. The system uses the time-proven dual-slope integration technique with all its advantages, i.e., non-critical components, high rejection of noise and AC signals, non-critical clock frequency, almost perfect differential linearity and true ratiometric readings.

When only 2000 counts of resolution are required the 7103 can be wired for 3-1/2 digits and give up to 30 readings/second making it ideally suited for a wide variety of applications.

Figure 1. Functional Block Diagram

ORDERING INFORMATION

3-1/2 Digit Pair

Part	Temp.Range	Package	Order Number
8068	0°C to 70°C	14 pin plastic DIP	ICL8068CPD
8068	0°C to 70°C	14 pin ceramic DIP	ICL8068CDD
7103	0°C to 70°C	28 pin plastic DIP	ICL7103CPI
7103	0°C to 70°C	28 pin ceramic DIP	ICL7103CDI

4-1/2 Digit Pair

Part	Temp.Range	Package	Order Number
8068A	0°C to 70°C	14 pin plastic DIP	ICL8068ACPD
8068A	0°C to 70°C	14 pin ceramic DIP	ICL8068ACDD
7103B	0°C to 70°C	28 pin plastic DIP	ICL7103BCPI
7103B	0°C to 70°C	28 pin ceramic DIP	ICL7103BCDI

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 500 mW
Storage Temperature ..... −65°C to +150°C

8068, 8068A

Supply Voltage ..... ±18V
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±15V
Output Short Circuit Duration,
All Outputs (Note 3) ..... Indefinite
Operating Temperature ..... 0°C to +70°C
Lead Temperature (Soldering, 60 Sec.) ..... 300°C

7103, 7103B

Source Current (I_S) ..... 100 mA
Drain Current (I_D) ..... 100 mA
Digital Inputs ..... 5 mA
V^+ to V^- 25V
Digital Input to V^+ ..... V^- to V^+
Digital Input to V^- ..... V^+ to V^-

Note 1: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below +70°C. For higher temperatures, derate 10mW/°C.
2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3: Short circuit may be to ground or either supply. Rating applies to +70°C ambient temperature.

SYSTEM ELECTRICAL CHARACTERISTICS

(V_{++} = +15V, V_+ = +5V, V_- = −15V, T_A = 25°C, Clock Frequency Set for 3 Reading/Sec)

CHARACTERISTICS	CONDITIONS	8068/7103(1)			8068A/7103B(2)			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Zero Input Reading	V_{in} = 0.0V Full Scale = 200.00mV	−00.00	±00.00	+00.00	−00.00	±00.00	+00.00	Digital Reading
Ratiometric Reading(3)	V_{in} = V_{Ref} Full Scale = 2.000V	+0.999	+1.000	+1.001	+0.9999	+1.0000	+1.0001	Digital Reading
Linearity over ± Full Scale (error of reading from best straight line)	$-2V \le V_{in} \le +2V$		0.2	1		0.5	1	Digital Count Error
Differential Linearity (difference between worse case step of adjacent counts and ideal step)	$-2V \le V_{in} \le +2V$		.01			.01		LSB
Rollover error (Difference in reading for equal positive & negative voltage near full scale)	$-V_{in} \approx +V_{in} \approx 2V$		0.2	1		0.5	1	Digital Count Error
Noise (P-P value not exceeded 95% of time)	V_{in} = 0V Full scale = 200.0mV		3			2		μV
Leakage Current at Input	V_{in} = 0V		200	300		100	200	pA
Zero Reading Drift	V_{in} = 0V $0° \le T_A \le 50°C$ (4)		1	5		0.5	2	μV/°C
Scale Factor Temperature Coefficient	V_{in} = +2V $0 \le T_A \le 50°C$ (4) (ext. ref. 0 ppm/°C)		3	15		2	5	ppm/°C

Note 1: Tested in 3-1/2 digit (2,000 count) circuit shown in Fig. 3 clock frequency 12 kHz. Pin 2 7103 connected to Gnd.
2: Tested in 4-1/2 digit (20,000 count) circuit shown in Fig. 3 clock frequency 120 kHz. Pin 2 7103A open.
3: Tested with a low dielectric absorption integrating capacitor. See Component Selection Section.
4: The temperature range can be extended to +70°C and beyond as long as the auto-zero and reference capacitors are increased to absorb the higher leakage of the 8068.

8068 ELECTRICAL CHARACTERISTICS (V_S = ±15V unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8068 MIN	8068 TYP	8068 MAX	8068A MIN	8068A TYP	8068A MAX	UNITS
EACH OPERATIONAL AMPLIFIER								
Input Offset Voltage	V_{CM} = 0V		20	65		20	65	mV
Input Current (either input) (Note 1)	V_{CM} = 0V		175	250		80	150	pA
Common-Mode Rejection Ratio	V_{CM} = ±10V	70	90		70	90		dB
Non-Linear Component of Common-Mode Rejection Ratio* (Note 2)	V_{CM} = ±2V		110			110		dB
Large Signal Voltage Gain	R_L = 50kΩ	20,000			20,000			V/V
Slew Rate			6			6		V/μs
Unity Gain Bandwidth			2			2		MHz
Output Short-Circuit Current			5	10		5	10	mA
COMPARATOR AMPLIFIER								
Small-signal Voltage Gain	R_L = 30kΩ		4000					V/V
Positive Output Voltage Swing		+12	+13		+12	+13		V
Negative Output Voltage Swing		−2.0	−2.6		−2.0	−2.6		V
VOLTAGE REFERENCE								
Output Voltage		1.5	1.75	2.0	1.60	1.75	1.90	V
Output Resistance			5			5		ohms
Temperature Coefficient			50			40		ppm/°C
±15V Supply Range		±12	±15	±18	±12	±15	±18	Volts
Supply Current Total			8	14		8	14	mA

Note 1: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_J = T_A + \Theta jA$ Pd where ΘjA is the thermal resistance from junction to ambient.

2: This is the only component that causes error in dual-slope converter.

7103 AND 7103B ELECTRICAL CHARACTERISTICS (V+ = +5.0V, V− = −15V, Ta = 25°C)

	PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
INPUTS	Clock In, Run/Hold, 4-1/2/3-1/2	I_{inL} I_{inH}	V_{in} = 0 V_{in} = +5V		.2 .1	.6 10	mA μA
	Comp. In	I_{inL} I_{inH}	V_{in} = 0 V_{in} = +5V		.1 .1	10 10	μA μA
OUTPUTS	All Outputs	V_{OL}	I_{OL} = 1.6ma		.25	.40	V
	B_1,B_2,B_4,B_8 D_1,D_2,D_3,D_4,D_5	V_{OH}	I_{OH} = −1mA	2.4	4.2		V
	Busy, Strobe, Over-range, Under-range Polarity	V_{OH}	I_{OH} = −10μA	4.9	4.99		V
SWITCH	Switches 1,3,4,5,6	$R_{DS\ ON}$			400		Ω
	Switch 2	$R_{DS\ ON}$			1200		Ω
	Switch Leakage (All)	$I_{D\ OFF}$			2		pA
SUPPLY	+5V Supply Range			+4	+5	+6	Volts
	−15V Supply Range			−12	−15	−18	Volts
	+5V Supply Current	I_{CC+}			20	30	mA
	−15V Supply Current	I_{CC-}			4	6	mA

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THEORY OF OPERATION

Figure 1 shows a function diagram for an A/D converter using the 8068/7103 pair. In this circuit, each measurement cycle is divided into four equal parts. The first part, phase 1, is the auto-zero cycle. The switch driver decoder recognizes this state and turns on hex switches number 1, 2, and 3. Switches 1 and 2 impress a voltage equal to V_{REF} across the reference capacitor. Switch 3 closes a loop around the integrator and comparator. The purpose of this loop is to charge up the auto-zero capacitor until the integrator output does not change with time. During the second part, Phase 2, switches 2, 3 and 3 are opened and switch 4 is closed. If the input voltage is zero, the buffer, integrator and comparator will see the same voltages that existed in the previous state. Thus, the integrator output will not change but will remain stationary during the entire signal-integrate cycle. If V_{IN} is not equal to zero, an unbalanced condition exists compared to the auto-zero cycle and the integrator will generate a ramp whose slope is proportional to V_{IN}. At the end of this cycle, the sign of the ramp is latched into the polarity F/F. The final part, reference integrate, includes phases 3 & 4. The switch driver decoder uses the output of the polarity F/F in deciding whether to close switch 5 or 6. If the input signal was positive, switch 6 is closed and a voltage which is V_{REF} more negative than during auto-zero is impressed on the buffer input. If the input signal was negative switch 5 is closed and a voltage which is V_{REF} more positive than during auto-zero is impressed on the buffer input. Thus, the reference capacitor generates the equivalent of a (+) reference or a (−) reference from the single reference voltage with negligible error. The reference voltage returns the output of the integrator to zero. The time, or number of counts, required to do this is proportional to the input voltage. Since the reference cycle can be twice as long as the signal integrate cycle, the input voltage required to give a full scale reading = 2 V_{REF}. The circuit, as described to this point, is not new to this application. It has be used successfully for several years. However, this system makes three major contributions to the accuracy of this circuit. These are: (1) low charge injection, (2) low noise Bi-FET op amp, and (3) zero-crossing flip-flop.

4

1. Low Charge Injection.

During auto-zero, there is no problem in charging the capacitors to the correct voltage. The problem is getting the switches off without changing this voltage. As the gate is driven off, the gate-to-drain capacitance of the switch injects a charge on the reference or auto-zero capacitor, changing its voltage. The designer, using discrete components, is forced into critical board layouts where charges of opposite polarity are injected to compensate or neutralize the driver injection. This balance will be upset by any unit-to-unit variation of switch capacitance so at best the final design is a compromise. In the 8068/7103 the critical layout has been done on the semiconductor chip and need not concern the user. Also, since a silicon-gate process is used for the switches, the unit-to-unit variation is extremely low. The net result is to give an error due to charge injection that is so low it is difficult to measure; but certainly less than 5μV referred to the input.

2. Bi-FET Op Amps.

Both the buffer and integrator use low noise Bi-FET inputs in a configuration that minimizes the noise voltage generated. The main contribution to system noise is the residual noise trapped on the auto-zero capacitor when the switch opens. With typically 2μV of noise, the low noise of the Bi-FET 8068 keeps this error to a minimum.

3. Zero-Crossing Flip Flop.

The problem that the zero-crossing flip-flop is designed to solve is shown in figure 2.

Figure 2. Integrator Output Near Zero-Crossing

The integrator output is approaching the zero-crossing point where the clock will be stopped and the reading displayed. The clock pulse feedthrough superimposed upon this ramp will cause a false reading by stopping the count prematurely. For a 20,000 count instrument, the ramp is changing approximately 0.50mV per clock pulse (10 volt max integrator output divided by 20,000 counts). The clock pulses have to be less than 100μV peak to avoid causing significant errors. The circuit layout to achieve this can be time consuming at best and impossible at worst. The suggested circuit gets around this problem by feeding the zero-crossing information into a flip-flop instead of using it directly. The flip-flop interrogates the data once every clock pulse after the transients of the previous clock pulse and half-clock pulse have died down. Any false zero-crossing caused by clock pulses are not recognized. Of course, the flip-flop delays the true zero-crossing by one count in every instance. If a correction was not made, the display would always be one count too high. The correction is to disable the counter for one clock pulse at the beginning of phase 3. This one count delay compensates for the delay of the zero-crossing flip-flop and allows the correct number to be latched into the display. Similarly, a one count delay at the beginning of phase 1 gives an overload display of 0000 instead of 0001. No delay occurs during phase 2 so that true ratiometric readings are possible.

APPLICATIONS

Specific Circuits Using the 8068A/7103B.

Figure 3 shows the complete circuit for a ±4-1/2 digit (±200.0mV full scale) A/D with LED readout using the internal reference of the 8068A. If an external reference is used, the reference supply (pin 7) should be connected to ground and the 300pF reference cap deleted. The circuit also shows a typical R-C input filter. Depending on the application, the time-constant of this filter can be made faster, slower or the filter deleted completely. The 1/2 digit LED is driven from the 7 segment decoder with a zero reading blanked by connecting a D5 signal to RBI input of the decoder.

A voltage translation network is connected between the comparator output of the 8068A and the auto-zero input of the 7103B. The purpose of this network is to assure that, during auto-zero, the output of the comparator is at or near the threshold of the 7103B logic (+2.5V) while the auto-zero capacitor is being charged to V_{REF} (+100.0mV for a 200.0mV instrument). Otherwise, even with zero volts in, some reference integrate period would be required to drive the comparator output to the threshold level. This would show

up as an equivalent offset error. Once the divider network has been selected, the unit-to-unit variation should contribute less than a tenth of a count error. A second feature of the network is that it holds the source of switch 3 to approximately +4V during the integrate and deintegrate cycles of positive input voltages. During this time, the comparator output is clamped by an internal diode on the 7103B to approximately +5.7V volts. Since the gate of switch 3 is at +5 volts for this off condition, the +1 volt Vgs of the FET assures the switch is off to the 1 or 2pA typical leakage level. Finally, the back-to-back diodes are used to lower the noise. In the normal operating mode they offer a high impedance and long integrating time constant to any noise pulses charging the auto-zero cap. At startup or recovery from an overload, their impedance is low to large signals so that the cap can be charged up in one auto-zero cycle. Therefore the circuit is identical to the 2.0000V scale for the 8052A/7103A (see ICL8052/ICL7103 data sheet for details). However, there are three changes to operate the 8068A at 200.00mV.

1. The buffer is run at a gain of 10 with the 90K, 10K voltage divider inserted in the (−) input of the 8068A. The gain does not have to be set precisely at 10 since the gain of the buffer is used both in the integrate and deintegrate phase.
2. The reference cap is increased to 10μF. Since the reference voltage is 100mV instead of 1V this capacitor is ten times as sensitive to leakage droop or charge injection.
3. A low cost diode (IN914 or equivalent) is required to clamp the comparator output for negative going signals. Without this clamp, the thermal dissipation of the comparator would be different in negative saturation than at auto-zero voltages. This would induce an offset in the comparator causing a different zero crossing at the auto-zero value and therefore an error for minus input signal. This diode is used on all scales of the 8068A.

Other Circuits Using the 8068A.

For optimum performance, care must be taken in the selection of values for the integrating capacitor and resistor, reference capacitor and conversion rate. These values must be selected to suit the particular application.

The most important consideration is that the integrator output swing (for full scale input) be as large as possible. This will reduce errors due to the comparator such as noise and thermal induced offsets. For ±15V supplies a ±10V integrator swing is recommended. For 100kHz clock (2-1/2 reading/sec) a 100K integrating resistor and .22μF capacitor should be used. For different frequencies the capacitor should be changed to keep a ±10V swing. For scale factors other than 200.00mV the gain of the buffer should be changed to give a ±2V buffer output. For 2.0000V full scale this means unity gain and for 20,000mV (1μV resolution) a gain of 100 is necessary. Not all 8068A can operate properly at a gain of 100 since their offset should be less than 10mV in order to accommodate the auto-zero circuitry. However, for devices selected with less than 10mV offset, the noise performance is reasonable with approximately 0.7μV p-p noise around zero, increasing linearly to approximately 1.5μV near full scale. On all scales less than 200.00mV, the voltage translation network should be made adjustable as an offset trim.

The auto-zero cap should be 1μF for all scales and the reference capacitor should be 1μF times the gain of the buffer amplifier. At this value if the input leakages of the 8068A are equal, the droop effects will cancel giving zero offset. This is especially important at high temperature. Finally the integrating capacitor should have low dielectric absorption. Polypropylene capacitors give negligible errors at reasonable cost. A good test for dielectric absorption is to test the subject capacitor in this circuit with the input tied to reference. This ratiometric condition should read 1.0000 and any deviation is probably due to dielectric absorption. In this test polycarbonate capacitor typically read .9992, polystyrene, .9997 and polypropylene, 1.0000. The increased temperature coefficient of polypropylene is of no consequence in this circuit. The dielectric absorption of the reference capacitor and auto-zero capacitor are only important at power-on or when the circuit is recovering from

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*For finer resolution on scale factor adjust, use a 10 turn pot or a small pot in series with a fixed resistor.

Figure 3. 8068A/7103B 4-1/2 Digit A-D Converter

an overload. Thus, smaller or cheaper capacitors can be used here if accurate readings are not required for the first few seconds of recovery.

Max Clock Frequency

The maximum conversion rate of most dual-slope A/D converters is limited by the frequency response of the comparator. Even though the comparator in this circuit is all NPN with an open-loop gain-bandwidth product of 300MHz, it is no exception. The comparator output follows the integrator ramp with a 3μs delay. At a clock frequency of 160kHz (6μs period) half of the first reference integrate period is lost in delay. This means that the meter reading will change from 0 to 1 with a 50μV input, 1 to 2 with 150μV, 2 to 3 at 250μV, etc. This transition at mid-point is considered desirable by most users. However, if the clock frequency is increased appreciably above this, the instrument will flash "1" on noise peaks even when the input is shorted.

For many dedicated applications where the input signal is always one polarity, the delay of the comparator need not be a limitation. Since the non-linearity and noise do not increase substantially with frequency, up to 500kHz clock rate may be used. For a fixed clock frequency, the extra count or counts caused by comparator delay will be a constant and can be subtracted out digitally.

The minimum clock frequency is established by leakage on the auto-zero and reference cap. With most devices, measurement cycles as long as 10 seconds give no measurable leakage error.

AUXILIARY INPUTS/OUTPUTS

The 7103 and 7103B include several pins that allow them to operate conveniently in more sophisticated systems. These include:

1. 4-1/2/3-1/2 (Pin 2). When high (or open) the internal counter operates as a full 4-1/2 decade counter with a complete measurement cycle requiring 40,000 counts. When hold low, the least significant decade is cleared and the clock is fed directly into the next decade. A measurement cycle now required only 4000 clock pulses. All 5 digit drivers are active in either case with each digit lasting 200 counts with pin 2 high (4-1/2 digit) and 20 counts for pin 2 low (3-1/2 digit). The only difference between 7103B and 7103 is that they were tested with this pin high and low respectively. Actually, most 7103 will operate satisfactorily in a 4-1/2 digit application. They simply have not received the more complex testing required to prove it.

2. Run/Hold (Pin 4). When high (or open) the A/D will free-run with equally spaced measurement cycles every 40,000/4,000 clock pulses. If taken low, the converter will continue the full measurement cycle that it is in and then hold this reading as long as pin 4 is held low. A short positive pulse (greater than 300ns) will now initiate a new measurement cycle beginning with 10,000/1,000 counts of auto zero. Of course if the pulse occurs before the full measurement cycle (40,000/4,000 counts) is completed, it will not be recognized and the converter will simply complete the measurement it is in. An external indication that a full measurement cycle has been completed is that the first strobe pulse (see below) will occur 100/10 counts after the end of this cycle. Thus, if Run/Hold is low and has been low for at least 100/10 counts, the converter is holding and ready to start a new measurement when pulsed high.

3. $\overline{\text{Strobe}}$ (Pin 18). This is a negative going output pulse that aids in transferring the BCD data to external latches, UARTs or microprocessors. There are 5 negative going $\overline{\text{Strobe}}$ pulses that occur in the center of each of the digit drive pulses and occur once and only once for each measurement cycle starting 100/10 pulses after the end of the full measurement cycle. Digit 5 (MSD) goes high at the end of the measurement cycle and stays on for 200/20 counts. In the center of this digit pulse (to avoid race conditions between changing BCD and digit drives) the first $\overline{\text{Strobe}}$ pulse goes negative for 1/2 clock pulse width. Similarly, after 200/20 clock pulses, digit 4 goes high and 100/10 pulses later the $\overline{\text{Strobe}}$ goes negative for the second time. This continues through digit 1 (LSD) when the fifth and last $\overline{\text{Strobe}}$ pulse is sent. The digit drive will continue to scan (unless the previous signal was over-range) but no additional $\overline{\text{Strobe}}$ pulses will be sent until a new measurement is available.

4. Busy (Pin 28). Busy goes high at the beginning of signal integrate and stays high until the first clock pulse after zero-crossing (or after end of measurement in the case of an over-range). The internal latches are enabled (i.e., transferred during the first clock pulse after busy and are latched at the end of this clock pulse. The circuit automatically reverts to auto-zero when not BUSY so it may also be considered a $\overline{\text{A-Z}}$ signal. A very simple means for transmitting the data down a single wire pair from a remote location would be to AND BUSY with clock and subtract 10,001/1,001 counts from the number of pulses received (as mentioned previously there is one NO count pulse in each reference integrate (cycle).

Figure 4. Timing Diagram

5. Over-range (Pin 14). This pin goes positive when the input signal exceeds the range (20,000/2,000) of the converter. The output F-F is set at the end of Busy and is reset to zero at the beginning of Reference integrate in the next measurement cycle.

6. Under-range (Pin 13). This pin goes positive when the reading is 9% of range or less. The output F-F is set at the end of busy (if the new reading is 1800/180 or less) and is reset at the beginning of signal integrate of the next reading.

7. Polarity (Pin 3). This pin is positive for a positive input signal. It is valid even for a zero reading. In other words, +0000 means the signal is positive but less than the least significant bit. The converter can be used as a null detector by forcing equal (+) and (−) readings. The null at this point should be less than 0.1 LSB. This output becomes valid at the beginning of reference integrate and remains correct until it is re-validated for the next measurement.

8. Digit Drives (Pins 19, 24, 25, 26 and 27). The digit drives are a positive going signal that each last for 200/20 clock pulses. The scan sequence is D_5 (MSD), D_4, D_3, D_2 and D_1 (LSD). All five digits are scanned even when operating in the 3-1/2 digit mode. The scan is continuous unless an over-range occurs. Then all digit drives are blanked from the end of the strobe sequence until the beginning of Reference Integrate when D_5 will start the scan again. This gives a blinking display as a visual indication of over-range

9. BCD (Pins 20, 21, 22 and 23). The Binary coded Decimal bits B_8, B_4, B_2 and B_1 are positive logic signals that go on simultaneously with the digit driver.

INTERFACING WITH UARTS AND MICROPROCESSORS

Figure 5 shows a very simple interface between a free-running 8068A/7103B and a UART. The five $\overline{\text{Strobe}}$ pulses start the transmission of the five data words. The digit 5 word is 0000XXXX, digit 4 is 1000XXXX, digit 3 is 0100XXXX, etc. Also the polarity is transmitted indirectly by using it to drive the Even Parity Enable Pin (EPE). If EPE of the receiver is held low, the parity flag at the receiver can be decoded as a positive signal, no flag as negative. Circuits for the 7103 to interface directly with three popular microprocessors are shown in Figures 7, 8 and 9. The main differences in the circuits are that IM6100 with its 12 bit word capability can accept polarity, over-range and under-range multiplexed onto the Digit 5 - as in the UART circuits. In each case the microprocessor can instruct the A/D when to begin a measurement and when to hold this measurement.

Figure 5. Simple 7103/7103B to UART Interface

Figure 6. Complex 7103/7103B to UART Interface

Figure 7. IM6100 to 7103/7103B Interface

Figure 8. Mc6800 to 7103/7103B Interface

Figure 9. Intel 8080 to 7103/7103B Interface

PACKAGE DIMENSIONS

14 Pin CERDIP Dual-In-Line Package

14 Pin Ceramic Dual-In-Line Package

28 Pin Plastic Dual-In-Line Package

28 Pin Ceramic Dual-In-Line Package

INTERSIL

ICL7106/ICL7107
3½ Digit Single Chip A/D Converter

FEATURES

- **Guaranteed zero reading for 0 volts input on all scales.**
- **True polarity at zero for precise null detection.**
- **1 pA input current typical.**
- **True differential input and reference.**
- **Direct display drive - no external components required. — LCD ICL7106**
  — LED ICL7107
- **Low noise - less than 15μV pk-pk.**
- **On-chip clock and reference.**
- **Low power dissipation - typically less than 10mW.**
- **No additional active circuits required.**
- **Evaluation Kit available.**

GENERAL DESCRIPTION

The Intersil ICL7106 and 7107 are high performance, low power 3-1/2 digit A/D converters. All the necessary active devices are contained on a single CMOS I.C., including seven segment decoders, display drivers, reference, and a clock. The 7106 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7107 will directly drive an instrument-size light emitting diode (LED) display.

The 7106 and 7107 bring together an unprecedented combination of high accuracy, versatility, and true economy. High accuracy like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10 pA max., and roll-over error of less than one count. The versatility of true differential input and reference is useful in all systems, but gives the designer an uncommon advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation (7106), enabling a high performance panel meter to be built with the addition of only 7 passive components and a display.

ICL7106 with Liquid Crystal Display

ICL7107 with LED Display

ORDERING INFORMATION

Part	Package	Temp. Range	Order Part #
7106	40 pin ceramic DIP	0°C to +70°C	ICL7106CDL
7106	40 pin plastic DIP	0°C to +70°C	ICL7106CPL
7107	40 pin ceramic DIP	0°C to +70°C	ICL7107CDL
7107	40 pin plastic DIP	0°C to +70°C	ICL7107CPL
7106 Kit 7107 Kit	Evaluation kits contain IC, display, circuit board, passive components and hardware. See page 10.		ICL7106EV/Kit ICL7107EV/Kit

PIN CONFIGURATION

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ABSOLUTE MAXIMUM RATINGS

ICL 7106

Supply Voltage (V+ to V−) 15V
Analog Input Voltage (either input) (Note 1) ..... V+ to V−
Reference Input Voltage (either input) ..... V+ to V−
Clock Input ..... Test to V+
Power Dissipation (Note 2)
Ceramic Package ..... 1000 mW
Plastic Package ..... 800 mW
Operating Temperature ..... 0° C to +70° C
Storage Temperature ..... −65° C to +160° C
Lead Temperature (Soldering, 60 sec) ..... 300° C

ICL 7107

Supply Voltage V+ ..... +6V
V− ..... −9V
Analog Input Voltage (either input) (Note 1) ..... V+ to V−
Reference Input Voltage (either input) ..... V+ to V−
Clock Input ..... Gnd to V+
Power Dissipation (Note 1)
Ceramic Package ..... 1000 mW
Plastic Package ..... 800 mW
Operating Temperature ..... 0° C to +70° C
Storage Temperature ..... −65° C to +160° C
Lead Temperature (Soldering, 60 sec) ..... 300° C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	Vin = 0.0V Full Scale = 200.0 mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	Vin = Vref Vref = 100 mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	−Vin = +Vin ≈ 200.0mV	−1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	-1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	Vcm = ±1V, Vin = 0V. Full Scale = 200.0mV.		50		μV/V
Noise (Pk - Pk value not exceeded 95% of time)	Vin = 0V Full Scale = 200.0mV		15		μV
Leakage Current @ Input	Vin = 0V		1	10	pA
Zero Reading Drift	Vin = 0 0° < T_A < 70° C		0.2	1	μV/° C
Scale Factor Temperature Coefficient	Vin = 199.0mV 0 < T_A < 70° C (Ext.Ref.0ppm/° C)		1	5	ppm/° C
Supply Current (Does not include LED current for 7107)	Vin = 0		0.8	1.8	mA
Analog Common Voltage (With respect to pos. supply)	25KΩ between Common & pos. Supply	2.4	2.8	3.2	Volts
Temp. Coeff. of Analog Common (with respect to pos. Supply)	25KΩ between Common & pos. Supply		80		ppm/° C
7106 ONLY Pk-Pk Segment Drive Voltage (Note 5)	V Supply = 9V	4	5	6	Volts
7106 ONLY Pk-Pk Backplane Drive Voltage (Note 5)	V Supply = 9V	4	5	6	Volts
7107 ONLY Segment Sinking Current (Except Pin 19)	+Supply = 5.0V Segment voltage = 3V	5	8.0		mA
7107 ONLY Segment Sinking Current (Pin 19 only)	+Supply = 5.0V Segment voltage = 3V	10	16		mA

Note 3: Unless otherwise noted, specifications apply to both the 7106 and 7107 at T_A = 25° C, f_{clock} = 48kHz. 7106 is tested in the circuit of Figure 1. 7107 is tested in the circuit of Figure 2.

Note 4: Refer to "Differential Input" discussion on page 4.

Note 5: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

TEST CIRCUITS

Figure 1: 7106

Figure 2: 7107

DETAILED DESCRIPTION

ANALOG SECTION

Figure 3 shows the Block Diagram of the Analog Section for the ICL 7106 and 7107. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) deintegrate (DE).

Figure 3: Analog Section of 7106/7107

1. Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog common. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10μV.

2. Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between input high and input low for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, input low can be tied to analog common to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is 1000 $(\frac{V_{in}}{V_{ref}})$.

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Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Differential Reference

The reference voltage can be generated anywhere within the power supply voltage of the converter. The main source of common mode error is a roll-over voltage caused by the reference capacitor losing or gaining charge to stray capacity on its nodes. If there is a large common mode voltage, the reference capacitor can gain charge (increase voltage) when called up to de-integrate a positive signal but lose charge (decrease voltage) when called up to deintegrate a negative input signal. This difference in reference for (+) or (−) input voltage will give a roll-over error. However, by selecting the reference capacitor large enough in comparison to the stray capacitance, this error can be held to less than 0.5 count for the worse case condition. (See Component Values Selection below).

Analog Common

This pin is included primarily to set the common mode voltage for battery operation (7106) or for any system where the input signals are floating with respect to the power supply. The common pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog common has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low voltage coefficient (.001%/%), low output impedance (≈15Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. With the 7107, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25 μV to 80 μVpk-pk. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a non-overload count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7106, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Fig. 4.

Figure 4: Using an External Reference

Analog common is also the voltage the input returns to during auto-zero and de-integrate. If signal low is different from analog common, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications input low will be set at a fixed known voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common mode voltage from the converter. The same holds true for the reference voltage. If reference can be conveniently referenced to analog common, it should be since this removes the common mode voltage from the reference system.

Within the IC, analog common is tied to an N channel FET that can sink 30mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so common may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The test pin serves two functions. On the 7106 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application.

Figure 5: Simple Inverter for Fixed Decimal Point

Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

The second function is a "lamp test". When Test is pulled high (to + supply) all segments will be turned on and the display should read - 1888. Caution: on the 7106, in the lamp test mode, the segments have a constant d-c voltage (no square-wave) and will burn the LCD display if left in this mode for several minutes.

DIGITAL SECTION

Figures 7 and 8 show the digital section for the 7106 and 7107, respectively. In the 7106, an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases neglible d-c voltage exists across the segments.

Figure 8 is the Digital Section of the 7107. It is identical except the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8 mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16 mA.

Figure 7: Digital Section 7106

Figure 8: Digital Section 7107

System Timing

Figure 9 shows the clocking arrangement used in the 7106 and 7107. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

Figure 9: Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33⅓ kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 66⅔ kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

COMPONENT VALUE SELECTION

1. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 470KΩ is near optimum and similarly a 47KΩ for a 200.0 mV scale.

2. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the 7106 or the 7107, when the analog common is used as a reference, a nominal ±2 volt full scale integrator swing is fine. For the 7107 with ±5 volt supplies and analog common tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48kHz clock), nominal values for C_{int} are .22 and .10μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

3. Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full scale where noise

is very important, a 0.47μF capacitor is recommended. On the 2 volt scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

4. Reference Capacitor

A 0.1μF capacitor gives good results in most applications. However, where a large common mode voltage exists (i.e. the reference low is not at analog common) and a 200 mV scale is used, a larger value is required to prevent roll-over error. Generally 1.0 μF will hold the roll-over error to 0.5 count in this instance.

5. Oscillator Components

For all ranges of frequency a 100KΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{.45}{RC}$. For 48kHz clock (3 readings/second), C = 100pF.

6. Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: Vin = 2Vref. Thus, for the 200.0mV and 2.000 volt scale, Vref should equal 100.0 mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select Vref = .341V. Suitable values for integrating resistor and capacitor would be 120KΩ and .22 μF. This makes the system slightly quieter and also avoids a divider network on the input. The 7107 with ±5 volts supplies can accept input signals up to ±4 volts. Another advantage of this system occurs when a digital reading of zero is desired for Vin ≠ 0. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between analog high and common and the variable (or fixed) offset voltage between common and analog low.

7. 7107 Power Supplies

The 7107 is designed to work from ±5 volt supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 10 shows this application.

Figure 10: Generating Negative Supply from +5v

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts.
3. An external reference is used.

TYPICAL APPLICATIONS

The 7106 and 7107 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

Figure 11: 7106 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second, floating supply voltage (9V battery).

Figure 12: 7107 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog Common on page 4).

TYPICAL APPLICATIONS (Contd.)

Figure 13: 7107 with an external band-gap reference (1.2V type). IN LO is tied to COMMON, thus establishing the correct common mode voltage. If COMMON is not shorted to GND, the input voltage may float with respect to the power supply and COMMON acts as a pre-regulator for the reference. If COMMON is shorted to GND, the input is single ended (referred to supply ground) and the pre-regulator is over-ridden.

Figure 14: 7107 with Zener diode reference. Since low T.C. zeners have breakdown voltages ~ 6.8V, diode must be placed across the total supply (10V). As in the case of Figure 12, IN LO may be tied to either COMMON or GND.

Figure 15: 7106/7107: Recommended component values for 2.000V full scale.

Figure 16: 7107 operated from single +5V supply. An external reference must be used in this application, since the voltage between V+ and V− is insufficient for correct operation of the internal reference.

Figure 17: 7107 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

Figure 18: 7106 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

TYPICAL APPLICATIONS (Contd.)

Figure 19: Circuit for developing Underrange and Overrange signals from 7106 outputs.

Figure 20: Circuit for developing Underrange and Overrange signals from 7107 outputs. The LM339 is required to ensure logic compatibility with heavy display loading.

Figure 21: AC to DC Converter with 7106. Test is used as a common mode reference level to ensure compatibility with most op-amps.

Figure 22: Display Buffering for increased drive current. Requires four DM7407 Hex Buffers. Each buffers is capable of sinking 40 mA max.

7106/7107 EVALUATION KITS

After purchasing a sample of the 7106 or the 7107, the majority of users will want to build a simple voltmeter. The parts can then be evaluated against the data sheet specifications, and tried out in the intended application. However, locating and purchasing even the small number of additional components required, then wiring a breadboard, can often cause delays of days or sometimes weeks. To avoid this problem and facilitate evaluation of these unique circuits, Intersil is offering a kit which contains all the necessary components to build a 3½ digit panel meter. With the help of this kit, an engineer or technician can have the system "up and running" in about half an hour.

Two kits are offered, the ICL7106EV/KIT and the ICL7107EV/KIT. Both contain the appropriate IC, a circuit board, a display (LCD for 7106EV/KIT, LEDs for 7107EV/KIT), passive components, and miscellaneous hardware.

APPLICATION NOTES

A016 "Selecting A/D Converters," by David Fullagar
A017 "The Integrating A/D Converter," by Lee Evans
A018 "Do's and Dont's of Applying A/D Converters," by Peter Bradshaw and Skip Osgood
A019 "4½ Digit Panel Meter Demonstrator/Instrumentation Boards," by Michael Dufort.
A023 "Low Cost Digital Panel Meter Designs," by David Fullagar & Michael Dufort.

PACKAGE DIMENSIONS TYPICAL CONNECTION DIAGRAMS

40 Pin Plastic Dual-in-Line Package

40 Pin Ceramic Dual-in-Line Package

INTERSIL

ICL7116/ICL7117 3½ Digit Single Chip A/D Converter with Display Hold

FEATURES

- **HOLD Reading Input allows indefinite display hold**
- **Guaranteed zero reading for 0 volts input on all scales.**
- **True polarity at zero for precise null detection.**
- **1 pA input current typical.**
- **True differential input and reference.**
- **Direct display drive - no external components required. — LCD ICL7116**
  — LED ICL7117
- **Low noise - less than 15 μV pk-pk typical.**
- **On-chip clock and reference.**
- **Low power dissipation - typically less than 10mW.**
- **No additional active circuits required.**

GENERAL DESCRIPTION

The Intersil ICL7116 and 7117 are high performance, low power 3-1/2 digit A/D converters. All the necessary active devices are contained on a single CMOS I.C., including seven segment decoders, display drivers, reference, and a clock. The 7116 is designed to interface with a liquid crystal display (LCD) and includes a backplane drive; the 7117 will directly drive an instrument-size light emitting diode (LED) display.

The 7116 and 7117 have almost all of the features of the 7106 and 7107 with the addition of a HOLD Reading input. With this input, it is possible to make a measurement and then retain the value on the display indefinitely. To make room for this feature the reference input has been referenced to Common rather than being fully differential. These circuits retain the accuracy, versatility, and true economy of the 7106 and 7107. High accuracy like auto-zero to less than 10μV, zero drift of less than 1μV/°C, input bias current of 10pA maximum, and roll over error of less than one count. The versatility of true differential input is of particular advantage when measuring load cells, strain gauges and other bridge-type transducers. And finally the true economy of single power supply operation (7116), enabling a high performance panel meter to be built with the addition of only seven passive components and a display.

TYPICAL CONNECTION DIAGRAMS

ICL7116 with Liquid Crystal Display

ICL7117 with LED Display

ORDERING INFORMATION

Part	Package	Temp. Range	Order Part #
7116	40 pin ceramic DIP	0°C to +70°C	ICL7116CDL
7116	40 pin plastic DIP	0°C to +70°C	ICL7116CPL
7117	40 pin ceramic DIP	0°C to +70°C	ICL7117CDL
7117	40 pin plastic DIP	0°C to +70°C	ICL7117CPL

PIN CONFIGURATION

4

ABSOLUTE MAXIMUM RATINGS

ICL7116

Supply Voltage (V^+ to V^-) 15V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Test to V^+
Power Dissipation (Note 2)
Ceramic Package ..... 1000 mW
Plastic Package ..... 800 mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

ICL7117

Supply Voltage V^+ ..... +6V
V^- ..... −9V
Analog Input Voltage (either input) (Note 1) ..... V^+ to V^-
Reference Input Voltage (either input) ..... V^+ to V^-
Clock Input ..... Gnd to V^+
Power Dissipation (Note 1)
Ceramic Package ..... 1000 mW
Plastic Package ..... 800 mW
Operating Temperature ..... 0°C to +70°C
Storage Temperature ..... −65°C to +160°C
Lead Temperature (Soldering, 60 sec) ..... 300°C

Note 1: Input voltages may exceed the supply voltages provided the input current is limited to ±100μA.

Note 2: Dissipation rating assumes device is mounted with all leads soldered to printed circuit board.

ELECTRICAL CHARACTERISTICS (Note 3)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Zero Input Reading	Vin = 0.0V Full Scale = 200.0mV	−000.0	±000.0	+000.0	Digital Reading
Ratiometric Reading	Vin = Vref Vref = 100mV	999	999/1000	1000	Digital Reading
Rollover Error (Difference in reading for equal positive and negative reading near Full Scale)	−Vin = +Vin = 200.0mV	−1	±.2	+1	Counts
Linearity (Max. deviation from best straight line fit)	Full scale = 200mV or full scale = 2.000V	−1	±.2	+1	Counts
Common Mode Rejection Ratio (Note 4)	Vcm = ±1V, Vin = 0V. Full Scale = 200.0mV		50		μV/V
Noise (Pk - Pk value not exceeded 95% of time)	Vin = 0V Full Scale = 200.0mV		15		μV
Leakage Current @ Input	Vin = 0V		1	10	pA
Zero Reading Drift	Vin = 0 0° < T_A < 70°C		0.2	1	μV/°C
Scale Factor Temperature Coefficient	Vin = 199.0mV 0 < T_A < 70°C (Ext. Ref. 0 ppm/°C)		1	5	ppm/°C
Supply Current (Does not include LED current for 7117)	Vin = 0		0.8	1.8	mA
Analog Common Voltage (With respect to pos. supply)	25kΩ between Common & pos. Supply	2.4	2.8	3.2	Volts
Temp. Coeff. of Analog Common (with respect to pos. Supply)	25kΩ between Common & pos. Supply		80		ppm/°C
Input Resistance, Pin 1 (Note 6)		30	70		kΩ
V_{IL}, Pin 1 (7116 only)				Test +1.5	Volts
V_{IL}, Pin 1 (7117 only)				GND +1.5	Volts
V_{IH}, Pin 1 (Both)		V^+ −1.5			Volts
7116 ONLY Pk-Pk Segment Drive Voltage (Note 5)	V Supply = 9V	4	5	6	Volts
7116 ONLY Pk-Pk Backplane Drive Voltage (Note 5)	V Supply = 9V	4	5	6	Volts
7117 ONLY Segment Sinking Current (Except Pin 19)	+Supply = 5.0V Segment voltage = 3V	5	8.0		mA
7117 ONLY Segment Sinking Current (Pin 19 only)	+Supply = 5.0V Segment voltage = 3V	10	16		mA

Note 3: Unless otherwise noted, specifications apply to both the 7116 and 7117 at T_A = 25°C, f_{clock} = 48kHz. 7116 is tested in the circuit of Figure 1. 7117 is tested in the circuit of Figure 2.

Note 4: Refer to "Differential Input" discussion on page 4.

Note 5: Back plane drive is in phase with segment drive for 'off' segment, 180° out of phase for 'on' segment. Frequency is 20 times conversion rate. Average DC component is less than 50mV.

Note 6: The 7116 logic input has an internal pull-down resistor connected from HLDR, pin 1, to TEST, pin 37. The 7117 logic input has an internal pull-down resistor connected from HLDR, pin 1 to GROUND, pin 21.

TEST CIRCUITS

Figure 1: 7116

Figure 2: 7117

DETAILED DESCRIPTION

ANALOG SECTION

Figure 3 shows the Block Diagram of the Analog Section for the ICL7116 and 7117. Each measurement cycle is divided into three phases. They are (1) auto-zero (A-Z), (2) signal integrate (INT) and (3) deintegrate (DE).

Figure 3: Analog Section of 7116/7117

1. Auto-zero phase

During auto-zero three things happen. First, input high and low are disconnected from the pins and internally shorted to analog common. Second, the reference capacitor is charged to the reference voltage. Third, a feedback loop is closed around the system to charge the auto-zero capacitor C_{AZ} to compensate for offset voltages in the buffer amplifier, integrator, and comparator. Since the comparator is included in the loop, the A-Z accuracy is limited only by the noise of the system. In any case, the offset referred to the input is less than 10µV.

2. Signal Integrate phase

During signal integrate, the auto-zero loop is opened, the internal short is removed, and the internal input high and low are connected to the external pins. The converter then integrates the differential voltage between input high and input low for a fixed time. This differential voltage can be within a wide common mode range; within one volt of either supply. If, on the other hand, the input signal has no return with respect to the converter power supply, input low can be tied to analog common to establish the correct common-mode voltage. At the end of this phase, the polarity of the integrated signal is determined.

3. De-integrate phase

The final phase is de-integrate, or reference integrate. Input low is internally connected to analog common and input high is connected across the previously charged reference capacitor. Circuitry within the chip ensures that the capacitor will be connected with the correct polarity to cause the integrator output to return to zero. The time required for the output to return to zero is proportional to the input signal. Specifically the digital reading displayed is 1000 $(\frac{V_{in}}{V_{ref}})$.

4

Differential Input

The input can accept differential voltages anywhere within the common mode range of the input amplifier; or specifically from 0.5 volts below the positive supply to 1.0 volt above the negative supply. In this range the system has a CMRR of 86 dB typical. However, since the integrator also swings with the common mode voltage, care must be exercised to assure the integrator output does not saturate. A worse case condition would be a large positive common-mode voltage with a near full-scale negative differential input voltage. The negative input signal drives the integrator positive when most of its swing has been used up by the positive common mode voltage. For these critical applications the integrator swing can be reduced to less than the recommended 2V full scale swing with little loss of accuracy. The integrator output can swing within 0.3 volts of either supply without loss of linearity.

Reference

The reference input must be generated as a positive voltage with respect to Common.

Analog Common

This pin is included primarily to set the common mode voltage for battery operation (7116) or for any system where the input signals are floating with respect to the power supply. The common pin sets a voltage that is approximately 2.8 volts more negative than the positive supply. This is selected to give a minimum end-of-life battery voltage of about 6V. However, the analog common has some of the attributes of a reference voltage. When the total supply voltage is large enough to cause the zener to regulate (>7V), the common voltage will have a low voltage coefficient (.001%/%), low output impedance (≈15Ω), and a temperature coefficient typically less than 80ppm/°C.

The limitations of the on-chip reference should also be recognized, however. With the 7117, the internal heating which results from the LED drivers can cause some degradation in performance. Due to their higher thermal resistance, plastic parts are poorer in this respect than ceramic. The combination of reference Temperature Coefficient (TC), internal chip dissipation, and package thermal resistance can increase noise near full scale from 25 μV to 80 μVpk-pk. Also the linearity in going from a high dissipation count such as 1000 (20 segments on) to a low dissipation count such as 1111 (8 segments on) can suffer by a count or more. Devices with a positive TC reference may require several counts to pull out of an overload condition. This is because overload is a low dissipation mode, with the three least significant digits blanked. Similarly, units with a negative TC may cycle between overload and a non-overload count as the die alternately heats and cools. All these problems are of course eliminated if an external reference is used.

The 7116, with its negligible dissipation, suffers from none of these problems. In either case, an external reference can easily be added, as shown in Fig. 4.

Analog common is also the voltage the input returns to during auto-zero and de-integrate. If signal low is different from analog common, a common mode voltage exists in the system and is taken care of by the excellent CMRR of the converter. However, in some applications input low will be set at a fixed known voltage (power supply common for instance). In this application, analog common should be tied to the same point, thus removing the common mode voltage from the converter.

Figure 4: Using an External Reference

Within the IC, analog common is tied to an N channel FET that can sink 30mA or more of current to hold the voltage 2.8 volts below the positive supply (when a load is trying to pull the common line positive). However, there is only 10μA of source current, so common may easily be tied to a more negative voltage thus over-riding the internal reference.

Test

The test pin serves two functions. On the 7116 it is coupled to the internally generated digital supply through a 500Ω resistor. Thus it can be used as the negative supply for externally generated segment drivers such as decimal points or any other presentation the user may want to include on the LCD display. Figures 5 and 6 show such an application.

Figure 5: Simple Inverter for Fixed Decimal Point

Figure 6: Exclusive 'OR' Gate for Decimal Point Drive

The second function is a "lamp test". When Test is pulled high (to + supply) all segments will be turned on and the display should read - 1888. Caution: on the 7116, in the lamp test mode, the segments have a constant d-c voltage (no square-wave) and will burn the LCD display if left in this mode for several minutes.

DIGITAL SECTION

Figures 7 and 8 show the digital section for the 7116 and 7117, respectively. In the 7116, an internal digital ground is generated from a 6 volt Zener diode and a large P channel source follower. This supply is made stiff to absorb the relative large capacitive currents when the back plane (BP) voltage is switched. The BP frequency is the clock frequency divided by 800. For three readings/second this is a 60 Hz square wave with a nominal amplitude of 5 volts. The segments are driven at the same frequency and amplitude and are in phase with BP when OFF, but out of phase when ON. In all cases neglible d-c voltage exists across the segments.

Figure 8 is the Digital Section of the 7117. It is identical except the regulated supply and back plane drive have been eliminated and the segment drive has been increased from 2 to 8 mA, typical for instrument size common anode LED displays. Since the 1000 output (pin 19) must sink current from two LED segments, it has twice the drive capability or 16 mA.

HOLD Reading Input

The HLDR input will prevent the latch from being updated when this input is at a logic "HI". The chip will continue to make A/D conversions, however, the results will not be updated to the internal latches until this input goes low. This input can be left open or connected to TEST (7116) or GROUND (7117) to continuously update the display. This input has been implemented as a CMOS compatible input with a 70K typical resistance to either TEST (7116) or GROUND (7117).

Figure 7: Digital Section 7116

Figure 8: Digital Section 7117

System Timing

Figure 9 shows the clocking arrangement used in the 7116 and 7117. Three basic clocking arrangements can be used:

1. An external oscillator connected to pin 40.
2. A crystal between pins 39 and 40.
3. An R-C oscillator using all three pins.

Figure 9: Clock Circuits

The oscillator frequency is divided by four before it clocks the decade counters. It is then further divided to form the three convert-cycle phases. These are signal integrate (1000 counts), reference de-integrate (0 to 2000 counts) and auto-zero (1000 to 3000 counts). For signals less than full scale, auto-zero gets the unused portion of reference deintegrate. This makes a complete measure cycle of 4,000 (16,000 clock pulses) independent of input voltage. For three readings/second, an oscillator frequency of 48kHz would be used.

To achieve maximum rejection of 60 Hz pickup, the signal integrate cycle should be a multiple of 60 Hz. Oscillator frequencies of 240kHz, 120kHz, 80kHz, 60kHz, 48kHz, 40kHz, 33 1/3 kHz, etc. should be selected. For 50Hz rejection, Oscillator frequencies of 200kHz, 100kHz, 66 2/3 kHz, 50kHz, 40kHz, etc. would be suitable. Note that 40kHz (2.5 readings/second) will reject both 50 and 60 Hz (also 400 and 440 Hz).

COMPONENT VALUE SELECTION

1. Integrating Resistor

Both the buffer amplifier and the integrator have a class A output stage with 100μA of quiescent current. They can supply 20μA of drive current with negligible non-linearity. The integrating resistor should be large enough to remain in this very linear region over the input voltage range, but small enough that undue leakage requirements are not placed on the PC board. For 2 volt full scale, 470kΩ is near optimum and similarly a 47kΩ for a 200.0 mV scale.

2. Integrating Capacitor

The integrating capacitor should be selected to give the maximum voltage swing that ensures tolerance build-up will not saturate the integrator swing (approx. 0.3 volt from either supply). In the 7116 or the 7117, when the analog common is used as a reference, a nominal ±2 volt full scale integrator swing is fine. For the 7117 with ±5 volt supplies and analog common tied to supply ground, a ±3.5 to ±4 volt swing is nominal. For three readings/second (48kHz clock), nominal values for C_{int} are .22 and .10μF, respectively. Of course, if different oscillator frequencies are used, these values should be changed in inverse proportion to maintain the same output swing.

An additional requirement of the integrating capacitor is it have low dielectric absorption to prevent roll-over errors. While other types of capacitors are adequate for this application, polypropylene capacitors give undetectable errors at reasonable cost.

3. Auto-Zero Capacitor

The size of the auto-zero capacitor has some influence on the noise of the system. For 200 mV full scale where noise

is very important, a 0.47μF capacitor is recommended. On the 2 volt scale, a 0.047μF capacitor increases the speed of recovery from overload and is adequate for noise on this scale.

4. Reference Capacitor

A 0.1μF capacitor gives good results in most applications. If rollover errors occur a larger value, up to 1.0μF may be required.

5. Oscillator Components

For all ranges of frequency a 100kΩ resistor is recommended and the capacitor is selected from the equation $f = \frac{.45}{RC}$. For 48kHz clock (3 readings/second), C = 100pF.

6. Reference Voltage

The analog input required to generate full-scale output (2000 counts) is: Vin = 2Vref. Thus, for the 200.0 mV and 2.000 volt scale, Vref should equal 100.0 mV and 1.000 volt, respectively. However, in many applications where the A/D is connected to a transducer, there will exist a scale factor other than unity between the input voltage and the digital reading. For instance, in a weighing system, the designer might like to have a full scale reading when the voltage from the transducer is 0.682V. Instead of dividing the input down to 200.0 mV, the designer should use the input voltage directly and select Vref = .341V. Suitable values for integrating resistor and capacitor would be 120kΩ and .22μF. This makes the system slightly quieter and also avoids a divider network on the input. The 7117 with ±5 volts supplies can accept input signals up to ±4 volts. Another advantage of this system occurs when a digital reading of zero is desired for Vin ≠ 0. Temperature and weighing systems with a variable tare are examples. This offset reading can be conveniently generated by connecting the voltage transducer between analog high and common and the variable (or fixed) offset voltage between common and analog low.

7. 7117 Power Supplies

The 7117 is designed to work from ±5 volt supplies. However, if a negative supply is not available, it can be generated from the clock output with 2 diodes, 2 capacitors, and an inexpensive I.C. Figure 10 shows this application.

Figure 10: Generating Negative Supply from +5v

In fact, in selected applications no negative supply is required. The conditions to use a single +5V supply are:

1. The input signal can be referenced to the center of the common mode range of the converter.
2. The signal is less than ±1.5 volts.
3. An external reference is used.

TYPICAL APPLICATIONS

The 7116 and 7117 may be used in a wide variety of configurations. The circuits which follow show some of the possibilities, and serve to illustrate the exceptional versatility of these A/D converters.

Figure 11: 7116 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second, floating supply voltage (9V battery).

Figure 12: 7117 using the internal reference. Values shown are for 200.0 mV full scale, 3 readings per second. IN LO may be tied to either COMMON for inputs floating with respect to supplies, or GND for single ended inputs. (See discussion under Analog Common on page 4).

Figure 13: 7116/7117: Recommended component values for 2.000V full scale.

Figure 14: 7117 operated from single +5V supply. An external reference must be used in this application, since the voltage between V+ and V− is insufficient for correct operation of the internal reference.

Figure 15: 7117 measuring ratiometric values of Quad Load Cell. The resistor values within the bridge are determined by the desired sensitivity.

Figure 16: 7116 used as a digital centigrade thermometer. A silicon diode-connected transistor has a temperature coefficient of about −2mV/°C. Calibration is achieved by placing the sensing transistor in ice water and adjusting the zeroing potentiometer for a 000.0 reading. The sensor should then be placed in boiling water and the scale-factor potentiometer adjusted for 100.0 reading.

PACKAGE DIMENSIONS

40 Pin Plastic Dual-in-Line Package

40 Pin Ceramic Dual-in-Line Package

INTERSIL

AM2502, AM2503, AM2504
Eight-Bit/Twelve-Bit Successive Approximation Registers

FEATURES

- Contains all the storage and control for successive approximation A-to-D converters.
- Provision for register extension or truncation.
- Can be operated in START-STOP or continuous conversion mode.
- 100% reliability assurance testing in compliance with MIL-STD-883.
- Can be used as serial-to-parallel counter or ring counters.
- Electrically tested and optically inspected dice for the assemblers of hybrid products.

GENERAL DESCRIPTION

The AM2502, 2503 and 2504 are 8-bit and 12-bit TTL Successive Approximation Registers. The registers contain all the digital control and storage necessary for successive approximation analog-to-digital conversion. They can also be used in digital systems as the control and storage element in recursive digital routines.

The registers consist of a set of master latches that act as the control elements in the device and change state when the input clock is LOW, and a set of slave latches that hold the register data and change on the input clock LOW-to-HIGH transition. Externally the device acts as a special purpose serial-to-parallel converter that accepts data at the D input of the register and sends the data to the appropriate slave latch to appear at the register output and the DO output on the 2502 and 2504 when the clock goes from LOW-to-HIGH. There are no restrictions on the data input; it can change state at any time except during the set-up time just prior to the clock transition. At the same time that data enters the register bit the next less significant bit is set to a LOW ready for the next iteration.

The register is reset by holding the $\overline{S}$ (Start) signal LOW during the clock LOW-to-HIGH transition. The register synchronously resets to the state $Q_7(11)$ LOW, (Note 2) and all the remaining register outputs HIGH. The $\overline{CC}$ (Conversion Complete) signal is also set HIGH at this time. The $\overline{S}$ signal should not be brought back HIGH until after the clock LOW-to-HIGH transition in order to guarantee correct resetting. After the clock has gone HIGH resetting the register, the $\overline{S}$ signal is removed. On the next clock LOW-to-HIGH transition the data on the D input is set into the $Q_7(11)$ register bit and the $Q_6(10)$ register bit is set to a LOW ready for the next clock cycle. On the next clock LOW-to-HIGH transition data enters the $Q_6(10)$ register bit and $Q_5(9)$ is set to a LOW. This operation is repeated for each register bit in turn until the register has been filled. When the data goes into Q_0, the $\overline{CC}$ signal goes LOW, and the register is inhibited from further change until reset by a Start signal.

In order to allow complementary conversion the complementary output of the most significant register bit is made available. An active LOW enable input, $\overline{E}$, on the 2503 and 2504 allows devices to be connected together to form a longer register by connecting the clock, D, and $\overline{S}$ inputs together and connecting the $\overline{CC}$ output of one device to the $\overline{E}$ input of the next less significant device. When the Start signal resets the register, the $\overline{E}$ signal goes HIGH, forcing the $Q_7(11)$ bit HIGH and inhibiting the device from accepting data until the previous device is full and its $\overline{CC}$ goes LOW. If only one device is used the $\overline{E}$ input should be held at a LOW logic level (Ground). If all the bits are not required, the register may be truncated and conversion time saved by using a register output going LOW rather than the CC signal to indicate the end of conversion.

4

LOGIC DIAGRAM/SYMBOLS

NOTE:
1. CELL LOGIC IS REPEATED FOR REGISTER STAGES. Q_5 TO Q_1 2502/3 Q_9 TO Q_1 2504
2. NUMBERS IN PARENTHESES ARE FOR 2504

V_{CC} = PIN 16
GND = PIN 8

V_{CC} = PIN 16
GND = PIN 12
NC = PINS 10, 15, 22

ABSOLUTE MAXIMUM RATINGS

Supply Voltage to Ground Potential Continuous	-0.5V to +7V
DC Voltage Applied to Outputs for High Output State	-0.5V to $+V_{CC}$ max
DC Input Voltage	-0.5V to +5.5V
Output Current, Into Outputs	30mA
DC Input Current	-30mA to +5.0mA
Temperature (Ambient) Under Bias	-55°C to +125°C
Storage Temperature	-65°C to +150°C

ORDERING INFORMATION

Temperature Range	Package	AM2502 Order No.	AM2503 Order No.	AM2504 Order No.
0 to +75°C	Ceramic DIP	AM2502CJE	AM2503CJE	AM2504CJG
0 to +75°C	Epoxy DIP	AM2502CPE	AM2503CPE	AM2504CPG
0 to +75°C	Dice	AM2502C/D	AM2503C/D	AM2504C/D
-55 to +125°C	Ceramic DIP	AM2502MJE	AM2503MJE	AM2504MJG
-55 to +125°C	Dice	AM2502M/D	AM2503M/D	AM2504M/D

ELECTRICAL CHARACTERISTICS

AM2502C 2503C 2504C T_A = 0°C to +75°C V_{CC} = 5.0V ±5%
AM2502M 2503M 2504M T_A = -55°C to +125°C V_{CC} = 5.0V ±10% (unless otherwise noted)

PARAMETERS	DESCRIPTION	TEST CONDITIONS			MIN.	TYP. (Note 1)	MAX.	UNITS
V_{OH}	Output HIGH Voltage	V_{CC} = MIN., I_{OH} = -0.48mA V_{IN} = V_{IH} or V_{IL}			2.4	3.6		Volts
V_{OL}	Output LOW Voltage	V_{CC} = MIN., I_{OL} = 9.6mA V_{IN} = V_{IH} or V_{IL}				0.2	0.4	Volts
V_{IH}	Input HIGH Level	Guaranteed input logical HIGH voltage for all inputs			2.0			Volts
V_{IL}	Input LOW Level	Guaranteed input logical LOW voltage for all inputs					0.8	Volts
I_{IL} (Note 2)	Unit Load Input LOW Current	V_{CC} = MAX., V_{IN} = 0.4V				-1.0	-1.6	mA
I_{IH} (Note 2)	Unit Load Input HIGH Current	V_{CC} = MAX., V_{IN} = 2.4V				6.0	40	μA
	Input HIGH Current	V_{CC} = MAX., V_{IN} = 5.5V					1.0	mA
I_{SC}	Output Short Circuit Current	V_{CC} = MAX., V_{OUT} = 0.0V			-10	-25	-45	mA
I_{CC}	Power Supply Current	V_{CC} = MAX.	AM2502	M		65	85	mA
				C		65	95	
			AM2503	M		60	80	mA
				C		60	90	
			AM2504	M		90	110	mA
				C		90	124	

NOTE 1: Typical Limits are at V_{CC} = 5.0V, 25°C ambient and maximum loading.
NOTE 2: Actual input currents are obtained by multiplying unit load current by input load factor (See Loading Rules).

SWITCHING CHARACTERISTICS T_A = 25°C, V_{CC} = 5.0V, C_L = 15pF

PARAMETERS	DESCRIPTION		MIN.	TYP.	MAX.	UNITS
t_{pd+}	Turn Off Delay CP to Output HIGH		10	26	38	ns
t_{pd-}	Turn On Delay CP to Output LOW		10	18	28	ns
t_s(D)	Set-up Time Data Input		-10	4	8	ns
t_s(S)	Set-up Time Start Input		0	9	16	ns
t_{pd+}(E)	Turn Off Delay E to Q_7(11) HIGH	(AM2503/4) C_P = H, $\overline{S}$ = L		13	19	ns
t_{pd-}(E)	Turn On Delay E to Q_7(11) LOW			16	24	ns
t_{pwL}(CP)	Minimum LOW Clock Pulse Width			28	46	ns
t_{pwH}(CP)	Minimum HIGH Clock Pulse Width			12	20	ns
f_{max}	Maximum Clock Frequency		15	25		MHz

2502/3 LOADING RULES (IN UNIT LOADS)

INPUT/ OUTPUT	PIN NO.'s	INPUT UNIT LOAD LOW	INPUT UNIT LOAD HIGH	FANOUT OUTPUT HIGH	FANOUT OUTPUT LOW
$\overline{E}$ (2503)	1	2	2	–	–
DO (2502)	1	–	–	12	6
$\overline{CC}$	2	–	–	12	6
Q_0	3	–	–	12	6
Q_1	4	–	–	12	6
Q_2	5	–	–	12	6
Q_3	6	–	–	12	6
D	7	2	2	–	–
GND	8	–	–	–	–
CP	9	1	1	–	–
$\overline{S}$	10	1	2	–	–
Q_4	11	–	–	12	6
Q_5	12	–	–	12	6
Q_6	13	–	–	12	6
$\overline{Q_7}$	14	–	–	12	6
Q_7	15	–	–	12	6
V_{CC}	16	–	–	–	–

2504 LOADING RULES (IN UNIT LOADS)

INPUT/ OUTPUT	PIN NO.'s	INPUT UNIT LOAD LOW	INPUT UNIT LOAD HIGH	FANOUT OUTPUT HIGH	FANOUT OUTPUT LOW
$\overline{E}$	1	2	2	–	–
DO	2	–	–	12	6
$\overline{CC}$	3	–	–	12	6
Q_0	4	–	–	12	6
Q_1	5	–	–	12	6
Q_2	6	–	–	12	6
Q_3	7	–	–	12	6
Q_4	8	–	–	12	6
Q_5	9	–	–	12	6
NC	10	–	–	–	–
D	11	2	2	–	–
GND	12	–	–	–	–
CP	13	1	1	–	–
$\overline{S}$	14	1	2	–	–
NC	15	–	–	–	–
Q_6	16	–	–	12	6
Q_7	17	–	–	12	6
Q_8	18	–	–	12	6
Q_9	19	–	–	12	6
Q_{10}	20	–	–	12	6
$\overline{Q_{11}}$	21	–	–	12	6
NC	22	–	–	–	–
Q_{11}	23	–	–	12	6
V_{CC}	24	–	–	–	–

NC = No Connection

MSI INTERFACING RULES

INTERFACING DIGITAL FAMILY	EQUIVALENT INPUT UNIT LOAD HIGH	EQUIVALENT INPUT UNIT LOAD LOW
Advanced Micro Devices 9300/2500 Series	1	1
FSC Series 9300	1	1
Advanced Micro Devices 54/7400	1	1
TI Series 54/7400	1	1
Signetics Series 8200	2	2
National Series DM 75/85	1	1
DTL Series 930	12	1

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INPUT/OUTPUT INTERFACE CONDITIONS

VOLTAGE INTERFACE CONDITIONS – LOW & HIGH

CURRENT INTERFACE CONDITIONS – LOW

CURRENT INTERFACE CONDITIONS – HIGH

SWITCHING TIME WAVEFORMS

KEY TO TIMING DIAGRAM

DEFINITION OF TERMS

SUBSCRIPT TERMS:

H HIGH, applying to a HIGH logic level or when used with V_{CC} to indicate high V_{CC} value.

I Input.

L LOW, applying to LOW logic level or when used with V_{CC} to indicate low V_{CC} value.

O Output.

FUNCTIONAL TERMS:

Fan-Out The logic HIGH or LOW output drive capability in terms of Input Unit Loads.

Input Unit Load One T^2L gate input load. In the HIGH state it is equal to I_{IH} and in the LOW state it is equal to I_{IL}.

CP The clock input of the register.

$\overline{CC}$ The conversion complete output. This output remains HIGH during a conversion and goes LOW when a conversion is complete.

D The serial data input of the regiter.

$\overline{E}$ The register enable. This input is used to expand the length of the register and when HIGH forces the Q_7(11) register output HIGH and inhibits conversion. When not used for expansion the enable is held at a LOW logic level (Ground).

Q_7(11) The true output of the MSB of the register.

$\overline{Q}_7$(11) The complement output of the MSB of the register.

Q_i i = 7(11) to 0 The outputs of the register.

$\overline{S}$ The start input. If the start input is held LOW for at least a clock period the register will be reset to Q_7(11) LOW and all the remaining outputs HIGH. A start pulse that is LOW for a shorter period of time can be used if it meets the set-up time requirements of the $\overline{S}$ input.

DO The serial data output. (The D input delayed one bit).

OPERATIONAL TERMS:

I_{IL} Forward input load current.

I_{OH} Output HIGH current, forced out of output V_{OH} test.

I_{OL} Output LOW current, forced into the output in V_{OL} test.

I_{IH} Reverse input load current.

Negative Current Current flowing out of the device.

Positive Current Current flowing into the device.

V_{IH} Minimum logic HIGH input voltage.

V_{IL} Maximum logic LOW input voltage.

V_{OH} Minimum logic HIGH output voltage with output HIGH current I_{OH} flowing out of output.

V_{OL} Maximum logic LOW output voltage with output LOW current I_{OL} flowing into output.

SWITCHING TERMS: (Measured at the 1.5V logic level).

t_{pd-} The propagation delay from the clock signal LOW-HIGH transition to an output signal HIGH-LOW transition.

t_{pd+} The propagation delay from the clock signal LOW-HIGH transition to an output signal LOW-HIGH transition.

t_{pd-}($\overline{E}$) The propagation delay from the Enable signal HIGH-LOW transition to the Q_7(11) output signal HIGH-LOW transition.

t_{pd+}($\overline{E}$) The propagation delay from the Enable signal LOW-HIGH transition to Q_7(11) output signal LOW-HIGH transition.

t_s(D) Set-up time required for the logic level to be present at the data input prior to the clock transition from LOW to HIGH in order for the register to respond. The data input should remain steady between t_s max, and t_s min. before the clock.

t_s($\overline{S}$) Set-up time required for a LOW level to be present at the $\overline{S}$ input prior to the clock transition from LOW to HIGH in order for the register to be reset, or time required for a HIGH level to be present on S before the HIGH to LOW clock transition to prevent resetting.

t_{pw}CP) The minimum clock pulse width (LOW or HIGH) required for proper register operation.

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AM2502/3 TRUTH TABLE

TIME	INPUTS			OUTPUTS									
t_n	D	$\overline{S}$	$\overline{E}$	D_0	Q_7	Q_6	Q_5	Q_4	Q_3	Q_2	Q_1	Q_0	$\overline{CC}$
0	X	L	L	X	X	X	X	X	X	X	X	X	X
1	D_7	H	L	X	L	H	H	H	H	H	H	H	H
2	D_6	H	L	D_7	D_7	L	H	H	H	H	H	H	H
3	D_5	H	L	D_6	D_7	D_6	L	H	H	H	H	H	H
4	D_4	H	L	D_5	D_7	D_6	D_5	L	H	H	H	H	H
5	D_3	H	L	D_4	D_7	D_6	D_5	D_4	L	H	H	H	H
6	D_2	H	L	D_3	D_7	D_6	D_5	D_4	D_3	L	H	H	H
7	D_1	H	L	D_2	D_7	D_6	D_5	D_4	D_3	D_2	L	H	H
8	D_0	H	L	D_1	D_7	D_6	D_5	D_4	D_3	D_2	D_1	L	H
9	X	H	L	D_0	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
10	X	X	L	X	D_7	D_6	D_5	D_4	D_3	D_2	D_1	D_0	L
	X	X	H	X	H	NC	NC	NC	NC	NC	NC	NC	NC

H = HIGH Voltage Level
L = LOW Voltage Level
X = Don't Care
NC = No Change

Note: Truth Table for 2504 is extended to include 12 outputs.

USER NOTES FOR A/D CONVERSION

1. The register can be used with either current switches that require a low voltage level to turn the switch on, or current switches that require a high voltage level to turn the current switch on. If current switches are used which turn on with a low logic level the resulting digital output from the register is active LOW. That is, a logic "1" is represented as a low voltage level. If current switches are used that turn on with a high logic level then the digital output is active HIGH; a logic "1" is represented as a high voltage level.
2. For a maximum digital error of ±½LSB the comparator must be biased. If current switches that require a high voltage level to turn on are used, the comparator should be biased +½LSB and if the current switches require a high logic level to turn on then the comparator must be biased -½LSB.
3. The register, by suitable selection of resistor ladder network, can be used to perform either binary or BCD conversion.
4. The register can be used to perform 2's complement conversion by offsetting the comparator ½ full range +½LSB and using the complement of the MSB Q_7(11) as the sign bit.
5. If the register is truncated and operated in the continuous conversion mode a lock-up condition may occur on power-on. This situation can be overcome by making the START input the OR function of $\overline{CC}$ and the appropriate register output.

AM2502/3 TIMING CHART

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AM2502/3/4 APPLICATION
CONTINUOUS CONVERSION ANALOG-TO-DIGITAL CONVERTER

This shows how the 2502/3/4 registers are used with a Digital-to-Analog converter and a comparator to form a very high-speed continuous conversion Analog-to-Digital converter. Conversion time is limited mainly by the speed of the D/A converter and comparator with typical conversion rates of 100,000 conversions per second. A 10-bit continuous conversion can be performed by connecting Q_1 to Q_3 and using Q_1 as the conversion complete signal.

PHYSICAL DIMENSIONS

2502/3

16-PIN MOLDED DIP

16-PIN HERMETIC DIP

16-PIN FLAT PAK

2504

24-PIN MOLDED DIP

24-PIN HERMETIC DIP

24-PIN FLAT PAK

CONNECTION DIAGRAMS
Top View

METALLIZATION AND PAD LAYOUT

Die size 0.95" x 0.142"

INTERSIL

ICL8018A, ICL8019A, ICL8020A

Quad Current Switch For D/A Conversion

GENERAL DESCRIPTION

The Intersil ICL8018A integrated circuit is a high speed precision current switch for use in current summing digital-to-analog converters. It consists of four logically controlled current switches and a reference device on a single monolithic silicon chip. The reference transistor combined with an external source and precision resistors determines the magnitude of the currents to be summed. By weighting the currents in proportion to the binary bit which controls them, the total output current will be proportional to the binary number represented by the input logic levels.

The performance and economy of the ICL8018A quad current switch make it ideal for use in digital-to-analog converters for industrial process control and instrumentation systems.

CONNECTION DIAGRAM

ORDERING INFORMATION

ACCURACY	MIL PART NO. CERAMIC DIP	COMMERCIAL PART NO. PLASTIC DIP
Individual Devices		
.01%	ICL8018AM–DD	ICL8018AC–PD
0.1%	ICL8019AM–DD	ICL8019AC–PD
1.0%	ICL8020AM–DD	ICL8020AC–PD
Matched Sets*		
.01%	ICL8018AM–X–DD	ICL8018AC–X–PD
0.1%	ICL8019AM–X–DD	ICL8019AC–X–PD
1.0%	ICL8020AM–X–DD	ICL8020AC–X–PD

*NOTE: Units ordered in equal quantities will be matched such that with respect to the V_{be} of the compensation transistor of the 8018 quad, the V_{be}'s of the 8019 will be within ±10 mV and the V_{be}'s of the 8020 will be within ±50 mV.

FEATURES

- TTL Compatible: LOW–0.8V HIGH–2.0V
- 12 Bit Accuracy
- 40 nsec, Switching Speed
- Wide Power Supply Range
- Low Temperature Coefficient

APPLICATIONS

- D/A-A/D Converters
- Digital Threshold Control
- Programmable Voltage Source
- Meter Drive
- X-Y Plotters

TRUTH TABLE

Logic Input	Nominal Output Current (mA)
0 0 0 0	1.875
0 0 0 1	1.750
0 0 1 0	1.625
0 0 1 1	1.500
0 1 0 0	1.375
0 1 0 1	1.250
0 1 1 0	1.125
0 1 1 1	1.000
1 0 0 0	0.875
1 0 0 1	0.750
1 0 1 0	0.625
1 0 1 1	0.500
1 1 0 0	0.375
1 1 0 1	0.250
1 1 1 0	0.125
1 1 1 1	0.000

SCHEMATIC DIAGRAM

EQUIVALENT CIRCUIT

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±20V	$V_O = V_B$ to +20V
Logic Input Voltage	−2 to V+	
Storage Temperature	−65°C to +150°C	$V_B = V^-$ to +5V
Operating Temperature ICL8018AM, ICL8019AM, ICL8020AM	−55°C to +125°C	Lead Temp (Soldering, 10 sec) 300°C
ICL8018AC, ICL8019AC, ICL8020AC	0°C to +70°C	

ELECTRICAL CHARACTERISTICS (4.5V ≤ V + ≤ 20V, V− = −15V, T_A = 25°C, V @ pin 6 = −5V)

PARAMETER	MIN	TYP	MAX	UNITS
Absolute Error				
ICL8018A			±.01	%
ICL8019A			±.1	%
ICL8020A			±1	%
Error Temperature Coefficient				
ICL8018A		± 2	±5	ppm/°C
ICL8019A		± 2	±25	ppm/°C
ICL8020A		± 2	±50	ppm/°C
Settling Time To ± ½LSB, R_L = 1 kΩ				
8 BIT		100		ns
12 BIT		200		ns
Switching Time To Turn On LSB		40		ns
Output Current (Nominal)				
BIT 1 (MSB)		1.0		mA
BIT 2		.5		mA
BIT 3		.250		mA
BIT 4 (LSB)		.125		mA
Zero Output Current		10	50	nA
Output Voltage Range	V_9 + 1V		+10	V
Input Coding-Complimentary Binary				
(See Truth Table)				
Logic Input Voltage				
"0" (Switch ON)			.8	V
"1" (Switch OFF)	2.0			V
Logic Input Current				
"0"		1.0	2	mA
"1"		.01	.1	μA
Power Supply Rejection				
V+		.005		%/V
V−		.0005		%/V
Supply Voltage Range				
V+	4.5	5	20	V
V−	−10	−15	−20	V
Supply Current (V_S = ±20V)				
I+		7	10	mA
I−		1	3	mA

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Linear

Amplifiers

Driver-Amplifier for Power Transistors
ICL8063 5-6

Driver; Power Driver for actuators, motors
ICH8510/20/30 5-14

Instrumentation, Commutating Auto Zero
ICL7605/6 5-22

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Operational, Commutating Auto Zero
ICL7600/1 5-40

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Waveform Generator
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Operational Amplifiers—General Purpose

Type	Description	V_{OS} (mV)	I_b (nA)	A_{VOL} (V/V)	GxB/W (MHz)	I_{CC} (mA)	T_A (°C)	Packages *	Remarks
101A	Gen Purpose, Uncompensated	2.0	75	50,000	0.8*	3.0	−55,+125	J,F,T	
101ALN	Guaranteed Noise 101A	2.0	75	50,000	0.8*	3.0	−55,+125	J,F,T	50nV/√Hz @ 10 Hz
107	Gen Purpose, Compensated	2.0	75	50,000	—	3.0	−55,+125	T	
108	Low Level, Uncompensated	2.0	2.0	50,000	1.0*	0.6	−55,+125	J,F,T	
108A	Low offset 108	0.5	2.0	80,000	1.0*	0.6	−55,+125	J,F,T	
108LN	Guaranteed Noise 108	2.0	2.0	50,000	1.0*	0.6	−55,+125	T	70nV/√Hz @ 10 Hz
124	Quad, Compensated	5.0	300	100,000*	1.0*	2.0	−55,+125	J	
207	Low bias, Compensated	2.0	75	50,000	—	3.0	−25,+85	T	
208	Low Level, Uncompensated	2.0	2.0	50,000	1.0*	0.6	−25,+85	J,F,T	
208A	Low offset 208	0.5	2.0	80,000	1.0*	0.6	−25,+85	J,F,T	
224	Quad, Compensated	7.0	500	100,000*	1.0*	2.0	−25,+85	J	
301A	Gen Purpose, Uncompensated	7.5	250	25,000	0.8*	3.0	0,+70	P,T	
301ALN	Guaranteed noise 301A	7.5	250	25,000	0.8*	3.0	0,+70	P,T	50nV/√Hz @ 10 Hz
307	Low bias, Compensated	7.5	250	25,000	—	3.0	0,+70	P,T	
308	Low Level, Uncompensated	7.5	7.0	25,000	1.0*	0.8	0,+70	F,J,P,T	
308A	Low offset 308	0.5	7.0	80,000	1.0*	0.8	0,+70	J,T	
308LN	Guaranteed noise 308	7.5	7.0	25,000	1.0*	0.8	0,+70	T	70nV/√Hz @ 10 Hz
324	Quad, Compensated	7.0	500	100,000*	1.0*	2.0	0,+70	J,P	
741	Gen Purpose, Compensated	5.0	500	50,000	1.0*	2.8	−55,+125	T	
741C	Gen Purpose, Compensated	6.0	500	25,000	1.0*	2.8	0,+70	P,T	
741HS	Guaranteed Slew Rate 741	5.0	500	50,000	1.0*	2.8	−55,+125	J,T	Slew Rate 0.7V/μS
741CHS	Guaranteed Slew Rate 741C	6.0	500	25,000	1.0*	2.8	0,+70	P,T	Slew Rate 0.7V/μS
741LN	Guaranteed Noise 741	5.0	500	50,000	1.0*	2.8	−55,+125	J,F,T	50nV/√Hz @ 10 Hz
741CLN	Guaranteed Noise 741C	6.0	500	25,000	1.0*	2.8	0,+70	P,T	50nV/√Hz @ 10 Hz
741K	High Accuracy 741	0.5	50	50,000	1.0	2.8	0 to 70	T	
748	General Purpose	1.0	80	25,000	0.8	2.0	−55 to 125	P,T	
748C	General Purpose, Compensated	1.0	80	25,000	0.8	2.0	0 to 70	P,T	
777	General purpose comparator	0.7	25	150,000	0.8	2.5	−55,+125	P,T	
777C	General purpose comparator	0.7	25	150,000	0.8	2.5	0,+70	P,T	
8008M	Low bias current, Compensated	5.0	10	20,00	1.0*	2.8	−55,+125	J,T	
8008C	Low bias current, Compensated	6.0	25	20,000	1.0*	2.8	0,+70	J,P,T	
IH5101	Ultra low noise		1,000	100,000	10.0	15.0	−55 to +125	I	
LH2101A	Dual high performance	2.0	100	25,000	0.8	2.5	−55 to 125	D	
LH2108	Dual super beta	2.0	3.0	25,000	1.0	0.4	−55 to 125	D	
LH2108A	Dual super beta	0.5	3.0	40,000	1.0	0.4	−55 to 125	D	
LH2301A	Dual high performance	7.5	300	15,000	0.8	2.5	0 to 70	D	
LH2308	Dual super beta	7.5	10	15,000	1.0	0.4	0 to 70	D	
LH2308A	Dual super beta	0.5	10	60,000	1.0	0.4	0 to 70	D	
LM2902	Quad, Compensated	2.0	45	100,000	1.0	0.7	−40 to 85	P	

Operational Amplifiers—Low Power Programmable

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Type	Description	V_{OS} (mV)	I_b (nA)	A_{VOL} (V/V)	GxB/W (MHz)	I_{CC} (μA)	at I_{set} (μA)	at V_S (V)	T_A (°C)	Packages
4250	Programmable, Uncompensated	5.0	10	25,000	—	8.0	1	±1.5	−55 to 125	T
4250C	Programmable, Compensated	5.0	10	25,000	—	8.0	1	±1.5	0,+70	T
		6.0	75	25,000	—	90	10	±1.5		
8021M	Programmable, Compensated	3.0	20	50,000	0.27	40	30	±6.0	−55,+125	J,T
8021C	Programmable, Compensated	6.0	30	50,000	0.27	50	30	±6.0	0,+70	T
8022M	Dual 8021M	3.0	20	50,000	0.27	40	30	±6.0	−55,+125	J,F
8022C	Dual 8021C	6.0	30	50,000	0.27	50	30	±6.0	0,+70	J,P
8023M	Triple 8021M	3.0	20	50,000	0.27	40	30	±6.0	−55,+125	J
8023C	Triple 8021C	6.0	30	50,000	0.27	50	30	±6.0	0,+70	J,P

*See package key, page 5-5

Operational Amplifiers—F.E.T. Input

Type	Description	V_{OS} (mV)	I_b (pA)	A_{VOL} (V/V)	GxB/W (MHz)	Slew Rate V/S	I_{CC} (mA)	T_A (°C)	Packages*	Remarks
LH0042	General Purpose	5.0	10	50,000		6	2.3	−55 to 125	T	
LF155	BIFET, Compensated	5	100	50,000	2.5*	5*	4	−55,+125	T	
LF155A	BIFET, Compensated	2	50	50,000	2.5*	3	4	−55,+125	T	
LF156	BIFET, Compensated	5	100	50,000	5*	7.5	7	−55,+125	T	
LF156A	BIFET, Compensated	2	50	50,000	4	10	7	−55,+125	T	
LF157	BIFET, Compensated for $A_V \geq 5$	5	100	50,000	20*	30	7	−55,+125	T	All BIFET amplifiers
LF157A	BIFET, Compensated for $A_{VK[A]} \geq 5$	2	50	50,000	15	40	7	−55,+125	T	offer low noise—
LV255	BIFET, Compensated	5	100	50,000	2.5*	5*	4	−25,+85	T	See data sheets
LF256	BIFET, Compensated	5	100	50,000	5*	7.5*	7	−25,+85	T	
LF257	BIFET, Compensated for $A_V \geq 5$	5	100	50,000	20*	30	7	−25,+85	T	
LF355	BIFET, Compensated	10	200	25,000	2.5*	5*	4	0,+70	T,P	
LF355A	BIFET, Compensated	2	50	50,000	2.5*	3	4	0,+70	T,P	
LF356	BIFET, Compensated	10	200	25,000	5*	12*	10	0,+70	T,P	
LF356A	BIFET, Compensated	2	50	50,000	4	10	7	0,+70	T,P	
LF357	BIFET, Compensated for $A_V \geq 5$	10	200	25,000	20*	50*	10	0,+70	T,P	
LF357A	BIFET, Compensated for $A_V \geq 5$	2	50	50,000	15	40	7	0,+70	T,P	
AD503	High accuracy, low offset	20	10	50,000		3	7 max	0,+70	T	
SU536	General Purpose	30	30	50,000		6	6	−55 to 85	T	
740M	General Purpose	20	200	50,000	3*	6*	5.2	−55,+125	T	
740C	General Purpose	110	2000	20,000	1*	6*	8.0	0,+70	T	
8007M	General Purpose, Compensated	20	20	50,000	1.0*	6*	5.2	−55,+125	T	
8007AM	8007M, Low I_b	30	1.0	20,000	1.0*	2.5	6	−55,+125	T	
8007C	General Purpose, Compensated	50	50	20,000	1.0*	6*	6	0,+70	T	
8007AC	8007C, Low I_b	30	1.0	20,000	1.0*	2.5	6	0,+70	T	
8007M-5	8007M, Low V_{os}, I_b	10	10	50,000	1.0*	3.0	5.2	−55,+125	T	15μV/°C
8007C-4	8007C, Low V_{os}, Offset Null	10	10	50,000	1.0*	3.0	6	0,+70	T	10μV/°C
8007C-5	8007C, Low V_{os}, Offset Null	10	10	50,000	1.0*	3.0	6	0,+70	T	15μV/°C
8043M	Dual 8007M	20	20	50,000	1.0*	6.0*	6	−55,+125	J	
8043C	Dual 8007C	50	50	20,000	1.0*	6.0*	6.8	−55,+125	J,P	
8500	MOSFET Input, Compensated	50	0.1	20,000	0.7*	0.5*	2.7*	−25,+85	T	
8500A	MOSFET Input, Super Low I_b	50	0.01	20,000	0.7*	0.5*	2.7*	−25,+85	T	

Operational Amplifiers—High Speed

Type	Description	V_{OS} (mV)	I_b (nA)	A_{VOL} (V/V)	GxB/W (MHz)	Slew Rate V/μS	I_{CC} (mA)	T_A (°C)	Packages
HA2500	High slew rate, Compensated	5.0	200	20,000	12*	25	6.0	−55,+125	F,T,J
HA2502	High slew rate, Compensated	8.0	250	15,000	12*	20	6.0	−55,+125	F,T,J
HA2505	High slew rate, Compensated	8.0	250	15,000	12*	20	6.0	0,+75	F,T
HA2507	High slew rate, Compensated	5.0	125	15,000	12	30	4.0	0 to 75	F,T
HA2510	High slew rate, Compensated	8.0	200	10,000	12*	50	6.0	−55,+125	F,T
HA2512	High slew rate, Compensated	10.0	250	7,500	12*	40	6.0	−55,+125	F,T
HA2515	High slew rate, Compensated	10.0	250	7,500	12*	40	6.0	0,+75	F,T
HA2517	High slew rate, Compensated	5.0	125	7,500	12	60	4.0	0 to 75	F,T
HA2520	Compensated for $A_V \geq 3$	8.0	200	10,000	30*	100	6.0	−55,+125	F,T,J
HA2522	Compensated for $A_V \geq 3$	10.0	250	7,500	30*	80	6.0	−55,+125	F,T,J
HA2525	Compensated for $A_V \geq 3$	10.0	250	7,500	30*	80	6.0	0,+75	F,T,J
HA2527	High slew rate, Compensated for $A_V \geq 3$	5.0	125	7,500	20	120	4.0	−65, to 150	F,T
8017M	High speed, Inverting	5.0	200	25,000	10*	130*	7.0	−55,+125	T,F
8017C	High speed, Inverting	7.0	200	25,000	10*	130*	8.0	0,+70	T,F

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Operational Amplifiers—High Impedance

Type	Description	V_{OS} (mV)	I_b (nA)	A_{VOL} (V/V)	Slew Rate (V/μS)	I_{CC} (mA)	T_A (°C)	Packages
HA2600	High impedance, Compensated	4.0	10	100,000	4	3.7	−55,+125	F,J,T
HA2602	High impedance, Compensated	5.0	25	80,000	4	4.0	−55,+125	F,J,T
HA2605	High impedance, Compensated	5.0	25	80,000	4	4.0	0,+75	F,J,T
HA2607	High impedance, Compensated	4.0	5	70,000	7	3.0	0 to 75	P
HA2620	2600 Compensated for $A_V \geq 5$	4.0	15	100,000	25	3.7	−55,+125	F,J,T
HA2622	2602 Compensated for $A_V \geq 5$	5.0	25	80,000	20	4.0	−55,+125	F,J,T
HA2625	2605 Compensated for $A_V \geq 5$	5.0	25	80,000	20	4.0	0,+75	F,J,T
HA2627	2607 Compensated for $A_V \geq 5$	4.0	5	70,000	35	3.0	0 to 75	P

Video Amplifiers

Type	Description	Gains (V/V)	Bandwidths (MHz)	E_N (IN) μV (rms)	Output Offset (V)	I_{CC} (mA)	T_A (°C)	Packages
733M	Gain selectable video amp.	400,100,10*	40,90,120*	12	1.5	24	−55,+125	T
733C	Gain selectable video amp.	400,100,10*	40,90,120*	12	1.5	24	0,+70	T

*See package key, page 5-5

Voltage Followers

Type	Description	V_{OS} (mV)	I_{IN} (nA)	A_V (MIN) (V/V)	3db B/W (MHz)	Slew Rate (V/μS)	Swing (V)	I_{CC} (mA)	T_A (°C)	Packages*
102	Voltage Follower	5	10	0.999	—	—	±10	4.0	−55,+125	F,T
110	Voltage Follower	4	3	0.999	—	—	±10	—	−55,+125	D,F,T
202	Voltage Follower	10	15	0.999	—	—	±10	—	−25,+85	T
210	Voltage Follower	4	3	0.999	15*	30*	±10	4.0	−25,+85	D,T
302	Voltage Follower	15	30	0.9985	15*	30*	±10	4.0	0,+70	T
310	Voltage Follower	7.5	7	0.999	15*	30*	±10	—	0,+70	D,P,T
LH2110		4.0	3	0.999	—	—	±10	4.0	−55 to 125	D
LH2310		7.5	7	0.999	—	—	±10	4.0	0 to 70	D

Comparators

Notes: Tpd measured for 100 mV step with 5 mV overdrive.
I_{CC} measured for $V_S = \pm 15V$

Type	Description	V_{OS} (V)	I_b (nA)	A_V (V/mV)	tpd (nS)	I_{CC} (mA)	V_{OL} at (V)	I_{OL} (mA)	T_A (°C)	Packages
111	Precision Comparator	3	100	200*	200*	6	0.4	8	−55,+125	D,F,T
211	Precision Comparator	3	100	200*	200*	6	0.4	8	−25,+85	D,F,T
311	Precision Comparator	7.5	250	200*	200*	7.5	0.4	8	0,+70	D,F,J,P,T
8001M	Low Power Comparator	3	100	15	250*	2	0.5	2	−55,+125	T
8001C	Low Power Comparator	5	250	15	250*	2	0.4	2	0,+70	T
LM139	Quad. Comparator	5	100	200*	1300*	2	0.7	4	−55,+125	D
LM139A	Low Offset 139	2	100	200*	1300*	2	0.4	3	−55,+125	D
LM239	Quad. Comparator	5	250	200*	1300*	2	0.7	4	−25,+85	D
LM239A	Low Offset 239	2	250	200*	1300*	2	0.4	3	−25,+85	D
LM339	Quad. Comparator	5	250	200*	1300*	2	0.7	4	0,+70	D,P
LM339A	Low Offset 339	2	250	200*	1300*	2	0.4	3	0,+70	D,P
LH2111	Dual Precision Comparator	3	100	200	200	6	0.4	8	−55 to 125	D
LH2311	Dual Precision Comparator	7.5	250	200	200	7.5	0.4	8	0 to 70	D
MC2901	Quad. Comparator	2	25	100	300	0.8	.25	4	0 to 70	D,F
MC3302	Quad. Comparator	3	25	30	300	0.8	.25	4	0 to 70	D,F

Power Amplifiers

Note 1. Specifications apply at ±30V supplies.
2. All units packaged in 8 lead TO3 can.
3. Fully protected against inductive current flow.
4. Externally settable output current limiting.

Type	Description	Use	Output Current (A)	Output Swing (V)	V_{OS} (mV)	I_b (nA)	A_{VOL} (V/V)	Slew Rate (V/μS)	Quiescent I_{CC} (mA)	T_A (°C)
ICH8510M	Hybrid Power Amp.	Servo	1.0	±26	3.0	250	100,000	0.5	40	−55,+125
ICH18510C	Hybrid Power Amp.	and	1.0	±26	6.0	500	100,000	0.5	50	−25,+85
ICH8520M	Hybrid Power Amp.	Actuator	2.0	±26	3.0	250	100,000	0.5	40	−55,+125
ICH8520C	Hybrid Power Amp.		2.0	±26	6.0	500	100,000	0.5	50	−25,+85
ICH8530M	Hybrid Power Amp.		2.7	±25	3.0	250	100,000	0.5	40	−55,+125
ICH8530C	Hybrid Power Amp.		2.7	±25	6.0	500	100,000	0.5	50	−25,+85
ICL8063C	Monolithic Power Amp.	Power	2.0	±27	50		6		250	0,+70
ICL8063M	Monolithic Power Amp.	Transistors	2.0	±27	75		6		300	−55,+125

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Voltage Regulators

Type	Input Voltage (V) MIN	Input Voltage (V) MAX	Output Voltage (V) MIN	Output Voltage (V) MAX	Input/Output Differential (V) MIN	Input/Output Differential (V) MAX	Load Current (mA) MIN	Load Current (mA) MAX	Load Reg^n O-F.L. (%)	Line Reg^n (%/V)	Avg. Temp Coeff (%/°C)	Pd at 25°C (mW)	T_j (°C)	Packages
100	8.5	40	2.0	30	3.0	30	3.0	12	0.5	0.2	0.005	500	−55,+150	F,T
105	8.5	50	4.5	40	3.0	30	0	12	0.05	0.06	0.005	500	−55,+150	F,T
300	8.0	30	2.0	20	3.0	20	3.0	12	0.5	0.2	0.03	300	0,+70	T
305	8.0	40	4.5	30	3.0	30	0	12	0.05	0.06	0.03	500	0,+70	T
723	9.5	40	2.0	37	3.0	38	0	50	0.15	0.03	0.015	800	−55,+125	T,J
723C	9.5	40	2.0	37	3.0	38	0	50	0.2	0.03	0.015	660	0,+70	P,T

Sample and Hold

Type	V_{analog} (V_{p-p})	Z_{in} (MΩ @ 10 Hz)	V_{OS} (mV)	Drift Rate (mV/sec)	Package
IH5110	±15	100	40	5	D
IH5111	±20	100	40	5	D
IH5112	±15	100	10	5	D
IH5113	±20	100	10	5	D
IH5114	±15	100	5	5	D
IH5115	±20	100	5	5	D

*See package key, page 5-5

Special Function Circuits

Type		Accuracy	V_S (V)	T_A (°C)	Packages
AD590	Temperature transducer—output linear at 1μA/°K	±1°C	4 to 15	−55 to 150	H
8013AM	Four quadrant multiplier. Output proportional to algebraic products	±0.5%	±15	−55,+125	T
8013BM	of two input signals. Features ±0.5% accuracy; internal op-amp	±1.0%	±15	−55,+125	T
8013CM	for level shift, division and square root functions; full ±10V	±2.0%	±15	−55,+125	T
8013AC	input/output range; 1 MHz bandwidth.	±0.5%	±15	0,+70	T
8013BC		±1.0%	±15	0,+70	T
8013CC		±2.0%	±15	0,+70	T
8038AM	Simultaneous Sine, Square, and Triangle wave outputs T²L	1.5%	±5 to ±15	−55,+125	J
8038AC	compatible to 28V over frequency range from 0.001 Hz to 1.0 MHz.	1.5%	±5 to +15	0,+70	P
8038BM	Low distortion (<1%); high linearity (0.1%); low frequency drift with	3.0%	±5 to ±15	−55,+125	J
8038BC	temperature (50ppm/°C max.), variable duty cycle 2%-98%).	3.0%	±5 to ±15	0,+70	P
8038CC	External frequency modulation.	5.0%	±5 to ±15	0,+70	P
8048BC	Log amp. 1V/decade (Adjustable). 120 db range	±30 mV	±15	0,+70	J,P
8048CC	with current input. Error referred to output	±60 mV	±15	0,+70	J,P
8049BC	Antilog amp, adjustable scale factor.	±10 mV	±15	0,+70	J,P
8049CC	Error referred to input	±30 mV	±15	0,+70	J,P
ICL8061	The ICL8061 converts a wide range of photographic variables				
ICL8062	to electronic signals from which f-stop, aperture, EV and BV may be obtained. The ICL8062 converts the signals from the 8061 into output drive voltages.				
8069	1.2V temperature compensated voltage reference		5 to 15	−55 to 125	Q
8211M	Micropower voltage detector/indicator/voltage regulator/		2 to 30	−55,+125	T
8211C	programmable zener. Contains 1.15V micropower reference		2 to 30	0,+70	P,T
8212M	plus comparator and hysteresis output. Main output		2 to 30	−55,+125	T
8212C	inverting (8212) or non-inverting (8211).		2 to 30	0,+70	P,T

Notes: 1. All parameters are specified at $V_S = \pm 15V$ and $T_A = +25°C$ unless otherwise noted.
2. All parameters are worst case MIN/MAX limits except for those marked * which are typical.

PACKAGE KEY
D—Solder lid side brazed ceramic dual in line.
F—Ceramic flat pack.
J—Glass frit seal ceramic dual in line.
P—Plastic dual in line.
T—Metal can (TO5 size)

Operational Amplifiers—CMOS

Type	Description	Compensation	Offset Null	V_{OS} Selection	I_{OS}	I_B	Input CMR	Output Swing	Packages
7611	Single, Selectable I_Q	Internal	Yes	2, 5, 15 mV	0.5pA	1pA	V_{SUPPLY} − 100m V	V_{SUPPLY} − 100 mV	P,T
7612	Single, Selectable I_Q, Extended CMVR	Internal	Yes	2, 5, 15 mV	0.5pA	1pA	V_{SUPPLY} + 300 mV	V_{SUPPLY} − 100 mV	P,T
7613	Single, Selectable I_Q, Input Protected	Internal	Yes	2, 5, 15 mV	0.5pA	1pA	V_{SUPPLY} − 100 mV	V_{SUPPLY} − 100 mV	P,T
7614	Single, Fixed I_Q	External	Yes	2, 5, 15 mV	0.5pA	1pA	V_{SUPPLY} − 100 mV	V_{SUPPLY} − 100 mV	P,T
7615	Single, Fixed I_Q, Input Protected	External	Yes	2, 5, 15 mV	0.5pA	1pA	V_{SUPPLY} − 100 mV	V_{SUPPLY} − 100 mV	P,T
7621	Dual, Fixed I_Q	Internal	No	2, 5, 15 mV	0.5pA	1pA	V_{SUPPLY} − 100 mV	V_{SUPPLY} − 100 mV	P,T
7622	Dual, Fixed I_Q	Internal	Yes	2, 5, 15 mV	0.5pA	1pA	V_{SUPPLY} − 100 mV	V_{SUPPLY} − 100 mV	P,J
7631	Triple, Selectable I_Q	Internal	No	5, 10, 20 mV	0.5pA	1pA	V_{SUPPLY} − 100 mV	V_{SUPPLY} − 100 mV	P,J
7632	Triple, Selectable I_Q	None	No	5, 10, 20 mV	0.5pA	1pA	V_{SUPPLY} − 100 mV	V_{SUPPLY} − 100 mV	P,J
7641	Quad, Fixed I_Q	Internal	No	5, 10, 20 mV	0.5pA	1pA	V_{SUPPLY} − 100 mV	V_{SUPPLY} − 100 mV	P,J
7642	Quad, Fixed I_Q	Internal	No	5, 10, 20 mV	0.5pA	1pA	V_{SUPPLY} − 100 mV	V_{SUPPLY} − 100 mV	P,J

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Instrumentation Amplifiers—Commutating Auto Zero

Type	Description	V_{OS} (μV)	ΔV_{OS} (μV/year)	I_{SUPP} (pA)	A_V (dB)	V_{SUPPLY}	I_{BIAS} (pA)	Packages	T_A °C
ICL7600C	Compensated	±2	0.2	1	90 min	+5 to +16	±30	J,P	0 to 70
ICL7600I	Compensated	±2	0.2	1	90 min	+5 to +16	+30	J,P	−25 to 85
ICL7600M	Compensated	±2	0.2	1	90 min	+5 to +16	±30	J,P	−55 to 125
ICL7601C	Uncompensated	±2	0.2	1	90 min	+5 to +16	±30	J,P	0 to 70
ICL7601I	Uncompensated	±2	0.2	1	90 min	+5 to +16	±30	J,P	−25 to 85
ICL7601M	Uncompensated	±2	0.2	1	90 min	+5 to +16	±30	J,P	−55 to 125

Operational Amplifiers—Commutating Auto Zero

Type	Description	V_{OS} (μV)	ΔV_{OS} (μV/year)	I_{SUPP} (mA)	A_V (dB)	V_{SUPPLY}	I_{BIAS} (pA)	Packages	T_A °C
ICL7605C	Compensated	±2	0.5	1.7	90 min	5 to 10	±30	J,P	0 to 70
ICL7605I	Compensated	±2	0.5	1.7	90 min	5 to 10	±30	J,P	−25 to 85
ICL7605M	Compensated	±2	0.5	1.7	90 min	5 to 10	±30	J,P	−55 to 125
ICL7606C	Uncompensated	±2	0.5	1.7	90 min	5 to 10	±30	J,P	0 to 70
ICL7606I	Uncompensated	±2	0.5	1.7	90 min	5 to 10	±30	J,P	−25 to 85
ICL7606M	Uncompensated	±2	0.5	1.7	90 min	5 to 10	±30	J,P	−55 to 125

INTERSIL

ICL8063 Power Transistor Driver-Amplifier

FEATURES:

- **Converts ±12V Outputs from Op Amps and other linear functions up to ±30V levels**
- **When used in conjunction with general-purpose op amps and external complementary power transistors, system can deliver > 50 Watts to external loads**
- **Has built-in Safe Area Protection and short-circuit proof protection**
- **Produces 25mA typical quiescent current in typical power amp configuration while capable of delivering ±2 Amps full output current**
- **Has built in ±13V Regulators to power op amps or other external functions**
- **500kΩ input impedance with R_{BIAS} = 1MΩ**

GENERAL DESCRIPTION

The ICL8063 is a unique monolithic power transistor driver *and* amplifier that allows construction of minimum chip power amplifier systems complete with safe operating area circuitry, short circuit protection and built-in voltage regulators, without adding extra power supplies. It is primarily intended for complementary symmetrical outputs.

Designed to operate with all varieties of operational amplifiers and other functions and two external power transistors of any construction technique and 8 to 10 passive components, the ICL8063 is ideal for use in such applications as linear and rotary actuator drivers, *stepper motor drivers, servo motor drivers*, power supplies, power DACs and electronically controlled orifices.

The ICL8063 takes the output levels (typically ±11V) from an op amp and boosts the levels up to ±30V to drive any power transistors, (e.g. 2N3055 (NPN) and 2N3789 (PNP)). The outputs from the ICL8063 drive the external power transistors' base leads with up to 100 milliamperes of current.

This amplifier-driver contains internal positive and negative regulators to drive an op amp, or numerous other functions; thus, only. ±30V supplies are needed for a complete power amp.

The ICL8063 provides built-in power supplies and will operate from inputs generated by most of the op amps in use today---regardless of technology---as well as many other linear functions, such as timers, comparators and waveform generators. And it will drive almost all power transistors with breakdown voltages up to 70 volts.

CONNECTION DIAGRAM

CHIP TOPOGRAPHY

ORDERING INFORMATION

ICL8063MJE	- CERDIP, -55°C TO 125°C
ICL8063CJE	- CERDIP, 0°C TO +70°C
ICL8063CPE	- PLASTIC DIP, 0°C TO 70°C

SCHEMATIC DIAGRAM

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ABSOLUTE MAXIMUM RATINGS @ $T_A = 25°C$

Supply Voltage	±35V
Power Dissipation	500mW
Input Voltage (Note 1)	±30V
Operating Temperature Range	ICL8063MJE −55°C to +125°C
	ICL8063CPE 0°C to 70°C
	ICL8063CJE 0°C to 70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 10 sec)	300°C

Note 1: For supply voltages less than ±30V the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (@ 25°C; V_{CC} = ±30V)

SYMBOL	CHARACTERISTIC	TEST CONDITIONS	MIN/MAX LIMITS						UNITS
			ICL8063M			ICL8063C			
			−55°C	+25°C	+125°C	0°C	+25°C	+70°C	
V_{OS}	Max. Offset Voltage	See Figure 1	150	50	50	150	75	75	mV
I_{OUT}^{+}	Min. Positive Drive Current	See Figure 2	50	50	50	40	40	40	mA
I_Q^{+}	Max. Positive Output Quiescent Current	See Figure 3	500	250	250	600	300	300	μA
I_{OUT}^{+}	Min. Negative Drive Current	See Figure 2	25	25	25	20	20	20	mA
I_Q^{-}	Max. Negative Output Quiescent Current	See Figure 4	500	250	250	600	300	300	μA
$V_{REG}^{\pm}$	Regulator Output Voltages Range	See Figure 5	±13.7 ±1.2V	±13.7 ±1.0V	±13.7 ±1.5V	±13.7 ±1.0V	±13.7 ±1.0V	±13.7 ±1.0V	V
Z_{IN}	A.C. Input Impedance	See Figure 6	400	400	400	400	400	400	kΩ
V_{CC}	Power Supply Range		±5 to ±35V						V
I_Q	Power Supply Quiescent Currents		10	6	6	12	7	7	mA
A_V	Range of Voltage Gain	See Figure 7 V_{IN} = 8Vp-p	6±2	6±2	6±2	6±2	6±2	6±2	V/V
$V_{OUT(MIN)}$	Minimum Output Swing	See Figure 7; Increase V_{IN} until V_{OUT} flattens	±27	±27	±27	±27	±27	±27	V
I_{IN}	Input Bias Current	See Figure 8	100	100	100	100	100	100	μA

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Figure 1: Offset Voltage Measurement

Figure 2: Output Current Measurement

Figure 3: Positive Output Quiescent Current

Figure 4: Negative Output Quiescent Current

Figure 5: On Chip Regulator Measurement

Figure 6: A.C. Input Impedance Measurement

Figure 7: Gain and Output Voltage Swing Measurement

Figure 8: Input Bias Current Measurement

APPLICATION

A problem that has been studiously ignored by integrated circuit manufacturers as being too difficult is a dilemma faced almost every day by circuit designers - interfacing the low voltage, low current output world (relatively speaking) of standard linear and digital devices to that of power transistors and darlingtons---higher by several orders of magnitude.

A low level op amp, for example, has a typical voltage range of ±6 to ±12V and output current usually on the order of about 5 or so milliamperes. A power transistor with a ±35 volt supply requirement and a collector current of 5 amperes or so, and with a beta, or gain of 100 needs at least 50 milliamperes to drive it.

Quite a jump.

For the majority of applications, cost considerations (among other things) mean that only one choice is possible: painstakingly building up a discrete circuit that performs this very necessary power transistor driving and amplifying function. But it's not just a matter of amplifying the current and voltage to the required levels. To protect the devices, all sorts of back up circuitry must be built in; such things as safe area protection and short circuit protection. It's also necessary to build in a number of supplies, because of the varying requirements of the different components.

Recently, integrated power amplifier devices have been introduced, but these are still only partial solutions---and expensive ones at that. Moreover, these so-called solutions often require additional protection circuitry. So, whatever reduction in component count and circuit complexity achieved is lost due to these additional protection requirements.

What's necessary is to integrate---totally---this crucial portion of almost every circuit design.

The ICL8063 is just such a total solution. It's a monolithic power transistor driver and power transistor amplifier circuit on the same chip, has all the necessary safe operating area circuitry and short circuit protection, and has on-chip ±13V voltage regulators to eliminate the need for extra external power supplies.

With the ICL8063 more time can be spent on designing systems---and less time designing circuits. Following are a few applications which illustrate this clearly:

1. Using the ICL8063 to make a complete Power Amplifier

As Figure 9 shows, using the ICL8063 allows the circuit designer to build a power amplifier block capable of delivering ±2 amperes at ±25 volts (50 watts) to any load, with only three additional discrete devices and 8 passive components. Moreover, the circuit draws only about ±30 milliamperes of quiescent current from either of the ±30V power supplies. A similar design using discrete components would require anywhere from 50 to 100 components.

Slew rate is about the same at that of a 741 op amp by itself, except that the output current can slew up to 2 amps at roughly 1V/μs (that's a 10 ohm load to ground and ±20V output across this resistance). Input current, voltage offset, CMRR and PSRR are also the same. Use of 1,000 picofarad

compensation capacitors (three in this configuration) allows good stability down to unity gain non-inverting (the worst case). This circuit will drive a 1000pF C_L to Gnd, with no significant problems. In other words the circuit can drive 30 feet of RG-58 coaxial cable for line driver applications with no problems.

As Figure 10 indicates, setting up a current limiting (safe area) protection circuit is straightforward. The 0.4 ohm, 5 watt resistors set the maximum current one can get out of the output. The equation this SOA circuit follows is: $V_{OUT} + I_L \times 0.4\Omega = 0.7V + I(24.5k)$. When $I_L R_3 - IR_2 = 0.7V$ safe area protection is achieved.

Figure 9: Standard Circuit Diagram

Figure 10: Current Limiting (Safe Area) Protection Circuit

Solving these equations we get the following:

V_{OUT}	I	I_L @ 25°C	I_L @ 125°C
24V	1ma	3 amps	2.4 amps
20V	830μA	2.8 amps	
16V	670μA	2.6 amps	
12V	500μA	2.4 amps	1.8 amps
8V	333μA	2.1 amps	
4V	167μA	1.9 amps	
0V	0μA	1.7 amps	1.1 amps

As these equations indicate, maximum power delivered to a load is obtained when $V_{OUT} \geq 24V$, the optimum voltage one needs when driving any DC motor, actuator, etc.

Often design requirements necessitate an unsymmetrical output current capability. In that case, instead of the 0.4 ohm resistors protecting the npn and pnp output stages, as shown in Figure 9, simply substitute any other value. For example, if up to 3 amps are required when $V_{OUT} \geq +24V$ and only 1 amp out when $V_{OUT} \geq -24V$, use a 0.4 ohm resistor between pin 8 and pin 9 on the ICL8063 and a 1 ohm, 2 watt resistor between pin 7 and pin 8. Maximum output current versus V_{OUT} for varying values of protection resistors are as follows:

V_{OUT}	0.4Ω @ 25°C	0.68Ω @ 25°C	1Ω @ 25°C
24V	3 amps	1.7 amps	1.2 amps
12V	2.4 amps	1.4 amps	0.9 amps
0V	1.7 amps	1.0 amps	0.7 amps

The biasing resistors located between pin 13 and pin 14 and between pin 2 and pin 4 are typically 1M-ohm for $V_{CC} = \pm 30V$, which guarantees adequate performance in such applications as DC motor drivers, power DACs, programmable power supplies and line drivers (with ±30 volt supplies). The table that follows shows the proper value for R_{BIAS} for optimum output current capability with supply voltages between ±5V and ±30V.

$\pm V_{CC}$	R_{BIAS}
30V	1 MΩ
25V	680kΩ
20V	500kΩ
15V	300kΩ
10V	150kΩ
5V	62kΩ

If 30V and 1 meg ohms are used, performance curves appear as shown in Figure 11.

Figure 11. Typical Performance Curve of Max. Output Current vs. V_{OUT} for Fixed R_{BIAS} = 1MΩ

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When buying external power transistors, careful attention should be paid to beta values. For 2N3055 and 2N3789 transistors used in this circuit, beta should be no more than 150 max at $I_C = 20mA$ and $V_{CE} = 30V$. This beta value sets the quiescent current at less than 30 mA when not delivering power to a load.

The design in Figure 9 will tolerate a short to ground indefinitely, provide adequate heat sinking is used. However if V_{OUT} is shunted to ±30V the output transistors (2N3055 and 2N3789) will be destroyed. But since the safe operating area for both devices is 4 amps at 30 volts, the problem does not occur for $V_{CC} = \pm 15V$.

A typical bode plot of the power amplifier system is shown in Figure 12. Referring to Figure 6, the schematic for this bode plot is shown below:

Figure 12: Bode Plot of Open Loop Gain of Above Schematic

Figure 13: Typical Performance of R_{OUT} vs. Frequency of Power Amplifier System

2. Designing A Simple Function Generator

Using a variation of the fundamental power amplifier building block described in the previous section, the ICL8063 can be implemented in the design of a simple, low cost function generator (Figure 14). It will allow generation of sine waves, triangular waves and square waves at the output from 2 hertz to 20 kilohertz. This complete test instrument can be plugged into a standard 110 VAC line for power. V_{OUT} will be up to ±25V (50V p-p) across loads as small as 10 ohms (that's about 2.5 amps maximum output current).

All capacitor working voltages should be greater than 50V DC. All resistors should be 500mW, unless otherwise indicated. Keep the interconnecting leads from pin 2 of the 741 to the 10k-ohm feedback resistor and 10k-ohm amplitude adjust potentiometer as short as possible. Less than 2 inches long is best, since this point is the summing junction of an operational amplifier. Failure to do so results in oscillation problems. Because of the slewing of the 741, the generator will not produce a 56V p-p amplitude all the way up to 20kHz. Full output swing is possible up to about 5kHz. Beyond this point slewing begins and undistorted p-p output will diminish. Due to this effect, amplitude at 20kHz is about 20V p-p (±10V). This could be remedied by using a higher slew rate op amp such as the LF156.

Figure 14: Power Function Generator

3. Building a Constant Current Motor Drive Circuit

The constant current motor drive configuration shown in Figure 15 is an extremely simple circuit to construct using the ICL8063. This minimum device circuit can be used to drive DC motors where there is some likelihood of stalling or lock up. If the motor locks, the current drive remains constant and the system does not destroy itself. Using this approach two 6V batteries are sufficient for decent performance. A 10 volt input will produce one amp of output current to drive the motor. If the motor is stalled, I_{OUT} remains at 1 amp.

For example, suppose it's necessary to drive a 24V DC motor with 1 amp of drive current into the motor. First make V_{CC} at least 6 volts more than the motor being driven (in this case 30 volts). Next select R_{BIAS} according to $\pm V_{CC}$ from the data sheet, which indicates an R_{BIAS} = 1M-ohm. Then choose R_1, R_2, and R_3 for optimum sensitivity. That means making R_a = 1 ohm to minimize the voltage drop across R_a (the drop will be 1amp x 1 ohm or 1 volt). If 1 amp/volt sensitivity is desireable let $R_2 = R_1$ and choose $R_2 = R_1$ = 10 k-ohms to minimize feedback current error. Then a ±1V input voltage will produce a ±1 amp current through the motor.

All capacitors should be at least 50 volts working voltage and all resistors 500 mW, except for those valued at 0.4 ohms, and R_a. Power across R_a = I x V = 1 amp x 1 volt = 1 watt, so at least a 2 watt value should be used. Use large heat sinks for the 2N3055 and 2N3791 power transistors. A Delta NC-641 or the equivalent is appropriate. Use a thermal compound when mounting the transistor to the heat sink. (See Intersil ICH8510 data sheet).

Figure 15: Constant Current Motor Drive

4. Building A Low Cost 8 ohm per channel Hi-fi Amplifier.

For about $20 per channel, it's possible to build a high fidelity amplifier using the ICL8063 capable of driving 8 ohm speakers. A channel is defined here as all amplification between turntable or tape output and power stage to drive 8 ohm speakers (Figure 16).

The input 741 stage is a preamplifier with R.I.A.A. equalization for records (disc). Following the first 741 stage is a 10k-ohm control pot, whose wiper arm feeds into the power amplifier stage consisting of a second 741, the ICL8063 and

the power transistors. To achieve good listening results, selection of proper resistance values in the power amplifier stage is important. Best listening is at a gain value of 6[(5kΩ + 1kΩ)/1kΩ = 6]. Don't go below 3, since the first stage 741 preamp puts out only ±10 volt maximum signals. So, if maximum power is necessary this value must be multiplied by 3 to get ±30 volt levels at the output of the power amp stage.

Each channel delivers about 56 volts p-p across an 8 ohm speaker and this converts to 50 watts RMS power. This is derived as follows:

$$\text{Power} = \frac{V_{rms}^2}{8\ \text{ohms}},\quad V_{rms} = \frac{56\text{V p-p}}{2.82} = 20\text{V},\ 20\text{V}^2 = 400\text{V}^2$$

$$\therefore \text{Power} = \frac{400^2}{8\ \text{ohms}} = 50\ \text{watts RMS Power.}$$

Distortion will be < 0.1% up to about 100Hz, and then it increases as the frequency increases, reaching about 1% at 20kHz.

The ganged switch at the input is for either disc playing or FM, either from an FM tuner or a tape amplifier. Assuming DC coupling (not capacitive coupling) on the outputs, there is no need for a DC reference to ground (resistor) for FM position. To clear the signal in the FM position, place a 51k-ohm resistor to ground as shown in Figure 16 (from FM input position to ground).

Figure 16: Hi Fi Amplifier

Figure 17: Typical Performance Curve of $\frac{E_{OUT}}{V_{IN}}$ vs. Frequency For Typical Circuit Shown

Figure 18: Typical Performance Curve of Input Impedance Versus Frequency for Typical Circuit Shown

NOTE: Intersil offers a hybrid power amplifier similar to the circuit shown in Figure 9, the ICH8510, ICH8520, & ICH8530, "Power Amplifier, Motor & Actuator Driver". This hybrid circuit has the following features:

- **Capable of delivering 2.7 amps @ 24-28V d.c. operation (30V supplies)**
- **Protected against inductive kick back with internal power limiting**
- **Programmable current limiting (short circuit protection)**
- **Package is electrically isolated (allowing easy heat sinking)**
- **d.c. gain > 100dB**
- **20mA typical standby quiescent current**
- **Popular 8 pin TO-3 package**
- **Internal frequency compensation**
- **Can drive up to 0.1 horsepower motors.**

5

PACKAGE DIMENSIONS

16 PIN CERDIP (JE)

16 PIN PLASTIC DIP (PE)

INTERSIL

ICH8510/ICH8520/ICH8530 Power Amplifier Motor and Actuator Driver

KEY FEATURES:

- Capable of delivering 2.7 amps @ 24–28V d.c. operation (30V supplies)
- Protected against inductive kick back with internal power limiting
- Programmable current limiting (short circuit protection)
- Package is electrically isolated (allowing easy heat sinking)
- d.c. gain >100dB
- 20mA typical standy quiescent current
- Popular 8 pin TO-3 package
- Internal frequency compensation
- Can drive up to 0.1 horsepower motors.

DESCRIPTION:

The ICH8510/8520/8530 is a family of hybrid power amplifiers that have been specifically designed to drive linear and rotary actuators, electronic valves, push-pull solenoids, and d.c. & a.c. motors.

There are three models available for up to ±30V power supply operation. One model will deliver up to 2.7 amps @ 24 volt output levels, while the remaining models deliver 2 amps & 1 amp @ 24V outputs. All amplifiers are protected against shorts to ground by the addition of 2 external protection resistors.

The design uses a conventional 741 operational amplifier, a special monolithic driver chip (BL8063), NPN & PNP power transistors, and internal frequency compensating capacitors. The chips are mounted on a beryllium oxide substrate, for optimum heat transfer to the metal package; this substrate provides electrical isolation between amplifiers and metal package.

The I.C. power driver chip has built-in regulators to drive the 741 @ typically ±13v supply voltages.

PACKAGE CONFIGURATION:

8 Lead TO-3 Metal Can

CONNECTION DIAGRAM

SCHEMATIC DIAGRAM

ORDERING INFORMATION:

ICH8510MKA* ICH8510IKA*	1 amp model
ICH8520MKA ICH8520IKA	2 amp model
ICH8530MKA ICH8530IKA	2.7 amp model

*(M) −55°C →+125°C operation
*(I) −25°C →+85°C operation

ABSOLUTE MAXIMUM RATINGS @ T_A = 25°C

Supply Voltage	±35V
Power Dissipation, Safe Operating Area	See Curves
Differential Input Voltage	±30V
Input Voltage	±13V (Note 1)
Peak Output Current	See Figs. 9 & 13 (Note 2)
Output Short Circuit Duration (to ground)	Continuous (Note 2)
Operating Temperature Range	M -55°C → +125°C
	I -25°C → +85°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C
Max Case Temperature	150°C

Note 1: Rating applies to supply voltage > ±18.

Note 2: Rating applies as long as maximum junction temperature is not exceeded (200°C). See important note on power dissipation, page 3.

ELECTRICAL SPECIFICATIONS @ T_A = +25°C (unless stated otherwise)

Description	Conditions	V_{CC}= ±30V		V_{CC}= ±30V		V_{CC}= ±30V	
		ICH8530I	ICH8530M	ICH8520I	ICH8520M	ICH8510I	ICH8510M
Max. Input Offset Change/Watt of Pdiss.	Part Mtd. on Wakefield 403 Heat Sink	4mv/watt	2mv/watt	4mv/watt	2mv/watt	4mv/watt	2mv/watt
Maximum Input Offset Voltage	$R_S \leq 10K\Omega$, Pdiss. < 1 watt	±6mv	±3mv	±6mv	±3mv	±6mv	±3mv
Maximum Input Offset Current	$R_S \leq 10K\Omega$, Pdiss. < 1 watt	200na	100na	200na	100na	200na	100na
Maximum Input Bias Current	$R_S \leq 10K\Omega$, Pdiss. < 1 watt	500na	250na	500na	250na	500na	250na
Minimum Large Signal Voltage Gain	R_L=20Ω, f=10HZ $V_{OUT} \geq 67\%$ V_{CC}	100dB	100dB	100dB	100dB	100dB	100dB
Minimum Input Voltage Range		±10v	±10v	±10v	±10v	±10v	±10v
Minimum CMRR	R_S=10KΩ, f=10HZ	70dB	70dB	70dB	70dB	70dB	70dB
Minimum PSRR	R_S=10KΩ, f=10HZ	77dB	77dB	77dB	77dB	77dB	77dB
Minimum Slew Rate	C_L=30Pf, A_V=1 R_L=20Ω, $V_{OUT} \geq 67\%$ V_{CC}	0.5v/μs	0.5v/μs	0.5v/μs	0.5v/μs	0.5v/μs	0.5v/μs
Minimum Output Voltage Swing (V_{SW})	R_L=20Ω, A_V= +10 f=1KC	±25v	±25v	±26v	±26v	(R_L = 30Ω) ±26v	(R_L = 30Ω) ±26v
Minimum Output Current Capability(I_{MAX})	$V_{OUT} \geq 24v$ Note 3	2.7 amps	2.7 amps	2 amps	2 amps	1 amp	1 amp
Max. ±V_{CC} Power Supply Quiescent Current	R_L=∞, V_{IN}=Ov	50ma	40ma	50ma	40ma	50ma	40ma

Note 3: Output current and V_{SWING} are reduced as power supplies are lowered. See Figures 1, 2, &9.

ELECTRICAL SPECIFICATIONS @ T_A = -55°C→+125°C(M) or T_A = -25°C→+85°C(I)

Maximum Input Offset Voltage	Pdiss < 1 watt	±10mv	±9mv	±10mv	±9mv	±10mv	±9mv
Maximum Input Bias Current	Pdiss < 1 watt	1.5μa	750na	1.5μa	750na	1.5μa	750na
Maximum Input Offset Current		500na	200na	500na	200na	500na	200na
Minimum Large Signal Voltage Gain	R_L=20Ω, V_{OUT}=67% V_{CC} f=10HZ; with heat sink	90dB	90dB	90dB	90dB	90dB	90dB
Minimum Output Voltage Swing	R_L = 20Ω, Pkg. Mtd. on Wakefield 403 Heat Sink	±24v	±24v	±24v	±24v	±24v	±24v
Maximum Thermal Resistance Junction to Ambient	Without Heat Sink	40°C/watt	40°C/watt	40°C/watt	40°C/watt	40°C/watt	40°C/watt
Maximum Thermal Resistance Junction to Case		2.5° C/watt	2.5° C/watt	2.5° C/watt	2.5° C/watt	3.0° C/watt	3.0° C/watt
Typical Thermal Resistance Junction to Ambient	Pkg. Mtd. on Wakefield 403 Heat Sink	4.0° C/watt	4.0° C/watt	4.0° C/watt	4.0° C/watt	4.5° C/watt	4.5° C/watt
±V_{CC} Range (typical)		±18V to ±30V	±18Vto ±30V	±18Vto ±30V	±18Vto ±30V	±18V to ±30V	±18Vto ±30V

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How To Set The Externally Programmable, Current Limiting Resistors:

The maximum output current is set by the addition of two external resistors—R+s.c. and R-s.c. Because of the INTERNAL POWER LIMITING CIRCUITRY, the maximum output current is only available when Vout is close to either power supply. As Vout moves away from ±Vcc, the maximum output current decreases in proportion to output voltage. The curve below shows maximum output current versus output voltage.

FIGURE 1 Maximum Output Current for Given Rs.c.

In general, for a given V_{OUT}, Isc limit, and case temperature T_C, Rs.c. can be calculated from the equation below (V_{OUT} in Volts):

$$R_{s.c.} = \frac{[600 + (24 \times V_{OUT}) - 2.2\,(T_C - 25°\,C)]\ \text{mV}}{I_{sc}\ \text{limit}}$$

i.e., If Iout (maximum) = 1.5 amps @ Vout = 25V, $T_C = 25°C$

$$R_{s.c.} = \frac{1200\ \text{mV}}{1.5\ \text{amps}} = 0.8\Omega$$

When an Rs.c. = 0.8Ω is used, Iout @ Vout = OV will be reduced to 750 mA. Except for small changes in the "Vsw Limit" area, the effects of changing Rs.c. on the I_{OUT} vs V_{OUT} characteristics can be determined by merely changing the I_{OUT} scale on Fig. 1 to correspond to the new value. Changes in T_C move the limit curve bodily up and down.

This INTERNAL POWER LIMITING CIRCUITRY however does not at all restrict the normal use of the driver. For any normal load, the static load line will be similar to that shown in Figure 1. Clearly, as V_{OUT} decreases, the I_{OUT} requirement falls also, more steeply than the I_{OUT} available. For reactive loads, the dynamic load lines are more complex. Two typical operating point loci are sketched here:

Capacitive Load

Inductive Load
(Note catch diode)

Thus the limiting circuitry protects the load and avoids needless damage to the driver during abnormal conditions. For any 24Vdc-28Vdc motor/actuator, the Rs.c. resistors must be calculated to get proper power delivered to the motor (up to a maximum of 2.7 amps) and ±Vcc set at ±30V. For lower supply and/or output voltages, the maximum output current will follow graphs of Figures 1 and 10.

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IMPORTANT NOTE ON POWER DISSIPATION OF POWER AMPLIFIER

The steady state power dissipation equation is:

$$P_{diss\ max} = \frac{T_{JMAX} - T_{AMB}}{\Theta_{JC} + \Theta_{CH} + \Theta_{HA}}$$

Where:

T_{JMAX} = Maximum junction temperature
T_{AMB} = Ambient temperature
Θ_{JC} = Thermal resistance from transistor junction to case of package
Θ_{CH} = Thermal resistance from case to heat sink
Θ_{HA} = Thermal resistance from heat sink to ambient air

Now:

T_{JMAX} = 200° C for silicon transistors
Θ_{JC} ≅ 2.0 C/WATT for a steel bottom TO-3 package with die attachment to beryllia substrate to header
Θ_{CH} = .045° C/W for 1mil thickness of Wakefield type 120 thermal joint compound.
.09° C/W for 2mil thickness of type 120
.13° C/W for 3mil thickness of type 120
.17° C/W for 4mil thickness of type 120
.21° C/W for 5mil thickness of type 120
.24° C/W for 6mil thickness of type 120

Θ_{HA} The choice of heat sink that a user selects depends upon the amount of room available to mount the heat sink. A sample calculation follows: by choosing a Wakefield 403 heat sink, with free air, natural convection (no fan). Θ_{HA} ≅ 2.0° C/W. Using 4 mil joint compound,

$$\therefore P_{diss\ MAX} = \frac{200°\,C - T_{AMB}}{2.0°\ C/W + .17°\,C/W + 2.0°\,C/W}$$

$$= \frac{200°\,C - T_{AMB}}{4.17°\ C/W}$$

$$\therefore P_{diss\ MAX} \text{ at } T_{AMB} = 25°\,C = \frac{200°\,C - 25°\,C}{4.17°\ C/W} = 42 \text{ watts}$$

$$P_{diss\ MAX} \text{ at } T_{AMB} = 125°\,C \text{ is } \frac{200°\,C - 125°\,C}{4.17°\ C/W} = 18 \text{ watts}$$

From Fig. 2 the worst case steady state power dissipation for an IH8520 (R_{SC} = 0.6Ω) are about 30 W and 18 W respectively. Thus this heat sink is adequate. The IH8530 (R_{SC} = 0.4Ω) would need a bigger heat sink (or a blower) giving about 1° C/W for Θ_{CA} to maintain satisfactory junction and case temperatures with 25 W dissipation and T_{AMB} = 125° C.

TYPICAL PERFORMANCE CURVES

Figure 2: Safe Operating Area; I_{OUT} vs V_{OUT} vs T_C

Figure 3: Input Offset Voltage vs Power Dissipation

Figure 4: Input Impedance vs Gain vs Frequency

Figure 5: Quiescent Current vs Power Supply Voltage

TYPICAL PERFORMANCE CURVES, CONTINUED.

Figure 6: Large Signal Power Band Width

Figure 7: Small Signal Frequency Response

Figure 8: Maximum Output Current vs. Case Temperature

Figure 9: Maximum Output Current and Voltage vs. V_{CC}

BRIEF APPLICATION NOTES

The maximum input voltage range, for $\pm V_{CC} > \pm 18V$, is substantially less than the available output voltage swing. Thus non-inverting amplifiers, as in Figure 11, should always be set up with a gain greater than about 2.5, (with ±30V V_{CC}), so that the full output swing is available without hazard to the input. At first sight, it would seem that no restrictions would apply to inverting amplifiers, since the inputs are virtual ground and ground. However, under fault (output short-circuited) or high slew conditions, the input can be substantially removed from ground. Thus for inverting amplifiers with gains less than about 5, some protection should be provided at this input. A suitable resistor from the input to ground will provide protection, but also increases the effect of input offset voltage at the output. A pair of diodes, as shown in Figure 12, has no effect on normal operation, but gives excellent protection.

Figure 10: Non-Inverting Amplifier

Figure 11: Inverting Amplifier

Power dissipation is another important parameter to consider. The current protection circuit protects the device against short circuits to ground, (but only for transients to the opposite supply) provided the device has adequate heat sink. A curve of power dissipation vs V_{OUT} under short circuit conditions is given in Figure 13. The limiting circuit is more closely dependent on case temperature than (output transistor) junction temperatures. Although these operating conditions are unlikely to be attained in actual use, they do represent the limiting case a heat sink must cope with. For fully safe design, the anticipated range of V_{OUT} values that could occur, (steady state, including faults) should be examined for the highest power dissipation, and the device provided with a heat sink that will keep the junction temperature below 200° C and the case temperature below 150° C with the worst case ambient temperature expected.

Figure 12: Power Dissipation under Short Circuit Conditions

TYPICAL APPLICATIONS

I. Actuator Driving Circuit (24→28Vd.c. rated)

Figure 13: Power Amp Driving Actuator

The gain of the circuit is set to +10, so a +2.4V input Vin will produce a +24V output (and will deliver up to 2.7 amps output current). To reverse the piston travel, invert Vin to −2.4V and Vout will go to −24V. Diodes D1 and D2 absorb the inductive kick of the motor during transients (turn-on or turn-off); their breakdown should exceed 60V.

II. Obtaining Up To 5 Amps Output Current Capability By Paralleling Amplifiers

Figure 14: Paralleling Power Amps for Increased Current Capability

This paralleling procedure can be repeated to get any desired output current. However, care must be taken to ensure that enough load is provided to avoid the amplifiers pulling against each other.

5

III. Driving A 48VDC Motor

Figure 15: Power Amp Driving 48 VDC Motor

IV. Precise Rate Control of an Electronic Valve

To get very fine control of the opening of an orifice, driven by an electronic valve, there are two ways to go.

1. Keep the voltage constant, i.e., 24Vdc or 12Vdc, and vary the time the voltage is applied, i.e., if it takes five seconds to completely open an orifice at 24Vdc, then applying 24V for only 2-1/2 seconds opens it only 50%.
2. Simply vary the d.c. driving voltage to valve. Most valves obtain full opening as an inverse of applied voltage., i.e., valves opens 100% in five seconds at 24Vdc and in 10 seconds at 12Vdc.

A circuit to perform the second method is shown below; the advantage of this is that digit switches can precisely set driving voltage to 0.2% accuracy (8-bit DAC), thereby controlling the rate at which the valve opens.

Figure 16: Digitally Controlled Electronic Value

V. The circuit presented in IV is also an excellent way to get a precise power supply voltage; in fact, a precision, variable power supply can be made. Using a BCD coded DAC with BCD Thumbwheel switches.

Figure 17: Digitally Programmable Power Supply

2^0	2^1	2^2	2^3	2^4	2^5	2^6	2^7	Ø BIT	Vout
1	1	1	1	1	1	1	1	1	+25Vd.c.
1	1	1	1	1	1	1	1	0	-25Vd.c.
0	1	0	1	1	0	0	1	1	+15Vd.c.
0	1	0	1	1	0	0	1	0	-15Vd.c.
1	0	0	0	0	0	0	0	1	+0.098Vd.c.
1	0	0	0	0	0	0	0	0	-0.098Vd.c.

Etc.

The power supply can be set to ±0.1Vd.c.

VI. There is great power available (no pun intended) in the sub-systems shown in IV and V; there the D/A converter is shown being set manually (via digit switches) to get a precise analog output (binary # × full scale voltage), then the driver amplifier multiplies this voltage to produce the final output voltage. It seems obvious that the next logical step is to let a microprocessor (local) or C.P.U. program the D/A converter. Then total, pre-programmable, electronic control of an actuator, electronic valve, motor, etc., is obtained. This would be used in conjunction with a transducer/multiplex system for electronic monitoring and control of any electro-mechanical function.

ELECTRONIC CONTROL SYSTEM:

MUX = INTERSIL IH5060 (1/16) or IH5070 (2/16)
S/H(SAMPLE & HOLD) = INTERSIL IH5111
D/A CONVERTER = INTERSIL 7520 or INTERSIL 7105
POWER AMP = IH8510 (1 AMP) or IH8520 (2 AMP) or IH8530 (2.7 AMP)
A/D CONVERTER = ICL8052/7103 or ICL8052/7104
μ COMPUTER = IM6100 family:

FOR OTHER APPLICATIONS etc. see
1) Intersil Applications Bulletin A021 "Power D/A Converters using the IH8510" by Dick Wilenken

HEAT SINK INFORMATION

Heat sinks are available from Intersil. Order part number 29-0305 ($10.00 ea.) with a Θ S/A = 1.3°C/watt. A convenient mating connector is also available. Order part number 29-0306 ($4.50 ea.).

NOTE. This product contains Beryllia. If used in an application where the package integrity may be breached and the internal parts crushed or machined, avoid inhalation of the dust.

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ICL7605/ICL7606

Commutating Auto-Zero (CAZ) Instrumentation Amplifier

FEATURES

- Exceptionally low input offset voltage — 2μV
- Low long term input offset voltage drift — 0.2μV/year
- Low input offset voltage temperature drift — 0.05μV/°C
- Wide common mode input voltage range — 0.3V above supply rail
- High common mode rejection ratio — 100 dB
- Excellent low supply voltage — Down to ±2V
- Short circuit protection on outputs for ±5V operation
- Static-protected inputs — no special handling required
- Fabricated using proprietary MAXCMOS™ process technology
- Compensated (ICL7605) or uncompensated (ICL7606) versions

SYMBOL

GENERAL DESCRIPTION

The ICL7605/ICL7606 commutating auto-zero (CAZ) instrumentation amplifiers are designed to replace almost any of today's expensive hybrid or monolithic instrumentation amplifiers for low frequency applications from DC to 10 Hz. This is made possible by the unique construction of this new Intersil device, which takes an entirely new design approach to low frequency amplifiers.

Unlike conventional amplifier designs which employ three op amps and require ultra-high accuracy in resistor tracking and matching, the CAZ instrumentation amplifier requires no trimming except for gain. The key feature of the CAZ principle involves automatic compensation for long term drift phenomena and temperature effects.

The ICL7605/ICL7606 is a monolithic CMOS chip which consists of two analog sections — a unity gain differential to single-ended voltage converter and a CAZ op amp. The first section serves to insure that at all times the differential input source is being sensed and applied to the CAZ amp section. The CAZ instrumentation amp section consists of an operational amplifier circuit which continuously corrects itself for input voltage errors, such as input offset voltage, temperature effects, and long term drift.

The ICL7605/ICL7606 is intended for low-frequency operation in applications such as strain gauges, which require voltage gains from 1 to 1000 and bandwidths from DC to 10 Hz. Since the CAZ amp automatically corrects itself for internal errors, the only periodic adjustment required is that of gain, which is established by two external resistors. The no-adjustment feature, combined with extremely low offset and temperature coefficient figures, makes the CAZ instrumentation amplifier very desirable for operation in severe environments (temperature, humidity, toxicity, radiation, etc.) where equipment service is difficult.

PIN CONFIGURATION

ORDERING INFORMATION

Order parts by the following part numbers:

Compensated	Uncompensated	Package	Temperature Range
ICL7605CJN	ICL7606CJN	CERDIP	0°C to +70°C
ICL7605IJN	ICL7606IJN	CERDIP	−25°C to +85°C
ICL7605MJN	ICL7606MJN	CERDIP	−55°C to +125°C

Order die by the following part numbers:

ICL7605/D
ICL7606/D

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (sum of both positive and negative supply voltages, V^+ and V^-) ..... 18 Volts
Positive Supply Voltage (GND to V^+) ..... 18 Volts
Negative Supply Voltage (GND to V^-) ..... 18 Volts
DR Input Voltage ..... (V^+ +0.3) to (V^+ −8) Volts
Input Voltage (C_1, C_2, +INPUT, −INPUT, BIAS, OSC (Note 2)) ..... (V^+ +0.3) to (V^- −0.3) Volts
Differential Input Voltage (Note 3) . ±(V^+ +0.3) to (V^- −0.3) Volts
Duration of Output Short Circuit (Note 4) ..... Unlimited
Continuous Total Power Dissipation at or below +25°C free air temperature (Note 5)
CERDIP Package ..... 500 mW
Plastic Package ..... 375 mW

Operating Temperature Range (ICL7600/ICL7601/MJD) ..... −55°C to +125°C
Operating Temperature Range (ICL7600/ICL7601/IJD) ..... −25°C to +85°C
Operating Temperature Range (ICL7600/ICL7601/CPD) ..... 0 to +70°C
Storage Temperature Range ..... −55 to +150°C
Lead Temperature (soldering, 60 seconds) ..... +300°C

Note 1: Stresses above those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent device failures. These are stress ratings only and functional operation of devices under conditions other than those indicated in the Table of Electrical Characteristics is not recommended. Exposure to absolute maximum rating conditions for extended periods of time can cause device failures.

Note 2: An SCR structure is inherent in the CMOS process used in the fabrication of these devices. If voltages in excess of (V^+ +0.3) to (V^- −0.3) volts are connected to either inputs or outputs, destructive latchup can occur. For this reason it is recommended that no inputs from sources not on the same power supply or supplies be applied before the ICL7600/ICL7601 supplies are established, and that if multiple supplies are used the ICL7600/ICL7601 supplies be activated first.

Note 3: No restrictions are placed on the differential input voltages on either the inverting or non-inverting inputs, so long as these voltages do not exceed the power supply voltages by more than 0.3V.

Note 4: Outputs may be shorted to ground (GND) or to either supply (V^+, V^-). Temperature and/or supply voltages must be limited to insure that the dissipation rating is not exceeded.

Note 5: For operation above 25°C free-air temperature, derate 4mW/°C from 500mW for CERDIP and 3mW/°C from 375mW for plastic above 25°C.

BLOCK DIAGRAM

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OPERATING CHARACTERISTICS

Test Conditions: $V^+ = +5$ volts, $V^- = -5$ volts, $T_A = +25°C$, DR pin connected to V^+ ($f_{COM} \cong 160Hz$, $f_{COM1} \cong 80Hz$), $C_1 = C_2 = C_3 = C_4 = 1\mu F$, Test Circuit 1 unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS		VALUE MIN	VALUE TYP	VALUE MAX	UNIT
Input Offset Voltage	V_{OS}	$R_S \leq 1k\Omega$	Low Bias Setting		±2		μV
			Med Bias Setting		±2	±5	μV
			High Bias Setting		±7		μV
		MIL version over temp.	Med Bias Setting			±20	μV
Average Input Offset Voltage Temperature Coefficient	TCV_{OS}	Low or Med Bias Settings	$-55°C > T_A > +25°C$		0.01	0.1	μV/°C
			$+25°C > T_A > +85°C$		0.01	0.1	μV/°C
			$+25°C > T_A > +125°C$		0.05	0.15	μV/°C
Long Term Input Offset Voltage Stability	$V_{OS/Time}$	Low or Med Bias Settings			0.5		μV/Year
Common Mode Input Range	CMVR			-5.3		+5.3	V
Common Mode Rejection Ratio	CMRR	$C_{OSC} = 0$, DR connected to V^+, $C_3 = C_4 = 1\mu F$			94		dB
		$C_{OSC} = 1\mu F$, DR connected to GND, $C_3 = C_4 = 1\mu F$			100		dB
		$C_{OSC} = 1\mu F$, DR connected to GND, $C_3 = C_4 = 10\mu F$			104		dB
Power Supply Rejection Ratio	PSRR				110		dB
-INPUT Bias Current	I_{NTB}	Any bias setting, $f_C = 160Hz$ (Includes charge injection currents)			0.15	1.5	nA
Equivalent Input Noise Voltage peak-to-peak	e_{np-p}	Band Width 0.1 to 10Hz	Low Bias Mode		4.0		μV
			Med Bias Mode		4.0		μV
			High Bias Mode		5.0		μV
Equivalent Input Noise Voltage	$\bar{e}_{np-p}$	Band Width 0.1 to 1.0Hz	All Bias Modes		1.7		μV
Voltage Gain	A_V	$R_L = 100k\Omega$	Low Bias Setting	90	105		dB
			Med Bias Setting	90	105		dB
			High Bias Setting	80	100		dB
Maximum Output Voltage Swing	V_{OUT}	$R_L = 1M\Omega$			±4.9		V
		$R_L = 100k\Omega$			±4.8		V
		$R_L = 10k\Omega$	Positive Swing	+4.4			V
			Negative Swing			-4.5	V
Band Width of Input Voltage Translator	GBW	$C_3 = C_4 = 1\mu F$	All Bias Modes		10		Hz
Nominal Commutation Frequency	f_{COM}	$C_{OSC} = 0pF$	DR Connected to V^+		160		Hz
			DR Connected to GND		2560		Hz
Nominal Input Converter Commutation Frequency	f_{COM1}	$C_{OSC} = 0pF$	DR Connected to V^+		80		Hz
			DR Connected to GND		1280		Hz
Bias Voltage to define Current Modes	V_{BA}	Low Bias Setting		$V^+-0.3$		$V^++0.3$	V
	V_{BM}	Med Bias Setting		$V^-+1.4$		$V^+-1.4$	V
	V_{BL}	High Bias Setting		$V^--0.3$		$V^-+0.3$	V
Bias (Pin 8) Input Current	I_{BIAS}				±30		pA
Division Ratio Input Current	I_{DR}	$V^+-8.0 \leq V_{DR} \leq V^++0.3$ volt			±30		pA
DR Voltage to define Oscillator division ratio	V_{DRH}	Internal oscillator division ratio 32		$V^+-0.3$		$V^++0.3$	V
	V_{DRL}	Internal oscillator division ratio 2		V^+-8		$V^+-1.4$	V
Effective Impedance of Voltage Translator Analog Switches	R_{AS}				30		kΩ
Supply Current	I_S	High Bias Setting		4	7	15	mA
		Med Bias Setting		0.6	1.7	5	mA
		Low Bias Setting		0.25	0.6	1.5	mA
Operating Supply Voltage Range	V^+-V^-	High Bias Setting		5		10	V
		Med or Low Bias Setting		4		10	V

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INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGES

INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C_1, C_2 = 1μF)

INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C_1, C_2 = 0.1 μF)

INPUT OFFSET VOLTAGE AND PK-TO-PK NOISE AS A FUNCTION OF SUPPLY VOLTAGE (V^+-V^-)

COMMON MODE REJECTION RATIO AS A FUNCTION OF THE INPUT DIFFERENTIAL TO SINGLE ENDED VOLTAGE CONVERTER CAPACITORS

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INPUT CURRENT AS A FUNCTION OF COMMUTATION FREQUENCY

MAXIMUM OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT LOAD RESISTANCE

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

OSCILLATOR FREQUENCY AS A FUNCTION OF EXTERNAL CAPACITIVE LOADING

AMPLITUDE RESPONSE OF THE INPUT DIFFERENTIAL TO SINGLE ENDED VOLTAGE CONVERTER

FREQUENCY RESPONSE OF THE 10 Hz LOW PASS FILTER USED TO MEASURE NOISE (TEST CIRCUIT 2).

TEST CIRCUIT 1: USE TO MEASURE:

a) INPUT OFFSET VOLTAGE $\left(\frac{V_{OUT}}{1000}\right)$

b) INPUT EQUIV NOISE VOLTAGE

c) SUPPLY CURRENT

d) CMRR

e) PSRR

TEST CIRCUIT 2: DC to 10Hz (1Hz) Unity Gain Low Pass Filter

DETAILED DESCRIPTION

CAZ Instrumentation Amp Overview

The CAZ instrumentation amplifier operates on principles which are very different from those of the conventional three op amp designs, which must use ultra-precise trimmed resistor networks in order to achieve acceptable accuracy. An important advantage of the ICL7605/ICL7606 CAZ instrumentation amp is the provision for self-compensation for internal error voltages, whether they are derived from steady-state conditions, temperature, supply voltage fluctuations, or are variable over a long term.

The CAZ instrumentation amplifier is constructed with monolithic CMOS technology, and consists of three distinct sections, two analog and one digital. The two analog sections — a differential to single-ended voltage converter, and a CAZ op amp — have on-chip analog switches to steer the input signal. The analog switches are driven from a self-contained digital section which consists of an RC oscillator, a programmable divider, and associated voltage translators. A functional layout of the ICL7605/ICL7606 is shown in Figure 1.

Figure 1: Simplified Block Diagram

The ICL7605/ICL7606 have approximately constant input equivalent noise voltage, CMRR, PSRR, input offset voltage and drift values independent of the gain configuration. By comparison, hybrid-type modules which use the traditional three op amp configuration have relatively poor performance at low gain (1 to 100) with improved performance above a gain of 100.

The only major limitation of the ICL7605/ICL7606 is its low-frequency operation (10 to 20 Hz maximum). However in many applications speed is not the most important parameter.

CAZ Op Amp Section

Operation of the CAZ amp section of the ICL7605/ICL7606 instrumentation amplifier is best illustrated by referring to Figure 2. The basic amplifier configuration, represented by the large triangles, has one more input than does a regular op amp — the AZ, or auto-zero terminal. The voltage on the AZ input is that level to which each of the internal op amps are to be auto-zeroed. In Mode A, op amp #2 is connected into a unity gain mode through on-chip analog switches, and charges external capacitor C_2 to a voltage equal to the DC input offset voltage of the amplifier, in addition to the instantaneous low-frequency noise voltage. A short time later, the analog switches reconnect the on-chip op amps to the configuration shown in Mode B. In this mode, op amp #2 has capacitor C_2 (which is charged to a voltage equal to the offset and noise voltage of op amp #2) connected in series to its non-inverting (+) input in such a manner as to null out the input offset and noise voltages of the amplifier. While one of the on-chip op amps is processing the input signal, the second op amp is in an auto-zero mode, and charges a capacitor to a voltage equal to its equivalent DC and low frequency error voltage. The on-chip amplifiers are connected and reconnected at a rate designated as the commutation frequency (f_{COM}) so that at all times one or the other of the on-chip op amps is processing the input signal while the voltages on capacitors C_1 and C_2 are being updated regularly to compensate for variables such as low frequency noise voltage and input offset voltage changes due to temperature, drift or supply voltages effects.

Compared to the standard bipolar or FET input op amps, the CAZ amp scheme demonstrates a number of important advantages:

* Effective input offset voltages can be reduced from 1000 to 10,000 times without trimming.
* Long-term offset voltage drift phenomena can be compensated and dramatically reduced.
* Thermal effects can be compensated for over a wide operating temperature range. Reductions can be as much as 100 times or better.
* Supply voltage sensitivity is reduced.

CMOS processing is ideally suited to implement the CAZ amp structure. The digital section is easily fabricated, and

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Figure 2: Diagrammatic representation of the 2 half cycles of operation of the CAZ OP AMP.

Figure 3: Schematic of analog switches connecting each internal OP AMP to the external inputs at the output.

the transmission gates (analog switches) which connect the on-chip op amps can be constructed for minimum charge injection and the widest operating voltage range. The analog section, which includes the on-chip op amps, contributes performance figures which are similar to bipolar or FET input designs. CMOS structure provides the CAZ amp concept with open-loop gains of greater than 100 dB, typical input offset voltages of ±5 mV, and ultra-low output leakage currents, typically 1 pA.

The CMOS transmission gates connect the on-chip op amps to external input and output terminals, as shown in Figure 3. Here, one op amp and its associated analog switches are required to connect each on-chip op amp so that at any time three switches are open and three switches are closed. Each analog switch consists of a P-channel transistor in parallel with an N-channel transistor.

DIFFERENTIAL-TO-SINGLE-ENDED UNITY GAIN VOLTAGE CONVERTER

An idealized schematic of a voltage converter block is shown in Figure 4. The mode of operation is quite simple, involving two capacitors and eight switches. The switches are arranged so that four are open and four are closed. The four conducting switches connect one of the capacitors across the differential input and the other from a ground or reference voltage to the input of the CAZ instrumentation amp. The output signal of this configuration is shown in Figure 5, where the voltage steps equal the differential voltage (V_A-V_B) at commutation times a, b, c, etc. The output waveform thus represents all information contained in the input signal from DC up to the commutation frequency, commutation and noise voltages are added. Sampling theory states that to preserve the integrity of the information to be processed, at least two samples must be taken within a period (1/f) of the highest frequency of the signal being

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MODE	S_1	S_2	S_3	S_4	S_5	S_6	S_7	S_8
A	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN
B	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED	OPEN	CLOSED

The note at which the modes A & B are cycled through is known as the INPUT COMMUTATION FREQUENCY

Figure 4: Schematic of the differential to single ended voltage converter

Figure 5: Input to Output Voltage waveforms from the differential to single ended voltage converter. For additional information, see frequency characteristics in Amplitude Response of the Input Differential to single ended voltage converter graph on page 5.

sampled. Consequently this scheme preserves information up to the commutation frequency. Above the commutation frequency, the input signal is transferred to a lower frequency. This phenomenon is known as aliasing. Although the output responds above the commutation frequency, the frequencies of the output responses have been aliased down to frequencies below the commutation frequency.

The example shown in Figure 4 for the voltage converter is fabricated with CMOS analog switches, which contain a parallel combination of P-channel and N-channel transistors. The switches have finite ON impedances of 30kΩ, plus parasitic capacitances to the substrate. Because of the charge injection effects which appear at both the switches and the output of the voltage converter, the values of capacitors C_0 and C_O must be about 1μF to preserve signal translation accuracies to 0.01%. The 1μF capacitors, coupled with the 30kΩ equivalent impedance of the switches, produce a low-pass filter response from the voltage converter which is approximately 3 dB at 10 Hz.

APPLICATIONS

USING THE ICL7605/ICL7606 TO BUILD A DIGITAL READOUT TORQUE WRENCH

A typical application for the ICL7605/ICL7606 is in a strain gauge system, such as the digital readout torque wrench circuit shown in Figure 6. In this application, the CAZ intrumentation amplifier is used as a preamplifier, taking the differential voltage of the bridge and converting this voltage to a single-ended voltage reference to ground. The signal is then amplifier by the CAZ instrumentation amplifier and applied to the input of a 3-1/2 digit dual-slope A/D converter chip for LCD panel meter display. The A/D converter device used in this instance is the Intersil ICL7106.

In the digital readout torque wrench circuit, the internal reference voltage of the ICL7106 is used instead of the conventional external reference source. In order to set the full-scale reading, it is required that, given a certain strain gauge bridge with a defined pressure voltage sensitivity, a value of gain for the ICL7605/ICL7606 instrumentation CAZ amp be selected along with an appropriate value for the reference voltage. The gain should be set so that at full scale the output will swing about 0.5V. The reference voltage required is about one-half the maximum output swing, or approximately 0.25V.

In this type of system, only one adjustment is required. Either the amplifier gain or the reference voltage must be varied for full-scale adjustment. Note that the common to V^+ voltage of the CAZ amp is about 2.8V. This voltage must therefore be divided by about 10 to provide the 0.25V reference voltage. Total current consumption of all circuitry, less the current through the strain gauge bridge, is typically 2 mA.

Figure 6: 3-1/2 Digit Digital Readout Torque Wrench

SOME HELPFUL HINTS

Testing the ICL7605/ICL7606 CAZ Instrumentation Amplifier

Test Circuits #1 and #2 provide convenient means of measuring most of the important electrical parameters of the CAZ instrumentation amp. The output signal can be viewed on an oscilloscope after being fed through a low-pass filter. It is recommended that for most applications, a low-pass filter of about 1.0 to 1.5 Hz be used to reduce the peak-to-peak noise to about the same level as the input offset voltage.

The output low-pass filter must be of a high-input impedance type — not a capacitor across the feedback resistor R_2 nor a low-impedance type of around 1kΩ — but rather must be rated at about 100kΩ and 1.0μF so that the output dynamic loading on the CAZ instrumentation amp is about 100kΩ.

Bias Control

The on-chip op amps consume over 90% of the power required by the ICL7605/ICL7606 instrumentation op amp. For this reason, the internal op amps have externally-programmable bias levels. These levels are set by connecting the BIAS terminal to either V^+, GND, or V^-. The difference between each bias setting is about a factor of 3, allowing a 9:1 ratio of power supply versus bias setting. This current programmability provides the user with a choice of device power dissipation levels, slew rates (the higher the slew rate, the lower the amplitude of commutation spikes) and offset errors due to "IR" voltage drops and thermoelectric temperature gradients across the chip and the higher the temperature gradients across the chip and the highe the input offset error). In most cases, the medium bias (MED BIAS) setting will be found to be the best choice.

Output Loading (Resistive)

With a 10kΩ load, the output voltage swing can vary across nearly the entire supply voltage range, and the device can be used with loads as low as 2kΩ.

However, with loads of less than 50kΩ, the on-chip op amps will begin to exhibit the characteristics of transconductance amplifiers, since their respective output impedances are nearly 50kΩ each. Thus the open-loop gain is 20 dB less with a 2kΩ load than it would be with a 20kΩ load. Therefore, for high gain configurations requiring high accuracy, an output loading of 100kΩ or less is suggested.

There is another consideration in applying the CAZ instrumentation op amps which must not be overlooked, and that is the additional power dissipation of the chip which will result from a large output voltage swing into a low resistance load. This added power dissipation can affect the initial input offset voltages under certain conditions.

Output Loading (Capacitive)

In many applications, it is desirable to include a low-pass filter at the output of the CAZ instrumentation op amp to reduce high-frequency noise outside the desired signal passband. An obvious solution when using a conventional op amp would be to place a capacitor across the external feedback resistor and thus produce a low-pass filter.

However, with the CAZ op amp concept this is not possible because of the nature of the commutation spikes. These voltage spikes exhibit a low-impedance characteristic in the direction of the auto-zero voltage and a high-impedance characteristic on the recovery edge, as shown in Figure 7. It can be seen that the effect of a large load capacitor produces an area error in the output waveform, and hence an effective gain error. The output low-pass filter must be of a high-impedance type to avoid these area errors. For example, a 1.5 Hz filter will require a 100kΩ resistor and a 1.0μF capacitor, or a 1 MΩ resistor and an 0.1μF capacitor.

Oscillator and Digital Circuitry Considerations

The oscillator has been designed to run free at about 5.2 kHz when the OSC terminal is open circuit. If the full divider network is used, this will result in a nominal commutation frequency of approximately 160 Hz. The commutation frequency is that frequency at which the on-chip op amps are switched between the signal processing and the auto-zero modes. A 160 Hz commutation frequency represents the best compromise between input offset voltage and low frequency noise. Other commutation frequencies may provide optimization of some parameters, but always at the expense of others.

The oscillator has a very high output impedance, so that a load of only a few picofarads on the OSC terminal will cause a significant shift in frequency. It is therefore recommended that if the natural oscillator frequency is desired (5.2 kHz) the terminal remains open circuit. In other instances, it may be desirable to synchronize the oscillator with an external clock source, or to run it at another frequency. The ICL7605/ICL7606 CAZ amp provides two degrees of flexibility in this respect. First, the DR (division ratio) terminal allows a choice of either dividing the oscillator by 32 (DR terminal to V^+) or by 2 (DR terminal to GND) to obtain the commutation frequency. Second, the oscillator may have its frequency lowered by the addition of an external capacitor connected between the OSC terminal and the V^+ or system GND terminals. For situations which require that the commutation frequency be synchronized with a master clock, (Figure 8) the OSC terminal may be driven from TTL logic (with resistive pull-up) or by CMOS logic, provided that the V^+ supply (with respect to ground) is +5V (±10%) and the logic driver also operates from a similar voltage supply. The

Figure 7: Effect of a load capacitor on output voltage waveforms.

Figure 8: ICL7605 being clocked from external logic into the oscillator terminal.

reason for this requirement is that the logic section (including the oscillator) operates from an internal –5V supply, referenced to V^+ support which is generated on-chip, and which is not accessible externally.

Thermoelectric Effects

The ultimate limitations to ultra-high-sensitivity DC amplifiers are due to thermoelectric, Peltier, or thermocouple effects whereby electrical junctions consist of various metals (alloys, silicon, etc.) Unless all junctions are at precisely the same temperature, small thermoelectric voltages will be produced, generally about 0.1μV/°C. However, these voltages can be several tens of microvolts per °C for certain thermocouple materials.

In order to realize the extremely low offset voltages which the CAZ op amp can produce, it is necessary to take precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement across device surfaces. Special thermoelectric solder (70% cadmium, 30% tin) should be used. In addition, the supply voltages and power dissipation should be kept to a minimum by use of the MED BIAS setting. Employ a high impedance load and keep well away from equipment which dissipates heat.

Component Selection

The two auto-zero capacitors (C_1 and C_2) should each be about 1.0μF value. These are relatively large values for non-electrolytic capacitors, but since the voltages stored on them do not change significantly, problems of dielectric absorption, charge bleed-off and the like are not as significant as they would be for integrating dual-slope A/D converter applications. Polypropylene and Mylar are the best.

Excellent results have been obtained for commercial temperature ranges using several of the less-expensive, smaller-size capacitors, since the absolute values of the capacitors is not critical. Even polarized electrolytic capacitors rated at 1.0μF and 50V have been used successfully at room temperature, although no recommendations are made concerning the use of such capacitors.

Commutation Voltage Transient Effects

Although in most respects the CAZ instrumentation amplifier resembles a conventional op amp, its principal applications will be in very low level, low-frequency preamplifiers limited to DC through 10 Hz. The is due to the finite switching transients which occur at both the input and output terminals because of commutation effects. These transients have a frequency spectrum beginning at the commutation frequency, and including all of the higher harmonics of the commutation frequency. Assuming that the commutation frequency is higher than the highest in-band frequency, then the commutation transients can be filtered out with a low-pass filter.

The input commutation transients arise when each of the on-chip op amps experiences a shift in voltage which is equal to the input offset voltages (about 5-10mV), usually occurring during the transition between the signal processing mode and the auto-zero mode. Since the input capacitances of the on-chip op amps are typically in the 10 pF range, and since it is desirable to reduce the effective input offset voltage about 10,000 times, the offset voltage auto-zero capacitors C_1 and C_2 must have values of at least 10,000 x 10 pF, or 0.1μF each.

The charge that is injected into the input of each op amp when being switched into the signal processing mode produces a rapidly-decaying voltage spike at the input, plus an equivalent DC input bias current averaged over a full cycle. This bias current is directly proportional to the commutation frequency, and in most instances will greatly exceed the inherent leakage currents of the input analog switches, which are typically 1.0 pA at an ambient temperature of 25°C.

The output waveform in Test Circuit #1 (with no input signal) is shown in Figure 9. Note that the equivalent noise voltage is amplified 1000 times, and that due to the slew rate of the on-chip op amps, the input transients of approximately 7 mV are not amplified by 1000.

Figure 9: Output waveform from Test Circuit 1.

Layout Considerations

Care should be exercised in positioning components on the PC board, particularly the capacitors C_1, C_2, C_3 and C_4, all of which must be shielded from the OSC terminal. Also, parasitic PC board leakage capacitances associated with these four capacitors should be kept as low as possible to minimize charge injection effects.

PACKAGE DIMENSIONS

INTERSIL

ICL8048, ICL8049
Monolithic Log Amplifier
Monolithic Antilog Amplifier

FEATURES
- 1/2% Full Scale Accuracy
- Temperature Compensated 0°C to 70°C
- Scale Factor 1V/Decade, Adjustable
- 120dB Dynamic Current Range (8048)
- 60dB Dynamic Voltage Range (8048 & 8049)
- Dual FET-Input Op-Amps

GENERAL DESCRIPTION
The 8048 is a monolithic logarithmic amplifier capable of handling six decades of current input, or three decades of voltage input. It is fully temperature compensated and is nominally designed to provide 1 volt of output for each decade change of input. For increased flexibility, the scale factor, reference current and offset voltage are externally adjustable.

The 8049 is the antilogarithmic counterpart of the 8048; it nominally generates one decade of output voltage for each 1-volt change at the input.

8048 SCHEMATIC DIAGRAM

CONNECTION DIAGRAM

8049 SCHEMATIC DIAGRAM

CONNECTION DIAGRAM

5

MAXIMUM RATINGS

Supply Voltage	±18 V	Operating Temperature Range	0°C to +70°C
I_{in} (Input Current)	2 mA	Output Short Circuit Duration	Indefinite
I_{ref} (Reference Current)	2 mA	Storage Temperature Range	–65°C to +125°C
Voltage between Offset Null and V^+	±0.5 V	Lead Temperature (Soldering, 60 sec.)	300°C
Power Dissipation	750 mW		

ELECTRICAL CHARACTERISTIC (Note 1)

PARAMETER	CONDITION	8048BC MIN.	8048BC TYP.	8048BC MAX.	8048CC MIN.	8048CC TYP.	8048CC MAX.	UNITS
Dynamic Range								
I_{in} (1 nA–1 mA)		120			120			dB
V_{in} (10 mV–10 V)	R_{IN} = 10 kΩ	60			60			dB
Error, % of Full Scale	T_A = 25°C, I_{IN} = 1 nA to 1 mA		.20	0.5		.25	1.0	%
Error, % of Full Scale	T_A = 0°C to +70°C, I_{IN} = 1 nA to 1 mA		.60	1.25		.80	2.5	%
Error, Absolute Value	T_A = 25°C, I_{IN} = 1 nA to 1 mA		12	30		14	60	mV
Error, Absolute Value	T_A = 0°C to +70°C, I_{IN} = 1 nA to 1 mA		36	75		50	150	mV
Temperature Coefficient of V_{OUT}	I_{IN} = 1 nA to 1 mA		0.8			0.8		mV/°C
Power Supply Rejection Ratio	Referred to Output		2.5			2.5		mV/V
Offset Voltage (A_1 & A_2)	Before Nulling		15	25		15	50	mV
Wideband Noise	At Output, for I_{IN} = 100 μA		250			250		μV (RMS)
Output Voltage Swing	R_L = 10 kΩ	±12	±14		±12	±14		V
	R_L = 2 kΩ	±10	±13		±10	±13		V
Power Consumption			150	200		150	200	mW
Supply Current			5	6.7		5	6.7	mA

NOTE 1: Unless otherwise noted, specifications apply for V_S = ±15V, T_A = 25°C, I_{REF} = 1mA, scale factor adjusted for 1 V/decade. Accuracy specifications assume that offset voltages and scale factor have been adjusted using the procedure outlined on page 3.

TRANSFER FUNCTION FOR CURRENT INPUTS

TRANSFER FUNCTION FOR VOLTAGE INPUTS

SMALL SIGNAL BANDWIDTH AS A FUNCTION OF INPUT CURRENT

MAXIMUM ERROR VOLTAGE AT THE OUTPUT AS A FUNCTION OF INPUT CURRENT

MAXIMUM ERROR VOLTAGE AT THE OUTPUT AS A FUNCTION OF INPUT VOLTAGE

SMALL SIGNAL VOLTAGE GAIN AS A FUNCTION OF INPUT VOLTAGE FOR R_S = 10 kΩ

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THEORY OF OPERATION

The 8048 relies for its operation on the well-known exponential relationship between the collector current and the base-emitter voltage of a transistor:

$$I_C = I_S\left[e^{qV_{BE}/kT} - 1\right] \quad (1)$$

For base-emitter voltages greater than 100mV, Eq. (1) becomes

$$I_C = I_S\, e^{qV_{BE}/kT} \quad (2)$$

From Eq. (2), it can be shown that for two identical transistors operating at different collector currents, the V_{BE} difference (ΔV_{BE}) is given by:

$$\Delta V_{BE} = -2.303 \times \frac{kT}{q} \log_{10}\left[I_{C1}/I_{C2}\right] \quad (3)$$

Referring to Fig. 1, it is clear that the potential at the collector of Q_2 is equal to the ΔV_{BE} between Q_1 and Q_2. The output voltage is ΔV_{BE} multiplied by the gain of A_2:

$$V_{OUT} = -2.303\left(\frac{R_1\, R_2}{R_2}\right)\left(\frac{kT}{q}\right) \log_{10}\left[I_{IN}/I_{REF}\right] \quad (4)$$

The expression $2.303 \times \frac{kT}{q}$ has a numerical value of 59mV at 25°C; thus in order to generate 1 volt/decade at the output, the ratio $(R_1 + R_2)/R_2$ is chosen to be 16.9. For this scale factor to hold constant as a function of temperature, the $(R_1 + R_2)/R_2$ term must have a 1/T characteristic to compensate for kT/q.

In the 8048 this is achieved by making R_1 a thin film resistor, deposited on the monolithic chip. It has a nominal value of 15.9kΩ at 25°C, and its temperature coefficient is carefully designed to provide the necessary compensation. Resistor R_2 is external and should be a low T.C. type; it should have a nominal value of 1kΩ to provide 1 volt/decade, and must have an adjustment range of ±20% to allow for production variations in the absolute value of R_1.

OFFSET AND SCALE FACTOR ADJUSTMENT

A log amp, unlike an op-amp, cannot be offset adjusted by simply grounding the input. This is because the log of zero approaches minus infinity; reducing the input current to zero starves Q_1 of collector current and open the feedback loop around A_1. Instead, it is necessary to zero the offset voltage of A_1 and A_2 separately, and then to adjust the scale factor. Referring to Fig. 1, this is done as follows:

1) Temporarily connect a 10kΩ resistor (R_0) between pins 2 and 7. With no input voltage, adjust R_4 until the output of A_1 (pin 7) is zero. Remove R_0.

   Note that for a current input, this adjustment is not necessary since the offset voltage of A_1 does not cause any error for current-source inputs.

2) Set $I_{IN} = I_{REF} = 1$mA. Adjust R_5 such that the output of A_2 (pin 10) is zero.

3) Set $I_{IN} = 1\mu A$, $I_{REF} = 1$mA. Adjust R_2 for $V_{OUT} = 3$ volts (for a 1 volt/decade scale factor) or 6 volts (for a 2 volt/decade scale factor).

Step #3 determines the scale factor. Setting $I_{IN} = 1\mu A$ optimizes the scale factor adjustment over a fairly wide dynamic range, from 1mA to 1nA. Clearly, if the 8048 is to be used for inputs which only span the range 100μA to 1mA, it would be better to set $I_{IN} = 100\mu A$ in Step #3. Similarly, adjustment for other scale factors would require different I_{IN} and V_{OUT} values.

FIGURE 1. 8048 OFFSET AND SCALE FACTOR ADJUSTMENT

MAXIMUM RATINGS

Supply Voltage	±18V
V_{in} (Input Voltage)	±15V
I_{ref} (Reference Current)	2mA
Voltage between Offset Null and V^+	±0.5V
Power Dissipation	750mW
Operating Temperature Range	0°C to +70°C
Output Short Circuit Duration	Indefinite
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTIC (Note 1)

PARAMETER	CONDITION	8049BC MIN.	8049BC TYP.	8049BC MAX.	8049CC MIN.	8049CC TYP.	8049CC MAX.	UNITS
Dynamic Range (V_{OUT})	V_{OUT} = 10mV to 10V	60			60			dB
Error, Absolute Value	T_A = 25°C, 0V≤V_{IN}≤3V		3	10		5	25	mV
Error, Absolute Value	T_A = 0°C to +70°C, 0V≤V_{IN}≤3V		20	75		30	150	mV
Temperature Coefficient, Referred to V_{IN}	V_{IN} = 3V		0.38			0.55		mV/°C
Power Supply Rejection Ratio	Referred to Input, for V_{IN} = 0V		2.0			2.0		μV/V
Offset Voltage (A_1 & A_2)	Before Nulling		15	25		15	50	mV
Wideband Noise	Referred to Input, for V_{IN} = 0V		26			26		μV(RMS)
Output Voltage Swing	R_L = 10kΩ	±12	±14		±12	±14		V
	R_L = 2kΩ	±10	±13		±10	±13		V
Power Consumption			150	200		150	200	mW
Supply Current			5	6.7		5	6.7	mA

NOTE 1: Unless otherwise noted, specifications apply for V_S = ±15V, T_A = 25°C, I_{REF} = 1mA, scale factor adjusted for 1 decade (out) per volt (in). Accuracy specifications assume that offset voltages and scale factor have been adjusted using the procedure on page 5.

TRANSFER FUNCTION (V_{OUT} AS A FUNCTION OF V_{IN})

MAXIMUM ERROR VOLTAGE REFERRED TO THE INPUT AS A FUNCTION OF V_{IN}

SMALL SIGNAL BANDWIDTH AS A FUNCTION OF INPUT VOLTAGE

SMALL SIGNAL VOLTAGE GAIN AS A FUNCTION OF INPUT VOLTAGE

5

THEORY OF OPERATION

The 8049 relies on the same logarithmic properties of the transistor as the 8048. The input voltage forces a specific ΔV_{BE} between Q_1 and Q_2 (Fig. 2). This V_{BE} difference is converted into a difference of collector currents by the transistor pair. The equation governing the behavior of the transistor pair is derived from (2) on Page 3 and is as follows:

$$I_{C_1}/I_{C_2} = \exp\left[q\Delta V_{BE}/kT\right] \quad (5)$$

When numerical values for q/kT are put into this equation, it is found that a ΔV_{BE} of 59mV (at 25°C) is required to change the collector current ratio by a factor of ten. But for ease of application, it is desirable that a 1 volt change at the input generate a tenfold change at the output. The required input attenuation is achieved by the network comprising R_1 and R_2. In order that scale factors other than one decade per volt may be selected, R_2 is external to the chip. It should have a value of 1kΩ, adjustable ±20%, for one decade per volt. R_1 is a thin film resistor deposited on the monolithic chip; its temperature characteristics are chosen to compensate the temperature dependence of equation 5, as explained on Page 3.

The overall transfer function is as follows:

$$I_{OUT}/I_{REF} = \exp\left[\frac{-R_2}{(R_1+R_2)} \times \frac{q V_{IN}}{kT}\right] \quad (6)$$

Substituting $V_{OUT} = I_{OUT} \times R_{OUT}$ gives:

$$V_{OUT} = R_{OUT}\, I_{REF} \exp\left[\frac{-R_2}{(R_1+R_2)} \times \frac{q V_{IN}}{kT}\right] \quad (7)$$

For voltage references equation 7 becomes

$$V_{OUT} = V_{REF} \times \frac{R_{OUT}}{R_{REF}} \exp\left[\frac{-R_2}{(R_1+R_2)} \times \frac{q V_{IN}}{kT}\right] \quad (8)$$

OFFSET AND SCALE FACTOR ADJUSTMENT

As with the log amplifier, the antilog amplifier requires three adjustments. The first step is to null out the offset voltage of A_2. This is accomplished by reverse biasing the base-emitter of Q_2. A_2 then operates as a unity gain buffer with a grounded input. The second step forces $V_{IN} = 0$; the output is adjusted for $V_{OUT} = 10V$. This step essentially "anchors" one point on the transfer function. The third step applies a specific input and adjusts the output to the correct voltage. This sets the scale factor. Referring to Fig. 2, the exact procedure for 1 decade/volt is as follows:

1) Connect the input (pin #16) to +15V. This reverse biases the base-emitter of Q_2. Adjust R_7 for $V_{OUT} = 0V$. Disconnect the input from +15V.
2) Connect the input to Ground. Adjust R_4 for $V_{OUT} = 10V$. Disconnect the input from Ground.
3) Connect the input to a precise 2V supply and adjust R_2 for $V_{OUT} = 100mV$.

The procedure outlined above optimizes the performance over a 3 decade range at the output (i. e., V_{OUT} from 10mV to 10V). For a more limited range of output voltages, for example 1V to 10V, it would be better to use a precise 1 volt supply and adjust for $V_{OUT} = 1V$. For other scale factors and/or starting points, different values for R_2 and R_{REF} will be needed, but the same basic procedure applies.

8049
FIGURE 2

APPLICATIONS INFORMATION

Scale Factor Adjustment

The scale factor adjustment procedures outlined on Page 3 (8048) and Page 5 (8049) are primarily directed towards setting up 1 volt (ΔV_{OUT}) per decade (ΔI_{IN} or ΔV_{IN}) for the log amp, or one decade (ΔV_{OUT}) per volt (ΔV_{IN}) for the antilog amp.

This corresponds to K = 1 in the respective transfer functions:

$$\text{Log Amp: } V_{OUT} = -K \log_{10}\left[{I_{IN}}/{I_{REF}}\right] \quad (9)$$

$$\text{Antilog Amp: } V_{OUT} = R_{OUT}\, I_{REF}\, 10^{-V_{IN}/K} \quad (10)$$

By adjusting R_2 (Fig. 1 and Fig. 2) the scale factor "K" in equation 9 and 10 can be varied. The effect of changing K is shown graphically in Fig. 3 for the log amp, and Fig. 4 for the antilog amp. The nominal value of R_2 required to give a specific value of K can be determined from equation 11. It should be remembered that R_1 has a ±20% tolerance in absolute value, so that allowance shall be made for adjusting the nominal value of R_2 by ±20%.

$$R_2 = \frac{941}{(K - .059)}\ \Omega \quad (11)$$

EFFECT OF VARYING "K" ON THE LOG AMPLIFIER

FIGURE 3

EFFECT OF VARYING "K" ON THE ANTILOG AMPLIFIER

FIGURE 4

Frequency Compensation

Although the op-amps in both the 8048 and the 8049 are compensated for unity gain, some additional frequency compensation is required. This is because the log transistors in the feedback loop add to the loop gain. In the 8048, 150 pF should be connected between Pins 2 and 7 (Fig. 1). In the 8049, 200 pF between Pins 3 and 7 is recommended (Fig. 2).

Error Analysis

Performing a meaningful error analysis of a circuit containing log and antilog amplifiers is more complex than dealing with a similar circuit involving only op-amps. In this data sheet every effort has been made to simplify the analysis task, without in any way compromising the validity of the resultant numbers.

The key difference in making error calculations in log/antilog amps, compared with op-amps, is that the gain of the former is a function of the input signal level. Thus, it is necessary, when referring errors from output to input, or vice versa, to check the input voltage level, then determine the gain of the circuit by referring to the graphs given on Pages 2 and 4.

The various error terms in the log amplifier, the 8048, are referred to the output (RTO) of the device. The error terms in the antilog amplifier, the 8049, are referred to the input (RTI) of the device. The errors are expressed in this way because in the majority of systems a number of log amps interface with an antilog amp, as shown in Fig. 5.

FIGURE 5

It is very straightforward to estimate the system error at node (A) by taking the square root of the sum-of-the squares of the errors of each contributing block.

$$\text{Total Error} = \sqrt{x^2 + y^2 + z^2} \quad \text{at (A)}$$

If required, this error can be referred to the system output through the voltage gain of the antilog circuit, using the voltage gain plot on Page 4.

The numerical values of x, y, and z in the above equation are obtained from the maximum error voltage plots given on Pages 2 and 4. For example, with the 8048BC, the maximum error at the output is 30mV at 25°C. This means that the measured output will be within 30mV of the theoretical transfer function, provided the unit has been adjusted per the procedures on Page 3. Fig. 6 illustrates this point.

To determine the maximum error over the operating temperature range, the 0 to 70°C absolute error values given in the table of electrical characteristics should be used. For intermediate temperatures, assume a linear increase in the error between the 25°C value and the 70°C value.

For the antilog amplifier, the only difference is that the error refers to the input, i. e., the horizontal axis. It will be noticed that the maximum error voltage of the 8049, over the temperature range, is strongly dependent on the input voltage. This is because the output amplifier, A_2, has an offset voltage drift which is directly transmitted to the output. When this error is referred to the input, it must be divided by the voltage gain, which is input voltage dependent. At V_{IN} = 3V, for example, errors at the output are multiplied by 1/.023 (= 43.5) when referred to the input.

It is important to note that both the 8048 and the 8049 require positive values of I_{REF}, and the input and output currents (or voltages) respectively must also be positive. Application of negative I_{IN} to the 8048 or negative I_{REF} to either circuit will cause malfunction, and if maintained for long periods, would lead to device degradation. Some protection can be provided by placing a diode between pin 7 and ground.

SETTING UP THE REFERENCE CURRENT

In both the 8048 and the 8049 the input current reference pin (I_{REF}) is not a true virtual ground. For the 8048, a fraction of the output voltage is seen on Pin 16 (Fig. 1). This does not constitute an appreciable error provided V_{REF} is much greater than this voltage. A 10V or 15V reference satisfies this condition. For the 8049, a fraction of the input voltage appears on Pin 3 (Fig. 2), placing a similar restraint on the value of V_{REF}.

Alternatively, I_{REF} can be provided from a true current source. One method of implementing such a current source is shown in Fig. 7.

LOG OF RATIO CIRCUIT, DIVISION

The 8048 may be used to generate the log of a ratio by modulating the I_{REF} input. The transfer function remains the same, as defined by equation 9:

$$V_{OUT} = -K \log_{10}\left[\frac{I_{IN}}{I_{REF}}\right] \qquad (9)$$

Clearly it is possible to perform division using just one 8048, followed by an 8049. For multiplication, it is generally necessary to use two log amps, summing their outputs into an antilog amp.

To avoid the problems caused by the I_{REF} input not being a true virtual ground (discussed in the previous section), the circuit of Fig. 7 is again recommended if the I_{REF} input is to be modulated.

5

TRANSFER FUNCTION FOR CURRENT INPUTS

Actual output will lie within shaded area for 8048 BC at 25°C

FIGURE 6

FIGURE 7

DEFINITION OF TERMS

In the definitions which follow, it will be noted that the various error terms are referred to the output of the log amp, and to the input of the antilog amp. The reason for this is explained on Page 6.

DYNAMIC RANGE The dynamic range of the 8048 refers to the range of input voltages or currents over which the device is guaranteed to operate. For the 8049 the dynamic range refers to the range of output voltages over which the device is guaranteed to operate.

ERROR, ABSOLUTE VALUE The absolute error is a measure of the deviation from the theoretical transfer function, after performing the offset and scale factor adjustments as outlined on Pages 3 (8048) or 5 (8049). It is expressed in mV and referred to the linear axis of the transfer function plot. Thus, in the case of the 8048, it is a measure of the deviation from the theoretical output voltage for a given input current or voltage. For the 8049 it is a measure of the deviation from the theoretical input voltage required to generate a specific output voltage.

The absolute error specification is guaranteed over the dynamic range.

ERROR, % OF FULL SCALE The error as a percentage of full scale can be obtained from the following relationship:

$$\text{Error, \% of Full Scale} = \frac{100 \times \text{Error, absolute value}}{\text{Full Scale Output Voltage}}$$

TEMPERATURE COEFFICIENT OF V_{OUT} OR V_{IN} For the 8048 the temperature coefficient refers to the drift with temperature of V_{OUT} for a constant input current.

For the 8049 it is the temperature drift of the input voltage required to hold a constant value of V_{OUT}.

POWER SUPPLY REJECTION RATIO The ratio of the voltage change in the linear axis of the transfer function (V_{OUT} for the 8048, V_{IN} for the 8049) to the change in the supply voltage, assuming that the log axis is held constant.

WIDEBAND NOISE For the 8048, this is the noise occurring at the output under the specified conditions. In the case of the 8049, the noise is referred to the input.

SCALE FACTOR For the log amp, the scale factor (K) is the voltage change at the output for a decade (i. e. 10:1) change at the input. For the antilog amp, the scale factor is the voltage change required at the input to cause a one decade change at the output. See equations 9 and 10.

ORDERING INFORMATION

TYPE	PACKAGE	MAX. ABSOLUTE ERROR (25°C)	TEMPERATURE RANGE	ORDER PART NUMBER
8048 BC	16 Pin Hermetic DIP	30mV	0°C to +70°C	ICL 8048 BC DE
8048 BC	16 Pin Plastic DIP	30mV	0°C to +70°C	ICL 8048 BC PE
8048 CC	16 Pin Hermetic DIP	60mV	0°C to +70°C	ICL 8048 CC DE
8048 CC	16 Pin Plastic DIP	60mV	0°C to +70°C	ICL 8048 CC PE
8049 BC	16 Pin Hermetic DIP	10mV	0°C to +70°C	ICL 8049 BC DE
8049 BC	16 Pin Plastic DIP	10mV	0°C to +70°C	ICL 8049 BC PE
8049 CC	16 Pin Hermetic DIP	25mV	0°C to +70°C	ICL 8049 CC DE
8049 CC	16 Pin Plastic DIP	25mV	0°C to +70°C	ICL 8049 CC PE

5

PACKAGE DIMENSIONS

16 PIN CERAMIC DIP (DE)

16 PIN PLASTIC DIP (PE)

INTERSIL

ICL7600/ICL7601
Commutating Auto-Zero (CAZ) Operational Amplifier

FEATURES
- Exceptionally low input offset voltage -- 2 μV
- Low long-term input offset voltage drift -- 0.2 μV/year
- Low input offset voltage temperature drift -- 0.005 μV/°C
- Low DC input bias current -- 300 pA
- Low DC input offset bias current -- 150 pA
- Wide common mode and differential input voltage ranges
- Excellent low supply voltage operation -- Down to ±2V
- Static-protected inputs -- no special handling required
- Fabricated using proprietary MAXCMOS™ technology
- Compensated (ICL7600) or uncompensated (ICL7601) versions

SYMBOL

GENERAL DESCRIPTION

The ICL7600/ICL7601 commutating auto-zero (CAZ) operational amplifiers are designed to replace almost any of today's expensive hybrid or monolithic ultra-low offset op amps, and will provide almost three orders of magnitude (1000x) reduction in input offset voltage compared with conventional device designs. This is achieved through Intersil's new CAZ amp principle, which uses an entirely new approach to low-frequency operational amplifier design.

The key feature of the CAZ principle is automatic compensation for long-term drift phenomena and temperature effects. Two internal op amps are connected so that when one amplifier is processing an input signal the other is maintained in an "auto-zero" mode. The ICL7600/ICL7601 contains all of the circuitry required for system operation, including an oscillator, a counter, level translators, analog switches and operational amplifiers. Only two external gain-setting resistors and two auto-zero capacitors are needed for complete amplifier function. Control of the oscillator and counter section is provided through the OSC and DR (division ratio) terminals. Internal biasing of the two on-chip op amps is programmable through a three-voltage-level terminal designated BIAS.

The ICL7600 is internally-compensated and is intended for applications which require voltage gains from unity through 100. The uncompensated ICL7601 is intended for those situations which require voltage gains of greater than 20. Major advantage of the ICL7601 over the ICL7600 at high gain settings is the reduction in commutation noise and subsequent greater accuracy.

Minimum periodic adjustments and extremely low offset voltage and temperature coefficients make the CAZ operational amplifiers very desirable for operation in adverse environments (temperature, humidity, toxic or radioactive) where equipment service is difficult. Since the device will auto-zero its internal offset errors, no adjustment is required other than that of gain, which is established by the external resistors.

PIN CONFIGURATION

ORDERING INFORMATION

Order parts by the following part numbers:

Compensated	Uncompensated	Package	Temperature Range
ICL7600 CPD	ICL7601 CPD	Plastic	0°C to +70°C
ICL7600 IJD	ICL7601 IJD	CERDIP	−25°C to +85°C
ICL7600 MJD	ICL7601 MJD	CERDIP	−55°C to +125°C

Order die by following part numbers: ICL7600/D ICL7601/D

5

ABSOLUTE MAXIMUM RATINGS (Note 1)

Total Supply Voltage (sum of both positive and negative supply voltages, V^+ and V^-) ..... 18 Volts
Positive Supply Voltage (GND to V^+) ..... 18 Volts
Negative Supply Voltage (GND to V^-) ..... 18 Volts
DR Input Voltage ..... (V^+ +0.3) to (V^+ −8) Volts
Input Voltage (C_1, C_2, +INPUT, −INPUT, BIAS, OSC (Note 2)) ..... (V^+ +0.3) to (V^- −0.3) Volts
Differential Input Voltage (Note 3) . ±(V^+ +0.3) to (V^- −0.3) Volts
Duration of Output Short Circuit (Note 4) ..... Unlimited
Continuous Total Power Dissipation at or below +25°C free air temperature (Note 5)
CERDIP Package ..... 500 mW
Plastic Package ..... 375 mW

Operating Temperature Range (ICL7600/ICL7601/MJD) ..... −55°C to +125°C
Operating Temperature Range (ICL7600/ICL7601/IJD) ..... −25°C to +85°C
Operating Temperature Range (ICL7600/ICL7601/CPD) ..... 0 to +70°C
Storage Temperature Range ..... −55 to +150°C
Lead Temperature (soldering, 60 seconds) ..... +300°C

Note 1: Stresses above those listed under "ABSOLUTE MAXIMUM RATINGS" may cause permanent device failures. These are stress ratings only and functional operation of devices under conditions other than those indicated in the Table of Electrical Characteristics is not recommended. Exposure to absolute maximum rating conditions for extended periods of time can cause device failures.

Note 2: An SCR structure is inherent in the CMOS process used in the fabrication of these devices. If voltages in excess of (V^+ +0.3) to (V^- −0.3) volts are connected to either inputs or outputs, destructive latchup can occur. For this reason it is recommended that no inputs from sources not on the same power supply or supplies be applied before the ICL7600/ICL7601 supplies are established, and that if multiple supplies are used the ICL7600/ICL7601 supplies be activated first.

Note 3: No restrictions are placed on the differential input voltages on either the inverting or non-inverting inputs, so long as these voltages do not exceed the power supply voltages by more than 0.3V.

Note 4: Outputs may be shorted to ground (GND) or to either supply (V^+, V^-). Temperature and/or supply voltages must be limited to insure that the dissipation rating is not exceeded.

Note 5: For operation above 25°C free-air temperature, derate 4mW/°C from 500mW for CERDIP and 3mW/°C from 375mW for plastic above 25°C.

BLOCK DIAGRAM

5

OPERATING CHARACTERISTICS:

Test Conditions: $V^+ = +5$ volts, $V^- = -5$ volts, $T_A = +25°C$, DR pin connected to V^+ ($f_{COM} \cong 160Hz$), $C_1 = C_2 = 1\mu F$, Test Circuit 1, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS		MIN	VALUE TYP	MAX	UNIT
Input Offset Voltage	V_{OS}	$R_S \leq 1k\Omega$	Low Bias Setting		±2		μV
		$C_1 = C_2 = 1\mu F$	Med Bias Setting		±2	±5	μV
			High Bias Setting		±7		μV
		MIL version over temp.	Med Bias Setting			±20	μV
Long Term Input Offset Voltage Stability	$V_{OS/Time}$	Low or Med Bias Settings			0.2		μV/year
Average Input Offset Voltage Temperature Coefficient	TCV_{OS}	Low or Med Bias Settings	$-55°C > T_A > +25°C$		0.005	0.1	μV/°C
			$+25°C > T_A > +85°C$		0.01	0.1	μV/°C
			$+25°C > T_A > +125°C$		0.05	0.15	μV/°C
Noise Voltage (RMS)	e_n	Band Width	Low Bias		0.8		μV
		0.1 to 10Hz	Med Bias		0.8		μV
		$R_S \leq 1k\Omega$	High Bias		1.0		μV
Equivalent Input Noise Voltage Peak-to-peak	e_{np-p}	Band Width	Low Bias		4.0		μV
		0.1 to 10Hz	Med Bias		4.0		μV
		$R_S \leq 1k\Omega$	High Bias		5.0		μV
Spot equivalent Noise voltage	e_{n10}	f = 10Hz Band Width 1Hz				700	nV/√Hz
Spot equivalent Noise Current	i_{n10}	f = 10Hz Band Width 1Hz				0.1	pA/√Hz
Differential Input Voltage Range	DIF V_{IN}			V^-−0.3	to	V^++0.3	V
Common Mode Input Range	CMVR	Low Bias		−4.2		+4.2	V
		Med Bias		−4.0		+4.0	V
		High Bias		−3.5		+3.5	V
Common Mode Rejection Ratio	CMRR	Any Bias Setting			88		dB
Power Supply Rejection Ratio	PSRR	Any Bias Setting			110		dB
Non Inverting Input Bias Current	I_{NIB}	Any Bias Setting. (Includes charge injection currents)			0.300	3	nA
Inverting Input Bias Current	I_{IB}	Any Bias Setting. (Includes charge injection currents)			0.150	1.5	nA
Voltage Gain	A_V	$R_L = 100k\Omega$	Low Bias	90	105		dB
			Med Bias	90	105		dB
			High Bias	80	100		dB
Maximum Output Voltage Swing	V_{OUT}	$R_L = 1M\Omega$			±4.9		V
							V
		$R_L = 100k\Omega$			±4.8		V
							V
		$R_L = 10k\Omega$	Positive Swing	+4.4			V
			Negative Swing			−4.5	V
Large Signal Slew Rate	SR	Unity	High Bias Setting		1.8		V/μs
		Gain	Med Bias Setting		0.5		V/μs
		ICL7600	Low Bias Setting		0.2		V/μs
Unity Gain Band Width	GBW		High Bias Setting		1.2		MHz
		ICL7600	Med Bias Setting		0.3		MHz
		Test Circuit 2	Low Bias Setting		0.12		MHz
Extrapolated Unity Gain Band Width	GBW		High Bias Setting		1.8		MHz
		ICL7601	Med Bias Setting		0.4		MHz
			Low Bias Setting		0.2		MHz
BIAS Terminal Input Current	I_{BIAS}	V^-−0.3 ≤ V_{BIAS} ≤ V^++0.3 volt			±30		pA
BIAS Voltage to Define Current Modes	V_{BH}	Low Bias Setting		V^+−0.3		V^++0.3	V
	V_{BM}	Med Bias Setting		V^-+1.4		V^+−1.4	V
	V_{BL}	High Bias Setting		V^-−0.3		V^-+0.3	V
DR (Division Ratio) Input Current	I_{DR}	V^+ −8.0V ≤ V_{DR} ≤ V^++0.3V			±30		pA
DR Voltage to define oscillator division ratio	V_{DRH}	Internal oscillator division ratio 32		V^+−0.3		V^++0.3	V
	V_{DRL}	Internal oscillator division ratio 2		V^+−8		V^+−1.4	V
Nominal Commutation Frequency	f_{COM}	C_{OSC} = 0 pF	DR Connected to V^+		160		Hz
			DR Connected to GND		2560		Hz
Supply Current	I_S	High Bias Setting		4	7	15	mA
		Medium Bias Setting		0.6	1.7	5	mA
		Low Bias Setting		0.25	0.6	1.5	mA
Operating Supply Voltage Range	V^+−V^-	High Bias Setting		5		16	V
		Medium or Low Bias Setting		4		16	V

5

TEST CIRCUITS

Test Circuit 1: Voltage Gain = 1000

Test Circuit 2: Unity Voltage Gain

Test Circuit 3: Voltage Gain = 10

Test Circuit 4: DC to 10Hz Unity Gain Low Pass Filter

TYPICAL CHARACTERISTICS

INPUT OFFSET VOLTAGE AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT OFFSET VOLTAGE AND PK TO PK NOISE VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGES

INPUT OFFSET VOLTAGE AND PK TO PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C_1, C_2 = 1µF)

INPUT OFFSET VOLTAGE AND PK TO PK NOISE VOLTAGE AS A FUNCTION OF COMMUTATION FREQUENCY (C_1, C_2 = 0.1µF)

INPUT OFFSET VOLTAGE AND PK TO PK NOISE AS A FUNCTION OF SUPPLY VOLTAGE (V^+-V^-)

INPUT CURRENT AS A FUNCTION OF COMMUTATION FREQUENCY

MAXIMUM OUTPUT VOLTAGE AS A FUNCTION OF OUTPUT LOAD RESISTANCE

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

OSCILLATOR FREQUENCY AS A FUNCTION OF EXTERNAL CAPACITIVE LOADING

FREQUENCY RESPONSE OF THE 10 Hz LOW PASS FILTER USED TO MEASURE NOISE (TEST CIRCUIT 4).

5

TOTAL EQUIVALENT INPUT OFFSET VOLTAGE AS A FUNCTION OF SOURCE IMPEDANCE — +INPUT

TOTAL EQUIVALENT INPUT OFFSET VOLTAGE AS A FUNCTION OF SOURCE IMPEDANCE — −INPUT

DETAILED DESCRIPTION

CAZ Operational Amplifier Operation

The CAZ operational amplifier functions on principles which are very different from those encountered in conventional op amp types. An important advantage of the ICL7600/ICL7601 devices is the ability to self-compensate for internal error voltages, whether they are steady-state, related to temperature or supply voltage, or variable in nature over a long term.

Operation of the ICL7600/ICL7601 CAZ operational amplifier is demonstrated in Figure 1. The basic amplifier configuration represented by the large triangles has one more input than does a regular op amp--the AZ, or auto-zero input. The voltage at the AZ input is that voltage to which each of the internal op amps must be auto-zeroed. In Mode A, op amp #2 is connected into a unity gain mode through on-chip analog switches, and charges the external capacitor C_2 to a voltage equal to the DC offset voltage of that amplifier, in addition to the instantaneous low frequency noise voltage. A short time later, the analog switches reconnect to the on-chip op amps in the configuration shown in Mode B. In this mode, op amp #2 has capacitor C_2 (which was charged to a voltage equal to its offset and noise voltage) connected in series to its non-inverting (+) input and nulls out the input offset and noise voltage of the amplifier. While one of the op amps is processing the input signal, the other is placed in an auto-zero mode and charges a capacitor to a voltage equal to its equivalent DC and low-frequency error voltage. The internal op amps are connected (at a rate designated as the commutation frequency, f_{COM}) so that at all times one or the other of the op amps is processing the input signal, while the voltages on capacitors C_1 and C_2 are being updated regularly to compensate for variables such as low-frequency noise voltage and input offset voltages due to drift with temperature, time, or supply voltage.

The CAZ amp concept offers a number of other advantages to the designer, as compared to standard bipolar or FET-input op amps:

- Effective input offset voltages can be made between 1000x and 10,000x less without trimming.
- Long-term drift phenomena are compensated for and dramatically reduced.
- Temperature effects are compensated for over a wide range. Reductions can be as high as 100 times or higher.
- Supply voltage sensitivity is reduced.

CMOS processing is ideally suited to implement the CAZ op amp structure. Not only is the digital section simple to design in CMOS, but the transmission gates (analog switches), which connect the internal op amps, are efficiently implemented for minimum charge injection and widest operating voltage range. The analog section, which includes the two on-chip op amps, provides performance which in most cases is similar to bipolar or FET input designs. Open loop gains of greater than 100 dB, typical offset voltages of ±5mV, and ultra-low input leakage currents (typically 1 pA) make the CMOS process quite suitable for the CAZ amp concept.

The on-chip op amps are connected internally to the external input and output terminals via CMOS analog switches, as shown in Figure 2. The analog switch structure shown in Figure 2 is arranged so that at any time three switches are open and three switches are conducting. Each analog switch includes a P-channel transistor in parallel with an N-channel transistor.

Figure 1: Diagramatic representation of the 2 half cycles of operation of the CAZ OP AMP.

Figure 2: Schematic of analog switches connecting each internal OP AMP to the external inputs at the output.

APPLICATIONS

The ICL7600/ICL7601 CAZ op amp is ideal for use as a front-end preamplifier for dual-slope A/D converters which require high sensitivity for single-ended input sources such as thermocouples.

A typical high-sensitivity A/D converter system is shown in Figure 3. The system uses an Intersil ICL7109 12-bit monolithic A/D binary converter, and is intended for direct interface with microprocessors. Both the ICL7600/ICL7601 and the ICL7109 use power supply voltages of ±5V, and the entire system consumes typically 2.5 mA of current.

The input signal is applied through a low-pass filter (150 Hz) to the CAZ op amp, which is connected in a non-inverting gain configuration of either 10 or 100. The internal oscillator of the CAZ amp is allowed to run free at about 5,200 Hz, resulting in a commutation frequency of 160 Hz, with the DR terminal connected to V^+. The error-storage capacitors C_1 and C_2 are each 1 μF value, and provide a good compromise between the minimum equivalent input offset voltage and the lowest value of low-frequency noise.

The output signal is then passed through a low-pass filter (1 MΩ and 0.1 μF), with a bandwidth of 1.5 Hz. This results in an equivalent DC offset voltage of 1 to 2 μV, and a peak-to-peak noise voltage of 1.7 μV, referred to the input of the CAZ amp. The output from the low-pass filter feeds directly into the input of the ICL7109.

In a system such as that shown in Figure 3 there is a degree of flexibility possible in assigning various gains to the ICL7600/ICL7601 pre-amplifier, and to various sensitivities for the ICL7109. For optimum performance, the CAZ op amp must amplify the input signal so that the equivalent 15μV input noise voltage of the A/D converter is masked. This implies a gain of at least 10 for the CAZ op amp preamplifier.

On the other hand, if the gain of the CAZ op amp is increased too much, its output swing will be limited by the ±5V supplies. This condition imposes a maximum gain of 200 to produce an output of ±0.000005 times 4,096 times 200, or ±4.096V, for a 5μV per count sensitivity. Use of an ICL7600 is recommended for low gains (<20) and the ICL7601 for gains of more than 20.

The values of the integrating resistor and the reference voltage must be chosen to suit the overall sensitivity of the system. For example, in a system requiring a sensitivity of 5μV per count, it is suggested to use a CAZ amp in a gain configuration of 100 (use ICL7601). Thus for a full scale count of 4096 (12 bits), the input voltage to the ICL7109 would be 5μV times 100 times 4096 or 2.048 volts. Since the ratio of input to reference is 2:1, the value of the reference voltage becomes 1.024V, and a 100kΩ integrating resistor is recommended. A system such as that shown in Figure 3 will allow a resolution of 1°C for low sensitivity platinum/rhodium junctions. For 0.1°C resolution, use high sensitivity thermocouples having copper/constantan junctions.

Figure 3: A/D system with 5μV resolution using an ICL7600/ICL7601 CAZ AMP preamplifier and an ICL7109 dual slope A/D converter.

The low-pass filter between the output of the CAZ op amp and the input of the ICL7109 A/D converter can be used to improve the signal-to-noise ratio of the system by reducing bandwidth. A 10 Hz filter will result in an equivalent peak-to-peak noise voltage figure of 4μV. If the bandwidth is reduced to 1.5 Hz, the peak-to-peak noise voltage will be reduced to about 1.7 μV, a reduction by a factor of three. The penalty for this reduction will be a lower system response time; however in most cases this will not be a major consideration, because of the large thermal inertia of many thermocouple probes.

SOME HELPFUL HINTS

Testing the ICL7600/ICL7601 CAZ Operational Amplifier

A simple and relatively accurate means of testing the CAZ op amp is to use a Tektronix Type 577 curve tracer, with the CAZ op amp inserted in a special 14-lead socket which plugs into a Tektronix 178, and which contains two soldered-in auto-zero capacitors of 1 μF each. This simple and convenient tester will provide most of the information needed for low-frequency parameters. The test setup will allow resolution of input offset voltages to about 10 μV.

For greater accuracy, it is suggested that a breadboard be built which minimizes thermoelectric effects and which includes an output low-pass filter of the type shown in Test Circuit #4. The output from the CAZ amp can be connected to a dual-slope A/D converter as shown in Figure 3. The low-frequency noise can then be displayed on a storage scope or on a strip chart recorder.

Bias Control

The on-chip op amps consume over 90% of the power required for the ICL7600/ICL7601. Three externally-programmable bias levels are provided. These levels are set by connecting the BIAS terminal to V^+, GND or V^-. The difference between each bias setting is approximately a factor of three, which allows a 9:1 ratio between supply current and the bias setting. The reason for this current programmability is to provide the user with a choice of device power dissipation levels, slew rate values (the higher the slew rate the better the recovery from commutation spikes), and offset errors due to chip "voltage drop" and thermoelectric effects (the higher the power dissipation the higher the input offset error). In most cases, the medium (MED BIAS) setting will be the best choice.

Output Loading (Resistive)

With a 10 kΩ load the output swing can cover nearly the entire supply voltage range, and the device can be used with loads as low as 2 kΩ. However, with loads of less than 50 kΩ, the on-chip op amps become transconductance amplifiers, since their output impedances are about 50 kΩ each. Thus the open-loop gain is 20 dB less with a 2 kΩ load than it would be with a 20 kΩ load. For high gain configurations requiring high accuracy, output loads of 100 kΩ or more are suggested.

Another consideration which must not be overlooked is the additional power dissipation of the chip which results from a large output swing into a low value load. This added variable can affect the initial input offset voltages under certain conditions.

Output Loading (Capacitive)

In many applications, it is desirable to include a low-pass filter at the output to reduce high-frequency noise outside the signal passband of interest. With conventional op amps, the obvious solution would be to place a capacitor across the external feedback resistor to provide the low pass filter.

However, with the CAZ op amp, this is not feasible because of the nature of commutation voltage spikes. The voltage spikes show a low impedance characteristic in the direction of the auto-zero voltage, and a high impedance on the recovery edge, as shown in Figure 4. It can be seen that the effect of a large load capacitor is to produce an area error in the output waveform, and hence an effective gain error. The output low pass filter must be a high impedance type to avoid output voltage area errors. For example, a 1.5 Hz filter should use a 100 kΩ resistor and a 1.0 μF capacitor, or a 1.0 MΩ resistor and an 0.1 μF capacitor.

Oscillator and Digital Considerations

The oscillator has been designed to run free at about 5.2 kHz when the OSC terminal is open-circuited. If the full divider network is used, this will result in a commutation frequency of about 160 Hz nominal. The commutation frequency is the frequency at which the on-chip op amps are switched between the signal processing and the auto-zero modes. A 160 Hz commutation frequency represents approximately the optimum frequency at which the input offset voltage is close to minimum, where the low-frequency noise is acceptable, and where errors derived from noise spikes will be low. Other commutation frequencies may provide optimization of other parameters, but always to the detriment of major characteristics.

The oscillator is of a high impedance type, so that a load of only a few picofarads on the OSC terminal will cause a significant shift in frequency. It is therefore recommended that if the desired frequency of the oscillation is 5.2kHz, the terminal should be left unattached and open. In other instances, it may be desirable to lock the oscillator to a clock

Figure 4: Effect of a load capacitor on output voltage waveforms.

or to run it at another frequency. The ICL7600/ICL7601 provides two degrees of flexibility. First, the DR (division ratio) terminal permits the user to choose between dividing the oscillator by 32 (DR terminal to V^+) or by 2 (DR terminal to GND), to obtain the commutation frequency. Second, the oscillator may have its frequency lowered by the addition of an external capacitor connected between the OSC terminal and V^+, or system ground terminals. For situations which required the commutation frequency to be locked onto a master clock, the OSC terminal can be driven from TTL logic (with resistive pull-up) or from CMOS logic, provided that the V^+ supply (with respect to ground) is +5V (±10%) and the logic driver also operates from a similar supply voltage. This is because the logic section -- including the oscillator -- operates from an internal -5V supply referenced to V^+ generated on-chip, and is not accessible externally.

Thermoelectric Effects

The ultimate limitations to ultra-high-precision DC amplifiers are due to thermoelectric, Peltier or thermocouple effects whereby junctions consist of various metals, alloys, silicon, etc. Unless all junctions are at precisely the same temperature, small thermoelectric voltages will be produced, generally about 0.1 μV/°C. However, these voltages can be several tens of microvolts per °C for certain thermocouple materials.

In order to realize the extremely low offset voltages which the CAZ op amp can provide, it is essential to take precautions to avoid temperature gradients. All components should be enclosed to eliminate air movement across device surfaces. Special low-temperature solder (70% cadmium, 30% tin) should be used. In addition, the supply voltages and power dissipation should be kept to a minimum. Use the medium bias mode as well as a high impedance load, and keep well away from heat dissipated by surrounding equipment.

Component Selection

The two required auto-zero capacitors, C_1 and C_2, should each be of 1.0 μF value. These are large values for non-electrolytic capacitors, but since the voltages impressed on them do not change significantly, problems of dielectric absorption and the like are not as important as they would be in applications involving integrating dual-slope A/D converters.

Excellent results have been obtained in operation at commercial temperature ranges when using several of the smaller-size and more economical capacitors, since the absolute values of the capacitors need not be critical. Although not guaranteed, polarized electrolytic capacitors rated at 1.0μF/50V have been used with success.

Commutating Voltage Transient Effects

While in most respects the CAZ op amp behaves like a conventional op amp, its principal applications will be in very low level, low-frequency preamplifiers limited to DC through 100 Hz. This is because of the finite switching transients which occur in the input and output terminals due to commutation effects. These transients have a frequency spectrum beginning at the commutation frequency, and include all of the higher harmonics. If the commutation frequency is higher than the highest in-band frequency, these transients can be effectively blanked with a low-pass filter.

The input commutation transients arise when each of the on-chip op amps experiences a shift in voltage equal to the input offset voltage about (5 - 10 mV), which usually occurs during the transition from the signal processing mode to the auto-zero mode. Since the input capacitances of the on-chip op amps are typically in the 10 pF range, and since it is desirable to reduce the effective input offset voltage about 10,000 times, the offset voltage auto-zero capacitors C_1 and C_2 must be at least 10,000 x 10 pF, or 0.1μF each.

Figure 5: Output waveform from Test Circuit 1.

The charge which is injected into the op amp when it is switched into the signal-processing mode produces a rapidly-decaying voltage spike at the input, in addition to an equivalent DC bias current averaged over a full cycle. This bias current is directly proportional to the commutation frequency, and in most instances will greatly exceed the inherent leakage currents of the input analog switches, which are typically about 1.0 pA at ambient temperature of 25°C.

The output waveform shown in Test Circuit #1 (with no input) is treated in Figure 5. Note that the equivalent noise voltage shown is amplified 1000 times, and that because of the finite slew rate of the on-chip op amps the 7 mV input transients are not amplified by 1000.

The output transient voltage effects (as distinct from the input effects which are propagated through the on-chip op amps) will occur if there is a difference in the output voltage of the internal op amps between the auto-zero modes and the signal-processing modes. The output stage of the on-chip op amp must slew from its auto-zero output voltage to the desired signal-processing output voltage. This is shown in Figure 6, where the system is auto-zeroed to ground.

The duration of the output transients is greatly affected by the gain configuration and the bias setting, since these two parameters have an effect on system slew rate. At low gains and high bias settings, the output transient durations are very short. For this reason there are two versions of the CAZ op amp, the ICL7600 which is compensated for unity gain and which can be used for gain configurations up to 100, and the ICL7601, which is uncompensated and recommended for operation in gain configurations greater than 20. Thus, when a signal is being processed in a high gain configuration, the effective output signal error is greater for the ICL7600 than it is for the ICL7601.

Figure 6: Simple CAZ OP AMP circuit and the output voltage waveform.

PACKAGE DIMENSIONS

14 LEAD CERDIP PACKAGE

14 LEAD PLASTIC PACKAGE

5

INTERSIL

LM101A, AD101A, LM301A, AD301A

General Purpose Operational Amplifier

GENERAL DESCRIPTION

The Intersil 101A and 301A integrated circuits are general purpose operational amplifiers. These high performance op amps are improved versions of the standard 101 and 709.

This general purpose op amp has many outstanding features; overload protection on the input and output, no latch-up when the common mode range is exceeded, and freedom from oscillations. The 101A also features better accuracy and lower noise in high impedance circuitry, and low input currents. Frequency compensation is achieved with a single 30 pF capacitor. It has advantages over internally compensated amplifiers in that the frequency compensation can be tailored to the particular application. For example, in low frequency circuits it can be overcompensated for increased stability margin. Or the compensation can be optimized to give more than a factor of ten improvement in high frequency performance for most applications.

The Intersil 101A operates over a temperature range from -55°C to +125°C. The 301A has an operating temperature range from 0°C to +70°C.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	101A	±22V
	301A	±18V
Power Dissipation (Note 1)		500 mW
Differential Input Voltage		±30V
Input Voltage (Note 2)		±15V
Output Short-Circuit Duration		Indefinite
Operating Temperature Range	101A	-55°C to 125°C
	301A	0°C to 70°C
Storage Temperature Range		-65°C to 150°C
Lead Temperature (Soldering, 60 sec)		300°C

NOTE 1: The maximum junction temperature of the 101A is 150°C, while that of the 301A is 100°C. For operating at elevated temperatures devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the flat package, the derating is based on thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

NOTE 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

SCHEMATIC DIAGRAM

TYPICAL APPLICATIONS

Fast Voltage Follower

Standard Compensation and Offset Balancing Circuit

Fast Summing Amplifier

CONNECTION DIAGRAMS

TO-5

NOTE: Pin 4 connected to case.

Flat Package

NOTE: Pin 5 connected to bottom of package.

8 Pin Plastic DIP

14 Pin DIP

NOTE: Pin 6 connected to bottom of package.

ELECTRICAL CHARACTERISTICS (Note)

PARAMETER	CONDITIONS	101A MIN	101A TYP	101A MAX	301A MIN	301A TYP	301A MAX	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50\ k\Omega$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		1.5	10		3	50	nA
Input Bias Current	$T_A = 25°C$		30	75		70	250	nA
Input Resistance	$T_A = 25°C$	1.5	4		0.5	2		MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm 20V$		1.8	3.0				mA
	$T_A = 25°C$, $V_S = \pm 15V$					1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	50	160		25	160		V/mV
Input Offset Voltage	$R_S \leq 50\ k\Omega$			3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	μV/°C
Input Offset Current				20			70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$		0.01	0.1				nA/°C
	$25°C \leq T_A \leq 70°C$					0.01	0.3	nA/°C
	$-55°C \leq T_A \leq 25°C$		0.02	0.2				nA/°C
	$0°C \leq T_A \leq 25°C$					0.02	0.6	nA/°C
Input Bias Current				100			300	nA
Supply Current	$T_A = +125°C$, $V_S = \pm 20V$		1.2	2.5				mA
Large Signal Voltage Gain	$V_S = \pm 15V$, $V_{OUT} = \pm 10V$, $R_L \geq 2\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm 15V$, $R_L = 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L = 2\ k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm 20V$	±15			±12			V
	$V_S = \pm 15V$							V
Common Mode Rejection Ratio	$R_S \leq 50\ k\Omega$	80	96		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\ k\Omega$	80	96		70	96		dB

NOTE: For the 101A, these specifications apply for $\pm 5V < V_S < \pm 20V$ and $-55°C \leq T_A \leq 125°C$ unless otherwise specified.
For the 301A, these specifications apply for $+5V \leq V_S \leq \pm 15V$ and $0°C \leq T_A \leq 70°C$, unless otherwise specified.

5

GUARANTEED PERFORMANCE FOR 101A, 301A*

INPUT VOLTAGE RANGE (101A/301A)

OUTPUT SWING (101A/301A)

TYPICAL PERFORMANCE FOR 101A, 301A*

SUPPLY CURRENT (101A)

VOLTAGE GAIN (101A)

INPUT CURRENT (101A/301A)

CURRENT LIMITING (101A/301A)

INPUT NOISE VOLTAGE (101A/301A)

INPUT NOISE CURRENT (101A/301A)

OPEN LOOP FREQUENCY RESPONSE (101A/301A)

LARGE SIGNAL FREQUENCY RESPONSE (101A/301A)

VOLTAGE FOLLOWER PULSE RESPONSE (101A/301A)

*301A only guaranteed to ±15V, 0°C ≤ T_A ≤ 70°C.

DEFINITION OF TERMS

INPUT VOLTAGE RANGE: The range of DC input voltages over which the regulator will operate within specifications.

OUTPUT VOLTAGE RANGE: The range of regulated output voltages over which the specifications apply.

OUTPUT-INPUT VOLTAGE DIFFERENTIAL: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate within specifications.

LINE REGULATION: The percentage change in regulated output voltage for a change in input voltage.

LOAD REGULATION: The percentage change in regulated output voltage for a change in load from the minimum load to the maximum load current specified.

CURRENT-LIMIT SENSE VOLTAGE: The voltage across the current limit terminals required to cause the regulator to current-limit with a short circuited output. This voltage is used to determine the value of the external current-limit resistor when external booster transistors are used.

TEMPERATURE STABILITY: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

FEEDBACK SENSE VOLTAGE: The voltage, referred to ground, on the feedback terminal of the regulator while it is operating in regulation.

OUTPUT NOISE VOLTAGE: The average AC voltage at the output with constant load and no input ripple.

STANDBY CURRENT DRAIN: That part of the operating current of the regulator which does not contribute to the load current.

PACKAGE OUTLINES

NOTES: All dimensions in inches.
Leads are gold-plated Kovar.

Order Number LM100H and LM300H

Order Number LM100F

ORDERING INFORMATION:

LM (or AD) 101 (or 301) AX

OPTIONAL

T	TO5
F	FLAT PACK
P	PLASTIC 8 PIN
D	CERAMIC 14 PIN

5

INTERSIL

AD741K General Purpose Operational Amplifier High Accuracy

GENERAL DESCRIPTION

The AD741K is a high accuracy version of the popular 741 op amp. By setting maximum limits on voltage drift, and significantly reducing errors due to offset voltage, bias and offset currents, gain, PSRR, and CMRR, improvements in accuracy on the order of five times can be achieved over that delivered by a standard 741.

SPECIFICATIONS

(Typical @ +25°C and ±15VDC, unless otherwise specified)

Model	AD741K
Open Loop Gain	
R_L = 1k Ω, V_O = ±10V	
R_L = 2k Ω, V_O = ±10V	50,000 min
Over Temp Range, $T_{min/max}$, same loads as above	25,000 min
Output Characteristics	
Voltage @ R_L = 1k Ω, $T_{min/max}$	
Voltage @ R_L = 2k Ω, $T_{min/max}$	±10V min
Short Circuit Current	25mA
Frequency Response	
Unity Gain, Small Signal	1MHz
Full Power Response	10kHz
Slew Rate, Unity Gain	0-5V/μsec
Input Offset Voltage	
Initial, $R_S \leq$ 10K Ω	2mV max
$T_{min/max}$	3mV max
Avg vs Temperature (untrim.)	15μV/°C max
vs Supply, $T_{min/max}$	15μV/V max
Input Offset Current	
Initial	10nA max
$T_{min/max}$	15nA max
Avg vs Temperature	0.2nA/°C max
Input Bias Current	
Initial	75nA max
$T_{min/max}$	120nA max
Avg vs Temperature	1.5nA/°C max
Input Impedance	
Differential	2M Ω
Input Voltage Range (Note 1)	
Differential, max safe	±30V
Common Mode, max safe	±15V
Common Mode Rejection $T_{min/max}$	90dB min
Power Supply	
Rated Performance	±15V
Operating	±(5 to 22)V
Current, Quiescent	2.8mA max
Temperature Range	
Operating, Rated Performance	0 to +70°C
Storage	−65°C to +150°C

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Power Dissipation	500mW
Differential Voltage	±30V
Input Voltage	±15V
Output Short Circuit Duration	indefinite
Operating Temp Range	0-70°C
Lead Temperature (soldering, 10 sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

CONNECTION DIAGRAMS/ ORDERING INFORMATION

TO-99

NOTE: PIN 4 CONNECTED TO CASE

Order No. AD741KH

8 PIN MINIDIP

NOTE: PIN 4 CONNECTED TO BOTTOM OF PACKAGE

Order No. AD741KN

5

INTERSIL

ICL741HS
High Speed 741 Operational Amplifier

FEATURES

- Pin For Pin and Electrically Equivalent to μA741
- Guaranteed Slew Rate – 0.7V/μs Min. Low Cost
- Short Circuit Protection
- Large Common-Mode Input Range
- Guaranteed Drift Characteristics
- No Latch Up
- Internal Frequency Compensation

GENERAL DESCRIPTION

The 741HS high slew rate version of the 741 general purpose operational amplifier is intended for applications where slew rate performance greater than 0.3V/μsec is required. Typical applications are oscillators, active filters, sample and hold and other large signal applications. This device has a guaranteed minimum slew rate of 0.7V/μsec and is identical and equivalent to the standard 741 operational amplifier. It will fill the application void between the 741 and 101A type amplifiers (slew rate = 0.3V/μsec) and the more costly high-speed amplifiers (slew rate = 30V/μsec).

HIGH-SPEED 741 OPERATIONAL AMPLIFIER

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Operating Temperature Range	0°C to +70°C
Storage Temperature Range	–65°C to +150°C
Lead Temperature (Soldering at 60 sec.)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

TEST CIRCUITS

TRANSIENT RESPONSE TEST CIRCUIT

FAST VOLTAGE FOLLOWER

Power Bandwidth: 15kHz
Slew Rate: 1V/μs

SCHEMATIC DIAGRAM

NOTE 1: The maximum junction temperature of the 741HS is 150°C, while that of the 741CHS is 100°C. For operating at elevated temperatures devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the flat package, the derating is based on thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

NOTE 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage. T_A = 25°C unless otherwise specified.

NOTE 3: Short circuit may be to ground or either supply.

NOTE 4: Pin 4 connected to case.

NOTE 5: Pin 5 connected to bottom of package.

NOTE 6: Pin 6 connected to bottom of package.

CONNECTION DIAGRAMS (Top View)

TO-5 (Note 4)

Flat Package (Note 5)

8 Pin Plastic DIP (Note 4)

14 Pin DIP (Note 6)

ELECTRICAL CHARACTERISTICS

PARAMETER	CONDITIONS	741CHS MIN	741CHS TYP	741CHS MAX	741MHS MIN	741MHS TYP	741MHS MAX	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50k\Omega$		2	6.0		1.0	5.0	mV
Input Offset Current	$T_A = 25°C$		20	200		20	200	nA
Input Bias Current	$T_A = 25°C$		200	500		200	500	nA
Input Resistance	$T_A = 25°C$	0.3	2.0		0.3	1.0		MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm15V$		1.7	2.8		1.7	2.8	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm15V$ $V_{OUT} = \pm10V$, $R_L \geq 2k\Omega$	25	160		50	160		V/mV
Input Offset Voltage	$R_S \leq 50k\Omega$			7.5			6	mV
Slew Rate	$V_{OUT} = \pm10V$, $R_L \geq 2k\Omega$ $C_L = 50pF$	0.7	1.0		0.7	1.0		V/μsec
Input Offset Current	$T_A = 25°C$			300			500	nA
Input Bias Current				0.8			1.5	μA
Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$ $R_L \geq 2k\Omega$	15			25			V/mV
Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k\Omega$	±12	±14		±12	±14		V
	$V_S = \pm15V$, $R_L = 2k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm15V$	±12			±12			V
Common Mode Rejection Ratio	$R_S \leq 50k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50k\Omega$	77	96		77	96		dB

DEFINITION OF TERMS

INPUT OFFSET VOLTAGE: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

INPUT OFFSET CURRENT: The difference in the currents into the two input terminals when the output is at zero.

INPUT VOLTAGE RANGE: The range of voltages on the input terminals for which the offset specifications apply.

INPUT BIAS CURRENT: The average of the two input currents.

COMMON MODE REJECTION RATIO: The ratio of the input voltage range to the peak-to-peak change in input offset voltage over this range.

INPUT RESISTANCE: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

SLEW RATE: A measure of the large signal capability of amplifier output to follow the amplifier input. Slew Rate = $2\pi BW_{Large\ Signal} V_{O\text{-}Peak}$.

SUPPLY CURRENT: The current required from the power supply to operate the amplifier with no load and the output at zero.

OUTPUT VOLTAGE SWING: The peak output voltage swing, referred to zero, that can be obtained without clipping.

LARGE-SIGNAL VOLTAGE GAIN: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

POWER SUPPLY REJECTION: The ratio of the change in input offset voltage to the change in power supply voltages producing it.

ORDERING INFORMATION

TYPE	TEMPERATURE RANGE	PACKAGE	ORDER NUMBER
741MHS	−55°C to +125°C	14 Pin DIP	ICL 741 MHS DD
741CHS	0°C to 70°C	8 Pin Plastic DIP	ICL 741 CHS PA
741MHS	−55°C to +125°C	TO-99	ICL 741 MHS TY
741MHS	−55°C to +125°C	Flat Pak	ICL 741 MHS FD
ICL 741 CHS	0°C to 70°C	TO-99	ICL 741 CHS TY

INTERSIL

ICL741-LN, ICL741C-LN, ICL101A-LN ICL301A-LN, ICL108-LN, ICL308-LN

Low Noise Operational Amplifiers

FEATURES

- Guaranteed Noise Specifications
- Complete Electrical Specifications

GENERAL DESCRIPTION

These low noise amplifiers are suitable for all applications where low level signals are encountered. The three important noise parameters, input referred voltage noise, input referred current noise, and popcorn noise, are all 100% screened and guaranteed.

CONNECTION DIAGRAMS

741/741C
TO-99

NOTE: PIN 4 CONNECTED TO CASE.

101A/301A
TO-99

NOTE: PIN 4 CONNECTED TO CASE.

108/308
TO-99

NOTE: PIN 4 CONNECTED TO CASE.

741
FLAT PACKAGE

NOTE: PIN 5 CONNECTED TO BOTTOM OF PACKAGE.

101A
FLAT PACKAGE

NOTE: PIN 5 CONNECTED TO BOTTOM OF PACKAGE.

741
HERMETIC
14 PIN DIP

NOTE: PIN 6 CONNECTED TO BOTTOM OF PACKAGE.

741C
PLASTIC
8 PIN DIP

101A
14 PIN DIP

NOTE: PIN 6 CONNECTED TO BOTTOM OF PACKAGE.

301A
PLASTIC
8 PIN DIP

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GUARANTEED NOISE SPECIFICATIONS ($T_A = 25°C$)

	741	741C	101A	301A	108	308	UNITS
Input Referred Voltage Noise @ 10 Hz (Max)	50	50	50	50	70	70	$nV/\sqrt{Hz}$
Input Referred Current Noise @ 10 Hz (Max)	0.4	0.4	0.7	0.7	0.2	0.2	$pA/\sqrt{Hz}$
Popcorn Noise Transition Amplitude for R_S = 100k (Max)	25	25	25	25	25	25	μV

741 INPUT REFERRED VOLTAGE NOISE

101A/301A INPUT REFERRED VOLTAGE NOISE

108/308 INPUT REFERRED VOLTAGE NOISE

741 INPUT REFERRED CURRENT NOISE

101A/301A INPUT REFERRED CURRENT NOISE

108/308 INPUT REFERRED CURRENT NOISE

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ORDERING INFORMATION

PART NUMBER	TYPE	PACKAGE	TEMPERATURE RANGE	ORDER NUMBER
741-LN	MIL	TO-99	-55°C to +125°C	ICL741-LN-TY
741C-LN	COM	TO-99	0°C to + 70°C	ICL741C-LN-TY
741-LN	MIL	14 Lead DIP	-55°C to +125°C	ICL741-LN-DD
741C-LN	COM	8 Lead DIP	0°C to + 70°C	ICL741C-LN-PA
741-LN	MIL	FLAT PACK	-55°C to +125°C	ICL741-LN-FB
101A-LN	MIL	TO-99	-55°C to +125°C	ICL101A-LN-TY
301A-LN	COM	TO-99	0°C to + 70°C	ICL301A-LN-TY
101A-LN	MIL	14 Lead DIP	-55°C to +125°C	ICL101A-LN-DD
301A-LN	COM	8 Lead DIP	0°C to + 70°C	ICL301A-LN-PA
101A-LN	MIL	FLAT PACK	-55°C to +125°C	ICL101A-LN-FB
108-LN	MIL	TO-99	-55°C to +125°C	ICL108-LN-TY
308-LN	COM	TO-99	0°C to + 70°C	ICL308-LN-TY

NOISE IN OPERATIONAL AMPLIFIERS

The noise of an amplifier may be expressed in terms of an input referred voltage generator (e_n) and an input referred current generator (i_n), see Figure 4. The total noise of an amplifier in a typical application contains contributions from both these generators, together with a contribution from the source resistance. The total mean square noise for a bandwidth of 1 Hz is given by:

$$e^2_T = e^2_n + i^2_n R^2_S + 4kTR_S \qquad (1)$$

Since both e_n and i_n are frequency dependent, the total mean square noise for a given bandwidth $\Delta f = f_2 - f_1$ is given by:

$$e^2_T = \int_{f_1}^{f_2} e^2_n \, df + R^2_S \int_{f_1}^{f_2} i^2_n \, df + 4kTR_S \Delta f \qquad (2)$$

With most amplifiers, the voltage noise term dominates for low source impedances. The current noise term is dominant at higher source impedances.

To specify operational amplifier noise performance one of two methods is used. One is to specify the total input referred noise for a given bandwidth and source impedance. This is defined as e_T from equation 1 above. The test circuit in Figure 5 is used. The typical broadband noise of the 741 and 101A type amplifier is shown in Figure 5.

The second method is to guarantee specific values of e_n and i_n (in equation 2) at various frequencies. A Noise Analyzer is used for this measurement (Figure 3). The values of e_n and i_n (for Δf = 1 Hz) are measured at 10 Hz, 100 Hz, 1 kHz, 10 kHz and 100 kHz. The recorded values may be plotted graphically, as shown on page 1. The noise information obtained from these measurements is considerably more general than that obtained from the first method, since the noise for any source impedance and bandwidth may be calculated from equation 2. (Graphical integration can determine the area under each curve.)

Popcorn noise should be screened visually using the circuit of Figure 3. Since popcorn noise is a function of the source impedance it is best represented by an input referred current source.

FIGURE 4.

FIGURE 5.

741/101A BROADBAND NOISE FOR VARIOUS BANDWIDTHS

FIGURE 6.

5

DEFINITION OF TERMS & TEST CIRCUITS

VOLTAGE NOISE: The noise due to the equivalent input voltage generator is measured using the circuit shown in Figure 1. It is expressed in $nV/\sqrt{Hz}$.

CURRENT NOISE: The noise due to the equivalent input current generator is measured using the circuit in Figure 2. It is expressed in $pA/\sqrt{Hz}$. Popcorn noise cannot be effectively screened using this test due to its erratic nature and very low frequency.

POPCORN NOISE: Popcorn noise, sometimes referred to as burst noise, is a low frequency noise phenomenon in which the output of the amplifier appears to jump erratically between two or more stable states. It is most noticeable when operating at high source impedances and is expressed as a transition amplitude, in μV, for a given source resistance. The test circuit of Figure 3 is used.

FIGURE 1.

FIGURE 2.

FIGURE 3.

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INTERSIL

ICL8008
Low Input Current Operational Amplifier

FEATURES

- Low Input Current
- No Frequency Compensation Required
- Offset Voltage Null Capability
- Large Common-Mode and Differential Voltage Ranges
- Low Power Consumption
- No Latch up

GENERAL DESCRIPTION

The 8008 is a high performance monolithic operational amplifier with very low input currents. It is intended for a wide range of analog applications. High common mode voltage range and absence of "latch-up" tendencies make the 8008 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The 8008 is short-circuit protected, has the same pin configuration as the popular 741 operational amplifier, and requires no external components for frequency compensation. The internal 6 dB/octave roll-off insures stability in closed loop applications.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Voltage between Offset Null and V^-	±0.5V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
8008M	-55°C to +125°C
8008C	0°C to +70°C
Lead Temperature (Soldering, 60 sec.)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

NOTE 1: Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.

NOTE 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 3: Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

SCHEMATIC DIAGRAM

CONNECTION DIAGRAMS

NOTE: Pin 4 CONNECTED TO CASE

ORDERING INFORMATION

PACKAGE DIMENSIONS

TO-5

Plastic DIP

NOTES: All dimensions in inches.
Dimensions as per latest J-10 committee.
Leads are gold-plated Kovar.
Package weight is 1.22 grams.

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ELECTRICAL CHARACTERISTICS (V_S = ±15V unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8008M MIN	8008M TYP	8008M MAX	8008C MIN	8008C TYP	8008C MAX	UNITS
The following specifications apply for T_A = 25°C:								
Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.0	5		1.0	6.0	mV
Input Offset Current			1.0	5		2.0	20	nA
Input Bias Current			2	10		5	25	nA
Input Resistance		5	25		5	25		MΩ
Input Capacitance			1.5			1.5		pF
Offset Voltage Adjustment Range			±15			±15		mV
Large-Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT} = ±10V	20,000	200,000		20,000	200,000		V/V
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Current			1.7	2.8		1.7	2.8	mA
Power Consumption			50	85		50	85	mW
Transient Response (unity gain)	V_{IN} = 20 mV, R_L = 2 kΩ,							
Risetime	$C_L \leq 100$ pF		0.3			0.3		μs
Overshoot			5.0			5.0		%
Slew Rate (unity gain)	$R_L \geq 2\ k\Omega$		0.5			0.5		V/μs
The following specifications apply for 0°C ≤ T_A ≤ +70°C (8008C), −55°C ≤ T_A ≤ +125°C (8008M):								
Input Offset Voltage	$R_S \leq 10\ k\Omega$		1.5	6		1.5	7.5	mV
Input Offset Voltage Average Temperature Coefficient	$R_S \leq 10\ k\Omega$		7			15		μV/°C
Input Offset Current				30			30	nA
Input Bias Current				50			50	nA
Input Voltage Range		±10	±12		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		30	150		30	150	μV/V
Large Signal Voltage Gain	$R_L \geq$ 2 kΩ, V_{OUT} = ±10V	15,000			15,000			V/V
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14		±12	±14		V
	$R_L \geq$ 2 kΩ	±10	±13		±10	±13		V

TYPICAL PERFORMANCE CURVES

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

TRANSIENT RESPONSE

CIRCUIT NOTES:

VOLTAGE OFFSET NULL CIRCUIT

TRANSIENT RESPONSE TEST CIRCUIT

INTERSIL

IH5101
Ultra Low Noise High Frequency Amplifier

FEATURES

- Input Noise Current $\leq 1.5 \frac{pA}{\sqrt{Hz}}$
- 10 MHz Bandwidth
- 40 dB Gain
- ±15V Supply

GENERAL DESCRIPTION

The IH5101 is specifically designed for transresistance amplifier applications. Its ultra low noise and high frequency capabilities make it ideal for vidicon head tube amplification. The low level current output of a vidicon head tube can be readily converted to a voltage level for system processing. For example, a 100 nA tube output current will be transformed into 75 mV of output voltage.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Current	1 mA
Peak Output Current	10 mA
Power Dissipation (Note)	1W
Storage Temperature	-65°C to +150°C
Operating Temperature (M)	-55°C to +125°C
(I)	-25°C to +85°C
Lead Temperature (soldering, 10 sec.)	300°C

NOTE: Dissipation rating assumes device is mounted with all leads welded or soldered to printed circuit board in ambient temperature below 70°C. For higher temperature, derate at rate of 10 mW/°C.

SCHEMATIC DIAGRAM

CONNECTION DIAGRAMS

ORDERING INFORMATION

PACKAGING DIMENSIONS

IE Package

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ELECTRICAL CHARACTERISTICS $V_S = \pm 15V$, (25°C unless otherwise noted)

PARAMETER	CONDITIONS	LIMITS MIN	LIMITS TYP	LIMITS MAX	UNITS
Transresistance (E_{OUT}/I_{IN})			0.75		mV/nA
Power Supply Current (Quiescent) (Pins 3 and 15)	$I_{IN} = 0$			15	mA
Output Impedance	f = 1 MHz			10	Ω
Output Swing	$R_L = 75\Omega$, f = 1 MHz		1.0		V_{p-p}
Bandwidth (3 dB)	$R_L = 75\Omega$	10^2		10^7	Hz
Transient Response (Step Response)	$R_L = 75\Omega$				
$t_{(ON)}$	10% to 90%			100	ns
$t_{(OFF)}$	90% to 10%			100	ns
Output Wide Band Noise	100 Hz to 10 MHz, $I_{IN} = 0$			3.0	mVrms
Input Current Noise				1.5	pA/√Hz

NOISE TESTING

OUTPUT WIDE BAND NOISE

BANDWIDTH FOR NOISE TEST

APPLICATION TIPS

VIDICON HEAD AMPLIFIER

TRANSRESISTANCE = 0.75 mV/nA

VIDEO AMPLIFIER WITH 40 dB VOLTAGE GAIN

5

INTERSIL

LH2101A/LH2301A Dual High Performance Op Amp

FEATURES

- Low offset voltage
- Low offset current
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode and supply voltage ranges
- Slew rate of 10V/μs

GENERAL DESCRIPTION

The LH2101A series of dual operational amplifiers consist of two LM101A type op amps in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, and reduced insertion cost.

The LH2101A is specified for operation over the −55°C to +125°C military temperature range, while the LH2301A is specified for operation over the 0°C to +70°C temperature range.

CONNECTION DIAGRAM

ORDER NUMBER LH2101AD, LH2301AD

AUXILIARY CIRCUITS

INVERTING AMPLIFIER WITH BALANCING CIRCUIT

†May be zero or equal to parallel combination of R_1 and R_2 for minimum offset.

ALTERNATE BALANCING CIRCUIT

SINGLE POLE COMPENSATION

TWO POLE COMPENSATION

FEEDFORWARD COMPENSATION

5

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Power Dissipation (Note 1) ..... 500 mW
Differential Input Voltage ..... ±30V
Input Voltage (Note 2) ..... ±15V
Output Short-Circuit Duration ..... Continuous
Operating Temperature Range LH2101A ..... −55°C to 125°C
LH2301A ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

ELECTRICAL CHARACTERISTICS Each side (Note 3)

PARAMETER	CONDITIONS	LIMITS LH2101A	LIMITS LH2301A	UNITS
Offset Voltage	$T_A = 25°C$, $R_S \leq 50k\Omega$	2.0	7.5	mV Max
Input Offset Current	$T_A = 25°C$	10	50	nA Max
Input Bias Current	$T_A = 25°C$	75	250	
Input Resistance	$T_A = 25°C$	1.5	0.5	MΩ Min
Supply Current	$T_A = 25°C$, $V_S = \pm20V$	3.0	3.0	mA Max
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm15V$ $V_{OUT} = \pm10V$, $R_L \geq 2k\Omega$	50	25	V/mV Min
Input Offset Voltage Average Temperature	$R_S \leq 50\ k\Omega$	3.0	10	mV Max
Coefficient of Input Offset Voltage		15	30	μV/°C Max
Input Offset Current		20	70	nA Max
Average Temperature	$25°C \leq T_A \leq 125°C$	0.1	0.3	nA/°C Max
Coefficient of Input Offset Current	$-55°C \leq T_A \leq 25°C$	0.2	0.6	
Input Bias Current		100	300	nA Max
Supply Current	$T_A = +125°C$, $V_S = \pm20V$	2.5		mA Max
Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$ $R_L \geq 2\ k\Omega$	25	15	V/mV Min
Output Voltage Swing	$V_S = \pm15V$, $R_L = 10\ k\Omega$	±12	±12	V Min
	$R_L = 2\ k\Omega$	±10	±10	
Input Voltage Range Common Mode	$V_S = \pm20V$	±15	±12	
Rejection Ratio Supply Voltage	$R_S \leq 50\ k\Omega$	80	70	dB Min
Rejection Ratio	$R_S \leq 50\ k\Omega$	80	70	

Note 1: The maximum junction temperature of the LH2101A is 150°C, and the thermal resistance is 100°C/W, junction to ambient.
Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
Note 3: These specifications apply for $\pm5V \leq V_S \leq \pm20V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified. For the LH2301A these specifications apply for $0°C \leq T_A \leq 70°C$, ±5V and $\leq V_S \leq \pm15V$. Supply current and input voltage range are specified as $V_S = \pm15V$ for the LH2301A. $C_1 = 30$ pF unless otherwise specified.

INTERSIL

LH2108, LH2308, LH2108A, LH2308A Dual Super Beta Op Amp

FEATURES

- Low offset current - 50 pA
- Low offset voltage - 0.7 mV
- Low offset voltage - LH2108A: 0.3 mV
  LH2108: 0.7 mV
- Wide input voltage range - ±15V
- Wide operating supply range - ±3V to ±20V

GENERAL DESCRIPTION

The LH2108A/LH2308A and LH2108/LH2308 series of dual operational amplifiers consist of two LM108A or LM108 type op amps in a single hermetic package. Featuring all the same performance characteristics of the single device, these duals also offer closer thermal tracking, lower weight, and reduced insertion cost.

The LH2108A/LH2108 is specified for operation over the -55°C to +125°C military temperature range, and the LH2308A/LH2308 is specified for operation from 0°C to +70°C.

CONNECTION DIAGRAM

ORDER NUMBER LH2108AD, LH2408AD, LH2108D, OR LH2408D

AUXILIARY CIRCUITS

STANDARD COMPENSATION CIRCUIT

ALTERNATE* FREQUENCY COMPENSATION

*Improves rejection of power supply noise by a factor of ten.

FEEDFORWARD COMPENSATION

5

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±20V
Power Dissipation (Note 1) ..... 500 mW
Differential Input Current (Note 2) ..... ±10mA
Input Voltage (Note 3) ..... ±15V
Output Short Circuit Duration ..... Continuous
Operating Temperature Range
LH2108A/LH2108 ..... −55°C to +125°C
LH2308A/LH2408 ..... 0°C to +70°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

ELECTRICAL CHARACTERISTICS Each side (Note 4)

PARAMETER	CONDITIONS	LIMITS LH2108	LIMITS LH2308	UNITS
Input Offset Voltage	$T_A = 25°C$	2.0	7.5	mV Max
Input Offset Current	$T_A = 25°C$	0.2	1.0	nA Max
Input Bias Current	$T_A = 25°C$	2.0	7.0	
Input Resistance	$T_A = 25°C$	30	10	MΩ Min
Supply Current	$T_A = 25°C$	0.6	0.8	mA Max
Large Signal Voltage Gain	$T_A = 25°C$ $V_S = \pm15V$ $V_{OUT} = \pm10V$, $R_L \geq 10\ k\Omega$	50	25	V/mV Min
Input Offset Voltage		3.0	10	mV Max
Average Temperature Coefficient of Input Offset Voltage		15	30	μV/°C Max
Input Offset Current		0.4	1.5	nA Max
Average Temperature Coefficient of Input Offset Current		2.5	10	pA/°C Max
Input Bias Current		3.0	10	nA Max
Supply Current	$T_A = +125°C$	0.4	—	mA Max
Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$ $R_L \geq 10\ k\Omega$	25	15	V/mV Min
Output Voltage Swing	$V_S = \pm15V$, $R_L = 10\ k\Omega$	±13	±13	V Min
Input Voltage Range	$V_S = \pm15V$	±13.5	±14	
Common Mode Rejection Ratio		85	80	dB Min
Supply Voltage Rejection Ratio		80	80	

PARAMETER	CONDITIONS	LIMITS LH2108A	LIMITS LH2308A	UNITS
Input Offset Voltage	$T_A = 25°C$	0.5	0.5	mV Max
Input Offset Current	$T_A = 25°C$	0.2	1.0	nA Max
Input Bias Current	$T_A = 25°C$	2.0	7.0	
Input Resistance	$T_A = 25°C$	30	10	MΩ Min
Supply Current	$T_A = 25°C$	0.6	0.8	mA Max
Large Signal Voltage Gain	$T_A = 25°C$ $V_S = \pm15V$ $V_{OUT} = \pm10V$, $R_L \geq 10\ k\Omega$	80	80	V/mV Min
Input Offset Voltage		1.0	0.73	mV Max
Average Temperature Coefficient of Input Offset Voltage		5	5	μV/°C Max
Input Offset Current		0.4	1.5	nA Max
Average Temperature Coefficient of Input Offset Current		2.5	10	pA/°C Max
Input Bias Current		3.0	10	nA Max
Supply Current	$T_A = +125°C$	0.4	-	mA Max
Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$ $R_L \geq 10\ k\Omega$	40	60	V/mV Min
Output Voltage Swing	$V_S = \pm15V$, $R_L = 10\ k\Omega$	±13	±13	V Min
Input Voltage Range	$V_S = \pm15V$	±13.5	±14	
Common Mode Rejection Ratio		96	96	dB Min
Supply Voltage Rejection Ratio		96	96	

Note 1: The maximum junction temperature of the LH2108/A is 150°C, and that of the LH2308/A is 85°C. The thermal resistance of the packages is 100°C/W, junction to ambient.
Note 2: The inputs are shunted with back-to-back diodes for overvoltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.
Note 3: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
Note 4: These specifications apply for $\pm5V \leq V_S \leq \pm20V$ and $-55°C \leq T_A \leq 125°C$, unless otherwise specified, and the LH2308A/LH2308 for $\pm5V \leq V_S \leq 15V$ and $0°C \leq T_A \leq 70°C$.

INTERSIL

LM107, LM207, LM307
Operational Amplifiers

FEATURES

- Offset voltage 3 mV maximum over temperature (107 and 207)
- Input current 100 nA maximum over temperature (107 and 207)
- Offset current 20 nA maximum over temperature (107 and 207)
- Guaranteed drift characteristics
- Offsets guaranteed over entire common mode range

GENERAL DESCRIPTION

The 107 series amplifiers are complete, general purpose operational amplifiers, with the necessary frequency compensation built into the chip. Advanced processing techniques make the input currents a factor of ten lower than industry standards like the 709. Yet, they are a direct, plug-in replacement for the 709, LM101, LM101A and 741.

The 107 series provides better accuracy and lower noise than its predecessors in high impedance circuitry. The low input currents also make it particularly well suited for long interval integrators of timers, sample and hold circuits and low frequency waveform generators. Further, replacing circuits where matched transistor pairs buffer the inputs of conventional IC op amps, it can give lower offset voltage and drift at reduced cost.

The 207 is identical to the 107, except that the 207 has its performance guaranteed over a −25°C to 85°C temperature range, instead of −55°C to 125°C. The 307 has somewhat different specifications, and operates from 0°C to 70°C.

SCHEMATIC DIAGRAM

5

CONNECTION DIAGRAMS

Metal Can

Order Number LM107T, LM207T or LM307T

TO-5 Can

Order Number LM307P

8-Pin MiniDIP

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 107, 207	±22V	Operating Temperature Range	107	−55°C to 125°C
307	±18V		207	−25°C to 85°C
Power Dissipation (Note 1)	500 mW		307	0°C to 70°C
Differential Input Voltage	±30V	Storage Temperature Range		−65°C to 150°C
Input Voltage (Note 2)	±15V	Lead Temperature (Soldering, 60 sec)		300°C
Output Short-Circuit Duration (Note 3)	Indefinite			

SWITCHING CHARACTERISTICS

PARAMETER	CONDITIONS	107, 207 MIN	107, 207 TYP	107, 207 MAX	307 MIN	307 TYP	307 MAX	UNITS
Input Offset Voltage	$T_A = 25°C$, $R_S \leq 50\,k\Omega$		0.7	2.0		2.0	7.5	mV
Input Offset Current	$T_A = 25°C$		1.5	10		3	50	nA
Input Bias Current	$T_A = 25°C$		30	75		70	250	nA
Input Resistance	$T_A = 25°C$	1.5	4		0.5	2		MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm20V$		1.8	3.0				mA
	$T_A = 25°C$, $V_S = \pm15V$					1.8	3.0	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L \geq 2\,k\Omega$	50	160		25	160		V/mV
Input Offset Voltage	$R_S \leq 50\,k\Omega$			3.0			10	mV
Average Temperature Coefficient of Input Offset Voltage			3.0	15		6.0	30	μV/°C
Input Offset Current				20			70	nA
Average Temperature Coefficient of Input Offset Current	$25°C \leq T_A \leq 125°C$		0.01	0.1				nA/°C
	$-55°C \leq T_A \leq 25°C$		0.02	0.2				nA/°C
	$25°C \leq T_A \leq 70°C$					0.01	0.3	nA/°C
	$0°C \leq T_A \leq 25°C$					0.02	0.6	nA/°C
Input Bias Current				100			300	mA
Supply Current	$T_A = +125°C$, $V_S = \pm20V$		1.2	2.5				mA
Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L \geq 2\,k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm15V$, $R_L = 10\,k\Omega$	±12	±14		±12	±14		V
	$R_L = 2\,k\Omega$	±10	±13		±10	±13		V
Input Voltage Range	$V_S = \pm20V$	±15						V
	$V_S = \pm15V$				±12			V
Common Mode Rejection Ratio	$R_S \leq 50\,k\Omega$	80	96		70	90		dB
Supply Voltage Rejection Ratio	$R_S \leq 50\,k\Omega$	80	96		70	96		dB

Note 1: The maximum junction temperature of the 107 is 150°C, while that of the 207 is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3: Continuous short circuit is allowed for case temperatures to 70°C and ambient temperatures to 55°C.

Note 4: These specifications apply for $\pm5V < V_S < \pm20V$ and $-55°C \leq T_A \leq 125°C$ for the 107 or $-25°C \leq T_A \leq 85°C$ for the 207, unless otherwise specified. For the 307, the specifications apply for $0°C \leq T_A \leq 70°C$ and $\pm5V \leq V_S \leq \pm15V$, unless otherwise specified.

INTERSIL

LM108/A, LM208/A, LM308/A
Low Level Operational Amplifiers

FEATURES

- Input Bias Current – 2 nA max to 7 nA max
- Input Offset Current – 0.2 nA max to 1 nA max
- Input Offset Voltage – 0.5 mV max to 7.5 mV max
- $\Delta V_{os}/\Delta T$ – 5 μV/°C to 30 μV/°C
- $\Delta I_{os}/\Delta T$ – 2.5 pA/°C to 10 pA/°C
- Pin for Pin Replacement for 101A/301A

GENERAL DESCRIPTION

These differential input, precision amplifiers provide low input currents and offset voltages competitive with FET and chopper stabilized amplifiers. They feature low power consumption over a supply voltage range of ±2V to ±20V. The amplifiers may be frequency compensated with a single external capacitor. The LM108A, LM208A, and LM308A are high performance selections from the 108/208/308 amplifier family.

FREQUENCY COMPENSATION CIRCUITS

STANDARD CIRCUIT

ALTERNATE CIRCUIT: IMPROVES REJECTION OF POWER SUPPLY NOISE BY A FACTOR OF TEN.

CONNECTION DIAGRAMS

TO-99 PACKAGE

NOTE: On metal Can, Pin 4 is connected to case.

DUAL-IN-LINE PACKAGE

NOTES: On DIP, Pin 7 is connected to case.
Pin 1 is marked for orientation.

5

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	
108, 208, 108A, 208A,	±20V
308, 308A	±18V
Internal Power Dissipation (Note 1)	
Metal Can (TO-99	500 mW
DIP (Hermetic)	500 mW
Differential Input Current (Note 2)	±10 mA
Input Voltage (Note 3)	±15V
Output Short-Circuit Duration	Indefinite
Operating Temperature Range	
108, 108A	−55°C to +125°C
208, 208A	−25°C to +85°C
308, 308A	0°C to +70°C
Storage Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec.)	300°C

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified) (Note 4)

PARAMETER	CONDITIONS	308			308A			108 208			108A 208A			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage			2.0	7.5		0.3	0.5		0.7	2.0		0.3	0.5	mV
Input Offset Current			0.2	1.0		0.2	1.0		0.05	0.2		0.05	0.2	nA
Input Bias Current			1.5	7		1.5	7		0.8	2.0		0.8	2.0	nA
Input Resistance		10	40		10	40		30	70		30	70		MΩ
Supply Current	V_S = ±20V								0.3	0.6		0.3	0.6	mA
	V_S = ±15V		0.3	0.8		0.3	0.8							mA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq 10\ k\Omega$	25	300		80	300		50	300		80	300		V/mV
THE FOLLOWING SPECIFICATIONS APPLY OVER THE OPERATING TEMPERATURE RANGES														
Input Offset Voltage				10			0.73			3.0			1.0	mV
Input Offset Current				1.5			1.5			0.4			0.4	nA
Average Temperature Coefficient of Input Offset Voltage			6.0	30		1.0	5.0		3.0	15		1.0	5.0	μV/°C
Average Temperature Coefficient of Input Offset Current			2	10		2.0	10		0.5	2.5		0.5	2.5	pA/°C
Input Bias Current				10			10			3.0			3.0	nA
Large Signal Voltage Gain	V_S = ±15V, V_{OUT} = ±10V, $R_L \geq 10\ k\Omega$	15			60			25			40			V/mV
Input Voltage Range	V_S = ±15V	±13.5			±13.5			±13.5			±13.5			V
Common Mode Rejection Ratio		80	100		96	110		85	100		96	110		dB
Supply Voltage Rejection Ratio		80	96		96	110		80	96		96	110		dB
Output Voltage Swing	V_S = ±15V, R_L = 10 kΩ	±13	±14		±13	±14		±13	±14		±13	±14		V
Supply Current	T_A = +125°C, V_S = ±20V								0.15	0.4		0.15	0.4	mA

NOTE 1: Derate Metal Can package at 6.8 mW/°C for operation at ambient temperatures above 75°C and the Dual In-Line package at 9 mW/°C for operation at ambient temperatures above 95°C.

NOTE 2: The inputs are shunted with back-to-back diodes for over-voltage protection. Therefore, excessive current will flow if a differential input voltage in excess of 1V is applied between the inputs unless some limiting resistance is used.

NOTE 3: For supply voltages less than ±15V, the maximum input voltage is equal to the supply voltage.

NOTE 4: Unless otherwise specified, these specifications apply for supply voltages from ±5V to ±20V for the 108, 208, 108A and 208A and from ±5V to ±15V for the 308 and 308A.

TYPICAL PERFORMANCE CURVES

INPUT CURRENTS

MAXIMUM DRIFT ERROR

MAXIMUM OFFSET ERROR

POWER SUPPLY REJECTION

INPUT NOISE VOLTAGE

VOLTAGE GAIN

OUTPUT SWING

SUPPLY CURRENT

OPEN LOOP FREQUENCY RESPONSE

CLOSED LOOP OUTPUT IMPEDENCE

LARGE SIGNAL FREQUENCY RESPONSE

VOLTAGE FOLLOWER PULSE RESPONSE

5

GUARDING

Extra care must be taken in the assembly of printed circuit boards to take full advantage of the low input currents of the 108 amplifier. Boards must be thoroughly cleaned with TCE or alcohol and blown dry with compressed air. After cleaning, the boards should be coated with epoxy or silicone rubber to prevent contamination.

Even with properly cleaned and coated boards, leakage currents may cause trouble at 125°C, particularly since the input pins are adjacent to pins that are at supply potentials. This leakage can be significantly reduced by using guarding to lower the voltage difference between the inputs and adjacent metal runs. Input guarding of the 8-lead TO-99 package is accomplished by using a 10-lead pin circle, with the leads of the device formed so that the holes adjacent to the inputs are empty when it is inserted in the board. The guard, which is a conductive ring surrounding the inputs, is connected to a low impedance point that is at approximately the same voltage at the inputs. Leakage currents from high-voltage pins are then absorbed by the guard.

The pin configuration of the dual in-line package is designed to facilitate guarding, since the pins adjacent to the inputs are not used (this is different from the standard 741 and 101A pin configuration).

CONNECTION OF INPUT GUARDS

INVERTING AMPLIFIER FOLLOWER NON-INVERTING AMPLIFIER

PHYSICAL DIMENSIONS

TO-99 PACKAGE

NOTES: All dimensions in inches.
Leads are gold-plated Kovar.

DUAL-IN-LINE PACKAGE

NOTES: All dimensions in inches.
Leads are intended for insertion in hole rows on .300 centers

ORDERING INFORMATION

PART NUMBER	PACKAGE TYPE	TEMPERATURE RANGE	ORDER NUMBER
108	TO-99 DIP	-55°C to +125°C	LM108T LM108D
208	TO-99 DIP	-25°C to +85°C	LM208T LM208D
308	TO-99 DIP	0°C to +70°C	LM308T LM308D
108A	TO-99 DIP	-55°C to +125°C	LM108AT LM108AD
208A	TO-99 DIP	-25°C to +85°C	LM208AT LM208AD
308A	TO-99 DIP	0°C to +70°C	LM308AT LM308AD

INTERSIL

LM124/LM224/LM324, LM124A/LM224A/LM324A, LM2902
Low Power Quad Operational Amplifiers

FEATURES

- Internally frequency compensated for unity gain
- Large dc voltage gain — 100dB
- Wide bandwidth (unity gain) (temperature compensated) — 1MHz
- Wide power supply range:
  - Single supply — $3V_{DC}$ to $30V_{DC}$
  - or dual supplies — $\pm1.5V_{DC}$ to $\pm15V_{DC}$
- Very low supply current drain (800μA) — essentially independent of supply voltage (1mW/op amp at $+5V_{DC}$)
- Low input biasing current (temperature compensated) — 45nA
- Low input offset — 2mV
  - and offset current — 5nA
- Input common-mode voltage range includes ground
- Differential input voltage range equal to the power supply voltage
- Large output voltage swing — $0V_{DC}$ to $V^+ - 1.5V_{DC}$

GENERAL DESCRIPTION

The LM124 series consists of four independent, high gain, internally frequency compensated operational amplifiers which were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage.

Application areas include transducer amplifiers, dc gain blocks and all the conventional op amp circuits which now can be more easily implemented in single power supply systems. For example, the LM124 series can be directly operated off of the standard $+5V_{DC}$ power supply voltage which is used in digital systems and will easily provide the required interface electronics without requiring the additional $\pm15V_{DC}$ power supplies.

In the linear mode the input common-mode voltage range includes ground, and the output voltage can also swing to ground, even though operated from only a single power supply voltage.

The unity gain cross frequency is temperature compensated, as is the input bias current.

CONNECTION DIAGRAM

DUAL-IN-LINE AND FLAT PACKAGE

CHIP CONFIGURATION

CHIP DIMENSION 56 x 61 MILS

SCHEMATIC DIAGRAM (Each Amplifier)

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE	ORDER NUMBERS
LM124D	55°C to +125°C	Ceramic Dip	LM124D DD
LM224D	−25°C to +85°C	Ceramic Dip	LM224D DD
LM324N	0°C to +70°C	Epoxy Dip	LM324N PD
LM324D	0°C to +70°C	Ceramic Dip	LM324D DD

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ABSOLUTE MAXIMUM RATINGS

	LM124/LM224/LM324 LM124A/LM224A/LM324A	LM2902
Supply Voltage, V^+	$32V_{DC}$ or $\pm16V_{DC}$	$26V_{DC}$ or $\pm13V_{DC}$
Differential Input Voltage	$32V_{DC}$	$26V_{DC}$
Input Voltage	$-0.3V_{DC}$ to $+32V_{DC}$	$-0.3V_{DC}$ to $+32V_{DC}$
Power Dissipation (Note 1)		
Molded DIP	570mW	570mW
Cavity DIP	900mW	
Flat Pack	800mW	
Output Short-Circuit to GND (One Amplifier) (Note 2) $V^+ \leq 15V_{DC}$ and $T_A = 25°C$	Continuous	Continuous
Input Current ($V_{IN} < -0.3\ V_{OL}$) (Note 3)	50mA	
Operating Temperature Range		−40°C to +85°C
LM324/LM324A	0°C to +70°C	
LM224/LM224A	−25°C to +85°C	
LM124/LM124A	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

ELECTRICAL CHARACTERISTICS ($V^+ = +5.0V_{DC}$, Note 4)

PARAMETER	CONDITIONS	LM124A MIN	LM124A TYP	LM124A MAX	LM224A MIN	LM224A TYP	LM224A MAX	LM324A MIN	LM324A TYP	LM324A MAX	LM124/LM224 MIN	LM124/LM224 TYP	LM124/LM224 MAX	LM324 MIN	LM324 TYP	LM324 MAX	LM2902 MIN	LM2902 TYP	LM2902 MAX	UNITS
Input Offset Voltage	$T_A = 25°C$, (Note 5)		1	2		1	3		2	3		±2	±5		±2	±7		±2	±7	mV_{DC}
Input Bias Current (Note 6)	$I_{IN(+)}$ or $I_{IN(-)}$, $T_A = 25°C$		20	50		40	80		45	100		45	150		45	250		45	250	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25°C$		2	10		2	15		5	30		±3	±30		±5	±50		±5	±50	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30V_{DC}$, $T_A = 25°C$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Supply Current	$R_L = \infty$ $V_{CC} = 30V$, (LM2902 $V_{CC} = 26C$)		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3		1.5	3	mA_{DC}
	$R_L = \infty$ On All Op Amps Over Full Temperature Range		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2		0.7	1.2	mA_{DC}
	$T_A = 25°C$																		3	mA_{DC}
Large Signal Voltage Gain	$V^+ = 15V_{DC}$ (For Large V_O Swing) $R_L \geq 2k\Omega$, $T_A = 25°C$	50	100		50	100		25	100		50	100		25	100			100		V/mV
Output Voltage Swing	$R_L = 2k\Omega$, $T_A = 25°C$ (LM2902 $R_L \geq 10k\Omega$)										0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Common-Mode Rejection Ratio	DC, $T_A = 25°C$	70	85		70	85		65	85		70	85		65	70		50	70		dB
Power Supply Rejection Ratio	DC, $T_A = 25°C$	65	100		65	100		65	100		65	100		65	100		50	100		dB
Amplifier-to-Amplifier Coupling (Note 8)	f = 1kHz to 20kHz, $T_A = 25°C$ (Input Referred)		−120			−120			−120			−120			−120			−120		dB
Output Current Source	$V_{IN^+} = 1V_{DC}$, $V_{IN-} = 0V_{DC}$, $V^+ = 15V_{DC}$, $T_A = 25°C$	20	40		20	40		20	40		20	40		20	40		20	40		mA_{DC}
Sink	$V_{IN-} = 1V_{DC}$, $V_{IN} = 0V_{DC}$, $V^+ = 15V_{DC}$, $T_A = 25°C$	10	20		10	20		10	20		10	20		10	20		10	20		mA_{DC}
	$V_{IN-} = 1V_{DC}$, $V_{IN^+} = 0V_{DC}$, $T_A = 25°C$, $V_O = 200mV_{DC}$	12	50		12	50		12	50		12	50		12	50					μA_{DC}
Short Circuit to Ground	$T_A = 25°C$, (Note 2)		40	60		40	60		40	60		40	60		40	60		40	60	mA_{DC}

ELECTRICAL CHARACTERISTICS (con't)

PARAMETER	CONDITIONS	LM124A			LM224A			LM324A			LM124/LM224			LM324			LM2902			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	(Note 5)			4			4			5			±7			±9			10	mV_{DC}
Input Offset Voltage Drift	$R_S = 0\Omega$		7	20		7	20		7	30		7			7			7		μV/°C
Input Offset Current	$I_{IN}(+) - I_{IN}(-)$			30			30			75			±100			±150		45	±200	nA_{DC}
Input Offset Current Drift			10	200		10	200		10	300		10			10			10		pA_{DC}/°C
Input Bias Current	$I(+)$ or $I_{IN}(-)$		40	100		40	100		40	200		40	500		40	500		40	500	nA_{DC}
Input Common-Mode Voltage Range (Note 7)	$V^+ = 30V_{DC}$	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	0		V^+-2	V_{DC}
Large Signal Voltage Gain	$V^+ = +15V_{DC}$ (For Large V_O Swing) $R_L \geq 2k\Omega$	25			25			15			25			15			15			V/mV
Output Voltage Swing																				
V_{OH}	$V^+ = 30V_{DC}$, $R_L = 2k\Omega$	26			26			26			26			26			22			V_{DC}
	$R_L \geq 10k\Omega$	27	28		27	28		27	28		27	28		27	28		23	24		V_{DC}
V_{OL}	$V^+ = 5V_{DC}$, $R_L \leq 10k\Omega$		5	20		5	20		5	20		5	20		5	20		5	100	mV_{DC}
Output Current																				
Source	$V_{IN} = +1V_{DC}$, $V_{IN-} = 0V_{DC}$, $V^+ = 15V_{DC}$	10	20		10	20		10	20		10	20		10	20		10	20		mA
Sink	$V_{IN-} = +1V_{DC}$, $V_{IN^+} = 0V_{DC}$, $V^+ = 15V_{DC}$	10	15		5	8		5	8		5	8		5	8		5	8		mA
Differential Input Voltage	(Note 7)			V^+			V^+			V^+			V^+			V^+			V^+	V_{DC}

Note 1: For operating at high temperatures, the LM324/LM324A, LM2902 must be derated based on a +125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM224/LM224A and LM124/LM124A can be derated based on a +150°C maximum junction temperature. The dissipation is the total of all four amplifiers — use external resistors, where possible, to allow the amplifier to saturate or to reduce the power which is dissipated in the integrated circuit.

Note 2: Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 40mA independent of the magnitude of V^+. At values of supply voltage in excess of $+15V_{DC}$, continuous short-circuits can exceed the power dissipation ratings and cause eventual destruction. Destructive dissipation can result from simultaneous shorts on all amplifiers.

Note 3: This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parsitic transistor action on the IC chip. This transistor action can cause the output voltages of the op amps to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative again returns to a value greater than $-0.3V_{DC}$.

Note 4: These specifications apply for $V^+ = +5V_{DC}$ and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM224/LM224A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM324/LM324A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2902 specifications are limited to $-40°C \leq T_A \leq +85°C$.

Note 5: $V_O \cong 1.4V_{DC}$, $R_S = 0\Omega$ with V^+ from $5V_{DC}$ to $30V_{DC}$; and over the full input common-mode range ($0V_{DC}$ to $V^+ - 1.5V_{DC}$).

Note 6: The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the input lines.

Note 7: The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is $V^+ - 1.5V$, but either or both inputs can go to $+32V_{DC}$ without damage ($+26V_{DC}$ for LM2902).

Note 8: Due to proximity of external components, insure that coupling is not originating via stray capacitance between these external parts. This typically can be detected as this type of capacitive increases at higher frequencies.

TYPICAL PERFORMANCE CHARACTERISTICS

INPUT VOLTAGE RANGE

INPUT CURRENT

SUPPLY CURRENT

VOLTAGE GAIN

OPEN LOOP FREQUENCY RESPONSE

COMMON MODE REJECTION RATIO

VOLTAGE FOLLOWER PULSE RESPONSE

VOLTAGE FOLLOWER PULSE RESPONSE (SMALL SIGNAL)

LARGE SIGNAL FREQUENCY RESPONSE

OUTPUT CHARACTERISTICS CURRENT SOURCING

OUTPUT CHARACTERISTICS CURRENT SINKING

CURRENT LIMITING

5

ICL741/AD741/ LM741/μA741 Operational Amplifiers

GENERAL DESCRIPTION

The 741 and 741C are general purpose operational amplifiers which feature improved performance over industry standards like the LM709. They are direct, plug-in replacements for the 709C, LM201, MC1439 and 748 in most applications.

The offset voltage and offset current are guaranteed over the entire common mode range. The amplifiers also offer many features which make their application nearly foolproof: overload protection on the input and output, no latch-up when the common mode range is exceeded, as well as freedom from oscillations.

The 741C is identical to the 741 except that the 741C has its performance guaranteed over a 0°C to 70°C temperature range, instead of −55°C to 125°C.

CONNECTION DIAGRAMS

TO-99 METAL CAN

TOP VIEW

NOTE: PIN 4 CONNECTED TO CASE

8 PIN MINIDIP

NOTE: PIN 4 CONNECTED TO BOTTOM OF PACKAGE

10 PIN FLATPACK

14 PIN PLASTIC, CERDIP

	TO-99 CAN (TY)	8-PIN MINIDIP (PA)	14 PIN PLASTIC (PD)	14 PIN CERDIP (JD)	10 PIN FLATPACK (FB)
LM741 LM741C	LM741H LM741CH	LM741CN	LM741CN-14	LM741J LM741CJ	LM741CJ
μA741 μA741C	μA741HM μA741HC	μA741TC	μA741PC	μA741DM μA741DC	μA741FM
AD741 AD741C	AD741H AD741CH	AD741CN			
ICL741 ICL741C	ICL741MTY ICL741CTY	ICL741CPA	ICL741CPD	ICL741MJD ICL741CJD	ICL741MFB

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage 741	±22V
741C	±18V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Output Short Circuit Duration	Indefinite
Operating Temperature Range 741	−55°C to 125°C
741C	0°C to 70°C
Storage Temperature Range	−65°C to 150°C
Lead Temperature (Soldering, 10 sec)	300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS	741			741C			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	$T_A = 25°C$, $R_S < 10\ k\Omega$		1.0	5.0		1.0	6.0	mV
Input Offset Current	$T_A = 25°C$		30	200		30	200	nA
Input Bias Current	$T_A = 25°C$		200	500		200	500	nA
Input Resistance	$T_A = 25°C$	0.3	1.0		0.3	1.0		MΩ
Supply Current	$T_A = 25°C$, $V_S = \pm15V$		1.7	2.8		1.7	2.8	mA
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm15V$ $V_{OUT} = \pm10V$, $R_L > 2\ k\Omega$	50	160		25	160		v/mV
Input Offset Voltage	$R_S < 10\ k\Omega$			6.0			7.5	mV
Input Offset Current				500			300	nA
Input Bias Current				1.5			0.8	μA
Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$ $R_L > 2\ k\Omega$	25			15			V/mV
Output Voltage Swing	$V_S = \pm15V$, $R_L = 10\ k\Omega$ $R_L = 2\ k\Omega$	±12 ±10	±14 ±13		±12 ±10	±14 ±13		V V
Input Voltage Range	$V_S = \pm15V$	±12			±12			V
Common Mode Rejection Ratio	$R_S < 10\ k\Omega$	70	90		70	90		dB
Supply Voltage Rejection Ratio	$R_S < 10\ k\Omega$	77	96		77	96		dB

Note 1: The maximum junction temperature of the 741 if 150°C, while that of the 741C is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to case.
Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
Note 3: These specifications apply for $V_S = \pm15V$ and $-55°C \le T_A \le 125°C$, unless otherwise specified. With the 741C, however, all specifications are limited to $0°C \le T_A \le 70°C$ and $V_S = \pm15V$.

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SCHEMATIC DIAGRAM

INTERSIL

LM748/LM748C
μA748/μA748C
Operational Amplifier

FEATURES

- **Short-circuit protection**
- **Offset voltage null capability**
- **Large common-mode and differential voltage ranges**
- **Low power consumption**
- **No latch up**

GENERAL DESCRIPTION

The 748 is a High Performance Monolithic Operational Amplifier and is intended for a high wide range of analog applications where tailoring of frequency characteristics is desirable. High common mode voltage range and absence of latch-up make the 748 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in integrator, summing amplifier, and general feedback applications. The 748 is short-circuit protected and has the same pin configuration as the popular 741 operational amplifier. Unity gain frequency compensation is achieved by means of a single 30 pF capacitor. For superior performance, see 777 data sheet.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22 V
Internal Power Dissipation (Note 1)	
Metal Can	500 mW
DIP	670 mW
Mini DIP	310 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Storage Temperature Range	
Metal Can, DIP	−65°C to +150°C
Mini DIP	−55°C to +125°C
Operating Temperature Range	
Military (748)	−55°C to +125°C
Commercial (748C)	0°C to +70°C
Lead Temperature (Soldering, 60 Seconds)	
Metal Can	300°C
Molded DIPs	260°C
Output Short Circuit Duration (Note 3)	Indefinite

NOTES:
1. Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3 mW/°C for metal can, 8.3 mW/°C for the DIP and 5.6 mW/°C for the mini DIP.
2. For supply voltages less than ±15V, absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

CONNECTION DIAGRAMS

8-LEAD MINI DIP

8-LEAD METAL CAN

NOTE: Pin 4 connected to case

14-LEAD DIP

(TOP VIEW)

ORDERING INFORMATION

	8-Lead Metal Can	8-Lead Mini DIP	14-Lead DIP
μA748 μA748A μA748C	μA748HM μA748AHM μA748HC	 μA748TC	μA748DM μA748ADM μA748DC
LM748 LM748C	LM748H LM748CH	LM748N LM748CN	

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748 ELECTRICAL CHARACTERISTICS ($V_S = \pm 15$ V, $T_A = 25°C$, $C_C = 30$ pF unless otherwise specified)

PARAMETERS (see definitions)		CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	5.0	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2.0		MΩ
Input Capacitance				2.0		pF
Offset Voltage Adjustment Range				±15		mV
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	50,000	150,000		V/V
Output Resistance				75		Ω
Output Short-Circuit Current				25		mA
Supply Current				1.9	2.8	mA
Power Consumption				60	85	mW
Transient Response (Voltage Follower, Gain of 1)	Rise Time	$V_{IN} = 20$ mV, $C_C = 30$ pF, $R_L = 2$ kΩ, $C_L \leq 100$ pF		0.3		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)		$R_L \geq 2$ kΩ		0.5		V/μs
Transient Response (Voltage Follower, Gain of 10)	Rise Time	$V_{IN} = 20$ mV, $C_C = 3.5$ pF, $R_L = 2$ kΩ, $C_L \leq 100$ pF		0.2		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)		$R_L \geq 2$ kΩ, $C_C = 3.5$ pF		5.5		V/μs
The following specifications apply for $-55°C \leq T_A \leq +125°C$:						
Input Offset Voltage		$R_S \leq 10$ kΩ		1.0	6.0	mV
Input Offset Current		$T_A = +125°C$		10	200	nA
		$T_A = -55°C$		50	500	nA
Input Bias Current		$T_A = +125°C$		0.03	0.5	μA
		$T_A = -55°C$		0.3	1.5	μA
Input Voltage Range			±12	±13		V
Common Mode Rejection Ratio		$R_S \leq 10$ kΩ	70	90		dB
Supply Voltage Rejection Ratio		$R_S \leq 10$ kΩ		30	150	μV/V
Large Signal Voltage Gain		$R_L \geq 2$ kΩ, $V_{OUT} = \pm 10$ V	25,000			V/V
Output Voltage Swing		$R_L \geq 10$ kΩ	±12	±14		V
		$R_L \geq 2$ kΩ	±10	±13		V
Supply Current		$T_A = +125°C$		1.5	2.5	mA
		$T_A = -55°C$		2.0	3.3	mA
Power Consumption		$T_A = +125°C$		45	75	mW
		$T_A = -55°C$		60	100	mW

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VOLTAGE OFFSET NULL CIRCUIT

SUGGESTED ALTERNATE

GAIN TEST CIRCUIT

748C ELECTRICAL CHARACTERISTICS (V_S = ±15 V, T_A = 25°C, C_C = 30 pF unless otherwise specified)

PARAMETERS		CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage		$R_S \leq 10\ k\Omega$		2.0	6.0	mV
Input Offset Current				20	200	nA
Input Bias Current				80	500	nA
Input Resistance			0.3	2.0		MΩ
Input Capacitance				2.0		pF
Offset Voltage Adjustment Range				±15		mV
Large Signal Voltage Gain		$R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	20,000	150,000		V/V
Output Resistance				75		Ω
Output Short-Circuit Current				25		mA
Supply Current				1.9	2.8	mA
Power Consumption				60	85	mW
Transient Response (Voltage Follower, Gain of 1)	Rise Time	V_{IN} = 20 mV, C_C = 30 pF, R_L = 2 kΩ, $C_L \leq 100$ pF		0.3		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)		$R_L \geq 2\ k\Omega$		0.5		V/μs
Transient Response (Voltage Follower, Gain of 10)	Rise Time	V_{IN} = 20 mV, C_C = 3.5 pF, R_L = 2 kΩ, $C_L \leq 100$ pF		0.2		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)		$R_L \geq 2\ k\Omega$, C_C = 3.5 pF		5.5		V/μs
The following specifications apply for 0°C ≤ T_A ≤ +70°C:						
Input Offset Voltage		$R_S \leq 10\ k\Omega$			7.5	mV
Input Offset Current					300	nA
Input Bias Current					800	nA
Input Voltage Range			±12	±13		V
Common Mode Rejection Ratio		$R_S \leq 10\ k\Omega$	70	90		dB
Supply Voltage Rejection Ratio		$R_S \leq 10\ k\Omega$		30	150	μV/V
Large Signal Voltage Gain		$R_L \geq 2\ k\Omega$, V_{OUT} = ±10 V	15,000			V/V
Output Voltage Swing		$R_L \leq 10\ k\Omega$	±12	±14		V
		$R_L \geq 2\ k\Omega$	±10	±13		V
Power Consumption				60	100	mW

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EQUIVALENT CIRCUIT

TYPICAL PERFORMANCE CURVES FOR 748

INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

TYPICAL PERFORMANCE CURVES FOR 748C

INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

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TYPICAL PERFORMANCE CURVES FOR 748 AND 748C

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE

OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

FREQUENCY CHARACTERISTICS AS A FUNCTION OF SUPPLY VOLTAGE

748 FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

748C FREQUENCY CHARACTERISTICS AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

INPUT NOISE CURRENT AS A FUNCTION OF FREQUENCY

BROAD BAND NOISE FOR VARIOUS BANDWIDTHS

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TYPICAL PERFORMANCE CURVES FOR 748 AND 748C

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY FOR VARIOUS GAIN/COMPENSATION OPTIONS

FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS

COMPENSATION CAPACITANCE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN

INPUT RESISTANCE AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY

OUTPUT RESISTANCE AS A FUNCTION OF FREQUENCY

COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY

VOLTAGE FOLLOWER TRANSIENT RESPONSE (GAIN OF 1)

TRANSIENT RESPONSE TEST CIRCUIT

VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE

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TYPICAL PERFORMANCE CURVES FOR 748 AND 748C

FEED FORWARD COMPENSATION

LARGE SIGNAL FEED FORWARD TRANSIENT RESPONSE

TYPICAL APPLICATIONS

PULSE WIDTH MODULATOR

$$f_c = \frac{1}{2\pi R_2 C1}$$

$$f_n = \frac{1}{2\pi R_1 C1} = \frac{1}{2\pi R_2 C2}$$

$$f_c < f_n < f_{unity\ gain}$$

PRACTICAL DIFFERENTIATOR

CIRCUIT FOR OPERATING THE 748 WITHOUT A NEGATIVE SUPPLY

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PACKAGE DIMENSIONS

8 LEAD PLASTIC MINI DIP (PA)

8 LEAD TO-99 METAL CAN (TY)

Note: Pin 4 connected to case.

14 LEAD PLASTIC (PD)

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μA777C
Precision Operational Amplifier

FEATURES

- **Low offset voltage and offset current**
- **Low offset voltage and current drift**
- **Low input bias current**
- **Low input noise voltage**
- **Large common mode and differential voltage ranges**

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	
Metal Can	500mW
DIP	670mW
Mini DIP	310mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Storage Temperature Range	
Metal Can and Hermetic DIP	−65°C to +150°C
Mini DIP	−55°C to +125°C
Operating Temperature Range	0°C to 70°C
Lead Temperature	
Metal Can and Hermetic DIP (Soldering, 60s)	300°C
Mini DIP (Soldering, 10s)	260°C
Output Short Circuit Duration (Note 3)	Indefinite

Note 1: Rating applies to ambient temperatures up to 70°C. Above 70°C ambient derate linearly at 6.3mW/°C for Metal Can, 8.3mW/°C for the DIP, and 5.6mW/°C for the Mini DIP.

Note 2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

Note 3. Short Circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature for $I_{SET} \leq 30\mu A$.

GENERAL DESCRIPTION

The μA777C is a monolithic Precision Operational Amplifier. It is an excellent choice when performance versus cost trade-offs are possible between super beta or FET input operational amplifiers and low cost general purpose operational amplifiers. Low offset and bias currents improve system accuracy when used in applications such as long term integrators, sample and hold circuits and high source impedance summing amplifiers. Even though the input bias current is extremely low, the μA777C maintains full ±30V differential voltage range. High common mode input voltage range, latch-up protection, short circuit protection and simple frequency compensation make the device versatile and easily used.

CONNECTION DIAGRAMS

8-LEAD METAL CAN
(TOP VIEW)

ORDER INFORMATION

TYPE	PART NO.
μA777C	μA777HC

CONNECTION DIAGRAM

8-LEAD MINI DIP
(TOP VIEW)

ORDER INFORMATION

TYPE	PART NO.
μA777C	μA777TC

PIN CONFIGURATION

14-LEAD DIP
(TOP VIEW)

ORDER INFORMATION

TYPE	PART NO.
μA777C	μA777DC

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ELECTRICAL CHARACTERISTICS FOR μA777C (V_S = ±15V, T_A = 25°C, C_C = 30pF unless otherwise specified)

PARAMETERS		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 50k\Omega$		0.7	5.0	mV
Input Offset Current				0.7	20.0	nA
Input Bias Current				25	100	nA
Input Resistance			1.0	2.0		MΩ
Input Capacitance				3.0		pF
Offset Voltage Adjustment Range				±25		mV
Large Signal Voltage Gain		$R_L \geq 2k\Omega$, V_{OUT} = ±10V	25,000	250,000		V/V
Output Resistance				100		Ω
Output Short Circuit Current				±25		mA
Supply Current				1.9	2.8	mA
Power Consumption				60	85	mW
Transient Response (Voltage Follower, Gain of 1)	Rise Time	V_{IN} = 20mV, C_C = 30pF, R_L = 2kΩ, $C_L \leq$ 100pF		0.3		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 1)		$R_L \geq 2k\Omega$		0.5		V/μs
Transient Response (Voltage Follower, Gain of 10)	Rise Time	V^{IN} = 20mV, C_C = 3.5pF, R_L = 2kΩ, $C_L \leq$ 100pF		0.3		μs
	Overshoot			5.0		%
Slew Rate (Voltage Follower, Gain of 10)		$R_L \leq 2k\Omega$, C_C = 3.5pF		5.5		V/μs
The following specifications apply for 0°C ≤ T_A ≤ +70°C						
Input Offset Voltage		$R_S \leq 50k\Omega$		0.8	5.0	mV
Average Input Offset Voltage Drift		$R_S \leq 50k\Omega$		4.0	30	μV/°C
Input Offset Current					40	nA
Average Input Offset Current Drift		25°C ≤ T_A ≤ +70°C		0.01	10.3	nA/°C
		0°C ≤ T_A ≤ +25°C		0.02	0.6	nA/°C
Input Bias Current					200	nA
Input Voltage Range			±12	±13		V
Common Mode Rejection Ratio		$R_S \leq 50k\Omega$	70	95		dB
Supply Voltage Rejection Ratio		$R_S \leq 50k\Omega$		15	150	μV/V
Large Signal Voltage Gain		$R_L \geq 2k\Omega$, V_{OUT} = ±10V	15,000			V/V
Output Voltage Swing		$R_L \geq 10k\Omega$	±12	±14		V
		$R_L \geq 2k\Omega$	±10	±13		V
Power Consumption				60	100	mW

5

EQUIVALENT CIRCUIT

TYPICAL PERFORMANCE CURVES

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

INPUT COMMON MODE VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

POWER CONSUMPTION AS A FUNCTION OF SUPPLY VOLTAGE

INPUT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT RESISTANCE AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT OFFSET CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT VOLTAGE SWING AS A FUNCTION OF LOAD RESISTANCE

OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT NOISE VOLTAGE AND CURRENT AS A FUNCTION OF FREQUENCY

5

TYPICAL PERFORMANCE CURVES

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY FOR VARIOUS GAIN/COMPENSATION OPTIONS

FREQUENCY RESPONSE FOR VARIOUS CLOSED-LOOP GAINS

COMPENSATION CAPACITANCE AS A FUNCTION OF CLOSED LOOP VOLTAGE GAIN

INPUT RESISTANCE, OUTPUT RESISTANCE, AND INPUT CAPACITANCE AS A FUNCTION OF FREQUENCY

COMMON MODE REJECTION RATIO AS A FUNCTION OF FREQUENCY

INPUT OFFSET VOLTAGE DRIFT AS A FUNCTION OF TIME

VOLTAGE FOLLOWER TRANSIENT RESPONSE (GAIN OF 1)

TRANSIENT RESPONSE TEST CIRCUIT

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

5

TYPICAL PERFORMANCE CURVES

THERMAL RESPONSE OF INPUT OFFSET VOLTAGE TO STEP CHANGE OF CASE TEMPERATURE

STABILIZATION TIME OF INPUT OFF—SET VOLTAGE FROM POWER TURN-ON

FEED FORWARD COMPENSATION

LARGE SIGNAL FEEDFORWARD TRANSIENT RESPONSE

VOLTAGE OFFSET NULL CIRCUIT

SUGGESTED

ALTERNATE

GAIN TEST CIRCUIT

TYPICAL APPLICATIONS

BIAS COMPENSATED LONG TIME INTEGRATOR

*ADJUST R_3 FOR MINIMUM INTEGRATOR DRIFT

SAMPLE AND HOLD

CAPACITANCE MULTIPLIER

$$C = \frac{R_1}{R_3} C_1$$

$$I_L = \frac{V_{OS} + I_{OS} R_1}{R_3}$$

$$R_S = R_3$$

AMPLIFIER FOR CAPACITANCE TRANSDUCERS

LOW FREQUENCY CUTOFF $R_1 \times C_1$

BILATERAL CURRENT SOURCE

$$I_{OUT} = \frac{R_3 V_{IN}}{R_1 R_5} \; ; R_1 = R_2; R_3 = R_4 + R_5$$

HIGH SLEW RATE POWER AMPLIFIER

±100V COMMON MODE RANGE INSTRUMENTATION AMPLIFIER

$$\frac{R_1}{R_7} \equiv \frac{R_3}{R_4} \text{ for best CMRR}$$

$$R_3 \approx R_4$$

$$R_1 = R_6 = 10R_3$$

$$\text{Gain} = \frac{R_7}{R_6}$$

INSTRUMENTATION AMPLIFIER WITH HIGH COMMON MODE REJECTION

$$\frac{R_2}{R_5} \equiv \frac{R_6}{R_7} \text{ for best CMRR}$$

$$\frac{R_1}{R_2} = \frac{R_4}{R_5}$$

$$\text{Gain} = \frac{R_6}{R_2}\left(1 + \frac{2R_1}{R_3}\right)$$

5

INTERSIL

AD503
High Accuracy Low Offset Op Amp

FEATURES

- **Low I_{BIAS}: 15pA MAX**
- **Low Drift: 25μV°C MAX**

GENERAL DESCRIPTION

The AD503 is an IC FET input op amp which provides the user with input currents of a few pA, high overall performance, low cost, and accurately specified, predictable operation. The device achieves maximum bias currents as low as 5pA, minimum gain of 75,000, CMRR of 80dB, and a minimum slew rate of 3V/μs. It is free from latch-up and is short circuit protected, and no external compensation is required, as the internal 6dB/octave rolloff provides stability in closed loop applications.

The AD503 is suggested for all general purpose FET input amplifier requirements where low cost is of prime importance.

The circuits are supplied in the TO-99 package; the AD503J, K are specified for 0 to +70°C temperature range operation; the AD503S for operation from −55°C to +125°C.

It provides performance comparable to modular FET op amps, but because of its monolithic construction, however, its cost is significantly below that of modules, and becomes even lower in large quantities.

The AD503 is especially designed for applications involving the measurement of low level currents or small voltages from high impedance sources, in which bias current can be a primary source of error. Input bias current contributes to error in two ways: (1) in current measuring configurations, the bias current limits the resolution of a current signal; (2) the bias current produces a voltage offset which is proportional to the value of input resistance (in the case of an inverting configuration) or source impedance (when the noninverting "buffer" connection is used). The AD503, therefore, is of use where small currents are to be measured or where relatively low voltage drift is necessary despite large values of source resistance.

OUTLINE DIMENSIONS

Dimensions shown in inches and *(mm)*.

PIN CONFIGURATION

5

SPECIFICATIONS (Typical @ +25°C and ±15Vdc, unless otherwise noted)

PARAMETER	AD503J	AD503K	AD503S
OPEN LOOP GAIN[1]			
V_{OUT} = ±10V, $R_L \geq 2k\Omega$	20,000 min (50,000 typ)	50,000 min (120,000 typ)	**
T_A = min to max	15,000 min	40,000 min	25,000 min
OUTPUT CHARACTERISTICS			
Voltage @ R_L = 2kΩ, T_A = min to max	±10V min (±13V typ)	*	*
Voltage @ R_L = 10kΩ, T_A = min to max	±12V min (±14V typ)	*	*
Load Capacitance[2]	750pF	*	*
Short Circuit Current	25mA	*	*
FREQUENCY RESPONSE			
Unity Gain, Small Signal	1.0MHz	*	*
Full Power Response	100kHz	*	*
Slew Rate, Unity Gain	3.0V/μs min (6.0V/μs typ)	*	*
Settling Time, Unity Gain (to 0.1%)	10μs	*	*
INPUT OFSET VOLTAGE[3]	50mV max (20mV typ)	20mV max (8mV typ)	**
vs Temperature, T_A = min to max	75μV/°C max (30μV/°C typ)	25μV/°C max (10μV/°C typ)	50μV°C max (20μV/°C typ)
vs Supply, T_A = min to max	400μV/V max (200μV/V typ)	200μV/V max (100μV/V typ)	**
INPUT BIAS CURRENT			
Either Input[4]	15pA max (5pA typ)	10pA max (2.5pA typ)	**
INPUT IMPEDANCE			
Differential	10^{11} Ω‖2pF	*	*
Common Mode	10^{12} Ω‖2pF	*	*
INPUT NOISE			
Voltage, 0.1Hz to 10Hz	15μV (p-p)	*	*
5Hz to 50kHz	5.0μV (rms)	*	*
f = 1kHz (spot noise)	30.0nV/√Hz	*	*
INPUT VOLTAGE RANGE			
Differential[5]	±3.0V	*	*
Common Mode, T_A = min to max	±10V min (±12V typ)	*	*
Common Mode Rejection, V_{IN} = ±10V	70dB min (90dB typ)	80dB min (90dB typ)	**
POWER SUPPLY			
Rated Performance	±15V	*	*
Operating	±(5 to 18)V	*	±(5 to 22)V
Quiescent Current	7mA max (3mA typ)	*	*
TEMPERATURE			
Operating, Rated Performance	0 to +70°C	*	−55°C to +125°C
Storage	−65°C to +150°C	*	*

Note 1. Open Loop Gain is specified with V_{OS} both nulled and unnulled.

Note 2. A conservative design would not exceed 500pF of load capacitance.

Note 3. Input offset voltage specifications are guaranteed after 5 minutes of operation at T_A = +25°C.

Note 4. Bias current specifications are guaranteed after 5 minutes of operation at T_A = +25°C. For higher temperatures, the current doubles every 10°C.

Note 5. See comments in Input Considerations section.

*Specifications same as for AD503J.
**Specifications same as for AD503K.
Specifications subject to change without notice.

APPLICATIONS CONSIDERATIONS

Bias Current

Most IC FET op amp manufacturers specify maximum bias currents as the value immediately after turn-on. Since FET bias currents double every 10°C and since most FET op amps have case temperature increases of 15°C to 20°C above ambient, initial "maximum" readings may be only ¼ of the true warmed up value. Furthermore, most IC FET op amp manufacturers specify I_b as the average of both input currents, sometimes resulting in twice the "maximum" bias current appearing at the input being used. The total result is that 8X the expected bias current may appear at either input terminal in a warmed up operating unit.

The AD503 specifies maximum bias currents at either input after warmup, thus giving the user the values he expected.

Improving Bias Current Beyond Guaranteed Values

Bias currents can be substantially reduced by decreasing the junction temperature of the device. One technique to accomplish this is to reduce the operating supply voltage. This procedure will decrease the power dissipation of the device, which will in turn result in a lower junction temperature and lower bias currents. The supply voltage effect on bias current is shown in Figure 1.

Figure 1. Normalized Bias Current vs Supply Voltage

Operation of the AD503K at ±5V reduces the warmed up bias current by 70% to a typical value of 0.75pA.

A second technique is the use of a suitable heat sink. Wakefield Engineering Series 200 heat sinks were selected to demonstrate this effect. The characteristic bias current vs case temperature above ambient is shown in Figure 2. Bias current has been normalized with unity representing the 25°C free air reading.

Figure 2. Normalized Bias Current vs Case Temperature

Note that the use of the model 209 heat sink reduces warmed up bias current by 60% to 1.0pA in the AD503K.

Both of these techniques may be used together for obtaining lower bias currents. Remember that loading the output can also affect the power dissipation.

Figure 3. Input Bias Current vs Temperature

Input Considerations

The common mode input characteristic is shown in Figure 4. Note that positive common mode inputs up to +13.5 Volts and negative common mode inputs to –Vs are permissible, without incurring excessive bias currents. To prevent possible damage to the unit, do not exceed V_{CM} = V_S.

Figure 4. Input Bias Current vs Common Mode Voltage

Like most other FET input op amps, the AD503 displays a degraded bias current specification when operated at moderate differential input voltages. It maintains its specified bias current up to a differential input voltage of ±3V typically, while the bias current will increase to approximately 400μA. This is not a failure mode. Above ±10V differential input voltage, the bias current will increase 100μA/V_{diff} (in volts), and other parameters may suffer degradation.

INTERSIL

ICH8500/ICH8500A Ultra Low Bias Current Operational Amplifier

FEATURES

- Input diode protection
- Input bias current less than 0.01 pA at all operating temperatures
- No frequency compensation required
- Offset voltage null capability
- Short circuit protection
- Low power consumption

SCHEMATIC DIAGRAM

CONNECTION DIAGRAM

(TOP VIEW)

NOTE: Pin 4 is not connected to case.

GENERAL DESCRIPTION

The ICH 8500 and ICH 8500A are hybrid circuits designed for ultra low input bias current operational amplifier applications. They are ideally suited for analog and electrometer applications where high input resistance and low input current are of prime importance.

APPLICATIONS

- Femto Ammeter
- Electrometers
- Long time integrators
- Flame detectors
- pH meter
- Proximity detector

ORDERING INFORMATION

ICH 8500A TV

- TV — PACKAGE (See Outline Drawing)
- 8500A — DEVICE TYPE
- ICH — INTERSIL HYBRID CIRCUIT

PACKAGE OUTLINE

TV PACKAGE

NOTES:
All dimensions in inches. Dimensions as per latest J-10 committee. Leads are gold plated Kovar. Package weight is 1.22 grams.

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MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Voltage	±0.5V
Storage Temperature	−65°C to +150°C
Operating Temperature	−25°C to +85°C
Lead Temperature (Soldering 60 sec)	300°C
Output Short Circuit Duration	Indefinite

NOTE:
1. Rating applies for ambient temperature to +70°C.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise specified, V_S = ±15V)

CHARACTERISTICS	ICH8500 MIN	ICH8500 TYP	ICH8500 MAX	ICH8500A MIN	ICH8500A TYP	ICH8500A MAX	UNITS	TEST CONDITIONS
Input Leakage Current (Inverting and Non-Inverting)			0.1			0.01	pA	Case at same potential as inputs
Input Offset Voltage			50			50	mV	
Offset Voltage Adjustment Range			±50			±50	mV	20kΩ Potentiometer
Change in Input Offset Voltage Over Temperature						±5.0 ±5.0	mV mV	+25 to +85°C −25 to +25°C
Common Mode Rejection Ratio	60	75		60	75		dB	±5 volts common mode voltage
Output Voltage Swing	±11			±11			V	$R_L \geqslant 10k\Omega$
Common Mode Voltage Range	±10			±10			V	
Large Signal Voltage Gain	20,000	10^5		20,000	10^5		—	
Feedback Capacitance			0.1			0.1	pF	Case guarded
Long Term Input Offset Voltage Stability			±3.0			±3.0	mV	At 25°C
Slew Rate		0.5			0.5		V/μs	$R_L \geqslant 2k\Omega$

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CIRCUIT NOTES

VOLTAGE OFFSET NULL CIRCUIT

VOLTAGE FOLLOWER

LOW LEVEL CURRENT MEASURING CIRCUIT

NOTE: Adjust input offset voltage to 0mV ±1mV before measuring leakage.

TYPICAL PERFORMANCE CURVES

OPEN LOOP VOLTAGE GAIN VERSUS FREQUENCY

INPUT VOLTAGE RANGE VERSUS SUPPLY VOLTAGE

COMMON MODE REJECTION RATIO VERSUS SUPPLY VOLTAGE

INPUT OFFSET VOLTAGE VERSUS SUPPLY VOLTAGE

± POWER SUPPLY REJECTION RATIO VERSUS SUPPLY VOLTAGE

OUTPUT VOLTAGE SWING VERSUS SUPPLY VOLTAGE

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± QUIESCENT SUPPLY CURRENT VERSUS SUPPLY VOLTAGE

INPUT REFERRED NOISE VOLTAGE

POWER CONSUMPTION VERSUS SUPPLY VOLTAGE

BASIC CHARACTERISTICS

The ICH8500 and ICH8500A are packaged in a TO-5 eight lead header. Functionally, they are pin for pin identical to the popular 741 monolithic amplifier. These amplifiers are unconditionally stable and the input offset voltage can be adjusted to zero with an external 20k potentiometer. The input bias current for the inverting and non-inverting inputs is 0.1 pA maximum for the ICH8500, and 0.01 pA maximum for the ICH8500A. In addition, the input bias currents of the ICH8500 and ICH8500A are constant over the operating temperature range from −25°C to +85°C. Like the 741, the slew rate of these two amplifiers is about 0.5 volts per μs. Unlike the 741 and other monolithic amplifiers, Pin 4 (the negative supply voltage terminal) is not connected to the case; however Pin 8 is connected to the case. This permits the designer to operate the case at any desired potential. This feature is the key to achieving the ultra low input currents associated with these two amplifiers. Forcing the case to the same potential as the inputs eliminates any current flow between the case and the input pins. In addition, any leakage currents that may otherwise have existed between any of the other pins and the inputs are intercepted by the case. This is possible since the case completely encircles every pin on the header, thus the case acts as a guard against any stray leakage currents.

APPLICATIONS

I. The Pico Ammeter

A very sensitive pico ammeter can be constructed with the ICH8500. The basic circuit (illustrated in Figure 1) employs the amplifier in the inverting or current summing mode.

Care must be taken to eliminate any stray currents from flowing into the current summing node. This can be accomplished by forcing all points surrounding the input to the same potential as the input. In this case, the potential of the input is at virtual ground, or 0V. The case of the device is, therefore, grounded to intercept any stray leakage currents that may otherwise exist between the ±15V input terminals and the inverting input summing junctions. Feedback capacitance* should also be minimized, in the pico ammeter, in order to maximize the response time of the circuit to step function input currents. The time constant of the circuit is approximately the product of the feedback capacitance C_{FB} times to feedback resistor R_{FB}. For instance, the time constant of the circuit in Figure 1 is 1 sec if C_S = 1 pF. Thus, it takes approximately 5 sec (5 time constants) for the circuit to stabilize to within 1% of its final output voltage after a step function of input current has been applied. C_{FB} of less than 0.2 to 0.3 pF can be achieved with proper circuit layout. A practical pico ammeter circuit is illustrated in Figure 2.

CR1, CR2 are internal diodes, along with R1 which protect the input stage of the amplifier from voltage transients. CR1 and CR2 are low leakage, high impedance diodes. These diodes do not, however, contribute any error currents, since there is zero volts potential across them under normal operating conditions.

*Feedback capacitance is the capacitance between the output and the inverting input terminal of the amplifier.

FIGURE 1. BASIC PICO AMMETER CIRCUIT.

FIGURE 2. PICO AMMETER CIRCUIT.

II. Sample and Hold Circuit

The circuit illustrated in Figure 3 is a sample and hold circuit employing the ICH8500. The basic principal of this circuit is to rapidly charge a capacitor C_S to a voltage equal to an input signal. The input signal is then electrically disconnected from the capacitor with the charge still remaining on C_S. Since C_S is in the negative feedback loop of an operational amplifier, the output voltage of the amplifier is equal to the voltage across the capacitor. Ideally, the voltage across C_S will remain constant, thus the output of the amplifier will also be constant. The voltage across C_S will, however decay at a rate proportional to the current being injected or taken out of the current summing node of the amplifier. This current can come from four sources: leakage resistance of C_S, leakage current due to the solid state switch SW2, currents due to high resistance paths on the circuit fixture, and most important, bias current of the operational amplifier. If the ICH8500A operational amplifier is employed, this bias current is almost non-existant (<0.01 pA). Study of the sample and hold circuit will show that the voltage on the source, drain and gate of switch SW2 is zero or near zero when the circuit is in the hold mode. Since there is no voltage, there is no leakage current due to SW2. Careful construction will eliminate stray resistance paths and capacitor resistance can be eliminated if a quality capacitor is selected. The net result is a quality sample and hold circuit.

As an example, suppose the leakage current due to all sources flowing into the current summing node of the sample and hold circuit is 100pA. The rate of change of the voltage across the 0.01 μF C_S capacitor is then 10mV/sec. In contrast, if an operational amplifier were employed that exhibited an input bias current of 1 nA, the rate of change of the voltage across C_S would be 0.1 V/sec. An error build up such as this could not be tolerated in most applications.

Wave forms illustrating the operation of the sample and hold circuit are illustrated in Figure 4.

III. The Gated Integrator

The circuit in Figure 3 can double as an integrator circuit. In this application the input voltage is applied to the integrator input terminal. The time constant of the circuit is the product of R1 and C_S. When the FET switch (SW2) is open, capacitor C_S charges at a rate equal to the current flowing through R1. Because of the low leakage current associated with the ICH8500 and ICH8500A, very large values of R1 (up to 10^{12} ohms) can be employed. This permits the use of small values of integrating capacitor (C_S) in applications that require long time delays. Waveforms for the integrator circuit are illustrated in Figure 5.

FIGURE 3. SAMPLE AND HOLD CIRCUIT OR INTEGRATOR CIRCUIT.

FIGURE 4. SAMPLE AND HOLD CIRCUIT WAVEFORMS.

FIGURE 5. GATED INTEGRATOR WAVEFORMS.

APPLICATION TIPS

This amplifier incorporates a pair of fast Ultra-Low Leakage back-to-back diodes at the amplifier inputs. The diodes do not interfere with the normal ultra-low input leakage currents of the amplifier.

These diodes will protect the amplifier inputs against static charge build-up damage and most transients. The diodes will not, however, react fast enough to ultra-high speed transients which may then damage the amplifier inputs.

When working with femto amp signals, teflon and ceramic should be used as insulators to keep leakage to a minimum. Teflon wire and ceramic switches should also be used along with metal film resistors.

The device input leakage resistance will adversely be affected by the package contamination. It is, therefore, recommended that the devices and finished assembly be washed in a freon bath for two minutes at a temperature of 50°C. Then baked in an oven for thirty minutes at +150°C.

ICL8007-1/-2/-3/-4/-5
FET Input Operational Amplifiers

FEATURES

- Very low input current – 1pA (max) 8007A
- Very low offset voltage – 2mV (max) 8007-1 & 8007-3
- Guaranteed low drift – 5μV/°C 8007-1
- High slew rate – 6V/μsec
- High input impedance – 1,000,000M ohm
- Internal frequency compensation

NOTE:

The 8007-1 thru -5 amplifiers are part of the 8007 family of FET-input op amps. See also the 8007C, 8007M data sheet.

GENERAL DESCRIPTION

The 8007 Series is a family of FET input operational amplifiers which provides a broad range of both general purpose products and special selections. The selections include devices with input currents of 1pA (max) and offset voltages of 2.0mV (max).

All are pin compatible with the 741 and have output short circuit protection. A unique bootstrap circuit insures unusually good common mode rejection and prevents the excessive gate currents seen in the majority of FET input amplifiers at high common mode voltages.

CONNECTION DIAGRAMS

8007-1, 8007-2 and 8007-3 (Without Offset Null)

NOTE: Pin 4 connected to case

8007-4 and 8007-5 (With Offset Null)

NOTE: Pin 4 connected to case

5

EQUIVALENT CIRCUIT

VOLTAGE OFFSET NULL CIRCUIT (8007-4 and 8007-5 only)

TRANSIENT RESPONSE TEST CIRCUIT

8007M-2 AND 8007M-5
(Selected 8007s – Military Temp. Range)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Voltage between Offset Null and V^-	±0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C
Lead Temperature (Soldering, 60 sec.)	300°C
Output Short-Circuit Duration	Indefinite

NOTES:
1. Rating applies for case temperatures to 125°C; derate linearly at 6.5mW/°C for ambient temperatures above +75°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

For connections to 8007M-2, see connection diagram for 8007C-2, page 3.

For connections to 8007M-5, see connection diagram for 8007C-5, page 4.

ELECTRICAL CHARACTERISTICS (V_S = ±15V unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8007M-2 MIN	8007M-2 TYP	8007M-2 MAX	8007M-5 MIN	8007M-5 TYP	8007M-5 MAX	UNITS
The following specifications apply for T_A = 25°C:								
Input Offset Voltage	$R_S \leq 100k\Omega$		1.0	2.0		5.0	10	mV
Input Offset Current			0.5			0.5		pA
Input Current (either input)			2.0	10		2.0	10	pA
Input Resistance			10^6			10^6		MΩ
Input Capacitance			2.0			2.0		pF
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{out} = ±10V	50,000			50,000			V/V
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Current			3.4	5.2		3.4	5.2	mA
Power Consumption			102	156		102	156	mW
Slew Rate		3.0	6.0		3.0	6.0		V/μs
Unity Gain Bandwidth			1.0			1.0		MHz
Transient Response (Unity Gain)	$C_L \leq 100pF$, $R_L = 2k\Omega$							
Risetime			300			300		ns
Overshoot			10			10		%
The following specifications apply for −55°C ≤ T_A ≤ +125°C:								
Input Voltage Range		±10	±12		±10	±12		V
Common Mode Rejection Ratio		70	90		70	90		dB
Supply Voltage Rejection Ratio			70	300		70	300	μV/V
Large Signal Voltage Gain		25,000			25,000			V/V
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		V
Input Offset Voltage				3.5			11.5	mV
Input Current (either input)	T_A = +125°C		2.0	15		2.0	15	nA
Average Temperature Coefficient of Input Offset Voltage				15			15	μV/°C

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8007C-1, 8007C-2 AND 8007C-3
(Selected 8007s Without Offset Null — Commercial Temp. Range)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Voltage between Offset Null and V^-	±0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 sec.)	300°C
Output Short-Circuit Duration	Indefinite

NOTE:

For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

CONNECTION DIAGRAM

TOP VIEW

NOTE: Pin 4 connected to case

ELECTRICAL CHARACTERISTICS (V_S = ±15V unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8007C-1 & 8007C-2 MIN	TYP	MAX	8007C-3 MIN	TYP	MAX	UNITS
The following specifications apply for T_A = 25°C:								
Input Offset Voltage	$R_S \leq 100k\Omega$		1.0	2.0		1.0	4.0	mV
Input Offset Current			0.5			0.5		pA
Input Current (either input)			2.0	10		2.0	20	pA
Input Resistance			10^6			10^6		MΩ
Input Capacitance			2.0			2.0		pF
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{out} = ±10V	50,000			50,000			V/V
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Current			3.4	6.0		3.4	6.0	mA
Power Consumption			102	180		102	180	mW
Slew Rate		3.0	6.0		3.0	6.0		V/μs
Unity Gain Bandwidth			1.0			1.0		MHz
Transient Response (Unity Gain)	$C_L \leq 100pF$, $R_L = 2k\Omega$							
Risetime			300			300		ns
Overshoot			10			10		%
The following specifications apply for 0°C ≤ T_A ≤ 70°C:								
Input Voltage Range		±10	±12		±10	±12		V
Common Mode Rejection Ratio		70	90		70	90		dB
Supply Voltage Rejection Ratio			70	300		70	300	μV/V
Large Signal Voltage Gain		25,000			25,000			V/V
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		V
Input Current (either input)	T_A = 70°C		50	175		50	400	pA
Average Temperature Coefficient of Input Offset Voltage								
8007-1				5				μV/°C
8007-2				15				μV/°C
8007-3							30	μV/°C

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8007C-4 AND 8007C-5
(Selected 8007s with Offset Null — Commercial Temp. Range)

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Voltage between Offset Null and V^-	±0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	0°C to +70°C
Lead Temperature (Soldering, 60 sec.)	300°C
Output Short-Circuit Duration	Indefinite

NOTE:

For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

CONNECTION DIAGRAM

TOP VIEW

NOTE: Pin 8 connected to case

ELECTRICAL CHARACTERISTICS (V_S = ±15V unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8007C-4 MIN	8007C-4 TYP	8007C-4 MAX	8007C-5 MIN	8007C-5 TYP	8007C-5 MAX	UNITS
The following specifications apply for T_A = 25°C:								
Input Offset Voltage	$R_S \leq 100k\Omega$		1.0	10		5.0	10	mV
Input Offset Current			0.5			0.5		pA
Input Current (either input)			2.0	10		2.0	10	pA
Input Resistance			10^6			10^6		MΩ
Input Capacitance			2.0			2.0		pF
Large Signal Voltage Gain	$R_L \geq 2k\Omega$, V_{out} = ±10V	50,000			50,000			V/V
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Current			3.4	6.0		3.4	6.0	mA
Power Consumption			102	180		102	180	mW
Slew Rate		3.0	6.0		3.0	6.0		V/μs
Unity Gain Bandwidth			1.0			1.0		MHz
Transient Response (Unity Gain)	$C_L \leq 100pF$, $R_L = 2k\Omega$							
Risetime			300			300		ns
Overshoot			10			10		%
The following specifications apply for 0°C ≤ T_A ≤ 70°C:								
Input Voltage Range		±10	±12		±10	±12		V
Common Mode Rejection Ratio		70	90		70	90		dB
Supply Voltage Rejection Ratio			70	300		70	300	μV/V
Large Signal Voltage Gain		25,000			25,000			V/V
Output Voltage Swing	$R_L \geq 10k\Omega$	±12	±14		±12	±14		V
	$R_L \geq 2k\Omega$	±10	±13		±10	±13		V
Input Current (either input)	T_A = 70°C		50	175		50	175	pA
Average Temperature Coefficient of Input Offset Voltage				10			15	μV/°C

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TYPICAL PERFORMANCE CURVES

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE

TRANSIENT RESPONSE

INPUT CURRENT AS A FUNCTION OF TEMPERATURE

OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

QUIESCENT SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

QUIESCENT SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY

WIDEBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE

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ORDERING INFORMATION

PART NUMBER	TEMP. RANGE	MAX. V_{OS} (mV)	MAX. $\Delta V_{OS}/\Delta T$ ($\mu V/^{\circ}C$)	MAX. I_b (pA)	PACKAGE
ICL8007C-1	0°C to +70°C	2	5	10	TO-99 Type
ICL8007M-2	–55°C to +125°C	2	15	10	TO-99 Type
ICL8007C-2	0°C to +70°C	2	15	10	TO-99 Type
ICL8007C-3	0°C to +70°C	4	30	20	TO-99 Type
ICL8007C-4	0°C to +70°C	10	10	10	TO-99 Type
ICL8007M-5	–55°C to +125°C	10	15	10	TO-99 Type
ICL8007C-5	0°C to +70°C	10	15	10	TO-99 Type

PACKAGE DIMENSIONS

NOTES: All dimensions in inches.
Leads are gold-plated Kovar.

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INTERSIL

ICL8007M/AM/C/AC
FET Input Operational Amplifier

GENERAL DESCRIPTION

The Intersil 8007 integrated circuit is a low input current FET input operational amplifier. The 8007A is selected for 1 pA max input current.

The devices are designed for use in very high input impedance applications. Because of their high slew rate, high common mode voltage range and absence of "latch-up", they are ideal for use as a voltage follower.

The Intersil 8007 and 8007A are short circuit protected. They require no external components for frequency compensation because the internal 6 dB/roll-off insures stability in closed loop applications. A unique bootstrap circuit insures unusually good commonmode rejection for an FET input amp and prevents large input currents as seen in some amplifiers at high common mode voltage.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
8007M, 8007AM	-55°C to +125°C
8007C, 8007AC	0°C to +70°C
Lead Temperature (Soldering, 10 sec.)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

NOTES:

1. Rating applies for case temperatures to 125°C; derate linearly at 6.5 mW/°C for ambient temperatures above +75°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
3. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

EQUIVALENT CIRCUIT

TRANSIENT RESPONSE TEST CIRCUIT

CONNECTION DIAGRAM

NOTE: Pin 4 connected to case

PACKAGE OUTLINE

NOTES: All dimensions in inches.
Leads are gold-plated Kovar.

ELECTRICAL CHARACTERISTICS (V_S = ±15V unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8007M			8007C			8007AM & 8007AC			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
The following specifications apply for T_A = 25°C:											
Input Offset Voltage	$R_S \leq 100\ k\Omega$		10	20		20	50		15	30	mV
Input Offset Current			0.5			0.5			0.2		pA
Input Current (either input)			2.0	20		3.0	50		0.5	1.0	pA
Input Resistance			10^6			10^6			10^6		MΩ
Input Capacitance			2.0			2.0			2.0		pF
Large Signal Voltage Gain	$R_L \geq 2\ k\Omega$, V_{OUT} = ±10V	50,000			20,000			20,000			V/V
Output Resistance			75			75			75		Ω
Output Short-Circuit Current			25			25			25		mA
Supply Current			3.4	5.2		3.4	6.0		3.4	6.0	mA
Power Consumption			102	156		102	180		102	180	mW
Slew Rate			6.0			6.0		2.5	6.0		V/μs
Unity Gain Bandwidth			1.0			1.0			1.0		MHz
Transient Response (Unity Gain)	$C_L \leq 100$ pF, R_L = 2 kΩ										
Risetime			300			300			300		ns
Overshoot			10			10			10		%
The following specifications apply for 0°C ≤ T_A ≤ +70°C (8007C and 8007AC), −55°C ≤ T_A ≤ +125°C (8007M and 8007AM):											
Input Voltage Range		±10	±12		±10	±12		±10	±12		V
Common Mode Rejection Ratio		70	90		70	90		86	95		dB
Supply Voltage Rejection Ratio			70	300		70	600		70	200	μV/V
Large Signal Voltage Gain		25,000			15,000			15,000			V/V
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±12	±14		±12	±14		±12	±14		V
	$R_L \geq 2\ k\Omega$	±10	±13		±10	±13		±10	±13		V
Input Current (either input)	T_A = +125°C		2.0						1.0		nA
	T_A = +70°C					50			30		pA
Average Temperature Coefficient of Input Offset Voltage				75			75			50	μV/°C

TYPICAL PERFORMANCE CURVES

OPEN LOOP VOLTAGE GAIN

VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

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INTERSIL

ICL8043M/C
Dual FET Input Operational Amplifier

FEATURES

- Low Cost
- Two High Performance FET Input Amplifiers in One Package.
- Very Low Input Current – 1 pA
- High Slew Rate – 6 V/μsec
- Internal Frequency Compensation

GENERAL DESCRIPTION

The 8043 is a dual monolithic FET input operational amplifier. The performance of each amplifier is similar to the Intersil 8007. It features exceptionally low input currents, high slew rate, and has excellent common mode rejection. The inputs and outputs are fully short circuit protected and there are no latch up problems. Offset nulling of each amplifier is accomplished using a potentiometer having its wiper connected to the positive supply voltage.

CONNECTION DIAGRAM

16 PIN DIP (TOP VIEW)

OFFSET VOLTAGE NULL CIRCUIT

EQUIVALENT CIRCUIT (One Side)

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18 V
Internal Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30 V
Input Voltage (Note 2)	±15 V
Voltage between Offset Null and V^+	±0.5 V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
8043M	−55°C to +125°C
8043C	0°C to +70°C
Lead Temperature (Soldering, 60 sec.)	300°C
Output Short-Circuit Duration	Indefinite

NOTES:
1. Rating applies for case temperatures to 125°C; derate linearly at 9 mW/°C for ambient temperatures above +95°C.
2. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS (V_S = ±15 V unless otherwise specified)

CHARACTERISTICS	CONDITIONS	8043M MIN.	8043M TYP.	8043M MAX.	8043C MIN.	8043C TYP.	8043C MAX.	UNITS
The following specifications apply for T_A = 25°C:								
Input Offset Voltage	R_S < 100 kΩ		10	20		20	50	mV
Input Offset Current			0.5			0.5		pA
Input Current (either input)			2.0	20		3.0	50	pA
Input Resistance			10^6			10^6		MΩ
Input Capacitance			2.0			2.0		pF
Large Signal Voltage Gain	R_L > 2 kΩ, V_{out} = ±10 V	50,000			20,000			V/V
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Current (Total)			4.5	6		4.5	6.8	mA
Power Consumption			135	180		135	204	mW
Slew Rate			6.0			6.0		V/μs
Unity Gain Bandwidth			1.0			1.0		MHz
Transient Response (Unity Gain)	C_L < 100 pF, R_L = 2 kΩ							
Risetime			300			300		ns
Overshoot			10			10		%
The following specifications apply for 0°C < T_A < +70°C (8043C), −55°C < T_A < +125°C (8043M):								
Input Voltage Range		±10	±12		±10	±12		V
Common Mode Rejection Ratio		70	90		70	90		dB
Supply Voltage Rejection Ratio			70	300		70	600	μV/V
Large Signal Voltage Gain		25,000			15,000			V/V
Output Voltage Swing	R_L > 10 kΩ	±12	±14		±12	±14		V
	R_L > 2 kΩ	±10	±13		±10	±13		V
Input Offset Voltage			15	30		30	60	mV
Input Current (either input)	T_A = +125°C		2.0	15				nA
	T_A = +70°C					50	175	pA
Average Temperature Coefficient of Input Offset Voltage				75			75	μV/°C

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TYPICAL PERFORMANCE CURVES

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

VOLTAGE FOLLOWER LARGE-SIGNAL PULSE RESPONSE

TRANSIENT RESPONSE

INPUT CURRENT AS A FUNCTION OF TEMPERATURE

OUTPUT SWING AS A FUNCTION OF SUPPLY VOLTAGE

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

INPUT VOLTAGE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

QUIESCENT SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

TOTAL QUIESCENT SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY

WIDEBAND NOISE AS A FUNCTION OF SOURCE RESISTANCE

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CHANNEL SEPARATION

Channel separation or crosstalk is measured using the circuit of Fig. 1. One amplifier is driven so that its output swings ±10 V; the signal amplitude seen in the other amplifier (referred to the input) is then measured. Typical performance is shown in Fig. 2.

$$\text{Channel Separation} = 20 \log \left(\frac{V_{OUT(A)}}{V_{IN(B)}} \right)$$

FIGURE 1

FIGURE 2

ORDERING INFORMATION

TYPE	ORDER PART NUMBER	PACKAGE	TEMPERATURE RANGE
8043M	ICL 8043M DE	Hermetic 16 Pin DIP	−55°C to 125°C
8043C	ICL 8043C PE	Plastic 16 Pin DIP	0°C to 70°C
8043C	ICL 8043C DE	Hermetic 16 Pin DIP	0°C to 70°C

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PACKAGE OUTLINES

16 LEAD CERAMIC DIP

16 LEAD PLASTIC DIP

NOTE: Board drilling dimensions will equal standard practices for .020 diameter lead.

INTERSIL

LF155, LF255, LF355, LF156, LF256, LF356, LF157, LF257, LF357

Monolithic JFET Input Operational Amplifiers

COMMON FEATURES

(LF155A, LF156A, LF157A)

- Low input bias current — 30 pA
- Low Input Offset Current — 3 pA
- High input impedance — $10^{12}\Omega$
- Low input offset voltage — 1 mV
- Low input offset voltage temperature drift — $3\mu V/^{\circ}C$
- Low input noise current — $0.01\ pA/\sqrt{Hz}$
- High common-mode rejection ratio — 100 dB
- Large dc voltage gain — 106 dB

UNCOMMON FEATURES

	LF155A	LF156A	LF157A (A_V=5)	UNITS
Extremely fast settling time to 0.01%	4	1.5	1.5	μs
Fast slew rate	5	12	50	$V/\mu s$
Wide gain bandwidth	2.5	5	20	MHz
Low input noise voltage	20	12	12	$nV/\sqrt{Hz}$

APPLICATIONS

- Precision high speed integrators
- Fast D/A and A/D converters
- High impedance buffers
- Wideband, low noise, low drift amplifiers
- Logarithmic amplifiers
- Photocell amplifiers
- Sample and Hold circuits

GENERAL DESCRIPTION

These monolithic JFET input operational amplifiers incorporate well matched, high voltage JFETs on the same chip with standard bipolar transistors (BIFET Technology). These amplifiers feature low input bias and offset currents, low offset voltage and offset voltage drift, coupled with offset adjust which does not degrade drift or common-mode rejection. The devices are also designed for high slew rate, wide bandwidth, extremely fast settling time, low voltage and current noise and a low 1/f noise corner.

ADVANTAGES

- Replace expensive hybrid and module FET op amps
- Rugged JFETs allow blow-out free handling compared with MOSFET input devices
- Excellent for low noise applications using either high or low source impedance—very low 1/f corner
- Offset adjust does not degrade drift or common-mode rejection as in most monolithic amplifiers
- New output stage allows use of large capacitive loads (10,000 pF) without stability problems
- Internal compensation and large differential input voltage capability

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SIMPLIFIED SCHEMATIC

CONNECTION DIAGRAM

Metal Can Package

NOTE 4: PIN 4 CONNECTED TO CASE.
TOP VIEW

8 Pin Minidip

ABSOLUTE MAXIMUM RATINGS

	LF155A/6A/7A	LF355A/6A/7A	LF155/6/7	LF255/6/7	LF355/6/7
Supply Voltage	±22V	±22V	±22V	±22V	±18V
Power Dissipation TO-99 (H package) (Note 1)	670 mW	500 mW	670 mW	570 mW	500 mW
Operating Temperature Range	−55°C to +125°C	0°C to +70°C	−55°C to +125°C	−25°C to +85°C	0°C to +70°C
$T_{j(MAX)}$	150°C	100°C	150°C	110°C	100°C
Differential Input Voltage	±40V	±40V	±40V	±40V	±30V
Input Voltage Range (Note 2)	±20V	±20V	±20V	±20V	±16V
Output Short Circuit Duration	Continuous	Continuous	Continuous	Continuous	Continuous
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C	300°C	300°C	300°C

DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF155A/6A/7A			LF355A/6A/7A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		1	2		1	2	mV
		Over Temperature			2.5			2.3	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		3	5		3	5	mV
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5		μV/°C per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3,5)		3	10		3	10	pA
		$T_j \leq T_{HIGH}$			10			1	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3,5)		30	50		30	50	pA
		$T_J \leq T_{HIGH}$			25			5	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}		Ω
A_{VOL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$, $V_O = \pm10V$, $R_L = 2k$	50	200		50	200		V/mV
		Over Temperature	25			25			V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k$	±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	+15.1		±11	+15.1		V
				−12			−12		V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		dB

AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$

SYMBOL	PARAMETER	CONDITIONS	LF155A/355A			LF156A/356A			LF157A/357A			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
SR	Slew Rate	LF155A/6A: $A_V = 1$, LF157A: $A_V = 5$	3	5		10	12		40	50		V/μs
GBW	Gain-Bandwidth Product			2.5		4	4.5		15	20		MHz
t_s	Settling Time to 0.01%	(Note 7)		4			1.5			1.5		μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$										
		f = 100 Hz		25			15			15		nV/$\sqrt{Hz}$
		f = 1000 Hz		20			12			12		nV/$\sqrt{Hz}$
i_n	Equivalent Input Noise Current	f = 100 Hz		0.01			0.01			0.01		pA/$\sqrt{Hz}$
		f = 1000 Hz		0.01			0.01			0.01		pA/$\sqrt{Hz}$
C_{IN}	Input Capacitance			3			3			3		pF

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DC ELECTRICAL CHARACTERISTICS (Note 3)

SYMBOL	PARAMETER	CONDITIONS	LF155/6/7			LF255/6/7			LF355/6/7			UNITS
			MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
V_{OS}	Input Offset Voltage	$R_S = 50\Omega$, $T_A = 25°C$		3	5		3	5		3	10	mV
		Over Temperature			7			6.5			13	mV
$\Delta V_{OS}/\Delta T$	Average TC of Input Offset Voltage	$R_S = 50\Omega$		5			5			5		$\mu V/°C$
$\Delta TC/\Delta V_{OS}$	Change in Average TC with V_{OS} Adjust	$R_S = 50\Omega$, (Note 4)		0.5			0.5			0.5		$\mu V/°C$ per mV
I_{OS}	Input Offset Current	$T_j = 25°C$, (Notes 3, 5)		3	20		3	20		3	50	pA
		$T_j \leq T_{HIGH}$			20			1			2	nA
I_B	Input Bias Current	$T_J = 25°C$, (Notes 3,5)		30	100		30	100		30	200	pA
		$T_J \leq T_{HIGH}$			50			5			8	nA
R_{IN}	Input Resistance	$T_J = 25°C$		10^{12}			10^{12}			10^{12}		Ω
AV_{OL}	Large Signal Voltage Gain	$V_S = \pm15V$, $T_A = 25°C$	50	200		50	200		25	200		V/mV
		$V_O = \pm10V$, $R_L = 2k$										
		Over Temperature	25			25			15			V/mV
V_O	Output Voltage Swing	$V_S = \pm15V$, $R_L = 10k$	±12	±13		±12	±13		±12	±13		V
V_{CM}	Input Common-Mode Voltage Range	$V_S = \pm15V$	±11	+15.1		±11	+15.1		±10	+15.1		V
				−12			−12			−12		V
CMRR	Common-Mode Rejection Ratio		85	100		85	100		80	100		dB
PSRR	Supply Voltage Rejection Ratio	(Note 6)	85	100		85	100		80	100		dB

DC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$

PARAMETER	LF155A/355A LF155/255		LF355		LF156A/356A LF156/256		LF356		LF157A/357A LF157/257		LF357		UNITS
	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	TYP	MAX	
Supply Current,	2	4	2	4	5	7	5	10	5	7	5	10	mA

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AC ELECTRICAL CHARACTERISTICS $T_A = 25°C$, $V_S = \pm15V$

SYMBOL	PARAMETER	CONDITIONS	LF155/LF255/ LF355	LF156/LF256	LF156/LF256/ LF356	LF157/LF257	LF157/LF257/ LF357	UNITS
			TYP	MIN	TYP	MIN	TYP	
SR	Slew Rate	LF155/6: $A_V = 1$, LF157: $A_V = 5$	5	7.5	12	30	50	$V/\mu s$
GBW	Gain-Bandwidth Product		2.5		5		20	MHz
t_s	Settling Time to 0.01%	(Note 7)	4		1.5		1.5	μs
e_n	Equivalent Input Noise Voltage	$R_S = 100\Omega$						
		f = 100 Hz	25		15		15	$nV/\sqrt{Hz}$
		f = 1000 Hz	20		12		12	$nV/\sqrt{Hz}$
i_n	Equivalent Input Current Noise	f = 100 Hz	0.01		0.01		0.01	$pA/\sqrt{Hz}$
		f = 1000 Hz	0.01		0.01		0.01	$pA/\sqrt{Hz}$
C_{IN}	Input Capacitance		3		3		3	pF

NOTES FOR ELECTRICAL CHARACTERISTICS

NOTE 1: The TO-99 package must be derated based on a thermal resistance of 150°C/W junction to ambient or 45°C/W junction to case.
NOTE 2: Unless otherwise specified the absolute maximum negative input voltage is equal to the negative power supply voltage.
NOTE 3: These specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $-55°C \leq T_A \leq +125°C$ and $T_{HIGH} = +125°C$ unless otherwise stated for the LF155A/6A/7A and the LF155/6/7. For the LF255/6/7, these specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $-25°C \leq T_A \leq +85°C$ and $T_{HIGH} = 85°C$ unless otherwise stated. For the LF355A/6A/7A, these specifications apply for $\pm 15V \leq V_S \leq \pm 20V$, $0°C \leq T_A \leq +70°C$ and $T_{HIGH} = +70°C$, and for the LF355/6/7 these specifications apply for $V_S = \pm 15V$ and $0°C \leq T_A \leq +70°C$. V_{OS}, I_B and I_{OS} are measured at $V_{CM} = 0$.
NOTE 4: The Temperature Coefficient of the adjusted input offset voltage changes only a small amount (0.5μV/°C typically for each mV of adjustment from its original unadjusted value. Common-mode rejection and open loop voltage gain are also unaffected by offset adjustment.
NOTE 5: The input bias currents are junction leakage currents which approximately double for every 10°C increase in the junction temperature, T_J. Due to limited production test time, the input bias currents measured are correlated to junction temperature. In normal operation the junction temperature rises above the ambient temperature as a result of internal power dissipation, Pd. $T_j = T_A + \Theta jA$ Pd where ΘjA is the thermal resistance from junction to ambient. Use of a heat sink is recommended if input bias current is to be kept to a minimum.
NOTE 6: Supply Voltage Rejection is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.
NOTE 7: Settling time is defined here, for a unity gain inverter connection using 2 kΩ resistors for the LF155/6. It is the time required for error voltage (the voltage at the inverting input pin on the amplifier) to settle to within 0.01% of its final value from the time a 10V step input is applied to the inverter. For the LF157, $A_V = -5$, the feedback resistor from output to input is 2 kΩ and the output step is 10V (See Settling Time Test Circuit, page 9).

TYPICAL DC PERFORMANCE CHARACTERISTICS

Curves are for LF155, LF156 and LF157 unless otherwise specified.

Input Bias Current

Input Bias Current

Input Bias Current

Voltage Swing

Supply Current

Supply Current

Negative Current Limit

Positive Current Limit

Positive Common-Mode Input Voltage Limit

5

TYPICAL DC PERFORMANCE CHARACTERISTICS (CON'T)

Negative Common-Mode Input Voltage Limit

Open Loop Voltage Gain

Output Voltage Swing

TYPICAL AC PERFORMANCE CHARACTERISTICS

Gain Bandwidth

Normalized Slew Rate

LF155 Small Signal Pulse Response, $A_V = +1$

LF156 Small Signal Pulse Response, $A_V = +1$

LF157 Small Signal Pulse Response, $A_V = +5$

LF155 Large Signal Pulse Response, $A_V = +1$

LF156 Large Signal Pulse Response, $A_V = +1$

LF157 Large Signal Pulse Response, $A_V = +5$

TYPICAL AC PERFORMANCE CHARACTERISTICS (CON'T)

Inverter Settling Time

Inverter Settling Time

Open Loop Frequency Response

Bode Plot

Bode Plot

Bode Plot

Common-Mode Rejection Ratio

Power Supply Rejection Ratio

Power Supply Rejection Ratio

Undistorted Output Voltage Swing

Equivalent Input Noise Voltage

Equivalent Input Noise Voltage (Expanded Scale)

5

TYPICAL AC PERFORMANCE CHARACTERISTICS (CON'T)

Output Impedance

Output Impedance

Output Impedance

DETAILED SCHEMATIC

*C = 2pF ON LF157

PACKAGE DIMENSIONS

TO-99 METAL CAN PACKAGE (H)

ORDER NUMBER:

LF155T
LF155AT
LF156T
LF156AT
LF157T
LF157AT
LF255T
LF256T
LF257T
LF355T
LF355AT
LF355AP
LF356T
LF356AT
LF356AP
LF357T
LF357AT
LF357AP

8 PIN MINIDIP

5

APPLICATION HINTS

The LF155/6/7 series are op amps with JFET input devices. These JFETs have large reverse breakdown voltages from gate to source and drain eliminating the need for clamps across the inputs. Therefore large differential input voltages can easily be accommodated without a large increase in input current. The maximum differential input voltage is independent of the supply voltage. However, neither of the input voltages should be allowed to exceed the negative supply as this will cause large currents to flow which can result in a destroyed unit.

Exceeding the negative common-mode limit on either input will cause a reversal of the phase to the output and force the amplifier output to the corresponding high or low state. Exceeding the negative common-mode limit on both inputs will force the amplifier output to a high state. In neither case does a latch occur since raising the input back within the common-mode range again puts the input stage and thus the amplifier in a normal operating mode.

Exceeding the positive common-mode limit on a single input will not change the phase of the output however, if both inputs exceed the limit, the output of the amplifier will be forced to a high state.

These amplifiers will operate with the common-mode input voltage equal to the positive supply. In fact, the common-mode voltage can exceed the positive supply by approximately 100 mV independent of supply voltage and over the full operating temperature range. The positive supply can therefore be used as a reference on an input as, for example, in a supply current monitor and/or limiter.

Precautions should be taken to ensure that the power supply for the integrated circuit never becomes reversed in polarity or that the unit is not inadvertently installed backwards in a socket as an unlimited current surge through the resulting forward diode within the IC could cause fusing of the internal conductors and result in a destroyed unit.

Because these amplifiers are JFET rather than MOSFET input op amps they do not require special handling.

All of the bias currents in these amplifiers are set by FET current sources. The drain currents for the amplifiers are therefore essentially independent of supply voltage.

As with most amplifiers, care should be taken with lead dress, component placement and supply decoupling in order to ensure stability. For example, resistors from the output to an input should be placed with the body close to the input to minimize "pickup" and maximize the frequency of the feedback pole by minimizing the capacitance from the input to ground.

A feedback pole is created when the feedback around any amplifier is resistive. The parallel resistance and capacitance from the input of the device (usually the inverting input) to ac ground set the frequency of the pole. In many instances the frequency of this pole is much greater than the expected 3 dB frequency of the closed loop gain and consequently there is negligible effect on stability margin. However, if the feedback pole is less than approximately six times the expected 3 dB frequency a lead capacitor should be placed from the output to the input of the op amp. The value of the added capacitor should be such that the RC time constant of this capacitor and the resistance it parallels is greater than or equal to the original feedback pole time constant.

TYPICAL CIRCUIT CONNECTIONS

V_{OS} Adjustment

- V_{OS} is adjusted with a 25k potentiometer
- The potentiometer wiper is connected to V^+
- For potentiometers with temperature coefficient of 100 ppm/°C or less the additional drift with adjust is ≈ 0.5μV/°C/m of adjustment.
- Typical overall drift: 50V/°C ≅ (0.5μV/°C/mV of adj.)

Driving Capacitive Loads

Due to a unique output stage design these amplifiers have the ability to drive large capacitive loads and still maintain stability. $C_{L\,MAX} \cong 0.01\mu F$.

Overshoot ≤ 20%.

Settling time (t_S) ≅ 5μs

LF157. A Large Power BW Amplifier

For distortion < 1% and a 20 Vp-p V_{OUT} swing power bandwidth is: 500 kHz.

TYPICAL APPLICATIONS

Settling Time Test Circuit

- Settling time is tested with the LF155/6 connected as unity gain inverter and LF157 connected for $A_V = -5$
- FET used to isolate the probe capacitance
- Output = 10V step

* $A_V = -5$ for LF157

Large Signal Inverter Output, V_{OUT} (from Settling Time Circuit)

5

Low Drift Adjustable Voltage Reference

- $\Delta V_{OUT}/\Delta T = \pm 0.002\%/°C$
- All resistors and potentiometers should be wire-wound
- P1: drift adjust
- P2: V_{OUT} adjust
- Use LF155 for
  - Low I_B
  - Low drift
  - Low supply current

TYPICAL APPLICATIONS (CON'T)

Fast Logarithmic Converter

$$|V_{OUT}| = \left[1 + \frac{R2}{R_T}\right]\frac{kT}{q} \quad \text{Ln } V_i \left[\frac{R_r}{V_{REF}R_i}\right] = \log V_i \frac{1}{R_i I_r}$$

R2 = 15.7k, R_T = 1k, 0.3%/°C (for temperature compensation)

- Dynamic range: 100μA ≤ I_i ≤ 1 mA (5 decades), $|V_O|$ = 1V/decade
- Transient response: 3μs for ΔI_i = 1 decade
- C1, C2, R2, R3: added dynamic compensation
- V_{OS} adjust the LF156 to minimize quiescent error
- R_T: Tel Labs type Q81 + 0.3%/°C.

Precision Current Monitor

- $V_O = 5\frac{R1}{R2}$ (V/mA of I_S)
- R1, R2, R3: 0.1% resistors
- Use LF155 for
  - Common mode range to supply voltage
  - Low I_B
  - Low V_{OS}
  - Low supply current

5

TYPICAL APPLICATIONS (CON'T)

LF156 as an Output Amplifier in a Fast 8-Bit DAC

- Quad 1, 2: precision current switches
- R1–R4: binary ladder
- V_{REF}: ICL 8069
- Use LF155/6 for
  - ▲ Fast settling time
  - ▲ Low V_{OS} drift
  - ▲ Good stability

Wide BW Low Noise, Low Drift Amplifier

- Power BW: $f_{MAX} = \frac{S_r}{2_\pi V_P} \cong 240\ kHz$
- Parasitic input capacitance C1 ≅ (3 pF for LF155, LF156, and LF157 plus any additional layout capacitance) interacts with feedback elements and creates undesirable high frequency pole. To compensate add C2 such that: R2C2 ≅ R1C1.

Isolating Large Capacitive Loads

- Overshoot 6%
- t_s 10μs
- When driving large C_L the V_{OUT} slew rate determined by C_L and $I_{OUT\ MAX}$:

$$\frac{\Delta V_{OUT}}{\Delta T} = \frac{I_{OUT}}{C_L} \cong \frac{0.02}{0.5} \quad V/\mu s = 0.04 V/\mu s$$

(with C_L shown)

TYPICAL APPLICATIONS (CON'T)

Boosting the LF156 with a Current Amplifier

- $I_{OUT\ MAX} \cong 150$ mA (will drive $R_L \geq 100\Omega$)
- $\frac{\Delta V_{OUT}}{\Delta T} = 15 V/\mu sec$ (with C_L shown)
- No additional phase shift added by the current amplifier

Low Drift Peak Detector

- By adding D1 and R_f, $V_{D1} = 0$ during hold mode. Leakage of D2 provided by feedback path through R_f.
- Leakage of circuit is essentially I_b (LF155, LF156) plus capacitor leakage of C_P.
- Diode D3 clamps V_{OUT} (A1) to $V_{IN} - V_{D3}$ to improve speed and to limit reverse bias of D2.
- Maximum input frequency should be $<< \frac{1}{2\pi R_f C_{D2}}$ where C_{D2} is the shunt capacitance of D2.

3 Decades VCO

$$f = \frac{V_C (R8 + R7)}{[8\ V_{PU} R8 R1]\ C}, \quad 0 \leq V_C \leq 30V,\ 10\ Hz \leq f \leq 10\ kHz$$

R1, R4 matched. Linearity 0.1% over 2 decades.

5

TYPICAL APPLICATIONS (CON'T)

High Impedance, Low Drift Instrumentation Amplifier

- $V_{OUT} = \frac{R3}{R}\left[\frac{2R2}{R1} + 1\right]$ ΔV, $V^- + 2V \leq V_{IN}$ Common-Mode $\leq V^+$
- System V_{OS} adjusted via A2 V_{OS} adjust
- Trim R3 to boost up CMRR to 120 dB. Instrumentation amplifier Resistor array RA201 (National Semiconductor) recommended

Fast Sample and Hold

- Both amplifiers (A1, A2) have feedback loops individually closed with stable responses (overshoot negligible)
- Acquisition time, T_A, estimated by:

$$T_A \cong \left[\frac{2R_{ON}, V_{IN}, C_h}{Sr}\right]^{1/2} \quad \text{provided that:}$$

$$V_{IN} < 2\pi S_r R_{ON} C_h \text{ and } T_A > \frac{V_{IN} C_h}{I_{OUT\,MAX}}$$, R_{ON} is of SW1

If inequality not satisfied: $T_A \cong \frac{V_{IN} C_h}{20\text{ mA}}$

- LF156 develops full S_r output capability for $V_{IN} \geq 1V$
- Addition of SW2 improves accuracy by putting the voltage drop across SW1 inside the feedback loop
- Overall accuracy of system determined by the accuracy of both amplifiers, A1 and A2

TYPICAL APPLICATIONS (CON'T)

High Accuracy Sample and Hold

- By closing the loop through A2 the V_{OUT} accuracy will be determined uniquely by A1. No V_{OS} adjust required for A2.
- T_A can be estimated by same considerations as previously but because of the added propagation delay in the feedback loop (A2) the overshoot is not negligible.
- Overall system slower than fast sample and hold
- R1, C_C: additional compensation
- Use LF156 for
  - ▲ Fast settling time
  - ▲ Low V_{OS}

High Q Band Pass Filter

- By adding positive feedback (R2) Q increases to 40
- f_{BP} = 100 kHz

$$\frac{V_{OUT}}{V_{IN}} = 10\sqrt{Q}$$

- Clean layout recommended
- Response to a 1 Vp-p tone burst: 300μs

TYPICAL APPLICATIONS (CON'T)

High Q Notch Filter

- 2R1 = R = 10MΩ
  2C = C1 = 300 pF
- Capacitors should be matched to obtain high Q
- f_{NOTCH} = 120 Hz, notch = −55 dB, Q > 100
- Use LF155 for
  - Low I_B
  - Low supply current

5

DEFINITION OF TERMS

Input Offset Voltage: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

Input Offset Current: The difference in the currents into the two input terminals when the output is at zero.

Input Bias Current: The average of the two input currents.

Input Common-Mode Voltage Range: The range of voltages on the input terminals for which the amplifier is operational. Note that the specifications are not guaranteed over the full common-mode voltage range unless specifically stated.

Common-Mode Rejection Ratio: The ratio of the input common-mode voltage range to the peak-to-peak change in input offset voltage over this range.

Input Resistance: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

Supply Current: The current required from the power supply to operate the amplifier with no load and the output midway between the supplies.

Output Voltage Swing: The peak output voltage swing, referred to zero, that can be obtained without clipping.

Large-Signal Voltage Gain: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

Power Supply Rejection Ratio: The ratio of the change in input offset voltage to the change in power supply voltage producing it. The typical curves in this sheet show values for each supply independently changed. The electrical specification, however, is measured for both supply magnitudes increasing or decreasing simultaneously, in accordance with common practice.

Settling Time: The time required for the error between input and output to settle to within a specified limit after an input is applied to the test circuit shown in typical applications.

INTERSIL

LH0042/LH0042C Operational Amplifiers/Buffers

FEATURES

- **Low input offset voltage—100 microvolts-typ.**
- **High open loop gain—100 dB typ.**
- **Excellent slew rate—3.0 V/μs typ.**
- **Internal 6 dB/octave frequency compensation**
- **Pin compatible with standard IC op amps (TO-5 package)**

GENERAL DESCRIPTION

The LH0042 is a FET input operational amplifier with very closely matched input characteristics, very high input impedance, and ultra-low input current, with no compromise in noise, common mode rejection ratio, open loop gain, or slew rate. Devices are internally compensated and free of latch-up and unusual oscillation problems, and may be offset nulled with a single 10K trimpot with negligible effect in CMRR.

The LH0042 is specified for operation over the −55°C to +125°C military temperature range. The LH0042C is specified for operation over the −25°C to +85°C temperature range.

The LH0042 IC op amp is intended to fulfill a wide variety of applications for process control, medical instrumentation, and other systems requiring very low input currents and tightly matched input offsets. The LH0042 provides low cost high performance for such applications as electrometer and photocell amplification, pico-ammeters, and high input impedance buffers.

CONNECTION DIAGRAM

TOP VIEW

SCHEMATIC

5

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Power Dissipation (see graph) ..... 500 mW
Input Voltage (Note 1) ..... ±15V
Differential Input Voltage (Note 2) ..... ±30V
Voltage Between Offset Null and V^- ..... ±0.5V
Short Circuit Duration ..... Continuous
Operating Temperature Range
LH0042 ..... −55°C to +125°C
LH0042C ..... −25°C to +85°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

DC ELECTRICAL CHARACTERISTICS for LH0042/LH0042C

(T_A = 25°C, V_S = ±15V, unless otherwise specified)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0042			LH0042C			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	$R_S \leq 100\ k\Omega$		5.0	20		6.0	20	mV
Temperature Coefficient of Input Offset Voltage	$R_S \leq 100\ k\Omega$		5			10		μV/°C
Offset Voltage Drift with Time			7			10		μV/week
Input Offset Current			1	5		2	10	pA
Temperature Coefficient of Input Offset Current		Doubles every 10°C			Doubles every 10°C			
Offset Current Drift with Time			0.1			0.1		pA/week
Input Bias Current			10	25		15	50	pA
Temperature Coefficient of Input Bias Current		Doubles every 10°C			Doubles every 10°C			
Differential Input Resistance			10^{12}			10^{12}		Ω
Common Mode Input Resistance			10^{12}			10^{12}		Ω
Input Capacitance			4.0			4.0		pF
Input Voltage Range		±12	±13.5		±12	±13.5		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$, V_{IN} = ±10V	70	86		70	80		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$, ±5V ≤ V_S ≤ ±15V	70	86		70	80		dB
Large Signal Voltage Gain	$R_L = 1\ k\Omega$, V_{OUT} = ±10V	50	150		25	100		V/mV
Output Voltage Swing	$R_L = 1\ k\Omega$	±10	±12.5		±10	±12		V
Output Current Swing	V_{OUT} = ±10V	±10	±15		±10	±15		mA
Output Resistance			75			75		Ω
Output Short Circuit Current			20			20		mA
Supply Current			2.5	3.5		2.8	4.0	mA
Power Consumption				105			120	mW

5

AC ELECTRICAL CHARACTERISTICS For all amplifiers (T_A = 25°C, V_S = ±15V)

PARAMETER	CONDITIONS	LIMITS						UNITS
		LH0042			LH0042C			
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Slew Rate	Voltage Follower	1.5	3.0		1.0	3.0		V/μs
Large Signal Bandwidth	Voltage Follower		40			40		kHz
Small Signal Bandwidth			1.0			1.0		MHz
Rise Time			0.3	1.5		0.3	1.5	μs
Overshoot			10	30		15	40	%
Settling Time (0.1 %)	ΔV_{IN} = 10V		4.5			4.5		μs
Overload Recovery			4.0			4.0		μs
Input Noise Voltage	R_S = 10 kΩ, f_o = 10 Hz		150			150		nV/√Hz
Input Noise Voltage	R_S = 10 kΩ, f_o = 100 Hz		55			55		nV/√Hz
Input Noise Voltage	R_S = 10 kΩ, f_o = 1 kHz		35			35		nV/√Hz
Input Noise Voltage	R_S = 10 kΩ, f_o = 10 kHz		30			30		nV/√Hz
Input Noise Voltage	BW = 10 Hz to 10 kHz, R_S = 10 kΩ		12			12		μVrms
Input Noise Current	BW = 10 Hz to 10 kHz		<.1			<.1		pArms

Notes:
1. For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
2. Rating applies for minimum source resistance of 10 kΩ, for source resistances less than 10 kΩ, maximum differential input voltage is ±5V.
3. Unless otherwise specified, these specifications apply for ±5V ≤ V_S ≤ ±20V and −55°C ≤ T_A ≤ ±125°C for the LH0042 and −25°C ≤ T_A+85°C for the LH0042C. Typical values are given for T_A = 25°C.

AUXILIARY CIRCUITS (shown for TO-5 pin out)

OFFSET NULL

BOOSTING OUTPUT DRIVE TO ±100 mA

NOTE: ALL DIODES ARE ULTRA LOW LEAKAGE

PROTECTING INPUTS FROM ±150V TRANSIENTS

5

TYPICAL APPLICATIONS

ALTERNATE LOW DRIFT SAMPLE

PRECISION VOLTAGE COMPARATOR

TYPICAL PERFORMANCE CHARACTERISTICS

MAXIMUM POWER DISSIPATION

INPUT OFFSET CURRENT VS TEMPERATURE

INPUT BIAS CURRENT VS TEMPERATURE

INPUT OFFSET VOLTAGE VS TEMPERATURE

OFFSET ERROR (WITHOUT V_{OS} NULL)

TOTAL INPUT NOISE VOLTAGE* VS SOURCE RESISTANCE

TOTAL INPUT NOISE VOLTAGE* VS FREQUENCY

COMMON MODE INPUT VOLTAGE VS SUPPLY VOLTAGE

STABILIZATION TIME OF INPUT OFFSET VOLTAGE FROM POWER TURN-ON

CHANGE IN INPUT OFFSET VOLTAGE DUE TO THERMAL SHOCK VS TIME

SUPPLY VOLTAGE VS SUPPLY CURRENT

VOLTAGE GAIN

*NOISE VOLTAGE INCLUDES CONTRIBUTION FROM SOURCE RESISTANCE.

TYPICAL PERFORMANCE CHARACTERISTICS (CON'T.)

OUTPUT SWING VS SUPPLY VOLTAGE

OUTPUT VOLTAGE SWING VS LOAD RESISTANCE

CURRENT LIMITING

OUTPUT VOLTAGE SWING VS FREQUENCY

VOLTAGE FOLLOWER LARGE SIGNAL RESPONSE

TRANSIENT RESPONSE

FREQUENCY CHARACTERISTICS VS AMBIENT TEMPERATURE

FREQUENCY CHARACTERISTICS VS SUPPLY VOLTAGE

OUTPUT RESISTANCE VS FREQUENCY

OPEN LOOP TRANSFER CHARACTERISTICS VS FREQUENCY

5

INTERSIL

LM740, μA740
FET Input Operational Amplifier

FEATURES

- High input impedance. . . 1MΩ
- No frequency compensation required
- Short-circuit protection
- Offset voltage null capability
- Large common-mode and differential voltage ranges
- No latch up

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22V
Internal Power Dissipation (Note 1)	500mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Voltage between Offset Null and V+	±0.5V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Military (740)	−55°C to +125°C
Commercial (740C)	0°C to +70°C
Lead Temperature (Soldering, 60 seconds)	300°C
Output Short-Circuit Duration (Note 3)	Indefinite

ORDERING INFORMATION

TYPE	PART NO.
740	LM740T
740C	LM740CT
	μA740T
	μA740CT

GENERAL DESCRIPTION

The 740 is a high performance monolithic FET-Input Operational Amplifier epitaxial process. It is intended for a wide range of analog applications where very high input impedance is required and features very low input offset current and very low input bias current. High slew rate, high common mode voltage range and absence of "latch up" make the 740 ideal for use as a voltage follower. The high gain and wide range of operating voltages provide superior performance in active filters, integrators, summing amplifiers, sample and holds, transducer amplifiers, and other general feedback applications. The 740 is short circuit protected and has the same pin configuration as the 741 operational amplifier. No external components for frequency compensation are required as the internal 6 dB/octave roll-off insures stability in closed loop applications.

CONNECTION DIAGRAM

NOTE: Pin 4 Connected to Case.

5

EQUIVALENT CIRCUIT

740

ELECTRICAL CHARACTERISTICS (V_S = ±15V, T_C = 25°C unless otherwise specified)

PARAMETER		CONDITIONS	MIN.	TYP.	MAX.	UNITS
Input Offset Voltage		$R_S \leq 100k\Omega$		10	20	mV
Input Offset Current (Note 4)				40	150	pA
Input Current (either input) (Note 4)				100	200	pA
Input Resistance				1		MΩ
Large Signal Voltage Gain		$R_L \geq 2k\Omega$, V_{OUT} = ±10V	50,000	1		
Output Resistance				75		Ω
Output Short-Circuit Current				20		mA
Common Mode Rejection Ratio			64	80		dB
Supply Voltage Rejection Ratio				70	300	μV/V
Supply Current				4.2	5.2	mA
Power Consumption				126	156	mW
Slew Rate				6.0		V/μs
Unity Gain Bandwidth				3.0		MHz
Transient Response (Unity Gain)	Risetime	$C_L \leq 100pF$, R_L = 2kΩ, V_{IN} = 100mV		110		ns
	Overshoot			10	20	%
The following specifications apply for T_C = –55°C to +85°C:						
Input Voltage Range			±10		±12	V
Large Signal Voltage Gain			25,000			
Output Voltage Swing		$R_L \geq 10k\Omega$	±12	±14		V
		$R_L \geq 2k\Omega$	±10	±13		V
Input Offset Voltage		$R_S \leq 100k\Omega$		15	30	mV
Input Offset Current		T_A = –55°C		30		pA
		T_A = +85°C		185		pA
Input Current (either input)		T_A = –55°C			200	pA
		T_A = +85°C		2.5	4.0	nA

VOLTAGE OFFSET NULL CIRCUIT

TRANSIENT RESPONSE TEST CIRCUIT

5

740C

ELECTRICAL CHARACTERISTICS ($V_S = \pm15V$, $T_C = 25°C$ unless otherwise specified)

PARAMETER		CONDITIONS	MIN	TYP	MAX	UNITS
Input Offset Voltage		$R_S \leq 100k\Omega$		30	110	mV
Input Offset Current (Note 4)				60	300	pA
Input Current (either input) (Note 4)				0.1	2.0	nA
Input Resistance				1		MΩ
Large Signal Voltage Gain		$R_L \geq 2k\Omega$, $V_{OUT} = \pm10V$	20,000	1		
Output Resistance				75		Ω
Output Short-Circuit Current				20		mA
Supply Current				4.2	8.0	mA
Power Consumption				126	240	mW
Slew Rate				6.0		V/μs
Unity Gain Bandwidth				1.0		MHz
Transient Response (Unity Gain)	Risetime	$C_L \leq 100pF$, $R_L = 2k\Omega$, $V_{IN} = 100mV$		300		ns
	Overshoot			10		%
The following specifications apply for $0°C \leq T_A \leq +70°C$:						
Input Voltage Range			±10	±12		V
Common Mode Rejection Ratio			55	80		dB
Supply Voltage Rejection Ratio				70	500	μV/V
Large Signal Voltage Gain				500,000		
Output Voltage Swing		$R_L \geq 10k\Omega$	±12	±14		V
		$R_L \geq 2k\Omega$	±10	±13		V
Input Offset Voltage				30		mV
Input Offset Current				60		pA
Input Current (either input)				1.1	10	nA

NOTE 1: Rating applies for ambient temperature to +70°C; derate linearly at 6.3mW/°C for ambient temperatures above +70°C.
NOTE 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
NOTE 3: Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.
NOTE 4: Typically doubles for every 10°C increase in ambient temperature.

5

TYPICAL PERFORMANCE CURVES FOR 740 AND 740C

INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

5

INTERSIL

SU536 FET Input Operational Amplifier

FEATURES

- 5pA input bias current
- Input and output protection
- Offset null capability
- Internally compensated
- 6V/μsec slew rate
- Standard pinout
- 1MHz unity gain bandwidth

PIN CONFIGURATION

DESCRIPTION

The 536 is a special purpose high performance operational amplifier utilizing a FET input stage for extremely high input impedance and low input current.

The device features internal compensation, standard pinout, wide differential and common mode input voltage ranges, high slew rate and high output drive capability.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±22V
Differential Input Voltage Range ..... ±30V
Common Mode Input Voltage Range ..... $\pm V_S$
Power Dissipation[1] 500mW
Operating Temperature Range ..... −55° to +85°C
Storage Temperature Range ..... −65° to +150°C
Lead Temperature (Solder, 60 sec) ..... 300°C
Output Short Circuit Duration[2] ..... indefinite

Notes:
1. Rating applies for case temperature to +25°C; derate linearly at 6.5mW/°C for ambient temperatures above 75°C.
2. Short circuit may be to ground or either supply. Rating applies to +125°C case temperature or +75°C ambient temperature.

5

DC ELECTRICAL CHARACTERISTICS T_A = 25°C, V_{SUPP} ±15V unless otherwise specified.[1]

PARAMETER		TEST CONDITIONS	SU536 MIN.	SU536 TYP.	SU536 MAX.	UNIT
V_{OS}	Offset Voltage	$R_S \leq 10k\Omega$		30	90	mV
		Over Temp., $R_S \leq 10k\Omega$		30		mV
$\Delta V_{OS}/\Delta T$	Drift	$R_S = 0\Omega$, Over Temp.		30		μV/°C
I_{OS}	Offset Current			5		pA
I_{BIAS}	Input Current[2]			30	100	pA
V_{CM}	Common Mode Voltage Range		±10	±11		V
CMRR	Common Mode Rejection Ratio	$R_S \leq 10k\Omega$, V_{IN} = ±10V	64	80		dB
R_{IN}	Input Resistance			100		MΩ
V_{OUT}	Output Voltage Swing	$R_L \geq 2k\Omega$, Over Temp.	±10	±11		V
		R_L 10kΩ, Over Temp.	±12	±13		V
I_{CC}	Supply Current	V_{OUT} = OV		6.0	8.0	mA
PSRR	Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$, $\pm 6 \leq V_S \pm 15$		100	300	μV/V
A_{VOL}	Large Signal Voltage Gain	V_O = ±10V, R_L 2kΩ	50			V/mV
		V_O = ±10V, $R_L \geq 2k\Omega$, Over Temp.	25			V/mV
V_{SUPP}	Power Supply Range		±6	±18		V

Notes:
1. Input current typically doubles every 10°C.

DC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$, $\pm 6V \leq V_S \leq \pm 20V$ unless otherwise specified.[2]

PARAMETER		TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
V_{OS}	Offset Voltage[2]	$R_S \leq 10k\Omega$ $R_S \leq 10k\Omega$		7.5 7.5	20 30	mV mV
$\Delta V_{OS}/\Delta T$	Drift	$R_S \leq 10k\Omega$		20		$\mu V/°C$
I_{OS}	Offset Current			5		pA
I_{BIAS}	Input Current[1,2]			5 250	30 3000	pA pA
V_{CM}	Common Mode Voltage Range	$V_{SUPP} = \pm 15V$	± 10	± 11		V
CMRR	Common Mode Rejection Ratio	$R_S \leq 10k\Omega$, $V_{IN} = \pm 10V$	70	80		dB
R_{IN}	Input Resistance			100		$M\Omega$
V_{OUT}	Output Voltage Swing[2]	$R_L \geq 2k\Omega$, $V_{SUPP} = \pm 15V$ $R_L \geq 10k\Omega$, $V_{SUPP} = \pm 15V$	± 10 ± 12	± 12 ± 13		V V
I_+	Supply Current	$V_{OUT} = 0V$, $V_{SUPP} = \pm 20V$		4.5	5.5	mA
P_{SRR}	Supply Voltage Rejection Ratio	$R_S \leq 10k\Omega$		50	150	$\mu V/V$
A_{VOL}	Large Signal Voltage Gain[2]	$V_{SUPP} = \pm 15V$, $V_O = \pm 10V$, $R_L \geq 2k\Omega$	50			V/mV
V_{SUPP}	Power Supply Range		± 6		± 20	V

Notes:
1. Input current typically doubles every 10°C.
2. Operating temperature range is −55°C to +85°C.

AC ELECTRICAL CHARACTERISTICS

$T_A = 25°C$ unless otherwise specified.[1,2]

SYMBOL	PARAMETER	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
C_{DIFF}	Differential Capacitance			6		pF
e_n	Input Noise Voltage	0.1Hz—100kHz		20		μVrms
Z_o	Output Impedance			100		Ω
G_{BW}	Unity Gain Frequency Full Power Bandwidth	$V_{SUPP} = \pm 15V$ $V_{SUPP} = \pm 15V$		1 100		MHz KHz
SR	Slew Rate, Inverter Slew Rate, Follower	$V_{SUPP} = \pm 15V$, $A = -1V$ $V_{SUPP} = \pm 15V$, $A = +1V$		6 6		$V/\mu s$ $V/\mu s$

Notes:
1. Temperature range is $-55 \leq T_A \leq 85°C$
2. $\pm 6V \leq T_A \pm 20V$

5

TEST CIRCUITS

VOLTAGE FOLLOWER CIRCUIT

OFFSET NULL CIRCUIT

TYPICAL PERFORMANCE CHARACTERISTICS

LARGE SIGNAL VOLTAGE FOLLOWER PULSE RESPONSE

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

OUTPUT VOLTAGE SWING AS A FUNCTION OF SUPPLY VOLTAGE

OPEN LOOP PHASE RESPONSE AS A FUNCTION OF FREQUENCY

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF FREQUENCY

VOLTAGE FOLLOWER TRANSIENT RESPONSE

OPEN LOOP VOLTAGE GAIN AS A FUNCTION OF SUPPLY VOLTAGE

INPUT VOLTAGE NOISE AS A FUNCTION OF FREQUENCY

INPUT CURRENTS AS A FUNCTION OF AMBIENT TEMPERATURE

OUTPUT SHORT-CIRCUIT CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

INTERSIL

HA2600, HA2605, HA2622, HA2602, HA2620, HA2625

High Impedance Operational Amplifiers

FEATURES

- Input Impedance – 500MΩ
- Offset Current – 1nA
- Bias Current – 1nA
- Gain Bandwidth Product – 100MHz
- High Gain – 150K
- Output Short Circuit Protection
- Meets MIL-STD-883

GENERAL DESCRIPTION

The 2600 series of high impedance operational amplifiers are monolithic integrated circuits fabricated using dielectric isolation. These internally compensated amplifiers feature excellent input parameters, low input bias and wide bandwidth. They are ideally suited for general purpose use in instrumentation and signal processing applications.

2600 through 2605 are compensated for unity gain. 2620 through 2625 are intended for closed loop gains of 5 or greater and feature increased slew rated and gain-bandwidth products.

CONNECTION DIAGRAMS, TOP VIEWS

TO-99

Case Connected to V−

TO-91 Flat Pack

14 Pin CerDIP

EQUIVALENT CIRCUIT

5

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22.5V
Input Voltage (Note 1)	±15V
Differential Input Voltage	±12V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation (Note 2)	300mW
Lead Temperature (Soldering, 60 sec.)	+300°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	-55°C to +125°C (2600, 2602) 0°C to +75°C (2605)

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±15V, unless otherwise specified)

PARAMETER	CONDITIONS	2600			2602			2605			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10k\Omega$		0.5	4		3	5		3	5	mV
Input Offset Current			1	10		5	25		5	25	nA
Input Bias Current			1	10		5	25		5	25	nA
Input Resistance		100	500		40	300		40	300		MΩ
Large Signal Voltage Gain	$R_L = 2k\Omega$, $V_O = \pm 10V$	100K	150K		80K	150K		80K	150K		V/V
Unity Gain Bandwidth	$V_O < 90mV$		12			12			12		MHz
Full Power Bandwidth	$R_L = 2k\Omega$, $C_L = 50pF$, $V_O = 20V_{p-p}$	50	75		50	75		50	75		KHz
Rise Time (Note 3)	$R_L = 2k\Omega$, $C_L = 100pF$		30	60		30	60		30	60	ns
Overshoot (Note 4)	$R_L = 2k\Omega$, $C_L = 100pF$		25	40		25	50		25	50	%
Slew Rate	$R_L = 2k\Omega$, $C_L = 100pF$, $V_O = \pm 5V$	4	7		4	7		4	7		V/μs
Setting Time (to ±10mV of Final Value)	$R_L = 2k\Omega$, $C_L = 100pF$, $V_O = \pm 5V$		1.5			1.5			1.5		ns
Output Current	$V_O = \pm 10V$	±15	±22		±10	±18		±10	±18		mA
Supply Current			3	3.7		3	4		3	4	mA
THE FOLLOWING SPECIFICATIONS APPLY FOR OPERATING TEMPERATURE RANGE											
Input Offset Voltage	$R_S \leq 10k\Omega$		2	6			7			7	mV
Input Offset Current			5	30			60			40	nA
Input Bias Current			10	30			60			40	nA
Offset Voltage Average Drift	$R_S \leq 10k\Omega$		5								μV/°C
Common Mode Rejection Ratio	$V_{CM} = \pm 5V$	80	100		74	100		74	100		dB
Common Mode Range		±11			±11			±11			V
Supply Voltage Rejection Ratio	$V_S = \pm 9V$ To $\pm 15V$	80	90		74	90		74	90		dB
Large Signal Voltage Gain	$R_L = 2k\Omega$, $V_O = \pm 10V$	70k			60k			70k			V/V
Output Voltage Swing	$R_L = 2k\Omega$	±10	±12		±10	±12		±10	±12		V

NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 2: Derate TO-91 at 4.5 mW/°C above 84°C; derate TO-99 at 6.6 mW/°C above 105°C.

NOTE 3: $V_O = 400\ mV_{p-p}$

NOTE 4: $V_O = 800\ mV_{p-p}$

TRANSIENT RESPONSE

SLEW RATE AND SETTLING TIME

SLEW RATE AND TRANSIENT RESPONSE

SUGGESTED OFFSET ZERO ADJUST HOOK-UP

NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSITIONS.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±22.5V
Input Voltage (Note 1)	±15V
Differential Input Voltage	±12V
Peak Output Current	Full Short Circuit Protection
Internal Power Dissipation (Note 2)	300mW
Lead Temperature (Soldering, 60 sec.)	300°C
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−55°C to +125°C (2620, 2622) 0°C to +75°C (2625)

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±15V, unless otherwise specified)

PARAMETER	CONDITIONS	2620			2622			2625			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage (Note 3)	$R_S \leq 10k\Omega$		0.5	4		3	5		3	5	mV
Input Offset Current			1	15		5	25		5	25	nA
Input Bias Current			1	15		5	25		5	25	nA
Input Resistance		65	500		40	300		40	300		MΩ
Large Signal Voltage Gain	R_L = 2kΩ, V_O = ±10V, C_L = 50pF	100K	150K		80K	150K		80K	150K		V/V
Gain Bandwidth (Notes 4 and 5)	R_L = 2kΩ, C_L = 50pF		100			100			100		MHz
Full Power Bandwidth	R_L = 2kΩ, C_L = 50pF, V_O = 20V_{p-p}	400	600		320	600		320	600		KHz
Rise Time (Note 6)	R_L = 2kΩ, C_L = 50pF		17	45		17	45		17	45	ns
Slew Rate (Note 6)	R_L = 2kΩ, C_L = 50pF, V_O = ±5.0V	±25	±35		±20	±35		±20	±35		V/μs
Output Current	V_O = ±10V	±15	±22		±10	±18		±10	±18		mA
Supply Current			3	3.7		3	4		3	4	mA
THE FOLLOWING SPECIFICATIONS APPLY FOR OPERATING TEMPERATURE RANGE											
Input Offset Voltage	$R_S \leq 10k\Omega$			6			7			7	mV
Input Offset Current			5	35			60			40	nA
Input Bias Current			10	35			60			40	nA
Common Mode Rejection Ratio	V_{CM} = ±5V	80	100		74	100		74	100		dB
Common Mode Range		±11			±11			±11			V
Supply Voltage Rejection Ratio	V_{Supply} = ±9V To ±15V	80	90		74	90		74	90		dB
Large Signal Voltage Gain	R_L = 2kΩ, V_O = ±10V, C_L = 50pF	70k			60k			70k			V/V
Output Voltage Swing	R_L = 2kΩ, C_L = 50pF	±10	±12		±10	±12		±10	±12		V

NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 2: Derate TO-91 at 4.5 mW/°C above 84°C; derate TO-99 at 6.6 mW/°C above 105°C.

NOTE 3: May be externally adjusted to zero.

NOTE 4: V_O < 90mV.

NOTE 5: 40dB gain.

NOTE 6: A_V = 5.0V.

5

TRANSIENT RESPONSE

SLEW RATE

SLEW RATE AND TRANSIENT RESPONSE

SUGGESTED OFFSET ZERO ADJUST AND BANDWIDTH CONTROL HOOK-UP

NOTE: MEASURED ON BOTH POSITIVE AND NEGATIVE TRANSITIONS.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE	ORDER NUMBER
HA2600	−55°C to +125°C	TO-99 TO-91 Flat Pack 14 Pin CerDIP	HA2-2600-2 * HA9-2600-2 * HA1-2600-2 *
HA2602	−55°C to +125°C	TO-99 TO-91 Flat Pack 14 Pin CerDIP	HA2-2602-2 * HA9-2602-2 * HA1-2602-2 *
HA2605	0°C to +75°C	TO-99 TO-91 Flat Pack 14 Pin CerDIP	HA2-2605-5 HA9-2605-5 HA1-2605-5
HA2620	−55°C to +125°C	TO-99 TO-91 Flat Pack 14 Pin CerDIP	HA2-2620-2 * HA9-2620-2 * HA1-2620-2 *
HA2622	−55°C to +125°C	TO-99 TO-91 Flat Pack 14 Pin CerDIP	HA2-2622-2 * HA9-2622-2 * HA1-2622-2 *
HA2625	0°C to +75°C	TO-99 TO-91 Flat Pack 14 Pin CerDIP	HA2-2625-5 HA9-2625-5 HA1-2625-5

*883B processing is available for these devices. Order -8 instead of -2.

PACKAGE DIMENSIONS

TO-91 Flat Pack

ALL DIMENSIONS ARE IN INCHES.
ALL DIMENSIONS ±.010 UNLESS OTHERWISE SHOWN.

TO-99 Package

14-Pin CerDIP

NOTES: All dimensions in inches.
Leads are gold-plated Kovar.

INTERSIL

HA2607/2627 Wide Band Operational Amplifier Series

FEATURES

	HA-2607	HA-2627	
• Wide gain-bandwidth	12	100	MHz
• High slew rate	7	35	V/μs
• Wide power bandwidth	75	600	KHz
• High gain	150KV/V		
• High input impedance	500MΩ		
• Output short circuit protection			

DESCRIPTION

HA-2607/2627 bipolar operational amplifiers are high performance, epoxy-packaged monolithic IC's designed to deliver outstanding wideband AC performance. HA-2607 has a specified bandwidth of 12MHz while HA-2627 has a typical gain-bandwidth of 100MHz!* HA-2607 and HA-2627 also offer correspondingly high slew rates of 7V/μ Sec and 35V/μ Sec respectively. These dynamic characteristics, coupled with 150,000V/V open-loop gain enables HA-2607/2627 to perform high-gain amplification of very fast, wideband signals.

The HA-2607 and HA-2627 op amps afford an economical means of designing high performance equipment for industrial and commercial use. These amplifiers are ideally suited to pulse amplification designs as well as high frequency (e.g. RF, video) applications. The frequency response of both amplifiers can be tailored to exact design requirements by means of an external bandwidth control capacitor.

*HA-2607/2627 are internally compensated—HA-2607 is stable for $A_V \geq 1$,—HA-2627 is stable for $A_V \geq 5$.

PIN CONFIGURATION

PACKAGE DIMENSIONS

SCHEMATIC

*VALUES OF C3 AND C4 VARY DEPENDING ON DEVICE TYPE.

5

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals 45.0V
Differential Input Voltage ..... ±12.0V
Peak Output Current ..... Full Short Circuit Protection
Internal Power Dissipation (Note 10) 300mW
Operating Temperature Range—
HA-2607/HA-2627 ..... $0° \leq T_A \leq +75°C$
Storage Temperature Range ... $-65°C \leq T_A \leq +150°C$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

ELECTRICAL CHARACTERISTICS $V^+ = +15VDC$, $V^- = -15VDC$

PARAMETER	TEMP.	HA-2607 0°C to +75°C LIMITS MIN.	TYP.	MAX.	HA-2627 0°C to +75°C MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS								
Offset Voltage	+25°C		4	6		4	6	mV
	Full			8			8	mV
Offset Voltage Average Drift	Full		5			5	30	nA
Bias Current	+25°C		5	30		5	30	nA
	Full			50			50	
Offset Current	+25°C		5	30		5	30	nA
	Full			50			50	nA
Input Resistance	+25°C	40	300		40	300		MΩ
Common Mode Range	Full	±10.0			±10.0			V
TRANSFER CHARACTERISTICS								
Large Signal Voltage Gain (Note 1)	+25°C	70	150K		70	150K		V/V
	Full	60			60			V/V
Common Mode Rejection Ratio (Note 2)	Full	74	100		74	100		dB
Gain Bandwidth Product (Note 3, 11)	+25°C		12			100		MHz
OUTPUT CHARACTERISTICS								
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±18		±10	±18		mA
Full Power Bandwidth (Note 4)	+25°C	50	75		290	600		kHz
TRANSIENT RESPONSE								
Rise Time (Notes 1, 5, 6 & 8)	+25°C		30	60		17	45	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	40		25	40	%
Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±4	±7		±17	±35		V/μs
Settling Time (Notes 1, 4, 5 & 8)	+25°C		1.5			1.5		μs
POWER SUPPLY CHARACTERISTICS								
Supply Current	+25°C		3.0	4.0		3.0	4.0	mA
Power Supply Rejection Ratio (Note 9)	Full	74	90		74	90		dB

Notes:
1. $R_L = 2K$
2. $V_{CM} = +5.0V$
3. $V_O < 90mV$
4. $V_O = +10V$
5. $C_L = 100pF$
6. $V_L = +200mV$
7. $V_O = +400mV$
8. For HA-2607, $A_V = 1$; For HA-2627, $A_V = 5$.
9. $V_S = +9.0V$ to $+15V$
10. Derate by 6.6mW/°C above 105°C
11. 40 dB gain setting used to measure Gain-Band width for HA-2627

5

INTERSIL

High Slew Rate Operational Amplifiers HA 2500/02/05/10/12/15/20/22/25

FEATURES

- Slew Rate – Up to 120 V/μs
- Settling Time – 200 ns to 0.1%
- Bias Current – 100 nA
- Gain Bandwidth Product – 30 MHz
- Internal Frequency Compensation
- Radiation Hardened
- Meets MIL-STD-883

GENERAL DESCRIPTION

The 2500 series of high slew rate operational amplifiers are monolithic integrated circuits fabricated using dielectric isolation and thin film resistors. These internally compensated amplifiers feature excellent input parameters, high gain and wide bandwidth. They are ideally suited for D/A and A/D converter circuits, pulse amplifiers and high frequency buffer amplifiers.

2500 through 2515 are compensated for unity gain. 2520 through 2525 are intended for closed loop gains of 3 or greater, and feature increased slew rates and gain-bandwidth products.

VOLTAGE OFFSET NULL CIRCUIT

PIN CONFIGURATIONS

(TOP VIEW)

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE	ORDER NUMBER
2500	-55°C to +125°C	TO-99 Flat Pack	HA2-2500-2 * HA9-2500-2 *
2502	-55°C to +125°C	TO-99 Flat Pack	HA2-2502-2 * HA9-2502-2 *
2505	0°C to +75°C	TO-99 Flat Pack	HA2-2505-5 HA9-2505-5
2510	-55°C to +125°C	TO-99 Flat Pack	HA2-2510-2 * HA9-2510-2 *
2512	-55°C to +125°C	TO-99 Flat Pack	HA2-2512-2 * HA9-2512-2 *
2515	0°C to +75°C	TO-99 Flat Pack	HA2-2515-5 HA9-2515-5
2520	-55°C to +125°C	TO-99 Flat Pack	HA2-2520-2 * HA9-2520-2 *
2522	-55°C to +125°C	TO-99 Flat Pack	HA2-2522-2 * HA9-2522-2 *
2525	0°C to +75°C	TO-99 Flat Pack	HA2-2525-5 HA9-2525-5

*883 processing is available for these devices.
Order -8 instead of -2.

5

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±20V
Input Voltage (Note 1) . . . . . ±15V
Differential Input Voltage . . . . . ±15V
Peak Output Current . . . . . ±50 mA
Internal Power Dissipation (Note 2) . . . . . 300 mW
Lead Temperature (Soldering, 60 sec) . . . . . 300°C
Storage Temperature Range . . . . . -65°C to +150°C
Operating Temperature Range . . . . . -55°C to +125°C (2500, 2502)
0°C to +75°C (2505)

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±15V unless otherwise specified)

PARAMETER	CONDITIONS	2500			2502			2505			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$R_S \leq 10\ k\Omega$		2	5		4	8		4	8	mV
Input Offset Current			10	25		20	50		20	50	nA
Input Resistance		25	50		20	50		20	50		MΩ
Large Signal Voltage Gain	R_L = 2kΩ, V_O = ±10V	20k	30k		15k	25k		15k	25k		V/V
Gain Bandwidth	$A_V > 10$		12			12			12		MHz
Full Power Bandwidth	R_L = 2kΩ, C_L = 50pF, V_O = 20Vp-p	350	500		300	500		300	500		kHz
Rise Time (Notes 3,4)	R_L = 2kΩ, C_L = 50pF		25	50		25	50		25	50	ns
Overshoot (Notes 3,4)	R_L = 2kΩ, C_L = 50pF		25	40		25	50		25	50	%
Slew Rate (Note 3)	R_L = 2kΩ, C_L = 50pF, V_O = ±5V	±25	±30		±20	±30		±20	±30		V/μs
Settling Time (to 0.1% of Final Value) (Note 3)	R_L = 2kΩ, C_L = 50pF, V_O = ±5V		330			330			330		ns
Output Current	V_O = ±10V	±10			±10			±10			mA
Supply Current			4	6		4	6		4	6	mA

THE FOLLOWING SPECIFICATIONS APPLY FOR OPERATING TEMPERATURE RANGE

Input Offset Voltage	$R_S \leq 10\ k\Omega$			8			10			10	mV
Input Offset Current				50			100			100	nA
Input Bias Current	+25°C to +125°C		100	200		125	250				nA
	-55°C to +25°C		200	400		250	500				nA
	+25°C to +75°C								125	250	nA
	0°C to +25°C								250	500	nA
Offset Voltage Average Drift	$R_S \leq 10\ k\Omega$		20			20			20		μV/°C
Offset Current Average Drift			0.1			0.1			0.1		nA/°C
Common Mode Rejection Ratio	V_{CM} = ±5V	80	90		74	90		74	90		dB
Common Mode Range		±10			±10			±10			V
Supply Voltage Rejection Ratio	ΔV = ±5V	80	90		74	90		74	90		dB
Large Signal Voltage Gain	R_L = 2kΩ, V_O = ±10V	7.5k			5k			10k			V/V
Output Voltage Swing	R_L = 2kΩ	±10	±12		±10	±12		±10	±12		V

NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
NOTE 2: Derate TO-86 at 4.5 mW/°C above 84°C; derate TO-99 at 6.6 mW/°C above 105°C.
NOTE 3: A_V = 1.
NOTE 4: V_O = 400 mV_{p-p}.

TRANSIENT RESPONSE

SLEW RATE AND SETTLING TIME

SLEW RATE AND TRANSIENT RESPONSE

SUGGESTED OFFSET ZERO ADJUST HOOK-UP

NOTE: Measured on both positive and negative transitions.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±20V
Input Voltage (Note 1) . . . . . ±15V
Differential Input Voltage . . . . . ±15V
Peak Output Current . . . . . ±50 mA
Internal Power Dissipation (Note 2) . . . . . 300 mW
Lead Temperature (Soldering, 60 sec) . . . . . 300°C
Storage Temperature Range . . . . . -65°C to +150°C
Operating Temperature Range . . . . . -55°C to +125°C (2510, 2512)
0°C to +75°C (2515)

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±15V unless otherwise specified)

PARAMETER	CONDITIONS	2510 MIN	2510 TYP	2510 MAX	2512 MIN	2512 TYP	2512 MAX	2515 MIN	2515 TYP	2515 MAX	UNITS
Input Offset Voltage	$R_S \leq 10\ k\Omega$		4	8		5	10		5	10	mV
Input Offset Current			10	25		20	50		20	50	nA
Input Resistance		50	100		40	100		40	100		MΩ
Large Signal Voltage Gain	R_L = 2 kΩ, V_O = ±10V	10k	15k		7.5k	15k		7.5k	15k		V/V
Gain Bandwidth	$A_V > 10$		12			12			12		MHz
Full Power Bandwidth	R_L = 2kΩ, C_L = 50pF, V_O = 20Vp-p	750	1000		600	1000		600	1000		kHz
Rise Time (Notes 3,4)	R_L = 2kΩ, C_L = 50pF		25	50		25	50		25	50	ns
Overshoot (Notes 3,4)	R_L = 2kΩ, C_L = 50pF		25	40		25	50		25	50	%
Slew Rate (Note 3)	R_L = 2kΩ, C_L = 50pF, V_O = ±5V	±50	±65		±40	±60		±40	±60		V/μs
Settling Time (to 0.1% of Final Value) (Note 3)	R_L = 2kΩ, C_L = 50pF, V_O = ±5V		250			250			250		ns
Output Current	V_O = ±10V	±10			±10			±10			mA
Supply Current			4	6		4	6		4	6	
THE FOLLOWING SPECIFICATIONS APPLY FOR OPERATING TEMPERATURE RANGE											
Input Offset Voltage	$R_S \leq 10\ k\Omega$			11			14			14	mV
Input Offset Current				50			100			100	nA
Input Bias Current	+25°C to +125°C		100	200		125	250				nA
	-55°C to +25°C		200	400		250	500				nA
	+25°C to +75°C								125	250	nA
	0°C to +25°C								250	500	nA
Offset Voltage Average Drift	$R_S \leq 10\ k\Omega$		20			30			30		μV/°C
Offset Current Average Drift			0.1			0.1			0.1		nA/°C
Common Mode Rejection Ratio	V_{CM} = ±5V	80	90		74	90		74	90		dB
Common Mode Range		±10			±10			±10			V
Supply Voltage Rejection Ratio	ΔV = ±5V	80	90		74	90		74	90		dB
Large Signal Voltage Gain	R_L = 2kΩ, V_O = ±10V	7.5k			5k			5k			V/V
Output Voltage Swing	R_L = 2kΩ	±10	±12		±10	±12		±10	±12		V

NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
NOTE 2: Derate TO-86 at 4.5 mW/°C above 84°C; derate TO-99 at 6.6 mW/°C above 105°C.
NOTE 3: A_V = 1.
NOTE 4: V_O = 400 $mV_{p=p}$.

TRANSIENT RESPONSE

SLEW RATE AND SETTLING TIME

SLEW RATE AND TRANSIENT RESPONSE

SUGGESTED OFFSET ZERO ADJUST HOOK-UP

NOTE: Measured on both positive and negative transitions.

5

ABSOLUTE MAXIMUM RATINGS

Supply Voltage . . . . . ±20V
Input Voltage (Note 1) . . . . . ±15V
Differential Input Voltage . . . . . ±15V
Peak Output Current . . . . . ±50 mA
Internal Power Dissipation (Note 2) . . . . . 300 mW
Lead Temperature (Soldering, 60 sec) . . . . . 300°C
Storage Temperature Range . . . . . -65°C to +150°C
Operating Temperature Range . . . . . -55°C to +125°C (2520, 2522)
0°C to +75°C (2525)

ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±15V unless otherwise specified)

PARAMETER	CONDITIONS	2520 MIN	2520 TYP	2520 MAX	2522 MIN	2522 TYP	2522 MAX	2525 MIN	2525 TYP	2525 MAX	UNITS
Input Offset Voltage	$R_S \leq 10\ k\Omega$		4	8		5	10		5	10	mV
Input Offset Current			10	25		20	50		20	50	nA
Input Resistance		50	100		40	100		40	100		MΩ
Large Signal Voltage Gain	R_L = 2 kΩ, V_O = ±10V	10k	15k		7.5k	15k		7.5k	15k		V/V
Gain Bandwidth	$A_V > 10$		30			30			30		MHz
Full Power Bandwidth	R_L = 2 kΩ, C_L = 50pF, V_O = 20Vp-p	1500	2000		1200	1600		1200	1600		kHz
Rise Time (Notes 3,4)	R_L = 2kΩ, C_L = 50pF		15	50		15	50		15	50	ns
Overshoot (Notes 3,4)	R_L = 2 kΩ, C_L = 50pF		25	40		25	50		25	50	%
Slew Rate (Note 3)	R_L = 2 kΩ, C_L = 50pF, V_O = ±5V	±100	±120		±80	±120		±80	±120		V/µs
Settling Time (to 0.1% of Final Value) (Note 3)	R_L = 2kΩ, C_L = 50pF, V_O = ±5V		200			200			200		ns
Output Current	V_O = ±10V	±10			±10			±10			mA
Supply Current			4	6		4	6		4	6	mA

THE FOLLOWING SPECIFICATIONS APPLY FOR OPERATING TEMPERATURE RANGE

Input Offset Voltage	$R_S \leq 10\ k\Omega$			11			14			14	mV
Input Offset Current				50			100			100	nA
Input Bias Current	+25°C to +125°C		100	200		125	250				nA
	-55°C to +25°C		200	400		250	500				nA
	+25°C to +75°C								125	250	nA
	0°C to +25°C								250	500	nA
Offset Voltage Average Drift	$R_S \leq 10\ k\Omega$		20			30			30		µV/°C
Offset Current Average Drift			0.1			0.1			0.1		nA/°C
Common Mode Rejection Ratio	V_{CM} = ±5V	80	90		74	90		74	90		dB
Common Mode Range		±10			±10			±10			V
Supply Voltage Rejection Ratio	ΔV = ±5V	80	90		74	90		74	90		dB
Large Signal Voltage Gain	R_L = 2 kΩ, V_O = ±10V	7.5k			5k			5k			V/V
Output Voltage Swing	R_L = 2 kΩ	±10	±12		±10	±12		±10	±12		V

NOTE 1: For supply voltage less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
NOTE 2: Derate TO-86 at 4.5 mW/°C above 84°C; derate TO-99 at 6.6 mW/°C above 105°C.
NOTE 3: A_V = 3.
NOTE 4: V_O = 600 mV_{p-p}.

TRANSIENT RESPONSE

SLEW RATE

SLEW RATE AND TRANSIENT RESPONSE

SUGGESTED OFFSET ZERO ADJUST AND BANDWIDTH CONTROL HOOK-UP

NOTE: Measured on both positive and negative transitions.

SCHEMATIC DIAGRAM

PHYSICAL DIMENSIONS

TO-99 Package

TO-86 Flat Pack

NOTE: All dimensions in inches.
Leads are gold plated Kovar.

5

INTERSIL

HA2507/2517/2527 High Slew Rate Operational Amplifier Series

FEATURES

	HA2507	HA2517	HA2527	
• High Slew Rate	30	60	120	V/μs
• Fast Settling	330	250	200	ns
• Wide Power Bandwidth	0.5	1.0	1.6	MHz
• High Gain Bandwidth	12	12	20	MHz
• High Input Impedance	50	100	100	MΩ

DESCRIPTION

HA2507/2517/2527 operational amplifiers are a series of high-performance, epoxy-packaged monolithic IC's designed to deliver excellent slew rate, bandwidth and settling time specifications. Typical slew rate specifications for HA2507, HA2517 and HA2527 are 30V/μ sec, 60V/μ sec and 120V/μsec respectively. Corresponding settling times (10V step to 0.1%) are 330ns, 250ns and 200ns for HA2507, HA2517 and HA2527 respectively. Bandwidths range from 12MHz to 20MHz. HA2507/2517/2527 are internally compensated; HA2507 and HA2517 are stable for closed loop gains (A_V) greater than or equal to unity. HA2527 is stable for $A_V > 3$.

This series of op amps affords an economical means of designing high performance equipment for industrial and commercial use. Their slew rate and settling time performance makes them ideally suited for high speed D/A, A/D and pulse amplification designs. The wide bandwidth offered by these devices also makes them valuable components in RF and video applications. HA2507/2517/2527 also deliver offset current, bias current and offset voltage specifications compatible with the requirements of accurate signal conditioning systems.

PIN CONFIGURATION

PACKAGE DIMENSIONS

SCHEMATIC

*VALUES OF C1 AND C2 VARY DEPENDING ON DEVICE TYPE.

ABSOLUTE MAXIMUM RATINGS

Voltage Between V^+ and V^- Terminals 40.0V
Differential Input Voltage ..... ±15.0V
Peak Output Current 50mA
Internal Power Dissipation 300mW
Operating Temperature Range—
HA-2507/HA-2517/HA-2527 ..... $0°C \leq T_A \leq +75°C$
Storage Temperature Range .. $-65° \leq T_A \leq +150°C$

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

ELECTRICAL CHARACTERISTICS $V^+ = +15V$ D.C., $V^- = -15V$ D.C.

PARAMETER	TEMP.	HA-2507 0°C to +75°C LIMITS MIN.	TYP.	MAX.	HA-2517 0°C to +75°C LIMITS MIN.	TYP.	MAX.	HA-2527 0°C to +75°C LIMITS MIN.	TYP.	MAX.	UNITS
INPUT CHARACTERISTICS											
Offset Voltage	+25°C		5	10		5	10		5	10	mV
	Full			14			14			14	mV
Offset Voltage Average Drift	Full		25			30			30		μV/°C
Bias Current	+25°C		125	250		125	250		125	250	nA
	Full			500			500			500	nA
Offset Current	+25°C		20	50		20	50		20	50	nA
	Full			100			100			100	nA
Input Resistance	+25°C	20	50		40	100		40	100		MΩ
Common Mode Range	Full	±10.0			±10.0			±10.0			V
TRANSFER CHARACTERISTICS											
Large Signal Voltage Gain (Note 1, 4)	+25°C	15K	25K		7.5K	15K		7.5K	15K		V/V
	Full	10K			5K			5K			V/V
Common Mode Rejection Ratio (Note 2)	Full	74	90		74	90		74	90		dB
Gain Bandwidth Product (Note 3)	+25°C		12			12			20		MHz
OUTPUT CHARACTERISTICS											
Output Voltage Swing (Note 1)	Full	±10.0	±12.0		±10.0	±12.0		±10.0	±12.0		V
Output Current (Note 4)	+25°C	±10	±20		±10	±20		±10	±20		mA
Full Power Bandwidth (Note 4)	+25°C	220	500		450	1000		750	1600		kHz
TRANSIENT RESPONSE											
Rise Times (Notes 1, 5, 6 & 8)	+25°C		25	50		25	50		25	50	ns
Overshoot (Notes 1, 5, 7 & 8)	+25°C		25	50		25	50		25	50	%
Slew Rate (Notes 1, 4, 5 & 8)	+25°C	±15	±30		±30	±60		±60	±120		V/μs
Settling Time to 0.1% (Notes 1, 4, 5 & 8)	+25°C		0.33			0.25			0.20		μs
POWER SUPPLY CHARACTERISTICS											
Supply Current	+25°C		4	6		4	6		4	6	mA
Power Supply Rejection Ratio (Note 9)	Full	74	90		74	90		74	90		dB

Notes:
1. $R_L = 2K$
2. $V_{CM} = +5.0V$
3. $A_V > 10$
4. $V_O = +10.0V$
5. $C_L = 50pF$
6. $V_O = +400mV$ for HA-2507 and HA-2517; $V_O = +200mV$ for HA-2527
7. $V_O = +600mV$
8. For HA-2507 and HA-2517, $A_V = 1$; For HA-2527, $A_V = 3$
9. $\Delta V = +5.0V$

5

INTERSIL

ICL 8017
High Speed Inverting Amplifier

FEATURES

- 130 V/μs Slew Rate
- Fast Settling Time
- 50 nA Input Current
- 10 MHz Bandwidth
- Simple Frequency Compensation
- Short Circuit Protection

APPLICATIONS

- High Speed Inverting Amplifier
- D/A Converter
- A/D Converter
- Pulse Amplifier
- Active Filter
- Sample and Hold Circuit
- Peak Detector

GENERAL DESCRIPTION

The Intersil 8017 integrated circuit is a high speed inverting amplifier combining excellent input characteristics with wide bandwidth and high slew rate. Frequency compensation is achieved with the minimum number of external components. The high slew rate and fast settling time ensure exceptional performance in high speed data acquisition circuits. Full power bandwidth of 2 MHz makes the 8017 amplifier suitable for all applications where large amplitude, high frequency signals are encountered.

The 8017 is available in the military version, 8017M, with a temperature range from −55°C to +125°C and in the commercial version, 8017C, from 0°C to +70°C.

VOLTAGE OFFSET NULL CIRCUIT

SCHEMATIC DIAGRAM

CONNECTION DIAGRAM

PACKAGE DIMENSIONS

TO-100

NOTE: Pin 5 connected to case.

ORDERING INFORMATION

IC L 8017 M TW

- TW — Package: TW – 10 pin TO-5
- M — Temperature Range
  - M – Military (−55°C to +125°C)
  - C – Commercial (0°C to 70°C)
- 8017 — Device Chip Type
- L — Linear Circuit
- IC — INTERSIL INC. Circuit

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Differential Input Voltage	±30V
Input Voltage (Note 2)	±15V
Operating Temperature Range	
ICL8017M	-55°C to +125°C
ICL8017C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (60 secs)	300°C

ELECTRICAL CHARACTERISTICS (V_S = ±15V)

PARAMETER	CONDITIONS	8017M MIN	8017M TYP	8017M MAX	8017C MIN	8017C TYP	8017C MAX	UNITS
The following specifications apply for T_A = 25°C:								
Input Offset Voltage			2.0	5.0		2.0	7.0	mV
Input Current			50	200		50	200	nA
Input Noise Voltage (rms)	10 Hz to 1 MHz		20			20		μV
Large Signal Voltage Gain	R_L = 2 kΩ	25	1000		25	1000		V/mV
Output Resistance			75			75		Ω
Output Short-Circuit Current			25			25		mA
Supply Current	V_{OUT} = 0V		5.0	7.0		5.0	8.0	mA
Power Consumption	V_{OUT} = 0V		150	210		150	240	mW
Slew Rate	R_{BW} = 20 kΩ		130			130		V/μs
Unity Gain Bandwidth (Note 3)	R_{BW} = 20 kΩ		10			10		MHz
Transient Response (Note 3)	Unity Gain, R_{BW} = 20 kΩ							
Risetime			30			30		ns
Overshoot			5			5		%
Settling Time (0.1%) (Note 3)	Unity Gain, R_{BW} = 20 kΩ		1.0			1.0		μs
(.01%) (Note 3)			3.5			3.5		μs
The following specifications apply for 0°C ≤ T_A ≤ +70°C (8017C), -55°C ≤ T_A ≤ +125°C (8017M):								
Input Offset Voltage				6.0			7.5	mV
Input Current				500			500	nA
Average Temperature Coefficient of Input Offset Voltage	-55°C ≤ T_A ≤ +125°C		10					μV/°C
	0°C ≤ T_A ≤ + 70°C					10		μV/°C
Large Signal Voltage Gain		15			15			V/mV
Output Voltage Swing	R_L = 2 kΩ	±10			±10			V
Supply Voltage Rejection Ratio				300			300	μV/V
Supply Current	V_{OUT} = 0V			9.0			9.0	mA

NOTE 1: The maximum junction temperature of the 8017M is 150°C, while that of the 8017C is 100°C. For operating at elevated temperatures the package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. Above 100°C it may be necessary to use a heatsink with the 8017M to avoid exceeding the maximum chip temperature.

NOTE 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 3: Circuit and compensation as in Figure 1.

5

TYPICAL PERFORMANCE CURVES*

INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

OPTIMUM VALUE OF R_{BW} AS A FUNCTION OF CLOSED LOOP GAIN (SEE FIG. 1)

FREQUENCY RESPONSE FOR VARIOUS CLOSED LOOP GAINS

UNITY GAIN TRANSIENT RESPONSE

UNITY GAIN LARGE SIGNAL PULSE RESPONSE

OUTPUT VOLTAGE SWING AS A FUNCTION OF FREQUENCY

OPEN-LOOP FREQUENCY RESPONSE

FREQUENCY CHARACTERISTICS AS A FUNCTION OF TEMPERATURE

*8017C only guaranteed for $0°C \leq T_A \leq +70°C$

DEFINITION OF TERMS

Input Offset Voltage: Voltage which must be applied to input terminal to obtain zero output voltage.

Input Current: Current into input terminal when at ground potential.

Large Signal Voltage Gain: The ratio of maximum output swing with load to the required change in input drive voltage.

Slew Rate: The maximum rate of change of output voltage in response to a large amplitude input pulse.

Unity Gain Bandwidth: The frequency at which the small signal gain is 3 dB below its low frequency value.

Transient Response: The 10% to 90% closed loop step-function response of the amplifier under small signal conditions.

Settling Time: The elapsed time between the application of a fast input pulse and the time at which the output has settled to its final value within a specified limit of accuracy.

APPLICATIONS INFORMATION

Figure 1. Inverting Voltage Amplifier

GAIN	R_S	R_f	R_{BW}	BAND-WIDTH	SLEW RATE
1X	10 kΩ	10 kΩ	20 kΩ	10 MHz	130 V/µs
10X	10 kΩ	100 kΩ	2 kΩ	6 MHz	100 V/µs
100X	1 kΩ	100 kΩ	short	800 kHz	50 V/µs

NOTE: If no bandwidth control resistor (R_{BW}) is connected between pins 3 and 4, the amplifier is unconditionally stable for normal feedback configurations. Some improvement in frequency performance can be realized by setting R_{BW} = 20 kΩ; the amplifier will still be unconditionally stable. However, for optimum frequency response, R_{BW} should be selected from the curve on page 3, based on the closed loop gain of the circuit. Additional control of the bandwidth/stability trade-off is possible by bypassing R_f with a low value capacitor. It is not necessary to alter the value of C_1, C_2 or C_3.

Figure 2. Current Summing Amplifier

NOTE: The analog output current of the 8018 Series D/A current switches can be converted to voltage using the 8017 as shown. Input compensation of approximately 10 kΩ and 30 pF helps improve settling time.

Figure 3. Settling Time Measurement

NOTE: Settling time is measured by creating a dummy summing junction and observing the error voltage waveform on a scope. The junction is clamped with high speed diodes to avoid overdriving the scope preamp.

Figure 4. Isolation of Capacitive Loads

NOTE: Excess phase shift caused by heavy capacitive loading (above 200 to 300 pF) can cause stability problems. By providing the amplifier with a minimum real load impedance (51Ω), these difficulties can be overcome. Note that at high output currents, maximum voltage swing will be reduced.

5

INTERSIL

ICL4250/C
Programmable Operational Amplifier

FEATURES

- ±1V to ±18V power supply operation
- 3 nA input offset current
- Standby power consumption as low as 500 nW
- No frequency compensation required
- Programable electrical characteristics
- Offset Voltage nulling capability
- Can be powered by two flashlight batteries
- Short circuit protection

GENERAL DESCRIPTION

The 4250 and 4250C are extremely versatile programable monolithic operational amplifiers. A single external master bias current setting resistor programs the input bias current, input offset current, quiescent power consumption, slew rate, input noise, and the gain-bandwidth product.

The 4250C is identical to the 4250 except that the 4250C has its performance guaranteed over a 0°C to 70°C temperature range instead of the −55°C to +125°C temperature range of the 4250.

CONNECTION DIAGRAM

Order Number ICL4250TY
or ICL4250CTY

8-Lead TO-5 Metal Can

SCHEMATIC DIAGRAM

5

RESISTOR BIASING

Set Current Setting Resistor to V⁻

	I_{SET}				
V_S	0.1 μA	0.5 μA	1.0 μA	5 μA	10 μA
±1.5V	25.6 MΩ	5.04 MΩ	2.5 MΩ	492 kΩ	244 kΩ
±3.0V	55.6 MΩ	11.0 MΩ	5.5 MΩ	1.09 MΩ	544 kΩ
±6.0V	116 MΩ	23.0 MΩ	11.5 MΩ	2.29 MΩ	1.14 MΩ
±9.0V	176 MΩ	35.0 MΩ	17.5 MΩ	3.49 MΩ	1.74 MΩ
±12.0V	236 MΩ	47.0 MΩ	23.5 MΩ	4.69 MΩ	2.34 MΩ
±15.0V	296 MΩ	59.0 MΩ	29.5 MΩ	5.89 MΩ	2.94 MΩ

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V	Output Short Circuit Duration	Indefinite
Power Dissipation (Note 1)	500 mW	Operating Temperature Range	
Differential Input Voltage	±30V	4250	$-55°C \leq T_A \leq 125°C$
Input Voltage (Note 2)	±15V	4250C	$0°C \leq T_A \leq 70°C$
I_{SET} Current	150μA	Storage Temperature Range	−65°C to 150°C
		Lead Temperature (Soldering, 10 sec)	300°C

ELECTRICAL CHARACTERISTICS 4250 ($-55°C \leq T_A \leq 125°C$ unless otherwise specified)

PARAMETERS	CONDITIONS	$V_S = \pm 1.5V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		MIN	MAX	MIN	MAX
V_{OS}	$T_A = 25°$ $R_S \leq 100\ k\Omega$		3 mV		5 mV
I_{OS}	$T_A = 25°$		3 nA		10 nA
I_{bias}	$T_A = 25°$		7.5 nA		50 nA
Large Signal Voltage Gain	$T_A = 25°$ $R_L = 100\ k\Omega$	40k			
	$V_O = \pm 0.6$, $R_L = 10\ k\Omega$			50k	
Supply Current	$T_A = 25°C$		7.5 μA		80 μA
Power Consumption	$T_A = 25°C$		23 μW		240 μW
V_{OS}	$R_S \leq 100\ k\Omega$		4 mV		6 mV
I_{OS}	$T_A = 125°C$		5 nA		10 nA
	$T_A = -55°C$		3 nA		10 nA
I_{bias}			7.5 nA		50 nA
Input Voltage Range		±0.7V		±0.7V	
Large Signal Voltage Gain	$V_O = \pm 0.6V$ $R_L = 100\ k\Omega$	30k			
	$R_L = 10\ k\Omega$			30k	
Output Voltage Swing	$R_L = 100\ k\Omega$	±0.6V			
	$R_L = 10\ k\Omega$			±0.6V	
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	76 dB		76 dB	
Supply Current			8 μA		90 μA
Power Consumption			24 μW		270 μW

PARAMETERS	CONDITIONS	$V_S = \pm 15V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		MIN	MAX	MIN	MAX
V_{OS}	$T_A = 25°C$ $R_S \leq 100\ k\Omega$		3 mV		5 mV
I_{OS}	$T_A = 25°C$		3 nA		10 nA
I_{bias}	$T_A = 25°C$		7.5 nA		50 nA
Large Signal Voltage Gain	$T_A = 25°C$ $R_L = 100\ k\Omega$	100k			
	$V_O = \pm 10V$ $R_L = 10\ k\Omega$			100k	
Supply Current	$T_A = 25°C$		10 μA		90 μA
Power Consumption	$T_A = 25°C$		300 μW		2.7 mW
V_{OS}	$R_S \leq 100\ k\Omega$		4 mV		6 mV
I_{OS}	$T_A = 125°C$		25 nA		25 nA
	$T_A = -55°C$		3 nA		10 nA
I_{bias}			7.5 nA		50 nA
Input Voltage Range		±13.5V		±13.5V	
Large Signal Voltage Gain	$V_O = \pm 10V$ $R_L = 100\ k\Omega$	50k			
	$R_L = 10\ k\Omega$			50k	
Output Voltage Swing	$R_L = 100\ k\Omega$	±12V			
	$R_L = 10\ k\Omega$			±12V	
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	76 dB		76 dB	
Supply Current			11 μA		100 μA
Power Consumption			330 μW		3 mW

Note 1: The maximum junction temperature of the 4250 is 150°C, while that of the 4250C is 100°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W junction to ambient, or 45°C/W junction to case. The thermal resistance of the dual-in-line package is 125°C/W.

Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

ELECTRICAL CHARACTERISTICS 4250C ($0°C \leq T_A \leq 70°C$ unless otherwise specified)

PARAMETERS	CONDITIONS	$V_S = \pm 1.5V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		MIN	MAX	MIN	MAX
V_{OS}	$T_A = 25°C$ $R_S < 100\ k\Omega$		5 mV		6 mV
I_{OS}	$T_A = 25°C$		6 nA		20 nA
I_{bias}	$T_A = 25°C$		10 nA		75 nA
Large Signal Voltage Gain	$T_A = 25°C$ $R_L = 100\ k\Omega$	25k			
	$V_O = \pm 0.6V$ $R_L = 10\ k\Omega$			25k	
Supply Current	$T_A = 25°C$		8 μA		90 μA
Power Consumption	$T_A = 25°C$		24 μW		270 μW
V_{OS}	$R_S < 10\ k\Omega$		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		$\pm 0.6V$		$\pm 0.6V$	
Large Signal Voltage Gain	$V_O = \pm 0.6V$ $R_L = 100\ k\Omega$	25k			
	$R_L = 10\ k\Omega$			25k	
Output Voltage Swing	$R_L = 100\ k\Omega$	$\pm 0.6V$			
	$R_L = 10\ k\Omega$			$\pm 0.6V$	
Common Mode Rejection Ratio	$R_S < 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S < 10\ k\Omega$	74 dB		74 dB	
Supply Current			8 μA		90 uA
Power Consumption			24 μW		270 uW

PARAMETERS	CONDITIONS	$V_S = \pm 15V$			
		$I_{SET} = 1\ \mu A$		$I_{SET} = 10\ \mu A$	
		MIN	MAX	MIN	MAX
V_{OS}	$T_A = 25°C$ $R_S < 100\ k\Omega$		5 mV		6 mV
I_{OS}	$T_A = 25°C$		6 nA		20 nA
I_{bias}	$T_A = 25°C$		10 nA		75 nA
Large Signal Voltage Gain	$T_A = 25°C$ $R_L = 100\ k\Omega$	60k			
	$V_O = \pm 10V$ $R_L = 10\ k\Omega$			60k	
Supply Current	$T_A = 25°C$		11 μA		100 μA
Power Consumption	$T_A = 25°C$		330 μW		3 mW
V_{OS}	$R_S < 10\ k\Omega$		6.5 mV		7.5 mV
I_{OS}			8 nA		25 nA
I_{bias}			10 nA		80 nA
Input Voltage Range		$\pm 13.5V$		$\pm 13.5V$	
Large Signal Voltage Gain	$V_O = \pm 10V$ $R_L = 100\ k\Omega$	50k			
	$R_L = 10\ k\Omega$			50k	
Output Voltage Swing	$R_L = 100\ k\Omega$	$\pm 12V$			
	$R_L = 10\ k\Omega$			$\pm 12V$	
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70 dB		70 dB	
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$	74 dB		74 dB	
Supply Current			11 uA		100 uA
Power Consumption			300 uW		3 mW

5

INTERSIL Preliminary

ICL761X/ 762X/763X/764X Low Power MAXCMOS™ Operational Amplifiers

FEATURES

- Wide operating voltage range ±0.5V to ±8V
- Single Ni-cad battery operation
- High input impedance — $10^{12}\Omega$
- Programmable power consumption — as low as 10μW
- Input current lower than BIFETs — typ 1pA
- Available as singles, duals, triples, and quads
- Input voltage swing ranges to within millivolts of V^- to V^+
- Low power replacement for many standard op amps
- Compensated and uncompensated versions

APPLICATIONS

- Portable instruments
- Telephone headsets
- Hearing aid/microphone amplifiers
- Meter amplifiers
- Medical instruments
- High impedance buffers

A number of special options are available. They include:

- Single, dual, triple, and quad configurations
- Internally compensated and uncompensated versions
- Inputs protected to ±200V (ICL7613/15)
- Input common mode voltage range greater than supply rails (ICL7612)

Note: See page 2 for table of options.

SCHEMATIC

TABLE OF JUMPERS	
ICL-7611	B, F, H
ICL-7612	B, F, H
ICL-7613	B, F, H
ICL-7614	C, D, E
ICL-7615	C, D, E
ICL-7621	C, E
ICL-7622	C, E
ICL-7631	B, F
ICL-7632	B, F, H
ICL-7641	C, G
ICL-7642	A, E

NOTES:
1. HIGH VALUE THIN FILM RESISTORS ARE PRESENT ONLY ON ICL-7613 AND 7615. FOR ALL OTHER DEVICES, THEY ARE REPLACED BY DIRECT CONNECTIONS.
2. OFFSET NULLING PINS ARE NOT AVAILABLE ON TRIPLE (ICL-763X) AND QUAD (ICL-764X) VERSIONS.
3. I_Q AND COMP TERMINALS ARE METAL MASK OPTIONS OF THE SAME BONDING PAD; ONLY ONE OF THESE FUNCTIONS IS AVAILABLE IN A GIVEN DEVICE.
4. FOR INTERNALLY COMPENSATED VERSIONS ONLY. THIS CAPACITOR IS REPLACED BY A DIRECT CONNECTION FOR ALL OTHER DEVICES.

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GENERAL DESCRIPTION

The ICL761X/762X/763X/764X series is a family of monolithic CMOS op amps, fabricated using Intersils' proven MAXCMOS™ process. These amplifiers provide the designer with high performance operation at low supply voltages and selectable quiescent currents, and are an ideal design tool when ultra low input current and low power drain are essential.

The basic amplifier will operate at supply voltages ranging from ±0.5 to ±8V, and may be operated from a single Ni-Cad battery.

A unique quiescent current programming pin allows setting of standby current to 1 mA, 100 μA, or 10 μA, with no external components. This results in power drain as low as 10 μW. Output swings range to within a few millivolts of the supply voltages.

Of particular significance is the extremely low (1 pA) input current, input noise current of .01pA/√Hz, and $10^{12}\Omega$ input impedance. These features optimize performance in very high source impedance applications.

The inputs are internally protected and require no special handling procedures. Outputs are fully protected against shorts to ground or to either supply.

AC performance is excellent, with a slew rate of 1.6V/μs, and unity gain bandwidth of 1 MHz at I_Q = 1 mA.

Because of the low power dissipation, operating temperatures and drift are quite low. Applications utilizing these features may include stable instruments, extended life designs, or high density packages.

SELECTION GUIDE

BASIC TYPE

76XX

EXTERNAL OFFSET NULL CAPABILITY
Y = YES
N = NO

I_Q SETTING
L = 10μA FIXED
M = 100μA FIXED
H = 1mA FIXED
P = PROGRAMMABLE

ORDERING INFORMATION[2]

ICL76XX M N O P

V_{OS} SELECTION
A = 2mV
B = 5mV
C = 10mV
D = 15mV
E = 25mV

TEMP. RANGE
C = 0°C TO 70°C
M = -55°C TO +125°C

PACKAGE CODE
TY – TO-99, 8 PIN, PIN 4 CONNECTED TO CASE
PA – PLASTIC 8 PIN MINIDIP
PD – 14 PIN PLASTIC
PE – 16 PIN PLASTIC
JD – 14 PIN CERDIP
JE – 16 PIN CERDIP

	BASIC TYPE					ORDER SUFFIX							
						TO-99		MINI DIP	PLASTIC DIP[1]	CERAMIC DIP[1]		DIE	
	COMPENSATED	EXTERNALLY COMPENSATED	COMPENSATED/ INPUT PROTECTED	EXTERNALLY COMPENSATED INPUT PROTECTED	EXTENDED CMVR	0°C to +70°C	55°C to +125°C	0°C to +70°C	0°C to +70°C	0°C to +70°C	55°C to +125°C	0°C to +70°C	55°C to +125°C
SINGLE	7611 Y P	7614 Y M	7613 Y P	7615 Y M	7612 Y P	ACTY BCTY DCTY	AMTY BMTY —	ACPA BCPA DCPA				DC/D	
DUAL 1458 PINOUT	7621 N M					ACTY BCTY DCTY	AMTY BMTY —	ACPA BCPA DCPA				DC/D	
DUAL 747 PINOUT	7622 Y M								ACPD BCPD DCPD	ACJD BCJD DCJD	AMJD BMJD —	DC/D	
TRIPLE	7631 N P	[3] 7632 N P							BCPE CCPE ECPE	BCJE CCJE ECJE	BMJE CMJE —	EC/D	
QUAD High I_Q	7641 N H								BCPD CCPD ECPD	BCJD CCJD ECPD	BMJD CMJD —	EC/D	
QUAD Low I_Q	7642 N L								BCPD CCPD ECPD	BCJD CCJD ECJD	BCJD CCJD —	EC/D	

NOTES: 1. Duals and quads are available in 14 pin DIP packages, triples in 16 pin only.
2. Ordering code must consist of basic device and order suffix, e.g., ICL7611BCPA.
3. ICL7632 is not compensatable. Recommended for use in high gain circuits only.

CONNECTION DIAGRAMS

DEVICE	DESCRIPTION	PIN ASSIGNMENTS
ICL7611XCPA ICL7611XCTY ICL7611XMTY ICL7612XCPA ICL7612XCTY ICL7612XMTY ICL7613XCPA ICL7613XCTY ICL7613XMTY	Internal compensation, plus external offset null capability and external I_Q control.	TO-99 (TOP VIEW) 8 PIN DIP (TOP VIEW)
ICL7614XCPA ICL7614XCTY ICL7614XMTY ICL7615XCPA ICL7615XCTY ICL7615XMTY	Fixed I_Q (100μA), external compensation, and internal offset null capability.	TO-99 (TOP VIEW) 8 PIN DIP (TOP VIEW)
ICL7621XCPA ICL7621XCTY ICL7621XMTY	Dual op amps with internal compensation; I_Q fixed at 100μA Pin compatible with Texas Inst. TL082 Motorola MC1458 Raytheon RC4558	TO-99 (TOP VIEW) 8 PIN DIP (TOP VIEW)
ICL7622XCPD	Dual op amps with internal compensation; I_Q fixed at 100μA Pin compatible with Texas Inst. TL083 Fairchild μA747	14 PIN DIP (TOP VIEW) Note: Pins 9 and 13 are internally connected.

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CONNECTION DIAGRAMS (Cont.)

DEVICE	DESCRIPTION	PIN ASSIGNMENTS
ICL7631XCPE ICL7632XCPE	Triple op amps with internal compensation (ICL7631) and no compensation (ICL7632). Adjustable I_Q Same pin configuration as ICL8023.	16 PIN DIP (TOP VIEW) Note: Pins 5 and 15 are internally connected.
ICL7641XCPD ICL7642XCPD	Quad op amps with internal compensation. I_Q fixed at 1mA (ICL7641) I_Q fixed at 10μA (ICL7642) Pin compatible with Texas Instr. TL084 National LM324 Harris HA4741	14 PIN DIP (TOP VIEW)

GENERAL INFORMATION

STATIC PROTECTION

All devices are static protected by the use of input diodes. However, strong static fields should be avoided, as it is possible for the strong fields to cause degraded diode junction characteristics, which may result in increased input leakage currents.

LATCHUP AVOIDANCE

Junction-isolated CMOS circuits employ configurations which produce a parasitic 4-layer (p-n-p-n) structure. The 4-layer structure has characteristics similar to an SCR, and under certain circumstances may be triggered into a low impedance state resulting in excessive supply current. To avoid this condition, no voltage greater than 0.3V beyond the supply rails may be applied to any pin. (An exception to this rule concerns the inputs of the ICL7613 and ICL7615, which are protected to ±200V.) In general, the op amp supplies must be established simultaneously with, or before any input signals are applied. If this is not possible, the drive circuits must limit input current flow to 2 mA to prevent latchup.

CHOOSING THE PROPER I_Q

Each device in the ICL76XX family has a similar I_Q set-up scheme, which allows the amplifier to be set to nominal quiescent currents of 10 μA, 100 μA or 1 mA. These current settings change only very slightly over the entire supply voltage range. The ICL7611/12/13 and ICL7631/32 have an external I_Q control terminal, permitting user selection of each amplifiers' quiescent current. (The ICL7614/15, 7621/22, and 7641/42 have fixed I_Q settings — refer to selector guide for details.) To set the I_Q of programmable versions, connect the I_Q terminal as follows:

I_Q = 10μA — I_Q pin to V^+

I_Q = 100μA — I_Q pin to ground. If this is not possible, any voltage from V^+ -0.8 to V^- +0.8 can be used.

I_Q = 1mA — I_Q pin to V^-

NOTE: The negative output current available is a function of the quiescent current setting. For maximum p-p output voltage swings into low impedance loads, I_Q of 1 mA should be selected.

OUTPUT STAGE AND LOAD DRIVING CONSIDERATIONS

Each amplifiers' quiescent current flows primarily in the output stage. This is approximately 70% of the I_Q settings. This allows output swings to almost the supply rails for output loads of 1M, 100K, and 10K, using the output stage in a highly linear class A mode. In this mode, crossover distortion is avoided and the voltage gain is maximized. However, the output stage can also be operated in Class AB, which can supply

higher output currents. (See graphs under Typical Operating Characteristics). During the transition from Class A to Class B operation, the output transfer characteristic is non-linear and the voltage gain decreases.

A special feature of the output stage is that it approximates a transconductance amplifier, and its gain is directly proportional to load impedance. Approximately the same open loop gains are obtained at each of the I_Q settings if loads of 10K, 100K, and 1M respectively are used.

INPUT OFFSET NULLING

For those models provided with OFFSET NULLING pins, nulling may be achieved by connecting a 25K pot between the OFFSET terminals with the wiper connected to V^+. At quiescent currents of 1 mA and 100 μA, the nulling range provided is adequate for all V_{OS} selections; however with $I_Q = 10\mu A$, nulling may not be possible with higher values of V_{OS}.

FREQUENCY COMPENSATION

The ICL7611/12/13, 7621/22, 7631, 7641/42 are internally compensated, and are stable for closed loop gains as low as unity for capacitive loads up to 100pF.

The ICL7614 and 15 are externally compensated by connecting a capacitor between the COMP and OUT pins. A 33pF capacitor is required for unity gain compensation; for greater than unity gain applications, increased bandwidth and slew rate can be obtained by reducing the value of the compensating capacitor.

Since the g_m of the first stage is proportional to $\sqrt{I_Q}$, greatest compensation is required when $I_Q = 1$ mA. The ICL7632 is not compensated internally, nor can it be compensated externally. The device is stable when used as follows:

I_Q of 1 mA for gains ≥ 20
I_Q of 100 μA for gains ≥ 10
I_Q of 10 μA for gains ≥ 5

HIGH VOLTAGE INPUT PROTECTION

The ICL7613 and 7615 include on-chip thin film resistors and clamping diodes which allow voltages of up to ±200 to be applied to either input for an indefinite time without device failure. These devices will be useful where high common mode voltages, differential mode voltages, or high transients may be experienced. Such conditions may be found when interfacing separate systems with separate supplies.

EXTENDED COMMON MODE INPUT RANGE

The ICL7612 incorporates additional processing which allows the input CMVR to exceed each power supply rail by 0.1 volt for applications where $V_{SUPP} \geq \pm 1.5V$. For those applications where $V_{SUPP} \leq \pm 1.5V$, the input CMVR is limited to the magnitude of the positive supply rail in the positive direction, but may exceed the negative supply rail by 0.1 volt in the negative direction (eg. for $V_{SUPP} = \pm 0.5V$, the input CMVR would be +0.5 volts to -0.6 volts).

OPERATION AT $V_{SUPP} = \pm 0.5$ VOLTS

Operation at $V_{SUPP} = \pm 0.5V$ is guaranteed at $I_Q = 10\mu A$ only. This applies to these devices with selectable I_Q, and those devices are set internally to $I_Q = 10\mu A$ (i.e., ICL7611, 7612, 7613, 7631, 7632, 7642).

Output swings to within a few millivolts of the supply rails are achievable for $R_L \geq 1$ MegΩ. Guaranteed input CMVR is ±0.1V minimum and typically +0.4V to -0.2 at $V_{SUPP} = \pm 0.5V$. For applications where greater common mode range is desirable, refer to description of ICL7612 above.

The user is cautioned that, due to extremely high input impedances, care must be exercised in layout, construction, board cleanliness, and supply filtering to avoid hum and noise pickup.

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ABSOLUTE MAXIMUM RATINGS[1]

Total Supply Voltage V^+ to V^- 18V
Positive Supply Voltage V^+ to GND 18V
Negative Supply Voltage V^- to GND ..... -18V
Input Voltage ..... V^++0.3 to V^- -0.3V
Input Voltage ICL7613/15 Only .... V^++200 to V^- -200V
Differential Input Voltage .... $\pm|(V^+ + 0.3) - (V^- - 0.3)|$V
Differential Input Voltage
ICL7613/15 Only ..... $\pm|(V^+ + 200) - (V^- - 200)|$V
Duration of Output Short Circuit[2] ..... Unlimited
Continuous Power Dissipation @ 25°C — Above 25°C derate as follows:

TO-99	250mW	2mW/°C
8 Lead Minidip	250mW	2mW/°C
14 Lead Plastic	375mW	3mW/°C
14 Lead Cerdip	500mW	4mW/°C
16 Lead Plastic	375mW	3mW/°C
16 Lead Cerdip	500mW	4mW/°C

Storage Temperature Range ..... -55°C to +150°C
Operating Temperature Range
M Series ..... -55°C to +125°C
C Series ..... 0°C to +70°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

Notes:

1. Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

2. The outputs may be shorted to ground or to either supply, for $V_{SUPP} \leq 10V$. Care must be taken to insure that the dissipation rating is not exceeded.

ELECTRICAL CHARACTERISTICS V_{SUPP} = ±5.0V, T_A = 25°C, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	76XXA MIN.	76XXA TYP.	76XXA MAX.	76XXB MIN.	76XXB TYP.	76XXB MAX.	76XXD MIN.	76XXD TYP.	76XXD MAX.	UNITS
Input Offset Voltage	V_{OS}	R_S≤100KΩ, T_A=25°C T_{MIN}≤T_A≤T_{MAX}			2 3			5 7			15 20	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	R_S≤100KΩ		10			15			25		μV/°C
Input Offset Current	I_{OS}	T_A=25°C ΔT_A=C[2] ΔT_A=M[2]		0.5	30 300 800		0.5	30 300 800		0.5	30 300 800	pA
Input Bias Current	I_{BIAS}	T_A=25°C ΔT_A=C ΔT_A=M		1.0	50 400 4000		1.0	50 400 4000		1.0	50 400 4000	pA
Common Mode Voltage Range (Except ICL7612)	V_{CMR}	I_Q=10μA[1] I_Q=100μA I_Q=1mA[1]	±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			V
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMR}	I_Q=10μA[1]	±5.3			±5.3			±5.3			V
		I_Q=100μA	+5.3 -5.1			+5.3 -5.1			+5.3 -5.1			
		I_Q=1mA[1]	+5.3 -4.5			+5.3 -4.5			+5.3 -4.5			
Output Voltage Swing	V_{OUT}	R_L=100KΩ, T_A=25°C ΔT_A=C ΔT_A=M	±4.9 ±4.8 ±4.6			±4.9 ±4.8 ±4.6			±4.9 ±4.8 ±4.6			V
		R_L=10KΩ, T_A=25°C R_L=10KΩ, ΔT_A=C R_L=10KΩ, ΔT_A=M	±4.5 ±4.3 ±4.0			±4.5 ±4.3 ±4.0			±4.5 ±4.3 ±4.0			
Large Signal Voltage Gain	A_{VOL}	V_O=4.0V, R_L=1MΩ I_Q=10μA[1], T_A=25°C ΔT_A=C ΔT_A=M	90 85 77	104		80 75 68	104		80 75 68	104		dB
		V_O=4.0V, R_L=10KΩ I_Q=100μA, T_A=25°C ΔT_A=C ΔT_A=M	90 85 77	102		80 75 68	102		80 75 68	102		
		V_O=4.0V, R_L=100KΩ I_Q=1mA[1], T_A=25°C ΔT_A=C ΔT_A=M	90 85 77	98		80 75 68	98		80 75 68	98		
Unity Gain Bandwidth	G_{BW}	I_Q=10μA[1] I_Q=100μA I_Q=1mA[1]		0.044 0.48 1.4			0.044 0.48 1.4			0.044 0.48 1.4		MHz
Input Resistance	R_{IN}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	R_S≤100KΩ, I_Q=10μA[1] R_S≤100KΩ, I_Q=100μA R_S≤100KΩ, I_Q=1mA[1]	76 76 66	96 91 87		70 70 60	96 91 87		70 70 60	96 91 87		dB
Power Supply Rejection Ratio	PSRR	R_S≤100KΩ, I_Q=10μA[1] R_S≤100KΩ, I_Q=100μA R_S≤100KΩ, I_Q=1mA[1]	80 80 70	94 86 77		80 80 70	94 86 77		80 80 70	94 86 77		dB
Input Referred Noise Voltage	e_n	R_S=100Ω, f=1KHz		100			100			100		nV/√Hz
Input Referred Noise Current	i_n	R_S=100Ω, f=1KHz		0.01			0.01			0.01		pA/√Hz
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load I_Q=10μA[1] I_Q=100μA I_Q=1mA[1]		0.01 0.1 1.0	0.02 0.25 2.5		0.01 0.1 1.0	0.02 0.25 2.5		0.01 0.1 1.0	0.02 0.25 2.5	mA
Channel Separation	V_{O1}/V_{O2}	A_{VOL}=100		120			120			120		dB
Slew Rate	SR	A_{VOL}=1, C_L=100pF, V_{IN}=8V I_Q=10μA[1], R_L=1MΩ I_Q=100μA, R_L=100KΩ I_Q=1mA[1], R_L=10KΩ		0.016 0.16 1.6			0.016 0.16 1.6			0.016 0.16 1.6		V/μs
Rise Time	t_r	V_{IN}=20μV, C_L=100pF I_Q=10μA[1], R_L=1MΩ I_Q=100μA, R_L=100KΩ I_Q=1mA[1], R_L=10KΩ		20 2 0.9			20 2 0.9			20 2 0.9		μs
Overshoot Factor		V_{IN}=20μV, C_L=100pF I_Q=10μA[1], R_L=1MΩ I_Q=100μA, R_L=100KΩ I_Q=1mA[1], R_L=10KΩ		5 10 40			5 10 40			5 10 40		%

Note: 1. ICL7611, 7612, 7613 only.
2. C = Commercial Temperature Range: 0°C to +70°C
M = Military Temperature Range: -55°C to +125°C

ELECTRICAL CHARACTERISTICS $V_{SUPP} = \pm 0.5V$, $I_Q = 10\mu A$, $T_A = 25°C$, unless otherwise specified. Specs apply to ICL7611/7612/7613 only.

PARAMETER	SYMBOL	CONDITIONS	76XXA MIN.	76XXA TYP.	76XXA MAX.	76XXB MIN.	76XXB TYP.	76XXB MAX.	76XXD MIN.	76XXD TYP.	76XXD MAX.	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 100K\Omega$, $T_A=25°C$ $T_{MIN} \le T_A \le T_{MAX}$			2 3			5 7			10 12	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \le 100K\Omega$		10			15			25		$\mu V/°C$
Input Offset Current	I_{OS}	$T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		0.5	30 300 800		0.5	30 300 800		0.5	30 300 800	pA
Input Bias Current	I_{BIAS}	$T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		1.0	50 500 4000		1.0	50 500 4000		1.0	50 500 4000	pA
Common Mode Voltage Range (Except ICL7612)	V_{CMR}		±0.1			±0.1			±0.1			V
Extended Common Mode Voltage Range (ICL7612 Only)	V_{CMR}		+0.1 to -0.6			+0.1 to -0.6			+0.1 to -0.6			V
Output Voltage Swing	V_{OUT}	$R=1M\Omega$, $T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		±0.49 ±0.48 ±0.41			±0.49 ±0.48 ±0.41			±0.49 ±0.48 ±0.41		V
		$R=100K\Omega$, $T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		±0.49 ±0.48 ±0.41			±0.49 ±0.48 ±0.41			±0.49 ±0.48 ±0.41		
Large Signal Voltage Gain	A_{VOL}	$V_O=\pm 0.1V$, $R_L=1M\Omega$ $T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		90 80 70			90 80 70			90 80 70		dB
		$V_O=\pm 0.1V$, $R_L=100K\Omega$ $T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		80 70 60			80 70 60			80 70 60		
Unity Gain Bandwidth	G_{BW}			0.044			0.044			0.044		MHz
Input Resistance	R_{IN}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	$R_S \le 100K\Omega$		80			80			80		dB
Power Supply Rejection Ratio	PSRR	$R_S \le 100K\Omega$		80			80			80		dB
Input Referred Noise Voltage	e_n	$R_S=100\Omega$; f=1KHz		100			100			100		$nV/\sqrt{Hz}$
Input Referred Noise Current	i_n	$R_S=100\Omega$, f=1KHz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load		6	15		6	15		6	15	μA
Channel Separation	V_{O1}/V_{O2}	$A_{VOL}=100$		120			120			120		dB
Slew Rate	SR	$A_{VOL}=1$, $C_L=100pF$, $V_{IN}=8V$ $R_L=1M\Omega$		0.016			0.016			0.016		V/μs
Rise Time	t_r	$V_{IN}=20\mu V$, $C_L=100pF$ $R_L=1M\Omega$		20			20			20		μs
Overshoot Factor		$V_{IN}=20\mu V$, $C_L=100pF$ $R_L=1M\Omega$		5			5			5		%

Note: C = Commercial Temperature (0°C to +70°C) Range; M = Military Temperature (-55°C to +125°C) Range.

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ELECTRICAL CHARACTERISTICS V_{SUPP}= ±5.0V, T_A = 25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	76XXB MIN.	76XXB TYP.	76XXB MAX.	76XXD MIN.	76XXD TYP.	76XXD MAX.	76XXE MIN.	76XXE TYP.	76XXE MAX.	UNITS
Input Offset Voltage	V_{OS}	R_S≤100KΩ, T_A=25°C T_{MIN}≤T_A≤T_{MAX}			5 7			10 15			20 25	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	R_S≤100KΩ		15			20			30		μV/°C
Input Offset Current	I_{OS}	T_A=25°C ΔT_A=C ΔT_A=M		0.5	30 300 800		0.5	30 300 800		0.5	30 300 800	pA
Input Bias Current	I_{BIAS}	T_A=25°C ΔT_A=C ΔT_A=M		1.0	50 500 4000		1.0	50 500 4000		1.0	50 500 4000	pA
Common Mode Voltage Range (Except ICL7612)	V_{CMR}	I_Q=10μA[1] I_Q=100μA I_Q=1mA[2]	±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			±4.4 ±4.2 ±3.7			V
Output Voltage Swing	V_{OUT}	R_L=100KΩ, T_A=25°C ΔT_A=C ΔT_A=M	±4.9 ±4.8 ±4.5			±4.9 ±4.8 ±4.5			±4.9 ±4.8 ±4.5			V
		R_L=10KΩ, T_A=25°C R_L=10KΩ, ΔT_A=C R_L=10KΩ, ΔT_A=M	±4.5 ±4.3 ±4.0			±4.5 ±4.3 ±4.0			±4.5 ±4.3 ±4.0			
Large Signal Voltage Gain	A_{VOL}	V_O=4.0V, R_L=1MΩ[1] I_Q=10μA[1], T_A=25°C ΔT_A=C ΔT_A=M	86 81 74	104		86 81 74	104		86 81 74	104		dB
		V_O=4.0V, R_L=100KΩ I_Q=100μA, T_A=25°C ΔT_A=C ΔT_A=M	86 81 74	102		86 81 74	102		86 81 74	102		
		V_O=4.0V, R_L=10KΩ I_Q=1mA[1], T_A=25°C ΔT_A=C ΔT_A=M	86 81 74	98		86 81 74	98		86 81 74	98		
Unity Gain Bandwidth	G_{BW}	I_Q=10μA[1] I_Q=100μA I_Q=1mA[2]		0.044 0.48 1.4			0.044 0.48 1.4			0.044 0.48 1.4		MHz
Input Resistance	R_{IN}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	R_S≤100KΩ, I_Q=10μA[1] R_S≤100KΩ, I_Q=100μA R_S≤100KΩ, I_Q=1mA[2]	76 76 66	96 91 87		70 70 60	96 91 87		70 70 60	96 91 87		dB
Power Supply Rejection Ratio	PSRR	R_S≤100KΩ, I_Q=10μA[1] R_S≤100KΩ, I_Q=100μA R_S≤100KΩ, I_Q=1mA[2]	80 80 70	94 86 77		80 80 70	94 86 77		80 80 70	94 86 77		dB
Input Referred Noise Voltage	e_n	R_S=100Ω, f=1KHz		100			100			100		nV/√Hz
Input Referred Noise Current	i_n	R_S=100Ω, f=1KHz		0.01			0.01			0.01		pA/√Hz
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load I_Q=10μA[1] I_Q=100μA I_Q=1mA[2]		0.01 0.1 1.0	0.022 0.25 2.5		0.01 0.1 1.0	0.022 0.25 2.5		0.01 0.1 1.0	0.022 0.25 2.5	mA
Channel Separation	V_{O1}/V_{O2}	A_{VOL}=100		120			120			120		dB
Slew Rate	SR	A_{VOL}=1, C_L=100pF, V_{IN}=8V I_Q=10μA[1], R_L=1MΩ I_Q=100μA, R_L=100KΩ I_Q=1mA[1], R_L=10KΩ[2]		0.016 0.16 1.6			0.016 0.16 1.6			0.016 0.16 1.6		V/μs
Rise Time	t_r	V_{IN}=20μV, C_L=100pF I_Q=10μA[1], R_L=1MΩ I_Q=100μA, R_L=100KΩ I_Q=1mA[2], R_L=10KΩ		20 2 0.9			20 2 0.9			20 2 0.9		μs
Overshoot Factor		V_{IN}=20μV, C_L=100pF I_Q=10μA[1], R_L=1MΩ I_Q=100μA, R_L=100KΩ I_Q=1mA[2], R_L=10KΩ		5 10 40			5 10 40			5 10 40		%

Note: 1. Does not apply to 7641.
2. Does not apply to 7642.
C = Commercial Temperature Range: 0°C to +70°C
M = Military Temperature Range: -55°C to +125°C

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ELECTRICAL CHARACTERISTICS $V_{SUPP} = \pm 0.5V$, $I_Q = 10\mu A$, $T_A = 25°C$, unless otherwise specified. Specs apply to ICL7631/7632/7642 only.

PARAMETER	SYMBOL	CONDITIONS	76XXB MIN.	76XXB TYP.	76XXB MAX.	76XXD MIN.	76XXD TYP.	76XXD MAX.	76XXE MIN.	76XXE TYP.	76XXE MAX.	UNITS
Input Offset Voltage	V_{OS}	$R_S \le 100K\Omega$, $T_A=25°C$ $T_{MIN} \le T_A \le T_{MAX}$			5 7			10 15			10 12	mV
Temperature Coefficient of V_{OS}	$\Delta V_{OS}/\Delta T$	$R_S \le 100K\Omega$		15			20			30		$\mu V/°C$
Input Offset Current	I_{OS}	$T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		0.5	30 300 800		0.5	30 300 800		0.5 15 500		pA
Input Bias Current	I_{BIAS}	$T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		1.0	50 500 4000		1.0	50 500 4000		1.0 30 3000		pA
Common Mode Voltage Range	V_{CMR}		±0.1			±0.1			±0.1			V
Output Voltage Swing	V_{OUT}	$R=1M\Omega$, $T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		±0.49 ±0.48 ±0.41			±0.49 ±0.48 ±0.41			±0.49 ±0.48 ±0.46		V
		$R=100K\Omega$, $T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		±0.49 ±0.46 ±0.39			±0.49 ±0.46 ±0.39			±0.47 ±0.46 ±0.39		
Large Signal Voltage Gain	A_{VOL}	$V_O=\pm 0.1V$, $R_L=1M\Omega$ $T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		90 80 70			90 80 70			90 80 70		dB
		$V_O=\pm 0.1V$, $R_L=100K\Omega$ $T_A=25°C$ $\Delta T_A=C$ $\Delta T_A=M$		80 70 60			80 70 60			90 80 70		
Unity Gain Bandwidth	G_{BW}			0.044			0.044			0.044		MHz
Input Resistance	R_{IN}			10^{12}			10^{12}			10^{12}		Ω
Common Mode Rejection Ratio	CMRR	$R_S \le 100K\Omega$		80			80			80		dB
Power Supply Rejection Ratio	PSRR			80			80			80		dB
Input Referred Noise Voltage	e_n	$R_S=100\Omega$, f=1KHz		100			100			100		$nV/\sqrt{Hz}$
Input Referred Noise Current	i_n	$R_S=100\Omega$, f=1KHz		0.01			0.01			0.01		$pA/\sqrt{Hz}$
Supply Current (Per Amplifier)	I_{SUPP}	No Signal, No Load		6	15		6	15		6	15	μA
Channel Separation	V_{O1}/V_{O2}	$A_{VOL}=100$		120			120			120		dB
Slew Rate	SR	$A_{VOL}=1$, $C_L=100pF$, $V_{IN}=8V$ $R_L=1M\Omega$		0.016			0.016			0.016		$V/\mu s$
Rise Time	t_r	$V_{IN}=20\mu V$, $C_L=100pF$ $R_L=1M\Omega$		20			20			20		μs
Overshoot Factor		$V_{IN}=20\mu V$, $C_L=100pF$ $R_L=1M\Omega$		5			5			5		%

Note: C = Commercial Temperature (0°C to +70°C) Range; M = Military Temperature (-55°C to +125°C) Range.

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APPLICATIONS

Note that in no case is I_Q shown. The value of I_Q must be chosen by the designer with regard to frequency and power dissipation, and will in no way affect the operation of the circuits shown.

SIMPLE FOLLOWER

LEVEL DETECTOR

By using the ICL7612 in these applications, the circuits will follow rail to rail inputs.

PHOTOCURRENT INTEGRATOR

Low leakage currents allow integration times up to several hours.

PRECISE TRIANGLE/SQUARE WAVE GENERATOR

Since the output range swings exactly from rail to rail, frequency and duty cycle are virtually independent of power supply variations.

WAVEFORM GENERATOR

AVERAGING AC TO DC CONVERTER FOR A/D CONVERTERS SUCH AS ICL7106, 7107, 7109, 7116, 7117.

MEDICAL INSTRUMENT PREAMP

Note that A_{VOL} = 25; single Ni-cad battery operation. Input current (from sensors connected to patient) limited to < 5μA under fault conditions.

FIFTH ORDER CHEBYSHEV MULTIPLE FEEDBACK LOW PASS FILTER

The low bias currents permit high resistance and low capacitance values to be used to achieve low frequency cutoff: $f_c = 10Hz$, $A_{VOL} = 4$, Passband ripple = 0.1 dB.

Note that small capacitors (25-50pF) may be needed for stability in some cases.

SECOND ORDER BIQUAD BANDPASS FILTER

Note that I_Q on each amplifier may be different.
$A_{VOL} = 10$, $Q = 100$, $f_o = 100Hz$.

VOS NULL CIRCUIT

BURN—IN AND LIFE TEST CIRCUIT

NOTES:
1. FOR DEVICES WITH EXTERNAL COMPENSATION, USE 33pF.
2. FOR DEVICES WITH PROGRAMMABLE STANDBY CURRENT, CONNECT I_Q PIN TO V^- (I_Q = 1mA MODE).

UNITY GAIN FREQUENCY COMPENSATION

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SUPPLY CURRENT PER AMPLIFIER AS A FUNCTION OF SUPPLY VOLTAGE

SUPPLY CURRENT PER AMPLIFIER AS A FUNCTION OF FREE-AIR TEMPERATURE

INPUT BIAS CURRENT AS A FUNCTION OF TEMPERATURE

LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AS A FUNCTION OF FREE-AIR TEMPERATURE

LARGE SIGNAL DIFFERENTIAL VOLTAGE GAIN AND PHASE SHIFT AS A FUNCTION OF FREQUENCY

COMMON MODE REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE

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POWER SUPPLY REJECTION RATIO AS A FUNCTION OF FREE-AIR TEMPERATURE

EQUIVALENT INPUT NOISE VOLTAGE AS A FUNCTION OF FREQUENCY

PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF FREQUENCY

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

MAXIMUM PEAK-TO-PEAK VOLTAGE AS A FUNCTION OF FREE-AIR TEMPERATURE

MAXIMUM OUTPUT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE AS A FUNCTION OF LOAD RESISTANCE

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

VOLTAGE FOLLOWER LARGE SIGNAL PULSE RESPONSE

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CHIP TOPOGRAPHY

761X

762X

CHIP TOPOGRAPHY (Cont.)

763X

764X

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PACKAGE DIMENSIONS

8 LEAD PLASTIC MINI DIP (PA)

8 LEAD TO-99 METAL CAN (TY)

Note: Pin 4 connected to case.

14 LEAD CERDIP (JD)

16 LEAD CERDIP (JE)

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14 LEAD PLASTIC (PD)

16 LEAD PLASTIC (PE)

INTERSIL

ICL8021M, ICL8021C
Low Power Operational Amplifier

FEATURES

- ΔV_{OS} = 3 mV max (adjustable to zero)
- ±1V to ±18V Power Supply Operation.
- Power Consumption – 20 μW @ V_{SS} ± 1V
- Input Bias Current – 30 nA max
- Internal Compensation.
- Pin-For-Pin Compatible With 741.
- Short Circuit Protected.

GENERAL DESCRIPTION

The Intersil 8021 integrated circuit is a low power operational amplifier specifically designed for applications requiring very low standby power consumption over a wide range of supply voltages. The electrical characteristics of the 8021 can be tailored to a particular application by adjusting an external resistor, R_{SET}, which controls the quiescent current. This is advantageous because I_Q can be made independent of the supply voltages: it can be set to an extremely low value where power is critical, or to a larger value for high slew rate or wideband applications.

Other features of the 8021 include low input current that remains constant with temperature, low noise, high input impedance, internal compensation and pin-for-pin compatibility with the 741.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Differential Input Voltage (Note 1)	±15V
Common Mode Input Voltage (Note 1)	±15V
Output Short Circuit Duration	Indefinite
Power Dissipation (Note 2)	300 mW
Operating Temperature Range	
8021M	-55°C to +125°C
8021C	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 10 sec)	+300°C

NOTE 1: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 2: Rating applies for case temperatures to +125°C; derate linearly at 5.6 mW/°C for ambient temperatures above +95°C.

SCHEMATIC DIAGRAM

CONNECTION DIAGRAM

NOTE: Pin 4 connected to case.

ORDERING INFORMATION

VOLTAGE OFFSET NULL CIRCUIT

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ELECTRICAL CHARACTERISTICS (V_S = ±6V, I_Q = 30 μA, unless otherwise specified.)

CHARACTERISTICS	CONDITIONS	8021M MIN	8021M TYP	8021M MAX	8021C MIN	8021C TYP	8021C MAX	UNITS
The following specifications apply for T_A = 25°C:								
Input Offset Voltage	$R_S \leq 100\ k\Omega$		2	3		2	6	mV
Input Offset Current			.5	7.5		.7	10	nA
Input Bias Current			5	20		7	30	nA
Input Resistance		3	10		3	10		MΩ
Input Voltage Range	V_S = ±15V	±12	±13		±12	±13		V
Common Mode Rejection Ratio	$R_S \leq 10\ k\Omega$	70	80		70	80		dB
Supply Voltage Rejection Ratio	$R_S \leq 10\ k\Omega$		30	150		30	150	μV/V
Output Resistance	Open Loop		2			2		kΩ
Output Voltage Swing	$R_L \geq 20\ k\Omega$, V_S = ±15V	±12	±14		±12	±14		V
	$R_L \geq 10\ k\Omega$, V_S = ±15V	±11	±13		±11	±13		V
Output Short-Circuit Current			±13			±13		mA
Power Consumption	V_{OUT} = 0		360	480		360	600	μW
Slew Rate (Unity Gain)			0.16			0.16		V/μs
Unity Gain Bandwidth	R_L = 20 kΩ, V_{IN} = 20 mV		270			270		kHz
Transient Response (Unity Gain)	R_L = 20 kΩ, V_{IN} = 20 mV							
Risetime			1.3			1.3		μs
Overshoot			10			10		%
The following specifications apply for 0°C ≤ T_A ≤ +70°C (8021C) −55°C ≤ +125°C (8021M)								
Input Offset Voltage	$R_S \leq 10\ k\Omega$		2.0	4.0		2.0	7.5	mV
Input Offset Current			1.0	5		1.5	15	nA
Input Bias Current			10	15		15	50	nA
Average Temperature Coefficient of Input Offset Voltage	$R_S \leq 10\ k\Omega$		5			5		μV/°C
Average Temperature Coefficient of Input Offset Current			1.7			0.8		pA/°C
Large Signal Voltage Gain	R_L = 10 kΩ	50	200		50	200		V/mV
Output Voltage Swing	$R_L \geq 10\ k\Omega$	±10	±13		±10	±13		V

QUIESCENT CURRENT ADJUSTMENT

QUIESCENT CURRENT SETTING RESISTOR (PIN 8 TO V⁻)

V_S \ I_Q	10 μA	30 μA	100 μA	300 μA
±1.5	1.5 MΩ	470 kΩ	150 kΩ	
± 3	3.3 MΩ	1.1 MΩ	330 kΩ	100 kΩ
± 6	7.5 MΩ	2.7 MΩ	750 kΩ	220 kΩ
± 9	13 MΩ	4 MΩ	1.3 MΩ	350 kΩ
± 12	18 MΩ	5.6 MΩ	1.5 MΩ	510 kΩ
± 15	22 MΩ	7.5 MΩ	2.2 MΩ	620 kΩ

QUIESCENT CURRENT SETTING RESISTOR (PIN 8 TO V⁻)

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TYPICAL PERFORMANCE CURVES* (T_A = +25°C, V_S = ±6V, I_Q = 30 μA, unless otherwise specified.)

INPUT BIAS CURRENT VS QUIESCENT CURRENT

INPUT BIAS CURRENT VS AMBIENT TEMPERATURE

DIFFERENTIAL INPUT IMPEDANCE VS QUIESCENT CURRENT

SLEW RATE VS QUIESCENT CURRENT

FREQUENCY RESPONSE VS QUIESCENT CURRENT

PHASE MARGIN VS QUIESCENT CURRENT

OPEN-LOOP FREQUENCY RESPONSE

TRANSIENT RESPONSE

MAXIMUM LOAD VS QUIESCENT CURRENT

OUTPUT VOLTAGE SWING VS SUPPLY VOLTAGE

EQUIVALENT INPUT NOISE VOLTAGE VS FREQUENCY

EQUIVALENT INPUT NOISE CURRENT VS FREQUENCY

*ICL8021C guaranteed only for 0°C ≤ T_A ≤ +70°C

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DEFINITION OF TERMS

INPUT OFFSET VOLTAGE: That voltage which must be applied between the input terminals through two equal resistances to obtain zero output voltage.

INPUT OFFSET CURRENT: The difference in the currents into the two input terminals when the output is at zero.

INPUT BIAS CURRENT: The average of the two input currents.

INPUT VOLTAGE RANGE: The range of voltages on the input terminals for which the amplifier operates within specifications.

COMMON MODE REJECTION RATIO: The ratio of the common mode input voltage to the differential input voltage which produces the same output signal.

TRANSIENT RESPONSE: The 10% to 90% closed loop step-function response of the amplifier under small-signal conditions.

UNITY GAIN BANDWIDTH: The frequency at which the small signal gain is 3 dB below its low frequency value.

SLEW RATE: The maximum rate of change of output voltage in response to a large amplitude input pulse.

INPUT RESISTANCE: The ratio of the change in input voltage to the change in input current on either input with the other grounded.

SUPPLY CURRENT: The current required from the power supply to operate the amplifier with no load and the output at zero.

OUTPUT VOLTAGE SWING: The peak output voltage swing, referred to zero, that can be obtained without clipping.

LARGE-SIGNAL VOLTAGE GAIN: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

POWER SUPPLY REJECTION: The ratio of the change in input offset voltage to the change in power supply voltage producing it.

OUTPUT RESISTANCE: The ratio of the change in output current to the change in output voltage. The average output current is zero and operation is without feedback.

APPLICATIONS INFORMATION

Figure 1. Battery Operated Thermocouple Amplifier

A Chromel-Alumel thermocouple has an output of about 41 μV/°C. (It should be noted that the voltage-temperature relationship is only linear over a limited temperature range). The circuit shown amplifies the output signal to 1 mV/°C and provides an output impedance of less then 0.1Ω. Two 2.7V 1000 mAH mercury cells will power the circuit for the shelf life of the battery, approximately two years.

Figure 2. Light-Emitting Diode Voltage Dropout Indicator

The circuit shown uses the 8021 as a comparator to drive a light-emitting diode (H.P. 5082-4403 for example). For the values shown, the indicator will turn on if the input voltage falls below about 6V. Operating life (assuming L.E.D. off) is greater than one year.

PACKAGE OUTLINE

TO-5

NOTES: All dimensions in inches.
Dimensions as per latest J-10 committee.
Leads are gold-plated Kovar.
Package weight is 1.22 grams.

Figure 3. Low Quiescent Power Regulator

The simple regulator shown is adequate for many applications. Line regulation is 0.1%/V, load regulation is ≤ .01%/mA, input voltage range is +8V to +36V, and the quiescent power consumption is 400 μW (For V_{IN} = 10V). Additional features such as current limiting can be added in the usual manner.

INTERSIL

ICL8022
Dual Low Power Operational Amplifier

FEATURES

- Two Op Amps in a Single 14-Pin DIP.
- Electrically Identical to the 8021.

GENERAL DESCRIPTION

The Intersil 8022 consists of two low power operational amplifiers in a single 14-pin DIP. Each amplifier is identical to an 8021 low power op amp, and has separate connections for adjusting its electrical characteristics by means of an external resistor, R_{SET}, which controls the quiescent current of that amplifier.

Detailed electrical parameters for each amplifier may be found on the 8021 data sheet.

ORDERING INFORMATION

IC L 8022 M DD

- DD — Package: 14-pin Ceramic DIP
- M — Temperature Range: M – Military (–55°C to +125°C), C – Commercial (0°C to +70°C)
- 8022 — Device Type
- L — Linear Circuit
- IC — INTERSIL INC. Circuit

PACKAGE OUTLINE

NOTE: All dimensions in inches.

14-PIN CERAMIC DIP

CONNECTION DIAGRAM

TOP VIEW

5

INTERSIL

ICL8023
Triple Low Power Operational Amplifier

FEATURES

- Three Op Amps in a Single 16-Pin DIP.
- Electrically Identical to the 8021.

GENERAL DESCRIPTION

The Intersil 8023 consists of three low power operational amplifiers in a single 16-pin DIP. Each amplifier is identical to an 8021 low power op amp, and has separate connections for adjusting its electrical characteristics by means of an external resistor, R_{SET}, which controls the quiescent current of that amplifier.

Detailed electrical parameters for each amplifier may be found on the 8021 data sheet.

ORDERING INFORMATION

PACKAGE OUTLINE

NOTE: All dimensions in inches.

16-PIN CERAMIC DIP

CONNECTION DIAGRAM

TOP VIEW

INTERSIL

μA733/C, LM733/C
Differential Video Amplifier Linear Integrated Circuits

FEATURES

- 120 MHz Bandwidth
- 250 kΩ Input Resistance
- Selectable Gains of 10, 100, and 400
- No Frequency Compensation Required

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±8 V
Differential Input Voltage	±5 V
Common Mode Input Voltage	±6 V
Output Current	10 mA
Internal Power Dissipation	
Metal Can	500 mW
Flatpak	570 mW
DIP	670 mW
Operating Temperature Range (Note 1)	
Military (733)	-55°C to +125°C
Commercial (733C)	0°C to +70°C
Storage Temperature Range	-65°C to +150°C
Lead Temperature (Soldering, 60 second time limit)	300°C

CONNECTION DIAGRAMS

10-LEAD METAL CAN
(TOP VIEW)

Note: Pin 5 connected to case.

14-LEAD DIP
(TOP VIEW)

GENERAL DESCRIPTION

The 733 is a monolithic two-stage Differential Input, Differential Output Video Amplifier. Internal series-shunt feedback is used to obtain wide bandwidth, low phase distortion, and excellent gain stability. Emitter follower outputs enable the device to drive capacitive loads and all stages are current-source biased to obtain high power supply and common mode rejection ratios. It offers fixed gains of 10, 100 or 400 without external components, and adjustable gains from 10 to 400 by the use of a single external resistor. No external frequency compensation components are required for any gain option. The device is particularly useful in magnetic tape or disc file systems using phase or NRZ encoding and in high speed thin film or plated wire memories.

CHIP TOPOGRAPHY

CHIP DIMENSION 43 x 45 MILS

EQUIVALENT CIRCUIT

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE	ORDER NUMBERS
μA733HM	-55°C to +125°C	10 Lead Can	μA733HM TB
μA733HC	0°C to +70°C	10 Lead Metal Can	μA733HC TB
μA733DM	-55°C to +125°C	14 Lead DIP	μA733DM DD
μA733DC	0°C to +70°C	14 Lead DIP	μA733DC DD
LM733H	-55°C to +125°C	10 Lead Can	LM733 TB
LM733CH	0°C to +70°C	14 Lead DIP	LM733CTB
LM733D	-55°C to +125°C	10 Lead Can	LM733 DD
LM733CD	0°C to +70°C	14 Lead DIP	LM733 CDD
LM733CN	0°C to +70°C	14 Lead DIP	LM733 CPD

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733M ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±6.0 V unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		300	400	500	
Gain 2 (Note 3)		90	100	110	
Gain 3 (Note 4)		9.0	10	11	
Bandwidth	R_S = 50Ω				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	R_S = 50Ω, V_{OUT} = 1 V_{p-p}				
Gain 1			10.5		ns
Gain 2			4.5	10	ns
Gain 3			2.5		ns
Propagation Delay	R_S = 50Ω, V_{OUT} = 1 V_{p-p}				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		kΩ
Gain 2		20	30		kΩ
Gain 3			250		kΩ
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	3.0	μA
Input Bias Current			9.0	20	μA
Input Noise Voltage	R_S = 50Ω, BW = 1 kHz to 10 MHz		12		μVrms
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	V_{CM} = ±1 V, f ≤ 100 kHz	60	86		dB
Gain 2	V_{CM} = ±1 V, f = 5 MHz		60		dB
Supply Voltage Rejection Ratio					
Gain 2	ΔV_S = ±0.5 V	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.0	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		V_{p-p}
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA
The following specifications apply for −55°C ≤ T_A ≤ +125°C					
Differential Voltage Gain					
Gain 1 (Note 2)		200		600	
Gain 2 (Note 3)		80		120	
Gain 3 (Note 4)		8.0		12	
Input Resistance					
Gain 2		8.0			kΩ
Input Offset Current				5.0	μA
Input Bias Current				40	μA
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio		50			dB
Supply Voltage Rejection Ratio		50			dB
Output Offset Voltage					
Gain 1				1.5	V
Gain 2 and Gain 3				1.2	V
Output Swing		2.5			V_{p-p}
Output Sink Current		2.2			mA
Positive Supply Current				27	mA

733C ELECTRICAL CHARACTERISTICS (T_A = 25°C, V_S = ±6.0 V unless otherwise specified)

PARAMETER (see definitions)	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Differential Voltage Gain					
Gain 1 (Note 2)		250	400	600	
Gain 2 (Note 3)		80	100	120	
Gain 3 (Note 4)		8.0	10	12	
Bandwidth	R_S = 50Ω				
Gain 1			40		MHz
Gain 2			90		MHz
Gain 3			120		MHz
Risetime	R_S = 50Ω, V_{OUT} = 1 V_{p-p}				
Gain 1			10.5		ns
Gain 2			4.5	12	ns
Gain 3			2.5		ns
Propagation Delay	R_S = 50Ω, V_{OUT} = 1 V_{p-p}				
Gain 1			7.5		ns
Gain 2			6.0	10	ns
Gain 3			3.6		ns
Input Resistance					
Gain 1			4.0		kΩ
Gain 2		10	30		kΩ
Gain 3			250		kΩ
Input Capacitance	Gain 2		2.0		pF
Input Offset Current			0.4	5.0	μA
Input Bias Current			9.0	30	μA
Input Noise Voltage	R_S = 50Ω, BW = 1 kHz to 10 MHz		12		μV_{rms}
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	V_{CM} = ±1 V, f ≤ 100 kHz	60	86		dB
Gain 2	V_{CM} = ±1 V, f = 5 MHz		60		dB
Supply Voltage Rejection Ratio					
Gain 2	ΔV_S = ±0.5 V	50	70		dB
Output Offset Voltage					
Gain 1			0.6	1.5	V
Gain 2 and Gain 3			0.35	1.5	V
Output Common Mode Voltage		2.4	2.9	3.4	V
Output Voltage Swing		3.0	4.0		V_{p-p}
Output Sink Current		2.5	3.6		mA
Output Resistance			20		Ω
Power Supply Current			18	24	mA
The following specifications apply for 0°C ≤ T_A ≤ ±70°C					
Differential Voltage Gain					
Gain 1 (Note 2)		250		600	
Gain 2 (Note 3)		80		120	
Gain 3 (Note 4)		8.0		12	
Input Resistance—Gain 2		8.0			kΩ
Input Offset Current				6.0	μA
Input Bias Current				40	μA
Input Voltage Range		±1.0			V
Common Mode Rejection Ratio					
Gain 2	V_{CM} = ±1 V, f ≤ 100 kHz	50			dB
Supply Voltage Rejection Ratio					
Gain 2	ΔV_S = ±0.5 V	50			dB
Output Offset Voltage (All Gain)				1.5	V
Output Voltage Swing		2.8			V_{p-p}
Output Sink Current		2.5			mA
Power Supply Current				27	mA

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14 LEAD CERAMIC (DD)

10 LEAD METAL CAN

5

INTERSIL

ICL8061/8062
Camera Exposure Control Circuits

FEATURES
- 50pA to 500μA photocell current range
- Low power dissipation
- Track & hold ckt for mirror-up or exposure memory use.
- Direct linearized inputs for aperture values, sensitivity, manual shutter speed, etc.
- Easy switching between automatic and manual ("match needle") control.
- 4 decade shutter speed control range.
- Minimal photocell voltage for optimum lowlight operation.
- Built-in temperature compensation.
- Minimum number of external components required.
- Built in exposure timer for long manual exposures.
- Low light level warning.

GENERAL DESCRIPTION
The ICL8061 log-converts a wide range of photocell input current to a temperature compensated voltage, and adds or subtracts external control signals, such as film sensitivity (ASA rating), shutter speed, and aperture setting. It will hold on command the desired value against changes, occurring for example during SLR mirror up, and allow use of the "meter here, expose there" technique.

Analog output signals corresponding to brightness value (BV), exposure value (EV), and calculated f-stop and shutter speed are provided; these can be used to drive indicating meters. In addition, since the ICL8061 antilog-converts the required shutter speed value back to a current source, standard electronic shutters may be driven as well.

The ICL8061 also contains + and − reference voltages, which track each other and are used by other sections of the circuit for reference and control signals.

The ICL8062 is a comparator, alarm driver, and control circuit. This device converts the output signals from the ICL8061 to OVER, UNDER, and CORRECT signals which may be used to drive LEDs, servo motors, etc. It also provides indications relating to low battery voltage and slow shutter speed.

PIN CONFIGURATION

ORDERING INFORMATION

PART NUMBER	TYPE	PACKAGE	TEMPERATURE RANGE	ORDER NUMBER
8061C	Com'l	18 lead pill pack	−10°C to +55°C	ICL8061CFN
8061C	Com'l	18 lead dip	−10°C to +55°C	ICL8061CPN
8061C	Com'l	DIE	−10°C to +55°C	ICL8061C/D
8062C	Com'l	18 lead pill pack	−10°C to +55°C	ICL8062CFN
8062C	Com'l	18 lead dip	−10°C to +55°C	ICL8062CPN
8062C	Com'l	DIE	−10°C to +55°C	ICL8062C/D

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ELECTRICAL CHARACTERISTICS: ICL8061

ABSOLUTE MAXIMUM RATINGS*

V_{CC} 10V
I_{CC} REVERSE 10mA
Operating Temp Range ..... −10°C to +50°C
Storage Temp Range ..... −65°C to +125°C
Lead Soldering Temp ..... (10 sec) 300°C
Power Dissipation
(25°C) 500mW

Derate above 50°C ..... @ 0.5mW/°C
I_{IN} (all inputs) 2mA*
I_{OUT} (all outputs) 5mA*
Output short circuits to either supply ..... Indefinite
V_{IN} (any input) ..... V^- to V^+

*Short duration only

Note: Stresses above those listed may cause permanent damage to the device. Functional operation at the listed stress level is not implied. Long term exposure to absolute maximum rating conditions may affect device reliability adversely.

DC CHARACTERISTICS

V^+ to V^- = 6V, All voltages measured with respect to Analog Common, T_A = 25°C unless otherwise specified.

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Supply Voltage Range	2.8		10	V	V^+ to V^-
Supply Current	--	0.8	2.0	mA	No external loads
Regulator Section					
Output Voltage V_{REF} to Common	580	650	720	mV	
Output Voltage V^- to Common	1.16	1.30	1.40	V	
Output Current V_{REF} Source	1.0			mA	
Output Common Sink	1.0			mA	
Output Common Source	1.0			mA	
Power Supply Rejection					
V_{REF}		.5	2	mV/V	
V^-		1	4	mV/V	Note 1
Temp Coefficient		50	150	ppm/°C	
Load Regulation (min to max load)					
V_{REF}		7	40	mV	
V^-		5	20	mV	Note 1
Log Amplifier					
Input Offset Voltage @ I_{IN}	−80	−12	+60	mV	
Temp Coefficient			50	μV/°C	
Input Bias Current (I_{IN})	−20		+20	pA	
Input Bias Current @ 50°C	−120	±50	+120	pA	
Dynamic Range	50pA		500	μA	I_{REF} of 100nA Note 3
Output Scale Factor	20	30	40	mV/octave	
Reference Current Range	0.1		1	μA	NB upper range can be extended
V_{OUT} for I_{IN} = I_{REF}	−30		+30	mV	
Accuracy (full dynamic range)			±30	% of octave	
(100pA to 100μA)			±10	% of octave	Note 2
Temperature Tracking (1nA to 100μA)	−10		+10	mV	Deviation of output from 25°C
Offset Null Range	$\pm V_{OS}$				O/N pin to V^- or V_{REF} Note 4
Input Offset Voltage (I_{REF})	−5	±1	+5	mV	
Input Bias Current (I_{REF})		10	40	nA	Note 3 (measure by scale factor error for small I_{REF}
SAMPLE & HOLD (A3)					
Input Offset Voltage	−5	±1	+5	mV	
Input Bias Current		10	50	nA	
Input Leakage on CH 1/P pin			50	pA	TRK/HOLD pin LO.
Output Voltage Swing	−700		+400	mV	5kΩ load to V^-, 10kΩ to Common
Charge Injection		0.8	1.5	nC	
Trk/Hold Threshold	0.8	1.2	1.6	V	With respect to V^-
Input impedance Trk/Hold pin	100			kΩ	Resistance to V^-
Inverting Amplifiers (A4, A5)					
Input Offset Voltage	−5	±1	+5		
Input Bias Current		10	40	nA	
Output Voltage Swing	−200		+400	mV	1kΩ to common

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PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Amplifier Match					
Input Offset Voltage Differential					
A3-A4	−7	+1.5	+7	mV	
A3-A5	−7	+1.5	+7	mV	
Antilog Amplifier					
Input Scale Factor	10	15	20	mV/Octave	
Dynamic Range	.05		500	μA	I_{REF} of 100nA
Input Bias Current		15	60	nA	
V_{IN} for $I_{OUT} = I_{REF}$	−30		+30	mV	
Accuracy			±10	% of Octave	
Output Voltage Range	Common		V^+		
AC CHARACTERISTICS					
Response Time (I_{IN} 10nA to 1nA) Log Mode			5	ms	
Power-up Time (I_{IN} @ 200pA)			150	ms	

Note 1: Analog common regulated with respect to V^-; measurement of common with respect to V^- is intended.
Note 2: Measured @ I_{IN} = 1nA, I_{REF}, 100μA; center must be ±10% of interpolated value.
Note 3: Not tested directly; guaranteed by other tests or design control.
Note 4: Offset null not available on Standard 18 pin part. An offset null pin is available in die form, or as a special bonding option in a 22 pin package, or an 18 pin package with the loss of one other pin. Consult factory for details on this or other options.

ELECTRICAL CHARACTERISTICS: ICL8062

ABSOLUTE MAXIMUM RATINGS (*)

V_{CC} 10V
I_{CC} reverse *10mA
Operating Temp Range ..... −10°C to +50°C
Storage Temp Range ..... −65°C to +125°C
Lead Soldering Temp ..... (10 sec) 300°C
Power Dissipation
(25°C) 500mW
Derate above 50°C ..... @ 0.5mW/°C
I_{IN} (all inputs) 2mA*
I_{OUT} (all outputs) 25mA

Outputs short circuits
to either supply ..... Indefinite
V^- to V^+

*Short duration only
V_{IN} (any input except "Osc off) ..... V^- to V^+
V_{IN} (Osc off only) ..... V^- to (V^-+5V)

Note: Stresses above those listed may cause permanent damage to the device. Functional operation at the listed stress levels is not implied. Continuous exposure to absolute maximum rating conditions may adversely affect device reliability.

DC CHARACTERISTICS ($V+ = +6V_1$ V = gnd, TA = 25°C unless otherwise specified)

PARAMETER	MIN	TYP	MAX	UNITS	CONDITIONS
Supply Voltage Range	2.7		10	V	V^+ to V^-
Supply Current					
(one o/p low)		1	2	mA	(excludes output load current)
(two o/p low)		1.5	2.5	mA	
Input bias currents (except Osc off)			50	nA	(per comparator; see loading table)
Input Offset voltages: As to Ac,					
upper trip	+2	+7	+12	mV	
lower trip	−12	−7	−2	mV	
upper trip to lower trip point	8	14	20	mV	
Amax to As, Tmax to T	−12	−7	−2	mV	
Amin to As, Tmin to T	+2	+7	+12	mV	
Tslo to T, LBAT to REF	−6	±1	+6	mV	
Input Common Mode Range	0.2		4.7	V	
Output Drive Current	10	15		mA	V_{OUT} = 1.5V
Output Saturation			0.4	V	I_{OUT} = 8mA
Output Leakage Current		.01	1	μA	V_{OUT} = 10V
Oscillator frequency		1		Hz	RI = 120k, R2 = 240k,
Oscillator duty cycle		30		%	C1 = 22μF
Input Impedance, Osc off	100	250		kΩ	
Osc off threshold	0.8	1.2	1.6	V	

LOADING TABLE

Input Pin	A_{max}	A_{min}	T_{slo}	T_{max}	T	T_{min}	REF	LBAT	A_c	A_s
Load multiple	1	1	1	1	3	1	1	1	2	4

5

CIRCUIT DESCRIPTION

The two circuits basically consist of an analog computation circuit, on one die, and an alarm and LED control circuit on the other. Each circuit will work with single floating supply voltages between 2.7V and 10V, and draw less than 1mA of quiescent supply current. A minimum of external components are required, over and above those inherently associated with controlling the camera.

FUNCTIONAL BLOCK DIAGRAM - ICL8061

5

ICL8061 Computation Circuit

The computation circuit, which in many applications can stand alone, contains several functions. In terms of normal camera control description, the first is a wide range logarithmic converter. This circuit establishes a voltage of less than 50mV across the photocell (offset null is available as an option, see Note 4 above), and generates a temperature-compensated logarithm of the input current from 50pA (at room temperature) to 500μA. The scale factor can be set anywhere below approximately 40mV/octave, though 20-30mV is generally most suitable. The photocell current is compared against a reference current, I_{REF} externally generated, but most conveniently derived from the built-in (band gap) reference voltage on V_{REF}. The output voltage on BV is referred to analog common, and goes positive for increasing brightness. The equivalent schematic of this portion of the circuit is shown in Fig. 1. Q_1 is the logging

Figure 1: Logarithmic Converter Equivalent Circuit

transistor, Q_2 the reference diode. (Note Q_2 collector and base tied together.) FET input amplifier A_1 drives Q_1, and A_2 drives Q_2. Additional circuitry, not shown, compensates for A_1 and Q_1 input leakage. The difference in Q_1 and Q_2 base-emitter voltages is amplified in the instrumentation amplifier IA1 by the ratio of resistors R_1 and R_2. This provides temperature compensation, since R_1 and R_2 have very different T.C.'s.

Subsequent analog processing is done with signals proportional to the log of the corresponding photographic variables. Note that A_1 may require external frequency compensation, depending on the capacitance of the photocell and interconnecting leads.

Next is an inverting track and hold circuit, see Fig. 2. The virtual ground input point can be used to add signals, such as ASA rating and (in the case of SLR cameras), metering aperture value, to the BV to obtain an EV. The required signals can be derived via potentiometers from V_{REF}; the suggested connections are indicated in Fig. 2.

The second section of the track and hold amplifier has a FET input, which allows a very slow droop rate; the value of the external hold capacitor, C_H can be chosen to provide the necessary compromise between droop rate and response time, while frequency compensating A3.

In general, a value of ~1μF will allow settling commensurate with the speed of the other sections of the circuit while maintaining a droop rate of under one EV per minute. The hold function can be used for holding an EV during mirror-up-time in an SLR (when the photocell is blocked) or for other situations where the shutter timing and metering functions are not simultaneous. If the hold function is not needed, the control pin may be held high, or a metal mask option can be provided to eliminate the switching function.

The next function consists of two independent but identical inverting amplifiers, see Fig. 3. These can be used to subtract two separate values from EV to generate output signals powerful enough to drive small meter movements. By subtracting actual shutter speed, a calculated desired aperture signal can be derived; by subtracting actual aperture value, a desired shutter speed can be derived. Since both amplifiers can be used, both calculations can be done, so that, in match needle systems, both desired and actual aperture and shutter speed can be shown; either needle-pair can be matched. For a motor-driven aperture system, automatic aperture setting can be achieved by driving the motor until calculated and actual aperture agree (see application section below). For automatic shutter systems, the shutter control input is connected to desired shutter speed. The described connections are shown in Fig. 3, which also shows voltages derived from V^- for very slow shutter speeds. By adjusting the scale factor for the slowest shutter speeds, a simple correction for reciprocity failure can be provided. Note that the two amplifiers can be used in other ways, as well; see applications section.

Figure 2: Track-Hold and Film Speed-Meter Sensitivity Circuit

Figure 3: Calculated Aperture and Shutter Speed Circuits

The final major function is an antilog circuit which converts the required shutter speed input (either calculated or set) to a high impedance current output over more than 13 octaves. Feeding this current into a suitable capacitor produces a ramp voltage suitable for driving standard electronic shutter control comparators. The circuit as presently constructed uses the track and hold control input to disable the antilog output during track, although this inter-connect is readily removed (metal mask option) if full-time antilog (or full-time track) operation is required. The equivalent schematic for this portion of the device is shown in Fig. 4. The instrumentation amplifier IA2 does the reverse temperature coefficient correction to that of IA1, and drives the emitter of Q_3, the antilog transistor. The current output, from the collector of Q_3, has a high output impedance from analog common to the maximum voltage allowed on Q_3, (+10V). Fig. 4 also shows a typical shutter control comparator using the current from Q_3 to time the shutter closure solenoid. The operation is as follows: when the shutter release occurs, SW1 opens first, putting the circuit in hold and antilog mode. The timing current stabilizes and flows through SW2, which opens at the same time as the shutter opens. The current charges C_S down till it reaches analog common, when the (external) comparator trips the shutter closing solenoid S1. The adjustment at the input to the T_S pin corrects for scale factor errors in the antilog circuit. These errors will track very closely between IA1 and IA2, and if no use is made of intermediate signals to drive scale-sensitive devices such as analog meters, the two scale factor adjustments can be omitted, and correction made with one adjustment to the aperture, film, and shutter speed switch voltage.

The remainder of the ICL8061 circuit contains the ground, or analog common, and reference lines. The equivalent

Figure 4: Shutter Timing and Control Circuit

schematic for this section is shown in Fig. 5. This figure also shows the recommended floating battery and external bypass capacitor connections.

Figure 5: Equivalent Circuit, Analog Common and Reference Voltage

Since the various sections of the circuit are fairly independent, the individual blocks can be reconfigured readily. The analog common line should be treated with care, however, as it connects to almost all portions of the circuit.

FUNCTIONAL BLOCK DIAGRAM

ICL8062 Alarm & LED Control Circuit

The Alarm and LED control circuit compares the voltages corresponding to shutter speed, calculated and actual aperture, and reference and track-hold-control (from the ICL8061) with the maximum and minimum aperture and shutter speed voltages, together with a slow shutter speed warning limit from the external circuits, and a divided battery voltage, and drives three LEDs or similar indicators, alarms, etc. If the calculated and actual aperture values are close enough (± 1/4 f-stop, typically), fall within acceptable limits, the shutter speed is within limits, and the control input is high (corresponding to "track" in the ICL8061 circuit), the "OK" output is on (pulled low) and the others are off. If everything is the same, except that the shutter speed is between the slow warning and the lowest allowed limit, the "OK" output flashes on and off at a frequency controlled by an external RC network. In either case, if the control input goes low (the "hold" position if tied to the ICL8061), the same oscillator will flash the "OK" output. The user can time long manual exposures by counting flashes.

If the calculated and actual apertures are different, the "OK" output goes high, and depending on whether the actual aperture is above or below the calculated value, the corresponding "under" or "over" outputs will go low. Using these outputs to drive a motor results in a simple aperture controlled motor drive. A deadband, together with a small amount of hysteresis, is provided to prevent "hunting". If the actual aperture reaches either the minimum or maximum value, and still does not agree with the calculated value, both "over" and "under" outputs go low, preventing the motor from trying to overdrive the aperture system. If the actual and indicated values agree, but are at or outside the minimum or maximum value, either "over" or "under" will go low, and "OK" go high. This allows aperture setting to be done electronically on the camera body, without regard to limits of separate lenses. Circuits showing these features are given in the applications section.

If the shutter speed is either too high or too low, or the battery voltage falls below a settable multiple of the reference voltage, both "over" and "under" will go low, and "OK" will go high.

Since aperture value and shutter speed are electronically interchangeable signals, the descriptions of function above may be interchanged freely, and the low battery detect can also be used for other functions. The minimum and maximum shutter speed and aperture limit values may also be used for other functions, if desired. The outputs are capable of guaranteed drive of 10mA each, but are limited against excessive currents if short circuited.

The comparators are similar to LM139 devices in principle, and the logic shown in the block diagram is mainly RTL (or DCTL). The various comparators have built-in offsets to avoid external "tweaking" of voltage levels for system compatibility.

The oscillator schematic is shown in more detail in Fig. 6. In some applications, the "OSC IN" pin can be used as an additional control input. In this case, "OSC OUT" provides an inverted logic output, with substantial hysteresis.

Figure 6: Equivalent Schematic 8062 Oscillator

APPLICATIONS

Since all inputs to the system, other than the photocell itself, are of logarithmic values (namely ASA rating, aperture value, f-stop and speed settings, etc.), and normal controls are most desirably set up on the same basis, the tapped potentiometers to feed these values to the circuit are linear, avoiding the difficulties of logarithmic potentiometers. The same reference and scale values are used for all control inputs and outputs, allowing for ease in setting up and calibration of the system. The specifications of the circuits are such that the set-up requirements in the minimal system can be reduced to one sensitivity adjustment (to control photocell sensitivity, shutter timing capacitor value, and all system offset voltages) and one scale value adjustment to equalize the internal and external scale calibration. The most sophisticated system can be set up with one extra scale adjustment (for meter scale equalization) and one photocell voltage adjustment, if needed, and possibly an adjustment for flasher frequency.

Some typical applications connections are shown in the following figures. The selection is intended to be illustrative, rather than exhaustive, and many other combinations are possible. Also, custom modifications of the circuits can be made to facilitate certain applications. Consult the factory for details. Note that in some cases it may be necessary to use a 4.7 kΩ pull down resistor from A3 to V⁻; it may also be required to insert a resistor in series with C_H to obtain a TC of 1ms. Table I shows a typical set of voltage values corresponding to the normal photographic variables.

Table 1

Voltage	+200	180	160	140	120	100	+80	+60	+40	+20	0	−12	−14	−60	−80	mV
Shutter speed	1000	500	250	120	60	30	15	8	4	2	1	1/2	1/4	1/8	1/16	1/sec
T_V, A_V	+10	+9	+8	+7	+6	+5	+4	+3	+2	+1	0	−1	−2	−3	−4	
Aperture (f#)	32	22	16	11	8	5.6	4	2.8	2	1.4	1	(.7)				
EV	+10	+9	+8	+7	+6	+5	+4	+3	+2	+1	0	−1	−2	−3	−4	
BV (1ASA 100)	+5	+4	+3	+2	+1	0	−1	−2	−3	−4	−5	−6	−7	−8	−9	
SV	+10	+9	+8	+7	+6	+5	+4	+3	+2	+1	0					
ASA	3200	1600	800	400	200	100	50	25	12	6	3					
DIN	36	33	30	27	24	21	18	15	12	9	6					

Figure 7: Simple Automatic Aperture Camera

Camera has fixed shutter speed. The shutter pre-release switch applies power to the circuit; photocell current, together with film speed (e.g. from cartridge sensor) activates aperture vane to give correct exposure. If the light level is too low, the optional LED comes on. If a flash cube is inserted, either fixed or focus related BV is used. Film speed correction is retained. Only one set-up adjustment may be required.

Figure 8: Servo-Control Movie Camera

During interframe time, mirror-shutter directs light to photocell, and the shutter switch activates track circuit. A_3 and A_4 together with the aperture vane act as a servo loop to maintain constant light level on the photocell. During film exposure, A_3 holds value, and the vane remains still. Corrections are made for film-speed and frame-rate. The same circuit can be used for a mechanical shutter still camera, with shutter speed replacing frames/sec. The TRK/HLD pin can be tied high if the photocell is illuminated during exposure.

Figure 9: Simple Automatic Shutter Camera

Camera has fixed aperture. Pre-release S_1 applies power, S_2 establishes antilog circuit, S_3 signals shutter opening, solenoid closes shutter.

Figure 10: Electronic Shutter Servo Control Camera

Similar to Fig. 8, but has electronic shutter.

Figure 11: Automatic Clamp-Aperture S.L.R. Camera

Meter indicates calculated aperture. The "actual aperture" input tracks the lens aperture as it closes just before exposure, and when it equals the calculated value the aperture clamp solenoid is tripped. The circuit can be used with either mechanical or electronic shutters.

Figure 12: Automatic-Manual Shutter Control Camera

A_{max} is metering aperture of lens, A_S is shooting aperture. Shutter speed control has 'Auto' position & manual settings.

Figure 13: Motor-Driven Auto Aperture Camera

Motor is driven until set (or actual) aperture is equal to calculated aperture. If either maximum or minimum aperture is reached, motor stops. If satisfactory balance is achieved, 'O.K.' L.E.D. comes on. If chosen shutter speed is below preset value, L.E.D. will blink.

Figure 14: Auto-Manual Aperture Auto-Manual Shutter Camera

Motor drive is similar to Figure 13. 'Manual-Manual' position gives L.E.D. indication of 'high/correct/low' settings. In 'Auto-Auto' position, S_X connects R_X in the circuit, so that both aperture and shutter speed are controlled. R_X sets the weighting of shutter to aperture. Both shutter-preferred and aperture-preferred operations are achieved by placing the other control to automatic (automatic aperture ties in motor control system). Metering can be done at open-aperture or closed-aperture via S_4. Monitor meters can be connected to the outputs of A_4 and A_5 if desired.

Figure 15: Digital Readout Circuits

PROM or EPROM can be programmed to read any scale. Direct readout is suitable for 'EV' scale as shown. Note that converters are near -ve common mode limit.

CHIP TOPOGRAPHY, ICL8061/D

CHIP TOPOGRAPHY, ICL8062/D

PACKAGE DIMENSIONS

18 PIN PLASTIC DIP (PN)

18 LEAD PILL (FN)

1. Lead no. 1 identified by dot or notch.
2. Dimensions in inches (millimeters).

INTERSIL

ICL8001
Precision Comparator

FEATURES

- Low Input Current $\leq$ 250 nA
- Low Power Consumption 30 mW
- Large Input Voltage Range $\geq \pm 10V$
- Low Offset Voltage Drift 3 $\mu V/^\circ C$
- Output Swing Compatible with Bipolar Logic

GENERAL DESCRIPTION

The Intersil 8001 integrated circuit is a monolithic voltage comparator featuring low input currents, low power consumption, and 250 ns response time. A versatile output stage enables the designer to control the output voltage swing. The use of thin film resistors ensures excellent long term stability and the device is particularly suitable for low power space and airborne applications.

SCHEMATIC DIAGRAM

ORDERING INFORMATION

IC L 8001 C TZ

- Package:
  - TZ 10 pin, TO-5
  - JD 14 pin cerdip
- Temperature Range:
  - C – Commercial (0°C to +70°C)
  - M – Military (-55°C to +125°C)
- Device Chip Type
- Linear Circuit
- INTERSIL INCORPORATED CIRCUIT

NOTES and Additional Electrical Characteristics on Page 2.

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Input Voltage (Note 2)	±18V
Differential Input Voltage	±15V
Internal Power Dissipation (Note 1)	500 mW
Peak Output Current	15 mA
Storage Temperature Range	-65°C to +150°C
Operating Temperature Range	
(8001C)	0°C to +70°C
(8001M)	-55°C to +125°C
Lead Temperature (Soldering,60 sec)	300°C

EQUIVALENT CIRCUIT

CONNECTION DIAGRAM

NOTE: Pin 5 connected to case.

PACKAGE DIMENSIONS

TO-100

NOTES: All dimensions in inches.
Leads are gold-plated Kovar.
Package weight is 1.32 grams.

5

ELECTRICAL CHARACTERISTICS (V^{++} = 15V, V^{+} = 5V, V^{-} = −15V unless otherwise specified)

PARAMETER	CONDITIONS	8001M MIN	8001M TYP	8001M MAX	8001C MIN	8001C TYP	8001C MAX	UNITS
The following specifications apply for T_A = +25°C:								
Input Offset Voltage	$R_S \leq 10\ k\Omega$		0.5	3.0		1.0	5.0	mV
Input Offset Current			2	20		10	50	nA
Input Bias Current			40	100		50	250	nA
Input Resistance			10			10		MΩ
Power Consumption	V_{OUT} = 2.5V		30	60		30	60	mW
The following specifications apply for −55°C ≤ T_A ≤ +125°C (8001M) 0°C ≤ T_A ≤ +70°C (8001C)								
Input Offset Voltage	$R_S \leq 10\ k\Omega$			4.0			6.0	mV
Average Temperature Coefficient of Input Offset Voltage			2.0	20		3.0	30	μV/°C
Input Offset Current			7	100		15	100	nA
Average Temperature Coefficient of Input Offset Current			35			35		pA/°C
Input Bias Current				250			300	nA
Input Voltage Range		±10	±12		±10	±12		V
Common Mode Rejection Ratio		70	90		70	90		dB
Supply Voltage Rejection Ratio				300			300	μV/V
Differential Input Voltage Range				±15			±15	V
Voltage Gain		15,000	60,000		15,000	60,000		V/V
Positive Output Level Max (Note 3)	V^{+} = +15V	7.0	9.0		7.0	9.0		V
Negative Output Level	At 2 mA Sink Current		200	500		200	400	mV
Response Time (Note 4)			250			250		ns

NOTE 1: Rating applies for ambient temperatures to +70°C.
NOTE 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
NOTE 3: Positive output level can be adjusted below 9V by changing V^{+}. See circuit.
NOTE 4: The response time specified is for a 100 mV input step with 5 mV overdrive.
NOTE 5: Input bias current is independent of V^{-}.

5

CIRCUIT NOTES:

VOLTAGE OFFSET NULL CIRCUIT

OUTPUT LEVEL COMPATIBLE WITH TTL, DTL, ETC.

NOTE: As with all high gain comparators, care must be taken to avoid feedback between output and input. Where possible, hysteresis should be used to provide a small deadband.

TYPICAL PERFORMANCE CURVES

INPUT BIAS CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

INPUT BIAS CURRENT AS A FUNCTION OF V^{++} (NOTE 5)

INPUT OFFSET CURRENT AS A FUNCTION OF AMBIENT TEMPERATURE

POWER CONSUMPTION AS A FUNCTION OF AMBIENT TEMPERATURE

COMMON MODE RANGE AS A FUNCTION OF SUPPLY VOLTAGE

POSITIVE OUTPUT SWING AS A FUNCTION OF V^+

VOLTAGE TRANSFER CHARACTERISTICS

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

5

CIRCUIT AND APPLICATION NOTES

SIMPLE VOLTAGE LEVEL DETECTOR

COMPARATOR WITH HYSTERESIS

CONNECTION TO PROVIDE LOGICAL OR OF TWO COMPARATOR OUTPUTS

USE OF EXTERNAL NAND GATES TO PROVIDE OUTPUT STORAGE

WINDOW DETECTOR

A TO D CONVERTER

5

INTERSIL

LM111, LM211, LM311
Precision Voltage Comparators

FEATURES

- Differential Input Voltage Range — ±30V
- Input Common Mode Voltage Range — ±14V
- Operating Power Supplies +5V to ±18V
- Input Offset Current — 20 nA max
- Input Offset Voltage — 3 mV max
- Output Flexibility — 35V; 50 mA; T^2L Compatible
- Strobed Output & Input Offset Adjustable

GENERAL DESCRIPTION

The LM111 Series comparators are designed for precision applications where the input and output characteristics of 710 and 106 high speed comparators are not adequate for low level signal detection and high level output drive capability. They are designed to operate from supplies up to ±18V and single supplies down to +5V. The output is capable of driving TTL, RTL, DTL as well as MOS and lamps or relays. Input offset voltage balancing and TTL strobe capability are provided. Outputs can be wire OR'ed.

Switching speeds to TTL logic levels are typically 250 ns.

CONNECTION DIAGRAMS*

METAL CAN

NOTE: Pin 4 connected to case.

TOP VIEW

FLAT PACKAGE

NOTE: Pin 5 connected to bottom of package.

TOP VIEW

*Pin connections shown on schematic diagram and typical applications are for TO-5 package.

DUAL-IN-LINE

NOTE: Pin 6 connected to bottom of package.

TOP VIEW

SCHEMATIC DIAGRAM

5

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage (V_{84})		36V
Output to Negative Supply Voltage (V_{74})	LM111, LM211	50V
	LM311	40V
Ground to Negative Supply Voltage (V_{14})		30V
Differential Input Voltage		±30V
Input Voltage (Note 1)		±15V
Power Dissipation (Note 2)		500 mW
Output Short Circuit Duration		10 sec
Operating Temperature Range	LM111	-55°C to +125°C
	LM211	-25°C to +85°C
	LM311	0°C to +70°C
Storage Temperature Range		-65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

ELECTRICAL CHARACTERISTICS (Note 3)

PARAMETER	CONDITIONS	LM111/LM211 MIN	LM111/LM211 TYP	LM111/LM211 MAX	LM311 MIN	LM311 TYP	LM311 MAX	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$		0.7	3.0		2.0	7.5	mV
Input Offset Current (Note 4)	$T_A = 25°C$		4.0	10		6.0	50	nA
Input Bias Current	$T_A = 25°C$		60	100		100	250	nA
Voltage Gain	$T_A = 25°C$		200			200		V/mV
Response Time (Note 5)	$T_A = 25°C$		200			200		ns
Saturation Voltage	$T_A = 25°C$							
	$V_{IN} \leq -5$ mV, $I_{OUT} = 50$ mA		0.75	1.5				
	$V_{IN} < -10$ mV, $I_{OUT} = 50$ mA					0.75	1.5	V
Strobe on Current	$T_A = 25°C$		3.0			3.0		mA
Output Leakage Current	$T_A = 25°C$							
	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$		0.2	10				
	$V_{IN} \geq 10$ mV, $V_{OUT} = 35V$					0.2	50	nA
Input Offset Voltage (Note 4)	$R_S \leq 50k$			4.0			10	mV
Input Offset Current (Note 4)				20			70	nA
Input Bias Current				150			300	nA
Input Voltage Range			±14			±14		V
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$							
	$V_{IN} \leq -6$ mV, $I_{SINK} \leq 8$ mA		0.23	0.4				
	$V_{IN} \leq -10$ mV, $I_{SINK} \leq 8$ mA					0.23	0.4	V
Output Leakage Current (Note 6)	$V_{IN} \geq 5$ mV, $V_{OUT} = 35V$		0.1	0.5				μA
Positive Supply Current	$T_A = 25°C$		5.1	6.0		5.1	7.5	mA
Negative Supply Current	$T_A = 25°C$		4.1	5.0		4.1	5.0	mA

NOTE 1: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.

NOTE 2: The maximum junction temperature of the 111 is 150°C, that of the 211 is 110°C while that of the 311 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductor. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

NOTE 3: These specifications apply for $V_S = \pm 15V$ and over the operating temperature range, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies.

NOTE 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.

NOTE 5: The response time specified (see definitions) is for a 100 mV input step with 5 mV overdrive.

NOTE 6: This specification applies for Pin 1 -15V, Pin 7 +20V.

TYPICAL PERFORMANCE

INPUT BIAS CURRENT 111/211

INPUT OFFSET CURRENT 111/211

OFFSET ERROR 111/211

INPUT BIAS CURRENT 311

INPUT OFFSET CURRENT 311

OFFSET ERROR 311

INPUT CHARACTERISTICS

COMMON MODE LIMITS

TRANSFER FUNCTION

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

OUTPUT SATURATION VOLTAGE

5

TYPICAL PERFORMANCE (Cont)

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES

OUTPUT LIMITING CHARACTERISTICS

SUPPLY CURRENT

SUPPLY CURRENT

LEAKAGE CURRENTS 111/211

LEAKAGE CURRENTS 311

DEFINITION OF TERMS

INPUT OFFSET VOLTAGE: The voltage between the input terminals required to make the output voltage greater than or less than specified voltages.

INPUT OFFSET CURRENT: The difference between the two input currents for which the output will be driven higher than or lower than specified voltages.

INPUT BIAS CURRENT: The average of the two input currents.

INPUT VOLTAGE RANGE: The range of voltage on the input terminals (common mode) over which the offset specifications apply.

VOLTAGE GAIN: The ratio of the change in output voltage to the change in voltage between the input terminals producing it.

RESPONSE TIME: The interval between the application of an input step function and the time when the output crosses the logic threshold voltage. The input step drives the comparator from some initial, saturated input voltage to an input level just barely in excess of that required to bring the output from saturation to the logic threshold voltage. This excess is referred to as the voltage overdrive.

SATURATION VOLTAGE: The low output voltage level with the input drive equal to or greater than a specified value.

STROBE ON CURRENT: The current that must be drawn out of the strobe terminal to disable the comparator.

OUTPUT LEAKAGE CURRENT: The current into the output terminal with a specified output voltage relative to the ground pin and the input drive equal to or greater than a given value.

SUPPLY CURRENT: The current required from the positive or negative supply to operate the comparator with no output load. The power will vary with input voltage, but is specified as a maximum for the entire range of input voltage conditions.

TYPICAL APPLICATIONS

TTL COMPATIBLE OUTPUT SWING

HIGH LEVEL TTL COMPATIBLE OUTPUT SWING

MOS LOGIC COMPATIBLE OUTPUT SWING

OBTAINING ±15 VOLT OUTPUT SWING

DRIVING GROUND-REFERRED LOAD

USING CLAMP DIODES TO IMPROVE RESPONSE

*INPUT POLARITY REVERSED WHEN USING PIN 1 AS OUTPUT

OFFSET BALANCING

STROBING

INCREASING INPUT STAGE SLEW RATE*

*INCREASES TYPICAL COMMON MODE SLEW FROM 7.0V/μs TO 18V/μs

5

INTERSIL

PACKAGE DIMENSIONS

METAL CAN

FLAT PACKAGE

DUAL-IN-LINE

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE	ORDER NUMBERS
111	-55°C to +125°C	TO-99	LM111T
		DIP	LM111D
		Flat Pack	LM111F
211	-25°C to +85°C	TO-99	LM211T
		DIP	LM211D
		Flat Pack	LM211F
311	0°C to +70°C	TO-99	LM311T
		DIP	LM311D
		Flat Pack	LM311F

5

INTERSIL

LH2111, LH2311 Dual Voltage Comparator

FEATURES

- **Wide operating range - ±15V to a single +5V**
- **Low input currents - 6 nA**
- **High sensitivity - 10 μV**
- **Wide differential input range - ±30V**
- **High output drive - 50V, 50 mA**

GENERAL DESCRIPTION

The LH2111 series of dual voltage comparators consist of two LM111 type comparators in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, and reduced insertion cost.

The LH2111 is specified for operation over the −55°C to +125°C military temperature range, and the LH2311 is specified for operation from 0°C to 70°C.

AUXILIARY CIRCUITS

OFFSET BALANCING

STROBING

INCREASING INPUT STAGE CURRENT*

*Increases typical common mode slew from 7.0/μs to 18V/μs.

DRIVING GROUND-REFERRED LOAD

USING CLAMP DIODES TO IMPROVE RESPONSES

COMPARATOR AND SOLENOID DRIVER

STROBING OFF BOTH INPUT* AND OUTPUT STAGES

*Typical input current is 50 pA with inputs strobed off.

TTL INTERFACE WITH HIGH LEVEL LOGIC

*Values shown are for a 0 to 30V logic swing and a 15V threshold. May be added to control speed and reduce susceptibility to noise spikes.

5

CONNECTION DIAGRAM

ORDER NUMBER LH2111D OR LH2311D

ABSOLUTE MAXIMUM RATINGS

Total Supply Voltage 36V
Output to Negative Supply Voltage (V_{OUT} - V−) 50V
Ground to Negative Supply Voltage (GND - V−) 30V
Differential Input Voltage ..... ±30V
Input Voltage (Note 1) ..... ±15V
Power Dissipation (Note 2) ..... 500 mW
Output Short Circuit Duration ..... 10 sec
Operating Temperature Range LH2111 ..... −55°C to 125°C
LH2311 ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

ELECTRICAL CHARACTERISTICS Each side (Note 3)

PARAMETER	CONDITIONS	LIMITS LH2111	LIMITS LH2311	UNITS
Input Offset Voltage (Note 4)	$T_A = 25°C$, $R_S \leq 50k$	3.0	7.5	mV Max
Input Offset Current (Note 4)	$T_A = 25°C$	10	50	nA Max
Input Bias Current	$T_A = 25°C$	100	250	
Voltage Gain	$T_A = 25°C$	200	200	V/mV Typ
Response Time (Note 5)	$T_A = 25°C$	200	200	ns Typ
Saturation Voltage	$V_{IN} \leq -5mV$, $I_{OUT} = 50mA$ $T_A = 25°C$	1.5	1.5	V Max
Strobe On Current	$T_A = 25°C$	3.0	3.0	mA Typ
Output Leakage Current	$V_{IN} \geq 5mV$, $V_{OUT} = 35V$ $T_A = 25°C$	10	50	nA Max
Input Offset Voltage (Note 4)	$R_S \leq 50k$	4.0	10	mV Max
Input Offset Current (Note 4)		20	70	nA Max
Input Bias Current		150	300	
Input Voltage Range		±14	±14	V Typ
Saturation Voltage	$V^+ \geq 4.5V$, $V^- = 0$ $V_{IN} \leq -5mV$, $I_{SINK} \leq 8$ mA	0.4	0.4	V Max
Positive Supply Current	$T_A = 25°C$	6.0	7.5	mA Max
Negative Supply Current	$T_A = 25°C$	5.0	5.0	

Note: This rating applies for ±15V supplies. The positive input voltage limit is 30V above the negative supply. The negative input voltage limit is equal to the negative supply voltage or 30V below the positive supply, whichever is less.
Note 2: The maximum junction temperature is 150°C. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.
Note 3: These specifications apply for $V_S = \pm15V$ and $-55°C \leq T_A \leq 125°C$ for the LH2111, and $0°C \leq T_A \leq 70°C$ for the LH2311, unless otherwise stated. The offset voltage, offset current and bias current specifications apply for any supply voltage from a single 5V supply up to ±15V supplies. For the LH2311, $V_{IN} = \pm10V$.
Note 4: The offset voltages and offset currents given are the maximum values required to drive the output within a volt of either supply with a 1 mA load. Thus, these parameters define an error band and take into account the worst case effects of voltage gain and input impedance.
Note 5: The response time specified is for a 100 mV input step with 5 mV overdrive.

INTERSIL

LM139/LM239/LM339/ LM139A/LM239A/LM339A/ LM2901/LM3302 Voltage Comparators

FEATURES

- **Wide single supply voltage range or dual supplies**
  LM139 series, 2 V_{DC} to 36 V_{DC} or
  LM139A series, LM2901 ±1 V_{DC} to ±18 V_{DC}
  LM3302 2 V_{DC} to 28 V_{DC} or ±1 V_{DC} to ±14 V_{DC}
- **Very low supply current drain (0.8 mA)—independent of supply voltage (2 mW/comparator at +5 V_{DC})**
- **Low input biasing current 25 nA**
- **Low input offset current ±5 nA**
  and offset voltage ±3 mV
- **Input common-mode voltage range includes gnd**
- **Differential input voltage range equal to the power supply voltage**
- **Low output saturation voltage 250 mV at 4 mA**
- **Output voltage compatible with TTL, DTL, ECL, MOS and CMOS logic systems**

GENERAL DESCRIPTION

The LM139 series consists of four independent precision voltage comparators with an offset voltage specification as low as 2 mV max for all four comparators. These were designed specifically to operate from a single power supply over a wide range of voltages. Operation from split power supplies is also possible and the low power supply current drain is independent of the magnitude of the power supply voltage. These comparators also have a unique characteristic in that the input common-mode voltage range includes ground, even though operated from a single power supply voltage.

Application areas include limit comparators, simple analog to digital converters; pulse, squarewave and time delay generators; wide range VCO; MOS clock timers; multivibrators and high voltage digital logic gates. The LM139 series was designed to directly interface with TTL and CMOS. When operated from both plus and minus power supplies, they will directly interface with MOS logic —where the low power drain of the LM339 is a distinct advantage over standard comparators.

SCHEMATIC AND CONNECTION DIAGRAMS

DUAL-IN-LINE AND FLAT PACKAGE

ORDERING INFORMATION

Order Number: LM139D, LM139AD, LM239D or LM239AD

Order Number: LM139J, LM139AJ, LM239J, LM239AJ, LM339J, LM339AJ, LM2901J or LM3302J

Order Number: LM139F, LM139AF, LM239F or LM239AF

Order Number: LM339N, LM339AN, LM2901N or LM3302N

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ABSOLUTE MAXIMUM RATINGS

	LM139/LM239/LM339 LM139A/LM239A/LM339A LM2901	LM3302
Supply Voltage, V+	36 V_{DC} or ±18 V_{DC}	28 V_{DC} or ±14 V_{DC}
Differential Input Voltage	36 V_{DC}	28 V_{DC}
Input Voltage	−0.3 V_{DC} to +36 V_{DC}	−0.3 V_{DC} to +28 V_{DC}
Power Dissipation (Note 1)		
Molded DIP	570 mW	570 mW
Cavity DIP	900 mW	
Flat Pack	800 mW	
Output Short-Circuit to GND, (Note 2)	Continuous	Continuous
Input Current ($V_{IN} < -0.3$ V_{DC}), (Note 3)	50 mA	50 mA
Operating Temperature Range		−40°C to +85°C
LM339A	0°C to +70°C	
LM239A	−25°C to +85°C	
LM139A	−55°C to +125°C	
Storage Temperature Range	−65°C to +150°C	−65°C to +150°C
Lead Temperature (Soldering, 10 seconds)	300°C	300°C

NOTE:

Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

ELECTRICAL CHARACTERISTICS ($V^+ = 5$ V_{DC}, Note 4)

PARAMETER	CONDITIONS	LM139A			LM239A, LM339A			LM139			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	$T_A = 25°C$, (Note 9)		±1.0	±2.0		±1.0	±2.0		±2.0	±5.0	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, $T_A = 25°C$, (Note 5)		25	100		25	250		25	100	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25°C$		±3.0	±25		±5.0	±50		±3.0	±25	nA_{DC}
Input Common-Mode Voltage Range	$T_A = 25°C$, (Note 6)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Supply Current	$R_L = \infty$ on all Comparators, $T_A = 25°C$ $R_L = \infty$, $V^+ = 30V$, $T_A = 25°C$		 0.8	 2.0		 0.8	 2.0		 0.8	 2.0	mA_{DC} mA_{DC}
Voltage Gain	$R_L \geq 15$ k Ω, $V^+ = 15$ V_{DC} (To Support Large V_O Swing), $T_A = 25°C$	50	200		50	200			200		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, $V_{REF} = 1.4$ V_{DC}, $V_{RL} = 5$ V_{DC}, $R_L = 5.1$ k Ω, $T_A = 25°C$		300			300			300		ns
Response Time	$V_{RL} = 5$ V_{DC}, $R_L = 5.1$ k Ω, $T_A = 25°C$, (Note 7)		1.3			1.3			1.3		μs
Output Sink Current	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $V_O \leq 1.5$ V_{DC}, $T_A = 25°C$	6.0	16		6.0	16		6.0	16		mA_{DC}
Saturation Voltage	$V_{IN(-)} \geq 1$ V_{DC}, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$ mA, $T_A = 25°C$		250	400		250	400		250	400	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq 1$ V_{DC}, $V_{IN(-)} = 0$, $V_O = 5$ V_{DC}, $T_A = 25°C$		0.1			0.1			0.1		nA_{DC}
Input Offset Voltage	(Note 9)			4.0			4.0			9.0	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±100			±150			±100	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			300			400			300	nA_{DC}
Input Common-Mode Voltage Range		0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	V_{DC}
Saturation Voltage	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4$ mA			700			700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq 1V_{DC}$, $V_{IN(-)} = 0$, $V_O = 30$ V_{DC}			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep all V_{IN}'s ≥ 0 V_{DC} (or V^-, if used), (Note 8)			V^+			V^+			36	V_{DC}

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ELECTRICAL CHARACTERISTICS (CON'T) ($V^+ = 5\ V_{DC}$, Note 4)

PARAMETER	CONDITIONS	LM239, LM339			LM2901			LM3302			UNITS
		MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Input Offset Voltage	$T_A = 25°C$, (Note 9)		±2.0	±5.0		±2.0	±7.0		±3	±20	mV_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range, $T_A = 25°C$, (Note 5)		25	250		25	250		25	500	nA_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$, $T_A = 25°C$		±5.0	±50		±5	±50		±3	±100	nA_{DC}
Input Common-Mode Voltage Range	$T_A = 25°C$, (Note 6)	0		$V^+-1.5$	0		$V^+-1.5$	0		$V^+-1.5$	V_{DC}
Supply Current	$R_L = \infty$ on all Comparators, $T_A = 25°C$ $R_L = \infty$, $V^+ = 30V$, $T_A = 25°C$		0.8	2.0		0.8 1	1.0 2.5		0.8	2	mA_{DC} mA_{DC}
Voltage Gain	$R_L \geq 15\ k\Omega$, $V^+ = 15\ V_{DC}$ (To Support Large V_O Swing), $T_A = 25°C$		200		25	100		2	30		V/mV
Large Signal Response Time	V_{IN} = TTL Logic Swing, V_{REF} = 1.4 V_{DC}, $V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$		300			300			300		ns
Response Time	$V_{RL} = 5\ V_{DC}$, $R_L = 5.1\ k\Omega$, $T_A = 25°C$, (Note 7)		1.3			1.3			1.3		μs
Output Sink Current	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $V_O \leq 1.5\ V_{DC}$, $T_A = 25°C$	6.0	16		6.0	16		2.0	16		mA_{DC}
Saturation Voltage	$V_{IN(-)} \geq 1\ V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ mA$, $T_A = 25°C$		250	400			400		250	500	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq 1\ V_{DC}$, $V_{IN(-)} = 0$, $V_O = 5\ V_{DC}$, $T_A = 25°C$		0.1			0.1			0.1		nA_{DC}
Input Offset Voltage	(Note 9)			9.0		9	15			40	mV_{DC}
Input Offset Current	$I_{IN(+)} - I_{IN(-)}$			±150		50	200			300	nA_{DC}
Input Bias Current	$I_{IN(+)}$ or $I_{IN(-)}$ with Output in Linear Range			400		200	500			1000	nA_{DC}
Input Common-Mode Voltage Range		0		$V^+-2.0$	0		$V^+-2.0$	0		$V^+-2.0$	V_{DC}
Saturation Voltage	$V_{IN(-)} \geq 1V_{DC}$, $V_{IN(+)} = 0$, $I_{SINK} \leq 4\ mA$			700		400	700			700	mV_{DC}
Output Leakage Current	$V_{IN(+)} \geq 1V_{DC}$, $V_{IN(-)} = 0$, $V_O = 30\ V_{DC}$			1.0			1.0			1.0	μA_{DC}
Differential Input Voltage	Keep all V_{IN}'s $\geq 0\ V_{DC}$ (or V^-, if used), (Note 8)			36	0		V^+			V_{CC}	V_{DC}

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Note:

1. For operating at high temperatures, the LM339/LM339A, LM2901, LM3302 must be derated based on a 125°C maximum junction temperature and a thermal resistance of 175°C/W which applies for the device soldered in a printed circuit board, operating in a still air ambient. The LM239 and LM139 must be derated based on a 150°C maximum junction temperature. The low bias dissipation and the "ON-OFF" characteristic of the outputs keeps the chip dissipation very small ($P_D \leq 100$ mW), provided the output transistors are allowed to saturate.
2. Short circuits from the output to V^+ can cause excessive heating and eventual destruction. The maximum output current is approximately 20 mA independent of the magnitude of V^+.
3. This input current will only exist when the voltage at any of the input leads is driven negative. It is due to the collector-base junction of the input PNP transistors becoming forward biased and thereby acting as input diode clamps. In addition to this diode action, there is also lateral NPN parasitic transistor action on the IC chip. This transistor action can cause the output voltages of the comparators to go to the V^+ voltage level (or to ground for a large overdrive) for the time duration that an input is driven negative. This is not destructive and normal output states will re-establish when the input voltage, which was negative, again returns to a value greater than —0.3 V_{DC}.
4. These specifications apply for $V^+ = 5\ V_{DC}$ and $-55°C \leq T_A \leq +125°C$, unless otherwise stated. With the LM239/LM239A, all temperature specifications are limited to $-25°C \leq T_A \leq +85°C$, the LM339/LM339A temperature specifications are limited to $0°C \leq T_A \leq +70°C$, and the LM2901, LM3302 temperature range is $-40°C \leq T_A \leq +85°C$.
5. The direction of the input current is out of the IC due to the PNP input stage. This current is essentially constant, independent of the state of the output so no loading change exists on the reference or input lines.
6. The input common-mode voltage or either input signal voltage should not be allowed to go negative by more than 0.3V. The upper end of the common-mode voltage range is V^+ —1.5V, but either or both inputs can go to +30 V_{DC} without damage.
7. The response time specified is for a 100 mV input step with 5 mV overdrive signals 300 ns can be obtained, see typical performance characteristics section.
8. Positive excursions of input voltage may exceed the power supply level. As long as the other voltage remains within the common-mode range, the comparator will provide a proper output state. The low input voltage state must not be less than —0.3 V_{DC} (or 0.3 V_{DC} below the magnitude of the negative power supply, if used).
9. At output switch point, $V_O = 1.4\ V_{DC}$, $R_S = 0\Omega$ with V^+ from 5 V_{DC}; and over the full input common-mode range (0 V_{DC} to V^+ —1.5 V_{DC}).
10. For input signals that exceed V_{CC}, only the overdriven comparator is affected. With a 5V supply V_{IN} should be limited to 25V max, and a limiting resistor should be used on all inputs that might exceed the positive supply.

TYPICAL PERFORMANCE CHARACTERISTICS LM139/LM239/LM339, LM139A/LM239A/LM339A, LM3302

SUPPLY CURRENT

INPUT CURRENT

OUTPUT SATURATION VOLTAGE

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES—NEGATIVE TRANSITION

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES—POSITIVE TRANSITION

TYPICAL PERFORMANCE CHARACTERISTICS LM2901

SUPPLY CURRENT

INPUT CURRENT

OUTPUT SATURATION VOLTAGE

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES—NEGATIVE TRANSITION

RESPONSE TIME FOR VARIOUS INPUT OVERDRIVES—POSITIVE TRANSITION

APPLICATION HINTS

The LM139 series are high gain, wide bandwidth devices which, like most comparators, can easily oscillate if the output lead is inadvertently allowed to capacitively couple to the inputs via stray capacitance. This shows up only during the output voltage transition intervals as the comparator changes states. Power supply bypassing is not required to solve this problem. Standard PC board layout is helpful as it reduces stray input-output coupling. Reducing the input resistors to < 10 kΩ reduces the feedback signal levels and finally, adding even a small amount (1 to 10 mV) of positive feedback (hysteresis) causes such a rapid transition that oscillations due to stray feedback are not possible. Simply socketing the IC and attaching resistors to the pins will cause input-output oscillations during the small transition intervals unless hysteresis is used. If the input signal is a pulse waveform, with relatively fast rise and fall times, hysteresis is not required.

All pins of any unused comparators should be grounded.

The bias network of the LM139 series establishes a drain current which is independent of the magnitude of the power supply voltage over the range of from 2 V_{DC} to 30 V_{DC}.

It is usually unnecessary to use a bypass capacitor across the power supply line.

The differential input voltage may be larger than V^+ without damaging the device. Protection should be provided to prevent the input voltages from going negative more than −0.3 V_{DC} (at 25°C). An input clamp diode can be used as shown in the applications section.

The output of the LM139 series is the uncommitted collector of a grounded-emitter NPN output transistor. Many collectors can be tied together to provide an output OR'ing function. An output pull-up resistor can be connected to any available power supply voltage within the permitted supply voltage range and there is no restriction on this voltage due to the magnitude of the voltage which is applied to the V^+ terminal of the LM139A package. The output can also be used as a simple SPST switch to ground (when a pull-up resistor is not used). The amount of current which the output device can sink is limited by the drive available (which is independent of V^+) and the β of this device. When the maximum current limit is reached (approximately 16 mA), the output transistor will come out of saturation and the output voltage will rise very rapidly. The output saturation voltage is limited by the approximately 60 Ω r_{sat} of the output transistor. The low offset voltage of the output transistor (1 mV) allows the output to clamp essentially to ground level for small load currents.

TYPICAL APPLICATIONS (V^+ = 15 V_{DC})

BASIC COMPARATOR

DRIVING CMOS

DRIVING TTL

AND GATE

OR GATE

TYPICAL APPLICATIONS (CON'T) ($V^+ = 15\ V_{DC}$)

ONE-SHOT MULTIVIBRATOR

BI-STABLE MULTIVIBRATOR

ONE-SHOT MULTIVIBRATOR WITH INPUT LOCK OUT

LARGE FAN-IN AND GATE

TIME DELAY GENERATOR

ORING THE OUTPUTS

TYPICAL APPLICATIONS ($V^+ = 5.0\ V_{DC}$)

SQUAREWAVE OSCILLATOR

PULSE GENERATOR

NON-INVERTING COMPARATOR WITH HYSTERESIS

INVERTING COMPARATOR WITH HYSTERESIS

COMPARING INPUT VOLTAGES OF OPPOSITE POLARITY

BASIC COMPARATOR

*OR LOGIC GATE WITHOUT PULL-UP RESISTOR

OUTPUT STROBING

TWO-DECADE HIGH-FREQUENCY VCO

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TYPICAL APPLICATIONS (CON'T) ($V^+ = 5\ V_{DC}$)

LIMIT COMPARATOR

CRYSTAL CONTROLLED OSCILLATOR

LOW FREQUENCY OP AMP

LOW FREQUENCY OP AMP
(V_O = OV FOR V_{IN} = OV)

TRANSDUCER AMPLIFIER

LOW FREQUENCY OP AMP
WITH OFFSET ADJUST

ZERO CROSSING DETECTOR
(SINGLE POWER SUPPLY)

SPLIT-SUPPLY APPLICATIONS ($V^+ = +15\ V_{DC}$ and $V^- = -15\ V_{DC}$)

MOS CLOCK DRIVER

ZERO CROSSING DETECTOR

COMPARATOR WITH A NEGATIVE REFERENCE

INTERSIL

LM102, LM202, LM302, LM110, LM210, LM310

High Performance Voltage Followers

FEATURES

- Low Input Current – 7 to 30 nA Max
- High Slew Rate – 10 to 30 V/μs
- Wide Bandwidth – 20 MHz (LM110/LM310)
- Internal Frequency Compensation
- Interchangeable with 741 in Follower Applications

GENERAL DESCRIPTION

The LM102/LM302 and LM110/LM310 are monolithic high performance voltage followers. In buffer applications they offer substantial advantages compared with general purpose operational amplifiers: input current, bandwidth, and slew rate are all significantly improved. Applications include high speed sample and hold circuits, instrumentation amplifiers, active filters, as well as general purpose buffers.

For new designs the LM110/LM310 is recommended.

CONNECTION DIAGRAMS

NOTE: Pin 4 connected to case.

TOP VIEW

NOTE: Pin 5 connected to bottom of package.

TOP VIEW

NOTE: Pin 6 connected to bottom of package.

TOP VIEW

EQUIVALENT CIRCUIT

OFFSET BALANCING

INCREASING NEGATIVE SWING UNDER LOAD

*May be added to reduce internal dissipation.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Input Voltage (Note 2)	±15V
Output Short Circuit Duration (Note 3)	Indefinite

Operating Temperature Range:	102, 110	−55°C to +125°C
	202, 210	−25°C to +85°C
	302, 310	0°C to +70°C
Storage Temperature Range		−65°C to +150°C
Lead Temperature (Soldering, 10 sec)		300°C

ELECTRICAL CHARACTERISTICS 102/202/302 (Note 4)

PARAMETER	CONDITIONS	LM102			LM202			LM302			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Offset Voltage			2	5		3	10		5	15	mV
Average Temperature Coefficient of Offset Voltage			6			15			20		μV/°C
Input Current			3	10		7	15		10	30	nA
Input Resistance		10^{10}	10^{12}		10^{10}	10^{12}		10^{9}	10^{12}		Ω
Voltage Gain	$R_L \geq 10$ kΩ	0.999	0.9996		0.999	0.9995	1.000	0.9985	0.9995	1.000	
Output Resistance			0.8	2.5		0.8	2.5		0.8	2.5	Ω
Output Voltage Swing (Note 6)	$R_L \geq 8$ kΩ	±10	±13		±10			±10			V
Supply Current			3.5	5.5		3.5	5.5		3.5	5.5	mA
Positive Supply Rejection		60			60			60			dB
Negative Supply Rejection		70			70			70			dB
Input Capacitance				3.0		3.0			3.0		pF
Offset Voltage	$T_{MIN} \leq T_A \leq T_{MAX}$			7.5			15			20	mV
Input Current	$T_A = T_{MAX}$		3	10		1.5	5.0		3.0	15	nA
	$T_A = T_{MIN}$		30	100		30	50		20	50	nA
Voltage Gain	$-55°C \leq T_A \leq 125°C$, $R_L \geq 10$ kΩ	0.999									
Supply Current	$T_A = 125°C$		2.6	4.0							mA

ELECTRICAL CHARACTERISTICS 110/210/310 (Note 5)

PARAMETER	CONDITIONS	LM110			LM210			LM310			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Input Offset Voltage	$T_A = 25°C$		1.5	4.0		1.5	4.0		2.5	7.5	mV
Input Bias Current	$T_A = 25°C$		1.0	3.0		1.0	3.0		2.0	7.0	nA
Input Resistance	$T_A = 25°C$	10^{10}	10^{12}		10^{10}	10^{12}		10^{10}	10^{12}		Ω
Input Capacitance			1.5			1.5			1.5		pF
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L = 8$ kΩ	0.999	0.9999		0.999	0.9999		0.999	0.9999		V/V
Output Resistance	$T_A = 25°C$		0.75	2.5		0.75	2.5		0.75	2.5	Ω
Supply Current	$T_A = 25°C$		3.9	5.5		3.9	5.5		3.9	5.5	mA
Input Offset Voltage				6.0			6.0			10	mV
Offset Voltage Temperature Drift			10			10			10		μV/°C
Input Bias Current				10			10			10	nA
Large Signal Voltage Gain	$V_S = \pm15V$, $V_{OUT} = \pm10V$, $R_L = 10$ kΩ	0.999			0.999			0.999			V/V
Output Voltage Swing (Note 6)	$V_S = \pm15V$, $R_L = 10$ kΩ	±10			±10			±10			V
Supply Current	$T_A = T_{MAX}$		2.0	4.0		2.0	4.0				mA
Supply Voltage Rejection Ratio	$\pm5V \leq V_S \leq \pm18V$	70	80		70	80		70	80		dB

NOTE 1: The maximum junction temperature of the 102 and 110 is 150°C, that of the 202 and 210 is 100°C, while that of the 302 and 310 is 85°C. For operating at elevated temperatures, devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient, or 45°C/W, junction to case. For the flat package, the derating is based on a thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten, 0.03-inch-wide, 2-ounce copper conductors. The thermal resistance of the dual-in-line package is 100°C/W, junction to ambient.

NOTE 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.

NOTE 3: Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 70°C. It is necessary to insert a resistor greater than 2 kΩ in series with the input when the amplifier is driven from low impedance sources to prevent damage when the output is shorted.

NOTE 4: These specifications apply for $T_A = 25°C$, $V_S = \pm15V$ and $C_L < 100$ pF unless otherwise noted.

NOTE 5: These specifications apply for $\pm5V \leq V_S \leq \pm18V$ and $-55°C < T_A \leq 125°C$, unless otherwise specified. With the 210, however, all temperature specifications are limited to $-25°C \leq T_A \leq 85°C$, while for the 310 the limits are $0°C \leq T_A < 70°C$.

NOTE 6: Increased output swing under load can be obtained by connecting an external resistor between the booster and V^- terminals. See curve.

TYPICAL PERFORMANCE

NORMALIZED INPUT CURRENT

OUTPUT NOISE VOLTAGE

LARGE SIGNAL PULSE RESPONSE

VOLTAGE GAIN

VOLTAGE GAIN*

VOLTAGE GAIN

OUTPUT RESISTANCE

SYMMETRICAL OUTPUT SWING

POSITIVE OUTPUT SWING

LARGE SIGNAL FREQUENCY RESPONSE

POWER SUPPLY REJECTION

SUPPLY CURRENT

*Note that optimum stability is obtained for a source resistance of 10 kΩ. For source resistances lower than 10 kΩ, it is advisable to put additional resistance in series with the input to ensure adequate stability margin.

5

APPLICATIONS

SAMPLE AND HOLD

INSTRUMENTATION AMPLIFIER

DEFINITION OF TERMS

OFFSET VOLTAGE: The voltage at the output of the amplifier with the input at zero.

OFFSET VOLTAGE TEMPERATURE DRIFT: The average drift rate of offset voltage for a thermal variation from room temperature to the indicated temperature extreme.

INPUT CURRENT: The current into the input of the amplifier with the input at zero.

INPUT RESISTANCE: The ratio of the rated output voltage swing to the change in input current required to drive the output from zero to this voltage.

LARGE SIGNAL VOLTAGE GAIN: The ratio of the output voltage swing to the change in input voltage required to drive the output from zero to this voltage.

OUTPUT RESISTANCE: The ratio of the change in output voltage to the change in output current with constant input voltage.

OUTPUT VOLTAGE SWING: The peak output voltage swing, referred to zero, that can be obtained without the large-signal voltage gain falling below the minimum specified value.

SUPPLY CURRENT: The current required from the power supply to operate the amplifier, with no load, anywhere within its linear range.

POWER SUPPLY REJECTION: The ratio of the change in input offset voltage to the change in power supply voltage producing it.

SLEW RATE: The internally-limited rate of change in output voltage with a large-amplitude step function applied to the input.

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ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE	ORDER NUMBER
102	−55°C to +125°C	TO-99 Flat Pack	LM102T LM102F
202	−25°C to +85°C	TO-99	LM202T
302	0°C to +70°C	TO-99	LM302T

PART NUMBER	TEMPERATURE RANGE	PACKAGE TYPE	ORDER NUMBER
110	−55°C to +125°C	TO-99 DIP Flat Pack	LM110T LM110D LM110F
210	−25°C to +85°C	TO-99 DIP	LM210T LM210D
310	0°C to +70°C	TO-99 DIP	LM310T LM310D

INTERSIL

LH2110, LH2310 Dual Voltage Follower

FEATURES

- Low input current - 1 nA
- High input resistance - 10 MΩ
- High slew rate - 30V/μs
- Wide bandwidth - 20 MHz
- Wide operating supply range - ±5V to ±18V
- Output short circuit protected.

GENERAL DESCRIPTION

The LH2110 series of dual voltage followers consist of two LM110 type followers in a single hermetic package. Featuring all the same performance characteristics of the single, these duals offer in addition closer thermal tracking, lower weight, and reduced insertion cost.

The LH2110 is specified for operation over the −55°C to +125°C military temperature range, and the LH2310 is specified for operation from 0°C to +70°C.

CONNECTION DIAGRAM

ORDER NUMBER LH2110D or LH2310D

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AUXILIARY CIRCUITS

INCREASING NEGATIVE SWING UNDER LOAD

*May be added to reduce internal dissipation

OFFSET BALANCING CIRCUIT

ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... ±18V
Power Dissipation (Note 1) ..... 500 mW
Input Voltage (Note 2) ..... ±15V
Output Short Circuit Duration (Note 3) ..... Continuous
Operating Temperature Range LH2110 ..... −55°C to 125°C
LH2310 ..... 0°C to 70°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

ELECTRICAL CHARACTERISTICS Each side (Note 4)

PARAMETER	CONDITIONS	LIMITS LH2110	LIMITS LH2310	UNITS
Input Offset Voltage	$T_A = 25°C$	4.0	7.5	mV Max
Input Bias Current	$T_A = 25°C$	3.0	7.0	nA Max
Input Resistance	$T_A = 25°C$	10M	10M	Ω Min
Input Capacitance		1.5	1.5	pF Typ
Large Signal Voltage Gain	$T_A = 25°C$, $V_S = ±15V$ $V_{OUT} = ±10V$, $R_L = 8\ k\Omega$	.999	.999	V/V Min
Output Resistance	$T_A = 25°C$	2.5	2.5	Ω Max
Supply Current (Each Amplifier)	$T_A = 25°C$	5.5	5.5	mA Max
Input Offset Voltage		6.0	10	mV Max
Offset Voltage	$-55°C \le T_A \le 85°C$	6	10	μV/°C Typ
Temperature Drift	$T_A = 125°C$	12	—	
Input Bias Current		10	10	nA Max
Large Signal Voltage Gain	$V_S = ±15V$, $V_{OUT} = ±10V$ $R_L = 10\ k\Omega$	.999	.999	V/V Min
Output Voltage Swing (Note 5)	$V_S = ±15V$, R_L 10 kΩ	±10	±10	V Min
Supply Current (Each Amplifier)	$T_A = 125°C$	4.0	—	mA Max
Supply Voltage Rejection Ratio	$±5V \le V_S \le ±18V$	70	70	dB Min

Note 1: The maximum junction temperature of the LH2110 is 150°C, while that of the LH2310 is 85°C. The thermal resistance of the package is 100°C/W, junction to ambient.
Note 2: For supply voltages less than ±15V, the absolute maximum input voltage is equal to the supply voltage.
Note 3: Continuous short circuit is allowed for case temperatures to 125°C and ambient temperatures to 70°C. It is necessary to insert a resistor greater than 2 KΩ in series with the inut when the amplifier is driven from low impedance sources to prevent damage when the output is shorted.
Note 4: These specifications apply for $±5V \le V_S \le ±18V$ and $-55°C \le T_A \le 125°C$, unless otherwise specified, and for the LH2310, all temperature specifications are limited to $0°C \le T_A \le 70°C$.
Note 5: Increased output swing under load can be obtained by connecting an external resistor between the booster and V− terminals.

INTERSIL

ICL8013
Four Quadrant Analog Multiplier

FEATURES

- ±0.5% Accuracy
- Internal Op-Amp for Level Shift, Division and Square Root Functions
- Uses Film Resistors for Minimum External Components
- Full ±10 Volt Input/Output Voltage Range
- Wide Bandwidth – 1 MHz
- Operates with Standard ±15 Volt Supplies

GENERAL DESCRIPTION

The 8013 is a four quadrant analog multiplier whose output is proportional to the algebraic product of two input signals. Feedback around an internal op-amp provides level shifting and can be used to generate division and square root functions. A simple arrangement of potentiometers may be used to trim gain accuracy, offset voltage and feedthrough performance. The high accuracy, wide bandwidth, and increased versatility of the 8013 makes it ideal for all multiplier applications in control and instrumentation systems.

CONNECTION DIAGRAM

TO-100 PACKAGE

APPLICATIONS

- Multiplication, Division, Squaring, Square Roots
- RMS Measurements
- Frequency Doubler
- Balanced Modulator and Demodulator
- Electronic Gain Control
- Function Generator and Linearizing Circuits
- Process Control Systems

SCHEMATIC DIAGRAM

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	±18V
Power Dissipation (Note 1)	500 mW
Input Voltages (X, Y, Z, X_o, Y_o, Z_o)	±V Supply
Lead Temperature (60 sec)	300°C
Storage Temperature Range	-65°C to +150°C

NOTE 1: Derate at 6.8 mW/°C for operation at ambient temperature above 75°C.

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ELECTRICAL CHARACTERISTICS

(Unless otherwise specified $T_A = 25°C$, $V_S = \pm15V$, Gain and Offset Potentiometers Externally Trimmed)

PARAMETER	CONDITIONS	8013A			8013B			8013C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	
Multiplier Function			$\frac{XY}{10}$			$\frac{XY}{10}$			$\frac{XY}{10}$		
Multiplication Error	$-10 < X < 10$ $-10 < Y < 10$			.5			1.0			2.0	% Full Scale
Divider Function			$\frac{10Z}{X}$			$\frac{10Z}{X}$			$\frac{10Z}{X}$		
Division Error	X = −10		0.3			0.3			0.3		% Full Scale
	X = −1		1.5			1.5			1.5		% Full Scale
Feedthrough	X = 0 Y = $20V_{pp}$ f = 50 Hz			50			100			200	mV_{pp}
	Y = 0 X = $20V_{pp}$ f = 50 Hz			50			100			150	mV_{pp}
Nonlinearity											
X Input	X = $20V_{pp}$ Y = ±10 Vdc		±0.5			±0.5			±0.8		%
Y Input	Y = 20 V_{pp} X = ±10 Vdc		±0.2			±0.2			±0.3		%
Frequency Response											
Small Signal Bandwidth (−3 dB)			1.0			1.0			1.0		MHz
Full Power Bandwidth			750			750			750		kHz
Slew Rate			45			45			45		V/μs
1% Amplitude Error			75			75			75		kHz
1% Vector Error (0.5° Phase Shift)			5			5			5		kHz
Settling Time (to ±2% of Final Value)	E_{IN} = ±10V		1			1			1		μs
Overload Recovery (to ±2% of Final Value)			1			1			1		μs
Output Noise	5 Hz to 10 kHz		0.6			0.6			0.6		mVrms
	5 Hz to 5 MHz		3			3			3		mVrms
Input Resistance											
X Input			10			10			10		MΩ
Y Input			6			6			6		MΩ
Z Input			36			36			36		kΩ
Input Bias Current											
X or Y Input			2	5			7.5			10	μA
Z Input			25			25			25		μA
Power Supply Variation											
Multiplication Error			0.2			0.2			0.2		%/%
Output Offset				50			75			100	mV/V
Scale Factor			0.1			0.1			0.1		%/%
Quiescent Current			3.5	6.0		3.5	6.0		3.5	6.0	mA

THE FOLLOWING SPECIFICATIONS APPLY OVER THE OPERATING TEMPERATURE RANGES

Multiplication Error	$-10 < X < 10$, $-10 < Y < 10$		1.5			2			3		% Full Scale
Average Temperature Coefficient of											
Accuracy			0.06			0.06			0.06		%/°C
Output Offset			0.2			0.2			0.2		mV/°C
Scale Factor			0.04			0.04			0.04		%/°C
Input Bias Current											
X or Y Input				10			10			20	μA
Z Input				70			70			100	μA
Input Voltage (X, Y, or Z)				±10			±10			±10	V
Output Voltage Swing	$R_L \geq 2k$ $C_L \leq 1000$ pF	±10			±10			±10			V

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APPLICATIONS INFORMATION

MULTIPLIER Trimming Procedure

1. Set X_{IN} = Y_{IN} = 0V and adjust Z_o for zero Output.
2. Apply a low frequency sweep ($f_o \leq$ 100 Hz sine or triangle) of = ±10V to Y_{IN} with X_{IN} = 0V and adjust X_o for minimum Output.
3. Apply the sweep signal of Step 2 to X_{IN} with Y_{IN} = 0V and adjust Y_o for minimum Output.
4. Readjust Z_o as in Step 1, if necessary.
5. With X_{IN} = 10.0V dc and the sweep signal of Step 2 applied to Y_{IN}, adjust the Gain potentiometer for Output = Y_{IN}. This is easily accomplished with a differential scope plug-in (A + B) by inverting one signal and adjusting Gain control for (Output – Y_{IN}) = Zero.

DIVIDER Trimming Procedure

1. Set trimming potentiometers at mid-scale by adjusting voltage on pins 7, 9 and 10 (X_o, Y_o, Z_o) for zero volts.
2. With Z_{IN} = 0V, trim Z_o to hold the Output constant, as X_{IN} is varied from –10V through –1V.
3. With Z_{IN} = 0V and X_{IN} = –10.0V adjust Y_o for zero Output voltage.
4. With Z_{IN} = X_{IN} (and/or Z_{IN} = $-X_{IN}$) adjust X_o for minimum worst-case variation of Output as X_{IN} is varied from –10V to –1V.
5. Repeat Steps 2 and 3 if Step 4 required a large initial adjustment.
6. With Z_{IN} = X_{IN} (and/or Z_{IN} = $-X_{IN}$) adjust the gain control until the output is the closest average around +10.0V (–10V for Z_{IN} = $-X_{IN}$) as X_{IN} is varied from –10V to –3V.

SQUARE ROOT Trimming Procedure

1. Connect the 8013 in the *Divider* configuration.
2. Adjust Z_o, Y_o, X_o and Gain using Steps 1 through 6 of Divider Trimming Procedure.
3. Convert to the Square Root configuration by connecting X_{IN} to the Output and inserting a diode between Pin 4 and the Output node.
4. With Z_{IN} = 0V adjust Z_o for zero Output voltage.

TYPICAL APPLICATIONS

MULTIPLICATION

POTENTIOMETERS FOR TRIMMING OFFSET AND FEEDTHROUGH

DIVISION

SQUARE ROOT

5

TYPICAL PERFORMANCE CURVES

AMPLITUDE AND PHASE AS A FUNCTION OF FREQUENCY

NONLINEARITY AS A FUNCTION OF FREQUENCY

FEEDTHROUGH AS A FUNCTION OF FREQUENCY

DEFINITION OF TERMS

Multiplication/Division Error: This is the basic accuracy specification. It includes terms due to linearity, gain, and offset errors, and is expressed as a percentage of the full scale output.

Feedthrough: With either input at zero the output of an ideal multiplier should be zero regardless of the signal applied to the other input. The output seen in a non-ideal multiplier is known as the feedthrough.

Nonlinearity: The maximum deviation from the best straight line constructed through the output data, expressed as a percentage of full scale. One input is held constant and the other swept through its nominal range. The nonlinearity is the component of the total multiplication/division error which cannot be trimmed out.

ORDERING INFORMATION

TYPE	TEMPERATURE RANGE	MULTIPLICATION ERROR	ORDER PART NUMBER
8013AM	-55°C to +125°C	±.5%	ICL 8013AM TZ
8013BM	-55°C to +125°C	±1%	ICL 8013BM TZ
8013CM	-55°C to +125°C	±2%	ICL 8013CM TZ
8013AC	0°C to +70°C	±.5%	ICL 8013AC TZ
8013BC	0°C to +70°C	±1%	ICL 8013BC TZ
8013CC	0°C to +70°C	±2%	ICL 8013CC TZ

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PACKAGE DIMENSIONS

TO-100

NOTE: Pin 5 connected to case.

INTERSIL

IH5110 — IH5115
General Purpose Sample & Hold

FEATURES

- Low cost
- Military and industrial temperature ranges
- ±10V input voltage range
- 0.5mV/sec drift typical @ $C_S = 0.01\mu F$
- TTL, DTL and CMOS compatible
- Short circuit protected
- Input offset voltage adjustable to < 100μV using a 20k potentiometer
- 0.1% guaranteed sample accuracy with 10V signals and $C_S = 0.01\mu F$
- Sample to hold offset is 5mV max

SCHEMATIC DIAGRAM

FIGURE 1

GENERAL DESCRIPTION

Each of the 5110 family is a complete Sample and Hold circuit, (except for sampling capacitor) including input buffer amplifier, output buffer amplifier and CMOS logic switching. The devices are designed to operate from ±15V and +5V supplies. The input logic is designed to "Sample" and "Hold" from standard TTL logic levels.

The design is such that the input and output buffering is performed by only one operational amplifier, by switching the sampling capacitor from the output back to input. Switches Q_1, Q_2, and Q_3 (see Fig. 1) accomplish this switching. In the sampling mode Q_1 and Q_3 are shorted and Q_2 is open; thus the op. amp. charges up the sampling capacitor. In the hold mode Q_1 and Q_3 are open and Q_2 is shorted; thus the sampling cap. is switched back to the non-inverting input of the op. amp.

This structure provides a very accurate d.c. gain of 1 with very fast settling times (i.e. 5μs); additionally the design has internal feedback to cancel charge injection effects (sample to hold offsets). Q_1 and Q_2 are driven 180 degrees out of phase to accomplish this charge nulling.

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ORDERING INFORMATION

TYPE	ORDER PART NUMBER	PACKAGE	TEMPERATURE RANGE
5110	IH5110IDE	16 Pin Hermetic DIP	-25°C to 85°C
5110	IH5110MDE	16 Pin Hermetic DIP	-55°C to 125°C
5111	IH5111IDE	16 Pin Hermetic DIP	-25°C to 85°C
5111	IH5111MDE	16 Pin Hermetic DIP	-55°C to 125°C
5112	IH5112IDE	16 Pin Hermetic DIP	-25°C to 85°C
5112	IH5112MDE	16 Pin Hermetic DIP	-55°C to 125°
5113	IH5113IDE	16 Pin Hermetic DIP	-25°C to 85°C
5113	IH5113MDE	16 Pin Hermetic DIP	-55°C to 125°C
5114	IH5114IDE	16 Pin Hermetic DIP	-25°C to 85°C
5114	IH5114MDE	16 Pin Hermetic DIP	-55°C to 125°C
5115	IH5115IDE	16 Pin Hermetic DIP	-25°C to 85°C
5115	IH5115MDE	16 Pin Hermetic DIP	-55°C to 125°C

CONNECTION DIAGRAM

Pin 1 is designated either by a dot or notch.

ABSOLUTE MAXIMUM RATINGS

Supply Voltages ..... ±16V
Power Dissipation 500mW
Operating Temperature ..... −25°C to 85°C
−55°C to 125°C
Storage Temperature Range ..... −65°C to 150°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

ELECTRICAL CHARACTERISTICS (Pin 7 = 5V, Pin 8 = GND, Pin 9 = −15V, Pin 11 = 15V, T_A = 25°C) Note 3

SYMBOL	CHARACTERISTIC	IH5110, 5112, 5114			IH5111, 5113, 5115			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Close	Aperature Time		120	200		120	200	ns
$t_{acq.}$	Acquisition Time for Max Analog Voltage Step							
	C_S = 0.1μF (0.1% Accur.)		25	35		25	35	μs
	C_S = 0.01μF (0.1% Accur.)		4	6		4	6	
	C_S = 0.001μF (0.1% Accur.) See fig. 4		4	6		4	6	
V_{drift}	Drift Rate							
	C_S = 0.1μF		0.3	2.5		0.3	2.5	mV/sec
	C_S = 0.01μF		0.5	5		0.5	5	
	C_S = 0.001μF See fig. 2		2.0	10		2.0	10	
V_{inject}	Charge Injection or Sample to Hold Offsets							
	C_S = 0.1μF		<1	5		<1	5	mV_{p-p}
	C_S = 0.01μF		<1	5		<1	5	
	C_S = 0.001μF See Note 1 & fig. 3		12	25		12	25	
V_{switch}	Switching Transients or Spikes (Duration Less than 2μs)							
	C_S = 0.1μF		0.1	0.5		0.1	0.5	V_p
	C_S = 0.01μF		0.1	0.5		0.1	0.5	
	C_S = 0.001μF See fig. 3		0.2	0.5		0.2	0.5	
V_{couple}	A.C. Feedthrough Coupled to Output			5			5	mV_{p-p}
V_{offset}	D.C. Offset When in Sample Mode (Trimmable to 0m V With Ext. 20kΩ Potentiometer) 5110			40				mV
	5111						40	
	5112			10				
	5113						10	
	5114			5				
	See fig. 2 5115						5	
R_{in}	Input Impedance in Hold or Sample Mode (f ≤ 10Hz)		100			100		MegΩ
$I_{\pm 15V}$	Plus or Minus 15V Supply Quiescent Current		3.4	6		3.4	6	mA
I_{5V}	5V Supply Quiescent Current		0.3	10		0.3	10	A
V_{analog}	D.C. Input Voltage Range			±7.5			±10	
$V_{A.C. range}$	A.C. Input Voltage Range See Note 2 & fig. 5	15			20			V
I_{strobe}	TTL Logic Strobe Input Current in Either Hold or Sample Mode		0.1	10		0.1	10	μA

NOTES: 1. Offset voltage of op. amp. must be adjusted to 0mV (using 20kΩ potentiometer) before charge injection is measured.
2. The A.C. input voltage range differs from the D.C. input voltage range. All versions will handle any analog input within the range of plus 10V to minus 10V; however the IH5110, 5112, 5114 has the added restriction that the peak to peak swing should be less than $15V_{p-p}$ i.e. ±7.5 Vac.
3. All of the electrical characteristics specs, are guaranteed with C_S = 0.01μF in series with 100Ω as per Fig. 2, C_S = 0.1μF & C_S = 0.001μF are for design aid only.
4. If supplies are reduced to ±12VDC, analog signal range will be reduced to ±7Vp-p.

APPLICATIONS INFORMATION

I. Typical Connection Diagram

NOTES: **1.** To trim output offset to 0mV, set strobe input to sample mode (3V), set analog input to GND, adjust potentiometer until S & H output is 0mV.
2. Use a low dielec[illegible] absorption capacitor such as polystyrene.

SAMPLE MODE occurs when logic input is greater than 2.4V.
HOLD MODE occurs when logic input is less than 0.8V.

FIGURE 2

II. Charge Injection (sample to hold offset) measurement circuit; also switching transients test circuit.

Adjust offset to 0mV before testing for charge injection. See note 1.

CHARGE INJECTION

SWITCHING TRANSIENTS

V_A = GND
LOGIC INPUT =
C_S = 0.01μF
+3V
0V

UPPER TRACE =
5V/DIV.
+3V
0V
LOWER TRACE = 5mV/DIV.
TIME = 10μs/cm

V_A = GND
LOGIC INPUT =
C_S = 0.01μs
+3V
0V

UPPER TRACE =
5V/DIV.
+3V
0V
LOWER TRACE = 500mV/DIV.
TIME = 10μs/cm

FIGURE 3

III. Typical Circuit for measurement of A.C. signal handling capability.

ACQUISITION TIME

NOTE: The acquisition time is actually a settling time spec. since the reading is only taken when the output has settled within 1% of its final value. The 6μs spec. (IH5111, 5113 & 5115 is the worst reading of the t_{on} or t_{off} settling time shown above. The above test can be performed with a 0 to +7.5V or 0 to −7.5V step for the IH5110, 5112, 5114.

FIGURE 4

IV. Typical Circuit for measurement of A.C. peak to peak signal handling capability.

A.C. PEAK TO PEAK

TYP. IH5111

To test this parameter, increase the amplitude of the signal generator until the output starts to distort (it will always show up on the positive excursion of the sine wave first); then back off until all distortion is gone. The resultant peak to peak swing must be greater than 15Vpp for the IH5110, 5112, 5114 and greater than 20Vpp for the IH5111, 5113, 5115.

FIGURE 5

V. Application Tips:

If you are undecided as to which sample and hold to use within the family, the following will give you a pretty good idea of the outstanding differences between the six models.

First, determine the voltage range you need to sample and hold.

The even numbered parts are designed to switch smaller a.c. signal amplitudes with the goal being to minimize the charge injection effects (sample to hold offsets). This charge injection error is shown in Fig. 3. Once the voltage offset is zeroed, the 5110 has typical error amplitudes of 1 to 2mVp-p (corresponds to 10pc to 20pc of charge). Thus one could sample very low level d.c. signals with extreme accuracy. If very low level a.c. signals are being sampled, voltage offset potentiometer can be adjusted for a zero charge injection effect. Once the potentiometer has been adjusted, there will be a zero error going from sample to hold; however there will be a d.c. error caused by adjusting the potentiometer for zero charge injection and not for zero voltage offset. In general, this d.c. error will be in the area of 2mV to 5mV.

The odd numbered parts are primarily designed to handle any input in the plus or minus 10V range, regardless of whether it is a.c. or d.c.; to obtain this, the charge injection is about a factor of 2 higher than the even numbered parts.

The use of Varafet switching elements similar to Intersil's IH401/401A leads to a trade-off between AC signal swing and charge injection.

After the voltage range and charge injection requirements have been determined, all that remains is to determine the input offset voltage the system can tolerate. By using the higher numbered parts, it is possible to eliminate the offset potentiometer if system accuracy will allow 5mV (5114, 5115) or 10mV (5112, 5113) due to the low input offset voltage on these devices.

The drift rate is specified at 10mV/sec. Max. for all models: this corresponds to approximately 100pA total leakage into a 0.01μF sampling capacitor (C_S). While the 10mV/sec. is the Max. encountered, a more typical reading is less than 1mV/sec. (true for any input between −10V and +10V); thus the IH5110 family is ideal for applications requiring very low drift or droop rates.

The aperture time is spec'd at 200ns Max. for all models, but a more typical value is 150ns; this is basically the off time of switch Q_1. The way this aperture time affects system accuracy is shown below:

Assume the input signal to the Sample and Hold is an a.c. signal of peak amplitude A (peak to peak swing is 2A) and frequency $2\pi f = w$, then $V_{input} = Ae^{jwt}$ then $dV/dt = Ae^{jwt}$. This means the slope of input signal = dV/dt; this slope is a maximum at t (time) = 0, this maximum value is wA (in amplitude). (i.e.) input frequency is 10kc, therefore dV/dt = $wA = 6.28 \times 10^4 \times 10V = 6.3 \times 10^5 V/sec.$ A = 10V, then slope or dV/dt = 0.63V/μs. Now if we wish error to be a Max. of say 1% of full scale 10V, we see that 100mV (1%/aperture time = 0.63V/μs. Solving this equation we see that aperture time must be 160ns or less to get 1% holding accuracy. Since our aperture time is 150ns typical, we have 1% accuracy in holding 10kHz varying signals; for signal frequencies 1kHz and less, Max. error is 0.1%. The simple interpretation of just how the off time of the switch causes this system error is due to the fact a finite time is required for the switch to react to a hold command; this reaction time manifests itself with a system voltage error because the time varying input signal is changing to a new value before the switch has actually turned off. (i.e.) in the above example off = 10kHz and A = 10V, suppose we gave the hold command (thru TTL logic) at t = 0 (a.c. signal goes thru zero pt.) At this point we have calculated the slope to be a Max. and equal to 0.63V/μs. If there were no aperture time error, we would read 0V at output of Sample and Hold; however because of finite time for switch to respond to hold command, 150ns passes before switch goes off. During this 150ns, the input signal has gone to 100mV above or below 0V, thus the stored value of signal will be 100mV and that is the reading at the output of the Sample and Hold. If the input frequency were 1kHz, the "error voltage" would be 10mV.

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VI. Connection for Hi-Speed Sample and Hold with following typical performance: w/C_S = 0.001
   a. 2μs settling time (acquisition time) to 1% accuracy
   b. 25mV charge injection amplitude
   c. 10mV/sec drift rate

HI-SPEED SAMPLE AND HOLD

NOTE: Typical times for the Sample and Hold to acquire the input are 2μs for turn on (output) goes to +10V and 3μs for turn off (output goes down to 0V). As a general note, all the electrical specifications are guaranteed with a sampling capacitor equal to 0.01μf. As the above application (Fig. 6) shows, other values of sampling capacitors can be used but the best combinations of S & H specs may not result with values other than 0.01μF. The only advantage of using a 0.001μF for C_S is the acquisition time is 2μs typical instead of 5μs typical (with 0.01μF; however the drift rate would be worse and charge injection would be affected). To minimize drift rate, use a 0.1μF capacitor; this should produce a 0.1mV/sec rate of change and a charge injection amplitude of 0.2mVp-p. Of course the acquisition time will be slowed down to the 25μs area. Also use a 0.1μs system for slow speed changes (i.e., input frequency is less than 1kHz. The series resistor should be about 100Ω-200Ω to stabilize the system.

FIGURE 6

PACKAGE OUTLINE

NOTE: Board drilling dimensions will equal standard practices for .020 diameter lead.

DEFINITION OF TERMS

Aperture Time: The time it takes to switch from sample mode to hold mode and the actual opening of switch.

Charge Injection: The amount of charge coupled across the switch with no input voltage.

Drift Rate: The amount of drift of output voltage at a rate caused by current flow through the storage capacitor.

$\left(\frac{dV}{dt} = \frac{i}{c}\right)$ This current is the leakage across the switch and the amplifier's bias current.

Feed Through: The amount of input signal that appears at the output when in the hold mode. Normally caused by capacitance across the switch.

Offset Voltage: Voltage measured at output with no input voltage and circuit in sample mode.

Acquisition Time: The time it takes amplifier to reach full scale output either plus or minus.

INTERSIL

AD590
Two-Terminal IC Temperature Transducer

FEATURES

- **Linear current output: 1μA/°K**
- **Wide range: −55°C to +150°C**
- **Two-terminal device: Voltage in/current out**
- **Laser trimmed to ±1°C calibration accuracy (AD590L)**
- **Excellent linearity: ±0.5°C over full range (AD590K, L)**
- **Wide power supply range: +4V to +30V**
- **Sensor isolation from case**
- **Low cost**

GENERAL DESCRIPTION

The AD590 is a two-terminal integrated circuit temperature transducer which produces an output current proportional to absolute temperature. The device acts as a high impedance, constant current regulator passing 1μA/°K for supply voltages between +4V and +30V. Laser trimming of the chip's thin film resistors is used to calibrate the device to 298.2μA output at 298.2°K (+25°C).

The AD590 should be used in any temperature sensing application between −55°C and +150°C in which conventional electrical temperature sensors are currently employed. The inherent low cost of a monolithic integrated circuit combined with the elimination of support circuitry makes the AD590 an attractive alternative for many temperature measurement situations. Linearization circuitry, precision voltage amplifiers, resistance-measuring circuitry and cold junction compensation are not needed in applying the AD590. In the simplest application a resistor, a power source and any voltmeter can be used to measure temperature.

In addition to temperature measurement, applications include temperature compensation or correction of discrete components, and biasing proportional to absolute temperature. The AD590 is available in chip form making it suitable for hybrid circuits and fast temperature measurements in protected environments.

The AD590 is particularly useful in remote sensing applications. The device is insensitive to voltage drops over long lines due to its high impedance current output. Any well-insulated twisted pair is sufficient for operation hundreds of feet from the receiving circuitry. The output characteristics also make the AD590 easy to multiplex: the current can be switched by a CMOS multiplexer or the supply voltage can be switched by a logic gate output.

SCHEMATIC DIAGRAM

OUTLINE DIMENSIONS AND PIN DESIGNATIONS

TO-52 PACKAGE

Dimensions shown in inches and (mm).

ORDERING INFORMATION

ACCURACY	NON-LINEARITY	ORDER PART NUMBER
±5.0°C max	±2.0°C max	AD590JH
±2.0°C max	±0.5°C max	AD590KH
±1.0°C max	±0.5°C max	AD590LH

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ABSOLUTE MAXIMUM RATINGS

(T_A = +25°C unless otherwise noted)

Forward Voltage (V^+ to V^-)	+44V
Reverse Voltage (V^+ to V^-)	−20V
Breakdown Voltage (Case to V^+ or V^-)	±200V
Rated Performance Temperature Range	−55°C to +150°C
Storage Temperature Range	−65°C to +275°C
Lead Temperature (Soldering, 10 sec)	+300°C

SPECIFICATIONS (Typical values at T_A = +25°C, V_S = 5V unless otherwise noted)

CHARACTERISTICS	AD5901	AD590J	AD590K	AD590L	AD590M	UNITS
Output Nominal Output Current @ +25°C (298.2°K)	298.2	298.2	298.2	298.2	298.2	μA
Nominal Temperature Coefficient	1.0	1.0	1.0	1.0	1.0	μA/°C
Calibration Error @ +25°C (notes)	±10.0max	± 5.0max	± 2.5max	± 1.0max	± 0.5max	°C
Absolute Error (−55 to +150°C) (Note 1) Without external calibration adjustment	±20.0max	±10.0max	± 5.5max	± 3.0max	± 1.7max	°C
With external calibration adjustment	± 5.8max	± 3.0max	± 2.0max	± 1.6max	± 1.0max	°C
Non-Linearity	± 3.0max	± 1.5max	± 0.8max	± 0.4max	± 0.3max	°C
Repeatability (Note 2)	± 0.1max	± 0.1max	± 0.1max	± 0.1max	± 0.1max	°C
Long Term Drift (Note 3)	± 0.1max	± 0.1max	± 0.1max	± 0.1max	± 0.1max	°C
Current Noise	40	40	40	40	40	pA/√Hz
Power Supply Rejection +4 < V_S < +5V	0.5	0.5	0.5	0.5	0.5	μA/V
+5 < V_S < +15V	0.2	0.2	0.2	0.2	0.2	μA/V
+15V < V_S < +30V	0.1	0.1	0.1	0.1	0.1	μA/V
Case Isolation to Either Lead	10^{10}	10^{10}	10^{10}	10^{10}	10^{10}	Ω
Effective Shunt Capacitance	100	100	100	100	100	pF
Electrical Turn-on Time (Note 1)	20	20	20	20	20	μS
Reverse Bias Leakage Current (Note 4)	10	10	10	10	10	pA
Power Supply Range	+4 to +30	+4 to +30	+4 to +30	+4 to +30	+4 to +30	Volts

Notes
1. Does not include self heating effects.
2. Maximum deviation between +25°C reading after temperature cycling between −55°C and +150°C; guaranteed, not tested.
3. Conditions: Constant +5V, constant +125°C; Guaranteed, not tested.
4. Leakage current doubles every +10°C.

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TYPICAL APPLICATIONS

Typical connection

INTERSIL

ICL8069 Series
Low Voltage Reference

FEATURES

- **Temperature Coefficient guaranteed to 10 ppm/°C max.**
- **Low Bias Current . . . 50μA min**
- **Low Dynamic Impedance**
- **Low Reverse Voltage**
- **Low Cost**

GENERAL DESCRIPTION

The ICL8069 is a 1.2V temperature compensated voltage reference. It uses the band-gap principal to achieve excellent stability and low noise at reverse currents down to 50μA. Applications include analog-to-digital converters, digital-to-analog converters, threshold detectors, and voltage regulators. Its low power consumption makes it especially suitable for battery operated equipment.

TYPICAL CONNECTION DIAGRAMS

(a) Simple Reference (1.2 volts or less)

(b) Buffered 10V Reference using a single supply.

(c) Double regulated 100mV reference for ICL7107 one-chip DPM circuit.

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ORDERING INFORMATION

MAX. TEMPERATURE COEFFICIENT OF V_{REF}	TEMP RANGE	ORDER PART #
.001%/°C	0°C to +70°C	ICL8069ACO
.0025 %/°C	0°C to +70°C	ICL8069BCQ
.005 %/°C	−55°C to +125°C	ICL8069CMQ
.005 %/°C	0°C to +70°C	ICL8069CCQ
.01 %/°C	−55°C to +125°C	ICL8069DMQ
.01 %/°C	0°C to +70°C	ICL8069DCQ

PIN CONFIGURATION AND PACKAGE DIMENSIONS

TWO LEAD TO-52 (Q Package)

Note: Pin 2 connected to case.

ABSOLUTE MAXIMUM RATINGS

Reverse Voltage ..... See Note 2
Forward Current 10mA
Reverse Current 10mA
Power Dissipation . Limited by max forward/reverse current
Storage Temperature ..... −65°C to +200°C
Operating Temperature
ICL8069C ..... 0°C to +70°C
ICL8069M ..... −55°C to +125°C
Lead Temperature (Soldering, 10 Sec) ..... 300°C

ELECTRICAL CHARACTERISTICS (@ 25°C unless otherwise noted)

CHARACTERISTICS	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse breakdown Voltage	$I_R = 500\mu A$	1.20	1.23	1.25	V
Reverse breakdown Voltage change	$50\mu A \le I_R \le 5mA$		15	20	mV
Reverse dynamic Impedance	$I_R = 50\mu A$ $I_R = 500\mu A$		1 1	2 2	Ω
Forward Voltage Drop	$I_F = 500\mu A$		.7	1	V
RMS Noise Voltage	$10Hz \le f \le 10kHz$ $I_R = 500\mu A$		5		μV
Breakdown voltage Temperature coefficient: ICL8069A ICL8069B ICL8069C ICL8069D	$I_R = 500\mu A$ T_A = operating temperature range (Note 3)			.001 .0025 .005 .01	%/°C
Reverse Current		.050		5	mA

TYPICAL PERFORMANCE CHARACTERISTICS

VOLTAGE CHANGE AS A FUNCTION OF REVERSE CURRENT

REVERSE VOLTAGE AS A FUNCTION OF CURRENT

REVERSE VOLTAGE AS A FUNCTION OF TEMPERATURE

Notes:

1) The diode should not be operated with shunt capacitances between 200pF and 0.22μF, as it may oscillate at some currents. If circuit strays in excess of 200pF are anticipated, a 4.7μF shunt capacitor will ensure stability under all operating conditions.
2) In normal use, the reverse voltage cannot exceed the reference voltage. However when plugging units into a powered-up test fixture, an instantaneous voltage equal to the compliance of the test circuit will be seen. This should not exceed 20V.
3) For the military part, measurements are made at 25°C, −55°C, and +125°C. The unit is then classified as a function of the worst case T.C. from 25°C to −55°C, or 25°C to +125°C.

INTERSIL

ICL8211, ICL8212
Micropower Voltage Detectors/Indicators

FEATURES

- High accuracy voltage sensing and generation: internal reference 1.15 volts typical
- Low sensitivity to supply voltage and temperature variations
- Wide supply voltage range: Typ. 1.8 to 30 volts
- Essentially constant supply current over full supply voltage range
- Easy to set hysteresis voltage range
- Defined output current limit - ICL8211
  High output current capability - ICL8212
- Innumerable useful applications including:
  1. Low voltage sensor/indicator
  2. High voltage sensor/indicator
  3. Non volatile out-of-voltage range sensor/indicator
  4. Programmable voltage reference or zener diode
  5. Series or shunt power supply regulator
  6. Fixed value constant current source

CONNECTION DIAGRAM

8 LEAD PLASTIC MINI DIP **TO99**

Pin 1 is designated by either a dot or a notch for dual inline package.

ORDERING INFORMATION

Part Number	Temperature Range	Package
ICL8211CPA	0 to +70°C	8 lead MiniDIP
ICL8211CTY	0 to +70°C	TO-99 Can
ICL8211MTY	-55 to +125°C	TO-99 Can
ICL8212CPA	0 to 70°C	8 lead MiniDIP
ICL8212CTY	0 to 70°C	TO-99 Can
ICL8212MTY	-55 to +125°C	TO-99 Can
ICL8211D	Dice only	
ICL8212D	Dice only	

GENERAL DESCRIPTION

The Intersil ICL8211/12 are micropower bipolar monolithic integrated circuits intended primarily for precise voltage detection and generation. These circuits consist of an accurate voltage reference, a comparator and a pair of output buffer/drivers.

Specifically, the ICL8211 provides a 7ma current limited output sink when the voltage applied to the 'THRESHOLD' terminal is less than 1.15 volts - the internal reference. The ICL8212 requires a voltage in excess of 1.15 volts to switch its output on (no current limit). Both devices have a low current output (HYSTERESIS OUTPUT) which is switched on for input voltages in excess of 1.15V. The HYSTERESIS output may be used to provide positive and noise free output switching using a simple feedback network.

Applications for the ICL8211/12 include a variety of voltage detection circuits such as low battery indicators (portable systems), power supply malfunction detectors for volatile memory systems, programmable zener diodes, both shunt and series power supply regulators, constant current sources.

The ICL8211/12 may be customized by the use of metal mask options to provide more complete integration on chip (including set resistors, etc.) for volume dedicated systems, thereby reducing component counts and cost.

SCHEMATIC DIAGRAM

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ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply Voltage ($V^+ - V^-$)	-0.5 to +30 volts
Output Voltage (with respect to V^-)	-0.5 to + 30 volts
Hysteresis Voltage (with respect to V^+)	+0.5 to -10 volts
Threshold Input Voltage	+30 to -5 volts with respect to V^- and +0 to -30 volts with respect to V^+
Current into Any Terminal	30mA
Power Dissipation (Note 2 & 3)	300mW
Operating Temperature Range ICL8211M/12M	-55°C to +125°C
Operating Temperature Range ICL8211C/12C	0 to +70°C
Storage Temperature Range	-55°C to +125°C

NOTE 1: Absolute maximum ratings define parameter limits that if exceeded may permanently damage or change the device.

NOTE 2: Rating applies for case temperatures to 125°C for ICL8211MTY/12MTY products. Derate linearly at -10mW/°C for ambient temperatures above 100°C.

NOTE 3: Derate linearly above 50°C by -10mW/°C for ICL8211C/12C products. The threshold input voltage may exceed +7 volts with respect to V- for short periods of time. However for continuous operation this voltage must be maintained at a value less than 7 volts.

TYPICAL OPERATING CHARACTERISTICS (V^+ to V^- = 5V, T_A = 25°C unless otherwise specified)

PARAMETER	SYMBOL	CONDITIONS	ICL8211 MIN	ICL8211 TYP.	ICL8211 MAX.	ICL8212 MIN.	ICL8212 TYP.	ICL8212 MAX.	UNITS
Supply Current	I^+	$2.0 < V^+ - V^- < 30$							
		V_T = 1.3V	10	22	40	50	110	250	μA
		V_T = 0.9V	50	140	250	10	20	40	μA
Threshold Trip Voltage	V_{TH}	I_{OUT} = 4mA $V^+ - V^-$ = 5V	0.98	1.15	1.19	1.00	1.15	1.19	V
		V_{OUT} = 2V $V^+ - V^-$ = 2V	0.98	1.145	1.19	1.00	1.145	1.19	V
		$V^+ - V^-$ = 30V	1.00	1.165	1.20	1.05	1.165	1.20	V
Threshold Voltage Disparity Between Output & Hysteresis Output	V_{THP}	I_{OUT} = 4mA V_{OUT} = 2V I_{HYST} = 7μA V_{HYST} = 3V		-8.0			-0.5		mV
Guaranteed Operating Supply Voltage Range	V_{OP}	+25°C	2.0		30	2.0		30	V
		0 to +70°C	2.2		30	2.2		30	V
		-55°C to +125°C	2.8		30	2.8		30	V
Typical Operating Supply Voltage Range	V_{OP}	+25°C	1.8		30	1.8		30	V
		+125°C	1.4		30	1.4		30	V
		-55°C	2.5		30	2.5		30	V
Threshold Voltage Temperature Coefficient	I_{VTH}	I_{OUT} = 4mA V_{OUT} = 2V		+200			+200		ppm/°C
Variation of Threshold Voltage with Supply Voltage	Δ_{VTH}	$\Delta(V^+ - V^-)$ = 10% at $V^+ - V^-$ = 5V		1.0			1.0		mV
Threshold Input Current	I_{TH}	V_{TH} = 1.15V		100	250		100	250	nA
		V_{TH} = 1.00V		5			5		nA
Output Leakage Current	I_{LO}	V_{OUT} = 30V V_{TH} = 1.0V						10	μA
		V_{OUT} = 30V V_{TH} = 1.3V			10				μA
		V_{OUT} = 5V V_{TH} = 1.0V						1	μA
		V_{OUT} = 5V V_{TH} = 1.3V			1				μA
Output Saturation Voltage	V_{SAT}	I_{OUT} = 4mA V_{TH} = 1.0V		0.17	0.4				V
		V_{TH} = 1.3V					0.17	0.4	V
Max Available Output Current	I_{HO}	(Note 4 & 5) V_{TH} = 1.0V	4	7.0	12				mA
		V_{OUT} = 5V V_{TH} = 1.3V				15	35		mA
		$-55°C \leq T_A \leq 125°C$ V_{TH} = 1.0V			15	12			mA
Hysteresis Leakage Current	I_{QHYST}	$V^+ + V^-$ = 10V V_{TH} = 1.0V V_{HYST} = V^-			0.1			0.1	μA
Hysteresis Sat Voltage	$V_{SATHYST}$	I_{HYST} = -7μA V_{TH} = 1.3V measured with respect to V^+		-0.1	-0.2		-0.1	-0.2	V
Max Available Hysteresis Current	I_{HHYST}	V_{TH} = 1.3V	-15	-21		-15	-21		μA

NOTE 4: The maximum output current of the ICL8211 is limited by design to 15ma under any operating condition. The output voltage may be sustained at any voltage up to +30 with respect to V^- as long as the maximum power dissipation of the device is not exceeded.

NOTE 5: The maximum output current of the ICL8212 is not defined and systems using the ICL8212 must therefore ensure that the output current does not exceed 50ma and that the maximum power dissipation of the device is not exceeded.

TYPICAL OPERATING CHARACTERISTICS

THRESHOLD INPUT CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE

Characteristics common to both the ICL8211 and the ICL8212

HYSTERESIS OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE

Characteristics ICL8211

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE

OUTPUT SATURATION CURRENT AS A FUNCTION OF TEMPERATURE

OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE

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TYPICAL OPERATING CHARACTERISTICS

Characteristics ICL8212

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

SUPPLY CURRENT AS A FUNCTION OF THRESHOLD VOLTAGE

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

OUTPUT SATURATION CURRENTS AS A FUNCTION OF THRESHOLD VOLTAGE

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF TEMPERATURE

THRESHOLD VOLTAGE TO TURN OUTPUTS "JUST ON" AS A FUNCTION OF SUPPLY VOLTAGE

OUTPUT SATURATION VOLTAGE AND CURRENT AS A FUNCTION OF TEMPERATURE

OUTPUT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

HYSTERESIS OUTPUT CURRENT AS A FUNCTION OF HYSTERESIS OUTPUT VOLTAGE

CIRCUIT DESCRIPTION

The ICL8211 and ICL8212 use a standard linear bipolar integrated circuit technology with high value thin film resistors. The reason for the use of thin film resistors is to be able to define extremely low value currents.

Components Q_1 thru Q_{10} and R_1, R_2 and R_3 set up an accurate voltage reference of 1.15 volts. This reference voltage is close to the value of the bandgap voltage for silicon and is highly stable with respect to both temperature and supply voltage. The deviation from the bandgap voltage is necessary due to the negative temperature coefficient of the thin film resistors (-5000 ppm per °C).

Components Q_2 thru Q_9 and R_2 make up a constant current source. Q_2 and Q_3 are identical and form a current mirror. Q_8 has 7 times the emitter area of Q_9. Due to the current mirror the collector currents of Q_8 and Q_9 are

forced to be equal and it can be shown that the collector current in Q_8 and Q_9 is

$$I_C\ (Q_8 \text{ or } Q_9) = \frac{1}{R_2} \times \frac{kT}{q} \ \ln 7$$

or approximately 1μA at 25°C

Where k = Boltzman's constant

q = charge on an electron

and T = absolute temperature in °K

Transistors Q_5, Q_6, and Q_7 assure that the collector to emitter voltage of Q_3, Q_4, and Q_9 remain constant with supply voltage variations thereby guaranteeing that the value of the constant current source is insensitive to supply voltage variations.

The base current of Q_1 provides sufficient current to ensure that the current source will start up; there being two stable states for this type of circuit - either as defined above or OFF if no start up current is provided. Leakage current in the transistors is not sufficient in itself to guarantee reliable startup.

Q_4 is matched to Q_3 and Q_2; and, Q_{10} is matched to Q_9. Thus the collector current and base emitter voltage Q_{10} are identical to that of Q_9 or Q_8. To generate the bandgap voltage it is necessary to sum a voltage equal to the base emitter voltage Q_9 to a voltage proportional to the difference of the base emitter voltages of two transistors Q_8 and Q_9 operating at two current densities.

$$\text{Thus } 1.15 = V_{BE}\ (Q_9 \text{ or } Q_{10}) + \frac{R_3}{R_2} \times \frac{kT}{q} \ \ln 7$$

$$\text{which provides } \frac{R_3}{R_2} = 12 \text{ (approx.)}$$

The total supply current consumed by the voltage reference section is approximately 6μA at room temperature. An input voltage at the THRESHOLD input is compared to the reference voltage 1.15 volts by the comparator consisting of transistors Q_{11} thru Q_{17}. The outputs from the comparator taken from the collectors of Q_{16} and Q_{17} are limited to two diode drops less than V^+ or approximately 1.1 volts. Thus the base current into the hysteresis output transistor is limited to about 500nA and the collector current of Q_{19} to 100μA.

In the case of the ICL8211, Q_{21} is proportioned to have 70 times the emitter area of Q_{20} thereby limiting the output current to approximately 7ma whereas, for the ICL8212 almost all the collector current of Q_{19} is available for base drive to Q_{21} resulting in a maximum available collector current of the order of 30ma. It is advisable to externally limit this current to 25ma or less.

APPLICATIONS

The ICL8211 and ICL8212 are similar in many respects especially with regard to the setup of the input trip conditions and hysteresis circuitry. The following discussion describes both devices and where differences occur they are clearly noted.

1. GENERAL INFORMATION

THRESHOLD INPUT CONSIDERATIONS

Although any voltage between -5V and V^+ may be applied to the THRESHOLD terminal, it is recommended that the THRESHOLD voltage does not exceed about +6 volts with respect to V^- since above that voltage the threshold input current increases sharply. Also, prolonged operation above this voltage will lead to degradation of device characteristics.

FIGURE 1 – VOLTAGE LEVEL DETECTION

The outputs change states with an input THRESHOLD voltage of approximately 1.15 volts. Input and output waveforms are shown in Figure 1 for a simple 1.15 volt level detector.

The HYSTERESIS output is a low current output and is intended primarily for input threshold voltage hysteresis applications. If this output is used for other applications it is suggested that output currents be limited to 10μA or less.

The regular OUTPUT's from either the ICL8211 or ICL-8212 may be used to drive most of the common logic families such as TTL or C-MOS using a single pullup resistor. The guaranteed TTL fanout for the ICL8211 is 2 and for the ICL8212 is 4.

FIGURE 2 – OUTPUT LOGIC INTERFACE

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A principal application of the ICL8211 is voltage level detection and for that reason the OUTPUT current has been limited to typically 7ma to permit direct drive to an LED lamp connected to the positive supply V^+ without a series current limiting resistor.

On the other hand the ICL8212 is intended for many applications such as programmable zener references and voltage regulators where output currents well in excess of 7ma are desirable. Therefore, the output of the ICL8212 is not current limited. If however, the output is used to drive an LED lamp then a series current limiting resistor must be used.

In many applications an input resistor divider network will be used. It is recommended that the current in this resistor network necessary to produce 1.15 volts be as follows. If the current in this network is of no concern, a current of 50μA may be used. If the current is a concern (battery operated systems) it is suggested a current of 6 to 8 μA represents a good compromise between accuracy and low power. Lower currents than 6μA are usable if accuracy is not important. The inaccuracy at lower currents is due to the input current of the device becoming a significant percentage of the current flowing in the resistor network.

FIGURE 3 – INPUT RESISTOR NETWORK CONSIDERATIONS

Case 1. High accuracy required, current in resistor network unimportant Set I = 50μA for V_{TH} = 1.15 volts ∴ $R_1 \Rightarrow$ 20K ohms.

Case 2. Good accuracy required, current in resistor network important Set I = 7.5μA for V_{TH} = 1.15 volts ∴ $R_1 \Rightarrow$ 150 K ohms.

SETUP PROCEDURES FOR VOLTAGE LEVEL DETECTION

Case 1. Simple voltage detection - no hysteresis

Unless an input voltage of approximately 1.15 volts is to be detected, resistor networks will be used to divide or multiply the unknown voltage to be sensed. Figure 4 shows procedures on how to set up resistor networks to detect INPUT VOLTAGES of any magnitude and polarity with respect to the negative supply V-.

a) Range of input voltage greater than +1.15 volts with respect to V-.
Input voltage to change the output states

$$= \frac{(R_1 + R_2)}{R_1} \times 1.15 \text{ volts}$$

b) Range of input voltage less than +1.15 volts with respect to V-.
Input voltage to change the output states

$$= \frac{(R_1 + R_2) \times 1.15}{R_1} - \frac{R_2\ V_{REF}}{R_1}$$

FIGURE 4 – INPUT RESISTOR NETWORK SETUP PROCEDURES

For supply voltage level detection applications the input resistor network is connected across the supply terminals as shown in Figure 5.

FIGURE 5 – COMBINED INPUT AND SUPPLY VOLTAGES

Conditions for correct operation of OUTPUT (terminal #4).

1. ICL8211
   1.8 volts ≤ Supply Voltage ≤ 30 volts
2. ICL8212
   0 ≤ Supply Voltage ≤ 30 volts

Case 2. Use of the HYSTERESIS function

The disadvantage of the simple detection circuits is that there is a small but finite input range whereby the outputs are neither totally 'ON' nor totally 'OFF'. The principle behind hysteresis is to provide positive feedback to the input trip point such that there is a voltage difference between the input voltage necessary to turn the outputs ON and to turn the outputs OFF.

The advantage of hysteresis is especially apparent in electrically noisy environments where simple but positive voltage detection is required. Hysteresis circuitry, however, is not limited to applications requiring better noise performance but may be expanded into highly complex systems with multiple voltage level detection and memory applications – refer to specific applications section.

There are two simple methods to apply hysteresis to a circuit for use in supply voltage level detection. These are shown in Figure 6.

a) Low trip voltage

$$V_{TR1} = \left[\frac{(R_1 + R_2) \times 1.15}{R_1} + 0.1\right] \text{ volts}$$

High trip voltage

$$V_{TR2} = \frac{(R_1 + R_2 + R_3)}{R_1} \times 1.15 \text{ volts}$$

b) Low trip voltage

$$V_{TR1} = \left[\frac{R_Q R_S}{(R_Q + R_S)} + R_P\right] \times \frac{1}{R_P} \times 1.15 \text{ volts}$$

High trip voltage

$$V_{TR2} = \frac{(R_P + R_Q)}{R_P} \times 1.15 \text{ volts}$$

FIGURE 6 – Two alternative voltage detection circuits employing hysteresis to provide pairs of well defined trip voltages.

Circuit (a) requires that the full current flowing in the resistor network be sourced by the HYSTERESIS output whereas for circuit (b) the current to be sourced by the HYSTERESIS output will be a function of the ratio of the two trip points and their values. For low values of hysteresis circuit (b) is to be preferred due to the offset voltage of the hysteresis output transistor.

A third way to obtain hysteresis (ICL8211 only) is to connect a resistor between the OUTPUT and the THRESHOLD terminals thereby reducing the total external resistance connected between the THRESHOLD and V⁻ terminals when the OUTPUT is switched on.

3. PRACTICAL APPLICATIONS

a) Low Voltage Battery Indicator

FIGURE 7 – LOW VOLTAGE BATTERY INDICATOR

This application is particularly suitable for portable or remote operated equipment which requires an indication of a depleted or discharged battery. The quiescent current taken by the system will be typically 35μA which will increase to 7ma when the lamp is turned on. R_3 will provide hysteresis if required.

b) |Non-Volatile| Low Voltage Detector

FIGURE 8 – LOW VOLTAGE DETECTOR AND MEMORY

In this application the high trip voltage V_{TR2} is set to be above the normal supply voltage range. On power up the initial condition is A. On momentarily closing switch S_1 the operating point changes to B and will remain at B until the

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supply voltage drops below V_{TR1} when the output will revert to condition A. Note that state A is always retained if the supply voltage is reduced below V_{TR1} (even to zero volts) and then raised back to V_{NOM}.

c) (Non-volatile) Power Supply Malfunction Recorder

In many systems a transient or an extended abnormal (or absence of a) supply voltage will cause a system failure. This failure may take the form of information lost in a volatile semiconductor memory stack, a loss of time in a timer or even possible irreversible damage to components if a supply voltage exceeds a certain value.

There is, therefore, a need to be able to detect and store a record that an **out-of-operating range** supply voltage condition has occurred, even in the case where a supply voltage may have dropped to zero. On power up to the normal operating voltage the record must have been retained and easily interrogated. This could be important in the case of, say, a transient power failure due to a faulty component or intermittent power supply, open circuit, etc., where direct observation of the failure is difficult.

A simple circuit to record an out of range voltage excursion may be constructed using an ICL8211, an ICL8212 plus a few resistors. This circuit will operate to 30 volts without exceeding the maximum ratings of the I.C.'s. The two voltage limits defining the in range supply voltage may be set to any value between 2.0 and 30 volts.

FIGURE 9 – SCHEMATIC OF RECORDER

FIGURE 10 – OUTPUT STATES OF THE ICL8211 AND ICL8212 AS A FUNCTION OF THE SUPPLY VOLTAGE

Referring to Figure 9, the ICL8212 is used to detect a voltage V_2 which is the upper voltage limit to the operating voltage range. The ICL8211 detects the lower voltage limit of the operating voltage range V_1. Hysteresis is used with the ICL8211 so that the output can be stable in either state over the operating voltage range V_1 to V_2 by making V_3 - the upper trip point of the ICL8211 much higher in voltage than V_2.

The output of the ICL8212 is used to force the output of the ICL8211 into the ON state above V_2. Thus there is no value of the supply voltage that will result in the output of the ICL8211 changing from the ON state to the OFF state. This may be achieved only by shorting out R_3 for values of supply voltage between V_1 and V_2.

d) Constant Current Sources

The ICL8212 may be used as a constant current source of value of approximately 25μA by connecting the THRESHOLD terminal to the V⁻ terminal. Similarly the ICL8211 will provide a 130μA constant current source. The equivalent parallel resistance is in the tens of megohms over the supply voltage range of 2 to 30 volts. These constant current sources may be used to provide biasing for various circuitry including differential amplifiers and comparators. See Typical Operating Characteristics for complete information.

FIGURE 11 – CONSTANT CURRENT SOURCE APPLICATIONS

e) Zener or Precision Voltage Reference

FIGURE 12 – PROGRAMMABLE ZENER OR VOLTAGE REFERENCE

The ICL8212 may be used to simulate a zener diode by connecting the OUTPUT terminal to the V_Z output and using a resistor network connected to the THRESHOLD terminal to program the zener voltage ($V_{ZENER} = \frac{(R_1 + R_2)}{R_1} \times 1.15$ volts).

Since there is no internal compensation in the ICL8212 it is necessary to use a large capacitor across the output to prevent oscillation.

Zener voltages from 2 to 30 volts may be programmed and typical impedance values between 300μA and 25ma will range from 4 to 7 ohms. The knee is sharper and occurs at a significantly lower current than other similar devices available.

f) Precision Voltage Regulators

FIGURE 13 – SIMPLE VOLTAGE REGULATOR

The ICL8212 may be used as the controller for a highly stable series voltage regulator. The output voltage is simply programmed using a resistor divider network R_1 and R_2. Two capacitors C_1 and C_2 are required to ensure stability since the ICL8212 is uncompensated internally.

This regulator may be used with lower input voltages than most other commercially available regulators and also consumes less power for a given output control current than any commercial regulator. Applications would therefore include battery operated equipment especially those operating at low voltages.

f) High supply voltage dump circuit

In many circuit applications it is desirable to remove the power supply in the case of high voltage overload. For circuits consuming less than 5ma this may be achieved using an ICL8211 driving the load directly. For higher load currents it is necessary to use an external pnp transistor or darlington pair driven by the output of the ICL8211. Resistors R_1 and R_2 set up the disconnect voltage and R_3 provides optional voltage hysteresis if so desired.

FIGURE 14 – HIGH VOLTAGE DUMP CIRCUITS

g) Frequency limit detectors

Simply frequency limit detectors providing a go/no-go output for use with varying amplitude input signals may be conveniently implemented with the ICL8211/12 devices. In the application shown the first device ICL8212 is used as a zero crossing detector. The output circuit consisting of R_3, R_4 and C_2 results in a slow output positive ramp. The negative range is much faster than the positive range. R_5 and R_6 provide hysteresis so that under all circumstances the second ICL8212 is turned on for sufficient time to discharge C_3 to V^-. The time constant of R_7 C_3 is much greater than R_4 C_2. Depending upon the desired output polarities for low and high input frequencies either an ICL8211 or an ICL8212 may be used as the output driver.

FIGURE 15 – FREQUENCY LIMIT DETECTOR

5

This circuit is sensitive to supply voltage variations and should be used with a stabilized power supply. At very low frequencies the output will switch at the input frequency.

h) Switch bounce filter

Single pole single throw (SPST) switches are less costly and more available than single pole double throw (SPDT) switches. SPST switches range from push button types, slide types to calculator keyboard types. A major problem with the use of SPST switches is the mechanical bounce of the electrical contacts on closure. Contact bounce times can range from a fraction of a millisecond to several tens of milliseconds depending upon the switch type. During this contact bounce time the switch may make and break contact several times.

The circuit shown in Figure 16 provides a rapid charge up of C_1 to close to the positive supply voltage (V^+) on a switch closure and a corresponding slow discharge of C_1 on a switch break. By proportioning the time constant of R_1 C_1 to approximately the manufacturer's bounce time the output at terminal #4 of the ICL8211/12 will be a single transition of state per desired switch closure.

SWITCH STATUS	OUTPUT ICL8211	OUTPUT ICL8212
CLOSED	HI	LO
OPEN	LO	HI

FIGURE 16 – SWITCH BOUNCE FILTER

j) Low voltage power disconnector

There are some classes of circuits that require the power supply to be disconnected if the power supply voltage falls below a certain value. As an example, the National LM199 precision reference has an on chip heater which malfunctions with supply voltages below 9 volts causing an excessive device temperature. The ICL8212 may be used to detect a power supply voltage of 9 volts and turn the power supply off to the LM199 heater section below that voltage.

FIGURE 17 – LOW VOLTAGE POWER SUPPLY DISCONNECT

CUSTOM OPTIONS

The ICL8211/12 have been designed with more on chip components than are used, in anticipation of more dedicated high volume system usage. The trigger voltage and hysteresis resistor network is integrated on chip but not connected. Consult the factory for more information on custom options.

DICE INFORMATION

ICL8211/12 dice may be die bonded using either eutectic or epoxy techniques, and may either be thermocompression gold ball or ultrasonic wire bonded.

CHIP TOPOGRAPHY

Die is passivated with a deposited oxide. Bonding pad oxide windows are 3.6 x 3.6 mils square.

PACKAGE DIMENSIONS

TO-99

NOTES: All dimensions in inches
Leads are gold-plated Kovar

8 LEAD PLASTIC DIP

NOTE: Board drilling dimensions will equal standard practices for .020 diameter lead.

INTERSIL

LM100, LM300
Voltage Regulator

FEATURES

- Output voltage adjustable from 2V to 30V
- One percent load and line regulation
- One percent stability over full military temperature range
- Adjustable short circuit current limiting
- Output currents in excess of 5A possible by adding external transistors
- Can be used as either a linear or high-efficiency switching regulator

GENERAL DESCRIPTION

The Intersil 100/300 monolithic integrated circuit is a voltage regulator. It is designed for use in applications that range from digital power supplies to precision regulators.

The output voltage is adjustable from 2V to 30V with a 1% load and line regulation. Short circuit current limiting is also adjustable. By adding external transistors, output currents in excess of 5A are possible.

The device can be used as either a linear or high-efficiency switching regulator, and will start on any load within rating. It responds quickly to both load and line transients and features small standby power dissipation, and freedom from oscillations with varying resistive and reactive loads.

CONNECTION DIAGRAMS

Flat Package

NOTE: Pin 4 connected to bottom of package.

TO-5

NOTE: Pin 4 connected to case.

SCHEMATIC DIAGRAM*

TYPICAL APPLICATIONS*

Basic Regulator Circuit

200 mA Regulator

2A Regulator With Foldback Current Limiting

4A Switching Regulator

* Pin connections shown are for Metal Can package.

5

ABSOLUTE MAXIMUM RATINGS

	LM100	LM300
Input Voltage	40V	35V
Input-Output Voltage Differential	40V	30V
Power Dissipation (Note 1)	500 mW	300 mW
Operating Junction Temperature Range	−55°C to +150°C	0°C to 70°C
Storage Temperature Range	−65°C to +150°C	−55°C to 125°C
Lead Temperature (Soldering, 60 sec)	300°C	260°C

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	LM100 MIN	LM100 TYP	LM100 MAX	LM300 MIN	LM300 TYP	LM300 MAX	UNITS
Input Voltage Range		8.5		40	8.0		30	V
Output Voltage Range		2.0		30	2.0		20	V
Output-Input Voltage Differential		3.0		30	3.0		20	V
Load Regulation (Note 3)	$R_{SC} = 0$, $I_O < 12$ mA		0.1	0.5		0.1	0.5	%
Line Regulation	$V_{IN} - V_{OUT} \leq 5V$		0.1	0.2		0.1	0.2	%/V
	$V_{IN} - V_{OUT} > 5V$		0.05	0.1		0.05	0.1	%/V
Temperature Stability	$-55°C \leq T_A \leq +125°C$		0.3	1.0				%
	$0°C \leq T_A \leq 70°C$					0.3	2.0	%
Feedback Sense Voltage			1.8			1.8		V
Output Noise Voltage	$10\ Hz \leq f \leq 10\ kHz$							
	$C_{REF} = 0$		0.005			0.005		%
	$C_{REF} = 0.1\ \mu F$		0.002			0.002		%
Long Term Stability			0.1	1.0		0.1	1.0	%
Standby Current Drain	$V_{IN} = 40V$		1.0	3.0				mA
	$V_{IN} = 30V$					1.0	3.0	mA
Minimum Load Current	$V_{IN} - V_{OUT} = 30V$		1.5	3.0				mA
	$V_{IN} - V_{OUT} = 20V$					1.5	3.0	mA

NOTE 1: The maximum junction temperature of the 100 is 150°C, while that of the 300 is 100°C. For operating at elevated temperatures devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the flat package, the derating is based on thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten 0.03-inch-wide, 2-ounce copper conductors. Peak dissipations to 1W are allowable providing the dissipation rating is not exceeded with the power averaged over a five second interval.

NOTE 2: These specifications apply for a junction temperature between −55°C and +150°C, (100) 0°C and 70°C, (300) for input and output voltages within the ranges given, and for a divider impedance seen by the feedback terminal of 2 kΩ, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

NOTE 3: The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.

INTERSIL

TYPICAL PERFORMANCE CHARACTERISTICS FOR 100, 300*

REGULATION CHARACTERISTICS WITHOUT CURRENT LIMITING

REGULATION CHARACTERISTICS WITH CURRENT LIMITING

CURRENT LIMITING CHARACTERISTICS

CURRENT LIMIT SENSE VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

SHORT CIRCUIT CURRENT AS A FUNCTION OF JUNCTION TEMPERATURE

OPTIMUM DIVIDER RESISTANCE VALUES AS A FUNCTION OF OUTPUT VOLTAGE

MINIMUM INPUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

REGULATOR DROPOUT VOLTAGE AS A FUNCTION OF JUNCTION TEMPERATURE

SUPPLY VOLTAGE REJECTION AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

MINIMUM LOAD CURRENT AS A FUNCTION OF INPUT-OUTPUT VOLTAGE DIFFERENTIAL

LOAD TRANSIENT RESPONSE

LINE TRANSIENT RESPONSE

*300 Only Guaranteed $0^\circ C \leq T_A \leq 70^\circ C$

5

DEFINITION OF TERMS

INPUT VOLTAGE RANGE: The range of DC input voltages over which the regulator will operate within specifications.

OUTPUT VOLTAGE RANGE: The range of regulated output voltages over which the specifications apply.

OUTPUT-INPUT VOLTAGE DIFFERENTIAL: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate within specifications.

LINE REGULATION: The percentage change in regulated output voltage for a change in input voltage.

LOAD REGULATION: The percentage change in regulated output voltage for a change in load from the minimum load to the maximum load current specified.

CURRENT-LIMIT SENSE VOLTAGE: The voltage across the current limit terminals required to cause the regulator to current-limit with a short circuited output. This voltage is used to determine the value of the external current-limit resistor when external booster transistors are used.

TEMPERATURE STABILITY: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

FEEDBACK SENSE VOLTAGE: The voltage, referred to ground, on the feedback terminal of the regulator while it is operating in regulation.

OUTPUT NOISE VOLTAGE: The average AC voltage at the output with constant load and no input ripple.

STANDBY CURRENT DRAIN: That part of the operating current of the regulator which does not contribute to the load current.

PACKAGE OUTLINES

NOTES: All dimensions in inches.
Leads are gold-plated Kovar.

ORDER NUMBER LM100T and LM300T

Order Number LM100F

INTERSIL

LM105, LM305
Voltage Regulator

FEATURES

- Output voltage adjustable from 4.5V to 40V (105)
- DC line regulation guaranteed at 0.03%/V
- Load regulation better than 0.1%
- Output current in excess of 10A possible by adding external resistor
- Direct, plug-in replacement for 100/300 giving improved regulation

GENERAL DESCRIPTION

The Intersil 105/305 monolithic integrated circuit is a positive voltage regulator. It is a direct replacement for the 100/300 with an extra gain stage added for improved regulation. In contrast to the 100/300, the 105/305 requires no minimum load current while permitting higher voltage operation by reducing standby current drain.

The Intersil 105/305 can be used as either a linear or switching regulator circuit with output voltages greater than 4.5V. It features fast response to both load and line transients, and freedom from oscillations with varying resistive and reactive loads.

SCHEMATIC DIAGRAM

CONNECTION DIAGRAMS

TO-5

NOTE: Pin 4 connected to case

Flat Package

NOTE: Pin 4 connected to bottom of package

TYPICAL APPLICATIONS*

10A Regulator with Foldback Current Limiting

Switching Regulator

1.0A Regulator with Protective Diodes

Shunt Regulator

*Pin connections shown are for TO-5

5

ABSOLUTE MAXIMUM RATINGS

	105	305
Input Voltage	50V	40V
Input-Output Voltage Differential	40V	40V
Power Dissipation (Note 1)	500 mW	500 mW
Operating Junction Temperature Range	−55°C to +150°C	0°C to 70°C
Storage Temperature Range	−65°C to +150°C	−55°C to 125°C
Lead Temperature (Soldering, 60 sec)	300°C	300°C

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	105 MIN	105 TYP	105 MAX	305 MIN	305 TYP	305 MAX	UNITS
Input Voltage Range		8.5		50	8.0		40	V
Output Voltage Range		4.5		40	4.5		30	V
Output-Input Voltage Differential		3.0		30	3.0		30	V
Load Regulation (Note 3)	$0 \leq I_O < 12$ mA							
	$R_{SC} = 18\Omega$, $T_A = 25°C$		0.02	0.05		0.02	0.05	%
	$R_{SC} = 10\Omega$, $T_A = 125°C$		0.03	0.1				%
	$R_{SC} = 18\Omega$, $T_A = -55°C$		0.03	0.1				%
	$R_{SC} = 15\Omega$, $T_A = 70°C$					0.03	0.1	%
	$R_{SC} = 18\Omega$, $T_A = 0°C$					0.03	0.1	%
Line Regulation	$V_{IN} - V_{OUT} \leq 5V$		0.025	0.06		0.025	0.06	%/V
	$V_{IN} - V_{OUT} > 5V$		0.015	0.03		0.05	0.03	%/V
Temperature Stability	$-55°C \leq T_A \leq +125°C$		0.3	1.0				%
	$0°C \leq T_A \leq 70°C$					0.3	1.0	%
Feedback Sense Voltage			1.8			1.8		V
Output Noise Voltage	$10\ Hz \leq f \leq 10\ kHz$							
	$C_{REF} = 0$		0.005			0.005		%
	$C_{REF} = 0.1\ \mu F$		0.002			0.002		%
Long Term Stability			0.1	1.0		0.1	1.0	%
Standby Current Drain	$V_{IN} = 50V$		0.8	2.0				mA
	$V_{IN} = 40V$					0.8	2.0	mA
Ripple Rejection	$C_{REF} = 10\ \mu F$, f = 120 Hz		0.003	0.01		0.003	0.01	%/V

NOTE 1: The maximum junction temperature of the 105 is 150°C, while that of the 305 is 85°C. For operating at elevated temperatures devices in the TO-5 package must be derated based on a thermal resistance of 150°C/W, junction to ambient or 45°C/W, junction to case. For the flat package, the derating is based on thermal resistance of 185°C/W when mounted on a 1/16-inch-thick epoxy glass board with ten 0.03-inch-wide, 2-ounce copper conductors. Peak dissipations to 1W are allowable providing the dissipation rating is not exceeded with the power averaged over a five second interval.

NOTE 2: These specifications apply for a junction temperature between −55°C and +150°C, (105) 0°C and 70°C, (305) for input and output voltages within the ranges given, and for a divider impedance seen by the feedback terminal of 2 kΩ, unless otherwise specified. The load and line regulation specifications are for constant junction temperature. Temperature drift effects must be taken into account separately when the unit is operating under conditions of high dissipation.

NOTE 3: The output currents given, as well as the load regulation, can be increased by the addition of external transistors. The improvement factor will be roughly equal to the composite current gain of the added transistors.

TYPICAL PERFORMANCE CHARACTERISTICS FOR 105,305*

LOAD REGULATION

LOAD REGULATION

CURRENT LIMITING CHARACTERISTICS

CURRENT LIMIT SENSE VOLTAGE

SHORT CIRCUIT CURRENT

OPTIMUM DIVIDER RESISTANCE VALUES

MINIMUM INPUT VOLTAGE

REGULATOR DROPOUT VOLTAGE

SUPPLY VOLTAGE REJECTION

MINIMUM OUTPUT VOLTAGE

STANDBY CURRENT DRAIN

TRANSIENT RESPONSE

*305 only guaranteed $0°C \leq T_A \leq 70°C$, V_{IN} = 40V max, V_{OUT} = 30V max.

DEFINITION OF TERMS

INPUT VOLTAGE RANGE: The range of DC input voltages over which the regulator will operate within specifications.

OUTPUT VOLTAGE RANGE: The range of regulated output voltages over which the specifications apply.

OUTPUT-INPUT VOLTAGE DIFFERENTIAL: The voltage difference between the unregulated input voltage and the regulated output voltage for which the regulator will operate within specifications.

LINE REGULATION: The percentage change in regulated output voltage for a change in input voltage.

LOAD REGULATION: The percentage change in regulated output voltage for a change in load from the minimum load to the maximum load current specified.

CURRENT-LIMIT SENSE VOLTAGE: The voltage across the current limit terminals required to cause the regulator to current-limit with a short circuited output. This voltage is used to determine the value of the external current-limit resistor when external booster transistors are used.

TEMPERATURE STABILITY: The percentage change in output voltage for a thermal variation from room temperature to either temperature extreme.

FEEDBACK SENSE VOLTAGE: The voltage, referred to ground, on the feedback terminal of the regulator while it is operating in regulation.

OUTPUT NOISE VOLTAGE: The average AC voltage at the output with constant load and no input ripple.

STANDBY CURRENT DRAIN: That part of the operating current of the regulator which does not contribute to the load current.

RIPPLE REJECTION: The line regulation for ac input signals at or above a given frequency with a specified value of bypass capacitor on the reference bypass terminal.

PACKAGE OUTLINES

NOTES: All dimensions in inches.
Leads are gold-plated Kovar.

Order Number LM105T and LM305T

Order Number LM105F

INTERSIL

LM723/LM723C/μA723
Voltage Regulator

FEATURES

- **150 mA output current without external pass transistor**
- **Output currents in excess of 10A possible by adding external transistors**
- **Input voltage 40V max**
- **Output voltage adjustable from 2V to 37V**
- **Can be used as either a linear or a switching regulator.**

GENERAL DESCRIPTION

The LM723/LM723C is a voltage regulator designed primarily for series regulator applications. By itself, it will supply output currents up to 150 mA; but external transistors can be added to provide any desired load current. The circuit features extremely low standby current drain, and provision is made for either linear or foldback current limiting.

The LM723/LM723C is also useful in a wide range of other applications such as a shunt regulator, a current regulator or a temperature-controller.

The LM723C is identical to the LM723 except that the LM723C has its performance guaranteed over a 0°C to 70°C temperature range, instead of −55°C to +125°C.

CONNECTION DIAGRAM

DUAL-IN-LINE PACKAGE

ORDER NUMBER
LM723J OR LM723CJ
LM723P OR LM723CP

METAL CAN PACKAGE

NOTE: Pin 5 connected to case.

ORDER NUMBER
LM723T OR LM723CT

BLOCK DIAGRAM

EQUIVALENT CIRCUIT*

*Pin numbers refer to metal can package.

5

ABSOLUTE MAXIMUM RATINGS

Pulse Voltage from V+ to V− (50 ms) 50V
Continuous Voltage from V+ to V− 40V
Input-Output Voltage Differential 40V
Maximum Amplifier Input Voltage (Either Input) 7.5V
Maximum Amplifier Input Voltage (Differential) 5V
Current from V_Z ..... 25 mA
Current from V_{REF} ..... 15 mA
Internal Power Dissipation Metal Can (Note 1) ..... 800 mW
Cavity DIP (Note 1) ..... 900 mW
Molded DIP (Note 1) ..... 660 mW
Operating Temperature Range LM723 ..... −55°C to +125°C
LM723C ..... 0°C to +70°C
Storage Temperature Range Metal Can ..... −65°C to +150°C
DIP ..... −55°C to +125°C
Lead Temperature (Soldering, 10 sec) ..... 300°C

ELECTRICAL CHARACTERISTICS (Note 2)

PARAMETER	CONDITIONS	LM723			LM723C			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Line Regulation	V_{IN} = 12V to V_{IN} = 15V		.01	0.1		.01	0.1	% V_{OUT}
	−55°C ≤ T_A ≤ +125°C			0.3				
	0°C ≤ T_A ≤ +70°C						0.3	
	V_{IN} = 12V to V_{IN} = 40V		.02	0.2		0.1	0.5	
Load Regulation	I_L = 1 mA to I_L = 50 mA		.03	0.15		.03	0.2	
	−55°C ≤ T_A ≤ +125°C			0.6				
	0°C ≤ T_A ≤ = +70°C						0.6	
Ripple Rejection	f = 50 Hz to 10 kHz, C_{REF} = 0		74			74		dB
	f = 50 Hz to 10 kHz, C_{REF} = 5μF		86			86		
Average Temperature Coefficient of Output Voltage	−55°C ≤ T_A ≤ +125°C		.002	.015				%/°C
	0°C ≤ T_A ≤ +70°C					.003	.015	
Short Circuit Current Limit	R_{SC} = 10Ω, V_{OUT} = 0		65			65		mA
Reference Voltage		6.95	7.15	7.35	6.80	7.15	7.50	V
Output Noise Voltage	BW = 100 Hz to 10 kHz, C_{REF} = 0		20			20		μVrms
	BW = 100 Hz to 10 kHz, C_{REF} = 5μF		2.5			2.5		
Long Term Stability			0.1			0.1		%/1000 hrs
Standby Current Drain	I_L = 0, V_{IN} = 30V		1.3	3.5		1.3	4.0	mA
Input Voltage Range		9.5		40	9.5		40	V
Output Voltage Range		2.0		37	2.0		37	
Input-Output Voltage Differential		3.0		38	3.0		38	

Note 1: See derating curves for maximum power rating above 25°C.
Note 2: Unless otherwise specified, T_A = 25°C, V_{IN} = V^+ = V_C = 12V, V− = 0, V_{OUT} = 5V, I_L = 1 mA, R_{SC} = 0, C_1 = 100 pF, C_{REF} = 0 and divider impedance as seen by error amplifier ≤ 10 KΩ connected as shown in Figure 1. Line and load regulation specifications are given for the condition of constant chip temperature. Temperature drifts must be taken into account separately for high dissipation conditions.
Note 3: L_1 is 40 turns of No. 20 enameled copper wire wound on Ferroxcube P36/22-3B7 pot core or equivalent with 0.009 in. air gap.
Note 4: Figures in parentheses may be used if R1/R2 divider is placed on opposite input of error amp.
Note 5: Replace R1/R2 in figures with divider shown in Figure 13.
Note 6: V^+ must be connected to a +3V or greater supply.
Note 7: For metal can applications where V_Z is required, an external 6.2 volt zener diode should be connected in series with V_{OUT}.

TYPICAL PERFORMANCE CHARACTERISTICS

LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

LOAD REGULATION CHARACTERISTICS WITH CURRENT LIMITING

LOAD & LINE REGULATION VS INPUT-OUTPUT VOLTAGE DIFFERENTIAL

CURRENT LIMITING CHARACTERISTICS

CURRENT LIMITING CHARACTERISTICS VS JUNCTION TEMPERATURE

STANDBY CURRENT DRAIN VS INPUT VOLTAGE

LINE TRANSIENT RESPONSE

LOAD TRANSIENT RESPONSE

OUTPUT IMPEDANCE VS FREQUENCY

5

MAXIMUM POWER RATINGS

LM723
POWER DISSIPATION VS AMBIENT TEMPERATURE

LM723C
POWER DISSIPATION VS AMBIENT TEMPERATURE

TABLE I: RESISTOR VALUES (KΩ) FOR STANDARD OUTPUT VOLTAGE

POSITIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		OUTPUT ADJUSTABLE ±10% (Note 5)			NEGATIVE OUTPUT VOLTAGE	APPLICABLE FIGURES	FIXED OUTPUT ±5%		5% OUTPUT ADJUSTABLE ±10%		
	(Note 4)	R1	R2	R1	P1	R2			R1	R2	R1	P1	R2
+3.0	1, 5, 6, 9, 12 (4)	4.12	3.01	1.8	0.5	1.2	+100	7	3.57	102	2.2	10	91
+3.6	1, 5, 6, 9, 12 (4)	3.57	3.65	1.5	0.5	1.5	+250	7	3.57	255	2.2	10	240
+5.0	1, 5, 6, 9, 12 (4)	2.15	4.99	.75	0.5	2.2	−6 (Note 6)	3, (10)	3.57	2.43	1.2	0.5	.75
+6.0	1, 5, 6, 9, 12 (4)	1.15	6.04	0.5	0.5	2.7	−9	3, 10	3.48	5.36	1.2	0.5	2.0
+9.0	2, 4, (5, 6, 12, 9)	1.87	7.15	.75	1.0	2.7	−12	3, 10	3.57	8.45	1.2	0.5	3.3
+12	2, 4, (5, 6, 9, 12)	4.87	7.15	2.0	1.0	3.0	−15	3, 10	3.65	11.5	1.2	0.5	4.3
+15	2, 4, (5, 6, 9, 12)	7.87	7.15	3.3	1.0	3.0	−28	3, 10	3.57	24.3	1.2	0.5	10
+28	2, 4, (5, 6, 9, 12)	21.0	7.15	5.6	1.0	2.0	−45	8	3.57	41.2	2.2	10	33
+45	7	3.57	48.7	2.2	10	39	−100	8	3.57	97.6	2.2	10	91
+75	7	3.57	78.7	2.2	10	68	−250	8	3.57	249	2.2	10	240

TABLE II: FORMULAE FOR INTERMEDIATE OUTPUT VOLTAGES

Outputs from +2 to +7 volts (Figures 1, 5, 6, 9, 12, (4)) $V_{OUT} = \left[V_{REF} \times \frac{R2}{R1 + R2}\right]$	**Outputs from +4 to +250 volts** (Figure 7) $V_{OUT} = \left[\frac{V_{REF}}{2} \times \frac{R2 - R1}{R1}\right]$; R3 = R4	**Current Limiting** $I_{LIMIT} = \frac{V_{SENSE}}{R_{SC}}$
Outputs from +7 to +37 volts (Figures 2, 4, (5, 6, 9, 12)) $V_{OUT} = \left[V_{REF} \times \frac{R1 + R2}{R2}\right]$	**Outputs from −6 to −250 volts** (Figures 3, 8, 10) $V_{OUT} = \left[\frac{V_{REF}}{2} \times \frac{R1 + R2}{R1}\right]$; R3 = R4	**Foldback Current Limiting** $I_{KNEE} = \left[\frac{V_{OUT}R3}{R_{SC}\,R4} + \frac{V_{SENSE}\,(R3 + R4)}{R_{SC}\,R4}\right]$ $I_{SHORT\ CKT} = \left[\frac{V_{SENSE}}{R_{SC}} \times \frac{R3 + R4}{R4}\right]$

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TYPICAL APPLICATIONS

TYPICAL PERFORMANCE

Regulated Ouput Voltage	5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

NOTE: $R_3 = \frac{R_1R_2}{R_1 + R_2}$ for minimum temperature drift.

FIGURE 1:
Basic Low Voltage Regulator
(V_{OUT} = 2 to 7 Volts)

TYPICAL PERFORMANCE

Regulated Ouput Voltage	15V
Line Regulation (ΔV_{IN} = 3V)	1.5 mV
Load Regulation (ΔI_L = 50 mA)	4.5 mV

NOTE: $R_3 = \frac{R_1R_2}{R_1 + R_2}$ for minimum temperature drift.

R_3 may be eliminated for minimum component count.

FIGURE 2:
Basic High Voltage Regulator
(V_{OUT} = 7 to 37 Volts)

TYPICAL PERFORMANCE

Regulated Ouput Voltage	-15V
Line Regulation (ΔV_{IN} = 3V)	1 mV
Load Regulation (ΔI_L = 100 mA)	2 mV

FIGURE 3:
Negative Voltage Regulator

TYPICAL PERFORMANCE

Regulated Ouput Voltage	+15V
Line Regulation (ΔV_{IN} = 3V)	1.5 mV
Load Regulation (ΔI_L = 1A)	15 mV

FIGURE 4:
Positive Voltage Regulator
(External NPN Pass Transistor)

TYPICAL PERFORMANCE

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 1A)	5 mV

FIGURE 5:
Positive Voltage Regulator
(External PNP Pass Transistor)

TYPICAL PERFORMANCE

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 10 mA)	1 mV
Short Circuit Current	20 mA

FIGURE 6:
Foldback Current Limiting

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TYPICAL APPLICATIONS (CON'T.)

TYPICAL PERFORMANCE

Regulated Output Voltage	+50V
Line Regulation (ΔV_{IN} = 20V)	15 mV
Load Regulation (ΔI_L = 50 mA)	20 mV

FIGURE 7:
Positive Floating Regulator

TYPICAL PERFORMANCE

Regulated Output Voltage	-100V
Line Regulation (ΔV_{IN} = 20V)	30 mV
Load Regulation (ΔI_L = 100 mA)	20 mV

FIGURE 8:
Negative Floating Regulator

TYPICAL PERFORMANCE

Regulated Output Voltage	+5V
Line Regulation (ΔV_{IN} = 30V)	10 mV
Load Regulation (ΔI_L = 2A)	80 mV

FIGURE 9:
Positive Switching Regulator

TYPICAL PERFORMANCE

Regulated Output Voltage	-15V
Line Regulation (ΔV_{IN} = 20V)	8 mV
Load Regulation (ΔI_L = 2A)	6 mV

FIGURE 10:
Negative Switching Regulator

NOTE: Current limit transistor may be used for shutdown if current limiting is not required.

TYPICAL PERFORMANCE

Regulated Ouput Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

FIGURE 11:
Remote Shutdown Regulator with Current Limiting

TYPICAL PERFORMANCE

Regulated Ouput Voltage	+5V
Line Regulation (ΔV_{IN} = 3V)	0.5 mV
Load Regulation (ΔI_L = 50 mA)	1.5 mV

FIGURE 12:
Shunt Regulator

FIGURE 13:
Output Voltage Adjust (See Note 5)

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INTERSIL

ICL8038 Precision Waveform Generator Voltage Controlled Oscillator

FEATURES

- Low Frequency Drift With Temperature – 50ppm/°C Max.
- Simultaneous Outputs – Sine-Wave, Square-Wave and Triangle.
- High Level Outputs – T^2L to 28V
- Low Distortion – 1%
- High Linearity – 0.1%
- Easy to Use – 50% Reduction in External Components.
- Wide Frequency Range of Operation 0.001Hz to 1.0MHz
- Variable Duty Cycle – 2% to 98%

GENERAL DESCRIPTION

The 8038 Waveform Generator is a monolithic integrated circuit, capable of producing sine, square, triangular, saw-tooth and pulse waveform of high accuracy with a minimum of external components (refer to Figures 8 and 9) The frequency (or repetition rate) can be selected externally over a range from less than 1/1000Hz to more than 1MHz and is highly stable over a wide temperature and supply voltage range. Frequency modulation and sweeping can be accomplished with an external voltage and the frequency can be programmed digitally through the use of either resistors or capacitors. The Waveform Generator utilizes advanced monolithic technology, such as thin film resistors and Schottky-barrier diodes. The 8038 Voltage Controlled Oscillator can be interfaced with phase lock loop circuitry to reduce temperature drift to below 50ppm/°C.

FUNCTIONAL DIAGRAM

FIGURE 1. BLOCK-DIAGRAM OF WAVEFORM GENERATOR.

CONNECTION DIAGRAM

ORDERING INFORMATION

TYPE	TEMPERATURE RANGE	STABILITY	PACKAGE	ORDER PART NUMBER
8038 CC	0°C to +70°C	50ppm/°C typ	DIP	ICL 8038 CC PD
8038 BC	0°C to +70°C	100ppm/°C max	DIP	ICL 8038 BC PD
8038 AC	0°C to +70°C	50ppm/°C max	DIP	ICL 8038 AC PD
8038 BM	–55°C to +125°C	100ppm/°C max	Hermetic DIP	ICL 8038 BM DD
8038 AM	–55°C to +125°C	50ppm/°C max	Hermetic DIP	ICL 8038 AM DD

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MAXIMUM RATINGS

Supply Voltage ..... ±18V or 36V Total
Power Dissipation ..... 750mW (Note 5)
Input Voltage (any pin) ..... Not To Exceed Supply Voltages
Input Current (Pins 4 and 5) 25mA
Output Sink Current (Pins 3 and 9) 25mA
Storage Temperature Range ..... −65°C to +125°C
Operating Temperature Range:
8038AM, 8038BM ..... −55°C to +125°C
8038AC, 8038BC, 8038CC ..... 0°C to +70°C
Lead Temperature (Soldering, 10 sec.) ..... 300°C

ELECTRICAL CHARACTERISTICS

(V_S = ±10V or +20V, T_A = 25°C, R_L = 10 KΩ, Unless Otherwise Specified) Note 3.

GENERAL CHARACTERISTICS	8038CC MIN	8038CC TYP	8038CC MAX	8038BC/BM MIN	8038BC/BM TYP	8038BC/BM MAX	8038AC/AM MIN	8038AC/AM TYP	8038AC/AM MAX	UNITS
Supply Voltage Operating Range										
Single Supply	+10		+30	+10		30	+10		30	V
Dual Supplies	±5		±15	±5		±15	±5		±15	V
Supply Current (V_S = ±10V) Note 1.										
8038AM, 8038BM					12	15		12	15	mA
8038AC, 8038BC, 8038CC		12	20		12	20		12	20	mA
FREQUENCY CHARACTERISTICS (all waveforms)										
Maximum Frequency of Oscillation	100,000			100,000			100,000			Hz
Sweep Frequency of FM		10			10			10		kHz
Sweep FM Range (Note 2)		40:1			40:1			40:1		
FM Linearity 10:1 Ratio		0.5			0.2			0.2		%
Frequency Drift With Temperature Note 6		50			50	100		20	50	ppm/°C
Frequency Drift With Supply Voltage (Over Supply Voltage Range)		0.05			0.05			0.05		%/V_S
Recommended Programming Resistors (R_A and R_B)	1000		1M	1000		1M	1000		1M	Ω
OUTPUT CHARACTERISTICS										
Square-Wave										
Leakage Current (V9 = 30v)			1			1			1	μA
Saturation Voltage (I_{SINK} = 2mA)		0.2	0.5		0.2	0.4		0.2	0.4	V
Rise Time (R_L = 4.7kΩ)		100			100			100		ns
Fall Time (R_L = 4.7kΩ)		40			40			40		ns
Duty Cycle Adjust	2		98	2		98	2		98	%
Triangle/Sawtooth/Ramp										
Amplitude (R_T = 100kΩ)	0.30	0.33		0.30	0.33		0.30	0.33		xV_S
Linearity		0.1			0.05			0.05		%
Output Impedance (I_{OUT} = 5mA)		200			200			200		Ω
Sine-Wave										
Amplitude (R_S = 100kΩ)	0.2	0.22		0.2	0.22		0.2	0.22		xV_S
THD (R_S = 1MΩ) Note 4.		0.8	5		0.7	3		0.7	1.5	%
THD Adjusted (Use Fig. 8b)		0.5			0.5			0.5		%

NOTE 1: R_A and R_B collection currents not included.
NOTE 2: V_S = 20V; R_A and R_B = 10kΩ, f ≅ 9kHz; Can be extended to 1000:1 See Figures 13 and 14
NOTE 3: All parameters measured in test circuit given in Fig. 2
NOTE 4: 82kΩ connected between pins 11 and 12, Triangle Duty Cycle set at 50%. (Use R_A and R_B)
NOTE 5: Derate plastic package at 6.7mW/°C for ambient temperatures above 50°C
Derate ceramic package at 12.5mW/°C for ambient temperatures above 100°C
NOTE 6: Over operating temperature range, Fig. 2, pins 7 and 8 connected, V_S = ±10V. See Fig. 6c for T.C. vs V_S

TEST CONDITIONS (See Fig. 2)

PARAMETER	R_A	R_B	R_L	C_1	SW_1	MEASURE
Supply Current	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Current into Pin 6
Maximum Frequency of Oscillation	1kΩ	1kΩ	4.7kΩ	100pf	Closed	Frequency at Pin 9
Sweep FM Range (Note 1)	10kΩ	10kΩ	10kΩ	3.3nF	Open	Frequency at Pin 9
Frequency Drift with Temperature	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 9
Frequency Drift with Supply Voltage (Note 2)	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Frequency at Pin 9
Output Amplitude: Sine	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk output at Pin 2
Triangle	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Pk-Pk output at Pin 3
Leakage Current (off) Note 3	10kΩ	10kΩ		3.3nF	Closed	Current into Pin 9
Saturation Voltage (on) Note 3	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Output (low) at Pin 9
Rise and Fall Times	10kΩ	10kΩ	4.7kΩ	3.3nF	Closed	Waveform at Pin 9
Duty Cycle Adjust: MAX	50kΩ	~1.6kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
MIN	~25kΩ	50kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 9
Triangle Waveform Linearity	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 3
Total Harmonic Distortion	10kΩ	10kΩ	10kΩ	3.3nF	Closed	Waveform at Pin 2

NOTE 1: The hi and lo frequencies can be obtained by connecting pin 8 to pin 7 (f_{hi}) and then connecting pin 8 to pin 6 (f_{lo}). Otherwise apply Sweep Voltage at pin 8 $(2/3\ V_{CC} + 2V) \leq V_{SWEEP} \leq V_{CC}$ where V_{CC} is the total supply voltage. In Fig. 2, Pin 8 should vary between 5.3V and 10V with respect to ground.

NOTE 2: $10V \leq V_{CC} \leq 30V$, or $\pm 5V \leq V_S \leq \pm 15V$.

NOTE 3: Oscillation can be halted by forcing pin 10 to +5 volts or −5 volts.

DEFINITION OF TERMS:

Supply Current	The current required from the power supply to operate the device, excluding load currents and the currents through R_A and R_B.
Frequency Range	The frequency range at the square wave output through which circuit operation is guaranteed.
Sweep FM Range	The ratio of maximum frequency to minimum frequency which can be obtained by applying a sweep voltage to Pin 8. For correct operation, the sweep voltage should be within the range $(2/3\ V_{CC} + 2V) < V_{sweep} < V_{CC}$.
FM linearity	The percentage deviation from the best-fit straight line on the control voltage versus output frequency curve.
Frequency Drift with Temperature	The change in output frequency as a function of temperature.
Frequency Drift with Supply Voltage	The change in output frequency as a function of supply voltage.
Output Amplitude	The peak-to-peak signal amplitude appearing at the outputs.
Saturation Voltage	The output voltage at the collector of Q_{23} when this transistor is turned on. It is measured for a sink current of 2mA.
Rise Time and Fall Time	The time required for the square wave output to change from 10% to 90%, or 90% to 10%, of its final value.
Triangle Waveform Linearity	The percentage deviation from the best-fit straight line on the rising and falling triangle waveform.
Total Harmonic Distortion	The total harmonic distortion at the sine-wave output.

TEST CIRCUIT

FIGURE 2

CHARACTERISTIC CURVES

FIGURE 3. PERFORMANCE OF THE SQUARE-WAVE OUTPUT (PIN 9).

FIGURE 4. PERFORMANCE OF TRIANGLE-WAVE OUTPUT.

FIGURE 5. PERFORMANCE OF SINE-WAVE OUTPUT.

FIGURE 6. CURRENT CONSUMPTION AND FREQUENCY STABILITY.

THEORY OF OPERATION

SQUARE-WAVE DUTY CYCLE – 50% SQUARE-WAVE DUTY CYCLE – 80%

FIGURE 7. PHASE RELATIONSHIP OF WAVEFORMS.

The performance of the sine-wave output is shown in Figure 5. Figure 6 shows additional general information concerning current consumption and frequency stability and Figure 7 shows the phase relationship between the three waveforms.

WAVEFORM TIMING

The *symmetry* of all waveforms can be adjusted with the external timing resistors. Two possible ways to accomplish this are shown in Figure 8. Best results are obtained by keeping the timing resistors R_A and R_B separate (a). R_A controls the rising portion of the triangle and sine-wave and the 1 state of the square-wave.

The magnitude of the triangle-waveform is set at 1/3 V_{CC}; therefore the rising portion of the triangle is,

$$t_1 = \frac{C \times V}{I} = \frac{C \times 1/3 \times V_{CC} \times R_A}{1/5 \times V_{CC}} = \frac{5}{3} R_A \times C$$

The falling portion of the triangle and sine-wave and the 0 state of the square-wave is:

$$t_2 = \frac{C \times V}{I} = \frac{C \times 1/3\, V_{CC}}{\frac{2}{5} \times \frac{V_{CC}}{R_B} - \frac{1}{5} \times \frac{V_{CC}}{R_A}} = \frac{5}{3} \times \frac{R_A R_B C}{2 R_A - R_B}$$

Thus a 50% duty cycle is achieved when $R_A = R_B$.

If the duty-cycle is to be varied over a small range about 50% only, the connection shown in Figure 8b is slightly more convenient. If no adjustment of the duty cycle is desired, terminals 4 and 5 can be shorter together, as shown in Figure 8c. This connection, however, carries an inherently larger variation of the duty-cycle.

With two separate timing resistors, the *frequency* is given by

$$f = \frac{1}{t_1 + t_2} = \frac{1}{\frac{5}{3} R_A C \left(1 + \frac{R_B}{2 R_A - R_B}\right)}$$

or, if $R_A = R_B = R$

$$f = \frac{0.3}{R C} \qquad \text{(for Figure 8a)}$$

If a single timing resistor is used (Figures 8c only), the frequency is

$$f = \frac{0.15}{R C}$$

Neither time nor frequency are dependent on supply voltage, even though none of the voltages are regulated inside the integrated circuit. This is due to the

FIGURE 8. POSSIBLE CONNECTIONS FOR THE EXTERNAL TIMING RESISTORS.

fact that both currents *and* thresholds are direct, linear function of the supply voltage and thus their effects cancel.

To minimize *sine-wave* distortion the 82kΩ resistor between pins 11 and 12 is best made a variable one. With this arrangement distortion of less than 1% is achievable. To reduce this even further, two potentiometers can be connected as shown in Figure 9. This configuration allows a reduction of sine-wave distortion close to 0.5%.

FIGURE 9. CONNECTION TO ACHIEVE MINIMUM SINE-WAVE DISTORTION.

SELECTING R_A, R_B and C

For any given output frequency, there is a wide range of RC combinations that will work. However certain constraints are placed upon the magnitude of the charging current for optimum performance. At the low end, currents of less than 1μA are undesirable because circuit leakages will contribute significant errors at high temperatures. At higher currents (I > 5 mA), transistor betas and saturation voltages will contribute increasingly larger errors. Optimum performance will be obtained for charging currents of 10μA to 1 mA. If pins 7 and 8 are shorted together, the magnitude of the charging current due to R_A can be calculated from:

$$I = \frac{R_1 \times V_{CC}}{(R_1 + R_2)} \times \frac{1}{R_A} = \frac{V_{CC}}{5R_A}$$

A similar calculation holds for R_B.

The capacitor value should be as large as possible.

WAVEFORM OUT LEVEL CONTROL AND POWER SUPPLIES

The waveform generator can be operated either from a single power-supply (10 to 30 Volts) or a dual power-supply (±5 to ±15 Volts). With a single power-supply the average levels of the triangle and sine-wave are at exactly one-half of the supply voltage, while the square-wave alternates between +V and ground. A split power supply has the advantage that all waveforms move symmetrically about ground.

The square-wave output is not committed. A load resistor can be connected to a different power-supply, as long as the applied voltage remains within the breakdown capability of the waveform generator (30V). In this way, the square-wave output be made TTL compatible (load resistor connected to +5 Volts) while the waveform generator itself is powered from a much higher voltage.

FREQUENCY MODULATION AND SWEEPING

The frequency of the waveform generator is a direct function of the DC voltage at terminal 8 (measured from $+V_{CC}$). By altering this voltage, frequency modulation is performed.

For small deviations (e.g. ±10%) the modulating signal can be applied directly to pin 8, merely providing dc decoupling with a capacitor, as shown in Figure 10a. An external resistor between pins 7 and 8 is not necessary, but it can be used to increase input impedance. Without it (i.e. terminals 7 and 8 connected together), the input impedance is 8kΩ; with it, this impedance increases to (R+8kΩ).

For larger FM deviations or for frequency sweeping, the modulating signal is applied between the positive supply voltage and pin 8 (Figure 10b). In this way the entire bias for the current sources is created by the modulating signal and a very large (e.g. 1000:1) sweep range is created (f = 0 at V_{sweep} = 0). Care must be taken, however, to regulate the supply voltage; in this configuration the charge current is no longer a function of the supply voltage (yet the trigger thresholds still are) and thus the frequency becomes dependent on the supply voltage. The potential on Pin 8 may be swept from V_{CC} to (2/3 V_{CC} + 2V).

FIGURE 10. CONNECTIONS FOR FREQUENCY MODULATION (a) AND SWEEP (b).

APPLICATIONS

FIGURE 11. SINE WAVE OUTPUT BUFFER AMPLIFIERS

The sine wave output has a relatively high output impedance (1KΩ Typ). The circuit of Figure 11 provides buffering, gain and amplitude adjustment. A simple op amp follower could also be used.

FIGURE 12. STROBE – TONE BURST GENERATOR

With a dual supply voltage the external capacitor on Pin 10 can be shorted to ground to halt the 8038 oscillation. Figure 12 shows a FEST switch, diode ANDed with an input strobe signal to allow the output to always start on the same slope.

FIGURE 13. VARIABLE AUDIO OSCILLATOR, 20Hz to 20 KHz

To obtain a 1000:1 Sweep Range on the 8038 the voltage across external resistors RA and RB must decrease to nearly zero. This requires that the highest voltage on control Pin 8 exceed the voltage at the top of RA and RB by a few hundred millivolts.

The Circuit of Figure 13 achieves this by using a diode to lower the effective supply voltage on the 8038. The large resistor on pin 5 helps reduce duty cycle variations with sweep.

FIGURE 14. LINEAR VOLTAGE CONTROLLED OSCILLATOR

The linearity of input sweep voltage verses output frequency can be significantly improved by using an op amp as shown in Figure 14.

This circuit is more fully described in "Electronics" magazine, October 30, 1975, page 96.

DETAILED SCHEMATIC

5 PACKAGE DIMENSIONS

14 PIN CERDIP

14 PIN PLASTIC DIP

Timers, Counters, and Digit Drivers

Watch and Clock Chip Chart

Timers

ICL8240/50/60	6-4
ICM7555/6	6-20
NE555	6-26
NE556	6-30

Counters

ICM7045	6-32
ICM7045A	6-40
ICM7208	6-42
ICM7215	6-50
ICM7216	6-56
ICM7226	6-72
ICM7217/27	6-84
ICM7224/25	6-96

Oscillators and Clock Generators

ICM7209	6-104
ICM7213	6-108

Timebases for Counters

ICM7207	6-114
ICM7207A	6-118

Display Drivers

ICM7211/12	6-120
ICM7218	6-130

Touch Tone Encoder

ICM7206/A/B	6-140

Counters, Timers and Display Drivers

Part Number	Circuit Description	Package	Crystal Frequency	Output
ICM7045A	Complete industrial stopwatch precision decade timer to count seconds, minutes or hours by selection of suitable oscillator frequencies.	28-Pin DIP	Seconds: 1.31 MHz Minutes: 2.18 MHz	Seven-digit common-cathode LED drive. Displays up to 240,000 seconds, 2,400 minutes, 24 hours.
ICM7201	Low battery voltage indicator	TO-72	Not applicable	Lights LED at voltage below 2.9V.
ICM7206	Touch-tone encoder; requires one contact per key	16-Pin DIP	3.57954 MHz	2-of-8 sine wave for tone dialing
ICM7206A	Touch-tone encoder; requires two contacts per key with common line connected to + supply.	16-Pin DIP	3.57954 MHz	2-of-8 sine wave for tone dialing
ICM7206B	Touch-tone encoder; common line connected to negative supply and oscillator enabled when key is pressed.	16-Pin DIP	3.57954 MHz	2-of-8 sine wave for tone dialing
ICM7207 ICM7207A	Frequency counter timebase. Includes 0.01, 0.1, or 1-second count window plus store, reset and MUX	14-Pin DIP 14-Pin DIP	6.5536 MHz 5.24288 MHz	Crysal frequency $\div 2^{13}$, $\div 2^{17}$, $\div 10$ (2^{17}) divider stage
ICM7208	7-digit unit counter. With addition of 7207 the circuit becomes a complete timer-frequency counter	28-Pin DIP	—	LED display drive
ICM7209	High-frequency clock-generator for 5-volt systems	8-Pin DIP	to 10 MHz	Crystal frequency, $\div 2^3$ divider stage
ICM7211 ICM7212	Four-digit display decoder drivers; ICM7211 is LCD; ICM7212 is LED; Non-multiplexed for low noise, BCD input, decoded display drive output.	40-Pin DIP (plastic)	—	Four-digit, seven-segment direct display drive; LED or LCD
ICM7213	Oscillator and frequency divider	14-Pin DIP (plastic)	to 10 MHz	1pps, 1ppm, 10 Hz, composite
ICM7216 ICM7226	Eight-digit universal counter; measures frequency, period, frequency ratio, time interval, units.	28-Pin DIP 40-Pin DIP (Cerdip, ceramic, plastic)	1 or 10 kHz	Eight-digit common anode or common cathode direct LED drive
ICM7217 ICM7227	Four-digit CMOS up/down counter; presettable start/count and compare register; for hard-wired or microprocessor control applications; cascadable	28-Pin Cerdip or plastic	—	Four-digit, seven-segment common anode or common cathode direct LED display drive; equal, zero, carry/borrow
ICM7218A/D ICM7218E	LED display driver system with 8 x 8 memory; numeric or dot (1 of 64) decoding; microprocessor compatible	28-Pin DIP 40-Pin DIP (ceramic or plastic)	—	Eight-digit, seven-segment plus decimal point; common cathode or common anode
ICM7219	Audio generator; digitally programmable; 5 bit input	14-Pin DIP (ceramic or plastic)		0-100 kHz output; waveform fully programmable
ICM7224 ICM7225	4½-digit high speed counter/decoder/driver; 25 MHz typ; ICM7224 is LCD, ICM7225 is LED; direct display drive; cascadable	40-Pin DIP (plastic)	—	4½-digit seven-segment direct display driver; LED or LCD
ICM7555 ICM7556	Single or dual CMOS version of industry-standard 555 timer; 80 μA typ. supply current; 500 kHz guaranteed; 2-18V power supply	8-Pin DIP 14-Pin DIP	—	
ICM7240 ICM7242 ICM7250 ICM7260	CMOS programmable counters/timers using external RC time base set. Programmable from minutes to years. Hr. accuracy = ± 0.5% typ.	16-Pin DIP	External	Timed output

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Watches and Clocks

All circuits available as dice

Part Number	Circuit Description	Package	Power	Crystal Frequency
ICM1115A/ ICM1115B	Quartz clock circuit, bipolar stepper motor application with simple alarm	8-Pin DIP	(1) 1.5-volt cell	4.194 MHz
ICM1424B	5-function LCD wristwatch circuit. Features: hrs, min, sec, month, date, 3½ digit display with rapid advance on setting	dice only	(1) 1.5-volt cell	32.768 kHz
ICM1424MB	Same electrical characteristics as ICM1424B but with mirror image configuration.	dice only	(1) 1.5-volt cell	32.768 kHz
ICM7038A	Quartz clock circuit with alarm, synchronous motor	8-Pin DIP	(2) 1.5-volt cells	2 to 10 MHz
ICM7038B	Quartz clock circuit with alarm, synchronous motor	8-Pin DIP	(1) 1.5 volt cell	2 to 10 MHz
ICM7045	Complete 4-function stop watch/24-hr. clock on single microcircuit chip with direct drive for LEDs on chip	28-Pin DIP	(3) 1.2 volt cells	6.5536 MHz
ICM7045A	Complete 4-function industrial stopwatch precision decade timer to count seconds, minutes or hours by selection of suitable oscillator frequencies	28-Pin DIP	(3) 1.2 volt cells	Seconds 1.31072 MHz Minutes 2.184533 MHz Hours 3.640889 MHz
ICM7049A	Quartz clock circuit, unipolar stepper motor application with complex alarm	8-Pin DIP	(1) 1.5-volt cell	4.1943 MHz
ICM7050	Quartz clock circuit, bipolar stepper motor application with complex alarm	8-Pin DIP	(1) 1.5-volt cell	4.1943 MHz
ICM7051A	Quartz automobile clock circuit for synchronous motor	8-Pin DIP	(1) 12.0-volt cell	4.1943 MHz
ICM7051B	Quartz automobile clock circuit for bipolar stepper motor	8-Pin DIP	(1) 12.0-volt cell	4.1943 MHz
ICM7205	Split and Taylor time stopwatch circuit with direct drive for LEDs on chip	24-Pin DIP	(3) 1.2-volt cells	3.2768 MHz
ICM7210/ ICM7210C	4-digit 6-function alpha-numeric LCD wristwatch circuit. Features: hrs, min, day, date, month, sec	dice only	(1) 1.5-volt cell	32.768 kHz
ICM7210M/MC	Same electrical characteristics as ICM7210 but with mirror image	dice only	(1) 1.5-volt cell	32.768 kHz
ICM7214A	6-function alpha-numeric LED readout wristwatch circuits with english, french, german and italian languages versions and perpetual calendar. Features: hrs, min, sec, day, date, month	24-Pin leadless	(2) 1.5-volt cells	32.768 kHz
ICM7215	Complete 4-function stopwatch including "time-out" function. Direct drive for LED on chip	24-Pin DIP	(3) 1.2-volt cells	32.768 kHz
ICM7220	6-digit and 6-function LCD wristwatch circuit, alphanumeric 12 or 24 hours	dice only	(1) 1.5-volt cell	32.768 kHz
ICM7220A	Same as ICM7220 with cricket alarm	dice only	(1) 1.5-volt cell	32.768 kHz
ICM7220B	Same as ICM7220 with two time zones	dice only	(1) 1.5-volt cell	32.768 kHz
ICM7220C	Same as ICM7220 with 1/10 sec. auto ranging chronograph.	dice only	(1) 1.5-volt cell	32.768 kHz
ICM7220M/ MA/MC	Same characteristics as 7220/A/C but with mirror image	dice only	(1) 1.5-volt cell	32.768 kHz
ICM7221	4-digit 6-function LCD watch circuit with alarm—can be used for clock circuits	dice only	(1) 1.5-volt cell	32.768 kHz
ICM7222	Same as ICM7220A	dice only		

6

INTERSIL

ICL8240, ICL8250, ICL8260 Programmable Timers/Counters

FEATURES

- Times from microseconds to minutes, hours, or days
- Time base set by simple R, C network or external clock
- Programmable with standard thumbwheel switches
- Select output count from
  - 1 RC to 255 RC (8240)
  - 1 RC to 99 RC (8250)
  - 1 RC to 59 RC (8260)
- Easily expanded to multiple decades (1 RC to 9,999 RC)
- Open collector outputs for flexibility
- High accuracy: ±0.5% typical
- Low drift: ±100ppm/°C typical
- Works over large supply range: 4V to 18V
- TTL compatible trigger and reset inputs

APPLICATIONS

- Programmable timing
  - Process timers
  - Appliance timers
  - Darkroom timers
- Programmable counter
  - Inventory/loading/filling
  - Counting/summing
- Frequency generation
  - Music synthesis
  - Harmonic synchronization
- Accurate, long-delay generator
- A/D conversion
- Digital Sample and Hold
- Pattern generation

PIN DIAGRAM

*NC FOR 8260

GENERAL DESCRIPTION

The 8240, 8250 and 8260 are a family of monolithic programmable timer circuits. They are intended to simplify the problem of selecting various time delays or frequency outputs available from a fixed oscillator circuit.

Each device consists of an accurate, low-drift oscillator a counter section of master-slave flip flops and appropriate logic and control circuitry all on one monolithic chip. The internal time base oscillator can be set with an external RC or can be disabled and the time base supplied from an external clock. The counter output taps are open collector transistors which can be programmed by a wire AND at external pins. Manual programming is easily accomplished by using standard thumbwheel switches. Additional logic circuitry will allow timing to be programmed by computer or microprocessor. These units are also very useful for generating ultra long delay times with relatively inexpensive RC components.

The 8260 is specifically designed to time accurate delays in seconds, minutes and hours. With its maximum count of 59 and carry out gate, a cascade of three 8260's will generate a one second clock from the 60 Hertz line, 60 seconds per minute and 60 minutes per hour programmable start to stop time. Thumbwheel switches with digits 0 to 5 and 0 to 9 are readily available to simplify the man-machine interface.

The 8250 is optimized for decimal counting and delays. It can be programmed by standard binary coded decimal (BCD) thumbwheel switches (0 to 9). Each unit gives 2 decades of counting allowing selection of time delays of from 1 RC to 99 RC. The carryout gate on the 8250 allows expansion to 9,999 or more.

The 8240 uses straight binary counting. With eight flip flops dividing down the base frequency, 8 suboctaves of the fundamental are available simultaneously in the astable mode. In the monostable mode the collectors can be wired AND to give any combination of pulse width of from 1 RC to 255 RC.

Applications for these versatile devices include appliance timers, darkroom timers and process timers. They can also be used as programmable counters. The internal clock can be disabled and the unit will count external pulses for programmable summing, loading or inventory applications. The internal clock can also be synchronized with the (m)th harmonic of an external sync and with the selectable counter, can provide a large number of non-harmonic frequencies from a single reference. Finally, they can be used as logic controlled switches in ramp type D-to-A and A-to-D converters.

ORDERING INFORMATION

TYPE	MAXIMUM COUNT	TEMPERATURE RANGE	16 PIN PACKAGE	ORDER PART NUMBER
8240C	255	0°C to +75°C	Plastic DIP	ICL 8240 C PE
8240M	255	-55°C to +125°C	Ceramic DIP	ICL 8240 M DE
8250C	99	0°C to +75°C	Plastic DIP	ICL 8250 C PE
8250M	99	-55°C to +125°C	Ceramic DIP	ICL 8250 M DE
8260C	59	0°C to +75°C	Plastic DIP	ICL 8260 C PE
8260M	59	-55°C to +125°C	Ceramic DIP	ICL 8260 M DE

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 18V
Power Dissipation
Ceramic Package 750mW
Derate above +25°C ..... 6mW/°C
Plastic Package 625mW
Derate above +25°C ..... 5.0mW/°C

Operating Temperature
8240M, 8250M, 8260M ..... −55°C to +125°C
8240C, 8250C, 8260C ..... 0°C to +75°C
Storage Temperature ..... −65°C to +150°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: See Figure 2, $V^+ = 5V$, $T_A = 25°C$, $R = 10k\Omega$, $C = 0.1\mu F$, unless otherwise noted.

PARAMETERS	8240M MIN.	8240M TYP.	8240M MAX.	8240C MIN.	8240C TYP.	8240C MAX.	UNITS	CONDITIONS
GENERAL CHARACTERISTICS								
Supply Voltage	4		18	4		18	V	For $V^+ < 4.5V$, Short Pin 15 to Pin 16
Supply Current								
Total Circuit (Reset)		3.5	6		4	7	mA	$V^+ = 5V$, $V_{TR} = 0$, $V_{RS} = 5V$
		12	16		13	18	mA	$V^+ = 15V$, $V_{TR} = 0$, $V_{RS} = 5V$
Total Circuit (Trigger)		24			24		mA	$V^+ = 15V$, $V_{TR} = 5V$, $V_{RS} = 0$ All outputs ON. (Worst Case)
Counter Only		1			1.5		mA	See Figure 3, 8240 only
Regulator Output, V_R	4.1	4.4		3.9	4.4		V	Measured at Pin 15, $V^+ = 5V$
(8240 only)	6.0	6.3	6.6	5.8	6.3	6.8	V	$V^+ = 15V$, See Figure 4
TIME BASE SECTION								See Figure 2
Timing Accuracy		0.5	2.0		0.5	5	%	$V_{RS} = 0$, $V_{TR} = 5V$, Note 1.
Temperature Drift		150	300		200		ppm/°C	$V^+ = 5V$ Over Operating Temperature
		80			80		ppm/°C	$V^+ = 15V$
Supply Drift		0.05	0.2		0.08	0.3	%/V	$V^+ \geq 8$ Volts, See Figure 11
Max. Frequency	100	130			130		kHz	$R = 1k\Omega$, $C = 0.007\mu F$
Time Base Output V_{TB} High	2.4	2.8		2.4	2.8		V	Measured at Pin 14 $I_{Source} = 80\mu A$
V_{TB} LOW		0.2	0.4		0.2	0.4	V	$I_{Sink} = 3.2mA$
Modulation Voltage Level	3.00	3.50	4.0	2.80	3.50	4.20	V	Measured at Pin 12 $V^+ = 5V$
		10.5			10.5		V	$V^+ = 15V$
Recommended Range of Timing Components								See Figure 8
Timing Resistor, R	0.001		10	0.001		10	MΩ	
Timing Capacitor, C	0.007		1000	0.01		1000	μF	
TRIGGER/RESET CONTROLS								
Trigger								
Trigger Threshold		1.4	2.0		1.4	2.0	V	Measured at Pin 11
Trigger Current		8			10		μA	$V_{RS} = 0$, $V_{TR} = 2V$
Impedance		25			25		kΩ	
Response Time		1			1		μsec.	Note 2
Reset								
Reset Threshold		1.4	2.0		1.4	2.0	V	Measured at Pin 10
Reset Current		8			10		μA	$V_{TR} = 0$, $V_{RS} = 2V$
Impedance		25			25		kΩ	
Response Time		0.8			0.8		μsec.	Note 2
COUNTER SECTION								See Figue 4, $V^+ = 5V$
Max. Toggle Rate	0.8	1.5			1.5		MHz	$V_{RS} = 0$, $V_{TR} = 5V$ Max Input to Pin 14
Input:								
Impedance		15			15		kΩ	Measured at Pin 14
Threshold	1.0	1.4		1.0	1.4		V	
Output:								Measured at Pins 1 thru 8
Rise Time		180			180		nsec.	$R_L = 3k$, $C_L = 10pf$
Fall Time		180			180			
V_{OUT} Low		0.2	0.4		0.2	0.4	V	$I_{SINK} = 3.2mA$
Leakage Current		0.01	8		0.01	15	μA	$V_{OH} = 15V$

NOTE 1: Timing error solely introduced by 8240, measured as % of ideal time-base period of T = 1.00 RC.
NOTE 2: Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at Pin 1.

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ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: See Figure 2, $V^+ = 5V$, $T_A = 25°C$, $R = 10k\Omega$, $C = 0.1\mu F$, unless otherwise noted.

PARAMETERS	8205M MIN.	8205M TYP.	8205M MAX.	8205C MIN.	8205C TYP.	8205C MAX.	UNITS	CONDITIONS
GENERAL CHARACTERISTICS								
Supply Voltage	4.5		18	4.5		18	V	
Supply Current								
Total Circuit (Reset)		3.5	6		4	7	mA	$V^+ = 5V$, $V_{TR} = 0$, $V_{RS} = 5V$
		12	16		13	18	mA	$V^+ = 15V$, $V_{TR} = 0$, $V_{RS} = 5V$
Total Circuit (Trigger)		24			24		mA	$V^+ = 15V$, $V_{TR} = 5V$, $V_{RS} = 0$ All outputs ON. (Worst Case)
TIME BASE SECTION								See Figure 2
Timing Accuracy		0.5	2.0		0.5	5	%	$V_{RS} = 0$, $V_{TR} = 5V$, Note 1
Temperature Drift		150	300		200		ppm/°C	$V^+ = 5V$ Over Operating Temp.
		80			80		ppm/°C	$V^+ = 15V$
Supply Drift		0.05	0.2		0.08	0.3	%/V	$V^+ \geq 8$ Volts, See Figure 11
Max. Frequency	100	130			130		kHz	$R = 1k\Omega$, $C = 0.007\ \mu F$
Time Base Output							V	Measured at Pin 14
V_{TB} HIGH	2.4	2.8		2.4	2.8		V	$I_{SOURCE} = 80\mu A$
V_{TB} LOW		0.2	0.4		0.2	0.4	V	$I_{SINK} = 3.2mA$
Modulation Voltage Level	3.00	3.50	4.0	2.80	3.50	4.20	V	Measured at Pin 12 $V^+ = 5V$
		10.5			10.5		V	$V^+ = 15V$
Recommended Range of Timing Components								See Figure 8
Timing Resistor, R	0.001		10	0.001		10	MΩ	
Timing Capacitor, C	0.007		1000	0.01		1000	μF	
TRIGGER/RESET CONTROLS								
Trigger								Measured at Pin 11
Trigger Threshold		1.4	2.0		1.4	2.0	V	
Trigger Current		8			10		μA	$V_{RS} = 0$, $V_{TR} = 2V$
Impedance		25			25		kΩ	
Response Time		1			1		μsec.	Note 2
Reset								
Reset Threshold		1.4	2.0		1.4	2.0	V	Measured at Pin 10
Reset Current		8			10		μA	$V_{TR} = 0$, $V_{RS} = 2V$
Impedance		25			25		kΩ	
Response Time		0.8			0.8		μsec.	Note 2
COUNTER SECTION								See Figure 4, $V^+ = 5V$
Max. Toggle Rate	0.8	1.5			1.5		MHz	$V_{RS} = 0$, $V_{TR} = 5V$ Max. Input Pin 14
Input:								
Impedance		15			15		kΩ	Measured at Pin 14
Threshold	1.0	1.4		1.0	1.4		V	
Output:								Measured at Pins 1 thru 8
Rise Time		180			180		nsec.	$R_L = 3k$, $C_L = 10pF$
Fall Time		180			180		nsec.	
V_{OUT} Low		0.2	0.4		0.2	0.4	V	$I_{SINK} = 3.2mA$
Leakage Current		0.01	8		0.01	15	μA	$V_{OH} = 15V$
CARRY OUT GATE								See Figure 4, $V^+ = 5V$
V_{CO} Low		0.2	0.4		0.2	0.4	V	Measured on Pin 15 $I_{SINK} = 3.2mA$
V_{CO} High	2.4	3.5		2.4	3.5		V	$I_{SOURCE} = 80\mu A$

NOTE 1: Timing error solely introduced by 8250, measured as % of ideal time-base period of T = 1.00 RC.
NOTE 2: Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at Pin 1.

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ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: See Figure 2, $V^+ = 5V$, $T_A = 25°C$, $R = 10k\Omega$, $C = 0.1\mu F$, unless otherwise noted.

PARAMETERS	8260M MIN.	8260M TYP.	8260M MAX.	8260C MIN.	8260C TYP.	8260C MAX.	UNITS	CONDITIONS
GENERAL CHARACTERISTICS								
Supply Voltage	4.5		18	4.5		18	V	
Supply Current								
Total Circuit (Reset)		3.5	6		4	7	mA	$V^+ = 5V$, $V_{TR} = 0$, $V_{RS} = 5V$
		12	16		13	18		$V^+ = 15V$, Vq4TR = 0, $V_{RS} = 5V$
Total Circuit (Trigger)		24			24			$V^+ = 15V$, $V_{TR} = 5V$, $V_{RS} = 0$ All outputs ON. (Worst Case)
TIME BASE SECTION								See Figure 2
Timing Accuracy		0.5	2.0		0.5	5	%	$V_{RS} = 0$, $V_{TR} = 5V$, Note 1
Temperature Drift		150	300		200		ppm/°C	$V^+ = 5V$ Over Operating Temp.
		80			80			$V^+ = 15V$
Supply Drift		0.05	0.2		0.08	0.3	%/V	$V^+ \geq 8$ Volts, See Figure 11
Max. Frequency	100	130			130		kHz	$R = 1k\Omega$, $C = 0.007\mu F$
Time Base Output V_{TB} HIGH	2.4	2.8		2.4	2.8		V	Measured at Pin 14 $I_{Source} = 80\mu A$
V_{TB} LOW		0.2	0.4		0.2	0.4		$I_{Sink} = 3.2mA$
Modulation Voltage Level	3.00	3.50	4.0	2.80	3.50	4.20		Measured at Pin 12 $V^+ = 5V$
		10.5			10.5			$V^+ = 15V$
Recommended Range of Timing Components								See Figure 8
Timing Resistor, R	0.001		10	0.001		10	MΩ	
Timing Capacitor, C	0.007		1000	0.01		1000	μF	
TRIGGER/RESET CONTROLS								
Trigger								Measured at Pin 11
Trigger Threshold		1.4	2.0		1.4	2.0	V	
Trigger Current		8			10		μA	$V_{RS} = 0$, $V_{TR} = 2V$
Impedance		25			25		kΩ	
Response Time		1			1		μsec.	Note 2
Reset								
Reset Threshold		1.4	2.0		1.4	2.0	V	Measured at Pin 10
Reset Current		8			10		μA	$V_{TR} = 0$, $V_{RS} = 2V$
Impedance		25			25		kΩ	
Response Time		0.8			0.8		μsec.	Note 2
COUNTER SECTION								See Figure 4, $V^+ = 5V$
Max. Toggle Rate	0.8	1.5			1.5		MHz	$V_{RS} = 0$, $V_{TR} = 5V$ Max Input Pin 14
Input:								
Impedance		20			20		kΩ	Measured at Pin 14
Threshold	1.0	1.4		1.0	1.4		V	
Output:								Measured at Pins 1 thru 7
Rise Time		180			180		nsec.	$R_L = 3k$, $C_L = 10pF$
Fall Time		180			180			
V_{OUT} Low		0.2	0.4		0.2	0.4	V	$I_{SINK} = 3.2mA$
Leakage Current		0.01	8		0.01	15	μA	$V_{OH} = 15V$
CARRY OUT GATE								See Figure 4, $V^+ = 5V$
V_{CO} Low		0.2	0.4		0.2	0.4	V	Measured on Pin 15 $I_{SINK} = 3.2mA$
V_{HIGH}	2.4	3.5		2.4	3.5			$I_{SOURCE} = 80\mu A$

NOTE 1: Timing error solely introduced by 8260, measured as % of ideal time-base period of T = 1.00 RC.
NOTE 2: Propagation delay from application of trigger (or reset) input to corresponding state change in counter output at Pin 1.

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BLOCK DIAGRAM

FIGURE 1.

FIGURE 2: Generalized Test Circuit

FIGURE 3: Test Circuit for Low-Power Operation (Time-Base Powered Down) 8240 Only

FIGURE 4: Test Circuit for Counter Section

FIGURE 5: Supply Current vs. Supply Voltage in Reset Condition

FIGURE 6: Recommended Range of Timing Component Values

FIGURE 7: Time-Base Period, T, as a Function of External RC

FIGURE 8: Minimum Trigger and Reset Pulse Widths at Pins 10 and 11

FIGURE 9: Power Supply Drift

FIGURE 10:
A) Minimum Trigger Delay Time Subsequent to Application of Power
B) Minimum Re-trigger Time, Subsequent to a Reset Input

FIGURE 11: Normalized Change in Time-Base Period As a Function of Modulation Voltage at Pin 12

FIGURE 12: Temperature Stability at V_{CC} = 5V

FIGURE 13: Temperature Stability at V_{CC} = 15V

6

INTRODUCTION TO PROGRAMMABLE TIMING

A timing diagram of waveforms and circuit states is shown in Figure 14. A generalized circuit connection for the 8240/50/60 is shown in Figure 15.

FIGURE 14: Timing Diagram of Output Waveforms (8240) (**NOTE:** BCD States are not all symmetrical)

The timing cycle is initiated by applying a positive-going trigger pulse to pin 11. This trigger pulse enables the counter section, sets all counter outputs to the "low" or "on" state, and starts the time base oscillator. Then external C is charged through external R from 20% to 70% of V^+, generating a timing waveform with period, T, equal to 1 RC. A short negative clock or time base pulse occurs during the capacitor discharge portion of the waveform. (Normally this time is small compared with the period T but has been enlarged for Figure 14.) These clock pulses are counted by the binary counter of the 8240 or by a Binary Coded Decimal (BCD) Counter in the 8250/60. The timing cycle terminates when a positive-going reset pulse is applied to pin 10. When the circuit is at reset state, both the time base and the counter sections are disabled and all the counter outputs are at a "high" or "off" state. The carry-out is also high.

In most timing applications, one or more of the counter outputs are connected back to the reset terminal, as shown in Figure 15, with S_1 closed. In this manner, the circuit will start timing when a trigger is applied and will automatically reset itself to complete the timing cycle when a programmed count is completed. If none of the counter outputs are connected back to the reset terminal (switch S_1 open), the circuit would operate in its astable or free-running mode, subsequent to a trigger input.

PROGRAMMING CAPABILITY

The counter outputs (pins 1 through 8) are open-collector type stages and can be shorted together to a common pull-up resistor to form a "wired-and" connection. The combined output will be "low" as long as any one of the outputs is low. In this manner, the time delays associated with each counter output can be *summed* by simply shorting them together to a common output bus as shown in Figure 15. For example, if only pin 6 is connected to the output and the rest left open, the total duration of the timing cycle. T_O, would be 32T for an 8240, and 20T for an 8250. Similarly, if pins 1, 5, and 6 were shorted to the output bus, the total time delay would be $T_O = (1 + 16 + 32)\ T = 49T$ (8240) or $(1 + 10 + 20)\ T \pm 31T$ (8250). In this manner, by proper choice of counter terminals connected to the output bus, one can program the timing cycle to be:

$$1T \leq T_O \leq 255T \text{ (8240)}$$
$$1T \leq T_O \leq 99T \text{ (8250)}$$
$$1T \leq T_O \leq 59T \text{ (8260)}$$

Note that for the 8250 and 8260 invalid count states (BCD values ≥ 10) will not be recognized, and the counter will not stop.

FIGURE 15: Generalized Circuit Connection for Timing Applications (Switch S_1 Open for Astable Operations, Closed for Monostable Operations)

THUMBWHEEL SWITCHES

While the 8240 is frequently hard wired for a particular function, the 8250 and 8260 can easily be programmed by using Thumbwheel switches. Standard BCD thumbwheel switches have four inputs (2^0, 2^1, 2^2, 2^3 or 1, 2, 4 and 8) and one "common", which are connected according to the binary equivalent of the digits 0 through 9.

For a single 8250 two such switches would select a time of from 01 RC to 99 RC. A cascade of two 8250's (using the carry out gate) would expand selection to 9999 RC. For an 8260 there are standard BCD Thumbwheel switches for the 0 through 5 digit (Twelve position, 0 to 5 repeated).

DESCRIPTION OF CIRCUIT CONTROLS

COUNTER OUTPUTS (PINS 1 THROUGH 8)

The binary counter outputs are buffered "open-collector" type stages, as shown in Figure 15. Each output is capable of sinking ≈ 5mA of load current. At reset condition, all the counter outputs are at high or non-conducting state. Subsequent to a trigger input, the outputs change state in accordance with the timing diagram of Figure 14.

The counter outputs can be used individually, or can be connected together in a wired-and configuration, as described in the Programming section.

GROUND (PIN 9)

This is the return or most negative supply for the device. It should have a very low impedance since capacitor discharge and other switched currents could create transients.

RESET AND TRIGGER INPUTS (PINS 10 AND 11)

The circuit is reset or triggered with positive-going control pulses applied to pins 10 and 11. The threshold level for these controls is approximately two diode drops (≈1.4V) above ground, and is therefore TTL/DTL compatible.

When power is applied to the 8240/50/60 with no trigger or reset inputs, the circuit reverts to "reset" state. Once triggered, the circuit is immune to additional trigger inputs, until the timing cycle is completed or a reset input is applied. If both the reset and the trigger controls are activated simultaneously, trigger overrides reset. Minimum pulse widths for reset and trigger inputs are shown in Figure 8.

MODULATION AND SYNC INPUT (PIN 12)

The period T of the time-base oscillator can be modulated by applying a dc voltage to this terminal (see Figure 11). The time-base oscillator can be synchronized to an external clock by applying a sync pulse to pin 12, as shown in Figure 26. Recommended sync pulse widths and amplitudes are also given in the figure.

TIMING TERMINAL (PIN 13)

The time-base period T is determined by the external RC network connected to this pin. When the time-base is triggered, the waveform at pin 13 is an exponential ramp with a period T = 1.0 RC. Figures 5 and 6 show RC values.

TIME-BASE OUTPUT (PIN 14)

Time-Base output is an open-collector type stage. An internal 10kΩ pull-up resistor is provided to ensure correct operation. At reset state, the time-base output is at "high" state. Subsequent to triggering, it produces a negative-going pulse train with a period T = RC, as shown in the diagram of Figure 14.

Time-base output is internally connected to the binary counter section and also serves as the input for the external clock signal when the circuit is operated with an external time-base.

The counter input triggers on the negative-going edge of the timing or clock pulses applied to pin 14. The trigger threshold for the counter section is ≈ +1.4 volts. The counter section can be disabled by clamping the voltage level at pin 14 to ground.

Under certain operating conditions such as high supply voltages (V+ > 7V) and small values of timing capacitor (C < 0.1μF) the pulse-width of the time-base output at pin 14 may be too narrow to trigger the counter section. This can be corrected by connecting a 300pF capacitor from pin 14 to ground.

CARRY OUTPUT (PIN 15, 8250 AND 8260 ONLY)

This pin will go HI for the last 10 counts of a 59 or 99 count, and can be used to drive another 8250 or 8260 counter stage, while still using all the counter outputs of the first. Thus, by cascading several 8250's a large BCD countdown can be achieved. The carry-out can also be used to drive TTL logic, etc.

REGULATOR OUTPUT (PIN 15, 8240 ONLY)

This terminal can serve as a V+ supply to additional 8240 circuits when several timer circuits are cascaded (see Figure 19), to minimize power dissipation. For circuit operation with external clock, pin 15 can be used as the V+ terminal to power-down the internal time-base and reduce power dissipation.

When the internal time-base is used with V+ ≤ 4.5V, pin 15 should be shorted to pin 16.

V+ (PIN 16)

This is the most positive supply voltage. (4.5V to 18V) A low supply impedance or 0.1μF to ground will help suppress voltage transients.

APPLICATIONS INFORMATION

PRECISION TIMING (Monostable Operation)

In precision timing applications, the 8240/50 is used in its monostable or "self-resetting" mode. The generalized circuit connection for this application is shown in Figure 16.

The output is normally "high" and goes to "low" subsequent to a trigger input. It stays low for the time duration T_O and then returns to the high state. The duration of the timing cycle T_O is given as:

$$T_O = NT = NRC$$

where T = RC is the time-base period as set by the choice of timing components at pin 13 (see Figure 7). N is an integer in the range of:

$$1 \leq N \leq 255\ (8240) \leq 99\ (8250) \leq 59\ (8260)$$

as determined by the combination of counter outputs (pins 1 through 8) connected to the output bus, as described before. (see page 7)

FIGURE 16: Circuit for Monostable Operation

ULTRA-LONG DELAY GENERATION

Two 8240/50/60 units can be cascaded as shown in Figure 17 to generate extremely long time delays. In this application, the reset and the trigger terminals of both units are tied together and the time base of Unit 2 disabled. In this manner, the output would normally be high when the system is at reset. Upon application of a trigger input, the output goes low for a total of $(256)^2$ or 65,536 cycles of the time-base oscillator (8240) or $(100)^2$ or 10,000 cycles (8250). The 8250/60 can also be connected as shown in Figure 18, allowing finer resolution in timing interval. The same applies to the 8260. PROGRAMMING: Total timing cycle of two cascaded 8240's can be programmed from T_O = 256RD to T_O = 65,536RC in 256 discrete steps by selectively shorting any one or the combination of the counter outputs from Unit 2 to the output bus. Two cascaded 8250's can be programmed from T_O = 1RC to T_O = 9999RC in 10,000 discrete steps by selectively shorting any combination of the counter outputs from both units to the output bus.

FIGURE 17: Cascaded Operation for Long Delay Generation (8240)

FIGURE 18: Cascaded Operation (8250 or 8260)

LOW-POWER OPERATION (8240 ONLY)

In cascaded operation, the time-base section of Unit 2 can be powered down to reduce power consumption, by using the circuit connection of Figure 19. In this case, the V+ terminal (pin 16) of Unit 2 is left open circuited, and the second unit is powered from the regulator output of Unit 1, by connecting pin 15 of both units. The V+ terminal of an 8250 can be connected to pin 15 of an 8240, but the power drain is not greatly reduced by this connection.

FIGURE 19: Low-Power Operation of Cascaded Timers (8240 only)

ELECTRONICALLY PROGRAMMED TIMER/COUNTER

The current interest in microprocessors, ROM's, PROM's, etc., requires timers which can be programmed electronically. Figures 20A and B show two ways of using readily available TTL/MSI logic to accomplish this. Although one is shown as a timer and the other as a counter, the choice of an external or internal clock would allow either circuit to perform either function.

The circuit of Figure 20A uses a standard 54/74 series TTL four bit magnitude comparator to compare the digitally programmed input with the 8240/50/60 counter outputs. The Greater, Less Than and Equal waveforms provide several outputs to choose from. An external start pulse triggers the timer and the A < B output is used as a reset.

FIGURE 20A: Electronically Programmed Timer

In Figure 20B two Quad Nor circuits with open collector outputs are wired together to form an inexpensive digital comparator. A start pulse triggers the 8240/50/60 counter and sets the output flip flop high. The digital comparator output goes high momentarily when A = B. This resets the flip flop which in turn resets the counter. For extended temperature range or higher speed operation, individual pull-up resistors may be needed on the counter outputs of both circuits 20A and 20B.

FIGURE 20B: Electronically Programmed Counter

ASTABLE OPERATION

The 8240/50 can be operated in its astable or free-running mode by disconnecting the reset terminal (pin 10) from the counter outputs. Two typical circuit connections for this mode of operation are shown in Figure 21. In the circuit connection of Figure 21(a), the circuit operates in its free-running mode, with external trigger and reset signals. It will start counting and timing subsequent to a trigger input until an external reset pulse is applied. Upon application of a positive-going reset signal to pin 10, the circuit reverts back to its rest state. The circuit of Figure 21(a) is essentially the same as that of Figure 15, with the feedback switch S_1 open.

The circuit of Figure 21(b) is designed for continuous operation. The circuit self-triggers automatically when the power supply is turned on, and continues to operate in its free-running mode indefinitely.

In astable or free-running operation, each of the counter outputs can be used individually as synchronized oscillators; or they can be interconnected or generate complex pulse patterns.

FIGURE 21: Circuit Connections for Astable Operation
(a) Operation with External Trigger and Reset Controls
(b) Free-running or Continuous Operation

BINARY OR DECIMAL PATTERN GENERATION

In astable operation, as shown in Figure 21, the output of the 8240/50 appears as a complex pulse pattern. The waveform of the output pulse train can be determined directly from the timing diagram of Figure 14 which shows the phase relations between the counter outputs. Figure 22 shows some of these complex pulse patterns. The pulse pattern repeats itself at a rate equal to the period of the *highest* counter bit connected to the common output bus. The minimum pulse width contained in the pulse train is determined by the *lowest* counter bit connected to the output.

FIGURE 22: Pulse Patterns Obtained by Shorting Various Counter Outputs (Shown for the 8240)

OPERATION WITH EXTERNAL CLOCK

The 8240/50 can be operated with an external clock or time-base, by disabling the internal time-base oscillator and applying the external clock input to pin 14. The recommended circuit connection for this application is shown in Figure 23. The internal time-base can be de-activated by connecting pin 13 to ground. The counters are triggered on the negative-going edges of the external clock pulse. For proper operation, a minimum clock pulse amplitude of 3 volts is required. Minimum external clock pulse width is 1μs.

FIGURE 23: Operation with External Clock

FREQUENCY SYNTHESIZER

The programmable counter section of 8240/50 can be used to generate many discrete frequencies from a given time base setting using the circuit connection of Figure 24. The output of the circuit is a positive pulse train with a pulse width equal to T, and a period equal to (N + 1) where N is the programmed count in the counter.

The modulus N is the *total count* corresponding to the counter outputs connected to the output bus. Thus, for example, if pins 1, 3 and 6 are connected together to the output bus, the total count is: N = 1 + 4 + 32 = 37 and the period of the output waveform is equal to (N + 1) T or 38T (25T for 8250). In this manner, many different frequencies can be synthesized from a given time-base setting.

FIGURE 24: Frequency Synthesis from Internal Time-Base

FIGURE 25: Frequency Synthesis by Harmonic Locking to an External Reference

FIGURE 26: Operation with External Sync Signal.
(a) Circuit for Sync Input
(b) Recommended Sync Waveform

HARMONIC SYNCHRONIZATION

The time-base can be synchronized with *integer multiples or harmonics* of an input sync frequency, by setting the time-base period, T, to be an integer multiple of the sync pulse period, T_S. This can be done by choosing the timing components R and C at pin 13 such that:

$$T = Rc = (T_S/m) \text{ where}$$
$$m \text{ is an integer, } 1 \leq m \leq 10.$$

Figure 27 gives the typical pull-in range for harmonic synchronization, for various values of harmonic modulus, m. For m < 10, typical pull-in range is greater than ±4% of time-base frequency. For m > 10, the circuit is too sensitive for reliable synchronization.

SYNTHESIS WITH HARMONIC LOCKING: The harmonic synchronization property of the 8240/50 time-base can be used to generate a wide number of discrete frequencies from a given input reference frequency. The circuit connection for this application is shown in Figure 25. (See Figures 26 and 27 for external sync waveform and harmonic capture range.) If the time base is synchronized to (m)th harmonic of input frequency where $1 \leq m \leq 10$, as described in the section on "Harmonic Synchronization", the frequency of f_O of the output waveform in Figure 25 is related to the input reference frequency f_R as:

$$f_O = f_R \frac{m}{(N + 1)}$$

where m is the harmonic number, and N is the programmed counter modulus. For a range of $1 \leq N \leq 255$, the circuit of Figure 19 can produce 2550 different frequencies from a single fixed reference.

One particular application of the circuit of Figure 25 is generating frequencies which are not harmonically related to a reference input. For example, by choosing the external RC to set m = 10 and setting N = 5, one can obtain a 100Hz output frequency synchronized to 60Hz power line frequency. See Figure 29.

FIGURE 27: Typical Pull-In Range for Harmonic Synchronization

6

8260 APPLICATIONS

The 8260 provides a convenient method of generating accurate long delays where the inputs are programmed in terms of seconds, minutes and hours. An example of this is the 100 hour timer shown in Fig. 28. The 8260 on the right uses the carryout gate to generate a one second clock from a 60 hertz line source. The diodes on the time base input rectify the input signal and alternately clamp and release the internal pull up resistor at pin 14. The input network depends on the amplitude of 60 Hertz signal available. The internal oscillators are disabled with a 1K resistor to ground at pin 13.

The second and third 8260's are programmable with thumbwheel switches up to 59 seconds and 59 minutes. The carryout of each divider drives the next counter. An 8250 was chosen as the final stage to give a maximum count of 99 hours. All Reset pins are tied together and back to the 10K output pull up at the thumbwheel switches. The timing cycle begins by closing the push button to pulse the trigger inputs which are also tied together. The output is a normally high voltage which goes low when triggered. The output will stay low until the counters reach the time programmed at the thumbwheel switches. At that time the output returns to the high state and resets all the counters.

Some applications require monitoring of the continuing count. The Intersil ICM7045 (or 7208) provides a counter chip plus direct drive to seven segment LED displays. The counter can be reset from the 8260 (or 8250) timer after the programmed count is reached.

The timing resolution can be increased to hundredths of a second by substituting 8250's for the initial stages and using the 60 Hertz line to generate a 100 Hertz clock. This was shown in Figure 25 under synthesis with harmonic locking. See Figure 29.

For applications with no 60 Hertz signal available the Intersil ICM7049 is recommended. This part works with a 4Mhz quartz crystal to generate a very stable one pulse per second clock frequency. See Figure 30.

FIGURE 28: Programmable 100 Hour Timer with Display

FIGURE 29: Front End for High Resolution Timer

FIGURE 30: Intersil 7049 CMOS 1 Second Reference Oscillator

STAIRCASE GENERATOR

The open collector outputs of the 8240/50/60 counter stages are useful in several applications where digitally sequenced switches are needed. One example is the staircase generator of Figure 31. In this circuit an array of resistors is switched to ground to generate binary (or BCD) weighted currents. The op amp converts these currents to an output voltage. Under reset condition the switches are off and the output is at ground. When a trigger is applied the output goes to V_{REF} and generates a negative going staircase of 256 (or 100) levels. The time duration of each stop is equal to the time base period (T = RC). The amplitude of the staircase can be varied by changing the input reference voltage. The staircase can be stopped at any desired level by applying a "disable" signal to pin 14 as shown.

FIGURE 31: Staircase Generator

DIGITAL SAMPLE AND HOLD

By adding a comparator and RS flip flop to the staircase circuit we obtain the digital sample and hold shown in Figure 32. When a "strobe" input is applied, the 8240/8250 is first reset and then triggered through the small RC at pin 11 which delays the strobe signal. The strobe also sets the flip flop which in turn enables the counter via pin 14. The op amp goes to the high state and begins to count down at a rate set by the counter time base. When the op amp output reaches the analog input to be sampled; the comparator switches, resetting the flip flop and stops the count. The op amp output will accurately hold the sampled value until the next strobe pulse is applied. If the 8240/50 time base is set as shown, the maximum acquisition time would be 256 (or 100) times .01 msec, or approximately 2.6 msec.

FIGURE 32: Digital Sample and Hold

ANALOG TO DIGITAL CONVERTER

Figure 33 shows an 8 bit binary (8240) or 2 digit BCD (8250) A/D converter using the staircase scheme of Figure 31. The operation is similar to the digital sample and hold of Figure 32 except digital outputs are taken off the counter output taps. In this circuit an input strobe pulse first resets then triggers the 8240/50 and sets the flip flop which enables the counter. The staircase from the op amp counts down until it reaches the analog input, at which time the comparator resets the flip flop and stops the count. The digital word at the 8 outputs is the complementary binary (or BCD) equivalent of the analog input. The maximum conversion time is again approximately 2.6 msec. The $\overline{Q}$ flip flop output is convenient to use as a data ready flag since its output goes high when the conversion is complete.

FIGURE 33: Analog-To-Digital Converter

PACKAGE DIMENSIONS

16 PIN CERAMIC DIP (DE)

16 PIN PLASTIC DIP (PE)

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INTERSIL

ICM7555
Low Power General Purpose Timer
ICM7556
Low Power Dual Timer

(High Performance Equivalents of the 555, 556, and 355 timers)

FEATURES

- **Exact equivalent in most cases for SE/NE555 or 556 or the 355.**
- **Low Supply Current** — **80μA Typ. (ICM7555)**, **160μA Typ. (ICM7556)**
- **Extremely low trigger, threshold and reset currents - 20pA Typical**
- **High speed operation - 500 kHz guaranteed**
- **Wide operation supply voltage range guaranteed 2 to 18 volts**
- **Well behaved Reset function - No crowbarring of supply during output transition.**
- **Can be used with higher impedance timing elements than regular 555/6 for longer RC time constants.**
- **Timing from microseconds through hours**
- **Operates in both astable and monostable modes**
- **Adjustable duty cycle**
- **High output source/sink driver-can drive TTL/CMOS**
- **Typical temperature stability of 0.005% per °C at 25°C**
- **Normally on and normally off output with very low offsets**
- **Completely static protected - no special handling considerations.**

GENERAL DESCRIPTION

The ICM7555/6 are CMOS RC timers providing significantly improved performance over the standard SE/NE555/6 and 355 timers, while at the same time being direct replacements for those devices in most applications. Improved parameters include the low supply current, wide operating supply voltage range, low THRESHOLD, TRIGGER and RESET currents, no crowbarring of the supply current during any output transition, higher frequency performance and no requirement to decouple CONTROL VOLTAGE for stable operation.

Specifically, the ICM7555/6 are stable controllers capable of producing accurate time delays or frequency. The ICM7556 is a dual ICM7555, with the two timers operating independently of one another, sharing only V^+(Vcc) and V^-(GND). In the time delay one shot mode of operation for each circuit, the time is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor, unlike the regular bipolar 555/6 devices, which also requires the CONTROL VOLTAGE terminal to be decoupled with a capacitor to prevent multiple output glitching during a transition. The circuits are triggered and reset on falling (negative) waveforms, and the output inverter can source or sink large currents to drive TTL loads or provide minimal offsets to drive CMOS loads.

APPLICATIONS

- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Missing Pulse Detector

ORDERING INFORMATION

ORDER PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7555IPA	-20 to 70°C	8 Lead MiniDip
ICM7555ITY	-20 to 70°C	TO-99 Can
ICM7555MTY	-55 to +125°C	TO-99 Can
ICM7556IPD	-20 to +70°C	14 Lead Plastic DIP
ICM7556MDD	-55 to +125°C	14 Lead Ceramic DIP
ICM7555D		DICE
ICM7556D		DICE

PIN CONFIGURATIONS (Top View)

ICM7555

TO-99

8-PIN DIP

ICM7556

6

ABSOLUTE MAXIMUM RATINGS (NOTE 1)

Supply Voltage V^+-V^-) +18 Volts

Input Voltage (Note 2)
- Trigger
- Threshold
- Reset
- Control Voltage

$\leq V^+ + 0.3V$ to $\geq V^- - 0.3V$

Output Current ..... 100 mA

Power Dissipation (Note 3) ICM7556 ..... 300 mW
ICM7555 ..... 200 mW

Operating Temperature Range
ICM7555IPA ..... -20°C to +70°C
ICM7555ITY ..... -20°C to +70°C
ICM7556IPD ..... -20°C to +70°C
ICM7555MTY ..... -55°C to +125°C
ICM7556MDD ..... -65°C to +150°C

Storage Temperature ..... -65°C to +150°C

Lead Temperature (Soldering 60 Seconds) ..... +300°C

OPERATING CHARACTERISTICS (T_A = 25°C, V^+-V^- = +2 to +15 Volts unless other specified)

PARAMETER	TEST CONDITIONS			VALUE MIN	VALUE TYP	VALUE MAX	UNITS
Supply Voltage	-20°C ≤ T_A ≤ +70°C -55°C ≤ T_A ≤ +125°C			2 3		18 16	V
Supply Current (Note 4)	ICM7555	V^+-V^- = 2V V^+-V^- = 18V			60 120	200 300	μA
Supply Current (Note 4)	ICM7556	V^+-V^- = 2V V^+-V^- = 18V			120 240	400 600	μA
Timing Error (Note 5)	R_A, R_B = 1k to 100k C = 0.1μF						
Initial Accuracy					2.0		%
Drift with Temperature					50		ppm/°C
Drift with Supply Voltage	V^+-V^- = 5V				1.0		%/Volt
Threshold Voltage					2/3(V^+-V^-)		V
Trigger Voltage					1/3(V^+-V^-)		V
Trigger Current	V^+-V^- = 18V V^+-V^- = 5V V^+-V^- = 2V				50 10 1		pA
Threshold Current	V^+-V^- = 18V V^+-V^- = 5V V^+-V^- = 2V				50 10 1		pA
Reset Current	V_{RESET} = V^-	V^+-V^- = 18V V^+-V^- = 5V V^+-V^- = 2V			100 20 2		pA
Reset Voltage	V^+-V^- = 18V V^+-V^- = 2V			0.4 0.4	0.7 0.7	1.0 1.0	V
Control Voltage Lead					2/3(V^+-V^-)		V
Output Voltage Drop	Output Lo	V^+-V^- = 18V V^+-V^- = 5V	I_{SINK} = 3.2mA I_{SINK} = 3.2mA		0.1 0.15	0.4 0.4	V
	Output Hi	V^+-V^- = 18V V^+-V^- = 5V	I_{SOURCE} = 1.0mA I_{SOURCE} = 1.0mA	17.8 4.0	17.25 4.5		V
Rise Time of Output	R_L = 10Mohms	C_L = 7pF	V^+-V^- = 5V		40.0		nS
Fall Time of Output	R_L = 10Mohms	C_L = 7pF	V^+-V^- = 5V		40.0		nS
Guaranteed Max Osc Freq	Astable Operation			500			kHz

NOTES:

1. Absolute Maximum ratings define stress limitations which, if exceeded, may permanently damage the device. These ratings may not be continuous duty ratings. For continuous operation these devices must be operated under the conditions defined under "OPERATING CHARACTERISTICS."
2. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V+ +0.3V or less than V^- -0.3V may cause destructive latchup. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple systems, the supply of the ICM7555/6 must be turned on first.
3. Junction temperatures should not exceed 135°C and the power dissipation must be limited to 20mW at 125°C. Below 125°C power dissipation may be increased to 300mW at 25°C. Derating factor is approximately 3mW/°C (7556) or 2mW/°C (7555).
4. The supply current value is essentially independent of the TRIGGER, THRESHOLD and RESET voltages.
5. For supply voltages between 5 and 15 volts.

6

TYPICAL CHARACTERISTICS

MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

OUTPUT SOURCE CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

OUTPUT SINK CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF SUPPLY VOLTAGE

DISCHARGE OUTPUT CURRENT AS A FUNCTION OF DISCHARGE OUTPUT VOLTAGE

PROPAGATION DELAY AS A FUNCTION OF VOLTAGE LEVEL OF TRIGGER PULSE

NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE AS A FUNCTION OF TEMPERATURE

FREE RUNNING FREQUENCY AS A FUNCTION OR RA, RB AND C

TIME DELAY IN THE MONOSTABLE MODE AS A FUNCTION OF RA AND C

6

APPLICATION NOTES

GENERAL

The ICM7555/6 devices are, in most instances, direct replacements for the NE/SE 555/6 devices. However, it is possible to effect economics in the external component count using the ICM7555/6. In general because the bipolar 555/6 devices produce large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The current transient is shown in Figure 2.

Figure 2: Supply Current Transient for a Standard Bipolar 555 During an Output Transition

The ICM7555/6 produces supply current spikes of only 2-3 mA instead of 300-400 mA and supply decoupling is normally not necessary. Secondly, in most instances, the CONTROL VOLTAGE decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. THUS, FOR MANY APPLICATIONS 2 CAPACITORS CAN BE SAVED USING AN ICM7555 AND 3 CAPACITORS WITH AN ICM7556.

POWER SUPPLY CONSIDERATIONS

Although the supply current consumed by the ICM7555/6 devices is very low, the total system supply can be high unless the timing components are high impedance. Therefore, use high values for R_A and R_B and low values for C in Figures 3 and 4.

OUTPUT DRIVE CAPABILITY

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5 volts or more the ICM7555/6 will drive at least 2 standard TTL loads.

ASTABLE OPERATION

The circuit can be connected to trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors. In this mode of operation, the capacitor charges and discharges between 1/3 and 2/3 (V^+-V^-). As in the triggered mode, the charge and discharge times, and therefore the frequency, are essentially independent of the supply voltage.

The frequency of oscillation is given by:

$$f = \frac{1}{t} = \frac{1.46}{(R_A + 2R_B)C}$$

Figure 3: Astable Operation

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot. Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative trigger pulse to pin 2, the flip flop is set which releases the short circuit across the external capacitor and drives the output high. The voltage across the capacitor now increases exponentially with a time constant $\gamma = R_AC$. When the voltage across the capacitor equals 2/3 ($V^+ - V^-$), the comparator resets the flip flop, which in turn discharges the capacitor rapidly and also drives the output to its low state.

Figure 4: Monostable Operation

CONTROL VOLTAGE

The CONTROL VOLTAGE terminal permits the two trip voltages for the THRESHOLD and TRIGGER internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the CONTROL VOLTAGE pin.

RESET

The RESET terminal is designed to have essentially the same trip voltage as the standard bipolar 555/6, i.e. 0.6 to 0.7 volts. At all supply voltages V^- to V^+ it represents an extremely high input impedance (Mohms). The mode of operation of the RESET function is, however, much improved over the standard bipolar 555/6 in that it controls only the internal flip flop, which in turn controls simultaneously the state of the OUTPUT and DISCHARGE pins. However, with the 555/6 the situation is much more complex and undesirable. When the RESET pin is slowly taken negatively through its trip voltage, the DISCHARGE terminal is initially partially turned on. Then the internal flip flop has its state changed. Finally the OUTPUT and the DISCHARGE pins are put into low impedance "LOW" states.

EQUIVALENT CIRCUIT

BLOCK DIAGRAM

This block diagram reduces the circuitry down to its simplest equivalent components.

TRUTH TABLE

THRESHOLD VOLTAGE	TRIGGER VOLTAGE	RESET	OUTPUT	DISCHARGE SWITCH
DON'T CARE	DON'T CARE	LOW	LOW	ON
$>2/3(V^+-V^-)$	$>2/3(V^+-V^-)$	HIGH	LOW	ON
$1/3<V_{TH}<2/3$	$1/3<V_{TH}<2/3$	HIGH	?	?
$<1/3(V^+-V^-)$	$<1/3(V^+-V^-)$	HIGH	HIGH	OFF

PACKAGE OUTLINES

TO-99 PACKAGE

8 LEAD PLASTIC DIP

14 PIN HERMETIC DUAL-IN-LINE PACKAGE

14 PIN PLASTIC DUAL-IN-LINE PACKAGE

NOTES 1 All leads gold plated KOVAR
2 All dimensions in inches (mm)

CHIP TOPOGRAPHIES

ICM7555

ICM7556

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INTERSIL

555
Precision Timer

FEATURES
- Timing From Microseconds Through Hours
- Operates In Both Astable And Monostable Modes
- Adjustable Duty Cycle
- High Current Output Can Source Or Sink 200mA
- Output Can Drive TTL
- Temperature Stability Of 0.005% Per °C
- Normally On And Normally Off Output

APPLICATIONS
- Precision Timing
- Pulse Generation
- Sequential Timing
- Time Delay Generation
- Pulse Width Modulation
- Pulse Position Modulation
- Missing Pulse Detector

GENERAL DESCRIPTION
The NE/SE 555 monolithic timing circuit is a highly stable controller capable of producing accurate time delays, or oscillation. Additional terminals are provided for triggering or resetting if desired. In the time delay mode of operation, the time is precisely controlled by one external resistor and capacitor. For a stable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled with two external resistors and one capacitor. The circuit may be triggered and reset on falling waveforms, and the output structure can source or sink large currents or drive TTL circuits.

BLOCK DIAGRAM

EQUIVALENT CIRCUIT

ORDERING INFORMATION

TYPE	PART NUMBER	TEMPERATURE RANGE	PACKAGE
555	NE555 V	0°C to 70°C	8 Pin DIP
555	NE555 T		TO-99
555	SE555 V	-55°C to 125°C	14 Pin Hermetic DIP
555	SE555 T		TO-99

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +18V
Power Dissipation 600mW
Operating Temperature Range
NE555 ..... 0°C to +70°C
SE555 ..... −55°C to +125°C
Storage Temperature Range ..... −65°C to +150°C
Lead Temperature (Soldering, 10 seconds) ..... +300°C

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: T_A = 25°C, V_{CC} = +5V to +15 unless otherwise specified

PARAMETER	TEST CONDITIONS	SE555 MIN	SE555 TYP	SE555 MAX	NE555 MIN	NE555 TYP	NE555 MAX	UNITS
Supply Voltage		4.5		18	4.5		16	V
Supply Current	V_{CC} = 5V R_L = ∞		3	5		3	6	mA
	V_{CC} = 15V R_L = ∞		10	12		10	15	
	Low State, Note 1							
Timing Error	R_A, R_B = 1kΩ to 100kΩ							
Initial Accuracy	C = 0.1μF Note 2		0.5	2		1		%
Drift with Temperature			30	100		50		ppm/°C
Drift with Supply Voltage			0.005	0.02		0.01		%/Volt
Threshold Voltage			2/3			2/3		X V_{CC}
Trigger Voltage	V_{CC} = 15V	4.8	5	5.2		5		V
	V_{CC} = 5V	1.45	1.67	1.9		1.67		
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Threshold Current	Note 3		0.1	.25		0.1	.25	μA
Control Voltage Level	V_{CC} = 15V	9.6	10	10.4	9.0	10	11	V
	V_{CC} = 5V	2.9	3.33	3.8	2.6	3.33	4	
Output Voltage Drop (low)	V_{CC} = 15V							
	I_{SINK} = 10mA		0.1	0.15		0.1	.25	
	I_{SINK} = 50mA		0.4	0.5		0.4	.75	
	I_{SINK} = 100mA		2.0	2.2		2.0	2.5	
	I_{SINK} = 200mA		2.5			2.5		
	V_{CC} = 5V							
	I_{SINK} = 8mA		0.1	0.25				
	I_{SINK} = 5mA					.25	.35	
Output Voltage Drop (high)	I_{SOURCE} = 200mA		12.5			12.5		
	V_{CC} = 15V							
	I_{SOURCE} = 100mA							
	V_{CC} = 15V	13.0	13.3		12.75	13.3		
	V_{CC} = 5V	3.0	3.3		2.75	3.3		
Rise Time of Output			100			100		nsec
Fall Time of Output			100			100		

NOTE 1: Supply Current when output high typically 1mA less.
NOTE 2: Tested at V_{CC} = 5V and V_{CC} = 15V.
NOTE 3: This will determine the maximum value of $R_A + R_B$. For 15V operation, the max. total R = 20 megohm.

TYPICAL CHARACTERISTICS

MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING

SUPPLY CURRENT VS SUPPLY VOLTAGE

HIGH OUTPUT VOLTAGE VS OUTPUT SOURCE CURRENT

LOW OUTPUT VOLTAGE VS OUTPUT SINK CURRENT

LOW OUTPUT VOLTAGE VS OUTPUT SINK CURRENT

LOW OUTPUT VOLTAGE VS OUTPUT SINK CURRENT

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DELAY TIME VS SUPPLY VOLTAGE

DELAY TIME VS TEMPERATURE

PROPAGATION DELAY VS VOLTAGE LEVEL OF TRIGGER PULSE

APPLICATION INFORMATION

MONOSTABLE OPERATION

TIME DELAY VS R_A, R_B AND C

In this mode of operation, the timer functions as a one-shot. Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative trigger pulse to pin 2, the flip-flop is set which releases the short circuit across the external capacitor and drives the output high. The voltage across the capacitor, now, increases exponentially with the time constant τ R_AC. When the voltage across the capacitor equals 2/3 V_{CC}, the comparator resets the flip-flop which in turn discharges the capacitor rapidly and drives the output to its low state.

ASTABLE OPERATION

FREE RUNNING FREQUENCY VS R_A, R_B AND C

The circuit can also be connected so as to trigger itself and free run as a multivibrator. The external capacitor charges through R_A and R_B and discharges through R_B only. Thus the duty cycle may be precisely set by the ratio of these two resistors. In this mode of operation, the capacitor charges and discharges between 1/3 V_{CC} and 2/3 V_{CC}. As in the triggered mode, the charge and discharge times, and therefore the frequency are independent of the supply voltage.

The frequency of oscillation is given by: $f = \frac{1}{T} = \frac{1.46}{(R_A + 2R_B)\,C}$

PIN CONFIGURATIONS

8-PIN DIP

14-PIN HERMETIC DIP

TO-99

6

INTERSIL

556
Dual Precision Timer

FEATURES
- Timing from Microseconds to Hours
- Replaces Two 555 Timers
- Operates in Both Astable, Monostable, Time Delay Modes
- High Output Current
- Adjustable Duty Cycle
- TTL Compatible
- Temperature Stability of 0.005% per °C

APPLICATIONS
- Precision Timing
- Sequential Timing
- Pulse Shaping
- Pulse Generator
- Missing Pulse Detector
- Tone Burst Generator
- Pulse Width Modulation
- Time Delay Generator
- Frequency Division
- Industrial Controls
- Pulse Position Modulation
- Appliance Timing
- Traffic Light Control
- Touch Tone Encoder

GENERAL DESCRIPTION
The NE/SE556 Dual Monolithic timing circuit is a highly stable controller capable of producing accurate time delays or oscillation. The 556 is a dual 555. Timing is provided by an external resistor and capacitor for each timing function. The two timers operate independently of each other sharing only V_{CC} and ground. The circuits may be triggered and reset on falling waveforms. The output structures may sink or source 150mA.

ABSOLUTE MAXIMUM RATINGS
Supply Voltage ..... +18V
Power Dissipation 800mW
Operating Temperature Range NE556 ..... 0°C to +70°C
SE556 .. -55°C to +125°C
SE556C . -55°C to +125°C
Storage Temperature Range ..... -65°C to +150°C
Lead Temperature (Soldering, 60 sec) ..... +300°C
*Derate linearly at 6.5mV/°C above ambient temperature of 75°C.

Power Dissipation*

BLOCK DIAGRAM

PIN CONFIGURATION

ORDER NO.: SE556A, NE556A

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: $T_A = 25°C$, $V_{CC} = +5V$ to $+15$ unless otherwise specified

PARAMETER	TEST CONDITIONS	SE556 MIN	SE556 TYP	SE556 MAX	NE556 MIN	NE556 TYP	NE556 MAX	UNITS
Supply Voltage		4.5		18	4.5		16	V
Supply Current (each device)	$V_{CC} = 5V$ $R_L = \infty$		3	5		3	6	mA
	$V_{CC} = 15V$ $R_L = \infty$ Low State, Note 1		10	11		10	14	
Timing Error (Monostable) Initial Accuracy	$R_A = 2K\Omega$ to $100K\Omega$ $C = 0.1\mu F$ Note 2		0.5	1.5		0.75		%
Drift with Temperature			30	100		50		ppm/°C
Drift with Supply Voltage			0.05	0.2		0.1		%/Volt
Timing Error (Astable) Initial Accuracy	R_A, $R_B = 2K\Omega$ to $100K\Omega$ $C = 0.1\mu F$ Note 2		1.5			2.25		%
Drift with Temperature			90			150		ppm/°C
Drift with Supply Voltage			0.15			0.3		%/Volt
Threshold Voltage			2/3			2/3		X V_{CC}
Threshold Current	Note 3		30	100		30	100	nA
Trigger Voltage	$V_{CC} = 15V$	4.8	5	5.2		5		V
	$V_{CC} = 5V$	1.45	1.67	1.9		1.67		
Trigger Current			0.5			0.5		μA
Reset Voltage		0.4	0.7	1.0	0.4	0.7	1.0	V
Reset Current			0.1			0.1		mA
Control Voltage Level	$V_{CC} = 15V$	9.6	10	10.4	9.0	10	11	V
	$V_{CC} = 5V$	2.9	3.33	3.8	2.6	3.33	4	
Output Voltage (low)	$V_{CC} = 15V$							
	$I_{SINK} = 10mA$		0.1	0.15		0.1	.25	
	$I_{SINK} = 50mA$		0.4	0.5		0.4	.75	
	$I_{SINK} = 100mA$		2.0	2.25		2.0	2.75	
	$I_{SINK} = 200mA$		2.5			2.5		
	$V_{CC} = 5V$							
	$I_{SINK} = 8mA$		0.1	0.25				
	$I_{SINK} = 5mA$					.25	.35	
Output Voltage (high)	$I_{SOURCE} = 200mA$		12.5			12.5		
	$V_{CC} = 15V$							
	$I_{SOURCE} = 100mA$							
	$V_{CC} = 15V$	13.0	13.3		12.75	13.3		
	$V_{CC} = 5V$	3.0	3.3		2.75	3.3		
Rise Time of Output			100			100		nsec
Fall Time of Output			100			100		
Discharge Leakage Current			20	100		20	100	nA
Matching Characteristics (Note 4) Initial Timing Accuracy			0.05	0.1		0.1	0.2	%
Timing Drift with Temperature			±10			±10		ppm/°C
Drift with Supply Voltage			0.1	0.2		0.2	0.5	%/Volt

NOTES:
1. Supply current when output is high is typically 1.0mA less.
2. Tested at $V_{CC} = 5V$ and $V_{CC} = 15V$.
3. This will determine the maximum value of $R_A + R_B$ for 15V operation. The maximum total R = 20 meg-ohms.
4. Matching characteristics refer to the difference between performance characteristics of each timer section.

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INTERSIL

ICM7045 Complementary MOS Precision Timer

FEATURES

- **Versatility of applications: precision timer, 4 stopwatch modes, 24-hour clock**
- **Simple to use:**
  - **4 controls stopwatch timer:** 1. Function 2. Start/Stop 3. Reset 4. Display
  - **24-hour clock:** 5. Rapid Minute Advance 6. Rapid Hour Advance
- **Total integration: includes oscillator, divider, decoder driver on chip**
- **Wide operating supply range: 2.5V ≤ V_{DD} ≤ 4.5V**
- **Low operating power consumption: display off typ. 0.9 mW at 3.6V supply**
- **High precision-high frequency operation: quartz crystal oscillator @ 6.5536 MHz**
- **High output current drive: 15 mA peak current per segment, with 12.5% duty cycle**
- **Leading zero suppression: timer stopwatch applications**
- **Fractional second suppression: 24-hour clock application**
- **Short duration short circuit protection on all inputs and outputs at 3.6V supply (Note 2)**
- **All terminals protected against static charges: no special handling precautions required**
- **Wide operating temperature range: −20°C to +70°C**

GENERAL DESCRIPTION

The ICM7045 is a fully integrated digital timer/stopwatch/24-hour clock circuit made using Intersil's low voltage metal gate C-MOS technology. The oscillator, frequency divider, multiplexer, decoder, segment and digit output buffers are all included on chip. The circuit is designed to interface directly with a fully multiplexed seven segment/eight digit common cathode LED display. The nominal supply voltage is 3.6V, equivalent to a stack of three nickel cadmium rechargeable batteries. The only external components required for a complete stopwatch in addition to the display and the batteries are a 6.5536 MHz quartz crystal, a trimming capacitor and four switches.

The circuit takes the oscillator frequency and divides it in sixteen binary stages to a frequency of 100 Hz. Some of these divider outputs are used to generate the multiplex waveforms at a 12.5% duty cycle/800 Hz rate. The 100 Hz signal is then processed in the counters which feed into latches which in turn are multiplexed into the decoder. The counter section spans the range of 1/100 sec. to 24 hours, which can be simultaneously displayed on the eight digits available. The digit drivers (cathodes) are connected to the multiplex lines through zero supression logic, while the segment drivers (anodes) are directly connected to the decoder outputs.

BLOCK DIAGRAM

ZENER DIODE HAS TYPICAL BREAKDOWN VOLTAGE OF 6.5V

PIN CONFIGURATION

TOP VIEW

ORDERING INFORMATION

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ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Notes 1 and 2) 1W
Supply Voltage (V_{DD}-V_{SS}) ..... +5.5V
Input Voltage ..... Equal to, but never in excess of the supply voltages
Output Voltage ..... Equal to, but never in excess of the supply voltages
Storage Temperature ..... −55°C to +125°C
Operating Temperature ..... −20°C to +70°C

NOTE: Absolute maximum ratings define parameter limits that if exceeded may permanently damage or change the device.

TYPICAL OPERATING CHARACTERISTICS

TEST CONDITIONS: $|V_{DD}| - |V_{SS}| = 3.6V$, $T_A = 25°C$, $f_{osc} = 6.5536MHz$, test circuit 1 unless otherwise stated.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I_{DD}	Display Off		180	2000	μA
Instantaneous Supply Current	I_{DD}	7 Segments 1.8V Dropped Across Display	70	105		mA
Instantaneous Supply Current	I_{DD}	2 Segments Lit 1.8V Dropped Across Display	28	42		mA
Operating Voltage	V_{DD}	$-20°C < T_A < 70°C$	2.5		4.5	V
Segment Current Drive		7 Segments Lit, 1.8V Dropped Across Display, 12.5% Duty Cycle				
Instantaneous	I_{SEG}		10	15		mA
Average	I_{SEG}		1.25	1.875		mA
Segment Current Drive		2 Segments Lit, 1.8V Dropped Across Display, 12.5% Duty Cycle				
Instantaneous	I_{SEG}		14	21		mA
Average	I_{SEG}		1.75	2.625		mA
Min. Switch Actuation Current Any Switch	I_{SW}		50			μA
Digit Driver Leakage Current	I_{LD}				200	μA
Segment Driver Leakage Current	I_{LS}				200	μA
Typical Oscillator Stability	f_{STAB}	$3V \le V_{DD} \le 4V$, $C_{TUNING} = 15$ pF		1.0		ppm
Max Time for Oscillator to Start	t	$V_{DD} = 3.6V$			0.1	sec
		$V_{DD} = 2.5V$			1.0	sec
Oscillator Input Capacitance	C_{IN}			17		pF

NOTE 1: This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.

NOTE 2: Short Circuit and High Output Drive Considerations:

The ICM7045 has been designed such that the maximum digit output drive current will not exceed 150 mA when used with any conventional LED displays and a fully charged stack of three nickel cadmium cells. If the 150 mA is exceeded for any extended duration of time, damage may result to the device.

It is, therefore, recommended that if the ICM7045 is to be used under conditions where the digit output drive could exceed 150 mA - high voltage operation at 5V for example - that additional external current limiting resistors be included in series with the LED display (segment lines).

If the digit outputs are short circuited to the positive supply (3.6V) the short circuit current will be approximately 300 mA. This will not damage the device momentarily. Unless this short circuit condition is immediately removed probable device failure will occur from extended time periods of short circuit operation.

Consult the factory if questions arise on your output drive requirements.

TYPICAL OPERATING CHARACTERISTICS

OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE

PEAK SEGMENT CURRENT DRIVE AS A FUNCTION OF DISPLAY VOLTAGE DROP

PEAK SEGMENT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

TEST CIRCUIT 1: FOUR STOPWATCH MODES

Quartz Crystal Parameters
f = 6.5536 MHz (parallel mode frequency)
R_S = 40 Ohms (series resistance)
C_1 = 15 mpF (motional capacitance)
C_0 = 3.5 pF (static package capacitance)

NOTE: Specify quartz crystal to have nominal frequency value when tuned by a total parallel capacitance value of 12 pF or less.
N.O. = Normally Open
N.C. = Normally Closed

FUNCTIONAL OPERATION

STOPWATCH/TIMER OPERATION

The control inputs used in the complete stopwatch application are: (refer to test circuit I for a schematic diagram).

START/STOP	RESET	SPLIT
DISPLAY	STANDARD	RALLY

START/STOP and DISPLAY are designed for connection to single pole double throw switches to insure operation free of contact bounce.

The switch connected to RESET can be a normally open single pole single throw. STANDARD, SPLIT and RALLY are control points with internal pull down resistors to V_{SS}. These are designed to be connected to a rotary function switch which will connect no more than one of these points to V_{DD}. If STANDARD (SPLIT, RALLY) is connected to V_{DD}, the stopwatch is said to be in the STANDARD (SPLIT, RALLY) mode. If all three are left open, the stopwatch is in the SEQUENTIAL mode.

RESET FUNCTION

When the stopwatch is turned on, the RESET will normally be activated. This puts the stopwatch in a ready condition by:

1. Resetting all circuitry
2. Blanking seconds, minutes, hour
3. Showing 00 in the fractional seconds position
4. Turning on the display if it was previously turned off

The display of just two zeros in the fractional seconds positions gives the complete assurance that the stopwatch is "ready to go."

STANDARD MODE

In the STANDARD mode, after a reset has taken place, START/STOP is activated at time t_0. The clock and display are moving simultaneously. A second activation of START/STOP stops the clock and holds the display at time t_{TOTAL}. This completes an event. For timing a second event there are two options. One is to activate START/STOP at the start of the second event. This will momentarily reset the counter and display so that the timing of the second event proceeds from zero. Another activation of START/STOP stops the counter and display at time t_{TOTAL} to end the second event. The other option is to activate RESET after the first event is over. Then the second event proceeds similarly to the first event. As is clear from this description, RESET can be used at any time to reset the stopwatch, including when a timing is in progress. The DISPLAY input can be activated to turn the display off and on. If the display is off when RESET is activated, it will reset and turn on. Turning off the display for timing long events will result in a very substantial power saving.

*Term momentarily means - that a reset pulse is applied to the circuit during a time interval which is negligeable compared to the resolution of the stopwatch, i.e. 0.01 seconds.

SEQUENTIAL MODE

The sequential mode of the stopwatch is designed for timing events consisting of more than one leg (such as relays, multilap races, etc.). After the initial reset the START/STOP is activated at t_0 to start the event. A second activation of START/STOP at time t_1 stops the display to allow t_1 to be read out, while the clock resets and starts counting again instantaneously. At time t_2 an activation of START/STOP enters t_2 (the time of leg no. 2) into the display. This sequence can continue indefinitely. Assuming the total event has N legs, the total elapsed time is then equal to the sum of the N times read out:

$$t_{TOTAL} = t_1 + t_2 \ldots + t_N$$

If it is desired to see the moving clock after a time has been recorded, the DISPLAY switch can be activated to release the display hold and catch up with the moving clock. The display cannot be turned off in the sequential mode. Reset can be activated at any time to reset clock and display.

SPLIT MODE

The split mode is another mode for timing multileg events. In contrast to the sequential mode, the timing in the split mode is cumulative. From a reset condition, the START/STOP switch is activated to t_0 to start the counter and display running. A second activation at t_1 stops the display so t_1 can be read out while the counter continues timing. A third activation at t_2 advances the display with the total elapsed time from t_0 to t_2 showing. Finally, at time t_N the total elapsed time of the event is entered in the display. The time of one leg of the event can be obtained by subtraction. The display can be synchronized to the counter (catch-up function) at any time by activating the display switch. To reset the timer, activate reset. The display cannot be turned off in the SPLIT mode.

RALLY MODE

The rally mode is designed for timing of events with interruptions. Consider an N leg event where the legs may be separated by intervals which should not be timed. The rally mode starts with a RESET. At time t_0 the stopwatch is started by activating START/STOP. After this point the RESET function is disabled to prevent accidental resets during long timing intervals. At time t_1 a START/STOP pulse stops counter and display. From here on each leg time is added to the total by a START/STOP pulse at the beginning of the leg and at the end. The individual leg times are determined by subtraction. The display can be turned on and off with the display switch.

CLOCK OPERATION

The control inputs used in a possible 24-hour clock configuration are (refer to test circuit no. 2):

START/STOP
MINUTES ADVANCE
HOURS ADVANCE
RALLY

START/STOP, MINUTES ADVANCE and HOURS ADVANCE are designed for connection to single pole double throw switches; this assures contact bounce elimination on these inputs. To avoid an additional switch for the DISPLAY input, the RALLY input should be connected to V_{DD} through a 20k resistor and to V_{SS} through a 0.01μF capacitor. These components insure that the display is on when power is applied to the circuit. The most convenient setting procedure is:

1. If clock is not running when power is applied activate START/STOP switch
2. Depress MINUTES ADVANCE switch to obtain correct minutes setting, one minute count per activation.
3. Depress HOURS ADVANCE switch to obtain correct HOURS setting, one hour count per activation.

It is possible to set the clock more accurately or to correct small time errors by using START/STOP in combination with MINUTES ADVANCE. If the clock is, for instance, 20 seconds slow, activate the MINUTES ADVANCE once, then activate the START/STOP, wait 40 seconds and activate the START/STOP again. If the clock is 20 seconds fast, the START/STOP switch should be activated to stop the clock, then after 20 seconds activated again to restart the clock. Other clock configurations are possible (see Application Notes).

TEST CIRCUIT NO. 2: CLOCK MODE

N.C. = NORMALLY CLOSED

APPLICATION NOTES

The ICM7045 has been designed with versatility of applications in the digital timer/stopwatch/24-hour clock field as the major objective. The simplicity of operating modes designed for an extremely practical, easy to use stopwatch, at the same time allow the design of a variety of simpler elapse timer, stopwatch and clock circuits; a few of these will be shown and discussed briefly here:

TIMER CIRCUIT I

This simple circuit (display connections not shown) allows interval timing up to 24 hours with a resolution of 0.01 seconds. Each interval is timed by one start and one stop pulse on the start/stop line. The start pulse for the next interval to be timed automatically resets the timer. Leading zero suppression is automatic.

TIMER CIRCUIT II

This circuit allows interval timing with a single pulse on the start/stop line. Each pulse enters the time elapsed since the previous pulse into the display, resets the timer and starts the timer for the next interval.

TIMER CIRCUIT II

This circuit allows cumulative timing of intervals. Each interval is timed by one start and one stop pulse on the start/stop line. Each subsequent interval timed adds to the total line displayed. The reset switch allows the timer to be reset to zero to start another sequence of intervals. Note that the time between the end of one interval and the start of the reset is not recorded or added to the total.

CLOCK CIRCUIT I

The standard clock circuit is shown and described in the general description. The clock accuracy with a stable voltage supply will depend mostly on the temperature and aging characteristics of the crystal.

The power supply can be modified to give battery standby power.

The standby circuit should be designed to provide the specified minimum voltage to the ICM7045.

OTHER CLOCK CIRCUITS

The basic clock circuit can be modified for various special applications. If it is desired to turn the display on and off, then connect the display input to an additional SPDT switch, while omitting the capacitor/resistor combination on the STANDARD input.

This input can then be wired directly to V_{DD}. This 24-hour clock version might be applicable to vehicles, boats, etc. where a battery is available to supply the display off clock current, while the display can be turned on with the ignition.

APPLICATION NOTES (con't)

Another possible configuration would connect a special circuit to the DISPLAY input which generates a double pulse about 3 seconds apart:

This means depressing the switch will turn on the clock's display for 3 seconds. This allows design of a battery operated "on demand" digital 24-hour clock.

OSCILLATOR CONSIDERATIONS

The oscillator is a high gain complementary MOS inverter with on-chip feedback resistors and an on-chip fixed input capacitor of 17 pF. For the 6.5536 MHz crystal needed for normal timing, it is suggested that the nominal load capacitance be kept under 12 pF, to keep total loading on the oscillator to a reasonable level. The actual trimmer range and the nominal load capacitance needed will have to be determined from the total stray capacitance of the particular circuit (including ICM7045 with package, PC board, etc.) and the tuning tolerance of the chosen crystal.

The series resistance of the crystal should also be kept to a low value (typically less than 50 ohms) to achieve adequate low voltage operation.

Tuning of the oscillator can be most easily performed using a pull-up resistor of 10K ohms on the fractional seconds digit, using period average tune for 1.25mS (800Hz).

STOPWATCH EXTERNAL SYNC CIRCUIT

If the stopwatch is connected as shown in test circuit 1, a few additional components will allow external synchronization of the stopwatch in any mode:

NOTE: Be sure to minimize the distance between the transistor and the ICM7045 to prevent noise from being generated along this connection, which could damage the device. Refer to Absolute Maximum Ratings, page 2 (Input Ratings). Noise spikes absolutely must not exceed the supply voltages.

The external sync signal source has to supply a positive pulse to active the START/STOP input. The minimum voltage of this pulse is about 1.2V in the circuit as shown, but the triggering level can be changed by modifying the input resistor ratio. The output impedance of the external sync signal source should be no greater than 4k ohms.

CHIP TOPOGRAPHY

PACKAGE DIMENSIONS

NOTE: Dimensions in inches (mm)

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INTERSIL

ICM7045A Complementary MOS Precision Decade Timer

FEATURES

- May Be Used to Count
  - —Seconds (1.31072 MHz osc.)
  - —Minutes (2.184533 MHz osc.)
  - —Hours (3.640889 MHz osc.)
- Total Integration—Includes Oscillator, Divider, Decoder Drivers On Chip
- Wide Operating Supply Voltage Range 2.5V ≤ V+ — V− ≤ 4.5V
- Low Operating Power Consumption — Display Off 7.2mW Maximum at 3.6V Supply
- High Output Current Drive — 18mA Peak Segment Current With 12.5% Duty Cycle
- Leading Zero Suppression
- All Terminals Protected Against Static Charge — No Special Handling Precautions Required
- Wide Operating Temperature Range −20° C to +70° C

GENERAL DESCRIPTION

The ICM7045A is a standard device derived from the ICM7045 generic C-MOS timer family and is intended to be used as a decimal timer. As such, either seconds, minutes or hours may be counted by the choice of suitable oscillator frequencies. The ICM7045A is designed to be operated with a nominal supply voltage of 3.6 volts, equivalent to a stack of three nickel cadmium rechargeable batteries and may drive many LED displays directly.

Specifically, the ICM7045A differs from the ICM7045 in that a) the two divide by sixty's used for counting seconds and minutes are replaced by four decade dividers; b) the least significant digit is not available (terminal #21 open circuit); c) the division ratio between the oscillator and the least available digit is $\div 2^{17}$ for the ICM7045A.

Refer to the ICM7045 data sheet for more complete information.

BLOCK DIAGRAM

ZENER DIODE HAS TYPICAL BREAKDOWN VOLTAGE OF 6.5V

ORDERING INFORMATION

PART NO.	TEMPERATURE RANGE	OPERATING VOLTAGE RANGE	PACKAGE
ICM7045A	-20°C to +70°C	$2.5V \leq V_{DD} \leq 4.5V$	Plastic DIP
Order Devices by Following Part Number—ICM7045A IPI			

CONNECTION DIAGRAM

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TYPICAL OPERATING CHARACTERISTICS

OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE

APPLICATION NOTES

The ICM7045A will count to a total of 2399999. The next count will show 0000000. On application of RESET the display will show 0 on the least significant digit; all other digits will be blanked. Leading zero suppression blanking is performed on pairs of digits. For example, 9 will show as 9, 10 will show as 010, 999 will show as 999, 1000 will show as 010000 and so forth.

The oscillator frequency *alone* determines whether the timer is to be used for second, minute or hour counting.

'SECONDS' TIMER Use a 1.31071MHz quartz crystal

DIGIT #	1	2	3	4	5	6	7
	100K Secs	10K Secs	1K Secs	100 Secs	10 Secs	Secs	Sec ÷ 10

'MINUTES' TIMER Use a 2.184533MHz quartz crystal

DIGIT #	1	2	3	4	5	6	7
	1K Mins	100 Mins	10 Mins	Mins	Min ÷ 10	Min ÷ 100	Min ÷ 1000

'HOURS' TIMER Use a 3.640889MHz quartz crystal

DIGIT #	1	2	3	4	5	6	7
	10 Hrs	Hrs	Hrs ÷ 10	Hrs ÷ 100	Hrs ÷ 1,000	Hrs ÷ 10,000	Hrs ÷ 100,000

OSCILLATOR CONSIDERATIONS

The oscillator on the ICM7045A is identical to that of the ICM7045 which was optimized for 6.55MHz operation. For 6.55MHz operation using an on chip input capacitance of 22pF and a nominal off chip output capacitor of 20pF resulted in excellent frequency stability with respect to supply voltage and a wide operating supply voltage range.

Using similar value tuning capacitances with the lower frequency crystals (1.310772MHz, 2.184533MHz and 3.64089MHz) the stability of the oscillator is significantly degraded. It is therefore recommended that the tuning capacitances be increased to a nominal total of 40pF at both the oscillator input and output. Since there is an on chip input capacitance of 20-22pF the additional external input capacitance should be approximately 20pF.

The ICM7045A is guaranteed to operate over the supply voltage range of 2.5 to 4.5V using nominal input and output tuning capacitances of 40pF and with crystals having the following characteristics:

f = 1.310772MHz or
2.184533MHz or
3.64089MHz

$R_S \leq 100\Omega$ (150Ω for 1.310772MHz

$C_M \rightarrow$ 10-20mpF

$C_O \leq 6$pF

$C_L = 20$pF (parallel resonance mode)

ABSOLUTE MAXIMUM RATINGS

—as per ICM7045 data sheet

Typical Operating Characteristics Test Circuit 1 as per ICM7045 data sheet except for oscillator data and absence of 8th digit.

Functional Operation Application Note as per ICM7045 data sheet.

PACKAGE DIMENSIONS

Pin 1 is identified by cutout pattern at end of package

6

INTERSIL

ICM7208
CMOS 7 Decade Counter

FEATURES

- Low operating power dissipation < 10mW
- Low quiescent power dissipation < 5mW
- Counts and displays 7 decades
- Wide operating supply voltage range
  $2V \leq |V+ - V-| \leq 6V$
- Drives directly 7 decade multiplexed common cathode LED display
- Internal store capability
- Internal inhibit to counter input
- Test speedup point
- All terminals protected against static discharge

DESCRIPTION

The ICM7208 is a fully integrated seven decade counter-decoder-driver and is manufactured using the Intersil low voltage metal gate C-MOS process. As such it has applications as either a unit, a frequency or period counter. For unit counter applications the only additional components are a 7 digit common cathode display, 3 resistors and a capacitor to generate the multiplex frequency reference, and the control switches.

Specifically the ICM7208 provides the following on chip functions: a 7 decade counter, multiplexer, 7 segment decoder, digit & segment drivers, plus additional logic for display blanking, reset, input inhibit, and display on/off.

The ICM7208 is intended to operate over a supply voltage of 2 to 6 volts as a medium speed counter or over a more restricted voltage range for high frequency applications.

As a frequency counter it is recommended that the ICM7208 be used in conjunction with the ICM7207 Oscillator Controller which provides a stable HF oscillator, and output signal gating.

CHIP TOPOGRAPHY

Chip may be die attached using conventional eutectic or epoxy procedures. Wire bonding may be either aluminum ultrasonic or gold compression.

CONNECTION DIAGRAM

ORDERING INFORMATION

Order Devices by following Part Number: -ICM 7208 IPI
Order Dice by following Part Number: – ICM7208D

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ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 1 watt
Supply voltage |V+ - V−| (Note 2) 6V
Output digit drive current (Note 3) 150mA
Output segment drive current ..... 30 mA
Input voltage range (any input terminal) ..... Not to exceed the supply voltage
Operating temperature range ..... −20°C to +70°C
Storage temperature range ..... −55°C to +125°C

NOTE: Absolute maximum rating define parameter limits that if exceeded may permanently damage the device.

TYPICAL OPERATION CHARACTERISTICS

TEST CONDITIONS: $V_{DD} - V_{SS} = 5V$, $T_A = 25°C$, TEST CIRCUIT, display off, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Quiescent Current	I_{+1}	All controls plus terminal 19 connected to V+. No multiplex oscillator		30	100	μA
Quiescent Current	I_{+2}	All control inputs plus terminal 19 connected to V+ except store which is connected to V−.		70	150	μA
Operating Supply Current	I_{+S}	All inputs connected to V+, RC multiplexer osc operating $f_{in} < 25KHz$		210	500	μA
Operating Supply Current		$f_{in} = 2MHz$			700	μA
Supply Voltage Range	V+	$f_{in} \leq 2MHz$	3.5		5.5	V
Digit Driver On Resistance	R_D			4	12	ohm
Digit Driver Leakage Current	I_D				500	μA
Segment Driver On Resistance	R_S			40		ohm
Segment Driver Leakage Current	I_S				500	μA
Pullup Resistance of Reset or Store Inputs	R_P		100	400		Kohms
Counter Input Resistance	R_{IN}	Terminal 12 either at V+ or V− potentials			100	Kohms
Counter Input Hysteresis Voltage	V_{HIN}			25	50	mV

NOTE 1: This value of power dissipation refers to that of the package and will not be obtained under normal operating conditions.
NOTE 2: The supply voltage must be applied before or at the same time as any input voltage. This poses no problems with a single power supply system. If a multiple power supply system is used, it is mandatory that the supply for the ICM7208 is not switched on after the other supplies otherwise the device may be permanently damaged.
NOTE 3: The output digit drive current must be limited to 150mA or less under steady state conditions. (Short term transients up to 250mA will not damage the device.) Therefore, depending upon the LED display and the supply voltage to be used it may be necessary to include additional segment series resistors to limit the digit currents.

TEST CIRCUIT

TEST PROCEDURES

The ICM7208 is provided with three input terminals 7, 23, 27 which may be used to accelerate testing. The least two significant decade counters may be tested by applying an input to the 'COUNTER INPUT' terminal 12. 'TEST POINT' terminal 23 provides an input which bypasses the 2 least significant decade counters and permits an injection of a signal into the third decade counter. Similarly terminals 7 and 27 permit rapid counter advancing at two points further along the string of decade counters.

CONTROL INPUT DEFINITIONS

INPUT	TERMINAL	VOLTAGE	FUNCTION
1. DISPLAY	9	V+	DISPLAY ON
		V-	DISPLAY OFF
2. STORE	11	V+	COUNTER INFORMATION STORED
		V-	COUNTER INFORMATION INFORMATION TRANSFERRING
3. INHIBIT	13	V+	INPUT TO COUNTER BLOCKED
		V-	NORMAL OPERATION
4. RESET	14	V+	NORMAL OPERATION
		V-	COUNTERS RESET

COUNTER INPUT DEFINITION

The internal counters of the ICM7208 index on the negative edge of the input signal at terminal #12.

TYPICAL PERFORMANCE CHARACTERISTICS

MAXIMUM COUNTER INPUT FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

SEGMENT OUTPUT CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

SUPPLY CURRENT AS A FUNCTION OF COUNTER INPUT FREQUENCY

APPLICATION NOTES

GENERAL

1. Format of Signal to be Counted

The noise immunity of the Signal Input Terminal is approximately 1/3 the supply voltage. Consequently, the input signal should be at least 50% of the supply in peak to peak amplitude and preferably equal to the supply. **NOTE: The amplitude of the input signal should not exceed the supply; otherwise, damage may be done to the circuit.**

The optimum input signal is a 50% duty cycle square wave equal in amplitude to the supply. However, as long as the rate of change of voltage is not less than approximately 10^{-4}V/μsec at 50% of the powr supply voltage, the input waveshape can be sinusoidal, triangular, etc.

2. Display Considerations

Any common cathode multiplexable LED display may be used. However, if the peak digit currents exceed 150ma for any prolonged time, it is recommended that resistors be included in series with the segment outputs (terminals 2, 3, 15, 17, 18, 26, 28) to limit current to 150mA. The ICM7208 is specified with 500μA of possible digit leakage current. With certain new LED displays that are extremely efficient at low currents, it may be necessary to include resistors between the cathode outputs and the positive supply V+ to bleed off this leakage current.

3. Display Multiplex Rate

The multiplex frequency reference is divided by eight to generate an 8 bit sequencer. Thus the display multiplex rate is one eighth of the multiplex frequency reference.

The ICM7208 has approximately 0.5μS overlap between output drive signals. Therefore, if the multiplex rate is very fast, digit ghosting will occur. The ghosting determines the upper limit for the multiplex frequency reference. At very low multiplex rates flicker becomes visible.

It is recommended that the display multiplex rate be within the range of 50Hz to 200Hz which corresponds to 400Hz to 1600Hz for the multiplex frequency reference.

4. Unit Counter

The unit counter updates the display for each negative transition of the input signal. The information on the display will count after reset from 00 to 9,999,999 and then will reset to 0000000 and will begin to count up again. To blank leading zeros actuate reset at the beginning of a count. Leading zero blanking affects two digits at a time.

For battery operated systems the display may be switched off to conserve power.

An external generator may be used to provide the multiplex frequency reference (input terminal 19). The signal applied to terminal 19 (terminals 16 and 20 open circuit) should be approximately equal to the supply voltage and for minimum power dissipation should be a square wave.

For stand alone systems two inverters are provided so that a simple but stable RC oscillator may be built using only 2 resistors and a capacitor.

Figure 1 shows the schematic of an extremely simple unit counter that can be used for remote traffic counting, to name one application. The power cell stack should consist of 3 or 4 nickel cadmium rechargeable cells (nominal 3.6 or 4.8 volts). If 4 x 1.5 volt cells are used it is recommended that a diode be placed in series with the stack to guarantee that the supply voltage does not exceed 6 volts.

The input switch is shown to be a single pole double throw switch (SPDT). A single pole single throw switch (SPST) could also be used with a pullup resistor. However, anti-bounce circuitry must be included in series with the counter input. In order to avoid all contact bounce problems due to the SPDT switch the ICM7208 contains an input latch on chip.

FIGURE 1: Schematic Unit Counter

5. Frequency Counter

The ICM7208 may be used as a frequency counter when used with an external frequency reference and gating logic. This can be achieved using the ICM7207 Oscillator Controller (Figure 2). The ICM7207 provides the store and reset pulses together with the counting window, and are generated from a crystal controlled oscillator. Figure 3 shows the recommended input gating waveforms to the ICM7208. At the end of a counting period (50% duty cycle) the counter input is inhibited. The counter information is then transferred and stored in latches and can be displayed. Immediately after this information is stored, the counters are cleared and are ready to start a new count when the counter input is enabled.

Using a 6,553,600Hz quartz crystal and the ICM7207 driving the ICM7208 two ranges of counting may be obtained using either 0.01 sec or 0.1 sec counter enable windows.

Previous comments on leading zero blanking, etc., apply as per the unit counter.

The ICM7207 provides the multiplex frequency reference of 1.6KHz.

FIGURE 2: Frequency Counter

Note: For a 1 sec count window which allows all 7 digits to be used with a resolution of 1Hz, the ICM7207 can be replaced with the ICM7207A. Circuit details are given on the 7207A data sheet.

FIGURE 3: Frequency Counter Input Waveforms

6. Period Counter

For this application, as opposed to the frequency counter, the gating and the input signal to be measured are reversed to the frequency counter. The input period is multiplied by two to produce a single polarity signal (50% duty cycle) equal to the input period, which is used to gate into the counter the frequency reference (1MHz in this case). Figure 5 shows a block schematic of the input waveform generator. The 1MHz frequency reference is generated by the ICM7209 Clock Geneator using an 8MHz oscillator frequency and internally dividing this frequency by 8. Alternatively, a 1MHz signal could be applied directly to the 'COUNTER INPUT'. Waveforms are shown in Figure 4.

FIGURE 4: Period Counter Input Waveforms

FIGURE 5: Period Counter Input Generator

BLOCK DIAGRAM

PACKAGE DIMENSIONS

NOTE: Dimensions in inches (mm)

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INTERSIL

ICM7215
Complementary MOS LED Stopwatch Circuit

FEATURES

- **Total integration: oscillator, divider, decoder, segment and digit drivers on chip**
- **Four functions: start/stop/reset, split, taylor, time-out**
- **Retrofit to ICM7205 for split and/or taylor applications**
- **Six digit display: ranges up to 59 minutes 59.99 seconds**
- **Requires only three low cost SPST switches without loss of accuracy: start/stop, reset, display unlock**
- **Chip enable pin to turn off both segment and digit outputs; can be used for multiple circuits driving one display**
- **Low battery indicator on chip turns on well above minimum operating voltage**
- **Digit blanking on seconds and minutes to conserve battery life**
- **High LED drive current: 13mA per segment at 16.7% duty cycle with 4.0 volt supply**
- **Wide operating range: 2.0 to 5.0 volts**
- **Oscillator requires only 3.2768MHz crystal and trimming capacitor**
- **1KHz multiplex rate prevents flickering display**
- **Fully protected against static charge, no special handling precautions required**
- **Can be used easily in four different single function stopwatches or two two-function stopwatches: start/stop/reset with time-out, split with taylor. The component count for a three- or four-function stopwatch will be slightly greater.**

GENERAL DESCRIPTION

The ICM7215 is a fully integrated six digit LED stopwatch circuit fabricated with Intersil's low threshold metal gate CMOS process. The circuit interfaces directly with a six digit/seven segment common cathode LED display. The low battery indicator can be connected to the decimal point anode or to a separate LED lamp. The only components required for a complete stopwatch besides the display are: three SPST switches, a 3.2768MHz crystal, a trimming capacitor, three AA batteries and an on-off switch. For a two function stopwatch or for adding a display off feature one additional slide switch would be required. The circuit divides the oscillator frequency by 2^{15} to obtain 100Hz which is fed to the fractional seconds, seconds and minutes counters. An intermediate frequency is used to obtain the 1/6 duty cycle 1.07KHz multiplex waveforms. The blanking logic provides leading zero blanking for seconds and minutes independently of the clock. The ICM7215 is packaged in a 24-lead plastic DIP.

PIN CONFIGURATIONS

ORDERING INFORMATION

Order devices by following part number ICM 7215 I PG

Order dice by following part number ICM 7215 D

CHIP TOPOGRAPHY

DIMENSIONS IN PARENTHESES ARE MM
OTHERS ARE INCHES

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... 5.5 Volts
Power Dissipation (Note 1) ..... 0.75 Watts
Operating Temperature ..... −20°C to +70°C
Storage Temperature ..... −55°C to +125°C
Input and Output Voltage ..... equal to but never exceeding the supply voltage

OPERATING CHARACTERISTICS

TEST CONDITIONS: T_A = +25°C, stopwatch circuit, V_{DD} = 4.0V unless otherwise specified.

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Voltage	−20°C ≤ T_A ≤ +70°C	2.0		5.0	Volts
Supply Current	Display off		0.6	1.5	mA
Segment Current	5 segments lit				mA
Peak	1.8 Volts across display	9.0	13.2		mA
Average			2.2		mA
Switch Actuation Current	All inputs except chip enable		20	50	μA
Switch Actuation Current	Chip enable		50	200	μA
Digit Leakage Current	V_{DIGIT} = 2.0V			50	μA
Segment Leakage Current	$V_{SEGMENT}$ = 2.0V			100	μA
Low Battery Indicator Trigger Voltage		2.2		2.8	Volts
LBI Output Current	V_{DD} = 2.0V, V_{LBI} = 1.6V		2.0		mA
Oscillator Stability	V_{DD} = 2.0V to V_{DD} = 5.0V		6		PPM
Oscillator Transconductance	V_{DD} = 2.0V	120			μmho
Oscillator Input Capacitance			30		pF

NOTE 1: This value of power dissipation refers to the package and will not be obtained under normal conditions. The output devices on the ICM7215 have very low impedance characteristics, especially the digit cathode drivers. If these devices are shorted to a low impedance power supply, the current could be as high as 300mA. This will not damage the device momentarily, but if the short circuit condition is not removed immediately probable device failure will occur.

STOPWATCH CIRCUIT

BLOCK DIAGRAM

TYPICAL PERFORMANCE CHARACTERISTICS

SUPPLY CURRENT VS VOLTAGE

SEGMENT CURRENT VS SUPPLY VOLTAGE

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OSC. STABILITY VS SUPPLY VOLTAGE

LBI TRIGGER VOLTAGE VS TEMPERATURE

FUNCTIONAL OPERATION

Turning on the stopwatch will bring up the reset state where the fractional seconds are on displaying 00 and the other digits are blanked. This display always indicates that the stopwatch is ready to go.

The display can be turned off in any mode by connecting the chip enable input to V_{DD}.

START/STOP/RESET

When the mode input is floating and the display input is floating or connected to V_{DD}, the circuit is in the start/stop/reset mode.

The start/stop/reset mode can be used for single event timing in a one-button stopwatch. An additional reset switch can be used to provide reset at any time capability. The diagram indicates the operation and the results. To time another event the display must be reset before the start of the event.

Seconds will be displayed after one second, minutes after one minute. The range of the stopwatch is 59 minutes 59.99 seconds. If an event exceeds one hour, the number of hours must be remembered by the user. Leading zeroes are not blanked after one hour.

TAYLOR

When the mode input is connected to V_{SS}, the stopwatch is in the taylor or sequential mode.

As depicted graphically above, each split time is measured from zero in the taylor mode, i.e., after stopping the watch, the counters reset to zero momentarily and start counting the next interval. The time displayed is the time elapsed since the last activation of start/stop. The display is stationary after the first interval unless the display unlock is used to show the running clock. Reset can be used at any time.

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SPLIT

When the mode input is connected to V_{DD}, the stopwatch is in the split mode.

The split mode differs from the taylor in that the lap times are cumulative in the split mode. The counters do not reset or stop after the first start until reset is activated. Any time displayed is the cumulative time elapsed since the first start after reset. Display unlock can be used to let the display 'catch up' with the clock. Reset can be used at any time.

TIME OUT

When the mode input is floating and the display input is tied to V_{SS}, the stopwatch is in the time-out mode.

In the time-out mode the clock and display alternately start and stop with activations of the start/stop switch. Reset can be used at any time. The display unlock button is bypassed in this mode.

LOW BATTERY INDICATOR

The on-chip low battery indicator is intended for use with a small LED lamp or the decimal points on a standard LED display. The output is the drain of a p-channel transistor two-thirds the size of the segment drivers. The LBI circuitry is designed to provide a trigger voltage of approximately 2.5 volts at room temperature. With normal AA type batteries the discharge characteristics will provide many hours of accurate timekeeping after the indicator comes on. However, the wide voltage spread between the LBI voltage and minimum operating voltage is required to guarantee low battery indication under worst case conditions.

SWITCH CHARACTERISTICS

The ICM7215 is designed for use with SPST switches throughout. On the display unlock and reset inputs the characteristics of the switches are unimportant, since the circuit responds to a logic level held for any level of time, however short. Switch bounce on these inputs does not need to be specified. The start/stop input, however, responds to an edge and it requires a switch with less than 15msec of switch bounce. The bounce protection circuitry has been specifically designed to let the circuit respond to the first edge of the signal, so as to preserve the full accuracy of the system.

APPLICATION NOTES

OSCILLATOR NOTES

The oscillator of the ICM7215 includes all components on chip except the 3.2768 MHz crystal and the trimming capacitor. The oscillator input capacitance has a nominal value of 30 pf. The circuit is designed to work with a crystal with a load capacitance of approximately 15 pf. If the crystal has characteristics as shown on page 2, an 8-40pf trimming capacitor will be adequate for a tuning tolerance of ±30PPM on the crystal. If the crystal's static capacitance is significantly lower, a narrower trimming range may be selected.

After deciding on a crystal and a nominal load capacitance, take the worst case values of C_{in}, C_{out} and R_S and calculate the g_m required by:

$$g_m = \omega^2 C_{out} R_S \left\{1 + \frac{C_o (C_{in} + C_{out})}{C_{in} C_{out}}\right\}^2$$

C_o = static capacitance
R_S = series resistance
C_{in} = input capacitance
C_{out} = output capacitance
ω = 2π x crystal frequency

The resulting g_m should be less than half the g_m specified for the device. If it is not, a lower value of crystal series resistance and/or load capacitance should be specified.

OSCILLATOR TUNING

To avoid loading the oscillator when tuning, a frequency counter cannot be connected to the oscillator itself. Easy tuning can be accomplished by using the |0th or |00th cathode with the device reset. The frequency on the cathode should be tuned to 1066.667 Hz, which is equivalent to a period of 937.5 microseconds.

TEST POINT

The test point input is used for high speed testing of the device. When the input is pulsed low, a latch is set which speeds up counting by a factor of 32. Also, each pulse on the test point rapid advances both minutes and seconds in a parallel mode. To accurately rapid advance the signal applied to the test point must be free of switch bounce. The circuit is taken out of the test point mode by using either reset or start/stop.

REPLACING THE ICM7205 WITH THE ICM7215

The ICM7215 is designed to be compatible with circuits using the ICM7205. If the 7205 is used only in the split mode no changes are required. If the 7205 is used in the taylor mode and the split/taylor input (pin 21) is left open, a jumper from pin 21 to V_{SS} must be added when converting to the 7215. A jumper may also be needed if the 7205 is used with a split/taylor switch. Once the jumper has been added the board can be used with either device.

CHIP ENABLE

The chip enable input is used to disable both segment and digit drivers without affecting any of the functions of the device. When the chip enable input is floating or connected to V_{SS}, the display is enabled. When the chip enable input is tied to V_{DD} the display is turned off. One example of the many possible uses of this feature is driving one display from two ICM7215 devices, one in the split mode and the other in the taylor mode. The circuit below indicates how the user can obtain lap and cumulative readings of the same event.

ALL OTHER SWITCHES COMMON TO BOTH DEVICES

LATCHUP CONSIDERATIONS

Due to the inherent structure of junction isolated CMOS devices, the circuit can be put in a latchup mode if large currents are injected into device inputs or outputs. For this reason special care should be taken in a system with multiple power supplies to prevent voltages being applied to inputs and/or outputs before power is applied to V_{DD} and V_{SS}. If only inputs are affected latchup can also be prevented by limiting the current into the input terminal to less than 1mA.

PACKAGE DIMENSIONS

DIMENSIONS IN PARENTHESES ARE MM
OTHERS ARE INCHES

NOTE: All dimensions in parentheses are metric.

6

ICM7216A 10 MHz Universal Counter, Drives Common Anode LED's
ICM7216B 10 MHz Universal Counter, Drives Common Cathode LED's
ICM7216C 10 MHz Frequency Counter, Drives Common Anode LED's
ICM7216D 10 MHz Frequency Counter, Drives Common Cathode LED's

FEATURES

ICM7216A AND B

- **Functions as a Frequency Counter, Period Counter, Unit Counter, Frequency Ratio Counter or Time Interval Counter**
- **Four Internal Gate Times:**
  0.01 sec, 0.1 sec, 1 sec, 10 sec in Frequency Counter Mode
- **1 Cycle, 10 Cycles, 100 Cycles, 1000 Cycles in Period, Frequency Ratio and Time Interval Modes**
- **Measures Frequencies from DC to 10 MHz**
- **Measures Period from 0.5μ sec to 10 sec**

ICM7216C AND D

- **Functions as a Frequency Counter. Measures Frequencies from DC to 10 MHz**
- **Decimal Point and Leading Zero Blanking May be Externally Selected**

ALL VERSIONS:

- **Eight Digit Multiplexed LED Outputs**
- **Output Drivers will Directly Drive Both Digits and Segments of Large LED Displays. Both Common Anode and Common Cathode Versions are Available**
- **Single Nominal 5V Supply Required**
- **Stable High Frequency Oscillator, Uses Either 1 MHz or 10 MHz Crystal**
- **Internally Generated Multiplex Timing with Interdigit Blanking, Leading Zero Blanking and Overflow Indication**
- **Decimal Point and Leading Zero Blanking Controlled Directly by the Chip**
- **Display Off Mode Turns Off Display and Puts Chip into Low Power Mode**
- **Hold and $\overline{\text{Reset}}$ Inputs for Additional Flexibility**
- **Test Speedup Function Included**
- **All Terminals Protected Against Static Discharge**

GENERAL DESCRIPTION

The ICM7216A and B are fully integrated Universal Counters with LED display drivers. They combine a high frequency oscillator, a decade timebase counter, an 8 decade data counter and latches, a 7 segment decoder, digit multiplexers and 8 segment and 8 digit drivers which can directly drive large LED displays. The counter inputs have a maximum frequency of 10 MHz in frequency and unit counter modes and 2 MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7216A and B can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or as a totalizing counter. The counter uses either a 10 MHz or 1 MHz quartz crystal timebase. For period and time interval, the 10MHz timebase gives a 0.1 μsec resolution. In period average and time interval average, the resolution can be in the nanosecond range. In the frequency mode, the user can select accumulation times of 0.01 sec, 0.1 sec, 1 sec and 10 sec. With a 10 sec accumulation time, the frequency can be displayed to a resolution of 0.1 Hz in the least significant digit. There is 0.2 seconds between measurements in all ranges.

The ICM7216C and D function as frequency counters only, as described above.

All versions of the ICM7216 incorporate leading zero blanking. Frequency is displayed in KHz. In the ICM7216A and B, time is displayed in μsec. The display is multiplexed at 500Hz with a 12.5% duty cycle for each digit. The ICM7216A and C are designed for common anode display with typical peak segment currents of 25mA. The ICM7216B and D are designed for common cathode displays with typical peak segment currents of 12mA. In the display off mode, both digit drivers and segment drivers are turned off enabling the display to be used for other functions.

ORDERING INFORMATION

Universal Counter for use with Common Anode LED Display:	**ICM 7216 A**	**IJI**
Universal Counter for use with Common Cathode LED Display:	**ICM 7216 B**	**IPI**
Frequency Counter for use with Common Anode LED Display:	**ICM 7216 C**	**IJI**
Frequency Counter for use with Common Cathode LED Display:	**ICM 7216 D**	**IPI**

Type

Package (See Outline Drawing)

Temperature Range -20° C to +70° C

Evaluation Kit:

ICM7226 EV/Kit

PIN CONFIGURATIONS

EVALUATION KIT

The ICM7226 Universal Counter System has all of the features of the ICM7216 plus a number of additional features. The ICM7226 Evaluation Kit consists of the ICM7226AIDL (Common Anode LED Display), a 10 MHz quartz crystal, 8 each 7 segment .3" LED's, P.C. board, resistors, capacitors, diodes, switches, socket: everything needed to quickly assemble a functioning ICM7226 Universal Counter System.

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage ($V^+ - V^-$) ..... 6.5 Volts
Maximum Digit Output Current 400mA
Maximum Segment Output Current 60mA
Voltage On Any Input or
Output Terminal[1] ..... $V^+ + .3V$ to $V^- - .3V$

Maximum Power Dissipation at
70°C ..... 1.0 Watts (ICM7216A & C)
0.5 Watts (ICM7216B & D)

Maximum Operating Temperature
Range ..... −20°C to +70°C

Maximum Storage Temperature
Range ..... −55°C to +125°C

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

Notes:
1. The ICM7216 may be triggered into a destructive latchup mode if either input signals are applied before the power supply is applied or if input or outputs are forced to voltages exceeding V^+ to V^- by more than 0.3 volts.

ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: $V^+ - V^- = 5.0V$, Test Circuit, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
ICM7216A/B						
Operating Supply Current	I_{DD}	Display Off, Unused Inputs to V^-		2	5	mA
Supply Voltage Range		-20°C < T_A < +70°C, Input A, Input B Frequency at F_{MAX}	4.75		6.0	Volts
Maximum Frequency Input A, Pin 28	$F_{A\,MAX}$	-20°C < T_A < +70°C 4.75 < $V^+ - V^-$ < 6.0V, Figure 1, Function = Frequency, Ratio, Unit Counter Function = Period, Time Interval	 10 2.5			 MHz MHz
Maximum Frequency Input B, Pin 2	F_{BMAX}	-20°C < T_A < +70°C 4.75V < $V^+ - V^- \leq$ 6.0V Figure 2	2.5			MHz
Minimum Separation Input A to Input B Time Interval Function		-20°C < T_A < 70°C 4.75V < $V^+ - V^- \leq$ 6.0V Figure 3	250			nsec
Maximum Osc. Freq. and Ext. Osc. Frequency		-20°C < T_A < +70°C 4.75 < $V^+ - V^-$ < 6.0V	10			MHz
Minimum Ext. Osc. Freq.					100	KHz
Oscillator Transconductance	g_m	$V^+ - V^-$ = 4.75V, T_A = +70°C	2000			μmhos
Multiplex Frequency	f_{mux}	f_{osc} = 10MHz		500		Hz
Time Between Measurements		f_{osc} = 10MHz		200		msec
Input Voltages: Pins 2,13,25,27,28 Input Low Voltage Input High Voltage	 V_{IL} V_{IH}	 -20°C < T_A < +70°C	 3.5		 1.0	 Volts Volts
Input Resistance to V^+ Pins 13,24	R	$V_{IN} = V^+ - 1.0V$	100K	400K		ohms
Input Leakage Pin 27,28,2	I_L				20	μA
ICM7216A						
Digit Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Low Output Current	 I_{OH} I_{OL}	 $V_{OUT} = V^+ - 2.0V$ $V_{OUT} = V^- + 1.0V$	 -150	 -180 +0.3		 mA mA
Segment Driver: Pins 4,5,6,7,9,10,11,12 Low Output Current High Output Current	 I_{OL} I_{OH}	 $V_{OUT} = V^- + 1.5V$ $V_{OUT} = V^+ - 2.5V$	 25	 35 -100		 mA μA
Multiplex Inputs: Pins 1,3,14 Input Low Voltage Input High Voltage Input Resistance to V^-	 V_{IL} V_{IH} R	 $V_{IN} = V^- + 1.0V$	 $V^- + 2.0$ 50	 100	 0.8	 Volts Volts KΩ
ICM7216B						
Digit Driver: Pins 4,5,6,7,9,10,11,12 Low Output Current High Output Current	 I_{OL} I_{OH}	 $V_{OUT} = V^- + 1.0V$ $V_{OUT} = V^+ - 2.5V$	 50	 75 -100		 mA μA
Segment Driver: Pins 15,16,17,19,20,21,22,23 High Output Current Leakage Current	 I_{OH} I_L	 $V_{OUT} = V^+ - 2.0V$ $V_{OUT} = V^+ - 2.5V$	 -10		 10	 mA μA
Multiplex Inputs: Pins 1,3,14 Input Low Voltage Input High Voltage Input Resistance to V^+	 V_{IL} V_{IH} R	 $V_{IN} = V^+ - 1.0V$	 $V^+ - 0.8$ 200	 360	 $V^+ - 2.0$	 Volts Volts KΩ

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ELECTRICAL CHARACTERISTICS

TEST CONDITIONS: $V^+ - V^- = 5.0V$, Test Circuit, $T_A = 25°C$, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN.	TYP.	MAX.	UNITS
ICM7216C/D						
Operating Supply Current	I_{DD}	Display Off, Unused Inputs to V^-		2	5	mA
Supply Voltage Range		-20°C < T_A < +70°C, Input A Frequency at F_{MAX}	4.75		6.0	Volts
Maximum Frequency Input A, Pin 28	F_{MAX}	-20°C < T_A < +70°C 4.75 < $V^+ - V^-$ < 6.0V, Figure 1	10			MHz
Maximum Osc. Freq and Ext. Osc. Frequency		-20°C < T_A < +70°C 4.75 < $V^+ - V^-$ < 6.0V	10			MHz
Minimum Ext. Osc. Freq.					100	KHz
Oscillator Transconductance	g_m	$V^+ - V^- = 4.75V$, $T_A = +70°C$	2000			μmhos
Multiplex Frequency	f_{mux}	$f_{osc} = 10MHz$		500		Hz
Time Between Measurements		$f_{osc} = 10MHz$		200		msec
Input Voltages: Pins 12,27,28						
Input Low Voltage	V_{IL}	-20°C < T_A < +70°C			1.0	Volts
Input High Voltage	V_{IH}		3.5			Volts
Input Resistance to V^+ Pins 12,24	R	$V_{IN} = V^+ - 1.0V$	100	400		KΩ
Input Leakage Pin 27, Pin 28	I_L				20	μA
Output Current Pin 2	I_{OL}	$V_{OL} = V^- + .4V$	0.36			mA
	I_{OH}	$V_{OH} = V^+ - .8V$	265			μA
ICM7216C						
Digit Driver: Pins 15,16,17,19,20,21,22,23						
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.0V$	-150	-180		mA
Low Output Current	I_{OL}	$V_{OUT} = 1.0V$		+0.3		mA
Segment Driver: Pins 3,4,5,6,8,9,10,11						
Low Output Current	I_{OL}	$V_{OUT} = V^- + 1.5V$	25	30		mA
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.5V$		-100		μA
Multiplex Inputs: Pins 1,13,14						
Input Low Voltage	V_{IL}				$V^- + 0.8$	Volts
Input High Voltage	V_{IH}		$V^- + 2.0$			Volts
Input Resistance to V^-	R	$V_{IN} = V^- + 1.0V$	50	100		KΩ
ICM7216D						
Digit Driver: Pins 3,4,5,6,8,9,10,11						
Low Output Current	I_{OL}	$V_{OUT} = V^- + 2.0V$	50	75		mA
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.5V$		100		μA
Segment Driver: Pins 15,16,17,19,20,21,22,23						
High Output Current	I_{OH}	$V_{OUT} = V^+ - 2.0V$	10	15		mA
Leakage Current	I_L	$V_{OUT} = V^+ - 2.5V$			10	μA
Multiplex Inputs: Pins 1,13,14						
Input Low Voltage	V_{IL}				$V^+ - 2.0$	Volts
Input High Voltage	V_{IH}		$V^+ - 0.8$			Volts
Input Resistance to V^+		$V_{IN} = V^+ - 1.0V$	200	360		kΩ

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FIGURE 1. Waveform for Guaranteed Minimum FAMAX Function = Frequency, Frequency Ratio, Unit Counter.

FIGURE 2. Waveform for Guaranteed Minimum FBMAX and FAMAX for Function = Period and Time Interval.

TIME INTERVAL MEASUREMENT

The ICM7216/7226 can be used to accurately measure the time interval between two events. With a 10 MHz timebase crystal, the time between the two events can be as long as ten seconds. Accurate resolution in time interval measurement is 100ns.

The feature operates with Channel A going low at the start of the event to be measured, followed by Channel B going low at the end of the event.

FIGURE 3a.

FIGURE 3b. Waveform for Minimum Time Between Transitions of Input A and Input B.

When in the time interval mode and measuring a single event, the ICM7216/7226 must first be "primed" prior to measuring the event of interest. This is done by placing both Channel A and Channel B at V^+, then causing A to toggle to V^- and back to V^+ followed by B toggling to V^- and back to V^+ The input is then ready for measurement.

FIGURE 3c.

This can be easily accomplished with the following circuit: (Figure 3d)

Device	Type
1	CD4049B Inverting Buffer
2	CD4070B Exclusive-OR

FIGURE 3d. Priming Circuit, Signal A&B High or Low.

Following the priming procedure (when in single event or 1 cycle range input) the device is ready to measure one (only) event.

When timing repetitive signals, it is not necessary to "prime" the ICM7216/7226 as the first alternating signal states automatically prime the device.

During any time interval measurement cycle, the ICM7216/7226 requires 200ms following B going low to update all internal logic. A new measurement cycle will not take place until completion of this internal update time.

FIGURE 3e.

NOTES: 1) FUNCTION INPUT AND INPUT B AVAILABLE ON ICM 7216A/B ONLY.
2) EXT D.P. INPUT AND MEASUREMENT IN PROGRESS OUTPUT AVAILABLE ON ICM 7216C/D ONLY.

BLOCK DIAGRAM

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TEST CIRCUIT

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OVERFLOW WILL BE INDICATED ON THE DECIMAL POINT OUTPUT OF DIGIT 7.

LED OVERFLOW INDICATOR CONNECTIONS

	CATHODE	ANODE
ICM 7216A	DEC. PT.	D_7
ICM 7216B	D_7	DEC. PT.
ICM 7216C	DEC. PT.	D_7
ICM 7216D	D_7	DEC. PT.

APPLICATIONS NOTES

GENERAL

Inputs A and B

Inputs A and B are digital inputs with a typical switching threshold of 2.0V at $V^+ = 5.0V$. For optimum performance the peak-to-peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from T2L logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs.

Note: The amplitude of the input should not exceed the supply, otherwise, the circuit may be damaged.

Multiplexed Inputs

The function, range, control and external decimal point inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate digit driver output to the inputs. The input function, range and control inputs must be stable during the last half of each digit output, (typically 125μsec). The multiplex inputs are active high for the common anode ICM7216A and C and active low for the common cathode ICM7216B and D.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the unit counter mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10K resistor should be placed in series with the multiplex inputs as shown in the application notes.

Table 1 shows the functions selected by each digit for these inputs.

Control Input Functions

Display Test — All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be blanked if Display Off is selected at the same time.

Display Off — To enable the Display Off mode it is necessary to input D_3 to the control input and have the HOLD input at V^+. The chip will remain in the Display Off mode until HOLD is switched back to V^-. While in the Display Off mode, the segment and digit driver outputs are open. During Display Off the oscillator continues to run with a typical supply current of 1.5mA with a 10 MHz crystal and no measurements are made. In addition, inputs to the multiplexed inputs will have no effect. A new measurement is initiated when the HOLD input is switched to V^-.

1 MHz Select — The 1 MHz select mode allows use of a 1 MHz crystal with the same digit multiplex rate and time between measurements as with a 10 MHz crystal. The decimal point is also shifted one digit to the right in Period and Time Interval, since the least significant digit will be in μsecond increments rather than 0.1 μsec increments.

External Oscillator Enable — In this mode the external oscillator input is used instead of the on-chip oscillator for Timebase input and Main Counter input in Period and Time interval modes. The on-chip oscillator will continue to function when the external oscillator is selected. The external oscillator input frequency must be greater than 100 KHz or the chip will reset itself to enable the on-chip oscillator.

TABLE 1

	FUNCTION	DIGIT
Function Input Pin 3 (ICM7216A & B Only)	Frequency	D_0
	Period	D_7
	Frequency Ratio	D_1
	Time Interval	D_4
	Unit Counter	D_3
	Oscillator Frequency	D_2
Range Input Pin 14	.01 sec/1 Cycle	D_0
	.1 sec/10 Cycles	D_1
	1 sec/100 Cycles	D_2
	10 sec/1K Cycles	D_3
Control Input Pin 1	Blank Display	D_3 and Hold
	Display Test	D_7
	1 MHz Select	D_1
	External Oscillator	D_0
	Enable	
	External Decimal Point Enable	D_2
	Test	D_4
External Decimal Point Input Pin 13, ICM7216C & D Only	Decimal point is output for same digit that is connected to this input	

External Decimal Point Enable — When external decimal point is enabled a decimal point will be displayed whenever the digit driver connected to the external decimal point is active. Leading Zero Blanking will be disabled for all digits following the decimal point.

Test Mode — In the test mode the main counter is split into groups of two digits each and the groups are clocked in parallel. The reference counter is split such that the clock into the reference count goes directly to the clock of the second decade counter (.1 sec/10 cycle range). The count in the main counter is continuously output.

Range Input — The range input selects whether the measurement is made for 1, 10 , 100, 1000 counts of the reference counter. In all functional modes except Unit Counter a change in the range input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the Range Input is changed.

Function Input — The six functions that can be selected are: Frequency, Period, Time Interval, Unit Counter, Frequency Ratio and Oscillator Frequency. This Input is available on the ICM7216A and B only.

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These functions select which signal is counted into the Main Counter and which signal is counted by the reference counter, as shown in Table 2. In Time Interval, a flip flop is toggled first by a 1-0 transition of Input A and then by a 1-0 transition of Input B. The oscillator is gated into the Main Counter from the time Input A toggles the flip flop until Input B gates the flip flop. A change in the function input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the Function Input is changed.

TABLE 2

DESCRIPTION	MAIN COUNTER	REFERENCE COUNTER
Frequency (F_A)	Input A	100 Hz (Oscillator ÷ 10^5 or 10^4)
Period (T_A)	Oscillator	Input A
Ratio (F_A/F_B)	Input A	Input B
Time Interval (A → B)	Osc•(Time Interval FF)	Time Interval FF
Unit Counter (Count A)	Input A	Not Applicable
Osc. Freq. (F_{osc})	Oscillator	100 Hz (Oscillator ÷ 10^5 or 10^4)

External Decimal Point Input — When the external decimal point is selected this input is active. Any of the digits, except D_7, can be connected to this point. D_7 should not be used since it will override the overflow output and leading zeros will remain unblanked after the decimal point. This input is available on the ICM7216C and D only.

Hold Input — When the Hold Input is at V^+, any measurement in progress is stopped, the main counter is reset and the chip is held ready to initiate a new measurement. The latches which hold the main counter data are not updated so the last complete measurement is displayed. When Hold is changed to V^-, a new measurement is initiated.

$\overline{\text{Reset}}$ Input — The $\overline{\text{Reset}}$ Input is the same as a Hold Input, except the latches for the Main Counter are enabled, resulting in an output of all zeros.

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DISPLAY CONSIDERATIONS

The display is multiplexed at a 500 Hz rate with a digit time of 244 μsec. An interdigit blanking time of 6 μsec is used to prevent ghosting between digits. The decimal point and leading zero blanking have been implemented for right hand decimal point displays, zeros following the decimal point will not be blanked. Also, the leading zero blanking will be disabled when the Main Counter overflows.

The ICM7216A and C are designed to drive common anode LED displays at peak current of 25mA/segment, using displays with $V_F = 1.8$ V at 25mA. The average DC current will be over 3mA under these conditions. The ICM7216B and D are designed to drive common cathode displays at peak current of 15mA/segment using displays with $V_F = 1.8$V at 15mA. Resistors can be added in series with the segment drivers to limit the display current in very efficient displays, if required. Figures 4,5,6 and 7 show the digit and segment currents as a function of output voltage.

To get additional brightness out of the displays, V^+ may be increased up to 6.0V. However, care should be taken to see that maximum power and current ratings are not exceeded.

FIGURE 4. ICM7216A & C Typical I_{DIG} vs. $V^+ - V_{OUT}$, $4.5V \leq V^+ - V^- \leq 6.0V$

FIGURE 5. ICM7216A & C Typical I_{SEG} vs. $V_{OUT} - V^-$

FIGURE 6. ICM7216B & D Typical I_{DIGIT} vs. $V_{OUT} - V^-$

FIGURE 7. ICM7216B & D Typical I_{SEG} vs. $V^+ - V_{OUT}$, $4.5V \leq V^+ - V^- \leq 6.0V$

The segment and digit outputs in ICM7216's are not directly compatible with either TTL or CMOS logic. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals.

Segment Identification:

ACCURACY

In a Universal Counter crystal drift and quantization errors cause errors. In Frequency, Period and Time Interval modes, a signal derived from the oscillator is used in either the Reference Counter or Main Counter. Therefore, in these modes an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppM/°C will cause a measurement error of 20ppM/°C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the Frequency mode the maximum accuracy is obtained with high frequency inputs and in Period mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 8, the least accuracy will be obtained at 10 KHz. In Time Interval measurements there can be an error of 1 count per interval. As a result there is the same inherent accuracy in all ranges as shown in Figure 9. In Frequency Ratio measurement can be more accurately obtained by averaging over more cycles of Input B as shown in Figure 10.

FIGURE 8. Maximum Accuracy of Frequency and Period Measurements Due to Limitations of Quantization Errors

FIGURE 9. Maximum Accuracy of Time Interval Measurement Due to Limitations of Quantization Errors

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FIGURE 10. Maximum Accuracy for Frequency Ratio Measurement Due to Limitation of Quantization Errors

CIRCUIT APPLICATIONS

The ICM7216 has been designed for use in a wide range of Universal and Frequency counters. In many cases, prescalers will be required to reduce the input frequencies to under 10 MHz. Because Input A and Input B are digital inputs, additional circuitry is often required for input buffering, amplification, hysterisis, and level shifting to obtain a good digital signal.

The ICM7216A or B can be used as a minimum component complete Universal Counter as shown in Figure 11. This circuit can use input frequencies up to 10 MHz at Input A and 2 MHz at Input B.

For input frequencies up to 40 MHz the circuit shown in Figure 12 can be used to implement a frequency counter. To obtain the correct measured value, it is necessary to divide the oscillator frequency by four as well as the input frequency. In doing this the time between measurements is also lengthened to 800 msec and the display multiplex rate is decreased to 125 Hz.

FIGURE 11. 10MHz Universal Counter

FIGURE 12. 40MHz Frequency Counter

If the input frequency is prescaled by ten, then the oscillator can remain at 10 or 1 MHz, but the decimal point must be moved one digit to the right. Figure 13 shows a frequency counter implemented with a ÷10 prescaler and an ICM7216C. Since there is no external decimal point with the ICM7216A or B, the decimal point must be implemented with additional drivers as shown in Figure 14. Note that there can be one zero to the left of the decimal point since the internal leading zero blanking cannot be changed. In Figure 15 additional logic has been added to count the input directly in period mode for maximum accuracy. In both Figures 13 and 14, Input A comes from Q_C of the prescaler rather than Q_A to obtain an input duty cycle of 40%. If the signal at Input A has a very low duty cycle then it may be necessary to use a 74121 monostable multivibrator or similar circuit to stretch the input pulse width to guarantee 50 nsec minimum pulse width.

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FIGURE 13. 100MHz Frequency Counter

FIGURE 14. 100MHz Multifunction Counter

FIGURE 15. 100MHz Frequency, 2MHz Period Counter

OSCILLATOR CONSIDERATIONS

The oscillator has been implemented as a high gain complementary FET inverter. An external resistor of 10MΩ or 22MΩ should be connected between the oscillator input and output to provide biasing. The oscillator is designed to work with a parallel resonant 10 MHz quartz crystal with a static capacitance of 22pF and a series resistance of less than 35 ohms.

For a specific crystal and load capacitance, the required g_m can be calculated as follows:

$$g_m = \omega^2 C_{in} C_{out} R_S \left(1 + \frac{C_O}{C_L}\right)^2$$

$$\text{where } C_L = \left(\frac{C_{in}C_{out}}{C_{in}+C_{out}}\right)$$

C_O = Crystal Static Capacitance
R_S = Crystal Series Resistance
C_{in} = Input Capacitance
C_{out} = Output Capacitance
$\omega = 2\pi f$

The required g_m should exceed the g_m specified for the ICM7216 by at least 50% to insure reliable startup. The oscillator input and output pins each contribute about 5pf to C_{in} and C_{out}. For maximum stability of frequency, C_{in} and C_{out} should be approximately twice the specified crystal static capacitance.

In cases where non decade prescalers are used it may be desirable to use a crystal which is neither 10 MHz or 1 MHz. In that case both the multiplex rate and time between measurements will be different. The multiplex rate is $f_{max} = \frac{f_{osc}}{2\times10^4}$ for 10 MHz mode and $f_{max} = \frac{f_{osc}}{2\times10^3}$ for the 1 MHz mode. The time between measurements is $\frac{2\times10^6}{f_{osc}}$ in the 10 MHz mode and $\frac{2\times10^5}{f_{osc}}$ in the 1 MHz mode.

The crystal and oscillator components should be located as close to the chip as practical to minimize pickup from other signals. Coupling from the External oscillator input to the oscillator output or input can cause undesirable shifts in oscillator frequency.

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CHIP TOPOGRAPHY

ICM7216A

ICM7216B

ICM7216C

ICM7216D

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$F_{A\,MAX}$, $F_{B\,MAX}$ as a Function of $V^+ - V^-$

FIGURE 16. Typical Operating Characteristics

PACKAGE DIMENSIONS

28 PIN CERDIP DUAL IN LINE PACKAGE

28 PIN PLASTIC DUAL IN LINE PACKAGE

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INTERSIL

ICM7226A/B
10 MHz Universal Counter System

ICM7226A Drives Common Anode LED's
ICM7226B Drives Common Cathode LED's

FEATURES

- **Functions as a frequency counter, period counter, unit counter, frequency ratio counter or time interval counter**
- **Output drivers directly drive both digits and segments of large 8 digit LED displays. Both common anode and common cathode versions are available**
- **Measures frequencies from DC to 10 MHz**
- **Measures period from 0.5μ sec to 10 sec**
- **Stable high frequency oscillator, uses either 1MHz or 10MHz crystal**
- **Control signals available for gating of prescalers and prescaler display logic**
- **Multiplexed BCD outputs**
- **All terminals protected against static discharge; no special handling precautions required**

GENERAL DESCRIPTION

The ICM7226 is a fully integrated Universal Counter and LED display driver. It combines a high frequency oscillator, a decade timebase counter, an 8 decade data counter and latches, a 7 segment decoder, digit multiplexer and 8 segment and 8 digit drivers which can directly drive large LED displays. The counter inputs accept a maximum frequency of 10MHz in frequency and unit counter modes and 2MHz in the other modes. Both inputs are digital inputs. In many applications, amplification and level shifting will be required to obtain proper digital signals for these inputs.

The ICM7226 can function as a frequency counter, period counter, frequency ratio (f_A/f_B) counter, time interval counter or as a totalizing counter. The counter uses either a 10MHz or 1MHz crystal timebase. An external timebase input is also provided. For period and time interval, the 10MHz timebase gives a 0.1μsec resolution. In period average and time interval average, the resolution can be in the nanosecond range. In the frequency mode, the user can select accumulation time of .01 sec, .1 sec, 1 sec and 10 sec. With a 10 sec accumulation time, the frequency can be displayed to a resolution of .1 Hz in the least significant digit. There is 0.2 second interval between measurements in all ranges. Control signals are provided to enable gating and storing of prescaler data.

Leading zero blanking has been incorporated with frequency displayed in KHz and time in usec. The display is multiplexed at a 500Hz rate with a 12.5% duty cycle for each digit. The ICM7226A is designed for common anode display with typical peak segment currents of 25mA. The ICM7226B is designed for common cathode displays with typical segment currents of 12mA. In the display off mode both digit drivers & segment drivers are turned off allowing the display to be used for other functions.

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ORDERING INFORMATION

Component:

- ICM7226A IDL (Common anode driver, −20° C to +70° C Operating temperature range, 40 pin ceramic DIP)
- ICM7226B IPL (Common cathode driver, −20° C to +70° C Operating temperature range, 40 pin plastic DIP)

Evaluation Kit:

- ICM7226 EV/KIT - See page 3

PIN CONFIGURATION

***FOR MAXIMUM FREQUENCY STABILITY, CONNECT TO V^+ OR V^-**

ABSOLUTE MAXIMUM RATINGS

Maximum Supply Voltage (V+-V-) ..... 6.5 volts
Maximum Digit Output Current 400mA
Maximum Segment Output Current 60mA
Voltage on any Input or Output Terminal (Note 2) ..... Not to exceed V^+-V^- by more than ±0.3 volts
Maximum Power Dissipation at ..... 1.0 watts (ICM7226A)
70° C (Note 1) ..... 0.5 watts (ICM7226B)
Maximum Operating Temperature Range ..... -20° C to +70° C
Maximum Storage Temperature Range ..... -55° C to +125° C

Absolute maximum ratings refer to values that if exceeded may destroy or permanently change the device. The device is guaranteed for continous operation only under the conditions defined under the section TYPICAL OPERATING CHARACTERISTICS.

Note 1: The ICM7226 may be triggered into a destructive latchup mode if either input signals are applied before the power supply is applied or if input or outputs are forced to voltages exceeding V^+-V^- by more than 0.3 volts.

ELECTRICAL CHARACTERISTICS V^+-V^- = 5.0V, Test Circuit, T_A = 25° C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
Operating Supply Current	I_{DD}	Display Off Unused inputs to V^-		2	5	mA
Supply Voltage Range		-20° C < T_A < 70° C Input A, Input B Frequency at F_{MAX}	4.75		6.0	volts
Maximum Guaranteed Frequency Input A, Pin 40	F_{AMAX}	-20° C < T_A < 70° C 4.75V < V^+-V^- < 6.0V Figure 1 Function = Frequency, Ratio, Unit Counter Function = Period, Time Interval	 10 2.5	 14 	 	 MHz MHz
Maximum Frequency Input B, Pin 2	F_{BMAX}	-20° C < T_A < 70° C 4.75V < V^+ -V^- < 6.0V Figure 2	2.5			MHz
Minimum Separation Input A to Input B Time Interval Function		-20° C < T_A < 70° C 4.75V < V^+ -V^- < 6.0V Figure 3	250			nsec
Maximum osc. freq. and ext. osc. freq. Minimum ext. osc. freq.		-20° C < T_A < 70° C 4.75V < V^+ -V^- < 6.0V	10		 100	MHz kHz
Oscillator Transconductance	gm	V^+ -V^- = 4.75V T_A = +70° C	2000			μS
Multiplex Frequency Time Between Measurements	F_{MAX}	f_{osc} = 10 MHz f_{osc} = 10 MHz		500 200		Hz msec

Figure 1: Waveform for Guaranteed Minimum F_{AMAX} Function = Frequency, Frequency Ratio, Unit Counter.

Figure 2: Waveform for Guaranteed Minimum F_{BMAX} and F_{AMAX} for Function = Period and Time Interval.

Figure 3: Waveform for Minimum Time Between Transitions of Input A and Input B.

For single or "one-shot" time interval measurements, Input A then Input B must have a high to low transition prior to the interval which is to be measured. Provisions for "priming" the circuit as described above must be made using external circuitry. For repetitive signals this occurs automatically.

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ELECTRICAL CHARACTERISTICS = $V^+ - V^-$ = 5.0V, test circuit, T_A = 25°C, unless otherwise specified.

PARAMETER	SYMBOL	CONDITION	MIN	TYP	MAX	UNITS
INPUT VOLTAGES PINS 2,19,33,39,40 input low voltage input high voltage	 V_{IL} V_{IH}	 −20°C < T_A < +70°C Referred to V^-	 1.0		 3.5	 V V
PIN 2, 39, 40 INPUT LEAKAGE, A, B	I_L				20	μA
PIN 33 input low voltage input high voltage	 V_{IL} V_{IH}	 −20°C < T_A < 70°C Referred to V^-	 .8		 2.0	 V V
Input resistance to V^+ PINS 19,33	R	$V_{IN} = V^+ - 1.0V$.	100	400		kΩ
Input resistance to V^- PIN 31	R	$V_{IN} = V^- + 1.0V$	50	100		kΩ
Output Current PINS 3,5,6,7,17,18,32,38	I_{OL}	$V_{OL} = V^- + 0.4V$	.40			mA
PINS 5,6,7,17,18,32	I_{OH}	$V_{OH} = V^- + 0.4V$	100			μA
PINS 3,38	I_{OH}	$V_{OH} = V^+ - .8V$	265			μA
ICM7226A DIGIT DRIVER PINS 22,23,24,26,27,28,29,30 high output current low output current	 I_{OH} I_{OL}	 $V_{out} = V^+ - 2.0V$ $V_{out} = V^- + 1.0V$	 150	 180 −.3		 mA mA
SEGMENT DRIVER PINS 8,9,10,11,13,14,15,16 low output current high output current	 I_{OL} I_{OH}	 $V_{out} = V^- + 1.5$ $V_{out} = V^+ - 1.0V$	 25	 35 100		 mA μA
MULTIPLEX INPUTS PINS 1,4,20,21 input low voltage input high voltage	 V_{IL} V_{IH}	 Referred to V^-	 2.0		 .8	 V V
Input Resistance to V−	R	$V_{IN} = V^- + 1.0V$	50	100		kΩ
ICM7226B DIGIT DRIVER PINS 8,9,10,11,13,14,15,16 low output current high output current	 I_{OL} I_{OH}	 $V_{out} = V^- + 1.0V$ $V_{out} = V^+ - 2.5V$	 50	 75 100		 mA μA
SEGMENT DRIVER PINS 22,23,24,26,27,28,29,30 high output current leakage current	 I_{OH} I_L	 $V_{out} = V^+ - 2.0V$ $V_{out} = V^-$	 10	 15	 10	 mA μA
MULTIPLEX INPUTS PINS 1,4,20,21 input low voltage input high voltage	 V_{IL} V_{IH}	 	 $V^+ - .8$		 $V^+ - 2.0$	 V V
input resistance to V^+	R	$V_{IN} = V^+ - 1.0V$	200	360		kΩ

6

EVALUATION KIT

An evaluation kit is available for the ICM7226. It includes all the components necessary to assemble and evaluate a universal frequency/period counter based on the ICM7226. With the help of this kit, an engineer or technician can have the ICM7226 "up-and-running" in less than an hour. Specifically, the kit contains an ICM7226AIDL, a 10MHz quartz crystal, eight each 7-segment .3" leds, PC board, resistors, capacitors, diodes, switches and IC socket. Ordering information for the kit is given on page 1.

BLOCK DIAGRAM

TEST CIRCUIT

APPLICATION NOTES

GENERAL

Inputs A & B

The signal to be measured is input at Input A in Frequency, Period, Unit Counter, Frequency Ratio and Time Interval modes. The other input signal to be measured is input at Input B in Frequency Ratio and Time Interval. In Frequency Ratio F_A should be larger than F_B.

Both inputs are digital inputs with a typical switching threshold of 2.0V at $V^+ = 5.0V$. For optimum performance the peak to peak input signal should be at least 50% of the supply voltage and centered about the switching voltage. When these inputs are being driven from TTL logic, it is desirable to use a pullup resistor. The circuit counts high to low transitions at both inputs.

Note: The amplitude of the input should not exceed the supply by more than .3 volt otherwise, the circuit may be damaged.

Multiplexed Inputs

The function, range, control and external decimal point inputs are time multiplexed to select the input function desired. This is achieved by connecting the appropriate digit driver output to the inputs. The input function, range and control inputs must be stable during the last half of each digit output, (typically 125 μsec). The multiplex inputs are active high for the common anode ICM7226A and active low for the common cathode ICM7226B.

Noise on the multiplex inputs can cause improper operation. This is particularly true when the unit counter mode of operation is selected, since changes in voltage on the digit drivers can be capacitively coupled through the LED diodes to the multiplex inputs. For maximum noise immunity, a 10K resistor should be placed in series with the multiplex inputs as shown in the application notes.

Table 1 shows the functions selected by each digit for these inputs.

TABLE 1

	FUNCTION	DIGIT
FUNCTION INPUT PIN 4	Frequency	D_0
	Period	D_7
	Frequency Ratio	D_1
	Time Interval	D_4
	Unit Counter	D_3
	Oscillator Frequency	D_2
RANGE INPUT PIN 21	.01 Sec/1 Cycle	D_0
	.1 Sec/10 Cycles	D_1
	1 Sec/100 Cycles	D_2
	10 Sec/1k Cycles	D_3
External Range Input PIN 31	Enabled	D_4
CONTROL INPUT PIN 1	Blank Display	D_3&Hold
	Display Test	D_7
	1MHz Select	D_1
	External Oscillator Enable	D_0
	External Decimal Point Enable	D_2
	Test	D_4
EXTERNAL DECIMAL POINT INPUT, PIN 20	Decimal Point is Output for Same Digit That is Connected to This Input	

Control Input Functions

Display Test - All segments are enabled continuously, giving a display of all 8's with decimal points. The display will be blanked if Display Off is selected at the same time.

Display Off - To enable the Display Off mode it is necessary to input D_3 to the control input and have the HOLD input at V^+. The chip will remain in the Display Off mode until HOLD is switched back to V^-. While in the Display Off mode, the segment and digit driver outputs are open. During Display Off the oscillator continues to run with a typical supply current of 1.5mA with a 10MHz crystal and no measurements are made. In addition, inputs to the multiplexed inputs will have no effect. A new measurement is initiated when the HOLD input is switched to V^-

1MHz Select - The 1MHz select mode allows use of a 1MHz crystal with the same digit multiplex rate and time between measurements as with a 10MHz crystal. The decimal point is also shifted one digit to the right in Period and Time Interval, since the least significant digit will be in μsecond increments rather than 0.1 μsec increments.

External Oscillator Enable - In this mode the external oscillator input is used instead of the on chip oscillator for the Timebase input and Main Counter input in Period and Time interval modes. The on chip oscillator will continue to function when the external oscillator is selected, but will have no effect on circuit operation. The external oscillator input frequency must be greater than 100KHz or the chip will reset itself to enable the on chip oscillator.

External Decimal Point Enable - When external decimal point is enabled a decimal point will be displayed whenever the digit driver connected to the external decimal point is active. Leading Zero Blanking will be disabled for all digits following the decimal point.

Test Mode - In the test mode the main counter is split into groups of two digits each and the groups are clocked in parallel. The reference counter is split such that the clock into the reference count goes directly to the clock of the third decade counter (10 sec/1k cycle range). Store is also enabled so the count in the main counter is continuously output.

Range Input - The range input selects whether the measurement is made for 1, 10, 100, 1000 counts of the reference counter or if the external range input determines the measurement time. In all functional modes except Unit Counter a change in the range input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the Range Input is changed.

Function Input - The six functions that can be selected are: Frequency, Period, Time Interval, Unit Counter, Frequency Ratio and Oscillator Frequency.

These functions select which signal is counted into the main counter and which signal is counted by the reference counter as shown in Table 2. In Time Interval a flip flop is toggled first by a 1 → 0 transition at Input A and then by a 1 → 0 transition at Input B. The oscillator is gated into the Main Counter from the time Input A toggles the flip flop until Input B gates the flip flop. A change in the function input will stop the measurement in progress without updating the display and then initiate a new measurement. This prevents an erroneous first reading after the Function Input is changed. If main counter overflows, an overflow indication is output on the decimal point output during D7.

TABLE 2

DESCRIPTION	MAIN COUNTER	REFERENCE COUNTER
Frequency (F_A)	Input A	100Hz (Oscillator ÷ 10^5 or 10^4)
Period (T_A)	Oscillator	Input A
Ratio (F_A/F_B)	Input A	Input B
Time Interval (A→B)	Osc•Time Interval FF	Time Interval FF
Unit Counter(Count A)	Input A	Not Applicable
Osc. Freq. (Fosc)	Oscillator	100Hz (Osc ÷ 10^5 or 10^4)

External Decimal Point Input - when the external decimal point is selected this input is active. Any of the digits, except D_7, can be connected to this point. D_7 should not be used since it will overide the overflow output and leading zeros will remain unblanked after the decimal point.

Hold Input - Except in the Unit counter mode when the Hold Input is at V^+, any measurement in progress is stopped, the main counter is reset and the chip is held ready to initiate a new measurement. The latches which hold the main counter data are not updated so the last complete measurement is displayed. In Unit counter mode when Hold Input is at V^+ the counter is stopped but not reset. When Hold is changed to V^- the count continues from where the counter stopped.

$\overline{\text{Reset}}$ Input - The $\overline{\text{Reset}}$ Input is the same as a Hold Input, except the latches for the main counter are enabled, resulting in an output of all zeros.

External Range Input - The External Range Input is used to select different ranges than those provided on the chip. Figure 4 shows the relationship between Measurement In Progress and External Range Input.

Figure 4: External Range Input to End of Measurement in Progress.

Measurement In Progress, $\overline{\text{Store}}$ and $\overline{\text{Reset}}$ Outputs - These outputs are provided to enable display of prescaler digits. Figure 5 shows the relationship between these signals during the time between measurements. All three outputs can drive a low power Schottky TTL load. The Measurement In Progress Output can directly drive an ECL load, if the ECL device is powered from the same power supply as the ICM7226.

Figure 5: Reset, $\overline{\text{Store}}$, and Measurement in Progress Outputs Between Measurements.

BCD Outputs - The BCD representation of each digit output is output on the BCD outputs. Leading zero blanking of the display has no effect on the BCD output. Each BCD output will drive one low power Schottky TTL load. Table 3 shows the truth table for the BCD outputs.

TABLE 3 Truth Table BCD Outputs

NUMBER	D PIN 7	C PIN 6	B PIN 17	A PIN 18
0	0	0	0	0
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	1

Buffered Oscillator Output - The Buffered Oscillator Output has been provided to enable use of the on chip oscillator signal without loading the oscillator itself. This output will drive one low power Schottky TTL load. Care should be taken to minimize capacitive loading on this pin.

DISPLAY CONSIDERATIONS

The display is multiplexed at a 500Hz rate with a digit time of 244 μsec. An interdigit blanking time of 6 μsec is used to prevent ghosting between digits. The decimal point and leading zero blanking have been implemented for right hand decimal point displays. Any zeros following the decimal point will not be blanked. Also, the leading zero blanking will be disabled if the Main Counter overflows. The decimal point has been implemented to display frequency in KHz and time in μsec.

The ICM7226A is designed to drive common anode LED displays at peak current of 25mA/segment, using displays with V_F = 1.8V at 25mA. The average DC current will be over 3mA under these conditions. The ICM7226B is designed to drive common cathode displays at peak current of 15mA/segment using displays with V_F = 1.8V at 15mA. Resistors can be added in series with the segment drivers to limit the display current in very efficient displays, if required. Figures 6, 7, 8 and 9 show the digit and segment currents as a function of output voltage for common anode and common cathode drivers.

Figure 6: ICM7226A Typical I_{DIG} Vs. V^+-V_{out}
$4.5 \le V^+ - V^- \le 6.0V$

Figure 7: ICM7226A Typical I_{SEG} Vs. V_{out}-V^-

Figure 8: ICM7226B Typical I_{DIGIT} Vs. $V_{OUT}-V^-$

Figure 9: ICM7226B Typical I_{SEG} Vs. V^+-V_{out}
$4.5V \leq V^+-V^- \leq 6.0V$

To increase the light output from the displays, V^+ may be increased up to 6.0V, however, care should be taken to see that maximum power and current ratings are not exceeded.

The segment and digit outputs in both the 7226A and B are not directly compatible with either TTL or CMOS logic. Therefore, level shifting with discrete transistors may be required to use these outputs as logic signals.

Segment Identification

ACCURACY

In a Universal Counter crystal drift and quantization errors cause errors. In Frequency, Period and Time Interval Modes, a signal derived from the oscillator is used in either the Reference Counter or Main Counter. Therefore, in these modes an error in the oscillator frequency will cause an identical error in the measurement. For instance, an oscillator temperature coefficient of 20ppm/°C will cause a measurement error of 20ppm/°C.

In addition, there is a quantization error inherent in any digital measurement of ±1 count. Clearly this error is reduced by displaying more digits. In the Frequency Mode the maximum accuracy is obtained with high frequency inputs and in Period Mode maximum accuracy is obtained with low frequency inputs. As can be seen in Figure 10, the least accuracy will be obtained at 10 KHz. In Time Interval measurements there is a maximum error of 1 count per interval. As a result there is the same inherent accuracy in all ranges as shown in Figure 11. In Frequency Ratio measurement more accuracy can be obtained by averaging over more cycles of Input B as shown in Figure 12.

Figure 10: Maximum Accuracy of Frequency and Period Measurements Due to Limitations of Quantization Errors.

Figure 11: Maximum Accuracy of Time Interval Measurement Due to Limitations of Quantization Errors.

Figure 12: Maximum Accuracy for Frequency Ratio Measurement Due to Limitations of Quantization Errors.

CIRCUIT APPLICATIONS

The ICM7226 has been designed to be used as a complete Universal Counter or with prescalers and other circuitry in a variety of applications. Since Input A and Input B are digital inputs additional circuitry will be required in many applications for input buffering, amplification, hysteresis, and level shifting to obtain the required digital voltages. For many applications an FET source follower can be used for input buffering and an ECL 10116 line receiver can be used for amplification and hysteresis to obtain a high impedance input, sensitivity and bandwidth. However, cost and complexity of this circuitry can vary widely depending upon the sensitivity and bandwidth required. When TTL prescalers or input buffers are used, pull up resistors to V^+ should be used to obtain optimal voltage swing at Inputs A and B.

If prescalers aren't required the ICM7226 can be used to implement a minimum component Universal counter as shown in figure 13. This circuit can be for input frequencies up to 10MHz at Input A and 2MHz at Input B.

For input frequencies up to 40 MHz the circuit shown in figure 14 can be used to implement a Frequency and Period Counter. To obtain the correct value when measuring

frequency and period it is necessary to divide the 10MHz oscillator frequency down to 2.5MHz. In doing this the time between measurements is also lengthened to 800 msec. and the display multiplex rate is decreased to 125 Hz.

If the input frequency is prescaled by ten then the oscillator frequency can remain at 10 or 1MHz, but the decimal point must be moved. Figure 15 shows use of a ÷10 prescaler in frequency counter mode. Additional logic has been added to have the 7226 count the input directly in Period mode for maximum accuracy. Note that Input A comes from Q_C rather than Q_D to obtain an input duty cycle of 40%. If an output without a duty cycle near 50% must be used then it may be necessary to use a 74121 monostable multivibrator or similar circuit to stretch the input pulse to guarantee a 50 nsec minimum pulse width.

Figure 13: 10MHz Universal Counter

Notes: 1) If a 2.5MHz crystal is used then diode D1 and I.C's 1 and 2 can be eliminated.

Figure 14: 40MHz Frequency, Period Counter

Figure 16 shows the use of a CD4016 analog multiplexer to multiplex the digital outputs back to the Function Input. Since the CD4016 is a digitally controlled analog transmission gate no level shifting of the digit output is required. CD4051's or CD4052's could also be used to select the proper inputs for the multiplexed input on the ICM7226 from 2 or 3 bit digital inputs. These analog multiplexers could also be used in systems in which the mode of operation is controlled by a microprocessor rather than directly from front panel switches. TTL multiplexers such as the 74153 or 74251 could also be used, but some additional circuitry will be required to convert the digit output to TTL compatible logic levels.

DEVICE NO.	TYPE
1	74LS00 OR 7400
2	7404 OR 74LS04
3	11C90
4	11C90
5	ICM7226A

Figure 15: 100MHz Multi Function Counter

DEVICE NO.	TYPE
1	7400 OR 74LS00
2	CD4016
3	11C90
4	ICM7226B

Figure 16: 100MHz Frequency Period Counter

If the prescaler information needs to be displayed, then the Measurement in Progress, Store and Reset outputs from the ICM7226 can be used to control the prescaler and data latch as shown in figure 17. Note that the output of IC 7 has been decoded with a NAND to obtain a 40% duty cycle for the signal into input A.

To obtain a full Universal Counter with prescalers with the count displayed, it is necessary to add significantly more circuitry to implement the Time External Mode as shown in figure 18.

All of the circuits shown directly drive a multiplexed LED display, however, the BCD outputs can be used with external BCD to 7 segment decoders and appropriate level shifting to drive other types of displays.

FIGURE 17
9 DIGIT MULTIFUNCTION COUNTER

DEVICE	TYPE
1,5	74LS04
2	7404
3	74S00
4	74LS00
6	11C90
7,8	75S112
9	7477
10	7446
11	ICM7226A

Figure 17: 9 Digit Multi Function Counter

FIGURE 18
9 DIGIT UNIVERSAL COUNTER

DEV. #	TYPE
1,2,5	74LS04 OR CD4049
3,9	74S04
4	74LS10
6,7,10	74S00
8	74S10
11	74LS80
12,13,14	74S112 OR 74S114
15	7477
16	7446
17	ICM7226A

Figure 18: 9 Digit Universal Counter

The circuit shown in figure 19 can be used in any of the circuit applications shown to implement a single measurement mode of operation. This circuit uses the Store output to put the ICM7226 into a hold mode. The Hold input can also be used to reduce the time between measurements. The circuit shown in figure 20 puts a short pulse into the Hold input a short time after Store goes low. A new measurement will be initiated at the end of the pulse on the Hold Input. This circuit reduces the time between measurements to less than 40 msec from 200 msec. Use of the circuit shown in Figure 20 on the circuit shown in Figure 14 will reduce the time between measurements from 800 msec. to 1600 msec.

SWITCH	FUNCTION
S1	OPEN = SINGLE MEAS MODE ENABLED
S2	CLOSED = INITIATE NEW MEASUREMENT
S3	CLOSED = HOLD INPUT

Figure 19: Single Measurement Circuit for Use With ICM7226

Figure 20: Circuit for Reducing Time Between Measurements

Figure 21: Typical Operating Characteristics

OSCILLATOR CONSIDERATIONS

The oscillator has been implemented as a high gain complementary FET inverter. An external resistor of 10MΩ or 22MΩ should be connected between the oscillator input and output to provide biasing. The oscillator is designed to work with a parallel resonance of 10 MHz quartz crystal with a static capacitance of 22pF and a series resistance of less than 35 ohms.

For a specific crystal and load capacitance, the required g_m can be calculated as follows:

$$g_m = \omega^2 \, C_{in} \, C_{out} \, R_s \left(1+\frac{C_O}{C_L}\right)^2$$

$$\text{where } C_L = \left(\frac{C_{in}C_{out}}{C_{in}+C_{out}}\right)$$

C_O = Crystal static capacitance
R_S = Crystal Series Resistance
C_{in} = Input Capacitance
C_{out} = Output Capacitance
$\omega = 2\pi f$

The required g_m should exceed the g_m specified for the ICM7226 by at least 50% to insure reliable startup. The oscillator input and output pins each contribute about 5pf to Cin and Cout. For maximum frequency stability, Cin and Cout should be approximately twice the specified crystal static capacitance.

In cases where non decade prescalers are used it may be desirable to use a crystal which is neither 10MHz. In that case, both the multiplex rate and time between measurements will be different. The multiplex rate is $f_{max} = \frac{f_{osc}}{2x10^4}$ for 10MHz mode and $f_{max} = \frac{f_{osc}}{2x10^3}$ for the 1MHz mode. The time between measurements is $\frac{2x10^6}{f_{osc}}$ in the 10MHz mode and $2x10^5$ in the 1MHz mode. The buffered oscillator output should be used for an oscillator test point or to drive additional logic. This output will drive one low power Schottky TTL load. When the buffered oscillator output is used to drive CMOS or to drive the external oscillator input, a 10kΩ resistor should be added from buffered oscillator output to V^+.

The crystal and oscillator components should be located as close to to the chip as practical to minimize pickup from other signals. In particular, coupling from the Buffered Oscillator Output and External Oscillator Input to the oscillator output or input can cause undesirable shifts in oscillator frequency. To minimize this coupling, pins 34 and 37 should be connected to V^+ or V^- and these two signals should be kept away from the oscillator circuit.

CHIP TOPOGRAPHY (ICM7226A SHOWN)

PACKAGE DIMENSIONS

40 Pin Plastic Dual-in-Line Package

40 Pin Ceramic Dual-in-Line Package

6

INTERSIL

ICM7217 Series
ICM7227 Series
4 Digit CMOS Up/Down Counter/ Display Driver

FEATURES

- **Four decade, presettable up-down counter with parallel zero detect**
- **Settable register with contents continuously compared to counter**
- **Directly drives multiplexed 7 segment common anode or common cathode LED displays**
- **On-board multiplex scan oscillator**
- **Schmitt trigger on count input**
- **TTL compatible BCD I/O port, carry/borrow, equal, and zero outputs**
- **Display blank control for lower power operation; quiescent power dissipation < 5mW**
- **All terminals fully protected against static discharge**
- **Single 5V supply operation**

DESCRIPTION

The ICM7217 and ICM7227 are four digit, presettable up/down counters, each with an onboard presettable register continuously compared to the counter. The ICM7217 versions are intended for use in hardwired applications where thumbwheel switches are used for loading data, and simple SPDT switches are used for chip control. The ICM7227 versions are for use in processor-based systems, where presetting and control functions are performed under processor control.

These circuits provide multiplexed 7 segment LED display outputs, with common anode or common cathode configurations available. Digit and segment drivers are provided to directly drive displays of up to 1" character height at a 25% duty cycle. The frequency of the onboard multiplex oscillator may be controlled with a single capacitor, or the oscillator may be allowed to free run. Leading zeroes can be blanked. The data appearing at the 7 segment and BCD outputs is latched; the content of the counter is transferred into the latches under external control by means of the Store pin.

The ICM7217/7227 (common anode) and ICM7217A/7227A (common cathode) versions are decade counters, providing a maximum count of 9999, while the ICM7217B, 7227B (common anode) and ICM7217C/7227C (common cathode) are intended for timing purposes, providing a maximum count of 5959.

These circuits provide 3 main outputs; a carry/borrow output, which allows for direct cascading of counters, a zero output, which indicates when the count is zero, and an equal output, which indicates when the count is equal to the value contained in the register. Data is multiplexed to and from the device by means of a tri-state BCD I/O port. The carry/borrow, equal, zero outputs, and the BCD port will each drive one standard TTL load.

To permit operation in noisy environments and to prevent multiple triggering with slowly changing inputs, the count input is provided with a Schmitt trigger.

Input frequency is guaranteed to 2MHz, although the device will typically run with f_{in} as high as 5MHz.

CONNECTION DIAGRAMS

COMMON ANODE

COMMON CATHODE

COMMON ANODE

COMMON CATHODE

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (common anode/Cerdip) ..... 1 Watt } Note 1
Power Dissipation (common cathode/Plastic) ..... 0.5 Watt }
Supply Voltage V^+-V^- 6V
Input voltage (any terminal) ..... V^++0.3V V^- −0.3V - Note 2
Operating temperature range ..... −20°C to +70°C
Storage temperature range ..... −55°C to +125°C

Absolute maximum ratings define stress limitations which if exceeded may permanently damage the device. For continuous operation these devices must be operated under the conditions defined under "Operating Characteristics."

OPERATING CHARACTERISTICS

V^+-V^- = 5V, T_A = 25°C, Test Circuit, Display Diode Drop 1.7V, unless otherwise specified

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply current (Lowest power mode)	I_{MIN}, (7217)	Display Off, LC, DC, UP/DN, ST, RS, BCD I/O Floating or at V^+ (Note 3)		350	500	μA
Supply current (Lowest power mode)	I_{MIN}, (7227)	Display off (Note 3)		300	500	μA
Supply current OPERATING	I_{OP}	Common Anode, Display On, all "8's"	175	200		mA
		Common Cathode, Display On, all "8's"	85	100		mA
Supply Voltage	V^+-V^-		4.5	5	5.5	V
Digit Driver output current	I_{DIG}	Common anode, V_{OUT} = V^+ −2.2V	175	200		mA peak
Segment driver output current	I_{SEG}	Common anode, V_{OUT} = V^- +1.3V	−25	−40		mA peak
Digit Driver output current	I_{DIG}	Common cathode, V_{OUT} = V^- +1.3V	−75	−100		mA peak
Segment Driver output current	I_{SEG}	Common cathode V_{OUT} = V^+ −2V	10	12.5		mA peak
$\overline{ST}$, $\overline{RS}$, UP/DN input pullup current	I_P	V_{OUT} = V^+ −2V (See Note 3)	5	25		μA
3 level input impedance				100		kΩ
BCD I/O input high voltage	V_{BIH}	ICM7217 common anode (Note 4)	1.3			V
		ICM7217 common cathode (Note 4)	4.1			V
		ICM7227 with 50pF effective load	3			V
BCD I/O input low voltage	V_{BIL}	ICM7217 common anode (Note 4)			0.8	V
		ICM7217 common cathode (Note 4)			3.7	V
		ICM7227 with 50pF effective load			1.5	V
BCD I/O input pullup current	I_{BPU}	ICM7217 common anode V_{IN} = V^+ −2V (Note 3)	5	25		μA
BCD I/O input pulldown current	I_{BPD}	ICM7217 common cathode V_{IN} = V^- +1.3V (Note 3)	5	25		μA
BCD I/O, Carry/borrow zero, equal outputs output high current	I_{BOH}	V_{OH} = V^+ −1.5V	100			μA
BCD I/O, Carry/borrow zero, equal outputs output low current	I_{BOL}	V_{OL} = V_{OL} V^- +0.4V	−2			mA
Count input frequency (Guaranteed)	f_{in}	V^+ - V^- = 5V ± 10%, −20°C < T_A < +70°C	0	5	2	MHz
Count input threshold	V_{TC}	V^+ - V^- = 5V		2		V
Count input hysteresis	V_{HC}	V^+-V^- = 5V		0.5		V
Display scan oscillator frequency	f_{ds}	Free-running (SCAN terminal open circuit)		10		KHz
Operating Temperature Range	T_A	Industrial temperature range	−20		70	°C

NOTE 1 These limited refer to the package and will not be obtained during normal operation.

NOTE 2 Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ or less than V^- may cause destructive device latchup. For this reason it is recommended that the power supply to the device be established before any inputs are applied and that in multiple systems the supply to the ICM7217/7227 be turned on first.

NOTE 3 In the ICM7217 the Up/Down, Store, Reset and the BCD I/O as inputs have pullup devices which consume power when connected to the negative supply. When all these terminals are connected to the negative supply, with the display off, the device will consume typically 750 μA. The ICM7227 devices do not have these pullups and thus are not subject to this condition.

NOTE 4 These voltages are adjusted to allow the use of thumbwheel switches for the ICM7217 versions. Note that a positive level is taken as a logic zero for ICM7217 common-cathode versions only.

TEST CIRCUITS

Figure 1

Figure 1 shows the ICM7217 in the common-anode version and the ICM7227 in the common-cathode version.

Figure 2: Block Diagram ICM7217

Figure 3: Multiplex Timing

Figure 4: Thumbwheel switch/diode connections

Figure 5: ICM7227 I/O Timing (See Table 2)

6

CONTROL INPUT DEFINITIONS ICM7217

INPUT	TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{Store}}$ ($\overline{\text{ST}}$)	9	V^+ (or floating) V^-	Output latches not updated Output latches updated
Up/Down (U/$\overline{\text{D}}$)	10	V^+ (or floating) V^-	Counter counts up Counter counts down
$\overline{\text{Reset}}$ ($\overline{\text{RST}}$)	14	V^+ (or floating) V^-	Normal Operation Counter Reset
Load Counter LC/I/O $\overline{\text{OFF}}$	12	Unconnected V^+ V^-	Normal operation Counter loaded with BCD data BCD port forced to Hi Z condition
Load Register LR/$\overline{\text{OFF}}$	11	Unconnected V^+ V^-	Normal operation Register loaded with BCD data Display drivers disabled; BCD port forced to Hi Z condition, mpx counter reset to D3; mpx oscillator inhibited
Display Control (DC)	23 Common Anode 20 Common Cathode	Unconnected V^+ V^-	Normal operation Segment drivers disabled Leading zero blanking inhibited

CONTROL INPUT DEFINITIONS ICM7227

INPUT		TERMINAL	VOLTAGE	FUNCTION
	$\overline{\text{Data Transfer}}$ ($\overline{\text{DT}}$)	13	V^+ V^-	Normal Operation Causes transfer of data as directed by select code
Control Word Port	Store (ST)	9	V^+ (During $\overline{\text{CWS}}$ Pulse) V^-	Output latches updated Output latches not updated
"	Up/Down (U/$\overline{\text{D}}$)	10	V^+ (During $\overline{\text{CWS}}$ Pulse) V^-	Counter counts up Counter counts down
" "	Select Code Bit 1 (SC1) Select Code Bit 2 (SC2)	11 12	$V^+ = 1$ $V^- = 0$	SC1, SC2 00 Change store and up/down latches. No data transfer. 01 Output latch data active 10 Counter to be preset 11 Register to be preset
	$\overline{\text{Control Word Strobe}}$ ($\overline{\text{CWS}}$)	14	V^+ V^-	Normal operation Causes control word to be written into control latches
	Display Control (DC)	23 Common Anode 20 Common Cathode	Unconnected V^+ V^-	Normal operation Display drivers disabled Leading zero blanking inhibited

6

DESCRIPTION OF OPERATION

OUTPUTS

The carry/borrow output is a positive going signal occurring typically 500nS after the positive going edge of the count input. It advances the counter from 9999 to 0000 when counting up and from 0000 to 9999 when counting down. This output allows direct cascading of counters.

The $\overline{\text{equal}}$ output assumes a negative level when the contents of the counter and register are equal.

The $\overline{\text{zero}}$ output assumes a negative level when the content of the counter is 0000.

The carry/borrow, $\overline{\text{equal}}$, and $\overline{\text{zero}}$ outputs will drive a single TTL load over the full range of supply voltage and ambient temperature; for a logic zero, these outputs will sink 2mA @ 0.4V (on resistance 200 ohms), and for a logic one, the outputs source >60μA.

The digit and segment drivers provide a decoded 7 segment display system, capable of directly driving common anode LED displays at typical peak currents of 40mA/seg. This corresponds to average currents of 10mA/seg at a 25% multiplex duty cycle. For the common cathode versions, peak segment currents are 12.5mA, corresponding to average segment currents of 3.1mA. The display pin controls the display output using three level logic. The pin is self-biased to a voltage approximately 1/2 (V^+-V^-); this corresponds to normal operation. When this pin is connected to V^+, the segments are inhibited, and when connected to V^-, the leading zero blanking feature is inhibited. For normal operation (display on with leading zero blanking) the pin may be left open. The display may be controlled with a 3 position SPDT switch; see fig. 1.

The BCD I/O port provides a means of transferring data to and from the device. The ICM7217 versions multiplex data into the counter or register via thumbwheel switches, depending on inputs to the load counter or load register pins; in the ICM7227 versions, input/output control and timing must be provided externally. When functioning as outputs, the BCD I/O pins will drive one standard TTL load.

The onboard multiplex scan oscillator has a nominal free-running frequency of 10kHz. This may be reduced by the addition of a single capacitor between the Scan pin and the positive supply, or the oscillator may be directly overdriven to about 20kHz. Capacitor values and corresponding nominal oscillator frequencies, digit repetition rates, and loading times (for ICM7217 versions) are shown in Table 1 below.

The internal oscillator output has a duty cycle of approximately 25:1, providing a short pulse occurring at the oscillator frequency. This pulse clocks the four-state counter which provides the four multiplex phases. The short pulse width is used to delay the digit driver outputs, thereby providing inter-digit blanking which prevents ghosting. The digits are scanned from MSD (D4) to LSD (D1). See Fig. 3 for the display digit multiplex timing.

Table 1

Scan Capacitor	Nominal Oscillator Frequency	Digit Repetition Date	Scan Cycle Time
None	10kHz	2.5kHz	400μs
20pF	5kHz	1.2kHz	800μs
90pF	1kHz	250Hz	4ms

CONTROL OF ICM7217

The counter is incremented by the rising edge of the count input signal when U/D is high. It is decremented when U/D is low. A Schmitt trigger on the count input provides hysteresis to prevent double triggering on slow rising edges and permits operation in noisy environments.

The $\overline{ST}$ pin controls the internal latches and consequently the signals appearing at the 7 segment and BCD outputs. Bringing the store pin to V^- transfers the contents of the counter into the latches.

The counter is asynchronously reset to 0000 by bringing the $\overline{RST}$ pin to V^-. The count input is inhibited during reset and load counter operations. The $\overline{ST}$, $\overline{RST}$ and Up/$\overline{Down}$ pins are provided with pullup resistors of approximately 75 kΩ.

The BCD I/O pins, the load counter (LC), and load register (LR) pins combine to provide presetting and compare functions. LC and LR are three-level inputs, being self-biased at approximately 1/2 (V^+-V^-) for normal operation. With both LC and LR open, the BCD I/O pins provide a multiplexed BCD output of the latch contents, scanned from MSD to LSD by the display multiplex. In this mode of operation, the BCD pins will drive one TTL load. When either or both of the LC or LR pins is connected to V^+, the TTL driver devices are turned off and the BCD pins become high-impedance inputs. When LC is connected to V^+, the count input is inhibited and the levels at the BCD pins are multiplexed into the counter. When LR is connected to V^+, the levels at the BCD pins are multiplexed into the register without disturbing the counter. When both are connected to V^+, the count is inhibited and both register and counter are presettable. When LR is connected to V^-, the oscillator is inhibited, the BCD I/O pins go to the high impedance state, and the segment and digit drivers are turned off. This allows the display to be used for other purposes and minimizes power consumption. In this display off condition, the circuit will continue to count, and the carry/borrow, equal, zero, up/down, reset and store functions operate as normal. When LC is connected to V^-, the BCD I/O pins are forced to the high impedance state without disturbing the counter or register. See "Control Input Definitions" for a cataloging of the pins that function as three-state self-biased inputs and their respective operations.

Note that the ICM7217 and 7217B have been designed to drive common anode displays. The BCD inputs are active high, as are the BCD outputs.

The ICM7217A and 7217C are used to drive common cathode displays, and the BCD inputs are active low. BCD outputs are active high.

The 7227 series has been designed to permit microprocessor control of the inputs. BCD inputs and outputs are active high.

NOTES ON THUMBWHEEL SWITCHES & MULTIPLEXING

The thumbwheel switches used with these circuits (both common anode and common cathode) are TRUE BCD coded; i.e. all switches open corresponds to 0000.

Since the thumbwheel switches are connected in parallel, diodes must be provided to prevent crosstalk between digits. See fig. 4.

In order to maintain reasonable noise margins, these diodes should be specified with low forward voltage drops.

During load counter and load register operations, the multiplex oscillator is disconnected from the scan input and is allowed to free-run. In all other conditions, the oscillator may be directly overdriven, however the internal oscillator output will be of the same duty cycle and phase as the overdriving signal, and the digits are blanked during the time the internal oscillator output is at a positive level. To insure proper leading zero blanking, the blanking time should not be less than about 2μs, and by varying the duty cycle, the display brightness may be altered. Overdriving the oscillator at less than 200Hz may cause display flickering. See fig. 6 for brightness control circuits.

These circuits are variable-duty-cycle oscillators suitable for overdriving the multiplex oscillator at the Scan input of an ICM7217. The inverters should be CMOS CD4000 series, and the diodes may be any inexpensive device such as IN914.

Figure 6: Brightness Circuits

OUTPUT AND INPUT RESTRICTIONS

The carry/borrow output is not valid during load counter and reset operations.

The $\overline{\text{equal}}$ output is not valid during load counter or load register operations.

The $\overline{\text{zero}}$ output is not valid during a load counter operation.

The reset input may be susceptible to noise if its input rise time (coming out of reset) is less than about 500μs. This will present no problems when this input is driven by active devices (i.e., TTL or CMOS logic) but in hardwired systems adding virtually any capacitance to the $\overline{\text{reset}}$ input can cause trouble. A simple circuit which provides a reliable power-up reset and a fast rise time on the $\overline{\text{reset}}$ input is shown below.

CONTROL OF 7227 VERSIONS

In the IM7227 versions, the Store, Up/$\overline{\text{Down}}$, SC1 and SC2 (select code bits 1 and 2) pins form a four-bit control word input. A negative-going pulse on the $\overline{\text{CWS}}$ (control word strobe) pin writes the data on these pins into four internal control latches, and resets the multiplex counter in preparation for sequencing a data transfer operation. The select code 00 is reserved for changing the state of the Store and/or Up/$\overline{\text{Down}}$ latches without initiating a data transfer. Writing a one into the Store latch sets the latch and causes the data in the counter to be transferred into the output latches, while writing a zero resets the latches causing them to retain data and not be updated. Similarly, writing a one into the Up/$\overline{\text{Down}}$ latch causes the counter to count up and writing a zero causes the counter to count down. The state of the Store and Up/$\overline{\text{Down}}$ latches may also be changed with a nonzero select code.

Writing a nonzero select code initiates a data transfer operation. Writing select code of 01 (SC1, SC2) indicates that the data in the output latches will be active and enables the BCD I/O port to output the data. Writing a select code of 11 indicates that the register will be preset, and a 10 indicates that the counter will be preset.

When a nonzero select code is read, the clock of the four-state multiplex counter is switched to the $\overline{\text{DT}}$ (data transfer) pin. Negative-going pulses at this pin then sequence a digit-by-digit data transfer, either outputting data or presetting the counter or register as determined by the select code. The output drivers of the BCD I/O port will be enabled only while $\overline{\text{DT}}$ is low during a data transfer initiated with a 01 select code.

The sequence of digits will be D4-D3-D2-D1, i.e. when outputting, the data from D4 will be valid during the first $\overline{\text{DT}}$ pulse, then D3 will be valid during the second pulse, etc. When presetting, the data for D4 must be valid at the positive-going transition (trailing edge) of the first $\overline{\text{DT}}$ pulse, the data for D3 must be valid during the second $\overline{\text{DT}}$ pulse, etc.

At the end of a data transfer operation, on the positive going transition of the fourth $\overline{\text{DT}}$ pulse, the SC1 and SC2 control latches will automatically reset, terminating the data transfer and reconnecting the multiplex counter clock to the oscillator. In the ICM7227 versions, the multiplex oscillator is always free-running, except during a data transfer operation when it is disabled.

Fig. 5 shows the timing of data transfers initiated with a 11 select code (writing into the register) and a 01 select code (reading out of the output latches). Typical times during which data must be valid at the control word and BCD I/O ports are indicated in Table 2.

Table 2

SYMBOL	DEFINITION	TIME, NS	SYMBOL	DEFINITION	TIME, NS
$t_{\overline{cws}}$	CONTROL WORD STROBE WIDTH	200	t_{cdh}	CONTROL DATA HOLD	100
t_{ics}	INTERNAL CONTROL SETUP	500	t_{ids}	INPUT DATA SETUP	100
			t_{idh}	INPUT DATA HOLD	100
$t_{\overline{dt}}$	DATA TRANSFER PULSE WIDTH	200	t_{oda}	OUTPUT DATA ACCESS	100
t_{cds}	CONTROL DATA SETUP	100	t_{odh}	OUTPUT DATA HOLD	100

APPLICATIONS

1. FIXED DECIMAL POINT

In the common anode versions, a fixed decimal point may be implemented by connecting the D.P. segment lead from the appropriate digit (with separate digit displays) through a 39Ω series resistor to V^-. With common cathode devices, the D.P. segment lead should be connected through a 75Ω series resistor to V^+

To force the device to display leading zeroes after a fixed decimal point, use a bipolar transistor and base resistor in a configuration like that of Fig. 8 with the resistor connected to the digit output driving the D.P. for left hand D.P. displays, and to the next least significant digit output for right hand D.P. display. For common cathode devices use a PNP and NPN transistor as shown below:

2. UNIT COUNTER WITH BCD OUTPUT (Figure 7)

The simplest application of the ICM7217 is a 4 digit unit counter. All that is required is an ICM7217, a power supply and a 4 digit display. Add a momentary switch for reset, an SPDT center-off switch to blank the display or view leading zeroes, and one more SPDT switch for up/down control. Using an ICM7217A and a common-cathode calculator-type display, results in the least expensive digital counter/display system available.

Figure 7: Unit Counter

3. PRECISION ELAPSED TIME/COUNTDOWN TIMER (Figure 8)

This circuit uses an ICM7213 precision one minute/one second timebase generator and a 4.1943 MHz crystal oscillator and divider for generating pulses counted by an ICM7217B. The thumbwheel switches allow a starting time to be entered into the counter for a preset-countdown type timer, and allow the register to be set for compare functions. For instance, to make a 24-hour clock with BCD output the register can be preset with 2400 and the $\overline{\text{Equal}}$ output used to reset the counter. Note the 10k resistor connected between the LC terminal and V^-. This resistor pulls the LC input low when not loading, thereby inhibiting the BCD output drivers. This resistor should be eliminated and SW4 replaced with an SPDT center-off switch if the BCD outputs are to be used. This technique may be used on any 3-level input. The 100k pullup resistor on the count input is used to ensure proper logic voltage swing from the ICM7213. For a less expensive (and less accurate) timebase, a 555 timer may be used in a configuration like that shown in Fig. 12 to generate a 1Hz reference.

Figure 8: Precision Timer

4. 8-DIGIT UP/DOWN COUNTER (Figure 9)

This circuit shows how to cascade counters and retain correct leading zero blanking. The NAND gate detects whether a digit is active since one of the two segments $\overline{a}$ or $\overline{b}$ is active on any unblanked number. The flip flop is clocked by the least significant digit of the high order counter, and if this digit is not blanked, the Q output of the flip flop goes high and turns on the NPN transistor, thereby inhibiting leading zero blanking on the low order counter.

It is possible to use separate thumbwheel switches for presetting, but as the devices load data with the oscillator free-running, the multiplexing of the two devices is difficult to synchronize. This presents no problems with the ICM7227 devices, since the two devices are operated as peripherals to a processor.

Figure 9: 8 Digit Up/Down Counter

5. TAPE RECORDER POSITION INDICATOR/ CONTROLLER (Figure 10)

This circuit shows an application which uses the up/down counting feature of the ICM7217 to keep track of tape position. This circuit is representative of the many applications of up/down counting in monitoring dimensional position. For example, an ICM7227 as a peripheral to a processor can monitor the position of a lathe bed or digitizing head, transfer the data to the processor, drive interrupts to the processor using the $\overline{\text{equal}}$ or $\overline{\text{zero}}$ outputs, and serve as a numerical display for the processor.

In the tape recorder application, the preset register, $\overline{\text{equal}}$ and $\overline{\text{zero}}$ outputs are used to control the recorder. To make the recorder stop at a particular point on the tape, the register can be set with the stop point and the $\overline{\text{equal}}$ output used to stop the recorder either on fast forward, play or rewind.

To make the recorder stop before the tape comes free of the reel on rewind, a leader should be used. Resetting the counter at the starting point of the tape, a few feet from the end of the leader, allows the zero output to be used to stop the recorder on rewind, leaving the leader on the reel.

The 1MΩ resistor and .0047μF capacitor on the count input provide a time constant of about 5ms to debounce the reel switch. The Schmitt trigger on the count input of the ICM7217 squares up the signal before applying it to the counter. This technique may be used to debounce switch-closure inputs in other applications.

Figure 10: Recorder Indicator

6. PRECISION FREQUENCY COUNTER/ TACHOMETER (Figure 11)

This circuit is a simple implementation of a four digit frequency counter, using an ICM7207A to provide the one second gating window and the $\overline{\text{store}}$ and $\overline{\text{reset}}$ signals. In this configuration, the display reads hertz directly. With Pin 11 of the ICM7027A connected to V^+, the gating time will be 0.1 second; this will display tens of hertz as the least significant digit. For shorter gating times, an ICM7207 may be used (with a 6.5536 MHz crystal), giving a 0.01 second gating with Pin 11 connected to V^+, and a 0.1 second gating with Pin 11 open.

To implement a four digit tachometer, the ICM7207A with one second gating should be used. To get the display to read directly in RPM, the rotational frequency of the object to be measured must be multiplied by 60. This can be done electronically using a phase-locked loop, or mechanically by using a disc rotating with the object with the appropriate number of holes drilled around its edge to interrupt the light from an LED to a photo-dector. For faster updating, use 0.1 second gating, and multiply the rotational frequency by 600.

Figure 11: Precision Frequency Counter

7. INEXPENSIVE FREQUENCY COUNTER/ TACHOMETER (Figure 12)

This circuit uses an inexpensive 556 dual timer rather than an ICM7027A to generate the gating, $\overline{\text{store}}$ and $\overline{\text{reset}}$ signals. To provide the gating signal, one timer is configured as an astable multivibrator, using R_A, R_B and C to provide an output that is positive for approximately 1 second and negative for approximately 300-500μS. The gating positive time is given by $G_L = 0.693\ (R_A + R_B)\ C$ while the gating low time is $G_L = 0.693 R_B C$. The system is calibrated by using a 5MΩ potentiometer for R_A as a "coarse" control and a 1k potentiometer for R_B as a "fine" control. The other timer in the 556 is configured as a one-shot triggered by the negative-going edge of the gating signal. This one-shot output is inverted to serve as the $\overline{\text{store}}$ pulse and to hold $\overline{\text{reset}}$ high. When the one-shot times out and $\overline{\text{store}}$ goes high, $\overline{\text{reset}}$ goes low, resetting the counter for the next measurement. The one-shot pulse width will be approximately 50μs with the component values shown. When "fine" trimming the gating signal with R_B, care should be taken to keep the gating low time (= $0.693 R_B C$) at least twice as long as the one-shot pulse width.

Figure 12: Inexpensive Frequency Counter

8. INEXPENSIVE CAPACITANCE METER (Figure 13)

This circuit uses two 555 timers (or one 556) to generate a gated count to the ICM7217 dependent on the value of an arbitrary capacitor. The clock timer operates as a fixed oscillator whose output period is determined by R_1, R_2 and C (which is switched with the range). The relation is $T_{CL} = 0.693\ (R_1 + 2R_2)\ C$. The gating timer also operates as an oscillator, but its output high time (and period) is determined by the value of the measured capacitor in combination with R_3 and R_4 (also switched with range). The output high time of this timer is given by $G_H = 0.693\ (R_3 + R_4)\ Cm$. The number of clock pulses during one gating time is thus given by

$$N = \frac{(R_3 + R_4)\ Cm}{(R_1 + 2R_2)\ C}$$

With the values shown, this number is ten times the number to be displayed when the circuit is calibrated. This allows the use of a dummy divide by 10 (the CD4017) to eliminate jitter in the least significant digit of the display. The R_3 resistors should be precision potentiometers for greatest accuracy, and the circuit must be calibrated in each range. Range A reads 1-9999pF, Range B reads 1-9999nF, and Range C reads 1-9999μF.

Note that in comparison to Fig. 12, the $\overline{\text{store}}$ and $\overline{\text{reset}}$ signals are generated by CD4000 series one-shots. The operation of the two circuits is similar.

Figure 13: Capacitance Meter

9. LCD DISPLAY INTERFACE (Figure 14)

The low-power operation of the ICM7217 makes an LCD interface desirable. The Siliconix CF411 4 digit BCD to LCD display driver easily interfaces to the ICM7217A with one CD4000-series package to provide a total system power consumption of less than 5mW. The common-cathode devices should be used, since the digit drivers are CMOS, while the common-anode digit drivers are NPN devices and will not provide full logic swing.

Figure 14: LCD Display Interface

10. MICROPROCESSOR INTERFACE-ICM7227 (Figure 15)

This circuit shows the hardware necessary to interface the ICM7227 to an Intersil IM6100 CMOS microprocessor. Using an IM6101 Parallel Interface Element (PIE) allows the addition of one or more ICM7227 devices as generalized peripherals to any IM6100 system, using a minimum of external components.

A similar configuration may be used with the MC6800 using the corresponding PIE, while an 8223 can be used to interface 8080 based systems.

The ICM7227 can perform many "accessory" functions that are inefficient or impossible for the processor to perform. For simple systems, the ICM7227 can provide a cost-effective display latch/decoder/driver. By adding a timebase such as an ICM7213, and using an ICM7227C or D, an inexpensive real-time clock/display, directly accessible by the processor, can be implemented.

In the area of "intelligent" instrumentation, the ICM7227 can serve as a high speed (up to 2MHz) counter/comparator. This is the element often used for converting time, frequency, and positional and occurence data into digital form. For example, an ICM7207A can be used with two ICM7227's to provide an 8 digit, 2MHz frequency counter.

Since the ICM7207A gating output has a 50% duty cycle, there is 1 second for the processor to respond to an interrupt, generated by the negative going edge of this signal while it inhibits the count. The processor can respond to the interrupt using ROM based subroutines, to store the data, reset the counter, and read the data into main memory. To add simultaneous period display, the processor inverts the data and an ICM7218 Universal Display Driver stores and displays it. Capacitance can be measured by counting the frequency of an oscillator, as in the Capacitance Meter circuit, allowing the measurement of fluid levels, proximity detectors, etc.

Future Application Notes and Bulletins will address the ICM7227 more fully, and users are welcome to submit any circuits or unique uses for review and possible publication in application information.

Figure 15: IM6100 Interface

OPTION MATRIX & ORDERING INFORMATION

	Order Part Number	Display Option	Count Option Max Count	28-LEAD Package
Hardwired Control Versions	ICM7217IJI	Common Anode	Decade/9999	CERDIP
	ICM7217AIPI	Common Cathode	Decade/9999	PLASTIC
	ICM7217BIJI	Common Anode	Timer/5959	CERDIP
	ICM7217C	Common Cathode	Timer/5959	PLASTIC
Processor Control Versions	ICM7227IJI	Common Anode	Decade/9999	CERDIP
	ICM7227AIPI	Common Cathode	Decade/9999	PLASTIC
	ICM7227BIJI	Common Anode	Timer/5959	CERDIP
	ICM7227CIPI	Common Cathode	Timer/5959	PLASTIC

PACKAGE DIMENSIONS

6

INTERSIL

ICM7224 (LCD)
ICM7225 (LED)
4½ Digit Counter/Decoder/Drivers

FEATURES

- **High frequency counting - guaranteed 15MHz, typically 25MHz at 5V**
- **Low power operation - less than 100μW quiescent**
- **Direct 4 1/2 digit seven-segment display drive - ICM7224 for LCD displays, ICM7225 for LED displays**
- **Store and Reset inputs permit operation as frequency or period counter**
- **True count inhibit disables first counter stage**
- **Carry output for cascading four-digit blocks**
- **Schmitt-trigger on the count input allows operation in noisy environments or with slowly changing inputs**
- **Leading zero blanking input and output for correct leading zero blanking with cascaded devices**
- **LCD devices provide complete onboard oscillator and divider chain to generate backplane frequency, or backplane driver may be disabled allowing segments to be slaved to a master backplane signal**
- **LED devices provide Brightness input which can function digitally as a display enable or with a single potentiometer as a continuous display brightness control**
- **All inputs fully protected against static discharge - no special handling precautions necessary**

DESCRIPTION

The ICM7224 and ICM7225 devices constitute a family of high-performance CMOS 4 1/2-digit counters, including decoders, output latches, display drivers, count inhibit, leading zero blanking, and reset circuitry.

The ICM7224 (19999 maximum count) and ICM7224A (15959 maximum count) provide 29 segment outputs and a backplane driver output, generating the zero dc component signals necessary to drive a conventional 4 1/2 digit liquid crystal display. These devices also include a complete RC oscillator and divider chain to generate the backplane frequency, and a backplane driver disable control which allows the segments to be slaved to a master backplane signal.

The ICM7225 (19999 maximum count) and ICM7225A (15959 maximum count) provide 28 segment and 1 half-digit open-drain n-channel transistor outputs, suitable for directly driving common-anode LED displays at greater than 5mA per segment. These devices provide a brightness input which may be used digitally as a display enable, or with a potentiometer as a continuous display brightness control.

The counter section of all the devices in the ICM7224/ICM7225 family provides direct static counting from DC to 15 MHz, guaranteed, with a 5V ±10% supply over the operating temperature range. At normal ambient temperatures, the devices will typically count up to 25 MHz. The count input is provided with a Schmitt trigger to allow operation in noisy environments and correct counting with slowly changing inputs. These devices also provide count inhibit, store and reset circuitry which allows a direct interface with the ICM7207/A devices to implement a low cost, low power frequency counter with a minimum component count.

These devices also incorporate several features intended to simplify cascading four-digit blocks. The carry output allows the counter to be cascaded, while the leading zero blanking input and output allows correct leading zero blanking between four-decade blocks. The backplane driver of the LCD devices may be disabled, allowing the segments to be slaved to another backplane signal, which is necessary when using an eight or twelve digit, single backplane display. In LED systems, the brightness input to several ICM7225 devices may be ganged to one potentiometer.

All the devices in the ICM7224/ICM7225 family are packaged in a standard 40-pin dual-in-line plastic package.

Table 1, the option matrix and ordering information, shows the four standard devices in the ICM7224/ICM7225 family and their markings, which serve as part numbers for ordering purposes.

6

CHIP TOPOGRAPHY

OPTION MATRIX AND ORDERING INFORMATION TABLE 1

	ORDER PART NUMBER	COUNT OPTION
LCD DISPLAY	ICM7224 IPL	19999
	ICM7224A IPL	15959
LED DISPLAY	ICM7225 IPL	19999
	ICM7225A IPL	15959

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5 Watt @ 70° C
Supply Voltage (V^+-V^-) ..... 6.5 Volts
Input Voltage (Any Terminal) (Note 2) ..... V^+ +0.3V, V^- −0.3V
Operating Temperature Range ..... −20° C to +70° C
Storage Temperature Range ..... −55° C to +125° C

Absolute maximum ratings define stress limitations which, if exceeded, may permanently damage the device. These are not continuous duty ratings. For continuous operation these devices must be operated under the conditions defined under "Operating Characteristics."

OPERATING CHARACTERISTICS TABLE 2

(All Parameters measured with V^+-V^- = 5V unless otherwise indicated)

ICM7224 CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current	I_{op}	Test circuit, Display blank		10	50	μA
Operating supply voltage range	V_s	V^+-V^-	3	5	6	V
Oscillator input current	I_{OSL}	Pin 36		±2	±10	μA
Segment rise/fall time	t_{rfs}	C_{load} = 200pf		0.5		μs
Backplane rise/fall time	t_{rfb}	C_{load} = 5000pf		1.5		μs
Oscillator frequency	f_{osc}	Pin 36 Floating		16		KHz
Backplane frequency	f_{bp}	Pin 36 Floating		125		Hz

ICM7225 CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating current display off	I_{OPQ}	Pin 5 (Brightness) at V^- Pins 29, 31-34 at V^+		10	50	μA
Operating supply voltage range	V_s	V^+-V^-	4	5	6	V
Operating current	I_{OP}	Pin 5 at V^+, Display 18888		200		mA
Segment leakage current	I_{SL}	Segment Off		±0.01	±1	μA
Segment on current	I_S	Segment On, Vout = V^- + 3V	5	8		mA
Half digit on current	I_H	Half digit on, Vout = V^- + 3V	10	16		mA

FAMILY CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Pullup Currents	I_{PU}	Pins 29, 31, 33, 34 Vout = V^+- 3V		10		μA
Input High Voltage	V_{IH}	Pins 29, 31, 33, 34	3			V
Input Low Voltage	V_{IL}	Pins 29, 31, 33, 34			2	V
Count Input Threshold	V_{CT}			2		V
Count Input Hysteresis	V_{CH}			0.5		V
Output High Current	I_{OH}	Carry Pin 28 Leading Zero Out Pin 30 Vout = V^+ −3V	350	500		μA
Output Low Current	I_{DL}	Carry Pin 28 Leading Zero Out Pin 30 Vout = V^- +3V	350	500		μA
Count Frequency	f_{count}	4.5V > (V^+-V^-) > 6V	0		15	MHz
Store, Reset Minimum Pulse Width	t_S,t_R		3			μs

NOTE 1: This limit refers to that of the package and will not be obtained during normal operation.

NOTE 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than V^+ or less than V^- may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7224/ICM7225 be turned on first.

TYPICAL CHARACTERISTICS

OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

BACKPLANE FREQUENCY AS A FUNCTION OF OSCILLATOR CAPACITOR COSC

BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE

OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE

6

CONTROL INPUT DEFINITIONS

In this table, V^+ and V^- are considered to be normal operating input logic levels. Actual input low and high levels are specified in Table 2. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	VOLTAGE	FUNCTION
Leading Zero Input	29	V^+ or Floating V^-	Leading Zero Blanking Enabled Leading Zeroes Displayed
Count Inhibit	31	V^+ or Floating V^-	Counter Enabled Counter Disabled
Reset	33	V^+ or Floating V^-	Inactive Counter Reset to 0000
Store	34	V^+ or Floating V^-	Output Latches not Updated Output Latches Updated

BLOCK DIAGRAMS

ICM7224 (A)

ICM7225 (A)

6

CONNECTION DIAGRAMS

TEST CIRCUIT

SEGMENT ASSIGNMENT

DISPLAY WAVEFORMS

DESCRIPTION OF OPERATION

LCD Devices

The LCD devices in the family (ICM7224 and ICM7224A) provide outputs suitable for driving conventional four digit by seven segment LCD displays, including 29 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p- channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any dc component which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the oscillator input (pin 36) to the negative supply. This allows the 29 segment outputs to be synchronized directly to a signal input at the BP terminal (pin 5). In this manner, several slave devices may be cascaded to the backplane output of one master device or the backplane may be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device will represent a load of approximately 200 pF (comparable to one additional segment). The limitation on how many devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits, and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimize power consumption is to keep the rise and fall times less than about 5 microseconds. The backplane driver devices of one device should handle the backplane to a display of 16 one-half-inch characters without the rise and fall times exceeding 5μs (ie, 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM7224 devices be slaved to it.

This external signal should be capable of driving very large capacitive loads with short (1-2 μs) rise and fall times. The maximum frequency for a backplane signal should be about 125Hz, although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 16KHz at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 125Hz with the oscillator free-running. The oscillator frequency may be reduced by connecting an external capacitor to the oscillator terminal (pin 36); see the plot of oscillator/backplane frequency vs. external capacitance for detailed information.

The oscillator may also be overdriven if desired, although care must be taken to insure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a d.c. component to the display). This

can be done by driving the oscillator input between the positive supply and a level out of the range where the backplane disable is sensed, about one fifth of the supply voltage above the negative supply. Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

LED Devices

The LED devices in the family (ICM7225, ICM7225A) provide outputs suitable for directly driving four digit by seven segment common-anode LED displays, including 28 individual segment drivers and one half-digit driver, each consisting of a low-leakage current-controlled open-drain n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the Brightness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Fig (3). The potentiometer should be a high value (100kΩ to 1MΩ) to minimize I^2R power consumption, which can be significant when the display is off.

The brightness input may also be operated digitally as a display enable; when at V^+, the display is fully on, and at V^- fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two supplies at the Brightness input.

Note that the LED devices have two connections for V^-; both of these pins should be connected to the negative supply. The double connection is necessary to minimize effects of bond wire resistance with the large total display currents possible.

When operating the LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (−15mW/°C above 35°C). Power dissipation for the device is given by:

$$P = [(V^+ - V^-) - V_{FLED}] \times I_S \times N_S$$

where V_{FLED} is the LED forward voltage drop, I_S is segment current, and N_S is the number of "on" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the Brightness input to keep power dissipation within the limits described above.

Figure 3: Brightness Control

COUNTER SECTION

The devices in the ICM7224/ICM7225 family implement a four digit ripple carry resetable counter, including a Schmitt trigger on the count input and a carry output. Also included is an extra D-type flip-flop, clocked by the carry signal and outputting to the half-digit segment driver, which can be used as either a true half-digit or as an overflow indicator. The counter will index on the negative-going edge of the signal at the count input, and the carry output will provide a negative-going edge following the count which indexes the counter from 9999 (or 5959) to 10000. Once the half-digit flip-flop has been clocked, it can only be reset (with the rest of the counter) by a negative level at the Reset terminal, pin 33. However, the four decades will continue to count in a normal fashion after the half digit is set, and subsequent carry outputs will not be affected.

A negative level at the Count Inhibit input disables the first divide-by-two in the counter chain without affecting its clock. This provides a true count inhibit which is not sensitive to the state of the count input, preventing false counts which can result from using a normal logic gate forcing the state of the clock to prevent counting.

Each decade of counter drives directly into a four-to-seven decoder which derives the seven segment output code. Each decoder output corresponds to one segment terminal of the device. The output data is latched at the driver; when the Store pin is at a negative level, these latches are updated, and when the Store pin is left open or at a positive level, the latches hold their contents.

The decoders also include zero detect and blanking logic to provide leading zero blanking. When the leading zero input is floating or at a positive level, this circuitry is enabled and the device will blank leading zeroes. When the leading zero input is at a negative level, or the half digit is set, leading zero blanking is inhibited, and zeroes in the four digits will be displayed. The leading zero output is provided to allow cascaded devices to blank leading zeroes correctly. This output will assume a positive level only when all four digits are blanked, which can only occur when the leading zero input is at a positive level and the half digit is not set.

For example in an eight-decade counter with overflow using two ICM7224/ICM7225 devices, the leading zero output of the high order digit device would be connected to the leading zero input of the low order digit device. This will assure correct leading zero blanking for all eight digits.

The Store, Reset, Count Inhibit, and Leading Zero inputs are provided with pullup devices, so that they may be left open when a positive level is desired. The Carry and Leading Zero outputs are suitable for interfacing to CMOS logic in general, and are specifically designed to allow cascading of ICM7224 or ICM7225 devices in four digit blocks.

MAXIMUM COUNT FREQUENCY (TYPICAL) AS A FUNCTION OF SUPPLY VOLTAGE

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SUPPLY CURRENT
AS A FUNCTION OF
COUNT FREQUENCY

APPLICATIONS

1. Two-Hour Precision Timer

2. Eight-Digit Precision Frequency Counter

3. Unit Counter

PACKAGE DIMENSIONS

40 Pin Plastic Dual-In-Line Package

INTERSIL

ICM7209
CMOS Clock Generator

FEATURES

- High frequency operation — 10MHz guaranteed
- Easy to use oscillator — requires only a quartz crystal and two capacitors
- Bipolar, MOS and CMOS compatibility
- High output drive capability — 5 x TTL fanout with 10nS rise and fall times
- Low power — 50mW at 10MHz
- Choice of two output frequencies — osc. plus osc. ÷8 frequencies
- Disable control for both outputs
- Wide industrial temperature range — −20°C to +70°C
- All inputs fully protected — circuits may be handled without any special precautions

GENERAL DESCRIPTION

The Intersil ICM7209 is a versatile CMOS clock generator capable of driving many 5 volt systems, having a variety of input requirements. When used to drive a fanout of 5 TTL gates the typical rise and fall times are 10nS.

The ICM7209 consists of an oscillator, a buffered output and a second buffered output having an output frequency one-eighth that of the oscillator. The guaranteed maximum oscillator frequency is 10MHz. Connecting the DISABLE terminal to the negative supply forces the ÷8 output into the '0' state and the output 1 into the '1' state.

SCHEMATIC DIAGRAM

*ZENER VOLTAGE IS TYPICALLY 6.3 VOLTS

ORDERING INFORMATION

Order Devices by Following Part Number – ICM7209 I PA

Order Dice by Following Part Number – ICM7209 D

CONNECTION DIAGRAM

TOP VIEW

Pin 1 is designated by either a dot or a notch.

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (25°C) 300mW
Supply Voltage ..... 6 volts
Output Voltages ..... Equal to or less than supplies
Input Voltages ..... Equal to or less than supplies
Storage Temp. ..... −55°C to +125°C
Operating Temp. Range ..... −20°C to +70°C

NOTE: Absolute maximum ratings define parameter limits that if exceeded may permanently damage or change the device.

TYPICAL OPERATING CHARACTERISTICS

TEST CONDITIONS: $V^+ - V^- = 5V \pm 10\%$, test circuit, $f_{osc} = 10MHz$, $T_A = 25°C$ unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP.	MAX	UNITS
Supply Current	I^+	Note 1 No Load		11	20	mA
Disable Input Capacitance	C_D				5	pf
Disable Input Leakage	I_D	Either '1' or '0' state			±10	μA
Output Low State	V_{OL}	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads			0.4	V
Output High State	V_{OH}	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads	4.0	4.9		
Output Rise Time (Note 3)	t_r	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads		10	25	nS
Output Fall Time (Note 3)	t_f	Either OUT 1 or OUT ÷8 simulated 5 x TTL loads		10	25	
Minimum OSC Frequency for ÷8 Output	f_{min}	Note 2	2			MHz
Output ÷8 duty cycle	D cycle	Any operating frequency Low state : High state		7:9		

NOTE 1: The power dissipation is a function of the oscillator frequency (1st ORDER EFFECT see curve) but is also effected to a small extent by the oscillator tank components.

NOTE 2: The ÷8 circuitry uses a dynamic scheme. As with any dynamic system whereby information or data is stored on very small nodal capacitances instead of latches (static systems) there is a lower cutoff frequency of operation. Dynamic dividers are used in the ICM7209 to significantly improve high frequency performance and to decrease power consumption.

NOTE 3: Rise and fall times are defined between the output levels of 0.5 and 2.4 volts.

TEST CIRCUIT

TYPICAL OPERATING CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY

TYPICAL OUT 1 RISE AND FALL TIMES

SUPPLY VOLTAGE RANGE FOR CORRECT OPERATION OF ÷8 COUNTER AS A FUNCTION OF OSCILLATOR FREQUENCY

Rise and fall times of OUT ÷8 are similar to those of OUT 1.

APPLICATION NOTES

OSCILLATOR CONSIDERATIONS

The oscillator consists of a C-MOS inverter having a non-linear resistor connected between the oscillator input and output to provide D.C. biasing. Using commercially obtainable quartz crystals the oscillator will operate from low frequencies (10KHz) to approximately 20MHz. However although the oscillator may operate to 20MHz the buffer to the divide by 8 and the OUT 1 is frequency limited to slightly in excess of 10MHz.

The oscillator circuit consumes about 500μA of current using a 10MHz crystal with a 5 volt supply, and is designed to operate with a high impedance tank circuit. It is therefore necessary that the quartz crystal be specified with a load capacitance (C_L) of 10pF instead of the standard 30pf. To maximize the stability of the oscillator as a function of supply voltage and temperature the motional capacitance of the crystal should be low (5mpf or less). Using a fixed oscillator input capacitor of 18pf and at the oscillator output a variable capacitor of nominal value of 18pf and at the oscillator output a variable capacitor of nominal value of 18pf will result in oscillator stabilities of typicaly 1ppm per one volt change in supply voltage.

THE ÷8 OUTPUT

A dynamic divider is used to divide the oscillator frequency by 8 for the ÷8 output. Dynamic dividers use small nodal capacitances to store voltage levels instead of latches which are used in static dividers. The dynamic divider has advantages in high speed operation and low power but suffers from limited low frequency operation. This results in a window of operation for any oscillator frequency (see graph under TYPICAL OPERATING CHARACTERISTICS).

OUTPUT DRIVERS

The output drivers consists of C-MOS inverters having active pullups and pulldowns. Thus the outputs can be used to drive directly TTL gates, other C-MOS gates operating with a 5 volt supply, or TTL compatible MOS gates.

The guaranteed fanout is 5 TTL loads although typically fanout capability is at least 10 TTL loads with slightly increased output rise and fall times.

COMMENTS ON THE DEVICE POWER CONSUMPTION

At low frequencies the principal component of the power consumption is due to the oscillator. At high oscillator frequencies the major portion of the power is consumed by the output drivers, thus by disabling the outputs (activating the DISABLE INPUT) the device power consumption can be dramatically reduced.

CHIP TOPOGRAPHY

PADS 4.2 x 4.2 MILS^2
(.107 mm x .107 mm)

Chip may be die attached using conventional enteric or epoxy procedures. Wire bonding may be either Aluminum ultrasonic or Gold compression.

PACKAGE DIMENSIONS

8 LEAD PLASTIC DIP

NOTE: Board drilling dimensions will equal standard practices for .020 diameter lead.

6

INTERSIL

ICM7213 CMOS One Second/One Minute Precision Clock And Reference Generator

FEATURES

- **Guaranteed 2 volts operation**
- **Very low current consumption: Typ. 100μA @ 3V**
- **All outputs TTL compatible**
- **On chip oscillator feedback resistor**
- **Oscillator requires only 3 external components: fixed capacitor, trim capacitor, and a quartz crystal**
- **Output inhibit function**
- **4 outputs: one pulse/sec, one pulse/min, 16Hz and composite 1024 + 16 + 2 Hz outputs**
- **Test speed-up: provides other frequency outputs**
- **Input static protection — no special handling required**

GENERAL DESCRIPTION

The ICM7213 is a fully integrated micropower oscillator and frequency divider with four buffered outputs suitable for interfacing with most logic families. The power supply may be either a two battery stack (Ni-cad, alkaline, etc.) or a regular power supply greater than 2 volts. Depending on the states of the 'TEST POINT' and 'INHIBIT' inputs and using a 4.194,304MHz quartz crystal oscillator a variety of output frequencies (including composite frequencies) may be obtained including 2048Hz, 1024Hz, 34.133Hz, 16Hz, 1Hz and 1/60Hz.

The ICM7213 utilizes a very high speed low power metal gate C-MOS technology which results in there being 6.4 volt zeners (typical value) between the drains and sources of each transistor and also across the supply terminals. Consequently, the ICM7213 is limited to 6 volt maximum supply voltage, although a simple dropping network can be used to extend the supply voltage range well above 6 volts (see Figure 2).

Applications for the ICM7213 include precision timers, frequency references and frequency counter timebases.

The ICM7213 may be obtained in a 14 lead plastic dual in line or as dice.

CONNECTION DIAGRAM

CHIP TOPOGRAPHY

Chip may be die attached using conventional eutetic or epoxy procedures. Wire bonding may be either aluminum ultrasonic or gold compression.

ORDERING INFORMATION

ICM7213 1 PD Plastic

- Package — See Outline Drawing
- Temperature Range — −20°C to +70°C
- Type

Order Devices by Following Part Number
ICM7213 1 PD

Order Dice by Following Part Number
ICM7213D

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V^+ - V^-) ..... 6.0 Volts
Output Current (Any output) 20mA
All Input and Oscillator Voltages (Note 1) ..... Equal to but not greater
(Terminals 1, 3, 5, 6, 11) ..... than the supply voltage
All Output Voltages (Note 1) ..... Not greater than +6 volts with respect to,
(Terminals 2, 12, 13, 14) nor less than, the negative supply (terminal 4.)
Operating Temperature Range ..... −20°C to +70°C
Storage Temperature Range ..... −40°C to +125°C
Power Dissipation (Note 2) 200mW

Absolute maximum ratings define parameter limits that if exceeded may permanently damage or change the device.

OPERATING CHARACTERISTICS

TEST CONDITIONS: V^+ - V^- = 3.0V, f_{osc} = 4.194304 MHz, Test Circuit, T_A = 25°C unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Supply Current	I^+			100	140	μA
Guaranteed Operating Supply Voltage Range	V_{SUPP}	−20°C < T_A < +70°C	2		4	Volts
Typical Operating Supply Voltage Range	V_{SUPP}	−20°C < T_A < +70°C	1.4		5	Volts
Output Leakage Current	I_L	Any output, V_{OUT} = 6 Volts, (Note 3)			10	μA
Output Sat. Resistance	R_{OUT}	Any output, I_L = 2.5mA		120	200	Ohms
Inhibit Input Current	I_R	Inhibit terminal connected to V_{DD}		10	40	μA
Test Point Input Current	I_{TP}	Test point terminal connected to V^+		10	40	μA
Width Input Current	I_W	Width terminal connected to V_{DD}		10	40	μA
Oscillator g_m	g_m	V^+ - V^- = 2V	100			umho
Typical Oscillator Frequency Range	f_{osc}	(NOTE 4)	1		10	MHz
Oscillator Stability	f_{STAB}	2V < (V^+ - V^-) < 4V, (NOTE 5)		1.0		ppm
Oscillator Start Time	t_s	V^+ - V^- = 3.0 volts		0.1		sec
		V^+ - V^- = 2.0 volts		0.2		sec

NOTE 1: The ICM7213 and most C-MOS devices have a destructive latchup mode if an input or output voltage is applied in excess of those defined and there is no supply current limiting.
NOTE 2: Derate linearly power rating of 200 mW at 25° to 50mW at 70°C.
NOTE 3: Leakage current in the output transistors is due to the inherent characteristics of an MOS transistor operating below threshold voltage in the expoential region of their characteristic. See "Ion-implanted C-MOS Transistors in Low Voltage Circuits", Swanson and Meindl, IEEE Journal of Solid State Circuits, April 1972.
NOTE 4: The ICM7213 uses dynamic dividers for high frequency division. As with any dynamic system, information is stored on very small nodal capacitances instead of latches (static system), therefore, there is a lower frequency of operation. Dynamic dividers are used to improve the high frequency performance while at the same time significantly decreasing power consumption. At low supply voltages, operation at less than 1MHz is possible. See application notes.
NOTE 5: The actual oscillator stability obtained will depend on the parameters of the quartz crystal and the value of the tuning capacitors. The value given therefore relates only to conditions given in the test circuit.
NOTE 6: When TP and RESET are open circuit or connected to V_{SS}, all outputs are 50% duty cycle except OUT 3 and OUT 4.

TEST CIRCUIT

OUTPUT DEFINITIONS (NOTE 6)

INPUT STATES*						
TP	INHIBIT	WIDTH	OUT 1	OUT 2	OUT 3	OUT 4
L	L	L	16Hz $\div 2^{18}$	$\overline{1024 + 16 + 2}$Hz ($\div 2^{12} \div 2^{18} \div 2^{21}$) composite	1Hz, 7.8mS $\div 2^{22}$	1/60Hz, 1 sec $\div(2^{26} \times 3 \times 5)$
L	L	H	16Hz $\div 2^{18}$	$\overline{1024 + 16 + 2}$Hz ($\div 2^{12} \div 2^{18} \div 2^{21}$) composite	1Hz, 7.8mS $\div 2^{24}$	1/60Hz, 125mS
L	H	L	16Hz $\div 2^{18}$	$\overline{1024 + 16}$Hz ($\div 2^{12} \div 2^{18}$) composite	OFF	OFF
L	H	H	16Hz $\div 2^{18}$	$\overline{1024 + 16}$Hz ($\div 2^{12} \div 2^{18}$) composite	OFF	SEE WAVEFORMS
H	L	L	ON	$\overline{4096 + 1024}$Hz ($\div 2^{10} \div 2^{12}$) composite	2048Hz $\div 2^{11}$	34.133Hz, 50% D.C. $\div 2^{13} \times 5 \times 3$)
H	L	H	ON	$\overline{4096 + 1024}$Hz ($\div 2^{10} \div 2^{12}$) composite	2048Hz $\div 2^{11}$	34.133Hz, 50% D.C. $\div(2^{13} \times 5 \times 3)$
H	H	L	ON	1024Hz $\div 2^{12}$	ON	ON
H	H	H	ON	1024Hz $\div 2^{12}$	ON	ON

* L denotes input open circuit or connected to V_{SS}
H denotes input connected to V_{DD}

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SIMPLIFIED BLOCK SCHEMATIC

OUTPUT WAVEFORMS

EFFECT OF INHIBIT INPUT (T.P. connected to V_{SS} or open circuit)

All time scales are arbitrary, and in the case of OUT 3 only the pulses coinciding with the negative edge of OUT 4 are shown. Where time intervals are relevant they are clearly shown.

SUPPLY CURRENT AS A FUNCTION OF TEMPERATURE

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

OSCILLATOR STABILITY AS A FUNCTION OF DEVICE TEMPERATURE

OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE

OUTPUT CURRENT AS A FUNCTION OF OUTPUT SATURATION VOLTAGE

DEVICE DESCRIPTION

The oscillator consists of a C-MOS inverter with a non-linear high value resistor connected between the OSC IN and OSC OUT terminals. The initial divider chain (2^9) consists of both dynamic (highest frequency) and static dividers. All other dividers are static.

The input designated TP inhibits the 2^{18} output and takes the 2^9 output and applies it to the 2^{21} divider, thereby permitting a speedup of the teting of the ÷60 section by a factor of 2048 times. This also results in alternative output frequencies (see table).

The WIDTH input may be used to change the pulse width of OUT 4 from 125 mS to 1 sec or, to change the state of OUT 4 from ON to OFF during INHIBIT (if OUT 4 is ON upon application of an inhibit signal).

APPLICATIONS

1. Supply Voltage Considerations

The ICM7213 may be used to provide various precision outputs having frequencies from 2048Hz to 1/60Hz using a 4.194,304Hz quartz oscillator. Other output frequencies may be obtained using other quartz crystal frequencies. Since the ICM7213 uses dynamic high frequency dividers for the initial frequency division there are limitations on the supply voltage range depending on the oscillator frequency. If for example a low frequency quartz crystal is selected the supply voltage should be selected in the center of the operating window, or approximately 1.7 volts.

FIGURE 1: Window of Correct Operation

The supply voltage to the ICM7213 may be derived from a high voltage supply by using a simple resistor divider (if power is of no concern), by using a series resistor for minimum current consumption, or by means of a regulator.

2. Logic Family Compatibility

Pull up resistors will generally be required to interface with other logic families. These resistors must be connected between the various outputs and a positive power supply with respect to V_{SS}.

3. Oscillator Considerations

The oscillator consists of a C-MOS inverter and a feedback resistor whose value is dependent on the voltage at the oscillator input and output terminals and the supply voltage. Oscillator stabilities of approximately 0.1ppm per 0.1 volt variation are achievable with a nominal supply voltage of 5 volts, and a single voltage dropping resistor. The crystal specifications are shown in the TEST CIRCUIT.

It is recommended that the crystal load capacitance (CL) be no greater than 22 pf for a crystal having a series resistance equal to or less than 75 ohms, otherwise the output amplitude of the oscillator may be too low to drive the divider reliably.

If a very high quality oscillator is desired, it is recommended that a quartz crystal be used having a tight tuning tolerance ±10ppm, a low series resistance (less than 25 ohms), a low motional capacitance of 5mpf and a load capacitance of 20pf. The fixed capacitor C_{IN} should be 30 pf and the oscillator tuning capacitor should range between approximately 16 and 60 pf.

Use of a high quality crystal will result in typical stabilities of 0.05ppm per 0.1 volt change of supply voltage.

4. C-MOS Latchup Considerations

A destructive latchup mode is possible if an input or output is forward biased with respect to either the positive or negative supplies. Example: if the oscillator output terminal is taken sufficiently negative with respect to V_{SS} or positive with respect to V_{DD} so that many milliamperes of current are forced to flow into/from this terminal, the device may present an extremely low impedance across its supply terminals V_{DD} and V_{SS} causing very high values of current to be drawn from the supply which can cause device failure.

If the supply current is limited to less than 20mA maximum the device may return to its normal operating state after an inadvertent input transient. It is, therefore, recommended that a supply series resistor and bypass capacitor be used in the breadboarding stage of a design, where mistakes can be made.

FIGURE 2: Biasing Schemes with High Voltage Supplies

PACKAGE DIMENSIONS

INTERSIL

ICM7207 CMOS Oscillator Controller

FEATURES

- **Stable HF oscillator**
- **Low power dissipation ≤ 5mW with 5 volt supply**
- **Counter chain has outputs at $\div 2^{12}$ and $\div 2^{17}$ or $\div(2^{17} \times 10)$**
- **Low impedance output drivers ≤ 100 ohms**

DESCRIPTION

The ICM7207 consists of a high stability oscillator and frequency divider providing 4 control outputs suitable for frequency counter timebases. Specifically, when used as a frequency counter timebase in conjunction with the ICM7208 frequency counter, the four outputs provide the gating signals for the count window, store function, reset function and multiplex frequency reference. Additionally, the duration of the count window may be changed by a factor of 10 to provide a 2 decade range counting system.

The normal operating voltage of the ICM7207 is 5 volts at which the typical dissipation is less than 2mW using an oscillator frequency of 6.5536MHz.

The ICM7207 is fabricated using Intersil's standard low voltage metal gate C-MOS process which has been used exclusively for all of Intersil's timing products.

Can be used for:

a) System timebase
b) Oscilloscope calibration generator
c) Marker generator strobe
d) Frequency counter controller

CHIP TOPOGRAPHY

Chip may be die attached using conventional eutectic or epoxy procedures. Wire bonding may be either aluminum ultrasonic or gold compression.

CONNECTION DIAGRAM

PACKAGE DIMENSIONS

ORDERING INFORMATION

ORDER DEVICES BY FOLLOWING PART NUMBER ICM 7207 I PD
ORDER DICE BY FOLLOWING PART NUMBER ICM 7207D

6

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6.0V
Input Voltages ..... Equal to or less than supply voltage
Output Voltages ..... Not more positive than +6V with respect to the negative supply V−
Output Currents 25mA
Power Dissipation @ 25°C Note 1 ..... 200mW
Operating Temperature Range ..... −20°C to +70°C
Storage Temperature Range ..... −55°C to +125°C

Absolute maximum ratings refer to values which if exceeded may permanently change or destroy the device.

NOTE 1: Derate by 2mW/°C above 25°C.

TYPICAL OPERATING CHARACTERISTICS

TEST CONDITIONS: f_{osc} = 6.5536MHz, V+ − V− = 5V, T_A = 25°C, test circuit unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage Range	V+ − V−	−20°C to +70°C	4		5.5	V
Supply Current	I_{DD}	All outputs open circuit		260	1000	μA
Output on Resistances	$r_{ds(ON)}$	Output current = 5mA All outputs		50	120	ohms
Output Leakage Currents	I_O	All outputs			50	μA
Input Pulldown Current	I_D	Terminal 11 connected to V+		50	200	μA
Input Noise Immunity	NF		25			% supply voltage
Oscillator	f_r	Note 2	2		10	MHz
Oscillator Stability	f_{STAB}	C_{IN} = C_{OUT} = 22pf		0.2	1.0	ppm/volt
Oscillator Feedback Resistance	R_{osc}	Quartz crystal open circuit Note 3	3			Mohm

NOTE 1: Dynamic dividers are used in the initial stages of the divider chain. These dividers have a lower frequency of operation determined by transistor sizes, threshold voltages and leakage currents.

NOTE 3: The feedback resistor has a non-linear value determined by the oscillator instantaneous input and output voltage voltages and the supply voltage.

BLOCK SCHEMATIC

6

OUTPUT TIMING WAVEFORMS

Referring to the test circuit, the 6.5536MHz oscillator frequency is divided by 2^{12} to provide both the multiplex frequency of 1.6KHz and to generate the duration of the output pulse widths (312μ for OUTPUT 1 and OUTPUT 2.

The GATING OUTPUT provides either a 50Hz or 5Hz 50% duty cycle signal depending upon whether the RANGE CONTROL terminal is connected to V+ or V− (or open circuit).

TEST CIRCUIT

SWITCHES S_1, S_2, S_3, S_4 OPEN CIRCUIT FOR SUPPLY CURRENT MEASUREMENT.
SWITCH S_5 OPEN CIRCUIT FOR SLOW GATING PERIOD.

SUPPLY CURRENT AS A FUNCTION OF OSCILLATOR FREQUENCY

OUTPUT SATURATION RESISTANCES AS A FUNCTION OF SUPPLY VOLTAGE

OSCILLATOR STABILITY AS A FUNCTION OF SUPPLY VOLTAGE

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

APPLICATION NOTES

OSCILLATOR CONSIDERATIONS

The oscillator consists of a C-MOS inverter and uses a non-linear resistor connected between the oscillator input and output terminals to provide biasing. Oscillator stabilities of approximately 0.1ppm per 0.1 volt change are achievable at a supply voltage change at 5 volts, using low cost crystals. The crystal specifications are shown in the TEST CIRCUIT.

It is recommended that the crystal load capacitance (CL) be no greater than 15pf for a crystal having a series resistance equal to or less than 75 ohms, otherwise the output amplitude of the oscillator may be too low to drive the divider reliably.

If a very high quality oscillator is desired, it is recommended that a quartz crystal be used having a tight tuning tolerance ±10 ppm, a low series resistance (less than 25 ohms), a low motional capacitance of 5mpf and a load capacitance of 20pf. The fixed capacitor C_{IN} should be 39pf and the oscillator tuning capacitor should range between approximately 8 and 60 pf.

Use of a high quality crystal will result in typical oscillator stabilities of 0.05 ppm per 0.1 volt change of supply voltage.

FREQUENCY LIMITATIONS

The ICM7207 uses dynamic frequency counters in the initial divider sections. Dynamic frequency counters are faster and consume less power than static dividers but suffer from the disadvantage that there is a minimum operating frequency at a given supply voltage.

For example, if instead of 6.5MHz, a 1MHz oscillator is required it is recommended that the supply voltage be reduced to between 2 and 2.5 volts. This may be realized by using a series resistor in series with the 5V positive supply line plus a decoupling capacitor. The quartz crystal parameters, etc., will determine the value of this resistor. NOTE: Except for the output open drain n-channel transistors no other terminal is permitted to exceed the supply voltage limits.

PRACTICAL FREQUENCY COUNTER

A complete frequency counter using the ICM7207 together with the ICM7208 Frequency Counter is described in the ICM7208 data sheet.

INTERSIL

ICM7207A Complementary MOS Oscillator Controller

FEATURES

- **Stable HF oscillator**
- **Low power dissipation ≤ 5mW with 5 volt supply**
- **Counter chain has outputs at ÷ 2^{12} and ÷ 2^{20} or ÷ (2^{20} x 10)**
- **1 sec and 100 ms count enable outputs**

GENERAL DESCRIPTION

The ICM7207A is pin for pin compatible with the ICM7207 but has an 0.1 second and 1 second count enable window output. When used with the ICM7208 frequency counter, the four outputs provide the gating signals for the count window, store function, reset function and multiplex frequency reference. With the 1 second count enable window it is now possible to obtain 7 significant digits when measuring frequencies over 1 MHz.

The gating output, output 2 and the multiplex output now provide both pull up and pull down, eliminating the need for 3 external resistors. However, buffering must be provided if interfacing with T²L is required. Output 2 occurs 391 μseconds after output 1, eliminating any potential problems of overlap between Store and Reset when using the ICM7208. In addition, a 5.24288 MHz crystal must be used instead of the 6.5536 MHz crystal used with the ICM7207.

The normal operating voltage of the ICM7207A is 5 volts at which the typical dissipation is less than 2mW using an oscillator frequency of 5.24288 MHz.

The ICM7207A is fabricated using Intersil's standard low voltage metal gate CMOS process which has been used exclusively for all of Intersil's timing products.

CONNECTION DIAGRAM

ORDERING INFORMATION

ORDER DEVICES BY FOLLOWING PART NUMBER ICM7207A I PD
ORDER DICE BY FOLLOWING PART NUMBER ICM7207A I D

CHIP TOPOGRAPHY

Chip may be die attached using conventional eutectic or epoxy procedures. Wire bonding may be either aluminum ultrasonic or gold compression.

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TYPICAL OPERATING CHARACTERISTICS

TEST CONDITIONS f_{osc} = 5.24288 MHz; V^+-V^- = 5.0V; T_A = 25°C; test circuit unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Operating Voltage Range	V^+-V^-	−20°C < T_A < 70°C	4		5.5	Volts
Supply Current	I_{DD}	Terminal 2 open circuit		190	1000	μA
Output On Resistance, Terminal 2	r_{ds}	Terminal 2 output current = 5 mA		50	120	Ohms
Output Leakage Current, Terminal 2	I_0	Terminal 2 connected to V^+			20	μA
Output Resistance Terminals 12, 13, 14	r_{ds}	Output current = 50μA			33K	Ohms
Input Pulldown Current	I_D	Terminal 11 connected to V_{DD}		50	200	μA
Oscillator Freq. Range	f_r		2		10	MHz
Osc. Stability	f_{STAB}	C_{IN} = C_{OUT} = 22pF			.2	ppm/Volt

TEST CIRCUIT

QUARTZ CRYSTAL PARAMETERS
f = 5.24288 MHz
R_S < 75Ω
C_O = 4 pF
C_M = 12 mpF
C_L = 12 pF

S1 CLOSED: 5 Hz GATING OUTPUT
S1 OPEN: 0.5 Hz GATING OUTPUT

PACKAGE DIMENSIONS

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INTERSIL

ICM7211 (LCD)
ICM7212 (LED)
Four Digit Display Decoder-Drivers

ICM7211 (LCD) FEATURES

- **Four digit non-multiplexed 7 segment LCD display outputs with backplane driver.**
- **Complete onboard RC oscillator to generate backplane frequency.**
- **Backplane input/output allows simple synchronization of slave-device segment outputs with a master backplane signal.**
- **ICM7211 devices provide separate digit select inputs to accept multiplexed BCD input (Pinout and functionally compatible with Siliconix DF411).**
- **ICM7211M devices provide data and digit select code input latches controlled by chip select inputs to provide a direct high speed processor interface.**
- **ICM7211 device for binary-to-hexadecimal decoding; ICM7211A device for binary-to-EHLP-dash-blank decoding.**

ICM7212 (LED) FEATURES

- **28 current-limited segment outputs provide 4 digit non-multiplexed direct LED drive at > 5mA per segment.**
- **Brightness input allows direct control of LED segment current with a single potentiometer, or can function digitally as a display enable.**

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FAMILY FEATURES

- **All devices fabricated using high density MAX-CMOS™ LSI technology for very low-power, high-performance operation.**
- **All inputs fully protected against static discharge; no special handling precautions necessary.**

DESCRIPTION

THE ICM7211(LCD) and ICM7212(LED) devices constitute a family of non-multiplexed four digit seven segment display decoder-drivers.

The ICM7211 devices are configured to drive conventional LCD displays, by providing a complete (no external components necessary) RC oscillator, divider chain, backplane driver devices, and 28 segment outputs. These outputs provide the zero d.c. component signals necessary for long display life.

The ICM7212 devices are configured to drive common-anode LED displays, providing 28 current-controlled low leakage open-drain n-channel outputs. These devices provide a Brightness input which may be used at normal logic levels as a display enable, or with a potentiometer as a continuous display brightness control.

Both the LCD and LED devices are available with two input configurations. The basic devices provide four data-bit inputs and four digit select inputs. This configuration is suitable for interfacing with multiplexed BCD or binary output devices, such as the ICM7217, ICM7226 and ICL7103. The microprocessor interface (suffix M) devices provide data input latches and digit select code latches under control of high-speed chip select inputs. These devices simplify the task of implementing a cost-effective alphanumeric 7 segment display for microprocessor systems, without requiring extensive ROM or CPU time for decoding and display updating.

The standard devices available will provide two different decoder configurations. The basic device will decode the four bit binary input into a seven-segment alphanumeric hexa-decimal output. The "A" versions will provide the same output code as the ICM7218 "Code B", i.e., 0-9, E, H, L, P, dash, blank. Either device will correctly decode true BCD to seven segment decimal outputs.

All devices in the ICM7211/7212 family are packaged in a standard 40 pin plastic dual-in-line package.

Table 1, the option matrix and ordering information, shows the 8 standard devices of the ICM7211/7212 family and their markings, which serve as part numbers for ordering purposes.

TABLE 1: OPTION MATRIX AND ORDERING INFORMATION

ORDER PART NUMBER		OUTPUT CODE	INPUT CONFIGURATIONS
LCD DISPLAY	ICM7211 IPL ICM7211A IPL	HEXADECIMAL CODE B	MULTIPLEXED 4-BIT
	ICM7211M IPL ICM7211AM IPL	HEXADECIMAL CODE B	MICROPROCESSOR INTERFACE
LED DISPLAY	ICM7212 IPL ICM7212A IPL	HEXADECIMAL CODE B	MULTIPLEXED 4-BIT
	ICM7212M IPL ICM7212AM IPL	HEXADECIMAL CODE B	MICROPROCESSOR INTERFACE

ABSOLUTE MAXIMUM RATINGS

Power Dissipation (Note 1) ..... 0.5 Watt @ 70°C
Supply Voltage (V^+-V^-) ..... 6.5 Volts
Input Voltage (Any Terminal) (Note 2) ..... V^+ +0.3V, V^- −0.3V
Operating Temperature Range ..... −20°C to +70°C
Storage Temperature Range ..... −55°C to +125°C

Absolute maximum ratings define stress limitations which, if exceeded, may permanently damage the device. These are not continuous duty ratings. For continuous operation these devices must be operated under the conditions defined under "Operating Characteristics."

TABLE 2: OPERATING CHARACTERISTICS

All parameters measured with V^+-V^- = 5V

ICM7211 CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_S	V^+-V^-	3	5	6	V
Operating Current	I_{op}	Test circuit, Display blank		10	50	μA
Oscillator Input Current	I_{OSL}	Pin 36		±2	±10	μA
Segment Rise/Fall Time	t_{rfs}	C_{load} = 200pf		0.5		μs
Backplane Rise/Fall Time	t_{rfb}	C_{load} = 5000pf		1.5		μs
Oscillator Frequency	f_{osc}	Pin 36 Floating		16		kHz
Backplane Frequency	f_{bp}	Pin 36 Floating		125		Hz

ICM7212 CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Operating Supply Voltage Range	V_S	V^+-V^-	4	5	6	V
Operating Current Display Off	I_{OPQ}	Pin 5 (Brightness) at V^- Pins 27-34		10	50	μA
Operating Current	I_{OP}	Pin 5 at V^+, Display all 8's		200		mA
Segment Leakage Current	I_{SL}	Segment Off		±0.01	±1	μA
Segment On Current	I_S	Segment On, Vout = V- +3V	5	8		mA

INPUT CHARACTERISTICS

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNIT
Logical "1" input voltage	V_{IH}	Referred to V^-	3			V
Logical "0" input voltage	V_{IL}	Referred to V^-			2	V
Input leakage current	I_{DL}	Pins 27-34		±.01	±1	μA
Input capacitance	C_{in}	Pins 27-34		5		pF
BP/Brightness input leakage	I_{LBPI}	Measured at pin 5 with Pin 36 at V^-		±.01	±1	μA
BP/Brightness input capacitance	C_{BPI}	All Devices		200		pF
AC CHARACTERISTICS - MULTIPLEXED INPUT CONFIGURATION						
Digit Select Active Pulse Width	t_{sa}	Refer to Timing Diagrams	1			μs
Data Setup Time	t_{ds}		500			ns
Data Hold Time	t_{dh}		200			ns
Inter-Digit Select Time	t_{ids}		2			μs
AC CHARACTERISTICS - MICROPROCESSOR INTERFACE						
Chip Select Active Pulse Width	t_{csa}	other chip select either held active, or both driven together	200			ns
Data Setup Time	t_{dsm}		100			ns
Data Hold Time	t_{dhm}		10	0		ns
Inter-Chip Select Time	t_{ics}		2			μs

NOTE 1: This limit refers to that of the package and will not be obtained during normal operation.

NOTE 2: Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to voltages greater than V^+ or less than V^- may cause destructive device latchup. For this reason, it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established, and that in multiple supply systems, the supply to the ICM7211/ICM7212 be turned on first.

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TYPICAL CHARACTERISTICS

OPERATING SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

BACKPLANE FREQUENCY AS A FUNCTION OF OSCILLATOR CAPACITOR COSC

BACKPLANE FREQUENCY AS A FUNCTION OF SUPPLY VOLTAGE

LED SEGMENT CURRENT AS A FUNCTION OF OUTPUT VOLTAGE

LED SEGMENT CURRENT AS A FUNCTION OF BRIGHTNESS CONTROL VOLTAGE

OPERATING POWER (LED DISPLAY) AS A FUNCTION OF SUPPLY VOLTAGE

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CONNECTION DIAGRAMS

BLOCK DIAGRAMS

ICM7211 (A)

ICM7212 (A)

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ICM7211(A)M

ICM7212(A)M

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INPUT DEFINITIONS

In this table, V^+ and V^- are considered to be normal operating input logic levels. Actual input low and high levels are specified in Table 2. For lowest power consumption, input signals should swing over the full supply.

INPUT	TERMINAL	CONDITION	FUNCTION	
B0	27	V^+ = Logical One V^- = Logical Zero	Ones (Least Significant)	Data Input Bits
B1	28	V^+ = Logical One V^- = Logical Zero	Twos	
B2	29	V^+ = Logical One V^- = Logical Zero	Fours	
B3	30	V^+ = Logical One V^- = Logical Zero	Eights (Most significant)	
OSC (LCD Devices Only)	36	Floating or with external capacitor V^-	Oscillator input Disables BP output devices, allowing segments to be synced to an external signal input at the BP terminal (Pin 5)	

ICM7211/ICM7212
MULTIPLEXED-BINARY INPUT CONFIGURATION

INPUT	TERMINAL	CONDITION	FUNCTION
D1	31	V^+ = Active V^- = Inactive	D1 (Least significant) Digit Select
D2	32		D2 Digit Select
D3	33		D3 Digit Select
D4	34		D4 (Most significant) Digit Select

ICM7211M/ICM7212M
MICROPROCESSOR INTERFACE INPUT CONFIGURATION

INPUT	DESCRIPTION	TERMINAL	CONDITION	FUNCTION
DS1	Digit Select Code Bit 1	31	V^+ = Logical One V^- = Logical Zero	DS1 & DS2 serve as a two bit Digit Select Code Input DS1, DS2 = 00 selects D4 DS1, DS2 = 01 selects D3 DS1, DS2 = 10 selects D2 DS1, DS2 = 11 selects D1
DS2	Digit Select Code bit 2	32		
CS1	Chip Select 1	33	V^+ = Inactive V^- = Active	When both CS1 and CS2 are taken to V^-, the data at the Data and Digit Select code inputs are written into the input latches. On the rising edge of either Chip Select, the data is decoded and written into the output latches.
CS2	Chip Select 2	34		

TEST CIRCUIT

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Figure 1: Multiplexed Input Timing Diagram

Figure 2: Microprocessor Interface Input Timing Diagram

Display Waveforms

DESCRIPTION OF OPERATION

LCD Devices

The LCD devices in the family (ICM 7211, 7211A, 7211M, 7211AM) provide outputs suitable for driving conventional four digit by seven segment LCD displays, including 28 individual segment drivers, backplane driver, and a self-contained oscillator and divider chain to generate the backplane frequency.

The segment and backplane drivers each consist of a CMOS inverter, with the n- and p- channel devices ratioed to provide identical on resistances, and thus equal rise and fall times. This eliminates any dc component which could arise from differing rise and fall times, and ensures maximum display life.

The backplane output devices can be disabled by connecting the oscillator input (pin 36) to the negative supply. This allows the 28 segment outputs to be synchronized directly to a signal input at the BP terminal (pin 5). In this manner, several slave devices may be cascaded to the backplane output of one master device or the backplane may be derived from an external source. This allows the use of displays with characters in multiples of four and a single backplane. A slave device will represent a load of approximately 200pF (comparable to one additional segment). The limitation on how many devices that can be slaved to one master device backplane driver is the additional load represented by the larger backplane of displays of more than four digits, and the effect of that load on the backplane rise and fall times. A good rule of thumb to observe in order to minimize power consumption is to keep the rise and fall times less than about 5 microseconds. The backplane driver devices of one device should handle the backplane to a display of 16 one-half-inch characters without the rise and fall times exceeding 5μs. (ie, 3 slave devices and the display backplane driven by a fourth master device). It is recommended that if more than four devices are to be slaved together, that the backplane signal be derived externally and all the ICM 7211 devices be slaved to it. This external signal should be capable of driving very large capacitive loads with short (1-2μs) rise and fall times. The maximum frequency for a backplane signal should be about 125Hz although this may be too fast for optimum display response at lower display temperatures, depending on the display used.

The onboard oscillator is designed to free run at approximately 16KHz at microampere power levels. The oscillator frequency is divided by 128 to provide the backplane frequency, which will be approximately 125Hz with the oscillator free-running. The oscillator frequency may be reduced by connecting an external capacitor to the oscillator terminal (pin 36); see the plot of oscillator/backplane frequency vs. external capacitance for detailed information.

The oscillator may also be overdriven if desired, although care must be taken to insure that the backplane driver is not disabled during the negative portion of the overdriving signal (which could cause a d.c. component to the display). This can be done by driving the oscillator input between the positive supply and a level out of the range where the backplane disable is sensed, about one fifth of the supply voltage above the negative supply. Another technique for overdriving the oscillator (with a signal swinging the full supply) is to skew the duty cycle of the overdriving signal such that the negative portion has a duration shorter than about one microsecond. The backplane disable sensing circuit will not respond to signals of this duration.

LED Devices

The LED devices in the family (ICM 7212, 7212A, 7212M, 7212AM) provide outputs suitable for directly driving four digit by seven segment common-anode LED displays, including 28 individual segment drivers, each consisting of a low-leakage current-controlled open-drain n-channel transistor.

The drain current of these transistors can be controlled by varying the voltage at the Brightness input (pin 5). The voltage at this pin is transferred to the gates of the output devices for "on" segments, and thus directly modulates the transistor's "on" resistance. A brightness control can be easily implemented with a single potentiometer controlling the voltage at pin 5, connected as in Fig (3). The potentiometer should be a high value (100KΩ to 1MΩ) to minimize I^2R power consumption, which can be significant when the display is off.

The brightness input may also be operated digitally as a display enable; when at V^+, the display is fully on, and at V^- fully off. The display brightness may also be controlled by varying the duty cycle of a signal swinging between the two supplies at the Brightness input.

Note that the LED devices have two connections for V^-; both of these pins should be connected to the negative supply. The double connection is necessary to minimize effects of

bond wire resistance with the large total display currents possible.

When operating the LED devices at higher temperatures and/or higher supply voltages, the device power dissipation may need to be reduced to prevent excessive chip temperatures. The maximum power dissipation is 1 watt at 25°C, derated linearly above 35°C to 500mW at 70°C (–15mW/°C above 35°C). Power dissipation for the device is given by:

$$P = [(V^{+}-V^{-})-V_{FLED}] \times I_S \times N_S$$

where V_{FLED} is the LED forward voltage drop, I_S is segment current, and N_S is the number of "on" segments. It is recommended that if the device is to be operated at elevated temperatures the segment current be limited by use of the Brightness input to keep power dissipation within the limits described above.

Figure 3: Brightness control

Input Configurations And Output Codes

The standard devices in the ICM 7211/12 family accept a four-bit true binary (ie, positive level = logical one) input at pins 27 thru 30, least significant bit at pin 27 ascending to the most significant bit at pin 30. The ICM 7211, ICM 7211M, ICM 7212, and ICM 7212M devices decode this binary input into a seven-segment alphanumeric hexadecimal output. The ICM 7211A, ICM 7211AM, ICM 7212A, and ICM 7212AM decode the binary input into the same seven-segment output as in the ICM 7218 "Code B", ie 0-9, E, H, L, P, dash, blank. These codes are shown explicitly in Table 3. Either decoder option will correctly decode true BCD to a seven-segment decimal output.

These devices are actually mask-programmable to provide any 16 combinations of the seven segment outputs decoded from the four input bits. For larger quantity orders, custom decoder options can be arranged. Contact the factory for details.

The ICM7211, ICM7211A, ICM7212, and ICM7212A devices are intended to accept multiplexed binary or BCD output. These devices provide four separate digit lines (least significant digit at pin 31 ascending to most significant digit at pin 34), each of which when taken to a positive level decodes and stores in the output latches of its respective digit the character corresponding to the data at the input port, pins 27 through 30. More than one digit select may be activated simultaneously (which will write the same character into all selected digits), although the timing requirements shown in Fig (1) and Table 2 for data setup, hold, and inter-digit select times must be met to ensure correct output.

The ICM7211M, ICM7211AM, ICM7212M, and ICM7212AM devices are intended to accept data from a data bus under processor control.

In these devices, the four data input bits and the two-bit digit select code (DS1 pin 31, DS2 pin 32) are written into input buffer latches when both chip select inputs (CS1 pin 33, CS2 pin 34) are taken to a negative level. On the rising edge of either chip select input, the content of the data input latches is decoded and stored in the output latches of the digit selected by the contents of the select code latches.

A select code of 00 writes into D4, SC2 = 0, SC1 = 1 writes into D3, SC2 = 1, SC1 = 0 writes into D2, and 11 writes into D1. The timing relationships for inputting data are shown in Fig (2), and the chip select pulse widths and data setup and hold times are specified in Table 2.

Table 3 Output Codes

BINARY B3	B2	B1	B0	HEXADECIMAL ICM7211(M) ICM7212(M)	CODE B ICM7211A(M) ICM7212A(M)
0	0	0	0	0	0
0	0	0	1	1	1
0	0	1	0	2	2
0	0	1	1	3	3
0	1	0	0	4	4
0	1	0	1	5	5
0	1	1	0	6	6
0	1	1	1	7	7
1	0	0	0	8	8
1	0	0	1	9	9
1	0	1	0	A	-
1	0	1	1	b	E
1	1	0	0	C	H
1	1	0	1	d	L
1	1	1	0	E	P
1	1	1	1	F	(BLANK)

SEGMENT ASSIGNMENT

APPLICATIONS

1. Ganged ICM7211's Driving 8-Digit LCD Display.

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2. 4 1/2 Digit LCD DPM with Digit Blanking on Overrange.

3. 8048/8748 Microprocessor Interface.

PACKAGE DIMENSIONS

40 Pin Plastic Dual-In-Line Package

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INTERSIL

ICM7218 Series CMOS Universal 8 Digit LED Driver System

FEATURES

- **Total circuit integration on chip includes:**
  - **a) Digit and segment drivers**
  - **b) All multiplex scan circuitry**
  - **c) 8X8 static memory**
  - **d) 7 segment Hexadecimal and Code B decoders**
- **Output drive suitable for large LED displays**
- **Both common anode and common cathode LED drive versions**
- **Single 5 volt supply required**
- **Data retention to 2 volts supply**
- **Shutdown feature - turns off display and puts chip into very low power dissipation mode**
- **Pin selectable choice of 2 seven segment decoders - Hexa or Code B**
- **Pin selectable choice of seven segment decode or no decoder**
- **Microprocessor compatible and hardwire versions**
- **All terminals protected against static discharge**

GENERAL DESCRIPTION

The ICM7218 series of universal LED driver systems provide, in a single package, all the circuitry necessary to interface most common microprocessors or digital systems and an LED display. Included on chip is an 8x8 static memory array providing storage for the displayed information, 2 types of 7 segment decoders, all the multiplex scan circuitry and the high power digit and segment drivers.

The ICM7218A and ICM7218B are intended to be used primarily in microprocessor systems. Data is read directly from the I/O bus line from the microprocessor. 2 Control lines ($\overline{\text{Write}}$, and Mode) define chip select, which reads either 4 bits of control information (Data Coming, $\overline{\text{Shutdown}}$, Decode, Hexa or Code B Decoding) or 8 bits of Display Input Data. Display Input Data (8 words, 8 bits each) is automatically sequenced into the memory on successive negative going $\overline{\text{Write}}$ pulses. Data may be displayed either directly or decoded in Hexadecimal or Code B formats. The ICM7218A drives a common anode display while the ICM7218B drives a common cathode display. (See Block Diagram 1)

The ICM7218C and ICM7218D feature 2 lines for control information ($\overline{\text{Write}}$, Three Level Input; Hexa, Code B, $\overline{\text{Shutdown}}$), 4 lines for Input Data and 3 lines for BCD Data Addressing of each of eight data memory locations.

Data is written into memory by setting up a BCD Data Address memory location, defining 4 lines of Input Data and then strobe the $\overline{\text{Write}}$ line low. The Three Level Control Input is independent of the $\overline{\text{Write}}$ instruction. Only Hexadecimal and Code B decoding are available for the Display Outputs. The ICM7218C drives a common anode display, the ICM7218D a common cathode display. (See Block Diagram 2)

The ICM7218E provides 4 separate lines for control information ($\overline{\text{Write}}$, Hexa-Code B, Decode, $\overline{\text{Shutdown}}$), 8 lines for input data, and 3 lines for BCD digit address. Data is written into the memory by setting up a BCD Data Address memory location, defining 8 lines of Input Data, and then strobe the $\overline{\text{Write}}$ line low. Control information is on separate lines and is independent of the $\overline{\text{Write}}$ instruction. Data may be displayed either directly or decoded in Hexadecimal or Code B formats. The ICM7218E drives a common anode display. (See Block Diagram 3)

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ORDERING INFORMATION

Typical App.	Order Part Number	Display Option	Package
Microprocessor Control	ICM7218A IJI	Common Anode	28 Lead CERDIP
	ICM7218B IPI	Common Cathode	28 Lead Plastic
Hardwire Control	ICM7218C IJI	Common Anode	28 Lead CERDIP
	ICM7218D IPI	Common Cathode	28 Lead Plastic
	ICM7218E IDL	Common Anode	40 Lead Ceramic

This is a preliminary specification and is subject to change.

CHIP TOPOGRAPHY ICM7218A

ABSOLUTE MAXIMUM RATINGS

Supply Voltage 6V
Digit Output Current 300mA
Segment Output Current 50mA
Input Voltage (any terminal) ..... V^+ +0.3V to V^- −0.3V NOTE 1
Power Dissipation (28 Pin CERDIP) ..... 1 watt NOTE 2
Power Dissipation (28 Pin Plastic) ..... 0.5 watt NOTE 2
Power Dissipation (40 Pin Ceramic) ..... 1 watt NOTE 2
Operating Temperature Range ..... −20°C to +70°C
Storage Temperature Range ..... −55°C to +125°C

NOTE 1 Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V^+ or less than V^- may cause destructive device latchup. For this reason it is recommended that no inputs from external sources not operating on the same power supply be applied to the device before its supply is established. When using multiple supply systems the supply to the ICM7218 should be turned on first.

NOTE 2 These limits refer to the package and will not be obtained during normal operation. Derate above 50°C by 25mW per °C.

SYSTEM ELECTRICAL CHARACTERISTICS V^+-V^- = 5V, T_A = 25°C, Test Circuit, Display Diode Drop 1.7V

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Operating Voltage	V^+-V^-		4		6	V
	V^+-V^-	Power Down Mode	2		6	V
Quiescent Supply Current	I_Q	Shutdown (Note 3)	6	10	300	μA
Operating Supply Current	I_{DP}	Decoder On, Outputs Open Ckt	250		950	μA
		No Decode, Outputs Open Ckt	200		450	μA
Digit Drive Current	I_D	Common Anode Vout = V^+ −2.0	−170			mA
		Common Cathode Vout = V^- +1V	50			mA
Digit Leakage Current	I_{DL}				100	μA
Peak Segment Drive Current	I_S	Common Anode Vout = V^- +1.5V	20	25		mA
		Common Cathode Vout = V^+ −2.0V	−10			mA
Segment Leakage Current	I_{SL}				50	μA
Display Scan Rate	F_{MUX}			250		Hz
Three Level Input						
Logical "1" Input Voltage	V_{TH}	Hexidecimal ICM7218C, D (Pin 9)	4.0			V
Floating Input	V_{TD}	Code B ICM7218C, D (Pin 9)	2.0		3.0	V
Logical "0" Input Voltage	V_{TL}	Shutdown ICM7218C, D (Pin 9)			1.75	V
Three Level Input Impedance				100		kΩ
Logical "1" Input Voltage	V_{IH}		2.4			V
Logical "0" Input Voltage	V_{IL}				.8	V
Write Pulse Width (Negative)	tw		400			nS
Write Pulse Width (Positive)	$t\overline{w}$		400			nS
Mode Pulse Width	tm		400			nS
Data Set Up Time	t_{ds}		400			nS
Data Hold Time	t_{dh}		25			nS
Digit Address Set Up Time	t_{das}	ICM7218	400			nS
Digit Address Hold Time	t_{dah}	ICM7218	100			nS
Operating Temperature Range	T_A	Industrial Temperature Range	−20		70	°C

NOTE 3 In the ICM7218C and D (hardwire control versions) the Hexa/Code B/$\overline{\text{Shutdown}}$ Input (Pin 9) has internal biasing resistors to hold it at $V^+/2$ when Pin 9 is open circuited. These resistors consume power and result in a Quiescent Supply Current (I_Q) of typically 50μA. The ICM7218A, B, and E devices do not have these biasing resistors and thus are not subject to this condition.

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BLOCK DIAGRAMS

ICM7218A, ICM7218B

ICM7218C, ICM7218D

ICM7218E

PIN CONFIGURATION

ICM7218A

COMMON ANODE

TOP VIEW

ICM7218B

COMMON CATHODE

TOP VIEW

ICM7218C

COMMON ANODE

TOP VIEW

ICM7218D

COMMON CATHODE

TOP VIEW

ICM7218E

COMMON ANODE

TOP VIEW

CONTROL INPUT DEFINITIONS ICM7218A and B

INPUT	TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{Write}}$	8	High Low	Input Not Loaded Into Memory Input Loaded Into Memory
Mode	9	High Low	Load Control Word on Write Pulse Load Input Data on Write Pulse
ID6 (Hexadecimal/Code B)	5	High Low	Hexadecimal Decoding Code B Decoding
ID5 (Decode/No Decode)	6	High Low	No Decode Decode
ID7 (Data Coming/Input $\overline{\text{D.P.}}$)	7	High Low	Data Coming No Data Coming
ID4 $\overline{\text{Shutdown}}$	10	High Low	Normal Operation Shutdown (Oscillator, Decoder, and Displays Disabled)
Input Data ID0-ID7	11,12,13, 14,5,6 10,7	High Low	Loads "One" (Note 2) Loads "Zero"

CONTROL INPUT DEFINITIONS ICM7218C and D

INPUT	TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{Write}}$	8	High Low	Inputs Not Loaded Into Memory Inputs Loaded Into Memory
Three Level Input (Note 1)	9	High Floating Low	Hexadecimal Decode Code B Decode Shutdown (Oscillator, Decoder and Displays Disabled)
Digit Address DA0-DA2	5,6,10	High Low	Loads "Ones" Loads "Zeros"
Input Data ID0-ID7	11,12,13, 14,5, 6,10,7	High Low	Loads "Ones" (Note 2) Loads "Zeros"

CONTROL INPUT DEFINITIONS ICM7218E

INPUT	TERMINAL	VOLTAGE	FUNCTION
$\overline{\text{Write}}$	9	High Low	Input Latches Not Updated Input Latches Updated
$\overline{\text{Shutdown}}$	10	High Low	Normal Operation Shutdown (Oscillator, Decoder and Displays Disabled)
Digit Address (0,1,2) DA0-DA2	13,14,12	High Low	Loads "Ones" Loads "Zeros"
Decode/No Decode	33	High Low	No Decode Decode
Hexadecimal/Code B	32	High Low	Code B Decoding Hexadecimal Decoding
Input Data ID0-ID7	16,17,18,19 6 7,11,8	High Low	Loads "Ones" (Note 2) Loads "Zeros"

NOTE 1 In the ICM7218C and ICM7218D versions, Hexadecimal, Code B and Shutdown are controlled with a three level input on Pin 9. Pulling Pin 9 high decodes Hexadecimal. Floating Pin 9 decodes Code B and pulling Pin 9 low puts the ICM7218 in a Shutdown mode.

NOTE 2 In the No Decode Mode, "Ones" represents "on" segments for all inputs except for the Decimal Point, where "Zero" represents "on" segments, (i.e. segments are positive true, decimal point is negative true).

Figure 1: Multiplex Timing

Figure 2: Segment Assignments

APPLICATIONS

Decode/No Decode

For the ICM7218A/B/E products, there are 3 input data formats possible; either direct segment and decimal point information-8 bits per digit or 2 BCD codes plus decimal point-5 bits per digit. The 7 segment decoder on chip may be disabled if direct segment information is inputted.

In the No Decode format, the inputs directly control the outputs as follows:

Input Data:	ID7	ID6	ID5	ID4	ID3	ID2	ID1	ID0
Output Segments:	$\overline{\text{D.P.}}$	a	b	c	e	g	f	d

The No Decode Mode, "Ones" represents on segments for all inputs except for the Decimal Point, where "zero" represents on segments.

Hexadecimal or Code B Decoding:
For all products, a choice of either Hexa or Code B decoding may be made. Hexa decoding provides 7 segment plus six alpha characters while Code B provides a negative sign (–), a blank (for leading zero blanking) and certain useful alpha characters for most numeric formats.

The four bit binary code is set up on inputs ID3-ID0.

Binary Code	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
Hexa Code	0	1	2	3	4	5	6	7	8	9	A	b	C	d	E	F
Code B	0	1	2	3	4	5	6	7	8	9	-	E	H	L	P	(Blank)

Shutdown

Shutdown performs several functions: it puts the device into a very low dissipation mode (typically 10µA at V^+-V^- = 5), turns off both the digit and segment drivers, stops the multiplex scan oscillator (this is the only way the scan oscillator can be disabled). However, it is still possible to input the memory during shutdown - only the output and read sections of the device are disabled.

Powerdown

In a Shutdown Mode, the supply voltage may be reduced to 2 volts without data being lost in memory. However, data should not be written into memory if the supply voltage is less than 4 volts.

Output Drive

The common anode output drive is approximately 200 mA per digit at a 12% duty cycle. With 5 segments being driven, this is equal to about 40mA per segment peak drive or 5mA average drive. The common cathode drive is approximately one half that of the common anode drive. If high impedance LED displays are used, the drive will be correspondingly less.

Inter Digit Blanking

A blanking time of approximately 10µs occurs between digit strobes to ensure that segment information is correct before the next digit drive thereby avoiding ghosting.

Leading Zero Blanking

This may be programmed into chip memory in the no-decode operation (each segment programmed for a zero for the blanked digits) or by using the 16th state (binary 15) with the Code B decoder.

Driving Larger Displays

If a higher average drive current per digit is required, it is possible to parallel connect digit drives together. For example, by paralleling pairs of digit drives together to drive a 4 digit display 10 mA average segment drive can be obtained.

APPLICATIONS, continued

Power Dissipation Considerations

Assuming common anode drive at $V^+-V^- = 5$ volts and all digits on with an average of 5 segments driven per digit, the average current would be approximately 200mA. Assuming further a 1.8 volt drop across the LED display would result in a 3.2 volt drop across the ICM7218. The device power dissipation will, therefore, be 640mW rising to about 900mW for all '8"s displayed. Caution: Position device in system such that air can flow freely to provide maximum cooling. The common cathode dissipation is approximately one half that of the common anode dissipation.

Processor Input Drive Considersations (ICM7218A/B)

The control instructions are read from the input bus lines if Mode is high and $\overline{\text{Write}}$ low. The instructions occur on 4 lines and are - Decode/no Decode, type of Decode (if desired), Shutdown/no Shutdown and Data Coming/not Coming. After the control instructions have been read (with Data Coming instruction) display data can be written into memory with each following negative going pulse of $\overline{\text{Write}}$, Mode being low. After all 8 words or digit memory locations have been re-written, additional transitions of the state of $\overline{\text{Write}}$ are ignored. It is not possible to change for example digit #7 only without refreshing the data for all the other digits. (This can, however, be achieved with the ICM7218C/D/E where the digits are individually addressed.)

Hardwire Input Drive Considerations (ICM7218C/D/E)

Control instructions are provided to the ICM7218C/D by a single three level input terminal (Pin 9), which operates independently of the $\overline{\text{Write}}$ pulse. The ICM7218E control instructions are also independent but are on three separate pins (10, 32, 33).

Data can be written into memory on the ICM7218C/D/E by setting up a 3 bit binary code (one of eight) on the digit address inputs, which define the digit where the data is to be written into the memory, and apply a negative going $\overline{\text{Write}}$ pulse. For example, it is possible to change only digit 7 without refreshing the data for all the other digits. (However, this cannot be achieved with the ICM7218A/B.

Supply Capacitor

A .1μF capacitor is recommended between V^+ and V^- to inhibit multiplex noise.

SWITCHING WAVEFORMS ICM7218

Figure 3

CHIP ADDRESS SEQUENCE ICM7218A and B

Figure 4

CHIP ADDRESS SEQUENCE EXAMPLE ICM7218C/D/E

Figure 5

6

TEST CIRCUITS

TEST CIRCUIT 1

TEST CIRCUIT 2

6

TYPICAL CHARACTERISTICS

COMMON ANODE SEG. DRIVER
$I_{SEG.}$ VS. (V_{OUT}-V^-) AT 25°C

COMMON ANODE SEG. DRIVER
$I_{SEG.}$ VS. (V_{OUT}-V^-)

COMMON ANODE DIGIT DRIVER
I_{DIG} VS. (V^+-V_{OUT})

TYPICAL CHARACTERISTICS, continued

COMMON CATHODE DIGIT DRIVER I_{DIG} VS. (V_{OUT}-V^-) AT 25°C

COMMON CATHODE SEG. DRIVER I_{SEG} VS. (V^+-V_{OUT})

COMMON CATHODE DIGIT DRIVER $I_{DIG.}$ VS. (V_{OUT}-V^-)

APPLICATION EXAMPLES

8 DIGIT MICROPROCESSOR DISPLAY APPLICATION

The display interface (ICM 7218) is shown with an Intel 8048 microprocessor. The 8 bit data bus DB0/DB7 - ID0/ID7 transfers control and data information to the 7218 display interface on successive Write pulses. When Mode is high a control word is transferred. Mode low allows data transfer on a Write pulse. Eight memory address locations in the 8 x 8 static memory are automatically sequenced on each successive Write pulse. After eight Write pulses have occurred, further pulses are ignored and the display interface returns to normal display operation until a new control word is transferred. See Figure 4.

Decoding of the stored data in memory is defined by the control word and may be decoded in Hexadecimal, Code B, or No-Decode formats.

Figure 6: 8 Digit Microprocessor Display

16 DIGIT MICROPROCESSOR DISPLAY APPLICATION

Both ICM7218's are addressed simultaneously with a 3 bit word, DA2-DA0.

Display data from the 8048 I/O bus (DB7-DB0) is transferred to both ICM7218 (ID3-ID0) simultaneously, 4 bits + 4 bits on Write enable.

Display digits from both ICM7218's are interleaved to allow adjacent pairs of digits to be loaded sequentially on a single 8 bit data bus, ie D0 D1, D2 D3, D4 D5, etc..

Decimal point information (from 8048, P26 - P27) is supplied to the ICM7218 on bus lines ID7 to both devices.

Choice of decoding is available in either Hexadecimal or Code-B format by hardwiring or decoding to a Three Level format on Pin 9 of the ICM7218.

Multiplexing is asynchronous with respect to the microprocessor and is completely performed by the ICM7218.

Figure 7: 16 Digit Display

The ICM7218 can be used as a microprocessor based LED status panel driver. The microprocessor selected control word would include "No Decode" and "Data Coming". The computer then outputs word oriented "Ones" and "Zeroes" to indicate on-off states. This data is read into the ICM7218 which in turn directly drives appropriate descrete LEDs. LED indicators can be red or green (8 "segments" x 8 digits = 64 dots ÷ 2 per red or green = 32 channels) on red, yellow or green (21 channels).

Additional ICM7218's may be bussed and addressed (see Figure 7) to expand the status panel capacity. Note per figure 4 that after the ICM7218 has read in its data (8 write pulses), it ignores additional information on the data lines. A new control word must be received before the next write sequence can be accommodated. Consequently, by address decoding and write pulse enabling, numerous ICM7218's can be bussed together to allow a large number of indicator channels.

PACKAGE DIMENSIONS

28 Pin CERDIP Dual-In-Line Package

28 Pin Plastic Dual-In-Line Package

40 Pin Ceramic Dual-In-Line Package

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INTERSIL

ICM7206, ICM7206A, ICM7206B Complementary MOS Touch Tone Encoder

FEATURES

- **Low cost system with minimum component count**
- **Fully integrated oscillator uses 3.58 MHz color TV crystal**
- **High current bipolar output driver**
- **Low output harmonic distortion**
- **Wide operating supply voltage range: 3 to 6 volts**
- **Requires inexpensive single contact per key calculator type keyboard (ICM7206 only)**
- **Extremely low power ≤ 5.5mW with a 5.5V supply**
- **Single and dual tone capabilities**
- **Multiple key lockout**
- **Disable output: provides output switch function whenever a key is enabled**
- **Custom options available**

CHIP TOPOGRAPHY

Chip Dimensions
0.060" (1.524mm) x 0.101" (2.565mm)

Chip may be die attached using conventional eutectic or epoxy procedures. Wire bonding may be either aluminum ultrasonic or gold compression.

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CONNECTION DIAGRAM

Pin 1 is designated either by a dot or a notch.

GENERAL DESCRIPTION

The Intersil ICM7206/A/B are 2-of-8 sine wave tone encoders for use in telephone dialing systems. Each circuit contains a high frequency oscillator, two separate programmable dividers, a D/A converter, and a high level output driver.

The reference frequency is generated from a fully integrated oscillator requiring only a 3.58 MHz color TV crystal. This frequency is divided by 8 and is then gated into two divide by N counters (possible division ratios 1 through 128) which provide the correct division ratios for the upper and lower band of frequencies. The outputs from these two divide by N counters are further divided by 8 to provide the time sequencing for a 4 voltage level synthesis of each sinewave. Both sinewaves are added and buffered to a high current output driver, with provisions made for up to two external capacitors for low pass filtering, if desired. Typically, the total output harmonic distortion is 20% with no L.P. filtering and it may be reduced to typically less than 5% with filtering. The output drive level of the tone pairs will be approximately -3dBV into a 900 ohm termination. The skew between the high and low groups is typically 2.5 dB without low pass filtering.

The 7206 uses either a 3 x 4 or 4 x 4 single contact keyboard; the oscillator will run whenever the power is applied, and the DISABLE output consists of a p-channel open drain FET whose source is connected to V^+.

The 7206A can also use a 3 x 4 or 4 x 4 keyboard, but requires a double contact type with the common line tied to V^+. The oscillator will be on whenever power is applied; the DISABLE output consists of a p-channel open drain FET; its' source is connected to V^+.

The 7206B requires a 4 x 4 double contact keyboard with the common line tied to V^-. The oscillator will be on only during the time that a ROW is enabled, and the DISABLE output consists of an n-channel open drain FET with its' source tied to V^-.

The ICM7206 family is fabricated using Intersil's standard low voltage metal gate C-MOS process which has been used exclusively for all Intersil timing products. Custom options are possible using different quartz crystal frequencies, two contacts per key type keyboards and any combinations of output frequencies as defined above.

ORDERING INFORMATION

PART NUMBER	TEMPERATURE RANGE	PACKAGE
ICM7206 JPE	-40°C to +85°C	Plastic
ICM7206A JPE	-40°C to +85°C	Plastic
ICM7206B JPE	-40°C to +85°C	Plastic
ICM7206/D	-40°C to +85°C	DICE
ICM7206A/D	-40°C to +85°C	DICE
ICM7206B/D	-40°C to +85°C	DICE

ABSOLUTE MAXIMUM RATINGS (Note 1)

Supply Voltage (Note 2) 6.0V
Supply Current V^- (terminal 8) 25mA
Supply Current V^+ (terminal 16) 40mA
Disable Output Volt. (term. 7) .. Not more pos. than V^+ nor more neg. than −6V with respect to V^+
Output Volt. (term. 15). Not more pos. than +5V with respect to V^+, nor more neg. than −1.0 with respect to V^-
Output Current (terminal 15) 25mA
Power Dissipation 300mW
Operating Temperature Range ..... −40°C to +85°C
Storage Temperature Range ..... −55°C to +125°C

NOTE 1. Absolute maximum ratings refer to values which if exceeded may permanently change or destroy the device. Additionally, absolute maximum ratings do not imply that the device will operate correctly if these values are used (see Typical Operating Characteristics).

NOTE 2. The ICM7206 family has a zener diode connected between V^+ and V^- having a breakdown voltage between 6.2 and 7.0 volts. If the currents into terminals 8 and 16 are limited to 25 and 40mA maximum respectively, the supply voltage may be increased above 6 volts to zener voltage. With no such current limiting, the supply voltage must not exceed 6 volts.

TYPICAL OPERATING CHARACTERISTICS

TEST CONDITIONS: $V^+ - V^- = 5.5V$, Test Circuit, $T_A = 25°C$ unless otherwise specified.

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNITS
Supply Current	I_S	R_L disconnected		450	1000	μA
Guaranteed Operating Supply Voltage Range (Note 3)	V_{OP}	$-40°C \le T_A \le +85°C$	3.0		6.0	V
Peak to Peak Output Voltage	V_{OUT}	C_1, C_2 disconnected — LOW BAND	0.90	1.15	1.45	V
		$R_L = 1k\Omega$ — HIGH BAND	1.10	1.40	1.7	
		NO FILTERING		490		
RMS Output Voltage	V_{OUT}	$R_L = 1k\Omega$ — C_2 only		480		mV
		$f_{out} = 697Hz$ — C_1 & C_2		480		
		NO FILTERING		655		
RMS Output Voltage	V_{OUT}	$R_L = 1k\Omega$ — C_2 only		490		mV
		$f_{out} = 1633Hz$ — C_1 & C_2		580		
Skew Between High and Low Band Output Voltages	V_{HL}	$R_L = 1k\Omega$		2.5	3.0	dB
		C_1, C_2 disconnected				
		$R_L = 1k\Omega$, operating		90	200	Ω
Output Impedance	Z_{OUT}	$R_L = 1k\Omega$, quiescent		25		kΩ
		$R_L = 1k\Omega$				
Total Output Harmonic Distortion	THD1	Either high or low bands		20.0	25.0	%
		No low pass filtering				
		$R_L = 1k\Omega$, $f_{out} = 697Hz$		2.3	10	
Total Output Harmonic Distortion	THD2	$C_1 = 0.002\mu F$				
		$C_2 = 0.02\mu F$, $f_{out} = 1633Hz$		1.0	10	
Maximum Output Voltage Level	V_{OH}	$R_L = 1k\Omega$			4.6	V
Minimum Output Voltage Level	V_{OL}	$R_L = 1k\Omega$	0.5			
Keyboard Input Pullup Resistors	R_{IN}	Terminals 3, 4, 5, 6, 11, 12, 13, 14	35	100	150	kΩ
Keyboard Input Capacitance	C_{IN}	Terminals 3, 4, 5, 6, 11, 12, 13, 14			5	pF
Guaranteed Oscillator Frequency Range (Note 4)	OFR_1	$3V \le (V^+ - V^-) \le 6.0V$	2.0		4.5	MHz
Guaranteed Oscillator Frequency Range	OFR_2	$4V \le (V^+ - V^-) \le 6.0V$	2.0		7	
System Startup Time on Application of Power	t_{ON}	Supply voltage and key depressed simultaneously		10		mS
Disable Output Saturation Resistance (ON STATE)	R_D	See Logic Table for Input Conditions Current = 4mA		330	700	Ω
Disable Output Leakage (OFF STATE)	I_D	See Logic Table for Input Conditions			10	μA
Oscillator Load Capacitance	C_{OSC}	Measured between terminals 9 & 10, no supply voltage applied to circuit $-40°C \le T_A \le 85°C$		7		pF
Guaranteed Output Frequency Tolerance	f_{out}	Any output frequency Crystal tolerance ±60ppm Crystal load capacitance $C_L = 30pF$			±0.75	%
Oscillator Startup Time ICM7206B	t_{START}	$V^+ - V^- = 3V$ Note 5			7	mS

NOTE 3: Operation above 6 volts must employ supply current limiting. Refer to 'ABSOLUTE MAXIMUM RATINGS' and the Application Notes for further information.

NOTE 4: The ICM7206 family uses dynamic high frequency circuitry in the initial 2^3 divider resulting in low power dissipation and excellent performance over a restricted frequency range. Thus, for reliable operation with a 6 volt supply an oscillator frequency of not less than 2MHz must be used.

NOTE 5: After row input is enabled.

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TRUTH TABLE

LINE	ROWS (1) ACTIVATED	COLS (2) ACTIVATED	OUTPUT (TERMINAL #15)	DISABLE (TERMINAL #7)	COMMENTS
1	0	0	Off	Off	Quiescent State
2	1	1	$f_{row} + f_{col}$	On	Dual Tone
3	1	2 or 3 (incl. col #4)	f_{row}	On	Single Tone
4	2 or 3	1	f_{col}	On	Single Tone
5	2 or 3	2 or 3 (excl. col #3)	D.C. Level	On	No Tone
6	1	4 or 3 (must excl. col #4)	f_{row}, 50% Duty Cycle	f_{row}, 50% Duty Cycle	f_{row} Test
7	4	1	f_{col}, 50% Duty Cycle	f_{col}, 50% Duty Cycle	f_{col} Test
8	0	1 or 2 or 3 or 4	Off	Off	n/a*
9	1	0	902Hz + f_{row}	On	n/a*
10	2 or 3	0	902Hz	On	n/a*
11	4	0	902Hz, 50% Duty Cycle	902Hz, 50% Duty Cycle	n/a*
12	2 or 3 or 4	4	D.C. Level	Indeterminate	Multiple Key Lockout
13	4	2 or 3 or 4	D.C. Level	Indeterminate	Multiple Key Lockout

*n/a — not applicable to telephone calling.

Note 1: Rows are activated for the ICM7206 by connecting to a negative supply voltage with respect to V^+ (terminal 16) at least 33% of the value of the supply voltage (V^+–V^-). For the ICM7206A rows (and columns) are activated by connecting to a positive supply voltage with respect to V^- (terminal 8) at least 33% of the value of the supply voltage (V^+–V^-). The rows and columns of the ICM7206B are activated by connecting to a negative supply voltage.

Note 2: Columns (ICM7206) are activated by being connected to a positive supply voltage with respect to V^- (terminal 8) at least 33% of the value of the supply voltage (V^+–V^-).

COMMENTS

All combinations of row and column activations are given in the truth table. Lines 1 thru 7 and 12, 13 represent conditions obtainable with a matrix keyboard. Lines 8 thru 11 are given only for completeness and are not pertinent to telephone dialing.

Lines 6 and 7 show conditions for generating 50% duty cycle full amplitude signals useful for rapid testing of the row and column frequencies on automatic test equipment. In all other cases, output frequencies on terminal 15 are single or dual 4 level synthesized sine waves.

A 'DC LEVEL' on terminal 15 may be any voltage level between approximately 1.2 and 4.3 volts with respect to V^- (terminal 8) for a 5.5 volt supply voltage.

The impedance of the OUTPUT (terminal 15) is approximately 20K ohms in the OFF state. The 'DISABLE OUT-OUT' ON and OFF conditions are defined in the TYPICAL OPERATING CHARACTERISTICS.

SCHEMATIC DIAGRAM

TEST CIRCUIT

TYPICAL OPERATING CHARACTERISTICS

SUPPLY CURRENT AS A FUNCTION OF SUPPLY VOLTAGE

TOTAL HARMONIC DISTORTION AS A FUNCTION OF LOAD RESISTANCE

OSCILLATOR FREQUENCY DEVIATION AS A FUNCTION OF SUPPLY VOLTAGE

PEAK TO PEAK OUTPUT VOLTAGE AS A FUNCTION OF SUPPLY VOLTAGE

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KEY	LOW BAND FREQ. Hz	HI BAND FREQ. Hz
1	697	1209
2	697	1336
3	697	1477
4	770	1209
5	770	1336
6	770	1477
7	852	1209
8	852	1336
9	852	1477
*	941	1209
0	941	1336
#	941	1477
A	697	1633
B	770	1633
C	852	1633
D	941	1633

FIGURE 1: Keyboard Frequencies

FIGURE 2

Figure 2 shows individual currents of a low band and high band frequency pair into the swimming mode A (See Figure 3) and the resultant voltage waveform.

DESIRED FREQUENCY Hz	ACTUAL FREQUENCY Hz	FREQUENCY DEVIATION %	DIVIDE BY N RATIO
697	699.13	+0.30	80
770	766.17	−0.50	73
852	847.43	−0.54	66
941	947.97	+0.74	59
1209	1215.88	+0.57	46
1336	1331.68	−0.32	42
1477	1471.85	−0.35	38
1633	1645.01	+0.74	34

APPLICATION NOTES

1. Device Description

The ICM7206 family is manufactured with a standard metal gate C-MOS technology having proven reliability and excellent reproducability resulting in extremely high yields. The techniques used in the design have been developed over many years and are characterized by wide operating supply voltage ranges and low power dissipation.

To minimize chip size, all diffusions used to define source-drain regions and field regions are butted up together. This results in approximately 6.3 volt zener breakdown between the supply terminals, and between all components on chip. As a consequence, the usual C-MOS static charge problems and handling problems are not experienced with the ICM7206.

The oscillator consists of a medium size C-MOS inverter having on chip a feedback resistor and two capacitors of 14pF each, one at the oscillator input and the other at the oscillator output. The oscillator is followed by a dynamic $\div 2^3$ circuit which divides the oscillator frequency to 447,443Hz. This is applied to two programmable dividers each capable of division ratios of any integer between 1 and 128, and each counter is controlled by a ROM. The outputs from the programmable counters drive sequencers (divide by 8) which generate the eight time slots necessary to synthesize the 4-level sine waves.

The control logic block recognizes signals on the row and column inputs that are only a small fraction of the supply voltage, thereby permitting the use of a simple matrix single contact per key keyboard, rather than the more usual two contacts per key type having a common line. The row and column pullup resistors are equal in value and connected to the opposite supply terminals (ICM7206 only; for the ICM7206A all pullup resistors are connected to the V^- terminal and for the ICM7206B they are tied to the V^+. Therefore, connecting a row input to a column input generates a voltage on those inputs which is one half of the supply voltage.

The ICM7206 family employs a unique but extremely simple digital to analog (D to A) converter. This D to A converter produces a 4 level synthesized sine wave having an intrinsic total harmonic distortion level of approximately 20%. Figure 3 shows a single channel D to A converter. The current sources Q_2 and Q_3 are proportioned in the ratio of 1:1.414. During time slots 1 and 8 both S_1 and S_2 are off, during time slots 2 and 7 only S_1 is on, during time slots 3 and 6 only S_2 is on, and during time slots 4 and 5 both S_1 and S_2 are on. The resultant currents are summed at node A, buffered by Q_4 and further buffered by R_3, R_4 and Q_5. Switch S_3 allows the output to go into a high impedance mode under quiescent conditions.

Node A is the common summing point for both the high and low band frequencies although this is not shown in Figure 3.

The synthesized sine wave has negligible even harmonic distortion and very low values of third and fifth harmonic distortion thereby minimizing the filtering problems necessary to reduce the total harmonic distortion to well below the 10% level required for touch tone telephone encoding. Figure 4 shows the low pass filter characteristic of the output buffer for $C_1 = 0.0022\mu F$ and $C_2 = 0.022\mu F$. A small peak of 0.4dB occurs at 1100Hz with sharp attention (12dB per octave) above 2500Hz. This type of active filter produces a sharper and more desirable knee characteristic than would two simple cascaded RC networks.

FIGURE 3: D to A Converter and Output Buffer

FIGURE 4: Frequency Attentuation Characteristics of the Output Buffer

2. Latchup Considerations

Most junction isolated C-MOS integrated circuits, especially those of moderate or high complexity, exhibit latchup phenomena whereby they can be triggered into an uncontrollable low impedance mode between the supply terminals. This can be due to gross forward biasing of inputs or outputs (with respect to the supply terminals), high voltage supply transients, or more rarely by exceptional fast rate of rise of supply voltages.

The ICM7206 family is no exception, and precautions must be taken to limit the supply current to those values shown in the ABSOLUTE MAXIMUM RATINGS. For an example, do not use a 6 volt very low impedance supply source in an **electrically extremely noisy** environment unless a 500 ohm current limiting resistor is included in series with the V^- terminal. For normal telephone encoding applications no problems are envisioned, even with low impedance transients of 100 volts or more, if circuitry similar to that shown in the next section is used.

3. Typical Application (Telephone Handset)

A typical encoder for telephone handsets is shown in Figure 5. This encoder uses a single contact per key keyboard and provides all other switching functions electronically. The diode connected between terminals 8 and 15 prevents the output going more than 1 volt negative with respect to the negative supply V^- and the circuit operates over the supply voltage range from 3.5 volts to 15 volts on the device side of the bridge rectifier. Transients as high as 100 volts will not cause system failure, although the encoder will not operate correctly under these conditions. Correct operation will resume immediately after the transient is removed.

The output voltage of the synthesized sine wave is almost directly proportional to the supply voltage (V^+-V^-) and will increase with increase of supply voltage until zener breakdown occurs (approximately 6.3 volts between terminals 8 and 16) after which the output voltage remains constant.

4. Portable Tone Generator

The ICM7206A/B require a two contact key keyboard with the common line connected to the positive supply (neg for ICM7206B) (terminal 16). A simple diode matrix may be used with this keyboard to provide power to the system whenever a key is depressed, thus negating the need for an on/off switch. In Figure 6 the tone generator is shown using a 9 volt battery. However, if instead, a 6 volt battery is used, the diode D_4 is not required. It is recommended that a 470 ohm resistor still be included in series with a negative (positive) supply to prevent accidental triggering of latchup.

NOTE: If dual contact keyboard is used, common should be left floating.

FIGURE 5: Telephone Handset Touch Tone Encoder

FIGURE 6: Portable Tone Generator

OPTIONS

(For additional information consult the factory)

New types of keyboards, new applications for tone generators and new system requirements, provide challenges and difficulties to the semiconductor manufacturer. The design criteria for the ICM7206 included the following:

a) Selecting the least expensive and most reliable keyboard
b) Selecting the lowest cost and most available quartz crystal
c) Minimizing the number of external components
d) Minimizing supply current drain and maximizing operating supply voltage range
e) Providing the smallest and least expensive circuit possible in a 16 lead package

Options can be achieved using metal mask additions to provide the following.

1) The sequence or position of either the row or column terminals can be interchanged i.e., row 1 terminal 3 could become terminal 11, etc.
2) Any frequency oscillator from approximately 0.5MHz to 7MHz can be chosen. Note that the accuracy of the output frequencies will depend on the exact oscillator frequency. For instance, a 1 MHz crystal could be used with worst case output frequency error of 0.8%. Or, if high accuracy is required, ±0.25%, oscillator frequencies of 5,117,376Hz or 2,558,688Hz could be selected. ROM's are used to program the dividers.
3) The 'DISABLE' output may be changed to an inverter or an uncommitted drain n-channel transistor.
4) The oscillator may be disabled until a key is depressed.

PACKAGE DIMENSIONS

NOTE 1: Board drilling dimensions will equal standard practices for .020 diameter lead.

NOTE 2: All dimensions in parenthesis are metric.

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NOTES

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CMOS RAM's

Organization	Max Access Time (ns)	No. of Pins	V_{CC} max (V)	I_{CC} Max (μA)	Pkg[2]	Temp Range
4096 x 1						
IM6504	170	18	5.5	0.2 (typ.)	D,J,F,	C,I,M
1024 x 1						
IM6508/6518	460	16/18	7.0	100	D,J,F	C,I,M
IM6508-1/6518-1	300	16/18	7.0	10	D,J,F	I,M
IM6508A/6518A	150	16/18	11.0	500	D,J,F	I,M
IM6508A-1/6518A-1	95	16/18	12.0	100	D,J,F	I,M
256 x 4						
IM6551/61	360	18/22	8.0	100	D,J,F	I,M
IM6551A/61A	180	18/22	12.0	500	D,J,F	I,M
256 x 1						
IM6523	800	16	7.0	50	D,J,F	I,M
64 x 12						
IM6512	460	18	8.0	100	D,J,F	C,I,M
IM6512A	150	18	12.0	500	D,J,F	I,M

UV-ERASABLE CMOS PROMS

Organization	Max Access Time (ns)	No. of Pins	Operating Range (V)	I_{CC} max (μA)	Pkg[2]	Temp Range
1024 x 4						
6653	600	24	5	20	D,J	I,M
6653-1	450	24	5	20	D,J	I
6653A	300	24	10	20	D,J	I
512 x 8						
6654	600	24	5	20	D,J	I,M
6654-1	450	24	5	20	D,J	I
5554A	300	24	10	20	D,J	I

CMOS ROM's

Organization	Max Access Time (ns)	No. of Pins	V_{CC} max (V)	I_{CC} Max (μA)	Pkg[2]	Temp Range
1024 x 12						
IM6312	400	18	7.0	100	D,J	C,I,M
IM6312A	200	18	11.0	500	D,J	I,M
2048 x 8						
IM6316	350 (typ)	24	7.0	100 (typ)	D,J	C,I,M
8192 x 8						
IM6364	350 (typ)	24	7.0	100 (typ)	D,J	C,I,M

BIPOLAR PROM's

Organization	Max Access Time (ns)	No. of Pins	Output Type[1]	Pkg[2]	Temp
FPLA					
IM5200	100	24	OC	J	C
48 Product Terms					
14 Inputs, 8 Outputs					
32 x 8					
IM5600	50	16	OC	D,J,F	C,M
IM5610	50	16	TS	D,J,F	C,M
256 x 4					
IM5603A	60	16	OC	D,J,F	C,M
IM5623	60	16	TS	D,J,F	C,M
512 x 4					
IM5604	70	16	OC	D,J,F	C,M
IM5624	70	16	TS	D,J,F	C,M
512 x 8					
IM5605	70	24	OC	D	C,M
IM5625	70	24	TS	D	C,M

Note 1: OC-Open Collector Output
TS-Tri-State Output

Note 2: D: Ceramic Dual-In-Line
J: Cerdip Dual-In-Line
F: Ceramic Flat Package

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Dynamic RAMS

Organization	Max Access Time (ns)	Min Read Cycle (ns)	Min Read/Mod Write Cycle (ns)	No. of Pins	Input Levels V_{IL}/V_{IH} (V)	Power Supplies (V)	Max Operating Power (mW)	Standby Power (mW)	Pkg (note 1)	Temp Range (note 2)
16384 x 1										
IM4116-2	150	375	375	16	.8/2.4	+12, ±5	550	27	J	C
IM4116-3	200	375	375	16	.8/2.4	+12, ±5	550	27	J	C
IM4116-4	250	375	375	16	.8/2.4	+12, ±5	550	27	J	C
4096 x 1										
IM7027-1	120	250	325	16	.8/2.2	+12, ±5	462	27	J	C
MK4027-2	150	320	325	16	.8/2.2	+12, ±5	462	27	J	C
MK4027-3	200	375	420	16	.8/2.2	+12, ±5	462	27	J	C
MK4027-4	250	375	480	16	.8/2.2	+12, ±5	462	27	J	C

Static RAMS

Organization	Max Access Time (ns)	Min Read Cycle (ns)	No of Pins	Input Levels V_{IL}/V_{IH} (V)	Power Supplies (V)	Max Operating Power (mW)	Pkg (note 1)	Temp Range (note 2)
4096 x 1								
IM7141-2	200	200	18	.8/2.0	+5	370	J	C,M
IM7141-3	300	300	18	.8/2.0	+5	370	J	C,M
IM7141	450	450	18	.8/2.0	+5	370	J	C,M
IM7141L2	200	200	18	.8/2.0	+5	265	J	C
IM7141L3	300	300	18	.8/2.0	+5	265	J	C
IM7141L	450	450	18	.8/2.0	+5	265	J	C
1024 x 4								
IM2114-2	200	200	18	.8/2.0	+5	525	J	C
IM2114-3	300	300	18	.8/2.0	+5	525	J	C
IM2114	450	450	18	.8/2.0	+5	525	J	C
IM2114L2	200	200	18	.8/2.0	+5	370	J	C,M
IM2114L3	300	300	18	.8/2.0	+5	370	J	C,M
IM2114L	450	450	18	.8/2.0	+5	370	J	C,M
IM7114L2	200	200	18	.8/2.0	+5	265	J	C
IM7114L3	300	300	18	.8/2.0	+5	265	J	C
IM7114L	450	450	18	.8/2.0	+5	265	J	C
IM2147	70	70	18	.8/2.4	+5	880/110	D,J	C
IM2147-3	55	55	18	.8/2.4	+5	990/165	D,J	C

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INTERSIL

IM7114/2114
NMOS 4096 Bit Static RAM

FEATURES

- Organization – 1024x4
- Maximum Access Time:
  - 7114L2, 2114L2, 2114-2: 200ns
  - 7114L3, 2114L3, 2113-3: 300ns
  - 7114L, 2114L, 2114: 450ns
- TTL Compatible Inputs and Outputs
- Common Data Input and Output
- Military Temperature Operation (–55°C to +125°C) Available
- 883A Class B Processing Available
- Minimum Cycle Time Equal to Access Time
- Power Dissipation:
  - 7114L: 265mW Maximum
  - 2114L: 385mW Maximum
  - 2114: 525mW Maximum
  - Military Temp Units – 495mW Maximum
- Completely Static Operation
- Pin Compatible with Intel 2114

GENERAL DESCRIPTION

The 7114 is a 4096-bit static Random Access Memory device. The 7114 is organized 1024x4. The storage cell, decode and control circuitry are completely static, therefore no clocks or refresh operations are required. Memory access occurs within the specified access time after all address inputs are stable. A Chip Select input is provided for simple memory array expansion.

The 7114 is pin and performance compatible with the Intel 2114 series with the exception that the 7114 has lower power dissipation.

The device is assembled in a standard 18-pin DIP for maximum system packing density.

BLOCK DIAGRAM

PIN CONFIGURATION

LOGIC SYMBOL

ORDERING INFORMATION

TEMP. RANGE	POWER	PACKAGE	ACCESS TIME 200nS	300nS	450nS
C	265mW	CERDIP	IM7114L2CJN	IM7114L3CJN	IM7114LCJN
C	370mW	CERDIP	IM2114L2CJN (D2114L2)	IM2114L3CJN (D2114L3)	IM2114LCJN (D2114L)
M	495mW	CERDIP	IM2114L2MJN (MD2114L2)	IM2114L3MJN (MD2114L3)	IM2114LMJN (MD2114L)
M	495mW w/883B	CERDIP	IM2114L2MJN/883B (MD2114L2/B)	IM2114L3MJN/883B (MD2114L3/B)	IM2114LMJN/883B (MD2114L/B)
C	525mW	CERDIP	IM2114-2CJN (D2114-2)	IM2114-3CJN (D2114-3)	IM2114CJN (D2114)
C	265mW	PLASTIC	IM7114L2CPN	IM7114L3CPN	IM7114LCPN
C	370mW	PLASTIC	IM2114L2CPN (P2114L2)	IM2114L3CPN (P2114L3)	IM2114LCPN (P2114L)
C	525mW	PLASTIC	IM2114-2CPN (P2114-2)	IM2114-3CPN (P2114-3)	IM2114CPN (P2114)

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ABSOLUTE MAXIMUM RATINGS

Operating Temperature MD2114 ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Voltage on Any Pin to Ground ..... −0.5V to +7V
Power Dissipation 1W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

AC CHARACTERISTICS

MD2114: V_{CC} = +5V ±10%, T_A = −55°C to +125°C
7114, 2114: V_{CC} = +5V ±5%, T_A = 0°C to +70°C
t_T = 10ns, V_{IL} = 0.8V, V_{IH} = 2.0V, Output Load = 1 TTL Gate and 100pf

READ CYCLE

SYMBOL	PARAMETER	7114L2 2114L2,2114-2		7114L3, 2114L3, 2114-3		7114L, 2114L 2114		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{RC}	Read Cycle Time	200		300		450		ns
t_A	Access Time		200		300		450	ns
t_{CO}	CS to Output Valid		70		100		100	ns
t_{CX}	CS to Output Active	20		20		20		ns
t_{OTD}	Output Three-State from Deselect	0	60	0	80	0	100	ns
t_{OHA}	Output Hold from Address Change	50		50		50		ns

WRITE CYCLE

SYMBOL	PARAMETER	7114L2, 2114L2 2114-2		7114L3, 2114L3, 2114-3		7114L, 2114L 2114		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{WC}	Write Cycle Time	200		300		450		ns
t_W	Write Time	120		150		200		ns
t_{WR}	Write Release Time	0		0		0		ns
t_{OTW}	Output Three-State from Write	0	60	0	80	0	100	ns
t_{DW}	Data to Write Time Overlap	120		150		200		ns
t_{DH}	Data Hold from Write Time	0		0		0		ns
t_{AW}	Address Setup Time	0		0		0		ns
t_{CW}	CS Select Pulse Width	120		150		200		ns

DC CHARACTERISTICS

MD2114: V_{CC} = +5V ±10%, T_A = −55°C to +125°C
7114, 2114: V_{CC} = +5V ±5%, T_A = 0°C to +70°C

SYMBOL	PARAMETER	7114L		2114L		2114		UNITS	TEST CONDITIONS
		MIN	MAX	MIN	MAX	MIN	MAX		
I_{L1}	Input Load Current		10		10		10	μA	V_{IN} = 0V to 5.25V
I_{LO}	I/O Leakage Current (All Inputs)		10		10		10	μA	CS = 2.4V, $V_{I/O}$ = +0.4V to V_{CC}
I_{CC2}	Power Supply Current		40		65		90	mA	V_{IN} = +5.25V, $I_{I/O}$ = 0mA, T_A = +25°C
I_{CC1}	Power Supply Current		50		70		100	mA	V_{IN} = +5.25V, $I_{I/O}$ = 0mA, T_A = 0°C
I_{CC3}	Power Supply Current				90			mA	V_{IN} = +5.5V, $I_{I/O}$ = 0mA, T_A = −55°C
V_{IL}	Input Low Voltage	−0.5	0.8	−0.5	0.8	−0.5	0.8	V	
V_{IH}	Input High Voltage	2.0	V_{CC}	2.0	V_{CC}	2.0	V_{CC}	V	
V_{OL}	Output Low Voltage		0.4		0.4		0.4	V	I_{OL} = 3.2mA
V_{OH}	Output High Voltage	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	I_{OH} = −200μA

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DEVICE OPERATION

When $\overline{WE}$ is high, the data input buffers are inhibited to prevent erroneous data from getting into the array. As long as $\overline{WE}$ remains high, the data stored cannot be changed by the address Chip Select, or data input voltage levels and timing transitions. The block diagram also shows data storage cannot be changed by $\overline{WE}$, the addresses, not the input data as long as $\overline{CS}$ is high. Either $\overline{CS}$ or $\overline{WE}$ by itself, or in conjunction with the other, can prevent the extraneous writing due to signal transitions.

Data within the array can only be changed during a Write time, defined as the overlap of $\overline{CS}$ low and $\overline{WE}$ low. To prevent the loss of data, the addresses must be properly established during the entire Write time plus t_{WR}.

CAPACITANCE

SYMBOL	PARAMETER	MAX	UNITS	TEST CONDITIONS
$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O} = 0V$
C_{IN}	Input Capacitance	5	pF	$V_{IN} = 0V$

TIMING DIAGRAMS

READ CYCLE

WRITE CYCLE

7114/2114 BIT MAP

PHYSICAL DIMENSIONS

CERDIP PACKAGE

18 LEAD CERDIP (JN)

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INTERSIL

2147
NMOS Static RAM
4096 Bit (4096 x 1)
Preliminary

FEATURES

- High speed — 55nS maximum access time (2147-3)
- Automatic low-power standby — 20mA maximum (2147)
- Completely static — no clock required
- Single +5V supply
- TTL compatible inputs and outputs
- Three-state outputs
- High-density SELOX III process technology
- Intel 2147 compatible

GENERAL DESCRIPTION

The Intersil 2147 is a high-speed 4096-bit static RAM organized as 4096 words by 1 bit, fabricated with Intersil's SELOX III, single-layer poly, selective-oxidation process. Innovative design techniques result in minimum cell area and optimum circuit performance.

Inputs and three-state outputs are TTL compatible and allow for direct interfacing with common system bus structures.

An automatic low-power standby mode is controlled by chip select ($\overline{S}$); less than one cycle time after $\overline{S}$ goes high, power dissipation drops from a maximum of 160mA to 20mA (2147).

The basic device operates over the 5V ±5% range with a worst-case access time of 70ns. A "-3" device is available with 55ns worst-case access time.

The Intersil 2147 is supplied in an 18-pin package with industry standard pin configuration.

LOGICAL BLOCK DIAGRAM

PIN CONFIGURATION

LOGIC SYMBOL

PIN NAMES

A0-A11	ADDRESS INPUTS
D	DATA INPUT
Q	DATA OUTPUT
$\overline{S}$	CHIP SELECT
$\overline{W}$	WRITE ENABLE

ORDERING INFORMATION

PART NO.	ACCESS TIME	ACTIVE CURRENT	STANDBY CURRENT	PACKAGE	TEMP RANGE
2147	70nS	160mA	20mA	18-pin CERDIP	0°C to +70°C
2147-3	55nS	180mA	30mA	18-pin CERDIP	0°C to +70°C

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
VIN	Voltage on any Pin Relative to GND	−0.5	+7	V	2
IOS	Short Circuit Output Current		20	mA	
TSTORE	Storage Temperature	−65	+150	°C	
TBIAS	Ambient Temperature Under Bias	−10	+85	°C	
PD	Power Dissipation		1	W	

NOTES:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.
2. This device contains internal circuitry to protect against damage due to static charge. Conventional precautions should be observed, however, during storage, handling, and use to avoid exposure to excessive voltages.

ELECTRICAL PARAMETERS[1] VCC = 5V ±5%, TA = 0°C to +70°C, unless otherwise noted

SYMBOL	DESCRIPTION	2147			2147-3			UNITS	NOTES
		MIN	TYP[1]	MAX	MIN	TYP[1]	MAX		
VIH	Input HIGH Voltage	2.0		6.0	2.0		6.0	V	
VIL	Input LOW Voltage	−0.3		0.8	−0.3		0.8	V	
IIL	Input Leakage Current		0.01	10		0.01	10	μA	2
VOH	Output HIGH Voltage	2.4			2.4			V	3
VOL	Output LOW Voltage			0.4			0.4	V	4
IOZ	Output Leakage Current		0.1	50		0.1	50	μA	5
ICCOP1	Operating Supply Current		50	150		60	170	mA	6, 7
ICCOP2	Operating Supply Current			160			180	mA	6, 8
ICCSB	Standby Supply Current		10	20		15	30	mA	9
ICCPON	Peak Power-On Supply Current		25	50		35	70	mA	10

NOTES:
1. Typical values are measured at VCC = 5.0V, TA = 25°C and are not guaranteed.
2. VCC = 5.25V, GND ≤ VIN ≤ VCC
3. IOH = −4.0mA
4. IOL = 8mA
5. VCC = 5.25V, $\overline{S}$ = VIH, GND ≤ VO ≤ 4.5V
6. VCC = 5.25V, $\overline{S}$ = VIL, IO = 0
7. TA = 25°C
8. TA = 0°C
9. VCC = 4.75 to 5.25V, $\overline{S}$ = VIH
10. VCC = GND to 4.75V, $\overline{S}$ = lower of VCC or VIH min. A pullup resistor on $\overline{S}$ is required during power-on in order to keep the device deselected; otherwise ICCPON approaches ICCOP. VCC slew rate _ 1V/μS.

TIMING PARAMETERS VCC = 5V ±5%, TA = 0°C to +70°C, unless otherwise noted

SYMBOL	DESCRIPTION	JEDEC SYMBOL	2147		2147-3		UNITS	NOTES
			MIN	MAX	MIN	MAX		
	READ CYCLE							
tRC	Read Cycle Time		70		55			
tAA	Address Access Time	TAVQV		70		55		
tASC1	Chip Select Access Time	TSLQV		70		55		2
tASC2	Chip Select Access Time	TSLQV		80		65		3
tOH	Output Hold from Address Change	TAXQX	5		5			
tLZ	Chip Selection to Output Enabled	TSLQX	10		10			
tHZ	Chip Deselection to Output Disabled	TSHQZ	0	40	0	40		
tPU	Chip Deselection to Power Up Time		0		0			
tPD	Chip Deselection to Power Down Time			30		30		
	WRITE CYCLE						ns	
tWC	Write Cycle Time		70		55			
tCW	Chip Selection to End of Write	TSLWH	55		45			
tAW	Address Valid to End of Write	TAVWH	55		45			
tAS	Address Setup Time	TAVWL	0		0			
tWP	Write Pulse Width	TWLWH	40		35			
tWR	Write Recovery Time	TWHAX	15		10			
tDW	Data Valid to End of Write	TDVWH	30		25			
tDH	Data Hold Time	TWHDX	10		10			
tWZ	Write Enabled to Output Disabled	TWLQZ	0	35	0	30		
tOW	Output Active from End of Write	TWHQX	0	35	0	30		

NOTES:
1. tR = tF = 10ns. Input and output timing reference level = 1.5V.
2. Device deselected for 55ns or more prior to selection.
3. Device deselected for a finite time less than 55ns prior to selection.

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TIMING DIAGRAMS

Read Cycle (Address)

Read Cycle (Chip Select)

Write Cycle

PRINTED CIRCUIT LAYOUT

PACKAGE DIMENSIONS

18-pin CERDIP*

*Hermetic: Maximum leakage rate 5 x 10^{-7} atm. cc/sec.

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INTERSIL

IM7027/MK4027 Dynamic RAM 4096 Bit (4K x 1)

FEATURES

- 4096 X 1 Bit Organization
- Gated $\overline{CAS}$
- $\overline{RAS}$ Only Refresh
- All Inputs TTL Compatible
- On-Chip Latches for Addresses, Chip Select and Data In
- 10% Supply Tolerances (+12V, +5V, -5V)
- Three-State TTL Compatible Output
- Low Power Dissipation
  —470 mW Operating
  — 27 mW Standby
- Chip Select Decode Does Not Add to Access Time
- Output Data Latched and Valid Into Next Cycle
- N-Channel Silicon Gate Technology
- Pin and Performance Compatibility with Mostek MK4027

GENERAL DESCRIPTION

The IM7027 is a 4096 X 1 bit dynamic random access memory which is packaged in 16 pin DIP. The cell array is organized into 64 rows of 64 cells. Each of the 64 row addresses requires refreshing every 2 milliseconds. Any read cycle refreshes the selected row as does a refresh cycle using $\overline{RAS}$ only. A write, read/write or read/modify/write cycle also refreshes the selected row, but non-accessed chips should not be selected to avoid writing data into the selected row. A page-mode feature is included to reduce the access and/or cycle time for block data operations. Page-mode operation is useful in direct memory access (DMA) operations.

System oriented features include direct interfacing with TTL, on-chip registers which eliminate the need for interface registers, logic input levels selected for best noise immunity. Twelve address bits are required to decode 1 of 4096 cell locations, and are multiplexed onto 6 address pins and latched into the row and column address latches. The Row Address Strobe ($\overline{RAS}$) latches the 6 row address bits onto the chip. The Column Address Strobe ($\overline{CAS}$) latches the 6 column address bits and Chip Select ($\overline{CS}$) onto the chip. Since the Chip Select signal is not required until well into the cycle, its decoding time does not add to the system address or cycle time.

PIN CONFIGURATION

LOGIC SYMBOL

BLOCK DIAGRAM

ORDERING INFORMATION

ORDER NUMBER	ACCESS TIME	CYCLE TIME	PACKAGE	EQUIVALENT
IM7027-1CJE	120 ns	250 ns	16 PIN CERDIP	—
IM7027-2CJE	150 ns	320 ns	16 PIN CERDIP	MK4072P-2
IM7027-3CJE	200 ns	375 ns	16 PIN CERDIP	MK4027P-3
IM7027-4CJE	250 ns	375 ns	16 PIN CERDIP	MK4027P-4

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ABSOLUTE MAXIMUM RATINGS

Operating Temperature . . . . . 0°C to +70°C
Storage Temperature . . . . . -55°C to +150°C
Voltage On Any Pin w/Respect to V_{BB} . . . . . -0.5V to +20.0V
Power Dissipation 1W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

DC CHARACTERISTICS

TEST CONDITIONS: V_{DD} = +12.0V ± 10%, V_{CC} = +5.0V ±10%, V_{SS} = 0V, V_{BB} = -5.0V ±10%, T_A = 0°C to +70°C

	SYMBOL	PARAMETER		MIN	MAX	UNITS	NOTES
1	V_{IHC}	$\overline{RAS}$, $\overline{CAS}$, $\overline{WRITE}$ Voltage High		2.4	7.0	V	
2	V_{IH}	Input Voltage High		2.2	7.0	V	
3	V_{IL}	Input Voltage Low		-1.0	0.8	V	
4	$I_{I(L)}$	Input Leakage Current			10	μA	4
5	$I_{O(L)}$	Output Leakage Current			10	μA	5, 6
6	I_{DD1}	Average V_{DD} Power Supply Current			35	mA	2
7	I_{CC}	V_{CC} Power Supply Current					3
8	I_{BB}	Average V_{BB} Power Supply Current	-2, -3, -4		300	μA	
			-1		400	μA	
9	I_{DD2}	Standby V_{DD} Power Supply Current			2	mA	5
10	I_{DD3}	Average V_{DD} Current ("$\overline{RAS}$ Only" Refresh)			25	mA	
11	V_{OH}	Output Voltage High I_{OH} = -5 mA		2.4		V	
12	V_{OL}	Output Voltage Low I_{OL} = 3.2 mA			0.4	V	

NOTES:
1. V_{BB} must be applied before and removed after other supply voltages.
2. I_{DD1} (max) measured at t_{RC} (min). I_{DD1} is proportional to cycle rate.
3. I_{CC} depends on output loading.
4. All pins except V_{BB} at 0V, V_{BB} = -5V and test pin = +10V.
5. Output disabled, $\overline{RAS}$ and $\overline{CAS}$ $\geqslant V_{IHC}$ (min).
6. 0V $\leqslant V_{OUT} \leqslant$ +10V.

TIMING DIAGRAMS

READ AND REFRESH CYCLE

WRITE CYCLE

RAS ONLY REFRESH CYCLE

READ/WRITE CYCLE

TIMING DIAGRAMS (Continued)

PAGE MODE READ CYCLE

PAGE MODE WRITE CYCLE

AC CHARACTERISTICS

TEST CONDITIONS: V_{DD} = +12.0V ± 10%, V_{CC} = +5.0V ± 10%, V_{SS} = 0V, V_{BB} = −5.0V ± 10%, T_A = 0°C to +70°C (NOTES 1, 5 and 8)

	SYMBOL	PARAMETER	IM7027-1CJE		MK4027 P-2		MK4027 P-3		MK4027 P-4		UNITS	NOTES
			MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX		
1	t_{RC}	Random Read or Write Cycle Time	250		320		375		375		ns	2
2	t_{RWC}	Read Write Cycle Time	325		330		420		480		ns	
3	t_{RAC}	Access Time from Row Address Strobe		120		150		200		250	ns	3
4	t_{CAC}	Access Time from Column Address Strobe		80		100		135		165	ns	3
5	t_{OFF}	Output Buffer Turn-off Delay		40		40		50		60	ns	
6	t_{RP}	Row Address Strobe Precharge Time	80		100		120		120		ns	
7	t_{RAS}	Row Address Strobe Pulse Width	120	10,000	150	10,000	200	10,000	250	10,000	ns	
8	t_{RSH}	Row Address Strobe Hold Time	80		100		135		165		ns	
9	t_{CAS}	Column Address Strobe Pulse Width	80		100		135		165		ns	
10	t_{RCD}	Row to Column Strobe Delay	20	40	20	50	25	65	35	85	ns	4
11	t_{ASR}	Row Address Set-up Time	0		0		0		0		ns	
12	t_{RAH}	Row Address Hold Time	20		20		25		35		ns	
13	t_{ASC}	Column Address Set-up Time	0		−10		−10		−10		ns	
14	t_{CAH}	Column Address Hold Time	45		45		55		75		ns	
15	t_{AR}	Column Address Hold Time Referenced to $\overline{RAS}$	95		95		120		160		ns	
16	t_{CSC}	Chip Select Set-up Time	−10		−10		−10		−10		ns	
17	t_{CH}	Chip Select Hold Time	45		45		55		75		ns	
18	t_{CHR}	Chip Select Hold Time Referenced to $\overline{RAS}$	95		95		120		160		ns	
19	t_T	Transition Time (Rise and Fall)	3	35	3	35	3	50	3	50	ns	
20	t_{RCS}	Read Command Set-up Time	0		0		0		0		ns	
21	t_{RCH}	Read Command Hold Time	0		0		0		0		ns	
22	t_{WCH}	Write Command Hold Time	45		45		55		75		ns	
23	t_{WCR}	Write Command Hold Time Referenced to $\overline{RAS}$	95		95		120		160		ns	
24	t_{WP}	Write Command Pulse Width	45		45		55		75		ns	
25	t_{RWL}	Write Command to Row Strobe Lead Time	50		50		70		85		ns	
26	t_{CWL}	Write Command to Column Strobe Lead Time	50		50		70		85		ns	
27	t_{DS}	Data in Set-up Time	0		0		0		0		ns	7
28	t_{DH}	Data in Hold Time	45		45		55		75		ns	7
29	t_{DHR}	Data in Hold Time Referenced to $\overline{RAS}$	95		95		120		160		ns	
30	t_{CRP}	Column to Row Strobe Precharge Time	0		0		0		0		ns	
31	t_{CP}	Column Precharge Time	60		60		80		110		ns	
32	t_{RFSH}	Refresh Period		2		2		2		2	ms	
33	t_{WCS}	Write Command Set-up Time	0		0		0		0		ns	6
34	t_{CWD}	$\overline{CAS}$ to $\overline{WRITE}$ Delay	60		60		80		90		ns	6
35	t_{RWD}	$\overline{RAS}$ to $\overline{WRITE}$ Delay	110		110		145		175		ns	6
36	t_{DOH}	Data Out Hold Time	10		10		10		10		ns	

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NOTES 1: t_T = 5 ns unless otherwise noted.
2: $t_{RC} > t_{RAS} + t_{RP} + 2\,t_T$ to limit power dissipation.
3: Load = 2TTL + 100 pF.
4: If t_{RCD} is greater than t_{RCD} (max) access time is controlled by t_{CAC}.
5: V_{IHC} (min), V_{IH} (min) and V_{IL} (max) are reference levels.
6: t_{WCS}, t_{CWD} and t_{RWD} are not restrictive parameters, they are electrical characteristics only as follows:
a. $t_{CWD} + t_T \leq t_{CWD}$ minimum output latch contains data written into current address.
b. $t_{CWD} \geq t_{CWD}$ (max) + t_T and $t_{RWD} \geq t_{RWD}$ (max) + t_T the data output latch contains data read from the current address.
c. If t_{CWD} does not meet the above, data output state is indeterminate.
7: Referenced to latest of $\overline{CAS}$ or $\overline{WRITE}$.
8: Any 8 cycles that perform refresh are required after power is applied.

TYPICAL DEVICE CHARACTERISTICS

TYPICAL ADDRESS DATA INPUT LEVELS VS. V_{DD}

TYPICAL DATA OUTPUT LEVEL VS. V_{DD}

TYPICAL I_{DD} CURRENT VS. OPERATING TEMPERATURE

TYPICAL I_{DD} CURRENT VS. OPERATING TEMPERATURE

TYPICAL I_{BB} CURRENT VS. OPERATING TEMPERATURE

TYPICAL t_{CAC} ACCESS TIME VS. V_{DD}

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TYPICAL DEVICE CHARACTERISTICS (Continued)

TYPICAL I_{DD} CURRENT VS. CYCLE TIME

TYPICAL t_{CAC} VS. t_{RCL}

BIT MAP

The memory cells are divided into 2 groups each organized as 64 rows by 32 columns. The column addresses run in pure binary order for Y_5 Y_4 Y_3 Y_2 Y_1 Y_0, where Y_5 is most significant. The row addresses run in binary order for X_5 X_4 X_3 X_2 X_1 X_0 except for X_1 and X_0 which run 1, 0, 2, 3 and repeat. The folded bit line approach requires that data be be stored either true or false depending on the row selected. If X_0 is at logic "0", data is stored true. If X_0 is at logic "1", data is stored false.

MAXIMUM STRESS VOLTAGES

It is of interest to know worst case stress voltages for power supply failure and/or turn-on conditions. The 7027 can tolerate combinations of V_{BB}, V_{DD} that operate within the curves of the figure shown below.

CAPACITANCE

TEST CONDITIONS: V_{IN} = OV, f = 1 MHz (NOTE 1)

	SYMBOL	PARAMETER	TYP	MAX	UNIT
1	C_{I1}	D_{IN}, $\overline{CS}$ Input Capacitance A_0 - A_5	3	5	pF
2	C_{I2}	Input Capacitance, $\overline{RAS}$, $\overline{CAS}$ $\overline{WRITE}$	5	7	
3	C_O	Output Capacitance, D_{OUT}	5	7	

NOTE 1: These parameters are characterized and periodically sampled but not 100% tested.

PACKAGE DIMENSIONS

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INTERSIL

IM4116/MK4116
16,384 Bit
NMOS Dynamic RAM

FEATURES

- Industry Standard 16-pin configuration
- Standard 10% Supplies (+12V, +5V, −5)
- Low Capacitance TTL Compatible Inputs
- TTL Compatible 3-State Outputs Controlled by CAS
- On-chip Address and Data Latches
- Common I/O Capability Using "Early Write" Cycle
- Read-Modify-Write, RAS-only Refresh, Page Mode Operation
- 128-Cycle RAS-Only Refresh
- Compatible with MOSTEK MK4116
- Read Access

4116-2	150 nS
4116-3	200 nS
4116-4	250 nS

- Page Mode Access

4116-2	100 nS
4116-3	135 nS
4116-4	165 nS

GENERAL DESCRIPTION

The Intersil IM4116/MK4116 is a 16,384-bit dynamic random access memory employing the latest advances in N-channel silicon-gate MOS technology. The use of double-level poly allows the highest possible density consistent with reliability, high performance and low cost.

The basic memory element is a single transistor which stores charge on a small capacitor. These dynamic memory "cells" are organized into an array of 128 rows by 128 columns. Each of the 128 rows requires refreshing at least every two milliseconds. This refresh may be accomplished on a given row by any read or $\overline{RAS}$-only cycle. A page-mode feature is included which reduces access and/or cycle time when multiple operations are performed within the same row.

All inputs and outputs are TTL compatible. On-chip address registers and three-state outputs simplify system design and allow for interfacing with common bus structures.

The device is packaged in a standard 16-pin DIP, providing high system bit density and compatibility with automatic testing and insertion equipment.

LOGICAL BLOCK DIAGRAM

PIN CONFIGURATION

Top View

ORDERING INFORMATION

ORDER CODE	ACCESS TIME NORMAL	ACCESS TIME PAGE	EQUIPMENT	PACKAGE
IM4116-2CJE	150ns	100ns	MK4116J-2	CERDIP
IM4116-2CDE	150ns	100ns	MK4116P-2	CERAMIC
IM4116-2CPE	150ns	100ns	—	PLASTIC
IM4116-3CJE	200ns	135ns	MK4116J-3	CERDIP
IM4116-3CDE	200ns	135ns	MK4116P-3	CERAMIC
IM4116-3CPE	200ns	135ns	—	PLASTIC
IM4116-4CJE	250ns	165ns	MK4116J-2	CERDIP
IM4116-4CDE	250ns	165ns	MK4116P-2	CERAMIC
IM4116-4CPE	250ns	165ns	—	PLASTIC

LOGIC SYMBOL

PIN NAMES MNEMONIC	PIN NAMES JEDEC	DESCRIPTION
A0-A6	A0-A6	Address Inputs
$\overline{CAS}$	$\overline{CE}$	Column Address Strobe
DI	D	Data In
DO	Q	Data Out
$\overline{RAS}$	$\overline{RE}$	Row Address Strobe
VBB	VBB	Power (−5V)
VCC	VCC	Power (+5V)
VDD	VDD	Power (+12V)
VSS	VSS	Ground
$\overline{WE}$	$\overline{W}$	Write Enable

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ABSOLUTE MAXIMUM RATINGS[1]

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
VIN	Voltage on any Pin Relative to VBB	−0.5	+20	V	2, 3
PD	Power Dissipation		1	W	
IOS	Short Circuit Output Current		50	mA	
TSTORE	Storage Temperature	−55	+150	°C	
TA	Ambient Temperature Under Bias	0	+70	°C	

NOTES:
1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.
2. VSS − VBB ≥ 4.5V
3. This device contains internal circuitry to protect against damage due to static charge. Conventional precautions should be observed, however, during storage, handling, and use to avoid exposure to excessive voltages.

OPERATING CONDITIONS[1]

SYMBOL	DESCRIPTION	MIN	MAX	UNITS
VBB	VBB Supply	−4.5	−5.5	V
VCC	VCC Supply	4.5	5.5	V
VDD	VDD Supply	10.8	13.2	V
VSS	VSS Supply	0	0	V
TA	Ambient Temperature Under Bias	0	+70	°C

NOTE: VBB must be applied prior to and removed after other supply voltages.

ELECTRICAL PARAMETERS VDD = +12V ± 10%, VCC = +5V ± 10%, VSS = 0V, VBB = −5V ± 10%, TA = 0° C to +70° C

SYMBOL	DESCRIPTION	MIN	MAX	UNITS	NOTES
IDD1	Average Operating Supply Currents		35	mA	
ICC1	(RAS, CAS cycling; tRC = tRC (min))				1
IBB1			200	μA	
IDD2	Standby Supply Current		1.5	mA	
ICC2	($\overline{RAS}$ = VIHC)	−10	10	μA	
IBB2			100	μA	
IDD3	Average Refresh Supply Currents		27	mA	
ICC3	($\overline{RAS}$ Cycling, CAS = VIHC; tRC = tRC (Min))	−10	10	μA	
IBB3			200	μA	
IDD4	Average Page Mode Supply Current		27	mA	
ICC4	($\overline{RAS}$ = VIL, CAS cycling; tPC = tPC (min))				1
IBB4			200	μA	
VIH	Input HIGH Voltage (A, DI)	2.4	7.0	V	
VIH1	Input HIGH Voltage ($\overline{RAS}$, $\overline{CAS}$, $\overline{WE}$)	2.7	2.7	V	
VIL	Input LOW Voltage	−1.0	+0.8	V	
IIL	Input Leakage Current	−10	+10	μA	
VOH	Output HIGH Voltage	2.4		V	
VOL	Output LOW Voltage		0.4	V	
IOZ	Output Leakage Current	−10	+10	μA	3, 4
CIN	Input Capacitance (A)		5	pF	2
CIN1	Input Capacitance ($\overline{RAS}$, $\overline{CAS}$, $\overline{DI}$, $\overline{WE}$)		10	pF	2
CO	Output Capacitance (DO)		7	pF	2

NOTES: **1.** ICC1 and ICC4 depend upon output loading.
2. These parameters characterized and periodically sampled; not 100% tested.
3. $0V \leq V_{OUT} \leq 10V$
4. $\overline{RAS} = \overline{CAS} = V_{IH}$

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TIMING PARAMETERS[1, 2, 3] VDD = +12V ± 10%, VCC = +5V ± 10%, VSS = 0V, VBB = −5V ± 10%, TA = 0°C to +70°C

SYMBOL			MK4116-2		MK4116-3		MK4116-4			
MNEMONIC	JEDEC[8]	DESCRIPTION	MIN	MAX	MIN	MAX	MIN	MAX	UNITS	NOTES
tAR	TRELAX (C)	$\overline{RAS}$ LOW to Column Address Hold Time	95		120		160			
tASC	TAVCEL	Column Address Set-up Time	−10		−10		−10			
tASR	TAVREL	Row Address Set-up Time	0		0		0			
tCAC	TCELQV	Access Time from $\overline{CAS}$		100		135		165		4
tCAH	TCELAX	$\overline{CAS}$ LOW to Column Address Hold Time	45		55		75			
tCAS	TCELCEH	$\overline{CAS}$ Pulse Width	100	10000	135	10000	165	10000		
tCP	TCEHCEL	Page Mode $\overline{CAS}$ Precharge Time	60		80		100			
tCRP	TCEHREL	$\overline{CAS}$ to $\overline{RAS}$ Precharge Time	−20		−20		−20			
tCSH	TRELCEH	$\overline{RAS}$ LOW to $\overline{CAS}$ HIGH Delay	150		200		250			
tCWD	TCELWL	$\overline{CAS}$ LOW to $\overline{WE}$ LOW Delay	70		95		125			5
tCWL	TWLCEH	$\overline{WE}$ LOW to $\overline{CAS}$ HIGH Set-up Time	60		80		100			
tDH	TCELDX or TWLDX	$\overline{CAS}$ LOW or $\overline{WE}$ LOW to Data In Valid Hold Time	45		55		75		nS	6
tDHR	TRELDX	$\overline{RAS}$ LOW to Data In Valid Hold Time	95		120		160			
tDS	TDVCEL or TDVWL	Data In Stable to $\overline{CAS}$ LOW or $\overline{WE}$ LOW Set-up Time	0		0		0			6
tOFF	TCEHQZ	$\overline{CAS}$ HIGH to Output OFF Delay	0	40	0	50	0	60		
tPC	TCELCEL (P)	Page Mode Cycle Time	170		225		275			
tRAC	TRELQV	Access Time from $\overline{RAS}$		150		200		250		4
tRAH	TRELAX (R)	$\overline{RAS}$ LOW to Row Address Hold Time	20		25		35			
tRAS	TRELREH	$\overline{RAS}$ Pulse Width	150	10000	200	10000	250	10000		
tRC	TRELREL	Random Read or Write Cycle Time	375		375		410			
tRCD	TRELCEL	$\overline{RAS}$ LOW to $\overline{CAS}$ LOW Delay	20	50	25	65	35	85		7
tRCH	TCEHWX	Read Hold Time	0		0		0			
tRCS	TWHCEL	Read Set-up Time	0		0		0			
tREF		Refresh Interval		2		2		2	mS	
tRMW	TRELREL (RMW)	Read-Modify-Write Cycle Time								
tRP	TREHREL	$\overline{RAS}$ Precharge Time	100		120		150			
tRSH	TCELREH	$\overline{CAS}$ LOW to $\overline{RAS}$ HIGH Delay	100		135		165			
tRWC	TRELREL (R/W)	Read/Write Cycle Time	375		375		515			
tRWD	TRELWL	$\overline{RAS}$ LOW to $\overline{WE}$ LOW Delay	120		160		200		nS	
tRWL	TWLREH	$\overline{WE}$ LOW to $\overline{RAS}$ HIGH Set-up Time	60		80		100			
tT		Transition Time	3	35	3	50	3	50		3
tWCH	TCELWH	Write Hold Time	45		55		75			
tWCR	TRELWH	$\overline{RAS}$ LOW to Write Hold Time	95		120		160			
tWCS	TWLCEL	$\overline{WE}$ LOW to $\overline{CAS}$ LOW Set-up Time	−20		−20		−20			5
tWP	TWLWH	Write Pulse Width	45		55		75			

NOTES:
1. Several cycles are required after power-up before proper device operation is achieved. Any eight cycles which perform refresh are adequate for this purpose.
2. Unless otherwise noted, tRISE = tFALL = 5nS
3. VIHC (min), VIH (min) and VIL (max) are reference levels for timing measurements.
4. Loading equivalent to two TTL inputs +100 pF
5. tWCS, tCWD, and tRWD are not restrictive operating parameters. They are included in the datasheet as electrical characteristics only: for tWCS ≥ TWCS (min), the cycle is an early-write cycle and the data output will remain high-impedance throughout the entire cycle; for tCWD > tCWD (min) and tRWD ≥ tRWD (min), the cycle is a read-write cycle and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data output (at access time) is indeterminate.
6. For positive tWCS these parameters are referenced to CAS. For negative tWCS, or read-write cycles these parameters are referenced to $\overline{WE}$.
7. For tRCD ≥ tRCD (max), access time is controlled by tCAC.

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FUNCTIONAL DESCRIPTION

Addressing

Fourteen address bits are required to select one of the 4116's 16,384 possible bit locations. These 14 address bits are latched on-chip in two groups of seven bits. The Row Address Strobe ($\overline{RAS}$) latches the 7-bit row address on its falling edge; similarly, the 7-bit column address is latched by $\overline{CAS}$.

The normal sequence of events is as follows: First, the 7-bit row address is applied to the address inputs. At the end of the row address setup time (tASR), $\overline{RAS}$ is brought LOW. After the row address hold time (tRAH) has elapsed, the 7-bit column address is applied and $\overline{CAS}$ is brought LOW.

The column address information is not used internally until tRCD (max) after $\overline{RAS}$-falls. Further, $\overline{CAS}$, is gated with the $\overline{RAS}$ clock generator such that it may occur at any time from tRCD (min) to tRCD (max), without effecting access time. If $\overline{CAS}$ occurs after tRCD (max) the access time will be lengthened by the delay from tRCD (max) to $\overline{CAS}$.

Page Mode Operation

Successive memory cycles accessing the same row in the memory array require the row address and $\overline{RAS}$ to be supplied only once. Further accesses to the same row require only column addresses and $\overline{CAS}$, with $\overline{RAS}$ held LOW.

In addition to savings in access and cycle time, page mode operation results in reduced power consumption since dynamic power due to $\overline{RAS}$ transitions is drawn only once per row address.

Data Input

Data to be written is strobed into the on-chip data latch by a combination of $\overline{CAS}$ and $\overline{WE}$ while $\overline{RAS}$ is active. Whichever of $\overline{CAS}$ and $\overline{WE}$ makes the later negative-going transition serves as the data strobe. Several different write cycles are made possible by this flexibility.

An "early-write" cycle takes place if $\overline{WE}$ goes LOW before $\overline{CAS}$. In the case where data-in (DI) is not valid when $\overline{CAS}$ goes LOW, $\overline{WE}$ must be delayed until after $\overline{CAS}$ falls. In this "delayed-write" cycle, data setup and hold times are referenced to the negative-going edge of $\overline{WE}$, rather than $\overline{CAS}$.

Data Output

The data output (DO) unconditionally assumes the high-impedance state wherever $\overline{CAS}$ is HIGH. For read, read-modify-write, or delayed-write cycles, DO remains high-impedance until access time, at which time it will reflect the logic state of the addressed cell. DO remains high-impedance in an early-write cycle, or in cycles where $\overline{RAS}$ and $\overline{CAS}$ are not both received. Thus, in systems which utilize early-write cycles exclusively, DI, and DO may be connected together with no conflict.

Input/Output Levels

All inputs, including $\overline{RAS}$ and $\overline{CAS}$, are low-capacitance high-impedance, and TTL-level compatible. Special clock drivers are not required, simplifying input driver design.

In order to prevent ringing, signal termination resistors are usually necessary. In general, transmission line techniques must be utilized on signal lines to achieve maximum system speeds.

Refresh

Any cycle in which $\overline{RAS}$ occurs serves to refresh the selected row. However, it is generally more convenient (and requires substantially less power) to perform the refresh operation using the $\overline{RAS}$-only cycle. Each of the 128 rows must be refreshed at least once per two milliseconds.

Power Sequencing

VBB should be applied before and removed after other supply voltages. Under system failure conditions in which one or more supplies exceed the specified limit, significant additional margin against catastrophic device failure may be achieved by forcing $\overline{RAS}$ and $\overline{CAS}$ to the inactive state.

After power is applied, the MK4116 requires several cycles before proper device operation is achieved. Any eight cycles which perform refresh are adequate for this purpose.

Power Dissipation

Because of the extensive use of dynamic circuitry in the MK4116, most of the dissipated power is as a result of a transition on $\overline{RAS}$ or $\overline{CAS}$. Thus, the dynamic power is primarily a function of operating frequency. Worst case power dissipation is 462 MW at 375nS cycle time.

VCC is utilized only to power the output buffer, and is not connected elsewhere; ICC, is thus a function only of output loading. VCC may be left unconnected for battery-backup operation.

READ CYCLE

EARLY WRITE CYCLE

PAGE MODE READ CYCLE

PAGE MODE WRITE CYCLE

READ-WRITE/READ MODIFY-WRITE CYCLE

RAS-only REFRESH CYCLE

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PACKAGE DIMENSIONS

18-pin CERDIP (J)*

*Hermetic: Maximum leakage rate 5 x 10^{-7} atm. cc/sec.

TYPICAL CHARACTERISTICS

TYPICAL ACCESS TIME (NORMALIZED) vs. V_{DD}

TYPICAL IDDAV vs. V_{DD}

TYPICAL IDDAV vs. JUNCTION TEMPERATURE

TYPICAL ACCESS TIME (NORMALIZED) vs. V_{DD}

TYPICAL IDDSB vs. V_{DD}

TYPICAL IDDSB vs. JUNCTION TEMPERATURE

TYPICAL ACCESS TIME (NORMALIZED) vs. V_{CC}

TYPICAL IDDRAV vs. V_{DD}

TYPICAL IDDRAV vs. JUNCTION TEMPERATURE

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TYPICAL ACCESS TIME (NORMALIZED) vs. JUNCTION TEMPERATURE

TYPICAL IDDPAV vs. V_{DD}

TYPICAL IDDPAV vs. JUNCTION TEMPERATURE

TYPICAL CLOCK INPUT LEVELS vs. V_{DD}

TYPICAL CLOCK INPUT LEVELS vs. V_{BB}

TYPICAL CLOCK INPUT LEVELS vs. T_J

TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{DD}

TYPICAL ADDRESS AND DATA INPUT LEVELS vs. V_{BB}

TYPICAL ADDRESS AND DATA INPUT LEVELS vs. T_J

SYMBOLS AND ABBREVIATIONS

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates HIGH (H), LOW (L) or off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IOZ — Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:

T X X X X

Signal name from which interval is defined
Transition direction for first signal
Signal name to which interval is defined
Transition direction for second signal

Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S Chip Select
G Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:

The example shows write-pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	——	HIGH IMPEDANCE

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INTERSIL

IM6512/IM6512A CMOS RAM 768 BIT (64 x 12)

FEATURES

- Low Power Operation
- TTL or CMOS Compatible on Inputs and Outputs
- 4V-11V V_{CC} Operation
- Static Operation
- On-Chip Address Register
- Two IM6512's can be used with IM6100 and IM6312 without additional components

GENERAL DESCRIPTION

The IM6512 is a high speed, low power, silicon gate CMOS 768 bit static RAM organized 64 words by 12 bits. In all static states these units exhibit the microwatt power requirements typical of CMOS. Inputs and three state outputs are TTL compatible. The basic part operates at 4-7 volts with a typical 5 volt, 25° C access time of 350ns. A wider operating voltage range, 4-11 volts, is available with the A version. Signal polarities and functions are specified for direct interfacing with the IM6100 microprocessor. The device is ideally suited for minimum system all CMOS applications where low power, minimum cost, or non-volatility is required.

FUNCTIONAL DESCRIPTION

The MSEL pin performs both chip enable and write-enable functions. The IM6512 has three modes of operation: read-modify-write, read only, and write. The ADR input allows two IM6512's to be used without additional decoding circuitry.

PACKAGE DIMENSIONS

18 LEAD CERAMIC DIP

18 LEAD CERDIP

CONNECTION DIAGRAM

18 LEAD FLAT PACK

ORDERING INFORMATION

MEMORY CIRCUIT AND PRODUCT CODE EXPLANATION:

IM 6 5 12A I DN

- Package
  - DN - Ceramic 18 pin DIP
  - JN - Cerdip 18 pin
  - FN - Flatpack 18 pin
- Temperature
  - C - Commercial (0 C to +70 C)
  - I - Industrial (−40 C to +85 C)
  - M - Military (−55 C to +125 C)
- Specific Type
- General Type
  - Random Access Memory (RAM)
- DCMOS Product
- INTERSIL INC.

FUNCTIONAL DIAGRAM IM6512/12A

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+12.0V
Input or Output Voltage Applied	GND − 0.3V to V_{CC} +0.3V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Industrial IM6512AI	−40°C to +85°C
Military IM6512AM	−55°C to +125°C

DC CHARACTERISTICS V_{CC} = 4V to 11V, T_A = Industrial or Military

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		70% V_{CC}			V
Logical "0" Input Voltage	V_{IL}				20% V_{CC}	V
Input Leakage	I_{IL}	$0V \leqslant V_{IN} \leqslant V_{CC}$	−1.0		1.0	μA
Logical "1" Output Voltage	V_{OH}	$I_{OUT} = 0$	V_{CC}−0.01			V
Logical "0" Output Voltage	V_{OL}	$I_{OUT} = 0$			GND+0.01	V
Output Leakage	I_O	$0V \leqslant V_O \leqslant V_{CC}$	−1.0		1.0	μA
Supply Current	I_{CC}	*		5.0	500	μA
	I_{CC}	*V_{CC} = 3.0V		0.1	10.0	μA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	pF

* STR = V_{CC}, all other inputs = V_{CC} or GND

AC CHARACTERISTICS V_{CC} = 10V, C_L = 50pF, T_A = 25°C

PARAMETER	SYMBOL	IM6512A		UNITS
		MIN	MAX	
Access Time From STR	t_{AC}		150	ns
Output Enable Time	t_{EN}		90	ns
Output Disable Time	t_{DIS}		90	ns
STR Pulse Width (Positive)	t_{STR}	95		ns
STR Pulse Width (Negative)	$t_{\overline{STR}}$	150		ns
Cycle Time	t_C	245		ns
Write Pulse Width (Negative)	t_{WP}	95		ns
Address Setup Time	t_{AS}	20		ns
Address Hold Time	t_{AH}	45		ns
Data Setup Time	t_{DS}	95		ns
Data Hold Time	t_{DH}	0		ns
MSEL Pulse Separation	t_{PS}	60		ns
MSEL Setup Time	t_{MS}	20		ns
MSEL Hold Time	t_{MH}	20		ns

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+8.0V
Input or Output Voltage Supplied	GND −0.3V to V_{CC} +0.3V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Industrial IM6512I	−40°C to +85°C
Military IM6512M	−55°C to +125°C

DC CHARACTERISTICS V_{CC} = 5.0V ±10% T_A = Industrial or Military

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}−2.0			V
Logical "0" Input Voltage	V_{IL}				0.8	V
Input Leakage	I_{IL}	$0V \leqslant V_{IN} \leqslant V_{CC}$	−1.0		1.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OH} = −0.2mA	2.4			V
Logical "0" Output Voltage	V_{OL}	I_{OL} = 2.0mA			0.45	V
Output Leakage	I_O	$0V \leqslant V_O \leqslant V_{CC}$	−1.0		1.0	μA
Supply Current	I_{CC}	*		1.0	100	μA
	I_{CC}	*V_{CC} = 3.0V		0.1	10.0	μA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	pF

* STR = V_{CC}, all other inputs = V_{CC} or GND

AC CHARACTERISTICS V_{CC} = 5.0V ±10%, C_L = 50 pF , T_A = Industrial or Military

PARAMETER	SYMBOL	IM6512		UNITS
		MIN	MAX	
Access Time From STR	t_{AC}		460	ns
Output Enable Time	t_{EN}		285	ns
Output Disable Time	t_{DIS}		285	ns
STR Pulse Width (Positive)	t_{STR}	300		ns
STR Pulse Width (Negative)	$t_{\overline{STR}}$	460		ns
Cycle Time	t_C	760		ns
Write Pulse Width (Negative)	t_{WP}	300		ns
Address Setup Time	t_{AS}	40		ns
Address Hold Time	t_{AH}	130		ns
Data Setup Time	t_{DS}	300		ns
Data Hold Time	t_{DH}	0		ns
MSEL Pulse Separation	t_{PS}	150		ns
MSEL Setup Time	t_{MS}	50		ns
MSEL Hold Time	t_{MH}	50		ns

ABSOLUTE MAXIMUM RATINGS

Supply Voltage	+7.0V
Input or Output Voltage Supplied	GND −0.3V to V_{CC} +0.3V
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	
Commercial IM6512C	0°C to +70°C

DC CHARACTERISTICS V_{CC} = 5.0V ±5%, T_A = Commercial

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}−1.5			V
Logical "0" Input Voltage	V_{IL}				0.8	V
Input Leakage	I_{IL}	$0V \leqslant V_{IN} \leqslant V_{CC}$	−5.0		5.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OH} = −0.2mA	2.4			V
Logical "0" Output Voltage	V_{OL}	I_{OL} = 1.6mA			0.45	V
Output Leakage	I_O	$0V \leqslant V_O \leqslant V_{CC}$	−5.0		5.0	μA
Supply Current	I_{CC}	*			800	μA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	pF

*STR = V_{CC}, all other inputs = V_{CC} or GND

AC CHARACTERISTICS V_{CC} = 5.0V ±5%, C_L = 50 pF , T_A = Commercial

PARAMETER	SYMBOL	IM6512C		UNITS
		MIN	MAX	
Access Time From STR	t_{AC}		600	ns
Output Enable Time	t_{EN}		375	ns
Output Disable Time	t_{DIS}		375	ns
STR Pulse Width (Positive)	t_{STR}	395		ns
STR Pulse Width (Negative)	$t_{\overline{STR}}$	600		ns
Cycle Time	t_C	995		ns
Write Pulse Width (Negative)	t_{WP}	395		ns
Address Setup Time	t_{AS}	40		ns
Address Hold Time	t_{AH}	130		ns
Data Setup Time	t_{DS}	395		ns
Data Hold Time	t_{DH}	0		ns
MSEL Pulse Separation	t_{PS}	150		ns
MSEL Setup Time	t_{MS}	50		ns
MSEL Hold Time	t_{MH}	50		ns

FIGURE 1. Read-Modify-Write or Read Cycle

Read-Modify-Write (MSEL high when STR goes low)

DX pins are high impedance until the first negative-going edge on MSEL ① which enables the outputs to read data from memory ②. When MSEL returns high ③ the DX pins return to high impedance for the remainder of the cycle.

The (optional) second negative-going MSEL pulse ④ causes a write to memory. Data at DX pins to be written into memory should be valid for a time (t_{DS}) prior to, and a time (t_{DH}) following the rising edge of MSEL ⑤. MSEL must remain high until STR returns high ending the cycle.

Read Only

Same as Read-Modify-Write except the second negative-going MSEL pulse is omitted.

FIGURE 2. Write Cycle

Write (MSEL low when STR goes low)

DX pins are always high impedance. Data at DX pins to be written into memory should be valid for a time (t_{DS}) prior to, and a time (t_{DH}) following the rising edge of MSEL ⑥.

FIGURE 3. A Typical Microprocessor System

Typical Microprocessor System (Figure 3)

In the example shown, the IM6312 RSEL (RAM Select) output is programmed to go low for addresses 0-255. IM6512 with ADR = "0" will respond to addresses 0-63 (and 128-191); IM6512 with ADR = "1" will respond to addresses 64-127 (and 192-255).

ADR

ADR should be either tied to logic "0" (GND) or logic "1" (V_{CC}). The data on this pin is compared internally with address data on DX5. If the two match, the chip will respond to MSEL and CS, otherwise the IM6512 DX lines remain high impedance and data is unchanged. As a result, two IM6512 memories can be used with the IM6100 and IM6312 without additional components.

ADR	DX5*	MSEL @ $\overline{STR}$[1]	FUNCTION
L	L	L	WRITE
L	L	H	READ-MODIFY-WRITE, READ ONLY
L	H	X	NO OP. (HI-Z)
H	L	X	NO OP. (HI-Z)
H	H	L	WRITE
H	H	H	READ-MODIFY-WRITE, READ ONLY

X = DON'T CARE

Note 1: Addresses are latched on chip by the falling edge of STR

FIGURE 4. IM6512 Truth Table

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INTERSIL

IM6508/IM6518
1024 Bit (1024 x 1) CMOS RAM

FEATURES

- **Low Standby Power: 5μW Typical Standby at 5V, 25°C**
- **Low Operating Power: 10mW/MHz Maximum**
- **High Speed Operation**
- **Data Retention to V_{CC} = 2.0V (non-C version)**
- **TTL Compatible Inputs and Outputs**
- **Three-State Outputs**
- **On-Chip Address Registers**
- **Completely Static and Synchronous**
- **Operating Voltage Range 4V to 11V (A version)**
- **Two Chip Selects (IM6518)**
- **Military and Industrial Temperature Ranges**

GENERAL DESCRIPTION

The IM6508 and IM6518 are high speed, low power silicon gate CMOS static RAMs organized 1024 words by 1 bit. In all static states these RAMs exhibit the microwatt power requirements typical of CMOS. The basic parts operate from 4.5 to 5.5 volts, with access times of 460 ns and standby supply currents of 100μa guaranteed over operating temperature range. Access times of 300 ns and standby supply currents of 10μa are offered in "-1" versions. Higher operating voltages and faster speeds are offered in "A" versions. Data retention is guaranteed to 2.0V on all non-C parts.

BLOCK DIAGRAM

*IM6508 FUNCTIONS AS IF $\overline{E}$, $\overline{S_1}$, $\overline{S_2}$, WERE TIED TOGETHER

PIN CONFIGURATION

TOP VIEW

Pin 1 is designated by a dot or a notch

ORDERING INFORMATION

SELECTION/TEMPERATURE RANGE

PACKAGE		COMMERCIAL	INDUSTRIAL				MILITARY			
		STD	STD 5V	STD 10V	HI SPEED 10V	HI SPEED LOW ICC 5V	STD 5V	STD 10V	HI SPEED 10V	HI SPEED LOW ICC 5V
PLASTIC	P	CP	IP	—	—	—	—	—	—	—
CERDIP	J	CJ	IJ	AIJ	A-1IJ	-1IJ	MJ	AMJ	A-1MS	-1MJ
CERAMIC	D	—	ID	AID	A-1ID	-1ID	MD	AMD	A-1MD	-1MD
FLAT	F	—	—	—	—	—	MF	AMF	A-1MF	-1MF

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +12.0V
Input or Output, Voltage Applied ..... GND -0.3V to V_{CC} to .3V
Storage Temperature Range ..... -65°C to +150°C
Operating Ranges
Temperature
Industrial ..... -40°C to +85°C
Military ..... -55°C to +125°C
Voltage
IM6508A/18A ..... 4V to 11V

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 4V to 11V, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}-2.0			V
Logical "0" Input Voltage	V_{IL}				.8	
Input Leakage	I_I	$0V \leq V_{IN} \leq V_{CC}$	-1.0		+1.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OUT} = 0	V_{CC}-0.01			V
Logical "0" Output Voltage	V_{OL}	I_{OUT} = 0			GND + 0.01	
Output Leakage	I_O	$0V \leq V_O \leq V_{CC}$	-1.0		+1.0	μA
Standby Supply Current	I_{CCSB}	$V_{IN} = V_{CC}$		5.0	500	
	I_{CCSB}	V_{CC} = 3.0V		.1	50	
Operating Supply Current	I_{CCOP}	f = 1MHz, $V_{IN} = V_{CC}$ or GND, I_O = 0			10	mA
Input Capacitance	C_I			5.0	7.0	pf
Output Capacitance	C_O			6.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ±5%, C_L = 50pf, T_A = 25°C

PARAMETER	SYMBOL	IM6508A-1/18A-1		IM6508A/18A		UNITS
		MIN	MAX	MIN	MAX	
Access Time From $\overline{E}$	TELQV		95		150	ns
Output Enable Time	TSLQX		55		90	
Output Disable Time	TSHQZ		55		90	
$\overline{E}$ Pulse Width (Pos)	TEHEL	65		95		
$\overline{E}$ Pulse Width (Neg)	TELEH	95		150		
$\overline{W}$ Pulse Width (Neg)	TWLWH	65		95		
Address Setup Time	TAVEL	5		10		
Address Hold Time	TELAX	30		45		
Data Setup Time	TDVEH	65		95		
Data Hold Time	TEHDX	0		0		

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +8.0V
Input or Output Voltage Applied ..... GND −0.3V to V_{CC} +0.3V
Storage Temperature Range ..... −65°C to +150°C
Operating Ranges
Temperature
Industrial ..... −40°C to +85°C
Military ..... −55°C to +125°C
Voltage
IM6508/18I, M, -1I, -1M 4.5V-5.5V

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}−2.0			V
Logical "0" Input Voltage	V_{IL}				.8	
Input Leakage	I_I	$0 \le V_{IN} \le V_{CC}$	−1.0		+1.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OH} = 0	V_{CC}−0.01			V
		I_{OH} = −0.2ma	2.4			
Logical "0" Output Voltage	V_{OL}	I_{OL} = 0			GND +0.01	
		I_{OL} = 2.0ma			.45	
Output Leakage	I_O		−1.0		+1.0	μA
Standby Supply Current IM6508-1/18-1	I_{CCSB}	V_{IN} = V_{CC}		.1	10	
	I_{CCSB}	V_{CC} = 3.0V		.01	5	
IM6508/18	I_{CCSB}	V_{IN} = V_{CC}		1.0	100	
	I_{CCSB}	V_{CC} = 3.0V		.1	50	
Operating Supply Current	I_{CCOP}	f = 1MHz, V_{IN} = V_{CC} or GND, I_O = 0			2	mA
Input Capacitance	C_I			5.0	7.0	pf
Output Capacitance	C_O			6.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, C_L = 50pf, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM6508-1/18-1		IM6508/18		UNITS
		MIN	MAX	MIN	MAX	
Access Time From $\overline{E}$	TELQV		300		460	ns
Output Enable Time	TSLQX		180		285	
Output Disable Time	TSHQZ		180		285	
$\overline{E}$ Pulse Width (Pos)	TEHEL	200		300		
$\overline{E}$ Pulse Width (Neg)	TELEH	300		460		
$\overline{W}$ Pulse Width (Neg)	TWLWH	200		300		
Address Setup Time	TAVEL	7		15		
Address Hold Time	TELAX	90		130		
Data Setup Time	TDVEH	200		300		
Data Hold Time	TEHDX	0		0		

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +7.0V
Input or Output Voltage Applied ..... GND −0.5V to V_{CC} +0.5V
Storage Temperature Range ..... −65°C to +150°C
Operating Ranges
Temperature
Commercial ..... 0°C to 75°C
Voltage
IM6508C/18C 4.75V-5.25V

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 5%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}−2.0			V
Logical "0" Input Voltage	V_{IL}				.8	
Input Leakage	I_I	$0V \le V_{IN} \le V_{CC}$	−5.0		+5.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OUT} = 0	V_{CC}−0.01			V
		I_{OH} = −.2mA	2.4			
Logical "0" Output Voltage	V_{OL}	I_{OUT} = 0			GND ±0.01	
		I_{OL} = 1.6mA			.45	
Output Leakage	I_O	$0V \le V_O \le V_{CC}$	−5.0		+5.0	
Standby Supply Current	I_{CCSB}	$V_{IN} = V_{CC}$		500	800	μA
Operating Supply Current	I_{CCOP}	f = 1MHz, $V_{IN} = V_{CC}$ or GND, I_O = 0			4	mA
Input Capacitance	C_I			5.0	7.0	pf
Output Capacitance	C_O			6.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ±5%, C_L = 50pf, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM6508C/18C MIN	IM6508C/18C MAX	UNITS
Access Time From $\overline{E}$	TELQV		600	ns
Output Enable Time	TSLQX		375	
Output Disable Time	TSHQZ		375	
$\overline{E}$ Pulse Width (Pos)	TEHEL	395		
$\overline{E}$ Pulse Width (Neg)	TELEH	600		
$\overline{W}$ Pulse Width (Neg)	TWLWH	395		
Address Setup Time	TAVEL	20		
Address Hold Time	TELAX	170		
Data Setup Time	TDVEH	395		
Data Hold Time	TEHDX	0		

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READ MODE OPERATION

In a typical READ operation the address lines are latched by the falling edge of strobe input $\overline{E}$. If the chip has been selected, i.e. $\overline{S_1}$ and $\overline{S_2}$ (6518 only) are low, data becomes valid an access time (TELQV) after the falling $\overline{E}$ edge. Data out for 6508 (16 pin) remains valid until $\overline{E}$ returns high. Data out for 6518 (18 pin) is latched when $\overline{E}$ returns high, and remains valid until a chip select ($\overline{S_1}$ or $\overline{S_2}$) is returned high.

Address information is edge triggered and must be valid a setup time (TAVEL) before and a hold time (TELAX) after the falling E edge. $\overline{S_1}$ and $\overline{S_2}$ on the 6518 are level sensitive and may occur after $\overline{E}$ transition without affecting access time.

READ CYCLE TIMING

FUNCTION TABLE • READ

TIME REF	INPUTS				OUTPUT	NOTES
	$\overline{E}$	A	$\overline{S}$	$\overline{W}$	Q	
-1	H	X	H	H	Z	Memory inactive, output high Z
0	↘	V	X	H	Z	Addresses latched, output sill high Z
1	L	X	L	H	X	Output enabled and active
2	L	X	L	H	V	Output valid
3	↗	X	L	H	V	Output latched and valid (6518). Output disabled (6508).
4	H	X	H	H	Z	Output disabled, high Z. Ready for next cycle.

WRITE MODE OPERATION

For a WRITE operation, address lines are latched by $\overline{E}$ as in a READ operation. Writing begins when strobe ($\overline{E}$), chip selects ($\overline{S_1}$, $\overline{S_2}$) and write ($\overline{W}$) are low and ends when one of these lines returns high. Data (D) must be valid a setup time (TDVEH) before and a hold time (TEHDX) after the final rising edge.

Minimum write pulse widths are specified as TWLWH for $\overline{W}$, $\overline{S_1}$ and $\overline{S_2}$. Minimum write pulse width is specified as TELEH for $\overline{E}$.

WRITE CYCLE TIMING

FUNCTION TABLE • WRITE

TIME REF	INPUT					OUTPUT	NOTES
	$\overline{E}$	A	$\overline{S}$*	$\overline{W}$	D	Q	
-1	H	X	H	X	X	Z	Memory inactive, output high Z
0	↘	V	H	X	X	Z	Addresses latched
1	L	X	L	↘	X	Z	Write operation begins
2	L	X	L	↗	V	Z	Write operation ends
3	H	X	H	H	X	Z	Output disabled, high Z. Ready for next cycle.

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PACKAGE DIMENSIONS

16 LEAD CERAMIC (DE)

18 LEAD CERAMIC (DN)

16 LEAD CERDIP (JE)

18 LEAD CERDIP (JN)

16 LEAD FLATPACK (FE)

18 PIN FLATPACK (FN)*

16 LEAD PLASTIC

18 LEAD PLASTIC (PN)

NOTE: Dimensions in inches (mm)

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INTERSIL

IM6551/IM6561
1024 (256 x 4) Bit CMOS RAM

FEATURES

- **Low Standby Power: 5μW Typical Standby at 5V, 25°C**
- **Low Operating Power: 10mW/MHz Maximum**
- **High Speed Operation**
- **Data Retention to VCC = 2.0V (non-C version)**
- **TTL Compatible Inputs and Outputs**
- **Three State Outputs**
- **On-Chip Address Registers**
- **Completely Static and Synchronous**
- **Operating Voltage Range 4V to 11V (A version)**
- **Military and Industrial Temperature Ranges**

GENERAL DESCRIPTION

The IM6551 and IM6561 are high speed, low power silicon gate CMOS 1024 bit static RAMs organized 256 words by 4 bits. In all static states these RAMs exhibit the microwatt power requirements typical of CMOS. The basic parts operate from 4.5 to 5.5 volts, with access times of 360 ns and standby supply currents of 100 μa guaranteed over operating temperature range. Higher operating voltages and correspondingly faster speeds are offered in "A" versions. Data retention is guaranteed to 2.0V on all non-C parts.

BLOCK DIAGRAM

PIN CONFIGURATION

Pin 1 is designated by a dot or a notch.

ORDERING INFORMATION

NO.	PACKAGE	INDUSTRIAL STD 5V	INDUSTRIAL STD 10V	MILITARY STD 5V	MILITARY STD 10V	COMMERCIAL STD 5V
IM6551	Cerdip JF	IJF	AIJF	MJF	AMJF	CJF
	Ceramic DF	IDF	AIDF	MDF	AMDF	CDF
	Plastic PF	IPF	—	—	—	CPF
IM6561	Cerdip JN	IJN	AIJN	MJN	AMJN	CJN
	Ceramic DN	IDN	AIDN	MDN	AMDN	CDN
	Plastic PN	IPN	—	—	—	CPN

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +12.0V
Input or Output Voltage Applied ..... GND −0.3V to VCC +0.3V
Storage Temperature Range ..... −65°C to +150°C
Operating Range
  Temperature
    Industrial ..... −40°C to +85°C
    Military ..... −55°C to +125°C
  Voltage
    IM6551A, IM6561A ..... 4V to 11V

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 4V to 11V, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}−2.0			V
Logical "0" Input Voltage	V_{IL}				0.8	
Input Leakage	I_{IL}	$0V \le V_{IN} \le V_{CC}$	−1.0		1.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OUT} = 0	V_{CC} −0.01			V
Logical "0" Output Voltage	V_{OL}	I_{OUT} = 0			GND +0.01	
Output Leakage	I_O	$0V \le V_o \le V_{CC}$	−1.0		1.0	μA
Standby Supply Current	I_{CCSB}	$V_{IN} = V_{CC}$		5.0	500	
	I_{CCSB}	V_{CC} = 3.0V = $\overline{E}_1$		0.1	50	
Operating Supply Current	I_{CCOP}	f = 1 MHz, $V_{IN} = V_{CC}$ or GND, I_O = 0			10	mA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ±5%, CL = 50pF, T_A = 25°C

PARAMETER	SYMBOL	IM6551A/61AI,M MIN	IM6551A/61AI,M MAX	UNITS
Access Time From $\overline{E}_1$	TE_1LQV		180	ns
Output Enable Time	TSLQV		90	
Output Disable Time	TSHQV		90	
$\overline{E}_1$ Pulse Width (Positive)	TE_1HE_1L	60		
$\overline{E}_1$ Pulse Width (Negative)	TE_1LE_1H	110		
$\overline{W}$ Pulse Width (Negative)	TWLWH	120		
Address Setup Time	$TAVE_1L$	25		
Address Hold Time	TE_1LAX	60		
Data Setup Time	$TDVE_1H$	60		
Data Hold Time	TE_1HDX	30		

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +8.0V
Input or Output Voltage Supplied ..... GND −0.3V to V_{CC} +0.3V
Storage Temperature Range ..... −65°C to +150°C
Operating Range
  Temperature
    Industrial ..... −40°C to +85°C
    Military ..... −55°C to +125°C
  Voltage
    6551/61 I,M ..... 4.5V to 5.5V

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ±10%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}−2.0			V
Logical "0" Input Voltage	V_{IL}				0.8	
Input Leakage	I_{IL}	$0V \le V_{IN} \le V_{CC}$	−1.0		1.0	μA
Logical "1" Output Voltage	V_{OH1}	I_{OH} = −0.2mA	2.4			V
Logical "0" Output Voltage	V_{OL1}	I_{OL} = 2.0mA			0.45	
Output Leakage	I_O	$0V \le V_O \le V_{CC}$	−1.0		1.0	μA
Standby Supply Current	I_{CCSB}	$V_{IN} = V_{CC}$		1	100	
	I_{CCSB}	V_{CC} = 3V = E_1		1	50	
Operating Supply Current	I_{CCOP}	f = 1 MHz, $V_{IN} = V_{CC}$ or GND, I_O = 0			2	mA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ±10%, C_L = 50pF, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM6551/61 I,M		UNITS
		MIN	MAX	
Access Time From $\overline{E}$	TE_1LQV		360	ns
Output Enable Time	TSLQV		180	
Output Disable Time	TSHQZ		180	
$\overline{E}_1$ Pulse Width (Positive)	TE_1HEL	120		
$\overline{E}_1$ Pulse Width (Negative)	TE_1LEH	220		
$\overline{W}$ Pulse Width (Negative)	TWLWH	240		
Address Setup Time	$TAVE_1L$	50		
Address Hold Time	TE_1LAX	120		
Data Setup Time	$TDEV_1H$	120		
Data Hold Time	TE_1HDX	60		

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... + 7.0V
Input or Output Voltage Applied ..... GND −0.3V to VCC +0.3V
Storage Temperature Range ..... −65°C to +150°C
Operating Range
  Temperature
    Commercial ..... 0°C to 70°C
  Voltage
    IM6551/61C ..... 4.75V to 5.25V

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 5%, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}−2.0			V
Logical "0" Input Voltage	V_{IL}				0.8	
Input Leakage	I_{IL}	$0V \le V_{IN} \le V_{CC}$	−5.0		5.0	μA
Logical "1" Output Voltage	V_{OH1}	I_{OH} = −0.2mA	2.4			V
Logical "0" Output Voltage	V_{OL}	I_{OL} = 1.6mA			0.45	
Output Leakage	I_O	$0V \le V_O \le V_{CC}$	−5.0		5.0	μA
Standby Supply Current	I_{CCSB}	$V_{IN} = V_{CC}$		500	800	
Operating Supply Current	I_{CCOP}	f = 1 MHz, $V_{IN} = V_{CC}$ or GND, I_O = 0			4.0	mA
Input Capacitance	C_{IN}			5.0	7.0	pF
Output Capacitance	C_O			6.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 5%, C_L = 50pF, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM6551C/61C MIN	IM6551C/61C MAX	UNITS
Access Time From $\overline{E}_1$	TE_1LQV		450	ns
Output Enable Time	TSLQV		200	
Output Disable Time	TSHQZ		200	
$\overline{E}_1$ Pulse Width (Positive)	TE_1HE_1L	150		
$\overline{E}_1$ Pulse Width (Negative)	TE_1LE_1H	250		
$\overline{W}$ Pulse Width (Negative)	TWLWH	300		
Address Setup Time	$TAVE_1L$	65		
Address Hold Time	TE_1LAX	200		
Data Setup Time	$TDVE_1H$	200		
Data Hold Time	TE_1HDX	65		

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READ MODE OPERATION

In a typical READ operation the address lines are latched by the falling edge of strobe input $\overline{E_1}$. If the chip has been selected, i.e. $\overline{S_1}$ and $\overline{S_2}$ (6551 only) are low, data becomes valid an access time (TE_1LQV) after the falling $\overline{E_1}$ edge. Data is latched into output registers by rising $\overline{E_1}$ and remains valid until the next cycle or until a chip select ($\overline{S_1}$ or $\overline{S_2}$) is returned high.

Address and $\overline{E_2}$ information is edge triggered and must be valid a setup time ($TAVE_1L$) before and a hold time (TE_1LAX) after the falling edge of $\overline{E_1}$. $\overline{S_1}$, $\overline{S_2}$ and $\overline{W}$ are level sensitive and may occur after $\overline{E_1}$ transitions without affecting access time.

READ CYCLE TIMING

FUNCTION TABLE • READ

TIME REF.	INPUTS $\overline{E_1}$	A	$\overline{E_2}$	$\overline{S}$	$\overline{W}$	OUTPUTS Q	NOTES
-1	H	X	X	H	X	Z	Memory Inactive, output high Z.
0	↘	V	L	X	H	Z	Addresses and $\overline{E_2}$ latched, output still high Z.
1	L	X	X	L	H	X	Output enabled and active.
2	L	X	X	L	H	V	Output valid
3	↗	X	X	L	H	V	Output latched and valid, memory inactive.
4	H	X	X	H	H	Z	Output disabled, high Z. Ready for next cycle.

WRITE MODE OPERATION

For a WRITE operation addresses and $\overline{E_2}$ are latched by $\overline{E_1}$ as in a READ operation. Data is written when strobe ($\overline{E_1}$), chip selects ($\overline{S_1}$, $\overline{S_2}$) and write ($\overline{W}$) are low. WRITE operation ends when one of these lines returns high. Minimum write pulse requirements are specified for $\overline{E_1}$ as TE_1LE_1H and for $\overline{S_1}$, $\overline{S_2}$, W as TWLWH.

Data must be valid a setup time ($TDVE_1H$) before and a hold time (TE_1HDX) after the final rising edge.

WRITE CYCLE TIMING

FUNCTION TABLE • WRITE

TIME REF.	INPUTS $\overline{E_1}$	A	$\overline{E_2}$	$\overline{S}$	$\overline{W}$	D	OUTPUTS Q	NOTES
-1	H	X	X	H	X	X	Z	Memory Inactive, Outputs high Z
0	↘	V	L	H	X	X	Z	Addresses and $\overline{E_2}$ latched
1	L	X	X	L	↘	X	Z	Write operation begins
2	L	X	X	L	↗	V	Z	Write operation ends
3	H	X	X	H	H	X	Z	Outputs disabled, high Z. Ready for next cycle.

PACKAGE DIMENSIONS

18 LEAD CERAMIC (DN)

22 LEAD CERAMIC (DF)

18 LEAD CERDIP (JN)

22 LEAD CERDIP (JF)

18 LEAD PLASTIC (PN)

22 LEAD PLASTIC (PF)

NOTE: All dimensions in parenthesis are metric.

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INTERSIL

IM6504
CMOS Static RAM
4096 Bit (4096 x 1)

FEATURES

- **Low Power Standby - Typically 1μW**
- **High Speed - 170nS Typical Access Time at 5V, 25°C**
- **Improved Chip Enable Function Simplifies Battery-Backup System Design**
- **TTL/CMOS Compatible Inputs and Outputs**
- **Three State Outputs**
- **Operating Voltage Range 4.5V to 5.5V (5V ±10%)**
- **Data Retention to VCC = 2V**
- **On-Chip Address Register**
- **Harris IM6504/Mostek MK4104 Compatible**

GENERAL DESCRIPTION

The IM6504 is a low power, high speed 4096-bit static RAM organized as 4096 words by 1 bit, fabricated with Intersil's selective-oxidation, ion-implanted, self-aligned silicon-gate CMOS process (SELOX-C). In all static states, this device exhibits the microwatt power dissipation typical of CMOS. Inputs and three-state outputs are TTL and CMOS compatible and allow for direct interface with common system bus structures. On-chip address registers simplify system timing requirements.

Battery-backup design is simplified by an improved chip enable which, when high, allows all other inputs to be floating without increased power dissipation.

The basic part operates over the 4.5V to 5.5V range with a typical 5V, 25°C access time of 170nS.

FUNCTIONAL DESCRIPTION

Read Cycle

The falling edge of chip enable ($\overline{E}$) latches addresses in the on-chip register and initiates a read cycle. Addresses to be latched must be present a setup time (TAVEL) prior to and a hold time (TELAX) following the falling edge of $\overline{E}$. After an access time, valid data will be present at the output. The read is terminated when $\overline{E}$ goes high, disabling the output buffers.

Early-Write Cycle

The falling edge of $\overline{E}$ latches addresses, data-in (D) and $\overline{W}$ in on-chip registers. For the early-write cycle, $\overline{W}$ will be latched low causing the output buffers to remain in the high-impedance state through the end of the cycle.

Read-Modify-Write Cycle

The read-modify-write cycle begins as a normal read. The falling edge of $\overline{E}$ latches addresses in the on-chip register and initiates the read cycle when $\overline{W}$ is high. After an access time, valid data will be present at the output. Data-in (D) and data-out (Q) are latched on the falling edge of $\overline{W}$. At this point, all input signals with the exception of $\overline{E}$ have been latched and may change without affecting the cycle. On the next rising edge of $\overline{E}$ the write portion is complete, inputs are unlatched, and the output returns to high-impedance.

LOGICAL BLOCK DIAGRAM

ORDERING INFORMATION

PART NO.	PACKAGE	TEMP. RANGE
IM6504IPN	18-PIN PLASTIC	-40°C to +85°C
IM6504IJN	18-PIN CERDIP	-40°C to +85°C
IM6504IDN	18-PIN CERAMIC	-40°C to +85°C
IM6504MJN	18-PIN CERDIP	-55°C to +125°C
IM6504MDN	18-PIN CERAMIC	-55°C to +125°C
IM6504MFN	18-PIN FLATPACK	-55°C to +125°C
IM6504CPN*	18-PIN PLASTIC	0°C to +70°C
IM6504CJN*	18-PIN CERDIP	0°C to +70°C

*Preliminary specifications for these devices have not yet been established.

PIN NAMES

A0-A11	ADDRESS INPUTS
D	DATA INPUT
Q	DATA OUTPUT
$\overline{E}$	ADDR. STROBE/CHIP ENABLE
$\overline{W}$	WRITE ENABLE

PIN ASSIGNMENTS

LOGIC SYMBOL

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage (VCC) ..... +8V
Input or Output Voltage Applied ... GND -0.3V to VCC +0.3V
Storage Temperature ..... -65° C to 150° C

NOTE: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. Functional operation of the device at these or any other conditions exceeding those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods of time may affect device reliability.

OPERATING CONDITIONS

Supply Voltage (VCC) ..... +4.5V to +5.5V
Operating Temperature
Industrial ..... -40° C to +85° C
Military ..... -55° C to +125° C

ELECTRICAL PARAMETERS VCC = 5V ± 10%, CL = 50pF, TA = Operating Temperature Range

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS	TEST CONDITIONS
ICCDR	Data Retention Supply Current		0.01		μA	VCC=3V, $\overline{E}$=VCC, D=$\overline{W}$=VCC or GND, IO=0
ICCSB	Standby Supply Current		0.1		μA	$\overline{E}$=VCC, D=$\overline{W}$=VCC or GND, IO=0
ICCOP	Operating Supply Current		2		mA	f = 1 MHz, VIN = VCC or GND, IO = 0
VCCDR	Data Retention Supply Voltage	2			V	
VIH	Input High Voltage	VCC - 2		VCC+0.3	V	
VIL	Input Low Voltage	-0.3		0.8	V	
II	Input Leakage	-1		+1	μA	GND ≤ VIN ≤ VCC
VOH	Output High Voltage	2.4			V	IOH = -0.4mA
VOL	Output Low Voltage			0.4	V	IOL = 2mA
IOZ	Output Leakage	-1		+1	μA	$\overline{E}$=VCC, GND ≤ VOUT ≤ VCC
CI	Input Capacitance[1]		5		pF	f = 1 MHz, VIN = VCC or GND
CO	Output Capacitance[1]		6		pF	f = 1 MHz, VIN = VCC or GND

TIMING PARAMETERS VCC = 5V ± 10%, CL = 50pF, TA = Operating Temperature Range

SYMBOL	DESCRIPTION	MIN	TYP	MAX	UNITS	TEST CONDITIONS
TELQV	Chip Enable Access Time		170		nS	TRISE = TFALL = 20nS
TAVQV	Address Access Time		170			
TEHQZ	Chip Enable Output Disable Time		50			
TELEH	Chip Enable Pulse Negative Width		170			
TEHEL	Chip Enable Pulse Positive Width		70			
TAVEL	Address Setup Time		-10			
TELAX	Address Hold Time		20			
TWLWH	Write Enable Pulse Width		40			
TWLEH	Write Enable Pulse Setup Time		70			
TWLEL	Early Write Pulse Setup Time		-10			
TWHEL	Write Enable Read Setup Time		-10			
TELWH	Early Write Pulse Hold Time		40			
TDVWL	Data Setup Time		0			
TDVEL	Early Write Data Setup Time		0			
TWLDX	Data Hold Time		40			
TELDX	Early Write Data Hold Time		40			
TQVWL	Data Valid to Write Time		0			
TELEL	Read or Write Cycle Time		240			

NOTE 1: This parameter periodically sampled, not 100% tested.

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FUNCTION TABLE

TIME REF.	INPUTS Ē	W̄	A	OUTPUT Q	NOTES
-1	H	X	X	Z	MEMORY INACTIVE
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES LATCHED
1	L	H	X	V	OUTPUT VALID
2	↗	H	X	V	READ COMPLETE
3	H	X	X	Z	MEMORY INACTIVE (SAME AS -1)
4	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

READ CYCLE

FUNCTION TABLE

TIME REF.	INPUTS Ē	W̄	A	D	OUTPUT Q	NOTES
-1	H	X	X	X	Z	MEMORY INACTIVE
0	↘	L	V	V	Z	CYCLE BEGINS, ADDRESSES LATCHED
1	L	X	X	X	Z	WRITE IN PROGRESS
2	↗	X	X	X	Z	WRITE COMPLETE
3	H	X	X	X	Z	MEMORY INACTIVE (SAME AS -1)
4	↘	L	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

EARLY WRITE CYCLE

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FUNCTION TABLE

TIME REF.	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	NOTES
-1	H	X	X	X	Z	MEMORY INACTIVE
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESSES LATCHED
1	L	H	X	X	V	OUTPUT VALID, READ/ MODIFY TIME
2	L	↘	X	V	V	WRITE BEGINS, DATA LATCHED
3	L	X	X	X	V	WRITE IN PROGRESS
4	↗	X	X	X	V	WRITE COMPLETE
5	H	X	X	X	Z	MEMORY INACTIVE (SAME AS -1)
6	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

READ-MODIFY-WRITE CYCLE

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SYMBOLS AND ABBREVIATIONS

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IOZ — Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:

T X X X X

Signal name from which interval is defined
Transition direction for first signal
Signal name to which interval is defined
Transition direction for second signal

Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)

EXAMPLE:

The example shows Write pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

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PACKAGE SPECIFICATIONS

18-Pin Ceramic Dip (DN)[1]

18-Pin CERDIP (JN)[1]

18 LEAD PLASTIC (PN)

NOTES:

1. Hermetic: Maximum Leakage Rate 5 x 10^{-7} atm. cc/sec

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INTERSIL

IM6514
CMOS Static RAM
4096 Bit (1024 x 4)

ADVANCE INFORMATION
Characteristics are subject to change without notice.

FEATURES

- Low Power Standby — Typically 1μW
- High Speed — 170nS Typical Access Time at 5V, 25° C
- Improved Chip Enable Function Simplifies Battery-Backup System Design
- TTL Compatible Inputs and Outputs
- Three State Outputs
- Operating Voltage Range 4.5V to 5.5V (5V ±10%)
- Data Retention to VCC = 2V
- On-Chip Address Register
- Harris IM6514/Mostek MK4114 Compatible

GENERAL DESCRIPTION

The IM6514 is a low power, high speed 4096-bit static RAM organized as 1024 words by 4 bits, fabricated with Intersil's selective-oxidation, ion-implanted, self-aligned silicon-gate CMOS process (SELOX-C). In all static states, this device exhibits the microwatt power dissipation typical of CMOS. Inputs and three-state outputs are TTL and CMOS compatible and allow for direct interface with common system bus structures. On-chip address registers simplify system timing requirements.

Battery-backup design is simplified by an improved chip enable which, when high, allows all other inputs to be floating without increased power dissipation.

The basic part operates over the 4.5V to 5.5V range with a typical 5V, 25° C access time of 170nS.

FUNCTIONAL DESCRIPTION

Read Cycle

The falling edge of chip enable ($\overline{E}$) latches addresses in the on-chip register and initiates a read cycle. Addresses to be latched must be present a setup time (TAVEL) prior to and a hold time (TELAX) following the falling edge of $\overline{E}$. During time T=1 the output will become valid. Write enable ($\overline{W}$) must remain high until after time T=2. The read is terminated when $\overline{E}$ goes high at time T=3 disabling the output buffers.

Write Cycle

The falling edge of $\overline{E}$ (T=0) latches addresses in on-chip registers. Write begins at T=1 and ends at T=2 with rising $\overline{E}$ or $\overline{W}$. Data in must remain valid until T=4.

Read-Modify-Write Cycle

The read-modify-write cycle begins as a normal read. The falling edge of $\overline{E}$ (T=0) latches addresses in the on-chip register and initiates the read cycle when $\overline{W}$ is high. During time T=1 the output will become active; at T=3 valid data must be present. Data-in (D) is latched on the rising edge of $\overline{W}$. On the rising edge of $\overline{E}$ (T=4) the write portion is complete, inputs are unlatched, and the output returns to high-impedance.

BLOCK DIAGRAM

ORDERING INFORMATION

PART NO.	PACKAGE	TEMP. RANGE
IM6514IPN	18-PIN PLASTIC	-40° C to +85° C
IM6514IJN	18-PIN CERDIP	-40° C to +85° C
IM6514IDN	18-PIN CERAMIC	-40° C to +85° C
IM6514MJN	18-PIN CERDIP	-55° C to +125° C
IM6514MDN	18-PIN CERAMIC	-55° C to +125° C
IM6514MFN	18-PIN FLATPACK	-55° C to +125° C
IM6514CPN	18-PIN PLASTIC	0° C to +70° C
IM6514CJN	18-PIN CERDIP	0° C to +70° C

PIN NAMES

A0-A9	ADDRESS INPUTS
D/Q0-3	DATA INPUTS, Q OUTPUTS
$\overline{E}$	ADDR. STROBE/CHIP ENABLE
$\overline{W}$	WRITE ENABLE

PIN ASSIGNMENTS

LOGIC SYMBOL

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ADVANCE INFORMATION
Characteristics are subject to change without notice.

FUNCTION TABLE

TIME REF.	INPUTS $\overline{E}$	$\overline{W}$	A	OUTPUT Q	NOTES
-1	H	X	X	Z	MEMORY INACTIVE
0	↘	H	V	Z	CYCLE BEGINS, ADDRESSES LATCHED
1	L	H	X	V	OUTPUT VALID
2	↗	H	X	V	READ COMPLETE
3	H	X	X	V	MEMORY INACTIVE (SAME AS -1)
4	↘	H	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

READ CYCLE

FUNCTION TABLE

TIME REF.	INPUTS $\overline{E}$	$\overline{W}$	A	I/O	NOTES
-1	H	X	X	Z	MEMORY INACTIVE
0	↘	X	V	Z	CYCLE BEGINS, ADDRESSES LATCHED
1	L	L	X	Z	WRITE IN PROGRESS
2	L	↗	X	V	WRITE COMPLETE
3	H	X	X	V	MEMORY INACTIVE (SAME AS -1)
4	↘	X	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS

WRITE CYCLE

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ADVANCE INFORMATION
Characteristics are subject to change without notice.

FUNCTION TABLE

TIME REF.	INPUTS $\overline{E}$	$\overline{W}$	A	D	OUTPUT Q	NOTES
-1	H	X	X	X	Z	MEMORY INACTIVE
0	↘	H	V	X	Z	CYCLE BEGINS, ADDRESSES LATCHED
1	L	H	X	X	V	OUTPUT VALID, READ/ MODIFY TIME
2	L	↘	X	X	Z	WRITE BEGINS, OUTPUT HIGH Z
3	L	L	X	V	Z	WRITE IN PROGRESS
4	↗	X	X	X	Z	WRITE COMPLETE
5	H	X	X	X	Z	MEMORY INACTIVE (SAME AS -1)
6	↘	H	V	X	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

READ-MODIFY-WRITE CYCLE

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PACKAGE SPECIFICATIONS

ADVANCE INFORMATION
Characteristics are subject to change without notice.

18 LEAD CERAMIC (DN)

18 LEAD CERDIP (JN)

18 LEAD PLASTIC (PN)

NOTES:

1. Hermetic: Maximum Leakage Rate 5 x 10^{-7} atm. cc/sec

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INTERSIL

IM7141
4096 Bit Static RAM

FEATURES

- 4096 X 1 Organization
- Maximum Access Time:
  - 7141-2, 7141L2 – 200ns
  - 7141-3, 7141L3 – 300ns
  - 7141, 7141L – 450ns
- TTL Compatible Inputs and Outputs
- Separate Data Input and Output
- Military Temperature Operation –55°C to +125°C Available
- 883A Class B Processing Available
- High Density 18 Pin Package
- Minimum Cycle Time Equal to Access Time
- Power Dissipation
  - 7141L – 275mW Maximum
  - 7141 – 385mW Maximum
  - Military Temp Units – 495mW Maximum
- Completely Static Operation

DESCRIPTION

The 7141 is a 4096-bit static Random Access Memory device organized 4096 X 1. The storage cell, decode and control circuitry are completely static, therefore no clocks or refresh operations are required. Memory access occurs within the specified access time after all address inputs are stable. A Chip Select input is provided for simple memory array expansion.

The 7141 is assembled in a standard 18 pin DIP for maximum system packing density.

BLOCK DIAGRAM

PIN CONFIGURATION

LOGIC SYMBOL

ORDERING INFORMATION

POWER	PACKAGE	ACCESS TIME		
		200ns	300ns	450ns
275mW	18 Pin CERDIP	IM7141L2CJN	IM7141L3CJN	IM7141LCJN
385mW	18 Pin CERDIP	IM7141-2CJN	IM7141-3CJN	IM7141CJN
495mW	18 Pin CERAMIC 18 Pin CERDIP w/8838	IM7141-2MJN IM7141-2MJN/B	IM7141-3MJN IM7141-3MJN/B	IM7141MJN IM7141MJN/B

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ABSOLUTE MAXIMUM RATINGS

Operating Temperature Military ..... −55°C to +125°C
Operating Temperature Commercial ..... 0°C to +70°C
Storage Temperature ..... −65°C to +150°C
Voltage on any Pin to Ground ..... −0.5V to +7V
Power Dissipation 1W

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

AC CHARACTERISTICS

Military Temp: $T_A = -55°C$ to $+125°C$, $V_{CC} = +5 \pm 10\%$
Commercial Temp: $T_A = 0°C$ to $+70°C$, $V_{CC} = +5 \pm 5\%$

READ CYCLE

$t_T = 10ns$, $V_{IL} = 0.8V$, $V_{IH} = 2.0V$, Output Load = 1 TTL Gate and 100pf

	SYMBOL	PARAMETER	7141L2, 7141-2		7141L3, 7141-3		7141L, 7141		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{RC}	Read Cycle	200		300		450		ns
2	t_A	Access Time		200		300		450	ns
3	t_{CO}	CS to Output Valid		70		100		100	ns
4	t_{CX}	CS to Output Active	0		0		0		ns
5	t_{OTD}	Output 3 State from Deselect	0	60	0	80	0	100	ns
6	t_{OHA}	Output Hold from Address Change	10		10		10		ns

WRITE CYCLE

	SYMBOL	PARAMETER	7141L2, 7141-2		7141L3, 7141-3		7141L, 7141		UNITS
			MIN	MAX	MIN	MAX	MIN	MAX	
1	t_{WC}	Write Time Cycle	200		300		450		ns
2	t_W	Write Time	120		150		200		ns
3	t_{WR}	Write Release Time	0		0		0		ns
4	t_{OTW}	Output 3 State from Write	0	60	0	80	0	100	ns
5	t_{DW}	Data to Write Time Overlap	120		150		200		ns
6	t_{DH}	Data Hold from Write Time	15		15		15		ns
7	t_{AW}	Address Setup Time	0		0		0		ns
8	t_{CW}	CS Select Pulse Width	120		150		200		ns

DC CHARACTERISTICS

Military Temp: $T_A = -55°C$ to $+125°C$, $V_{CC} = +5 \pm 10\%$
Commercial Temp: $T_A = 0°C$ to $+70°C$, $V_{CC} = +5 \pm 5\%$

	SYMBOL	PARAMETER	7141L		7141		UNITS	TEST CONDITIONS
			MIN	MAX	MIN	MAX		
1	I_{L1}	Input Load Current (All Inputs)		10		10	μA	$V_{IN} = 0$ to 5.25V
2	I_{L0}	I/O Leakage Current		10		10	μA	CS = 2.4V, $V_{I/O} = 0.4V$ to V_{CC}
3	I_{CC2}	Power Supply Current		40		65	mA	$V_{IN} = 5.25V$, $I_{I/O} = 0mA$ $T_A = 25°C$
4	I_{CC1}	Power Supply Current		50		70	mA	$V_{IN} = 5.25V$, $I_{I/O} = 0mA$ $T_A = 0°C$
5	I_{CC3}	Power Supply Current				90	mA	$V_{IN} = +5.5V$, $I_{I/O} = 0mA$ $T_A = -55°C$
6	V_{IL}	Input Low Voltage	−0.5	0.8	−0.5	0.8	V	
7	V_{IH}	Input High Voltage	2.0	V_{CC}	2.0	V_{CC}	V	
8	V_{OL}	Ouput Low Voltage		0.4		0.4	V	$I_{OL} = 3.2mA$
9	V_{OH}	Output High Voltage	2.4	V_{CC}	2.4	V_{CC}	V	$I_{OH} = -200\mu A$

DEVICE OPERATION

When $\overline{WE}$ is high, the data input buffers are inhibited to prevent erroneous data from getting into the array. As long as $\overline{WE}$ remains high, the data stored cannot be changed by the address Chip Select, or data input voltage levels and timing transitions. The block diagram also shows data storage cannot be changed by $\overline{WE}$, the addresses, nor the input data as long as $\overline{CS}$ is high. Either $\overline{CS}$ or $\overline{WE}$ by itself – or in conjunction with the other – can prevent extraneous writing due to signal transitions.

Data within the array can only be changed during a Write time – defined as the overlap of $\overline{CS}$ low and $\overline{WE}$ low. To prevent the loss of data, the addresses must be properly established during the entire Write time plus t_{WR}.

CAPACITANCE

	SYMBOL	PARAMETER	MAX	UNIT	TEST CONDITIONS
1	$C_{I/O}$	Input/Output Capacitance	5	pF	$V_{I/O} = 0V$
2	C_{IN}	Input Capacitance	5	pF	$V_{IN} = 0V$

TIMING DIAGRAMS

READ CYCLE

WRITE CYCLE

7141 BIT MAP DIAGRAM

PHYSICAL DIMENSIONS

CERDIP PACKAGE

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INTERSIL

IM6312 CMOS ROM 1024 Word x 12 Bit

FEATURES

- IM6100 compatible
- Low standby power: 5μW typical standby at 5V, 25°C
- Low operating power: 10mW/MHz maximum
- High speed operation
- TTL compatible inputs and outputs
- On-chip address registers
- Completely static and synchronous
- Operating voltage range 4V to 11V (A version)
- Military and industrial temperature ranges

GENERAL DESCRIPTION

The IM6312 is a high speed low power silicon gate CMOS static ROM organized 1024 words by 12 bits. In all static states it exhibits the microwatt power requirements typical of CMOS. The basic part offers a maximum 5V access time of 640 ns guaranteed over the industrial temperature range. A "-1" version guarantees 510 ns under the same conditions, and an "A" version offers 200 ns with a 10V supply. Signal polarities and functions are specified for interfacing with the IM6100 microprocessor. A decoder for RAM enable is provided on chip, eliminating an external 4 bit register and decoder. Upto 4 ROMs may be present in a system without external decoders to select ROM.

FUNCTIONAL DIAGRAM

PIN CONFIGURATIONS

Pin 1 is designated either by a dot or a notch.

ORDERING INFORMATION

MEMORY CIRCUIT MARKING AND PRODUCT CODE EXPLANATION

IM 6 3 12 A I DN

- Package
  - DN — Ceramic 18 pin DIP
  - JN — Cerdip 18 pin
  - FN — Flatpack 18 pin
- Temperature Range
  - I — Industrial (-40°C to +85°C)
  - M — Military (-55°C to +125°C)
  - C — Commercial (0°C to 70°C)
- Voltage Range
  - — 5V
  - A — 10V
- Specific Type
- General Type
  - Read Only Memory (ROM)
- CMOS Product Family
- INTERSIL Memory

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +12.0V
Applied Input or Output
Voltage ..... GND - 0.3V to V_{CC} + 0.3V
Storage Temperature Range ..... -65°C to +150°C
Operating Range
Temperature
Industrial (IM6312AI) ..... -40°C to +85°C
Military (IM6312AM) ..... -55°C to +125°C
Voltage
IM6312AI, AM 4-11V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

DC CHARACTERISTICS V_{CC} = 4-11V, T_A = Industrial or Military

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Logical "1" Input Voltage	V_{IH}		70% V_{CC}			V
Logical "0" Input Voltage	V_{IL}				20% V_{CC}	V
Input Leakage	I_{IL}	$0V \leq V_{IN} \leq V_{CC}$	−1.0		+1.0	μA
Logical "1" Output Voltage	V_{OH}	I_O = 0.0mA	V_{CC} −.01			V
Logical "0" Output Voltage	V_{OL}	I_O = 0.0mA			GND +.01	V
Output Leakage	I_O	$0V \leq V_O \leq V_{CC}$	−1.0		1.0	μA
Supply Current	I_{CCSB}			1.0	500	μA
Dynamic Supply Current	I_{CCOP}	f = 1MHz			2	mA
Input Capacitance	C_{IN}			5.0	7.0	pf
Output Capacitance	C_{OUT}			6.0	10.0	pf

AC CHARACTERISTICS V_{CC} = 10V ±5%, C_L = 50pf, T_A = 25°C

PARAMETER	SYMBOL	6312AI		6312AM		UNITS
		MIN	MAX	MIN	MAX	
Access time from $\overline{E}$	TELQV		200		220	ns
Output enable time	TGHQV		160		175	ns
Output disable time	TGLQZ		160		175	ns
Strobe ($\overline{E}$) positive pulse width	TEHEL	125		140		ns
Address setup time	TAVEL	30		35		ns
Address hold time	TELAX	60		60		ns
Propagation delay, address to $\overline{F}$	TAVFV		100		110	ns
Propagation delay, address to $\overline{F}$	TAZFX		100		110	ns

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +8.0V
Applied Input or Output
Voltage ..... GND -0.3V to V_{CC} +0.3V
Storage Temperature Range .... -65°C to +150°C
Operating Range
Temperature
Industrial (IM6312I/-1I) ..... -40°C to +85°C
Military (IM6312-1M) ..... -55°C to +125°C
Voltage
IM6312-1I, -1M, I, M 4.5-5.5V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

DC CHARACTERISTICS V_{CC} = 5.0V ±10%, T_A = Industrial or Military

PARAMETER	SYMBOL	CONDITIONS	IM6312-1I/-1M MIN.	IM6312-1I/-1M TYP.	IM6312-1I/-1M MAX.	IM6312I, M MIN.	IM6312I, M TYP.	IM6312I, M MAX.	UNITS
Logical "1" Input Voltage	V_{IH}		V_{CC}-2V			V_{CC}-1.5			V
Logical "0" Input Voltage	V_{IL}				0.8V			0.8	V
Input Leakage	I_{IL}	$0V \le V_{IN} \le V_{CC}$	-1.0		+1.0				μA
Input Leakage	I_{IL}	$0V \le V_{IN} \le V_{CC}$				-5.0		+5.0	μA
Logical "1" Output Voltage	V_{OH}	I_{OH}=-0.2mA	2.4			2.4			V
Logical "0" Output Voltage	V_{OL}	I_{OL}=2.0mA			0.45				V
Logical "0" Output Voltage	V_{OL}	I_{OL}=1.6mA						0.45	V
Output Leakage	I_O	$0V \le V_O \le V_{CC}$	-1.0		1.0				μA
Output Leakage	I_O	$0V \le V_O \le V_{CC}$				-5.0		+5.0	μA
Supply Current	I_{CCSB}	V_{IN}=V_{CC} or GND		1.0	100			800	μA
Dynamic Supply Current	I_{CCOP}	f=1MHz		1.5	1.8		1.5	1.8	mA
Input Capacitance	C_{IN}			5.0	7.0		5.0	7.0	pf
Output Capacitance	C_{OUT}			6.0	10.0		6.0	10.0	pf

AC CHARACTERISTICS V_{CC} = 5.0V ±10%, C_L = 50pf, T_A = Industrial or Military

PARAMETER	SYMBOL	IM6312-1I MIN.	IM6312-1I MAX.	IM6312-1M MIN.	IM6312-1M MAX.	IM6312I,M MIN.	IM6312I,M MAX.	UNITS
Access Time from $\overline{E}$	TELQV		510		560		640	ns
Output Enable Time	TGHQV		290		320		390	ns
Output Disable Time	TGLQZ		290		320		390	ns
Strobe Positive Pulse Width	TEHEL	260		285		300		ns
Address Setup Time	TAVEL	75		85		75		ns
Address Hold Time	TELAX	120		135		140		ns
Propagation Delay, Address to $\overline{F}$	TAVFV		220		240		250	ns
Propagation Delay, Address to $\overline{F}$	TAZFX		220		240		250	ns

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PIN ASSIGNMENTS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1	$\overline{F}$	H/L	RAM select, can be programmed to be active high or low. Used to enable specified RAM address field and disable ROM outputs.
2	$\overline{E}$	L	Strobe, latches address lines and enables outputs
3	G	H	Output enable
4-8, 10-16	DX_0-DX_{11}	—	Address inputs, data outputs
9	GND	—	Ground
17	$\overline{G}$	L	Output enable
18	V_{CC}	—	Chip +V supply

READ CYCLE TIMING

READ OPERATION

Address information is latched into on-chip registers by the falling edge of strobe line $\overline{E}$. Address information must be removed after address hold time (TELAX) to allow placing of Data Out on DX lines. Data Out is valid an access time (TELQV) after the falling edge of $\overline{E}$ if outputs are enabled, i.e. if $\overline{E}$ remains low, G is high and $\overline{G}$ is low.

RAM select $\overline{F}$ becomes valid a propagation delay time TAVFV after the address has been asserted, and invalid a propagation time TAZFX after the address has been removed.

Valid output data will be read only if decoded states of DX0 and DX1 are true. (See Chip Select Programming)

FUNCTION TABLE

TIME REF	INPUTS			OUTPUTS		NOTES
	E	G	A*	F	Q*	
-1	H	X	X	$\overline{V}$	Z	Memory inactive, DX lines indeterminate RAM is disabled
0		X	V	$\overline{V}$	Z	Addresses placed on DX lines, latched by E
1	L	X	X	V	Z	RAM select valid
2	L	H	Z	V	V	Data out valid on DX lines or RAM selected depending on address
3	H	X	X	$\overline{V}$	Z	Output disabled, DX lines switching to high Z

*Addresses (A) and data out (Q) multiplexed on DX lines.
**$\overline{V}$ = Invalid Level

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IM6312 CUSTOM ROM PROGRAMMING

An IM6312 ROM programming papertape consists of two segments (A and B), preceded by at least one foot of sprocket holes (no channels punched). Segment A is the header, and consists of frames 1-15 (see Fig. 1). Segment B contains at least one leader frame, location setting commands, data and checksum. The tape concludes with a minimum of one leader/trailer frame and a foot or more of sprocket holes.

NOTES

1. Each ROM pattern must be prepared on a separate papertape.
2. Data/address (DX) lines are numbered from DX0 (MSB) to DX11 (LSB).
3. A *punched* hole is considered a logical "1".
4. The following terms are synonymous
   (True, High, T, H, Logical "1")
   (False, Low, F, L, Logical "0")
5. No field change characters are allowed.

HEADER (Frames 1-15)

The header (Figure 1) begins with a rubout followed by six ASCII characters identifying the customer and pattern number. Frames 8 and 9 specify the states of DX0 and DX1 during $\overline{E}$, which enable the chip. The RAM Select ($\overline{F}$) output is programmed with frames 10-14. A rubout (all eight channels punched) in frame 15 concludes the header. Any rubout between frames 1 and 15 will invalidate the header and cause programming failure.

The example shown above has customer ID and pattern ISL004. Chip selects are programmed to recognize addresses 6000-7777_8 or 3072-4095_{10}. $\overline{F}$ is active low for addresses 0000-0377_8 or 0000-0255_{10}. Unused locations are automatically programmed to a logic zero.

Figure 1

CHIP SELECT PROGRAMMING (Frames 8, 9)

IM6312 outputs are enabled when $\overline{G}$ and $\overline{E}$ are low, G is high, and the states of DX0 and DX1 agree with the conditions specified in frames 8 (DX0) and 9 (DX1) of the header. To specify a particular ROM address field frames 8 and 9 must be programmed as follows:

Table 1

FRAME 8 (DX_0)	FRAME 9 (DX_1)	ADDRESS FIELD
F	F	0000_8-1777_8
F	T	2000_8-3777_8
T	F	4000_8-5777_8
T	T	6000_8-7777_8

For example, to program the ROM for address field 4000_8-5777_8 header frame 8 must be T and frame 9 must be F. Figure 2 diagrams the chip and RAM select logic.

*The "positions" of these "switches" are specified by the ROM programming tape (segment A).

Figure 2

RAM SELECT PROGRAMMING (Frames 10-14)

Most memory systems contain both RAM and ROM. The designer of such a system must insure that accesses to RAM memory space do not enable the ROMs and vice versa. The IM6312 ROM decodes address information on DX0 and DX1 to provide a unique 1024 word address space dedicated to itself. It also provides a RAM Select ($\overline{F}$) output which may be used to enable an address space dedicated to RAM. The states of DX0-DX3 which activate $\overline{F}$ are programmed by frames 10-13 respectively. Frame 14 determines whether $\overline{F}$ is considered active when high (frame 14 = H) or active when low (frame 14 = L).

Frames 10-13 may be T (true), V (don't care), or F (false). For example, if frames 10-13 are FTFV respectively, $\overline{F}$ will be active when address information on DX0 and DX2 is F (low) and DX1 is T (high). DX3 may be either T or F, since it is programmed V ("don't care") (see Table 3). Thus, in this example, RAMs using $\overline{F}$ as an enable will respond to addresses 2000_8 through 2777_8.

Table 2

Channel	Function
8 only	Leader/Trailer
8+ (6-1)	Header
7+ (6-1)	Location Setting (first frame)
6-1 only	Data, Checksum, Location Setting (second frame)

Table 3

Frames 10-13	RSEL Enable Condition
T	DXn must be high to enable
F	DXn must be low to enable
V	DXn may be either high or low to enable

LOCATION SETTING/DATA

It is not necessary to specify the contents of all 1024 words in the IM6312. Words that are not explicitly programmed will contain all zeros.

Data words are entered into sequential locations in ROM, beginning from the address specified by the most recently encountered location setting command. For this reason, such a command must precede any data words. A new location setting command may be given; subsequent data words will be entered beginning at the *new* address.

The location setting command consists of two sequential frames. The initial frame has channel 7 punched with the remaining channels (6-1) representing the most significant six bits of a 12-bit word. The second frame has no punches in channel 8 or 7, and represents the least significant 6 bits of the word (see Table 1).

Figure 3 shows an example of location setting to 0410_8. Subsequent data words will be stored in locations 0410_8, 0411_8, etc.

Figure 3

A data word consists of two frames with channels 8 and 7 unpunched. The two groups of six holes remaining are then concatenated to form a 12-bit binary number (punched = H, unpunched = L). The most significant six bits are punched first (channels 6-1 with 8 and 7 unpunched), followed by the least significant bits. The MSB of the 12-bit data word is channel 6 of the first frame; the LSB is channel 1 of the second frame. Figure 3 shows examples of two data words, 7440_8 and 6210_8.

CHECKSUM

A two frame checksum precedes the leader/trailer at the end of segment B. It is the modulo 4096 sum of all frames in segment B following the initial leader/trailer and preceding the final leader/trailer (except the two frames that represent the checksum itself). For purposes of checksum computation, each frame is to be considered an 8-bit binary word. The 12-bit result is punched out in two sequential frames, with channels 8 and 7 unpunched. The most significant six bits are punched first, followed by the least significant six bits as with the data word format. Any frame with channel 7 or 8 punched (e.g. leader or location setting command) is not included in the checksum computation. For additional BIN format information, refer to "PDP®-8 Family Commonly Used Utility Routines".

COMPATIBLE ASSEMBLER PROGRAMS

PAL III, FOPAL III, MACRO-8, PAL 8, and IFDOS PAL are assembler programs for the IM6100 microprocessor which prepare a papertape conforming to the specifications for the second tape segment. The header must in any case be produced manually.

The input to a PAL assembler is ASCII source code. More information and PAL assemblers are available from Intersil. The first frame-pair in a segment B produced by PAL III is a location setting command to address 0200_8. This is ignored if another origin setting follows immediately afterwards.

Some PAL assemblers produce a checksum with 13 bits (i.e., channel 7 of the first frame of the checksum may be punched). If channel 7 is punched, it is ignored.

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A MINIMAL MICROPROCESSOR SYSTEM (64 OR 128 WORDS OF RAM)

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PACKAGE DIMENSIONS

18 LEAD CERDIP (JN)

18 PIN FLATPACK (FN)*

INTERSIL

IM6316 CMOS ROM 16,384 Bit (2048x8)

FEATURES

- Low power: 500μW typical standby at 5V, 25°C
- High speed: 350ns typical access time at 5V, 25°C
- On-chip address registers
- TTL/CMOS compatible inputs and three-state outputs
- Completely static and synchronous
- Single 5V supply
- Intel 2316E and Mostek MK34000 compatible
- Two mask programmable chip selects (active level latched/unlatched)
- Outputs mask programmable (latched/unlatched)

GENERAL DESCRIPTION

The IM6316 is a 16,384-bit static silicon-gate CMOS read-only-memory (ROM) organized 2048 words by 8 bits. In all static states, this device exhibits the microwatt power dissipation typical of CMOS. Inputs and three-state outputs are TTL and CMOS compatible and allow for direct interface with common system bus structures. On-chip address registers and two mask programmable chip-selects simplify system interfacing requirements.

The IM6316 operates over a 4V to 6V range, with a typical 5V, 25°C access time of 350ns.

FUNCTIONAL DESCRIPTION

The falling edge of chip enable ($\overline{E}$) latches addresses in the on-chip register and initiates a read cycle. Address and chip selects to be latched must be present a setup time (TAVEL) prior to and a hold time (TELAX) following the falling edge of $\overline{E}$. After an access time, valid data will be available.

Optional latched outputs are active when S1 and S2 (or latched S1 and S2) are active. For unlatched outputs, $\overline{E}$ must also be low to enable.

Optional latches for S1 and S2 are level sensitive. When $\overline{E}$ is high, latched S1 and S2 thus perform as if they were not latched.

LOGICAL BLOCK DIAGRAM

PIN ASSIGNMENTS

LOGIC SYMBOL

ORDERING INFORMATION

PART NO.	PACKAGE	TEMP. RANGE
IM6316IJG	24 PIN CERDIP	−40°C to +85°C
IM6316IDG	24 PIN CERAMIC	−40°C to +85°C
IM6316MJG	24 PIN CERDIP	−55°C to +125°C
IM6316MDG	24 PIN CERAMIC	−55°C to +125°C

PIN NAMES

A0-A10	ADDRESS INPUTS
Q0-Q7	DATA OUTPUTS
$\overline{E}$	ADDR. STROBE/CHIP ENABLE
S1, S2	CHIP SELECTS

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READ CYCLE TIMING • Latched Chip Selects

FUNCTION TABLE • Latched Chip Selects

TIME REF	INPUTS			Q OUTPUTS		NOTES
	Ē	A	$S_1 \cdot S_2$	LATCHED	UNLATCHED	
-1	H	X	$\overline{V}$	Z	Z	MEMORY INACTIVE, OUTPUTS HIGH Z
0	↘	V	V	Z	Z	STROBE LATCHES VALID ADDRESS, CHIP SELECT INFORMATION
1	L	X	X	ACTIVE	ACTIVE	OUTPUTS ENABLED AND ACTIVE
2	L	X	X	V	V	OUTPUTS VALID
3	↗	X	X	V	V	STROBE RETURNS HIGH, LATCHES OUTPUTS
4	H	X	X	V	Z	OUTPUTS DISABLED ON UNLATCHED DEVICES
5	↘	V	V	V	Z	NEXT CYCLE BEGINS, SAME AS 0.

READ CYCLE TIMING • Unlatched Chip Selects

FUNCTION TABLE • Unlatched Chip Selects

TIME REF	INPUTS			Q OUTPUTS		NOTES
	Ē	A	$S_1 \cdot S_2$	LATCHED	UNLATCHED	
-1	H	X	$\overline{V}$	Z	Z	MEMORY INACTIVE, OUTPUTS HIGH Z
0	↘	V	$\overline{V}$	Z	Z	STROBE LATCHES ADDRESS INFORMATION
1	L	X	V	ACTIVE	ACTIVE	OUTPUTS ENABLED AND ACTIVE
2	L	X	V	V	V	OUTPUTS VALID
3	↗	X	V	V	V	STROBE RETURNS HIGH, LATCHES OUTPUTS
4	H	X	V	V	Z	OUTPUTS DISABLED ON UNLATCHED DEVICES
5	H	X	$\overline{V}$	Z	Z	OUTPUTS DISABLED ON LATCHED DEVICES
6	↘	V	$\overline{V}$	Z	Z	NEXT CYCLE BEGINS, SAME AS 0.

NOTES

1. X = Don't Care **2.** V = Valid **3.** Z = High Impedance 4. $\overline{V}$ = Invalid.

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APPLICATIONS

2k x 8 External CMOS ROM Memory for 8048 Microprocessor

2k x 8 ROM Memory for Z80 Microprocessor

2k x 8 ROM, 512 x 8 RAM System for 8085 Microprocessor

INTERSIL

IM6316 16K ROM ORDER FORM

CUSTOMER DATA

Date: _____

Company: _____

P.O. # _____

Engineer: _____

Engineer Telephone Number: _____

INTERSIL PART NUMBER

IM6316 [ ] [ ] [G]

I/M J/D

INTERSIL USE ONLY

6316S [ ][ ][ ]

DATA FORMAT

- ☐ Intellec™ HEX
- ☐ "PN"

MEDIA (all data must be in card form regardless of media)

- ☐ Punched Cards
- ☐ Magnetic Tape (9-track, 800 bpi, odd parity)
- ☐ Paper Tape

LOGIC FORMAT

- ☐ Positive (default)
- ☐ Negative

VERIFICATION

- ☐ Hold for verification (default)
- ☐ Not required

UNSPECIFIED LOCATIONS

- ☐ Programmed to FFH (default)
- ☐ Programmed to 00H

CUSTOMER OPTIONS (check only one box in each section)

- ☐ Latched Outputs
- ☐ Unlatched Outputs

- ☐ Latched Chip Selects
- ☐ Unlatched Chip Selects

- ☐ S1 Active High
- ☐ S1 Active Low
- ☐ S1 Always Active

- ☐ S2 Active High
- ☐ Active Low
- ☐ S2 Always Active

Intellec™ is a trademark of Intel Corporation

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SYMBOLS AND ABBREVIATIONS

This data sheet utilizes a new set of specification nomenclature. This new format is an IEEE and JEDEC supported standard for semiconductor memories. It is intended to clarify the symbols, abbreviations and definitions, and to make all memory data sheets consistent. We believe, once acclimated, you will find this standardized format easy to read and use.

ELECTRICAL PARAMETER ABBREVIATIONS

All abbreviations use upper case letters with no subscripts. The initial symbol is one of these four characters:

V (Voltage)
I (Current)
P (Power)
C (Capacitance)

The second letter specifies input (I) or output (O), and the third letter indicates high (H), low (L) or off (Z) state of the pin during measurements. Examples:

VIL — Input Low Voltage
IOZ — Output Leakage Current

TIMING PARAMETER ABBREVIATIONS

All timing abbreviations use upper case characters with no subscripts. The initial character is always T and is followed by four descriptors. These characters specify two signal points arranged in a "from-to" sequence that define a timing interval. The two descriptors for each signal point specify the signal name and the signal transitions. Thus the format is:

T X X X X

Signal name from which interval is defined
Transition direction for first signal
Signal name to which interval is defined
Transition direction for second signal

Signal Definitions:

A = Address
D = Data In
Q = Data Out
W = Write Enable
E = Chip Enable
S = Chip Select
G = Output Enable

Transition Definitions:

H = Transition to High
L = Transition to Low
V = Transition to Valid
X = Transition to Invalid or Don't Care
Z = Transition to Off (High Impedance)
V = Transition to level opposite that of valid state

EXAMPLE:

The example shows write pulse setup time defined as TWLEH-Time from Write enable Low to chip Enable High.

TIMING LIMITS

The table of timing values shows either a minimum or a maximum limit for each parameter. Input requirements are specified from the external system point of view. Thus, address set-up time is shown as a minimum since the system must supply at least that much time (even though most devices do not require it). On the other hand, responses from the memory are specified from the device point of view. Thus, the access time is shown as a maximum since the device never provides data later than that time.

WAVEFORMS

WAVEFORM SYMBOL	INPUT	OUTPUT
	MUST BE VALID	WILL BE VALID
	CHANGE FROM H TO L	WILL CHANGE FROM H TO L
	CHANGE FROM L TO H	WILL CHANGE FROM L TO H
	DON'T CARE: ANY CHANGE PERMITTED	CHANGING: STATE UNKNOWN
	—	HIGH IMPEDANCE

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PACKAGE SPECIFICATIONS

Ceramic Package (DG)*

CERDIP Package (JG)*

*Hermetic: Maximum leakage rate 5 x 10-7 atm. cc/sec.

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INTERSIL

ADVANCE INFORMATION
Characteristics are subject to change without notice.

IM6364 CMOS ROM 65,536 Bit (8192 x 8)

FEATURES

- **Low power: 500μW typical standby at 5V, 25°C**
- **High speed: 300ns typical access time at 5V, 25°C**
- **On-chip address registers**
- **TTL/CMOS compatible inputs and three-state outputs**
- **Completely static and synchronous**
- **Single 4V to 6V supply**
- **Outputs programmable latched/unlatched**

GENERAL DESCRIPTION

The IM6364 is a 65,536-bit static silicon-gate CMOS read-only-memory (ROM) organized 8192 words by 8 bits. In all static states, this device exhibits the microwatt power dissipation typical of CMOS. Inputs and three-state outputs are TTL and CMOS compatible and allow for direct interface with common system bus structures.

The IM6364 operates over a 4V to 6V range, with a typical 5V, 25°C access time of 300ns.

FUNCTIONAL DESCRIPTION

In both the latched and unlatched output configuration, the falling edge of chip enable ($\overline{E}$) latches the address inputs into the on-chip address register and initiates a read cycle. The address must be present a setup time (TAVEL) prior to and a hold time (TELAX) following the falling edge of $\overline{E}$.

In both output configurations, the outputs switch to active "1" level about 120ns after the falling edge of $\overline{E}$. The outputs remain at this level until making a transition to valid data, an access time following the falling edge of $\overline{E}$.

In the latched output configuration, the outputs remain latched for at least an address hold time (TELAX) following the falling edge of $\overline{E}$. This feature allows outputs to be fed back as address bits.

LOGICAL BLOCK DIAGRAM

PIN ASSIGNMENTS

LOGIC SYMBOL

ORDERING INFORMATION

PART NO.	PACKAGE	TEMP. RANGE
IM6364IJG	24 PIN CERDIP	-40°C to +85°C
IM6364IDG	24 PIN CERAMIC	-40°C to +85°C
IM6364MJG	24 PIN CERDIP	-55°C to +125°C
IM6364MDG	24 PIN CERAMIC	-55°C to +125°C

PIN NAMES

A0-A12	ADDRESS INPUTS
Q0-Q7	DATA OUTPUTS
$\overline{E}$	ADDRESS STROBE/ CHIP ENABLE

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ADVANCE INFORMATION
Characteristics are subject to change without notice.

TIMING DIAGRAM

FUNCTION TABLE

TIME REFERENCE	INPUTS		Q OUTPUTS		FUNCTION
	$\overline{E}$	A	LATCHED	UNLATCHED	
-1	H	V	PREVIOUS DATA	Z	ADDRESS SET UP
0	↘	V	PREVIOUS DATA	Z	CYCLE BEGINS, ADDRESSES ARE LATCHED
1	L	X	H	Z	LATCHED OUTPUTS BECOME ACTIVE HIGH
2	L	X	H	H	UNLATCHED OUTPUTS BECOME ACTIVE HIGH
3	L	X	V	V	VALID DATA AT OUTPUTS AFTER ACCESS TIME
4	H	X	V	Z	UNLATCHED OUTPUTS BECOME HIGH IMPEDANCE
5	H	V	V	Z	ADDRESS SET UP FOR NEXT CYCLE (SAME AS -1)
6	↘	V	V	Z	CYCLE ENDS, NEXT CYCLE BEGINS (SAME AS 0)

IM6364

INTERSIL

ADVANCE INFORMATION

Characteristics are subject to change without notice.

PACKAGE DIMENSIONS

24 LEAD CERAMIC (DG)

24 LEAD CERDIP (JG)

NOTES:
1. ALL DIMENSIONS IN INCHES AND (MILLIMETERS).
2. BOARD DRILLING DIMENSIONS WILL EQUAL STANDARD PRACTICES FOR .020 DIAMETER LEAD.

CUSTOMER DATA

Date: _____

Company: _____

P.O. #: _____

Engineer: _____

Engineer Telephone Number: _____

INTERSIL PART NUMBER

IM6364 [ ] [ ] [G]
I/M J/D

INTERSIL USE ONLY

63S [ ][ ][ ][ ]

DATA FORMAT

- ☐ Intellec™ HEX
- ☐ "PN"

VERIFICATION

- ☐ Hold for verification (default)
- ☐ Not required

MEDIA (all data must be in card image form regardless of media)

- ☐ Punched Cards
- ☐ Magnetic Tape (9-track, 800 bpi, odd parity)
- ☐ Paper Tape

UNSPECIFIED LOCATIONS

- ☐ Programmed to FFH (default)
- ☐ Programmed to 00H

LOGIC FORMAT

- ☐ Positive (default)
- ☐ Negative

CUSTOMER OPTIONS (check only one box)

- ☐ Latched Outputs
- ☐ Unlatched Outputs

Intellec™ is a trademark of Intel Corporation.

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INTERSIL

IM6653/IM6654 4096 Bit CMOS UV Erasable PROM

FEATURES

- **Organization — IM6653: 1024 x 4**
  IM6654: 512 x 8
- **Low Power — 5μW Typical Standby**
- **High Speed**
  — 300ns 10V Access Time for IM6653/54 AI
  — 450ns 5V Access Time for IM6653/54 -1I
- **Single +5V supply operation**
- **UV erasable**
- **Synchronous operation for low power dissipation**
- **Three-state outputs and chip select for easy system expansion**
- **Full −55°C to +125°C MIL range device — IM6653/54 M**

GENERAL DESCRIPTION

The Intersil IM6653 and IM6654 are fully decoded, 4096-bit, CMOS electrically programmable ROMs (EPROMs) fabricated using Intersil's advanced CMOS processing technology. The EPROMs are specifically designed for program development applications where rapid turn-around for program changes is required.

The 24 pin packages have a transparent lid to allow the user to erase the EPROM by exposing it to ultraviolet light. The EPROM may then be reprogrammed.

BLOCK DIAGRAM

PIN CONFIGURATION

ORDERING INFORMATION

24 PIN PACKAGE		SELECTION/TEMPERATURE RANGE			
		INDUSTRIAL			MILITARY
		STD 5V	HI SPEED 5V	STD 10V	STD 5V
CERDIP (FRIT SEAL)	JG	IJG	-1I JG	AIJG	MJG
CERAMIC (SIDE BRAZE)	DG	IDG	-1I DG	AIDG	MDG

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ABSOLUTE MAXIMUM RATINGS

Supply Voltages
- V_{DD} ..... +11.0V
- $V_{CC} = V_{DD}$ ..... +11.0V

Input or Output Voltage Supplied ..... GND −0.5V to V_{DD} +0.5V
Storage Temperature Range ..... −65°C to +150°C
Operating Range
- Temperature
  - Industrial ..... −40°C to +85°C
  - Military ..... −55°C to +125°C
- Voltage
  - 6653/54 I, -1I 4.5-5.5
  - 6653/54 M 4.5-5.5
  - 6653/54 AI 9.5-10.5

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

DC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = V_{DD}$ = Operating Voltage Range, T_A = Operating Temperature Range

PARAMETER	SYMBOL	CONDITIONS	IM6653/54I, -1I, M		IM6653/54AI		UNITS
			MIN	MAX	MIN	MAX	
Logical "1" Input Voltage	V_{IH}	$\overline{E_1}$, $\overline{S}$	V_{DD} - 2.0		V_{DD} - 2.0		V
	V_{IH}	Address Pins	2.7		V_{DD} - 2.0		
Logical "0" Input Voltage	V_{IL}			0.8		0.8	
Input Leakage	I_I	$0V \leq V_{IN} \leq V_{DD}$	-1.0	1.0	-1.0	1.0	μA
Logical "1" Output Voltage	V_{OH2}	$I_{OUT} = 0$	V_{CC} - 0.01		V_{CC} - 0.01		V
Logical "1" Output Voltage	V_{OH1}	I_{OH} = -0.2 mA	2.4				
Logical "0" Output Voltage	V_{OL2}	$I_{OUT} = 0$		GND +0.01		GND +0.01	
Logical "0" Output Voltage	V_{OL1}	I_{OL} = 2.0 mA		0.45			
Output Leakage	I_{OZ}	$0V \leq V_O \leq V_{CC}$	-1.0	1.0	-1.0	1.0	μA
Standby Supply Current	I_{DDSB}	$V_{IN} = V_{DD}$		100		100	
	I_{CC}	$V_{IN} = V_{DD}$		40		40	
Operating Supply Current	I_{DDOP}	f=1 MHz		6		12	mA
Input Capacitance	C_I	Note 1		7.0		7.0	pF
Output Capacitance	C_O	Note 1		10.0		10.0	

Note: These parameters guaranteed but not 100% tested.

AC CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = V_{DD}$ = Operating Voltage Range, T_A = Operating Temperature Range

PARAMETER	SYMBOL	IM6653/54-1I		IM6653/54 I		IM6653/54 M		IM6653/54 AI		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
Access Time From $\overline{E_1}$	TE1LQV		450		550		600		300	ns
Output Enable Time	TSLQV		110		140		150		60	
Output Disable Time	TE1HQZ		110		140		150		60	
$\overline{E_1}$ Pulse Width (Positive)	TE1HE1L	130		150		150		125		
$\overline{E_1}$ Pulse Width (Negative)	TE1LE1H	450		550		600		300		
Address Setup Time	TAVE1L	0		0		0		0		
Address Hold Time	TE1LAX		80		100		100		60	
Chip Enable Setup Time (6654)	TE2VE2L	0		0		0		0		
Chip Enable Hold Time (6654)	TE2LE2X		80		100		100		60	

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PIN ASSIGNMENTS

PIN	SYMBOL	ACTIVE LEVEL	DESCRIPTION
1-8,23	A_0-A_7,A_8	—	Address Lines
9-11,13-17	Q_0-Q_7	—	Data lines, 6654
	Q_0-Q_3	—	Data lines, 6653
12	V_{SS}	—	GND
18	Program	—	Programming pulse input
19	V_{DD}	—	Chip +V supply, normally tied to V_{CC}
20	$\overline{E_1}$	L	Strobe line, latches both address lines and, for 6654, Chip enable E_2
21	$\overline{S}$	L	Chip select line, must be low for valid data outputs
22	A_9	—	Additional address line for 6653
	$\overline{E_2}$	L	Chip enable line, latched by strobe E_1 on 6654
24	V_{CC}	—	Output buffer +V supply

READ CYCLE TIMING

*A9 IM6653 only, E2 IM6654 only

READ MODE OPERATION

In a typical READ operation the address lines are latched by a downward edge on the strobe line, $\overline{E_1}$. The chip must then be selected by driving pin 21 ($\overline{S}$) low. If the chip has been selected the data outputs become valid an access time (TELQV) after the downward strobe edge. The data outputs remain valid until the strobe line is returned to a high level. Both $\overline{S}$ and $\overline{E_2}$ may be tied low during the READ cycle. Note that $\overline{E_2}$ is latched by the downward strobe edge, but $\overline{S}$ is not. The PROGRAM pin must be tied high to V_{DD}.

FUNCTION TABLE

TIME REF.	INPUTS $\overline{E1}$	$\overline{E2}$*	$\overline{S}$	A	OUTPUTS Q	NOTES
−1	H	X	X	X	Z	DEVICE INACTIVE
0	↘	L	X	V	Z	CYCLE BEGINS; ADDRESSES, $\overline{E2}$ LATCHED*
1	L	X	X	X	Z	INTERNAL OPERATIONS ONLY
2	L	X	L	X	A	OUTPUTS ACTIVE UNDER CONTROL OF (E1,$\overline{S}$)
3	L	X	L	X	V	OUTPUTS VALID AFTER ACCESS TIME
4	↗	X	L	X	V	READ COMPLETE
5	H	X	X	X	Z	CYCLE ENDS (SAME AS −1)
0	↘	H	X	V	Z	CYCLE BEGINS: ADDRESSES, $\overline{E2}$ LATCHED
1	L	X	X	X	Z	OUTPUTS REMAIN HIGH-Z SINCE $\overline{E2}$ LATCHED HIGH

*$\overline{E2}$ not present on IM6653 which functions as if $\overline{E2}$ were tied LOW.

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READ AND PROGRAM CYCLES

DC CHARACTERISTICS FOR PROGRAMMING OPERATION

TEST CONDITIONS: $V_{CC} = V_{DD} = 5V \pm 5\%$, $T_A = 25°C$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Program Pin Load Current	I_{PROG}			80	100	mA
Programming Pulse Amplitude	V_{PROG}		38	40	42	V
V_{CC} Current	I_{CC}			0.1	5	mA
V_{DD} Current	I_{DD}			40	100	
Address Input High Voltage	V_{IHA}		V_{DD} -2.0			V
Address Input Low Voltage	V_{ILA}				0.8	
Data Input High Voltage	V_{IH}		V_{DD} -2.0			
Data Input Low Voltage	V_{IL}				0.8	

AC CHARACTERISTICS FOR PROGRAMMING OPERATION

TEST CONDITIONS: $V_{CC} = V_{DD} = 5V \pm 5\%$, $T_A = 25°C$

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Program Pulse Width	TPLPH	$t_{rise} = t_{fall} = 5\mu s$	18	20	22	ms
Program Pulse Duty Cycle					75%	
Data Setup Time	TDVPL		9	10		μs
Data Hold Time	TPHDX		9	10		
Strobe Pulse Width	TE1HE1L		150			ns
Address Setup Time	TAVE1L		0			
Address Hold Time	TE1LAX				100	
Access Time	TE1LQV				1000	

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PROGRAM MODE OPERATION

Initially, all 4096 bits of the EPROM are in the logic one (output high) state. Selective programming of proper bit locations to "0"s is performed electrically.

In the PROGRAM mode, V_{CC} and V_{DD} are tied together to the normal operating supply. High logic levels at all of the appropriate chip inputs and outputs must be set at V_{DD}-2V minimum. Low logic levels must be set at V_{SS}+.8V maximum.

Addressing of the desired location in PROGRAM mode is done as in the READ mode. Address and data lines are set at the desired logic levels, and PROGRAM and chip select ($\overline{S}$) pins are set high. The address is latched by the downward edge on the strobe line ($\overline{E_1}$). During valid DATA IN time, the PROGRAM pin is pulsed from V_{DD} to -40V. This pulse initiates the programming of the device to the levels set on the data outputs. Duty cycle limitations are specified from chip heat dissipation considerations. Pulse rise and fall times must not be faster than 5μs.

Intelligent programmer equipment with successive READ/PROGRAM/VERIFY sequences is recommended.

PROGRAMMING SYSTEM CHARACTERISTICS

1. During programming the power supply should be capable of limiting peak instantaneous current to 100mA.
2. The programming pin is driven from V_{DD} to −40V volts (±2V) by pulses of 20 milliseconds duration. These pulses should be applied following the algorithm shown in the flow chart. Pulse rise and fall times of 10 microseconds are recommended. Note that any individual location may be programmed at any time.
3. Addresses and data should be presented to the device within the recommended setup/hold time and high/low logic level margins.
4. The programming is to be done at room temperature.

ERASING PROCEDURE

The IM6653/54 may be erased by exposure to high intensity short-wave ultraviolet light at a wavelength of 2537 Å. The recommended integrated dose (i.e., UV intensity x exposure time) is 10W sec/cm². The lamps should be used without short-wave filters, and the IM6653/54 to be erased should be placed about one inch away from the lamp tubes. For best results it is recommended that the device remain inactive for 5 minutes after erasure, before programming.

PROGRAMMING FLOW CHART

INTERSIL

PHYSICAL DIMENSIONS

CERAMIC PACKAGE (DG)

CERDIP PACKAGE (JG)

NOTE: All dimensions in parenthesis are metric.

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INTERSIL

IM5600/IM5610 256 Bit Bipolar Read Only Memory

FEATURES

- Uses Patented AIM Programming Element for
  - Superior Reliability
  - High Programming Yield
  - Fast Programming Speed < 1 sec
  - TTL Processing Compatibility
- Low Power Consumption 1.5 mW/bit
- Operating Speed
  - Address to Output — 50nS
  - Chip Enable to Output — 40nS
- Large Output Drive — 16mA @ 0.45V
- TTL Compatible Inputs & Outputs
- Two Output Designs
  - 5600 Open Collector
  - 5610 Active Pull-up
- Chip Enable Facilitates Memory Expansion and Use in Bus Organized Systems

APPLICATIONS

- Code Conversion
- Logic Implementation
- Microprogramming
- Look-up Tables
- Control of Sequential Circuits
- Character Generation

GENERAL DESCRIPTION

The Intersil IM5600 and IM5610 are high speed, electrically programmable, fully decoded, bipolar 256 bit read only memories organized as 32 words by 8 bits. On-chip address decoding, chip enable input and uncomitted collector or three-state outputs provide for simplified memory expansion and use in bus organized systems.

Unprogrammed AIM elements are sensed as ZERO's or low logic levels at the outputs. Programming with a commercially available programmer irreversibly converts selected elements in the array so that they are sensed as ONE's or high logic levels.

The following companies make programmers approved by Intersil:

1. Data I/O Corp., P.O. Box 1603, Bellevue, Wash. 98009
2. PRO-LOG Corp., 2411 Garden Rd., Monterey, CA 93940

Detailed programming specifications for all Intersil PROMs are presented in the Intersil BIPOLAR PROM PROGRAMMING SPECIFICATION Data Sheet.

CONNECTION DIAGRAM

TOP VIEW

BLOCK DIAGRAM

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE	ORDER NUMBER
IM5600	16 Pin Ceramic DIP	0°C to +75°C Commercial -55°C to +125°C Military	IM5600CDE IM5600MDE
	16 Pin Flatpack	0°C to +75°C Commercial -55°C to +125°C Military	IM5600CFE IM5600MFE
	16 Pin Plastic DIP	0°C to +75°C	IM5600CPE
	16 Pin Cerdip DIP	0°C to +75°C Commercial -55°C to +125°C Military	IM5600CJE IM5600MJE
IM5610	16 Pin Ceramic DIP	0°C to +75°C Commercial -55°C to +125°C Military	IM5610CDE IM5610MDE
	16 Pin Flatpack	0°C to +75°C Commercial -55°C to +125°C Military	IM5610CFE IM5610MFE
	16 Pin Plastic DIP	0°C to +75°C	IM5610CPE
	16 Pin Cerdip DIP	0°C to +75°C Commercial -55°C to +125°C Military	IM5610CJE IM5610MJE

TRUTH TABLE

ADDRESS INPUTS A_0–A_4	$\overline{CE}$	ANY OUTPUT O_1–O_8
Any one of 32 possible addresses.	L	H—if the bit uniquely associated with this output and address has been electrically programmed. L—if it has not been programmed.
Any one of 32 possible addresses.	H	All outputs are forced to a high impedance state regardless of the address.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +7.0V
Input Voltage Applied ..... −1.5V to +5.5V
Output Voltage Applied ..... −0.5V to +V_{CC}
Output Voltage Applied (Programming Only) 28V
Current Into Output (Programming Only) ..... 210 mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature Range*
(IM5600C and IM5610C) ..... 0°C to +75°C
(IM5600M and IM5610M) ..... −55°C to +125°C

*Operating temperature is defined as ambient temperature for the DIP and case temperature for the flatpack. Case temperature is measured directly below the die.

DC CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS V_{CC} = 5.0V ±5% T = 0°C to +75°C MIN	TYP	MAX	LIMITS V_{CC} = 5.0V ±10% T = −55°C to +125°C MIN	TYP	MAX	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		−0.63	−1.0		−0.63	−1.0	mA	V_A = 0.4V
I_{FE}	Chip Enable Input Load Current		−0.63	−1.0		−0.63	−1.0		$V_{\overline{CE}}$ = 0.4V
I_{RA}	Address Input Leakage Current		5.0	40		5.0	60	μA	V_A = 4.5V
I_{RE}	Chip Enable Input Leakage Current		5.0	40		5.0	60		$V_{\overline{CE}}$ = 4.5V
V_{OL}	Output Low Voltage		0.3	0.45		0.3	0.45	V	I_{OL} = 16 mA V_{CE} = 0.4V '0' bit is addressed.
V_{IL}	Input Low Voltage			0.8			0.8		
V_{IH}	Input High Voltage	2.0			2.0				
V_C	Input Clamp Voltage		−0.9	−1.5		−0.9	−1.5		I_{IN} = −10 mA
BV_{IN}	Input Breakdown Voltage	5.5	6.5		5.5	6.5			I_{IN} = 1.0 mA
I_{CC}	Power Supply Current		75	100		75	100	mA	Inputs Either Open or at Ground
I_O (High R State)	Output Leakage Current		<1.0	40		<1.0	100	μA	V_O = 5.5V, V_{CE} = 2.4V
I_O (High R State)	Output Leakage Current		<−1.0	−40		<−1.0	−100		V_O = 0.4V, V_{CE} = 2.4V
C_{IN}	Input Capacitance		5.0			5.0		pF	V_{IN} = 2.0V, V_{CC} = 0V
C_{OUT}	Output Capacitance		7.0			7.0			V_O = 2.0V, V_{CC} = 0V

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The following are guaranteed characteristics of the output high level state when the chip is enabled ($\overline{CE}$ = 0.4V) and a programmed bit is addressed. These characteristics cannot be tested prior to programming but are guaranteed by design.

I_{OLK}	Output Leakage Current		<1.0	100		<1.0	100	μA	V_O = 5.5V, $V_{\overline{CE}}$ = 0.4V
V_{OH} (IM5610)	Output High Voltage	2.4	3.2		2.4	3.2		V	I_{OH} = −1.0 mA (IM5610M) I_{OH} = −2.4 mA (IM5610C)
I_{SC} (IM5610)	Output Short Circuit	−15	−30	−60	−15	−30	−60	mA	V_O = 0V

NOTE 1: Typical characteristics are for V_{CC} = 5.0V, T_A = 25°C.

SWITCHING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	LIMITS V_{CC} = 5V T_A = 25°C MIN	MAX	LIMITS V_{CC} = 5V ±5% T_A = 0°C to +75°C MIN	MAX	LIMITS V_{CC} = 5V ±10% T_A = −55°C to +125°C MIN	MAX	UNITS
T_{AA}	Address Access Time	20	50	20	65	20	75	ns
T_{DIS}	Output Disable Time*	10	40	10	50	10	60	ns
T_{EN}	Output Enable Time*	5	40	5	50	5	60	ns

* Output disable time is the time taken for the output to reach a high resistance state when the chip enable is taken high. Output enable time is the time taken for the output to become active when the chip enable is taken low. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

SWITCHING WAVEFORMS

FIGURE 1: Access Time Via Address Input

FIGURE 2: Output Disable And Enable Time

FIGURE 3: Output Stage Schematics

SWITCHING TIME TEST CONDITIONS

FIGURE 4: Output Load Circuit

SWITCHING PARAMETER	IM5600 R_1	R_2	C_L	IM5610 R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF
t_{DIS}"1"	∞	3.3 KΩ	10 pF	∞	600Ω	10 pF
t_{DIS}"0"	300Ω	600Ω	10 pF	300Ω	600Ω	10 pF
t_{EN}"1"	∞	3.3 KΩ	30 pF	∞	600Ω	30 pF
t_{EN}"0"	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF

INPUT CONDITIONS

Amplitude — 0V to 3V
Rise and Fall Time — 5 ns From 1V to 2V
Frequency — 1 MHz

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PACKAGE OUTLINES

16 LEAD CERAMIC DIP (DE)

16 LEAD PLASTIC DIP (PE)

16 LEAD CERDIP PACKAGE (JE)

16 LEAD FLAT-PACK (FE)

NOTE 1: All dimensions in parenthesis are metric.
NOTE 2: Board drilling dimensions will equal standard practices for .020 diameter lead.

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INTERSIL

IM5603/IM5623 Electrically Programmable 1024 Bit Bipolar Read Only Memory

FEATURES

- Uses Patented AIM Programming Element for
  - Superior Reliability
  - High Programming Yield
  - Fast Programming Speed < 1 sec
  - TTL Processing Compatibility
- Low Power Consumption 439 μW/bit
- Operating Speed
  - Address to Output — 60nS
  - Chip Enable to Output — 35nS
- Large Output Drive — 16mA @ 0.45V
- TTL Compatible Inputs & Outputs
- Two Output Designs
  - 5603 Open Collector
  - 5623 Active Pull-up
- Chip Enables Facilitate Memory Expansion and Use in Bus Organized Systems

APPLICATIONS

- Code Conversion
- Logic Implementation
- Microprogramming
- Look-up Tables
- Control of Sequential Circuits
- Character Generation

GENERAL DESCRIPTION

The Intersil IM5603 and IM5623 are high speed, electrically programmable, fully decoded, bipolar 1024 bit read only memories organized as 256 words by 4 bits. On-chip address decoding, chip enable inputs and uncomitted collector or three-state outputs provide for simplified memory expansion and use in bus organized systems.

Unprogrammed AIM elements are sensed as ZERO's or low logic levels at the outputs. Programming with a commercially available programmer irreversibly converts selected elements in the array so that they are sensed as ONE's or high logic levels.

The following companies make programmers approved by Intersil:

1. Data I/O Corp., P.O. Box 1603, Bellevue, Wash. 98009
2. PRO-LOG Corp., 2411 Garden Rd., Monterey, CA 93940

Detailed programming specifications for all Intersil PROMs are presented in the Intersil BIPOLAR PROM PROGRAMMING SPECIFICATION Data Sheet.

CONNECTION DIAGRAM

TOP VIEW

BLOCK DIAGRAM

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE	ORDER NUMBER
IM5603	16 Pin Ceramic DIP	0°C to +75°C Commercial -55°C to +125°C Military	IM5603CDE IM5603MDE
	16 Pin Flatpack	0°C to +75°C Commercial -55°C to +125°C Military	IM5603CFE IM5603MFE
	16 Pin Plastic DIP	0°C to +75°C	IM5603CPE
	16 Pin Cerdip DIP	0°C to +75°C Commercial -55°C to +125°C Military	IM5603CJE IM5603MJE
IM5623	16 Pin Ceramic DIP	0°C to +75°C Commercial -55°C to +125°C Military	IM5623CDE IM5623MDE
	16 Pin Flatpack	0°C to +75°C Commercial -55°C to +125°C Military	IM5623CFE IM5623MFE
	16 Pin Plastic DIP	0°C to +75°C	IM5623CPE
	16 Pin Cerdip DIP	0°C to +75°C Commercial -55°C to +125°C Military	IM5623CJE IM5623MJE

TRUTH TABLE

ADDRESS INPUTS A_0-A_7	CHIP ENABLE INPUTS $\overline{CE_1}$	CHIP ENABLE INPUTS $\overline{CE_2}$	ANY OUTPUT O_1-O_4
Any one of 256 possible addresses	L	L	H-if the bit uniquely associated with this output and address has been electrically programmed. L-if it has not been programmed.
Any one of 256 possible addresses	H X	X H	All outputs are forced to a high impedance state regardless of address.

X = Don't Care

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +7.0V
Input Voltage Applied ..... −1.5V to 5.5V
Output Voltage Applied ..... −0.5V to +V_{CC}
Output Voltage Applied (Programming Only) 28V
Current Into Output (Programming Only) ..... 210 mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature Range*
(IM5603C and IM5623C) ..... 0°C to +75°C
(IM5603M and IM5623M) ..... −55°C to +125°C

*Operating temperature is defined as ambient temperature for the DIP and case temperature for flatpack. Case temperature is measured directly below the die.

DC CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS V_{CC} = 5.0V ±5% T = 0°C to +75°C MIN	TYP	MAX	LIMITS V_{CC} = 5.0V ±10% T = −55°C to +125°C MIN	TYP	MAX	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		0.63	−1.0		−0.63	−1.0	mA	V_A = 0.4V
I_{FE}	Chip Enable Input Load Current		−0.63	−1.0		−0.63	−1.0	mA	V_{CE} = 0.4V
I_{RA}	Address Input Leakage Current		5	40		5	60	μA	V_A = 4.5V
I_{RE}	Chip Enable Input Leakage Current		5	40		5	60	μA	V_{CE} = 4.5V
V_{OL}	Output Low Voltage		0.3	0.45		0.3	0.45	V	I_{OL} = 16 mA, $V_{\overline{CE1}}$ = $V_{\overline{CE2}}$ = 0.4V '0' bit is addressed.
V_{IL}	Input Low Voltage			0.8			0.8	V	
V_{IH}	Input High Voltage	2.0			2.0			V	
V_C	Input Clamp Voltage		−0.9	−1.5		−0.9	−1.5	V	I_{IN} = −10 mA
BV_{IN}	Input Breakdown Voltage	5.5	6.5		5.5	6.5		V	I_{IN} = 1.0 mA
I_{CC}	Power Supply Current		90	130		90	130	mA	Inputs Either Open or at Ground
I_O (High R State)	Output Leakage Current		<1	40		<1	100	μA	V_O = 5.5V, $V_{\overline{CE1}}$ or
I_O (High R State)	Output Leakage Current		<−1	−40		<−1	−100	μA	V_O = 0.4V, $V_{\overline{CE2}}$ = 2.4V
C_{IN}	Input Capacitance		5			5		pF	V_{IN} = 2.0V, V_{CC} = 0V
C_{OUT}	Output Capacitance		7			7		pF	V_O = 2.0V, V_{CC} = 0V

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The following are guaranteed characteristics of the output high level state when the chip is enabled ($\overline{CE1}$ and $\overline{CE2}$ = 0.4V) and a programmed bit is addressed. These characteristics cannot be tested prior to programming but are guaranteed by design.

I_{OLK}	Output Leakage Current		<1	100		<1	100	μA	V_O = 5.5V
V_{OH} (IM5603)	Output High Voltage	2.4	3.3		2.4	3.3		V	I_{OH} = −0.4 mA
V_{OH} (IM5623)	Output High Voltage	2.4	3.2		2.4	3.2		V	I_{OH} = −2.4 mA (IM5623C) I_{OH} = −1.0 mA (IM5623M)
I_{SC} (IM5603)	Output Short Circuit Current	−1.0	−3.0	−6.0	−1.0	−3.0	−6.0	mA	V_O = 0V
I_{SC} (IM5623)	Output Short Circuit Current	−15	−30	−60	−15	−30	−60	mA	V_O = 0V

NOTE: Typical characteristics are for V_{CC} = 5.0V T_A = 25°C.

SWITCHING CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS V_{CC} = 5.0V T_A = 25°C		LIMITS V_{CC} = 5.0V ±5% T_A = 0°C to +75°C		LIMITS V_{CC} = 5.0V ±10% T_A = −55°C to +125°C		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
t_{AA}	Access Time (Via Address Inputs) (See Figure 1)	20	60	20	70	20	80	ns
t_{DIS}	Output Disable Time* (See Figure 2)	10	35	10	50	10	60	ns
t_{EN}	Output Enable Time* (See Figure 2)	5	35	5	50	5	60	ns

***NOTE:** Output disable time is the time taken for the output to reach a high resistance state when either chip enable is taken high. Output enable time is the time taken for the output to become active when both chip enables are taken low. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

SWITCHING WAVEFORMS

FIGURE 1: Access Time Via Address Inputs

FIGURE 2: Output Enable And Disable Times

SWITCHING TIME TEST CONDITIONS

FIGURE 3: Output Load Circuit

SWITCHING PARAMETER	IM5603			IM5623		
	R_1	R_2	C_L	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF
t_{DIS}"1"	∞	3.3 KΩ	10 pF	∞	600Ω	10 pF
t_{DIS}"0"	300Ω	600Ω	10 pF	300Ω	600Ω	10 pF
t_{EN}"1"	∞	3.3 KΩ	30 pF	∞	600Ω	30 pF
t_{EN}"0"	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF

INPUT CONDITIONS

Amplitude — 0V to 3V
Rise and Fall Time — 5 ns From 1V to 2V
Frequency — 1 MHz

TYPICAL SWITCHING CHARACTERISTICS

IM5603 ADDRESS TO OUTPUT ACCESS DELAY (T_{AA}) VS TEMPERATURE

IM5603 CHIP ENABLE TO OUTPUT ACCESS DELAY (t_{EN}) VS TEMPERATURE

IM5603 CHIP ENABLE TO OUTPUT DISABLE TIME DELAY (t_{DIS}) VS TEMPERATURE

IM5623 ADDRESS TO OUTPUT ACCESS DELAY (t_{AA}) VS TEMPERATURE

IM5623 CHIP ENABLE TO OUTPUT ACCESS DELAY (t_{EN}) VS TEMPERATURE

IM5623 CHIP ENABLE TO OUTPUT DISABLE TIME DELAY (t_{DIS}) VS TEMPERATURE

IM5603 DELAY INCREASE WITH LOAD CAPACITANCE

IM5623 DELAY INCREASE WITH LOAD CAPACITANCE

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TYPICAL DC CHARACTERISTICS

IM5603 OUTPUT LOW CURRENT (I_{OL}) VS OUTPUT LOW VOLTAGE (V_{OL})

IM5623 OUTPUT LOW CURRENT (I_{OL}) VS OUTPUT LOW VOLTAGE (V_{OL})

IM5603 OUTPUT HIGH CURRENT (I_{OH}) VS OUTPUT HIGH VOLTAGE (V_{OH})

IM5623 OUTPUT HIGH CURRENT (I_{OH}) VS OUTPUT HIGH VOLTAGE (V_{OH})

IM5603 OR IM5623 CHIP ENABLE INPUT CURRENT VS INPUT VOLTAGE

IM5603 OR IM5623 ADDRESS INPUT CURRENT VS INPUT VOLTAGE

OUTPUT STAGE SCHEMATICS

IM5603

IM5623

PACKAGE DIMENSIONS

16 LEAD CERAMIC DIP (DE)

16 LEAD PLASTIC DIP (PE)

16 LEAD CERDIP PACKAGE (JE)

16 LEAD FLAT-PACK (FE)

NOTE 1: All dimensions in parenthesis are metric.
NOTE 2: Board drilling dimensions will equal standard practices for .020 diameter lead.

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INTERSIL

IM5604/IM5624 2048 Bit Bipolar Programmable Read Only Memory

FEATURES

- Uses Patented AIM Programming Element for
  - Superior Reliability
  - High Programming Yield
  - Fast Programming Speed < 1 sec
  - TTL Processing Compatibility
- Low Power Consumption 244 μW/bit
- Operating Speed
  - Address to Output — 70nS
  - Chip Enable to Output — 35nS
- Large Output Drive — 16mA @ 0.45V
- TTL Compatible Inputs & Outputs
- Two Output Designs
  - 5604 Open Collector
  - 5624 Active Pull-up
- Chip Enable Facilitates Memory Expansion and Use in Bus Organized Systems

APPLICATIONS

- Code Conversion
- Logic Implementation
- Microprogramming
- Look-up Tables
- Control of Sequential Circuits
- Character Generation

GENERAL DESCRIPTION

The Intersil IM5604 and IM5624 are high speed, electrically programmable, fully decoded, bipolar 2048 bit read only memories organized as 512 words by 4 bits. On-chip address decoding, chip enable inputs and uncomitted collector or three-state outputs provide for simplified memory expansion and use in bus organized systems.

Unprogrammed AIM elements are sensed as ZERO's or low logic levels at the outputs. Programming with a commercially available programmer irreversibly converts selected elements in the array so that they are sensed as ONE's or high logic levels.

The following companies make programmers approved by Intersil:

1. Data I/O Corp., P.O. Box 1603, Bellevue, Wash. 98009
2. PRO-LOG Corp., 2411 Garden Rd., Monterey, CA 93940

Detailed programming specifications for all Intersil PROMs are presented in the Intersil BIPOLAR PROM PROGRAMMING SPECIFICATION DATA SHEET.

CONNECTION DIAGRAM

TOP VIEW

BLOCK DIAGRAM

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE	ORDER NUMBER
IM5604	16 Pin Ceramic DIP	0°C to +75°C Commercial -55°C to +125°C Military	IM5604CDE IM5604MDE
	16 Pin Flatpack	0°C to +75°C Commercial -55°C to +125°C Military	IM5604CFE IM5604MFE
	16 Pin Cerdip DIP	0°C to +75°C Commercial -55°C to +125°C Military	IM5604CJE IM5604MJE
	16 Pin Plastic DIP	0°C to +75°C	IM5604CPE
IM5624	16 Pin Ceramic DIP	0°C to +75°C Commercial -55°C to +125°C Military	IM5624CDE IM5624MDE
	16 Pin Flatpack	0°C to +75°C Commercial -55°C to +125°C Military	IM5624CFE IM5624MFE
	16 Pin Cerdip DIP	0°C to +75°C Commercial -55°C to +125°C Military	IM5624CJE IM5624MJE
	16 Pin Plastic DIP	0°C to +75°C	IM5624CPE

TRUTH TABLE

ADDRESS INPUTS A_0 — A_8	$\overline{CE}$	ANY OUTPUT O_1 — O_4
Any one of 512 possible addresses	L	H — if the bit uniquely associated with this output and address has been electrically programmed. L — if it has not been programmed.
Any one of 512 possible addresses	H	All outputs are forced to a high impedance state regardless of the address.

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +7.0V
Input Voltage Applied ..... −1.5V to +5.5V
Output Voltage Applied ..... −0.5V to +V_{CC}
Output Voltage Applied (Programming Only) 28V
Current Into Output (Programming Only) ..... 210 mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature Range*
(IM5604C and IM5624C) ..... 0°C to +75°C
(IM5604M and IM5624M) ..... −55°C to +125°C

*Operating temperature is defined as ambient temperature for the DIP and case temperature for the flatpack. Case temperature is measured directly below the die.

DC CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS V_{CC} = 5.0V ±5% T = 0°C to +75°C MIN	TYP	MAX	LIMITS V_{CC} = 5.0V ±10% T = −55°C to +125°C MIN	TYP	MAX	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		−0.63	−1.0		−0.63	−1.0	mA	V_A = 0.4V
I_{FE}	Chip Enable Input Load Current		−0.63	−1.0		−0.63	−1.0		$V_{\overline{CE}}$ = 0.4V
I_{RA}	Address Input Leakage Current		5.0	40		5.0	60	μA	V_A = 4.5V
I_{RE}	Chip Enable Input Leakage Current		5.0	40		5.0	60		$V_{\overline{CE}}$ = 4.5V
V_{OL}	Output Low Voltage		0.3	0.45		0.3	0.45	V	I_{OL} = 16 mA $V_{\overline{CE}}$ = 0.4V '0' bit is addressed.
V_{IL}	Input Low Voltage			0.8			0.8		
V_{IH}	Input High Voltage	2.0			2.0				
V_C	Input Clamp Voltage		−0.9	−1.5		−0.9	−1.5		I_{IN} = −10 mA
BV_{IN}	Input Breakdown Voltage	5.5	6.5		5.5	6.5			I_{IN} = 1.0 mA
I_{CC}	Power Supply Current		100	140		100	140	mA	Inputs Either Open or at Ground
I_O (High R State)	Output Leakage Current		<1.0	40		<1.0	100	μA	V_O = 5.5V, $V_{\overline{CE}}$ = 2.4V
I_O (High R State)	Output Leakage Current		<−1.0	−40		<−1.0	−100		V_O = 0.4V, $V_{\overline{CE}}$ = 2.4V
C_{IN}	Input Capacitance		5.0			5.0		pF	V_{IN} = 2.0V, V_{CC} = 0V
C_{OUT}	Output Capacitance		7.0			7.0			V_O = 2.0V, V_{CC} = 0V

The following are guaranteed characteristics of the output high level state when the chip is enabled ($\overline{CE}$ = 0.4V) and a programmed bit is addressed. These characteristics cannot be tested prior to programming but are guaranteed by design.

I_{OLK}	Output Leakage Current		<1.0	100		<1.0	100	μA	V_O = 5.5V, $V_{\overline{CE}}$ = 0.4V
V_{OH} (IM5604)	Output High Voltage	2.4	3.3		2.4	3.3		V	I_O = −0.4 mA
V_{OH} (IM5624)	Output High Voltage	2.4	3.2		2.4	3.2			I_O = −1.0 mA (IM5624M) I_O = −2.4 mA (IM5624C)
I_{SC} (IM5604)	Output Short Circuit Current	−1.0	−3.0	−6.0	−1.0	−3.0	−6.0	mA	V_O = 0V
I_{SC} (IM5624)	Output Short Circuit Current	−15	−30	−60	−15	−30	−60		V_O = 0V

NOTE: Typical characteristics are for V_{CC} = 5.0V, T_A = 25°C.

SWITCHING CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS V_{CC} = 5V T_A = 25°C MIN	MAX	LIMITS V_{CC} = 5V ±5% T_A = 0°C to 70°C MIN	MAX	LIMITS V_{CC} = 5V ±10% T_A = -55°C to +125°C MIN	MAX	UNITS
T_{AA}	Access Time (Via Address Inputs) (See Figure 1)	20	70	20	80	20	90	ns
T_{DIS}	Output Disable Time* (See Figure 2)	10	35	10	50	10	60	ns
T_{EN}	Output Enable Time* (See Figure 2)	5	35	5	50	5	60	ns

***NOTE:** Output disable time is the time for the output to reach a high resistance state when either chip enable is taken high. Output enable time is the time taken for the output to become active when both chip enables are taken low. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

SWITCHING WAVEFORMS

FIGURE 1: Access Time Via Address Inputs

FIGURE 2: Output Enable And Disable Times

SWITCHING TIME TEST CONDITIONS

FIGURE 3: Output Load Circuit

SWITCHING PARAMETER	IM5604 R_1	R_2	C_L	IM5624 R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF
t_{DIS}"1"	∞	3.3 KΩ	10 pF	∞	600Ω	10 pF
t_{DIS}"0"	300Ω	600Ω	10 pF	300Ω	600Ω	10 pF
t_{EN}"1"	∞	3.3 KΩ	30 pF	∞	600Ω	30 pF
t_{EN}"0"	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF

INPUT CONDITIONS

Amplitude — 0V to 3V
Rise and Fall Time — 5 ns From 1V to 2V
Frequency — 1 MHz

TYPICAL DC CHARACTERISTICS

IM5604 OUTPUT LOW CURRENT (I_{OL}) VS OUTPUT LOW VOLTAGE (V_{OL})

IM5624 OUTPUT LOW CURRENT (I_{OL}) VS OUTPUT LOW VOLTAGE (V_{OL})

IM5604 OUTPUT HIGH CURRENT (I_{OH}) VS OUTPUT HIGH VOLTAGE (V_{OH})

IM5624 OUTPUT HIGH CURRENT (I_{OH}) VS OUTPUT HIGH VOLTAGE (V_{OH})

IM5604 OR IM5624 CHIP ENABLE INPUT CURRENT VS INPUT VOLTAGE

IM5604 OR IM5624 ADDRESS INPUT CURRENT VS INPUT VOLTAGE

OUTPUT STAGE SCHEMATICS

IM5604

IM5624

PACKAGE DIMENSIONS

16 LEAD CERAMIC DIP (DE)

16 LEAD PLASTIC DIP (PE)

16 LEAD CERDIP PACKAGE (JE)

16 LEAD FLAT-PACK (FE)

NOTE 1: All dimensions in Parenthesis are metric.
NOTE 2: Board drilling dimensions will equal standard practices for .020 lead.

INTERSIL

IM5605/IM5625 4096 Bit Bipolar Programmable Read Only Memory

FEATURES

- Uses Patented AIM Programming Element for
  - Superior Reliability
  - High Programming Yield
  - Fast Programming Speed < 1 sec
  - TTL Processing Compatibility
- Low Power Consumption 171 μW/bit
- Operating Speed
  - Address to Output — 70 nS
  - Chip Enable to Output — 45 nS
- Large Output Drive — 16mA @ 0.45V
- TTL Compatible Inputs & Outputs
- Two Output Designs
  - 5605 Open Collector
  - 5625 Active Pull-up
- Chip Enables Facilitate Memory Expansion and Use in Bus Organized Systems

APPLICATIONS

- Code Conversion
- Logic Implementation
- Microprogramming
- Look-up Tables
- Control of Sequential Circuits
- Character Generation

GENERAL DESCRIPTION

The Intersil IM5605 and IM5625 are high speed, electrically programmable, fully decoded, bipolar 4096 bit read only memories organized as 512 words by 8 bits. On-chip address decoding, chip enable inputs and uncommitted collector or three-state outputs provide for simplified memory expansion and use in bus organized systems.

Unprogrammed AIM elements are sensed as ZERO's or low logic levels at the outputs. Programming with a commercially available programmer irreversibly converts selected elements in the array so that they are sensed as ONE's/or high logic levels.

The following companies make programmers approved by Intersil:

1. Data I/O Corp., P.O. Box 1603, Bellevue, Wash. 98009
2. PRO-LOG Corp., 2411 Garden Rd., Monterey, CA 93940

Detailed programming specifications for all Intersil PROMs are presented in the Intersil BIPOLAR PROM PROGRAMMING SPECIFICATION Data Sheet.

BLOCK DIAGRAM

CONNECTION DIAGRAM

NOTE 1: Pin 22 must be left open during normal operation and connected to V_{CC} during programming.

NOTE 2: The chip is enabled when $\overline{CE_1}$ and $\overline{CE_2}$ are low and CE_3 and CE_4 are high.

TRUTH TABLE

ADDRESS INPUTS A_0-A_8	CHIP ENABLE INPUTS $\overline{CE_1}$	$\overline{CE_2}$	CE_3	CE_4	ANY OUTPUT O_1-O_8
Any one of 512 possible addresses.	L	L	H	H	H-if the bit uniquely associated with this output and address has been electrically programmed. L-if it has not been programmed.
Any one of 512 possible addresses.	H X X X	X H X X	X X L X	X X X L	All outputs are forced to a high impedance state regardless of the address.

X = Don't Care.

ORDERING INFORMATION

PART NUMBER	PACKAGE	TEMPERATURE RANGE	ORDER NUMBER
IM5605	24 Pin Cerdip DIP	0°C to +75°C Commercial	IM5605CJG
		-55°C to +125°C Military	IM5605MJG
	24 Pin Ceramic DIP	0°C to +75°C Commercial	IM5605CDG
		-55°C to +125°C Military	IM5605MDG
IM5625	24 Pin Cerdip DIP	0°C to +75°C Commercial	IM5625CJG
		-55°C to +125°C Military	IM5625MJG
	24 Pin Ceramic DIP	0°C to +75°C Commercial	IM5625CDG
		-55°C to +125°C Military	IM5625MDG

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ABSOLUTE MAXIMUM RATINGS

Supply Voltage ..... +7.0V
Input Voltage Applied ..... −1.5V to +5.5V
Output Voltage Applied ..... −0.5V to +V_{CC}
Output Voltage Applied (Programming Only) 28V
Current Into Output (Programming Only) 210mA
Storage Temperature ..... −65°C to +150°C
Operating Temperature Range*
(IM5605C and IM5625C) ..... 0°C to +75°C
(IM5605M and IM5625M) ..... −55°C to +125°C

*Operating temperature is defined as ambient temperature for the DIP and case temperature for the flatpack. Case temperature is measured directly below the die.

DC CHARACTERISTICS

SYMBOL	CHARACTERISTICS	LIMITS V_{CC} = 5.0V ±5% T = 0°C to +75°C MIN	TYP	MAX	LIMITS V_{CC} = 5.0V ±10% T = −55°C to +125°C MIN	TYP	MAX	UNITS	CONDITIONS
I_{FA}	Address Input Load Current		−0.63	−1.0		−0.63	−1.0	mA	V_A = 0.4V
I_{FE}	Chip Enable Input Load Current		−0.63	−1.0		−0.63	−1.0		V_{CE} = 0.4V
I_{RA}	Address Input Leakage Current		5.0	40		5.0	60	μA	V_A = 4.5V
I_{RE}	Chip Enable Input Leakage Current		5.0	40		5.0	60		V_{CE} = 4.5V
V_{OL}	Output Low Voltage		0.3	0.45		0.3	0.45	V	I_{OL} = 16 mA $V_{\overline{CE1}}$ & $V_{\overline{CE2}}$ = 0.4V, V_{CE3} & V_{CE4} = 4.5V "0" bit is addressed
V_{IL}	Input Low Voltage			0.8			0.8		
V_{IH}	Input High Voltage	2.0			2.0				
V_C	Input Clamp Voltage		−0.9	−1.5		−0.9	−1.5		I_{IN} = −10 mA
BV_{IN}	Input Breakdown Voltage	5.5	6.5		5.5	6.5			I_{IN} = 1.0 mA
I_{CC}	Power Supply Current		140	185		140	185	mA	Inputs Either Open or at Ground
I_O(High R State)	Output Leakage Current		<1.0	40		<1.0	100	μA	V_O = 5.5V, $V_{\overline{CE1}}$ = 2.4 or $V_{\overline{CE2}}$ = 2.4V or V_{CE3} = 0.4V or V_{CE4} = 0.4V
I_O(High R State)	Output Leakage Current		<−1.0	−40		<−1.0	−100		V_O = 0.4V
C_{IN}	Input Capacitance		5.0	10		5.0	10	pF	V_{IN} = 2.0V, V_{CC} = 0V
C_{OUT}	Output Capacitance		7.0	12		7.0	12		V_O = 2.0V, V_{CC} = 0V

The following are guaranteed characteristics of the output high level state when the chip is enabled and a programmed bit is addressed. These characteristics cannot be tested prior to programming but are guaranteed by design.

I_{OLK}	Output Leakage Current		<1.0	100		<1.0	100	μA	V_O = 5.5V
V_{OH}(IM5605)	Output High Voltage	2.4	3.3		2.4	3.3		V	I_{OH} = −0.4 mA
V_{OH}(IM5625)	Output High Voltage	2.4	3.2		2.4	3.2			I_{OH} = −1.0 mA (IM5625M) I_{OH} = −2.4 mA (IM5625C)
I_{SC}(IM5605)	Output Short Circuit Current	−1.0	−3.0	−6.0	−1.0	−3.0	−6.0	mA	V_O = 0V
I_{SC}(IM5625)	Output Short Circuit Current	−15	−30	−60	−15	−30	−60		V_O = 0V

NOTE: Typical characteristics are for V_{CC} = 5V, T_A = 25°C.

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SWITCHING CHARACTERISTICS

SYMBOL	CHARACTERISTIC	LIMITS V_{CC} = 5V T_A = 25°C		LIMITS V_{CC} = 5V ± 5% T_A = 0 to 75°C		LIMITS V_{CC} = 5V ± 10% T_A = −55°C to +125°C		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
T_{AA}	Address Access Time (See Figure 1)	20	70	20	90	20	105	ns
T_{DIS}	Output Disable Time* (See Figure 2)	10	45	10	55	10	65	ns
T_{EN}	Output Enable Time* (See Figure 2)	5	45	5	55	5	65	ns

***NOTE:** Output disable time is the time taken for the output to reach a high resistance state when any chip enable is taken to its inactive level. Output enable time is the time taken for the output to become active when all chip enables are taken to their active (enabling) levels. The high resistance state is defined as a point on the output waveform equal to a ΔV of 0.5V from the active output level.

SWITCHING WAVEFORMS

FIGURE 1: Access Time Via Address Inputs

FIGURE 2: Output Enable And Disable Times

SWITCHING TIME TEST CONDITIONS

FIGURE 3: Output Load Circuit

SWITCHING PARAMETER	IM5605			IM5625		
	R_1	R_2	C_L	R_1	R_2	C_L
t_{AA}	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF
t_{DIS}"1"	∞	3.3KΩ	10 pF	∞	600Ω	10 pF
t_{DIS}"0"	300Ω	600Ω	10 pF	300Ω	600Ω	10 pF
t_{EN}"1"	∞	3.3 KΩ	30 pF	∞	600Ω	30 pF
t_{EN}"0"	300Ω	600Ω	30 pF	300Ω	600Ω	30 pF

INPUT CONDITIONS

Amplitude — 0V to 3V
Rise and Fall Time — 5 ns From 1V to 2V
Frequency — 1 MHz

TYPICAL DC CHARACTERISTICS

IM5605 OUTPUT LOW CURRENT (I_{OL}) VS OUTPUT LOW VOLTAGE (V_{OL})

IM5625 OUTPUT LOW CURRENT (I_{OL}) VS OUTPUT LOW VOLTAGE (V_{OL})

IM5605 OUTPUT HIGH CURRENT (I_{OH}) VS OUTPUT HIGH VOLTAGE (V_{OH})

IM5625 OUTPUT HIGH CURRENT (I_{OH}) VS OUTPUT HIGH VOLTAGE (V_{OH})

IM5605 OR IM5625 CHIP ENABLE INPUT CURRENT VS INPUT VOLTAGE

IM5605 OR IM5625 ADDRESS INPUT CURRENT VS INPUT VOLTAGE

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APPLICATION NOTES

Memory expansion is accomplished by the use of the chip enable inputs. The chip is enabled if $\overline{CE_1}$ and $\overline{CE_2}$ are low and CE_3 and CE_4 are high.

2048 WORD X 32 BIT MEMORY

The memory is organized as 4 groups of 512 words X 32 bits each. The 4 groups are controlled by I_9 & I_{10} of the data bus which are connected to the chip enable inputs (See Truth Table). Word selection, within a word group, is controlled by I_0 through I_8 of the data bus connected in parallel with A_0 through A_8 of all 16 chips. Chip outputs, Q_0 through Q_7 are connected in parallel by column to give a system output of 32 bits (4 columns X 8 bits).

TRUTH TABLE

GROUP	I_9	I_{10}	SELECTED GROUP CHIP SELECT CONDITIONS			
			$\overline{CE_1}$	$\overline{CE_2}$	CE_3	CE_4
0 ~ 511	L	L	I_9	I_{10}	V_{CC}	V_{CC}
512 ~ 1023	H	L	V_{SS}	I_{10}	I_9	V_{CC}
1024 ~ 1535	L	H	V_{SS}	I_9	I_{10}	V_{CC}
1536 ~ 2047	H	H	V_{SS}	V_{SS}	I_9	I_{10}

ADDRESS BUS

POWER SWITCHING

4096 WORDS × 16 BIT PROM ORGANIZATION
POWER SWITCHED WITH DISCRETE PNP TRANSISTOR SWITCHES AND 1/8 SCHOTTKY TTL DECODER

5V CURRENT
≈ 345 mA including PNP switches and 1 of 8 decoder or 26μW/bit

PARTS
8 PNP's - 2N3467
8 R_1 = 1 KOhm, 1/4W, ±5%
8 R_2 = 300 Ohm, 1/4W, ±5%
8 C_1 = 560 pF
16 5605's
1 74S138

Note: Access time via power switches is dependent on the RC time constant of the switch and other filter capacitors.

OUTPUT STAGE SCHEMATICS

IM5605

IM5625

PACKAGE DIMENSIONS

24 LEAD CERDIP PACKAGE (JG)

NOTE 1: All dimensions in parenthesis are metric.
NOTE 2: Board drilling dimensions will equal standard practices for .020 diameter lead.

Bipolar PROM Programming Specification

PROGRAMMING PROCEDURES

1. Preceding a programming cycle the part to be programmed must be searched for previously programmed bits. This procedure eliminates the risk of beginning programming on a part that has some bits not conforming to the pattern desired.
2. Programming is begun by addressing the first word in the sequence, normally address ZERO, although satisfactory programming is not dependent on the word sequence or bit order used.
3. Disable the device by applying a normal TTL high logic level to any active low CE pin. Each device in the family has at least one active low Chip Enable pin. Disabling the device forces the normal output circuitry to a high impedance condition so that it will not be affected by programming pulses applied through the output pins to the programming element array.
4. Sense the bit status by forcing 20mA into the associated output pin and comparing the resultant voltage to the SENSE VOLTAGE.
5. If the bit is to be programmed, increase the 20mA to 200mA at the proper ramp rate and maintain 200mA for 2.5μS. The constant current source must be clamped at 28V.
6. Reduce the current from 200 to 20mA and after 1μS compare the resultant 20mA voltage level to the SENSE VOLTAGE.
7. If the voltage is greater than the SENSE VOLTAGE the current should be increased again to 200mA for another 2.5μS. Generally programming occurs on the first pulse, but repeated attempts are allowed up to an elapsed time of 100mS.

PROGRAMMING PARAMETER SPECIFICATIONS

The following specification details the necessary requirements for the correct programming of the IM56XX Series of AIM PROMs. Intersil will not accept responsibility for any device found to be defective if it was not programmed according to these specifications.

PARAMETER	LIMITS MIN	NOM	MAX	UNITS	CONDITIONS
Programming Current Pulse Amplitude	190	200	210	mA	Constant current to be supplied over a 10 to 28V voltage range. Set the nominal value with a 100Ω, 6W load @ 20V.
Voltage Clamp	27.5	28	28.5	Volts	Constant voltage clamp when sinking 130 to 210 mA. Adjust nominal level when sinking 200 mA.
Ramp Rate $\frac{dv}{dt}$ of Program Current Source	50	60	70	V/μs	Voltage ramp rate is measured by switching from 20 to 200 mA into a 100 ohm, 6W resistor with the maximum voltage clamped at 28V.
Pulse Width	2.0	2.5	3.0	μs	Measured at 10V when switching between 20 and 200 mA into a 100 ohm, 6W load resistor.
Duty Cycle	20	25	30	%	Measured at 10V when switching between 20 and 200 mA into a 100 ohm, 6W load resistor.
Sense Current Amplitude	19.5	20.0	20.5	mA	Constant current source amplitude is adjusted for a nominal value of 20 mA into a 12V, 400 mW zener diode load.
Ramp Rate $\frac{dv}{dt}$ Sense Current Source	50	60	70	V/μs	Voltage ramp rate is measured by switching from 0 to 20 mA into a 1.5k ohm, 1W resistor with the maximum voltage clamped at 28V.
Sense Voltage Analog Comparator Reference Voltage	6.9	7.0	7.1	Volts	An element is considered programmed when the voltage sensed at the appropriate output pin with 20 mA forced through the element is less than the analog comparator reference voltage.
5600/10 Only	12.4	12.5	12.6	Volts	
Min. delay from trailing edge of programming pulse before sensing	0.9	1.0	1.1	μs	Measured from the 10V level of the voltage pulse when switching from 200 to 20 mA into a 100 ohm, 6W load resistor.
Vcc	4.9	5.0	5.5	Volts	100 to 200 mA current range.
Programming Time Allocation/Bit	—	100	—	ms	Maximum time allowed to program a bit.
Extra Programming Pulses	—	4	—	Pulse	Absolute number of programming pulses to be issued after the bit output is first sensed as a programmed '1'. This occurs when the sensed voltage is less than the comparator reference voltage.

PROGRAMMING PROCEDURES (Continued)

8. If the voltage after a programming current pulse is less than the SENSE VOLTAGE, four additional programming pulses are applied with a sense after each pulse.
9. After the fourth extra pulse and correct sense, programming is complete. The 20mA current pulse then is shut off and the address is changed to program the next bit.
10. Repeat steps 4 thru 9 until a successful programming and sense operation is performed at all address locations to be programmed.
11. After the programming cycle is complete, a logical verification must be performed. This is done by cycling through all address locations with the chip enabled and testing the voltage level at each output under the appropriate current forcing conditions (20mA for a low level and 100μA for a high level). This cycle should be completed at both low and high V_{CC}.

POST PROGRAMMING LOGICAL VERIFICATION

Both high (V_{OH}) and low (V_{OL}) logic levels on all outputs should be tested. For all truth-table addresses two passes must be made, one with V_{CC} high (V_{CCH}) and one with V_{CC} low (V_{CCL}). Forcing conditions and limits for level testing are specified in the following tables.

HIGH V_{CC} TESTS — V_{CCH} = 6.5 ± .1V

PARAMETER	LIMIT MIN	LIMIT MAX	FORCING CONDITION	LEVEL TESTED
V_{OL}	—	.85	I_{OL} = 20mA ± 1mA	Zero
V_{OH}	6.9	—	I_{OLK} = 100μA ± 10μA	One

LOW V_{CC} TESTS — V_{CCL} = 4.0V ± .1V

PARAMETER	LIMIT MIN	LIMIT MAX	FORCING CONDITION	LEVEL TESTED
V_{OL}	—	.85	I_{OL} = 20mA ± 1mA	Zero
V_{OH}	4.5	—	I_{OLK} = 100μA ± 10μA	One

PROGRAMMING CYCLE TIMING DIAGRAM

A - 20mA CURRENT SOURCE TURNED ON (VOLTAGE OVERSHOOT MAY OCCUR)
B - VOLTAGE LEVEL IS SENSED AND COMPARED
C - 180mA CURRENT SOURCE IS TURNED ON (180 + 20 = 200mA)
D - VOLTAGE FALLS INDICATING PROGRAMMING
E - 180mA CURRENT SOURCE IS TURNED OFF
F - VOLTAGE LEVEL IS SENSED AND COMPARED
G - 180mA CURRENT SOURCED IS TURNED ON
H - 20mA CURRENT SOURCE IS TURNED OFF
I - ADDRESS IS CHANGED

INTERSIL

IM6100 CMOS 12 Bit Microprocessor

FEATURES

- Silicon Gate Complementary MOS
- Fully Static - 0 to 5.7 MHz
- Single Power Supply
  IM6100 V_{CC} = 5 volts
  IM6100A V_{CC} = 10 volts
- Crystal Controlled On Chip Timing
- PDP®-8/e, Instruction Set Compatible
- Low Power Dissipation
  < 10mW @ 3.3 MHz @ 5 volts
- TTL Compatible at 5 volts
- Excellent Noise Immunity
- Direct Memory Access (DMA)
- Interrupt

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GENERAL DESCRIPTION

The IM6100 is a fixed word length, single word instruction, parallel transfer microprocessor using 12-bit, two's complement arithmetic which recognizes the instruction set of Digital Equipment Corporation's PDP-8/e minicomputer. The internal circuitry is completely static and designed to operate at any speed between DC and the maximum operating frequency. Two pins are available to allow for an external crystal, thereby eliminating the need for clock generators and level translators. The crystal can be removed and the processor clocked by an external clock generator. The device design is optimized to minimize the number of external components required for interfacing with standard memory and peripheral devices.

The IM6100 family includes IM6101 (Programmable Interfacing Element), IM6102 (Memory Extension/DMA Controller/Interval Timer), IM6103 (Parallel Input-Output Port), IM6512 (64 x 12 RAM), IM6312 (1k x 12 ROM), and IM6402/03 (UART), all featuring ultra low power-high noise immunity CMOS characteristics. The entire family is supported by the 6910 Intercept II Microcomputer Development System.

PIN CONFIGURATION

PACKAGE DIMENSIONS

ORDERING INFORMATION

ORDER CODE	IM6100-1	IM6100A	IM6100
PLASTIC PKG.	IM6100-1IPL	IM6100-AIPL	IM6100-IPL
CERAMIC PKG.	IM6100-1IDL	IM6100-AIDL	—
MILITARY TEMP.	IM6100-1MDL	IM6100-AMDL	—
MILITARY TEMP. WITH 883B	IM6100-1MDL/883B	IM6100-AMDL/883B	—

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Figure 1: Functional Block Diagram

FUNCTIONAL PIN DESCRIPTIONS

PIN	SYMBOL	DESCRIPTION
1	Vcc	Supply voltage.
2	RUN	The signal indicates the runstate of the CPU and may be used to power down the external circuitry
3	DMAGNT	Direct Memory Access Grant—DX lines are three-state.
4	$\overline{\text{DMAREQ}}$	Direct Memory Access Request—DMA is granted at the end of the current instruction. Upon DMA grant, the CPU suspends program execution until the DMAREQ line is released.
5	$\overline{\text{CPREQ}}$	Control Panel Request—a dedicated interrupt which bypasses the normal device interrupt request structure.
6	$\overline{\text{RUN/HLT}}$	Pulsing the Run/Halt line causes the CPU to alternately run and halt by changing the state of the internal RUN/HLT flip flop.
7	$\overline{\text{RESET}}$	Clears the AC and loads 7777_8 into the PC. CPU is halted.
8	$\overline{\text{INTREQ}}$	Peripheral device interrupt request.
9	XTA	External coded minor cycle timing—signifies input transfers to the IM6100.
10	LXMAR	The Load External Memory Address Register is used to store memory and peripheral addresses externally.
11	$\overline{\text{WAIT}}$	Indicates that peripherals or external memory is not ready to transfer data. The CPU state gets extended as long as WAIT is active. The CPU is in the lowest power state with clocks running.
12	XTB	External coded minor cycle timing—signifies output transfers from the IM6100.
13	XTC	External coded minor cycle timing—used in conjunction with the Select Lines to specify read or write operations.
14	OSC OUT	Crystal input to generate the internal timing (also external clock input).
15	OSC IN	See Pin 14—OSC OUT (also external clock ground)
16	DX_0	DataX—multiplexed data in, data out and address lines.
17	DX_1	See Pin 16—DX_0.

PIN	SYMBOL	DESCRIPTION
18	DX_2	See Pin 16—DX_0.
19	DX_3	See Pin 16—DX_0.
20	DX_4	See Pin 16—DX_0.
21	DX_5	See Pin 16—DX_0.
22	DX_6	See Pin 16—DX_0.
23	DX_7	See Pin 16—DX_0.
24	DX_8	See Pin 16—DX_0.
25	DX_9	See Pin 16—DX_0.
26	GND	Ground
27	DX_{10}	See Pin 16—DX_0.
28	DX_{11}	See Pin 16—DX_0.
29	LINK	Indicates state of link flip flop.
30	$\overline{\text{DEVSEL}}$	Device Select for I/O transfers.
31	$\overline{\text{SWSEL}}$	Switch Register Select for the OR THE SWITCH REGISTER INSTRUCTION (OSR). OSR is a Group 2 Operate Instruction which reads a 12 bit external switch register and OR's it with the contents of the AC.
32	$\overline{C_0}$	Control line inputs from the peripheral device during an I/O transfer (Table VI).
33	$\overline{C_1}$	See Pin 32—$\overline{C_0}$.
34	$\overline{C_2}$	See Pin 32—$\overline{C_0}$.
35	$\overline{\text{SKP}}$	Skips the next sequential instruction if active during an I/O instruction.
36	IFETCH	Instruction Fetch Cycle
37	$\overline{\text{MEMSEL}}$	Memory Select for memory transfers.
38	$\overline{\text{CPSEL}}$	The Control Panel Memory Select becomes active, instead of the MEMSEL, for control panel routines. Signal may be used to distinguish between control panel and main memories.
39	INTGNT	Peripheral device Interrupt Grant.
40	DATAF	Data Field pin indicates the execute phase of indirectly addressed AND, TAD, ISZ and DCA instructions so that the data transfers are controlled by the Data Field, DF, and not the Instruction Field, IF, if Extended Memory Control hardware is used to extend the addressing space from 4K to 32K words.

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ARCHITECTURE

The IM6100 has 6 twelve bit registers, a programmable logic array, an arithmetic and logic unit and associated gating and timing circuitry. A block diagram of the IM6100 is shown in Figure 1.

ACCUMULATOR (AC)

The AC is a 12-bit register in which arithmetic and logical operations are performed. Data words may be transferred from memory to the AC or transferred from the AC into memory. Arithmetic and logical operations involve one or two operands, one held in the AC and the other fetched from the memory. The result of the operation is left in the AC which may be cleared, complemented, tested, incremented or rotated under program control. The AC also serves as an input-output register, as all programmed data transfers pass through the AC.

LINK (L)

The Link is a 1-bit flip-flop that serves as a high-order extension of the AC. It is used as a carry flip-flop for 2's complement arithmetic. A carry out of the accumulator complements the Link. Link can be cleared, set, complemented and tested under program control and rotated as part of the AC.

MQ REGISTER (MQ)

The MQ is a 12-bit temporary register which is program accessible. The contents of AC may be transferred to the MQ for temporary storage, or MQ can be OR'ed with the AC and the result stored in the AC. The contents of the AC and the MQ may also be exchanged.

MEMORY ADDRESS REGISTER (MAR)

While accessing memory, the 12-bit MAR register contains the address of the memory location that is currently selected for reading or writing. The MAR is also used as an internal register for microprogram control during data transfers to and from memory and peripherals.

PROGRAM COUNTER (PC)

The 12-bit PC contains the address of the memory location from which the next instruction is fetched. During an instruction fetch, the PC is transferred to MAR and the PC is then incremented by 1. When there is a branch to another address in memory, the branch address is set into the PC. Branching normally takes place under program control, however, during an input-output operation, a device may specify a branch address. A skip (SKP) instruction increments the PC by 1, thus causing the next instruction to be skipped. The SKP instruction may be unconditional, or conditional on the state of the AC or the Link. During an input-output operation, a device can also cause the next sequential instruction to be skipped. Interrupts force the PC to 0000. Reset forces the PC to 7777_8.

ARITHMETIC AND LOGICAL UNIT (ALU)

The ALU performs both arithmetic and logical operations, –two's complement binary addition, AND, OR and complement. The ALU can perform a single position shift either to the left or to the right; a double rotate is implemented in two single bit shifts. The ALU can also shift by 3 positions to implement a byte swap in two steps. The AC is always one of the inputs to the ALU, however, under internal microprogram control, AC may be gated off and all one's or all zero's gated in. The second input may be any one of the other registers under internal microprogram control.

TEMPORARY REGISTER (TEMP)

The 12-bit TEMP register latches the result of an ALU operation, before it is sent to the destination register, to avoid race conditions. The TEMP is also used as an internal register for microprogram control.

INSTRUCTION REGISTER (IR)

During an instruction fetch, the 12-bit IR is loaded with the instruction that is to be executed by the CPU. The IR specifies the initial step of the microprogram sequence for each instruction, and is also used as an internal register to store temporary data for microprogram control.

MULTIPLEXER (DX)

The 12-bit Input/Output Multiplexer handles data, address and instruction transfers into and out of the CPU, and to or from the main memory and peripheral devices on a time-multiplexed basis.

MAJOR STATE GENERATOR AND THE PROGRAMMED LOGIC ARRAY (PLA)

During an instruction fetch the instruction to be executed is loaded into the IR. The PLA is then used for the correct sequencing of the CPU for the appropriate instruction. After an instruction is completely sequenced, the major state generator scans the internal priority network, which decides whether the machine is going to fetch the next instruction in sequence, or service one of the external request lines.

PLA OUTPUT LATCH

The PLA Output Latch permits the PLA to be pipelined; it fetches the next control sequence while the CPU is executing the current sequence.

MEMORY AND DEVICE CONTROL, ALU AND REG TRANSFER LOGIC

The Memory and Device Control Unit provides external control signals to communicate with peripheral devices (DEVSEL), switch register (SWSEL), memory (MEMSEL) and/or control panel memory (CPSEL). During I/O instructions this unit also modifies the PLA outputs depending on the states of the four device control lines (SKP, C_0, C_1, C_2). The ALU and Register Transfer Logic provides the control signals for the internal register transfers and ALU operation.

ARCHITECTURE (CONTINUED)

TIMING AND STATE CONTROL

The IM6100 internally generates all the timing and state signals. A crystal is used to control the CPU operating frequency, which is divided by two by the CPU. With a 4MHz crystal, the internal states will be of 500nsec duration. The major timing states are described in Figure 2.

T_1 For memory reference instructions, a 12-bit address is sent on the DX lines. The Load External Memory Address Register, LXMAR, is used to clock an external register to store the address information externally, if required. When executing an Input-Output I/O instruction, the instruction being executed is sent on the DX lines to be stored externally. The external address register then contains the device address and control information. The LXMAR pulse occurs only if a valid address is present on the DX lines.

Various CPU request lines are priority sampled if the next cycle is an Instruction Fetch cycle. Current state of the CPU is available externally.

T_2 Memory/Peripheral data is read for an input transfer (READ). WAIT controls the transfer duration. If WAIT is active during input transfers, the CPU waits in the T_2 state. The wait duration is an integral multiple of the crystal frequency — 250nsec for 4MHz.

For memory reference instructions, the Memory Select, MEMSEL, line is active. For I/O instructions the Device Select, DEVSEL, line is active. Control lines, therefore, distinguish the contents of the external register as memory or device address.

External device sense lines, C_0, C_1, C_2, and SKP, are sampled if the instruction being executed is an I/O instruction.

Control Panel Memory Select, CPSEL, and Switch Register Select, SWSEL, become active low for data transfers between the IM6100 and Control Panel Memory and the Switch Register, respectively.

T_3,T_4,T_5 ALU operation and internal register transfers.

T_6 This state is entered for an output transfer (WRITE). The address is defined during T_1. WAIT controls the time for which the Write data must be maintained.

Figure 2: IM6100 AC Timing Diagram

MEMORY ORGANIZATION

The IM6100 has a basic addressing capacity of 4096 12-bit words which may be extended by Extended Memory Control hardware to 32K. The memory system is organized in 4096 word blocks, called MEMORY FIELDS. The first 4096 words of memory are in Field 0; if a full 32K of memory is installed, the uppermost Memory Field will be numbered 7. In any given Memory Field every location has a unique 4 digit octal (12 bit binary) address, 0000_8 to 7777_8 (0000_{10} to 4095_{10}). Each Memory Field is subdivided into 32 PAGES of 128 words each. Memory Pages are numbered sequentially from Page 00_8, containing addresses 0000-0177_8, to Page 37_8, containing addresses 7600_8-7777_8. The first 5 bits of a 12-bit MEMORY ADDRESS denote the PAGE NUMBER and the low order 7 bits specify the PAGE ADDRESS of the memory location within the given Page.

During an instruction fetch cycle, the IM6100 fetches the instruction pointed to by the PC, the contents of the PC are transferred to the MAR, and the PC is incremented by 1. The PC now contains the address of the 'next' sequential instruction and the MAR contains the address of the 'current' instruction which must be fetched from memory. Bits 0-4 of the MAR identify the CURRENT PAGE, that is, the Page from which instructions are currently being fetched, and bits 5-11 of the MAR identify the location within the Current Page. (PAGE ZERO (0), by definition, denotes the first 128 words of memory, 0000_8-0177_8.)

Memory Organization

INSTRUCTION SET

The IM6100 instructions are 12-bit words stored in memory. The IM6100 makes no distinction between instructions and data; it can manipulate instructions as stored variables or execute data as instructions when it is programmed to do so. There are three general classes of IM6100 instructions. They are referred to as Memory Reference Instruction (MRI), Operate Instruction (OPR) and Input/Output Transfer Instruction (IOT).

The notations used in the following instruction tables are defined in Table I below:

TABLE 1. Notation Definitions

1. ( ) denotes the contents of the register or location within parenthesis. (EA) is read as "... the contents of the Effective Address."
2. ((I)) denotes the contents of the location pointed to by the contents of the location within the double parenthesis. ((PA)) is read as "... the contents of the location pointed to by the contents of the Pointer Address."
3. ← denotes "... is replaced by ..."
4. ↔ denotes the interchange operation.
5. ∧ denotes logical AND operation.
6. ∨ denotes logical OR operation.
7. EA denotes the Effective Address for Direct Addressing.
8. PA denotes the Pointer Address for Indirect Addressing. PA can be any address on the CURRENT PAGE or PA can be any address (0000_8) through (0177_8) on PAGE ZERO other than the addresses (0010_8) through (0017_8) which are reserved for autoindexing.
9. PAIX denotes the Pointer Address for autoindexing. It can be any address (0010_8) through (0017_8).
10. I represents bit 3, the Indirect Addressing Bit, of the instruction.
11. EA, PA, or PAIX is specified by bit 4 through bit 11 of the memory reference instruction.
12. PC denotes the Program Counter.
13. SR denotes the Switch Register.
14. (AC)n denotes the nth bit of the AC contents.
15. DEV denotes a specific peripheral device and "dddddd" denotes the device address code. CMND is the command issued to the device during an I/O operation and "eee" is its three bit code.

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INSTRUCTION SET (CONTINUED)

MEMORY REFERENCE INSTRUCTION (MRI)

The Memory Reference Instructions operate on the contents of a memory location or use the contents of a memory location to operate on the AC or the PC. The first 3 bits of a Memory Reference Instruction specify the operation code, or OPCODE, and the low order 9 bits, the OPERAND address, as shown in Figure 3.

Figure 3: Memory Reference Instruction Format

Bits 5 through 11, the PAGE ADDRESS, identify the location of the OPERAND on a given page, but they do not identify the page itself. The page is specified by bit 4, called the CURRENT PAGE OR PAGE 0 BIT. If bit 4 is a 0, the page address is interpreted as a location on Page 0. If bit 4 is a 1, the page address specified is interpreted to be on the Current Page.

For example, if bits 5 through 11 represent 123_8 and bit 4 is a 0, the location referenced is the absolute address 0123_8. However, if bit 4 is a 1 and the current instruction is in a memory location whose absolute address is 4610_8 the page address 123_8 designates the absolute address 4723_8, as shown below.

4610_8 = 100 110 001 000 = PAGE 10 011 = PAGE 23_8
Location 4610_8 is in PAGE 23_8. Location 123_8 in PAGE 23_8, CURRENT PAGE, will be:

10 011 1 010 011 = 100 111 010 011 = 4723_8
- 1 010 011 — PAGE ADDRESS 123_8
- 10 011 — PAGE NUMBER 23_8

By this method, 256 locations may be directly addressed, 128 on PAGE 0 and 128 on the CURRENT PAGE. Other locations are addressed indirectly by setting bit 3. An INDIRECT ADDRESS (pointer address) identifies the location that contains the desired address (effective address). To address a location that is not directly addressable, not in PAGE 0 or in the CURRENT PAGE, the absolute address of the desired location is stored in one of the 256 directly addressable locations (pointer address). Upon execution, the MRI will operate on the contents of the location identified by the address contained in the pointer location.

It should be noted that locations 0010_8-0017_8 in PAGE 0 are AUTOINDEXED. If these locations are addressed indirectly, the contents are incremented by 1 and restored before they are used as the operand address. These locations may, therefore, be used for indexing applications.

Table II lists the mnemonics for the six memory reference instructions, their OPCODEs, the operations they perform and the number of states required for execution.

It should be noted that the data is represented in Two's Complement Integer notation. In this system, the negative of a number is formed by complementing each bit in the data word and adding "1" to the complemented number. The sign is indicated by the most significant bit. In the 12-bit word used by the IM6100, when bit 0 is a "0", it denotes a positive number and when bit 0 is a "1", it denotes a negative number. The maximum single precision number ranges for this system are 3777_8 (+2047) and 4000_8 (−2048).

Table II

MNEMONIC	OP CODE	IA	STATES	OPERATION
AND EA	0_8	0	10	LOGICAL AND DIRECT Operation: (AC)←(AC) ∧ (EA) Description: Contents of the EA are logically AND'ed with the contents of the AC and the result is stored in AC.
AND I PA		1	15	LOGICAL AND INDIRECT (PA ≠ 0010-0017_8) Operation: (AC)←(AC) ∧ ((PA))
AND PAIX		1	16	LOGICAL AND AUTOINDEX (PAIX = 0010-0017_8) Operation: (PA)←(PA) + 1; (AC)←(AC) ∧ ((PA))
TAD EA	1_8	0	10	BINARY ADD DIRECT Operation (AC)←(AC) + (EA) Description: Contents of the EA are ADD'ed with the contents of the AC and the result is stored in the AC, carry out complements the LINK. If AC is initially cleared, this instruction acts as LOAD from Memory.
TAD I PA		1	15	BINARY ADD INDIRECT (PA ≠ 0010-0017_8) Operation (AC)←(AC) + ((PA))
TAD I PAIX		1	16	BINARY ADD AUTOINDEX (PAIX = 0010-0017_8) Operation (PA)←(PA) + 1, (AC)←(AC) + ((PA))
ISZ EA	2_8	0	16	INCREMENT AND SKIP IF ZERO DIRECT Operation: (EA)←(EA) + 1, if (EA) = 0000_8, PC←PC + 1 Description: Contents of the EA are incremented by 1 and restored. If the result is zero, the next sequential instruction is skipped.
ISZ I PA		1	21	INCREMENT AND SKIP IF ZERO INDIRECT (PA ≠ 0010-0017_8) Operation: ((PA))←((PA)) + 1, if ((PA)) = 0000_8, PC←PC + 1
ISZ I PAIX		1	22	INCREMENT AND SKIP IF ZERO AUTOINDEX (PAIX = 0010-0017_8) Operation (PA)←(PA) + 1; ((PA))←((PA)) + 1; if ((PA)) = 0000_8, PC←PC + 1
DCA EA	3_8	0	11	DEPOSIT AND CLEAR THE ACCUMULATOR DIRECT Operation (EA)←(AC), (AC)←0000_8 Description: The contents of the AC are stored in EA and the AC is cleared.
DCA I PA		1	16	DEPOSIT AND CLEAR THE ACCUMULATOR INDIRECT (PA ≠ 0010-0017_8) Operation ((PA))←(AC), (AC)←0000_8
DCA I PAIX		1	17	DEPOSIT AND CLEAR THE ACCUMULATOR AUTOINDEX (PAIX = 0010-0017_8) Operation (PA)←(PA) + 1, ((PA))←(AC), (AC)←0000_8
JMS EA	4_8	0	11	JUMP TO SUBROUTINE DIRECT Operation: (EA)←(PC), (PC)←EA + 1 Description: The contents of the PC are stored in the EA. The PC is incremented by 1 immediately after every instruction fetch. The contents of the EA now point to the next sequential instruction following the JMS (return address). The next instruction is taken from EA + 1
JMS I PA		1	16	JUMP TO SUBROUTINE INDIRECT (PA ≠ 0010-0017_8) Operation ((PA))←PC, (PC)←(PA) + 1
JMS I PAIX		1	17	JUMP TO SUBROUTINE AUTOINDEX (PAIX = 0010-0017_8) Operation (PA)←(PA) + 1, ((PA))←PC, (PC)←(PA) + 1
JMP EA	5_8	0	10	JUMP DIRECT Operation (PC)←EA Description: The next instruction is taken from the EA.
JMP I PA		1	15	JUMP INDIRECT (PA ≠ 0010-0017_8) Operation (PC)←(PA)
JMP I PAIX		1	16	JUMP AUTOINDEX (PAIX = 0010-0017_8) Operation (PA) + 1, (PC)←(PA)

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INSTRUCTION SET (CONTINUED)

OPERATE INSTRUCTIONS

The Operate Instructions, which have an OPCODE of 7_8 (111), consist of 3 groups of microinstructions. Group 1, which is identified by the presence of the 0 in bit 3, is used to perform logical operations on the contents of the accumulator and link. Group 2, which is identified by the presence of a 1 in bit 3 and a 0 in bit 11, is used primarily to test the contents of the Accumulator and/or Link and then conditionally skip the next sequential instruction. Group 3 has a 1 in bit 3 and a 1 in bit 11 and performs logical operations on the contents of the AC and MQ.

The basic OPR instruction format is shown in Figure 4.

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	A								B

MICROINSTRUCTION	A	B
GROUP 1	0	0/1
GROUP 2	1	0
GROUP 3	1	1

Figure 4: Basic OPR Instruction Format

Operate microinstructions from any group may be microprogrammed with other operate microinstructions of the same group providing the instruction codes do not conflict. The actual code for a microprogrammed combination of two, or more, microinstructions is the bitwise logical OR of the octal codes for the individual microinstructions. When more than one operation is microprogrammed into a single instruction, the operations are performed in a prescribed sequence, with logical sequence number 1 performed first, logical sequence number 2 performed second, logical sequence number 3 performed third and so on. Two operations with the same logical sequence number, within a given group of microinstructions, are performed simultaneously.

GROUP MICROINSTRUCTIONS

Figure 5 shows the instruction format of a group 1 microinstruction. Any one of bits 4 to 11 may be set, loaded with a binary 1, to indicate a specific group 1 microinstruction. If more than one of these bits is set, the instruction is a microprogrammed combination of group 1 microinstructions, which will be executed according to the logical sequence shown in Figure 5.

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	0	CLA	CLL	CMA	CML	RAR/RTR	RAL/RTL	0/1	IAC

BSW IF BITS 8 & 9 ARE 0 AND BIT 10 IS 1.

LOGICAL SEQUENCES:
1—CLA, CLL
2—CMA, CML
3—IAC
4—RAR, RAL, RTR, RTL, BSW

Figure 5: Group 1 Microinstruction Format

Table III lists commonly used group 1 microinstructions, their assigned mnemonics, octal code, logical sequence, the number of states, and the operation they perform. The same format is followed in Table IV and V which lists group 2 and 3 microinstructions, respectively.

Table III: Group 1 Operate Microinstructions

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
NOP	7000	1	10	NO OPERATION—This instruction causes a 10 state delay in program execution, without affecting the state of the IM6100. It may be used for timing synchronization or as a convenient means of deleting an instruction from a program.
IAC	7001	3	10	INCREMENT ACCUMULATOR—The content of the AC is incremented by one (1) and carry out complements the Link (L).
RAL	7004	4	15	ROTATE ACCUMULATOR LEFT—The contents of the AC and L are rotated one binary position to the left. AC (0) is shifted to L and L is shifted to AC (11).
RTL	7006	4	15	ROTATE TWO LEFT—The contents of the AC and L are rotated two binary positions to the left. AC (1) is shifted to L and L is shifted to AC (10).
RAR	7010	4	15	ROTATE ACCUMULATOR RIGHT—The content of the AC and L are rotated one binary position to the right. AC (11) is shifted to L and L is shifted to AC (0).
RTR	7012	4	15	ROTATE TWO RIGHT—The contents of the AC and L are rotated two binary positions to the right. AC (10) is shifted to L and L is shifted to AC (1).
BSW	7002	4	15	BYTE SWAP—The right six (6) bits of the AC are exchanged or SWAPPED with the left six bits. AC (0) is swapped with AC (6), AC (1) with AC (7), etc. L is not affected.
CML	7020	2	10	COMPLEMENT LINK—The content of the link is complemented.
CMA	7040	2	10	COMPLEMENT ACCUMULATOR—The content of each bit of the AC is complemented having the effect of replacing the content of the AC with its one's complement.
CIA	7041	2,3	10	COMPLEMENT AND INCREMENT ACCUMULATOR—The content of the AC is replaced with its two's complement. Carry out complements the LINK.
CLL	7100	1	10	CLEAR LINK—The link is loaded with a binary 0.
CLL RAL	7104	1,4	15	CLEAR LINK—ROTATE ACCUMULATOR LEFT.
CLL RTL	7106	1,4	15	CLEAR LINK—ROTATE TWO LEFT.
CLL RAR	7110	1,4	15	CLEAR LINK—ROTATE ACCUMULATOR RIGHT.
CLL RTR	7112	1,4	15	CLEAR LINK—ROTATE TWO RIGHT.
STL	7120	1,2	10	SET THE LINK—The LINK is loaded with a binary 1 corresponding with a microprogrammed combination of CLL and CML.
CLA	7200	1	10	CLEAR ACCUMULATOR—The accumulator is loaded with binary 0's.
CLA IAC	7201	1,3	10	CLEAR ACCUMULATOR—INCREMENT ACCUMULATOR.
GLT	7204	1,4	15	GET THE LINK—The AC is cleared; the content of L is shifted into AC (11), a 0 is shifted into L. This is a microprogrammed combination of CLA and RAL.
CLA CLL	7300	1	10	CLEAR ACCUMULATOR—CLEAR LINK.
STA	7240	1,2	10	SET THE ACCUMULATOR—Each bit of the AC is set to 1 corresponding to a microprogrammed combination of CLA and CMA.

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INSTRUCTION SET (CONTINUED)

GROUP 2 MICROINSTRUCTIONS

Figure 6 shows the instruction format of group 2 microinstructions. Bits 4-10 may be set to indicate a specific group 2 microinstruction. If more than one of bits 4-7 or 9-10 is set, the instruction is a microprogrammed combination of group 2 microinstructions, which will be executed according to the logical sequence shown in Figure 6.

Skip microinstructions may be microprogrammed with CLA, OSR, or HLT microinstructions. When two or more skip microinstructions are microprogrammed into a single instruction, the resulting condition on which the decision will be based is the logical OR of the individual conditions when bit 8 is 0, or, when bit 8 is 1, the decision will be based on the logical AND.

By combining skip instructions properly, all possible relational conditions can be tested (i.e., =, ≠, <, ≤, >, ≥). Skip microinstructions which have a 0 in bits 5, 6, 7, or 8 may not be microprogrammed with skip microinstructions which have a 1 in those same bits.

0	1	2	3	4	5	6	7	8	9	10	11
1	1	1	1	CLA	SMA / SPA	SZA / SNA	SNL / SZL	0 / 1	OSR	HLT	0

LOGICAL SEQUENCES:
1 (BIT 8 IS ZERO)—SMA OR SZA OR SNL
(BIT 8 IS ONE) —SPA AND SNA AND SZL
2 —CLA
3 —OSR, HLT

Figure 6: Group 2 Microinstruction Format

Table IV: Group 2 Operate Microinstructions

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
NOP	7400	1	10	NO OPERATION—See Group 1 MICROINSTRUCTIONS
HLT	7402	3	10	HALT—Program stops at the conclusion of the current machine cycle. If HLT is combined with others in OPR 2, the other operations are completed before the end of the cycle.
OSR	7404	3	15	OR WITH SWITCH REGISTER—The content of the Switch Register if OR'ed with the content of the AC and the result is stored in the AC. The OSR INSTRUCTION TIMING is shown in Figure 7. The IM6100 sequences the OSR instruction through a 2-cycle execute phase referred to as OPR 2A and OPR 2B.
SKP	7410	1	10	SKIP—The content of the PC is incremented by 1, to skip the next sequential instruction.
SNL	7420	1	10	SKIP ON NON-ZERO LINK—The content of L is sampled, the next sequential instruction is skipped if L contains a 1. If L contains a 0, the next instruction is executed.
SZL	7430	1	10	SKIP ON ZERO LINK—The content of L is sampled, the next sequential instruction is skipped if L contains a 0. If the L contains a 1, the next instruction is executed.
SZA	7440	1	10	SKIP ON ZERO ACCUMULATOR—The content of the AC is sampled; the next sequential instruction is skipped if the AC has all bits which are 0. If any bit in the AC is a 1, the next instruction is executed.
SNA	7450	1	10	SKIP ON NON-ZERO ACCUMULATOR—The content of the AC is sampled; the next sequential instruction is skipped if the AC has any bits which are not 0. If every bit in the AC is 0, the next instruction is executed.
SZA SNL	7460	1	10	SKIP ON ZERO ACCUMULATOR, OR SKIP ON NON-ZERO LINK, OR BOTH
SNA SZL	7470	1	10	SKIP ON NON-ZERO ACCUMULATOR AND SKIP ON ZERO LINK
SMA	7500	1	10	SKIP ON MINUS ACCUMULATOR—If the content of AC (0) contains a 1, indicating that the AC contains a negative two's complement number, the next sequential instruction is skipped. If AC (0) contains a 0, the next instruction is executed.
SPA	7510	1	10	SKIP ON POSITIVE ACCUMULATOR—The contents of AC (0) are sampled. If AC (0) contains a 0, indicating that the AC contains a positive two's complement number, the next sequential instruction is skipped. If AC (0) contains a 1, the next instruction is executed.
SMA SNL	7520	1	10	SKIP ON MINUS ACCUMULATOR OR SKIP ON NON-ZERO LINK OR BOTH
SPA SZL	7530	1	10	SKIP ON POSITIVE ACCUMULATOR AND SKIP ON ZERO LINK
SMA SZA	7540	1	10	SKIP ON MINUS ACCUMULATOR OR SKIP ON ZERO ACCUMULATOR OR BOTH
SPA SNA	7550	1	10	SKIP ON POSITIVE ACCUMULATOR AND SKIP ON NON-ZERO ACCUMULATOR
SMA SZA SNL	7560	1	10	SKIP ON MINUS ACCUMULATOR OR SKIP ON ZERO ACCUMULATOR OR SKIP ON NON-ZERO LINK OR ALL
SPA SNA SZL	7570	1	10	SKIP ON POSITIVE ACCUMULATOR AND SKIP ON NON-ZERO ACCUMULATOR AND SKIP ON ZERO LINK
CLA	7600	2	10	CLEAR ACCUMULATOR—The AC is loaded with binary 0's.
LAS	7604	1,3	15	LOAD ACCUMULATOR WITH SWITCH REGISTER—The content of the AC is loaded with the content of the SR, bit for bit. This is equivalent to a microprogrammed combination of CLA and OSR.
SZA CLA	7640	1,2	10	SKIP ON ZERO ACCUMULATOR THEN CLEAR ACCUMULATOR
SNA CLA	7650	1,2	10	SKIP ON NON-ZERO ACCUMULATOR THEN CLEAR ACCUMULATOR
SMA CLA	7700	1,2	10	SKIP ON MINUS ACCUMULATOR THEN CLEAR ACCUMULATOR
SPA CLA	7710	1,2	10	SKIP ON POSITIVE ACCUMULATOR THEN CLEAR ACCUMULATOR

INSTRUCTION SET (CONTINUED)

(1) INSTRUCTION ADDRESS (2) INSTRUCTION→CPU (3) SWITCH REGISTER,→CPU DATA

Figure 7: OSR Instruction Timing

GROUP 3 MICROINSTRUCTIONS

Figure 8 shows the instruction format of group 3 microinstructions which requires bits 3 and 11 to contain a 1. Bits 4, 5 or 7 may be set to indicate a specific group 3 microinstruction. If more than one of the bits is set, the instruction is a microprogrammed combination of group 3 microinstructions following the logical sequence listed in Figure 8. All unused bits are "don't care".

*DON'T CARE

LOGICAL SEQUENCES:
1—CLA
2—MQA, MQL
3—ALL OTHERS

Figure 8: Group 3 Microinstruction Format

Table V: Group 3 Operate Microinstructions

MNEMONIC	OCTAL CODE	LOGICAL SEQUENCE	NUMBER OF STATES	OPERATION
NOP	7401	3	10	NO OPERATION—See Group 1 Microinstructions
MQL	7421	2	10	MQ REGISTER LOAD—The content of the AC is loaded into the MQ, the AC is cleared and the original content of the MQ is lost.
MQA	7501	2	10	MQ REGISTER INTO ACCUMULATOR—The content of the MQ is OR'ed with the content of the AC and the result is loaded into the AC. The original content of the AC is lost but the original content of the MQ is retained. This instruction provides the programmer with an inclusive OR operation.
SWP	7521	3	10	SWAP ACCUMULATOR AND MQ REGISTER—The content of the AC and MQ are interchanged accomplishing a microprogrammed combination of MQA and MQL.
CLA	7601	1	10	CLEAR ACCUMULATOR
CAM	7621	3	10	CLEAR ACCUMULATOR AND MQ REGISTER—The content of the AC and MQ are loaded with binary 0's. This is equivalent to a microprogrammed combination of CLA and MQL.
ACL	7701	3	10	CLEAR ACCUMULATOR AND LOAD MQ REGISTER INTO ACCUMULATOR—This is equivalent to a microprogrammed combination of CLA and MQA.
CLA SWP	7721	3	10	CLEAR ACCUMULATOR AND SWAP ACCUMULATOR AND MQ REGISTER—The content of the AC is cleared. The content of the MQ is loaded into the AC and the MQ is cleared.

INSTRUCTION SET (CONTINUED)

INPUT/OUTPUT (IOT) INSTRUCTIONS

The input/output transfer instructions, which have an OP-CODE of 6_8 are used to control the operation of peripheral devices and to transfer data between peripherals and the IM6100. Three types of data transfer may be used to receive or transmit information between the IM6100 and one or more peripheral I/O devices: PROGRAMMED DATA TRANSFER, which provides a straightforward means of communicating with relatively slow I/O devices, such as Teletypes, cassettes, card readers and CRT displays, INTERRUPT TRANSFERS which use the interrupt system to service several peripheral devices simultaneously, and DIRECT MEMORY ACCESS, DMA, which transfers variable-size blocks of data between high-speed peripherals and memory without IM6100 intervention.

IOT INSTRUCTION FORMAT

The Input/Output Transfer Instruction format is represented in Figure 9. The instruction executes in 17 states.

The first three bits, 0-2, are always set to 6_8 (110) to specify an IOT instruction. The low order nine bits are used for device selection and control. PDP-8/e compatible interfaces use bits 3-8 for device selection and bits 9-11 for control of the selected device. The IM6101 PIE interface uses bits 3-7 for device selection and bits 8-11 for control. In user designed systems, the 512 possible IOT instructions may be alloted according to the user's needs. The nature of this operation for any given IOT instruction depends entirely upon the circuitry designed into the I/O device interface.

PROGRAMMED DATA TRANSFER

Programmed Data Transfer is the easiest, simplest, most convenient and most common means of performing data I/O. For microprocessor applications, it may also be the most cost effective approach. The data transfer begins when the IM6100 fetches an instruction from the memory and recognizes that the current instruction is an IOT (Figure 10). This is referred to as IFETCH and consists of five (5) internal states. The IM6100 sequences the IOT instruction through a 2-cycle execute phase referred to as IOT_A and IOT_B. Bits 0-11 of the IOT instructions are available on DX0-11 at $IOT_A \bullet$ LXMAR; these bits must be latched in an external address register. DEVSEL is active low to enable data transfers between the IM6100 and the peripheral device(s). The selected peripheral device communicates with the IM6100 through 4 control lines - C_0, C_1, C_2 and SKP. In the IM6100 the type of data transfer, during an IOT instruction, is specified by the peripheral device(s) by asserting the control lines as shown in Table VI.

The control line SKP, when low during an IOT, causes the IM6100 to skip the next sequential instruction. This feature is used to sense the status of various signals in the device interface. The C_0, C_1, and C_2 lines are treated independently of the SKP line. In the case of a RELATIVE or ABSOLUTE JUMP, the skip operation is performed after the jump. The input signals to the IM6100, DX 0-11, C_0, C_1, C_2, and SKP, are sampled at IOT_A during DEVSEL $\bullet$ XT_C and the data from the IM6100 is available to the device(s) during that time. IOT_B is used by the IM6100 to perform the operations requested during IOT_A. Both IOT_A and IOT_B consist of six (6) internal states.

In summary, Programmed Data Transfer performs data I/O with a minimum of hardware support. The maximum rate at which programmed data transfers may take place is limited by the IM6100 instruction execution rate, however, the data rate of the most commonly used peripheral devices is much lower than the maximum rate at which programmed transfers can take place in the IM6100. The major drawback associated with Programmed Data Transfer is the IM6100 must hang up in a waiting loop while the I/O device completes the last transfer and prepares for the next transfer. On the other hand, this technique permits easy hardware implementation and simple, economical interface design. For this reason, almost all devices except mass storage units rely on programmed data transfer.

Figure 9: IOT Instruction Format

Figure 10: Input-Output Instruction Timing

INSTRUCTION SET (CONTINUED)

Table VI: Programmed I/O Control Lines

CONTROL LINES C_0	C_1	C_2	OPERATION	DESCRIPTION
H	H	H	DEV ←AC	The content of the AC is sent to the device.
L	H	H	DEV ←AC; CLA	The content of the AC is sent to a device and then the AC is cleared.
H	L	H	AC ←AC V DEV	Data is received from a device, OR'ed with the data in the AC and the result is stored in the AC.
L	L	H	AC←DEV	Data is received from a device and loaded into the AC.
*	H	L	PC←PC + DEV	Data from the device is added to the contents of the PC. This is referred to as a RELATIVE JUMP.
*	L	L	PC ←DEV	Data is received from a device and loaded into the PC. This is referred to as an ABSOLUTE JUMP.

*Don't Care

INTERRUPT TRANSFER

PROGRAM INTERRUPT TRANSFERS

The program interrupt system may be used to initiate programmed data transfers in such a way that the time spent waiting for device I/O is greatly reduced or eliminated altogether. This is accomplished by isolating the I/O handling routines from the mainline program and using the interrupt system to ensure that these routines are entered only when an I/O device status is set, indicating that the device is actually ready to perform a data transfer.

The interrupt system allows certain external conditions to interrupt the computer program by driving the INTREQ input Low. If no higher priority requests are outstanding and the interrupt system is enabled, the IM6100 grants the device interrupt at the end of the current instruction. After an interrupt has been granted, the Interrupt Enable Flip-Flop in the IM6100 is reset so that no more interrupts are acknowledged until the interrupt system is re-enabled under program control.

DEVICE INTERRUPT GRANT TIMING

The current contents of the Program Counter, PC, are deposited in location 0000_8 of the memory and the program fetches the instruction from location 0001_8. The return address is available in location 0000_8. This address must be saved in a software stack, before the interrupts are re-enabled, if nested interrupts are permitted. The INTGNT signal, Figure 11, is activated by the IM6100 when a device interrupt is acknowledged; this signal is reset by executing any IOT instruction as shown in Figure 12. The INTGNT signal is necessary to implement an External Vectored Priority Interrupt network. The IM6101 PIE contains the logic necessary to implement both vectored and non-vectored interrupts.

The user program controls the interrupt mechanism of the IM6100 by executing the processor IOT instructions listed in Table VII. Several of these interrupt IOT instructions are also used if the memory is extended beyond 4K words to save and restore extended memory status during interrupt servicing.

Figure 11: Device Interrupt Grant Timing

Figure 12: Device Interrupt Grant Reset Timing

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INSTRUCTION SET (CONTINUED)

Table VII: Processor IOT Instructions

MNE-MONIC	OCTAL CODE	OPERATION
SKON	6000	SKIP IF INTERRUPT ON — If interrupt system is enabled, the next sequential instruction is skipped. The Interrupt system is disabled.
ION	6001	INTERRUPT TURN ON — The internal interrupt acknowledge system is enabled. The interrupt system is enabled after the CPU executes the next sequential instruction. The INTERRUPT ENABLE TIMING is shown in Figure 13.
IOF	6002	INTERRUPT TURN OFF — The interrupt system is disabled. Note that the interrupt system is automatically disabled when the CPU acknowledges an INT request.
SRQ	6003	SKIP IF INT REQUEST — The next sequential instruction is skipped if the INT request bus is low.
GTF	6004	GET FLAGS — The following machine states are read into the indicated bits of AC. bit 0 — Link bit 2 — INT request bus bit 4 — Interrupt Enable FF Other bits may be modified by external devices by controlling the C-lines, (ex. Extended memory control).
RTF	6005	RETURN FLAGS — Link is restored from AC (0). Interrupt system is enabled after the next sequential instruction is executed. All AC bits are available externally to restore external states. (ex. Extended memory control).
SGT	6006	Operation is determined by external devices, if any.
CAF	6007	CLEAR ALL FLAGS — AC and Link are cleared. Interrupt system is disabled.

① INSTRUCTION ADDRESS
② INSTRUCTION FETCH
③ DEVICE ADDRESS (6001_8)
④ DON'T CARE DEV READ, SAMPLE C0, C1, C2 & SKP
⑤ DON'T CARE DEV WRITE
⑥ INSTRUCTION ADDRESS
⑦ INSTRUCTION FETCH
⑧ SAMPLE REQUEST LINES

Figure 13: Interrupt Enable FF ON (ION)

CONTROL PANEL INTERRUPT TRANSFER

The IM6100 supports a memory space completely separate from main memory, called control panel memory. Therefore, the IM6100 control panel and other supervisory functions are implemented in software. This implementation need not use any part of the main memory or change the processor state. This is an important feature, since the final version of the system may not have a control panel and the system designer would like to use the entire capacity of the main memory for the specific system application.

The control panel communicates with the IM6100 with the Control Panel Request, CPREQ, line. The CPREQ is functionally similar to the INTREQ with some important differences. The CPREQ is granted even when the machine is in the HALT state; the IM6100 is temporarily put in the RUN state for the duration of the panel routine. The IM6100 reverts to its original processor state after the panel routine has been executed.

The CPREQ does not affect the interrupt enable system, and the processor IOT instruction, ION is redefined and IOF is ignored while the IM6100 is in the Control Panel Mode. Once a CPREQ is granted, the IM6100 will not recognize any DMAREQ or INTREQ until CPREQ has been fully serviced.

When a CPREQ is granted, the PC is stored in location 0000_8 of the Panel Memory and the IM6100 resumes operation at location 7777_8. The Panel Memory would be organized with RAM's in the lower pages and PROM's in the higher pages. The control panel service routine would be stored in the higher pages in the nonvolatile PROM's, starting at 7777_8.

① ADDRESS 0000_8
② DON'T CARE READ
③ PC WRITTEN IN LOC 0000_8 OF CP MEM
④ ADDRESS 7777_8
⑤ INSTRUCTION FETCHED FROM LOC 7777_8 OF CP MEM
⑥ IF CPU IS HALTED, THE RUN IS TRUE AT T1 OF CPINT

Figure 14: Control Panel Interrupt Grant Timing

INSTRUCTION SET (CONTINUED)

A Control Panel Flip-Flop, CNTRL FF, internal to the IM6100, is set when the CPREQ is granted. The CNTRL FF prevents further CPREQ's from being granted.

When the CNTRL FF is set, the Control Panel Memory Select, CPSEL, is active rather than the Memory Select, MEMSEL, for memory references. The CPSEL signal may therefore be used to distinguish the Control Panel Memory from the Main Memory. However, during the Execute phase of indirectly addressed AND, TAD, ISZ or DCA instructions, the MEMSEL is made active. The instructions are always fetched from the control panel memory, and the operand address for indirectly address AND, TAD, ISZ or DCA refers first to the control panel memory for an effective address, which, in turn, refers to a location in the main memory. A main memory location may therefore be examined and changed by indirectly addressed TAD and DCA instructions, Figure 15, respectively. Every location in the main memory is accessible to the control panel routine.

Exiting from the control panel routine is achieved by executing the following sequence with reference made to Figure 16.

ION

JMP I 0000_8 (Loc 0000_8 in CPMEM)

The ION, 6001_8, instruction will reset the CP FF after executing the next sequential instruction, but will not affect the interrupt system since the CNTRL FF is still active. Location 0000_8 of the CPMEM contains either the original return address, deposited by the IM6100 when the CP routine was entered, or a new starting address defined by the CP routine, for example, by activating the LOAD ADDRESS SWITCH. CPREQ's are normally generated by the manual actuation of the control switches. If the CPU registers must be displayed in real-time, the CPREQ's must be generated by a timer at fixed intervals.

The designer may also make use of the control panel features to implement Bootstrap loaders in the CP Memory so that the loader will be "transparent" to the main memory. Programs will be loaded by DCA I POINTER instruction, the pointer being developed in the CP RAM to point to the main memory location to be loaded.

Approximately 64 P/ROM locations are sufficient to implement all the functions of the PDP®-8/e Control Panel. The IM6100 provides for a 12-bit switch register which can be read by the IM6100 under program control with the SWITCH REGISTER, OSR, instruction even without a control panel.

An RTF, 6005_8, instruction also resets the internal CNTRL FF. Exiting from a panel routine can be achieved by activating the RESET line since RESET has a higher priority than CPREQ, see Figure 18. If the RUN/HLT line is pulsed while the IM6100 is in the panel mode, it will 'remember' the pulses(s) but defer any action until the IM6100 exits from the panel mode.

① INSTRUCTION ADDRESS
② INSTRUCTION FROM CP MEMORY
③ EFFECTIVE ADDRESS
④ OPERAND ADDRESS FROM CP MEMORY
⑤ OPERAND ADDRESS
⑥ DON'T CARE MAIN MEM READ
⑦ AC WRITTEN INTO MAIN MEMORY

Figure 15: "DCA Indirect" In Control Panel Routine

① INSTRUCTION ADDRESS
② INSTRUCTION FETCH FROM CP MEM
③ DEVICE ADDRESS (6001_8)
④ DON'T CARE DEVICE READ, SAMPLE C0, C1, C2 & SKP
⑤ DON'T CARE DEVICE WRITE
⑥ INSTRUCTION ADDRESS
⑦ INSTRUCTION FETCH FROM CP MEM
⑧ EFFECTIVE ADDRESS (0000_8)
⑨ JMP ADDRESS FROM CP MEM LOC 0000_8
⑩ IF CPU WAS IN THE HALT STATE, THE RUN IS FALSE AT T1

Figure 16: "ION; JMP I 0000_8" In Control Panel Routine

7

DIRECT MEMORY ACCESS (DMA)

Direct Memory Access, sometimes called data break, is the preferred form of data transfer for use with high-speed storage devices such as magnetic disk or tape units. The DMA mechanism transfers data directly between memory and peripheral devices, and the IM6100 is involved only in setting up the transfer; the transfers take place on a "cycle stealing" basis. The DMA transfer rate is limited only by the bandwidth of the memory and the data transfer characteristics of the device.

The device generates a DMA Request when it is ready to transfer data. The IM6100 grants the DMAREQ by activating the DMAGNT signal at the end of the current instruction as shown in Figure 17. The IM6100 suspends any further instruction fetches until the DMAREQ line is released. The DX lines are tri-stated, all SEL lines are high, and the external timing signals XT_A, XT_B, and XT_C are active and LXMAR remains low. The device which generated the DMAREQ must provide the address and the necessary control signals to the memory for data transfers. The DMAREQ line can also be used as a level sensitive "pause" line.

DMA may also be implemented in a transparent mode without stealing processor cycles by using the DX bus during idle periods. The IM6102 MEDIC operates in this manner.

① DMAREQ REMOVED AFTER DMAGNT

Figure 17: Direct Memory Access (DMA)

INTERNAL PRIORITY STRUCTURE

After an instruction is completely sequenced, the major state generator scans the internal priority network as shown in Figure 18. The state of the priority network decides the next sequence of the IM6100.

The request lines, RESET, CPREQ, RUN/HLT, DMAREQ and INTREQ, are sampled in the last cycle of an instruction execution, at time T1. The worst case response time of the IM6100 to an external request is, therefore, the time required to execute the longest instruction preceded by any 6-state execution cycle. For the IM6100, this is an autoindexed ISZ, 22 states, preceded by any 6-state execution cycle instruction.

When the IM6100 is initially powered up, the state of the timing generator is undefined. The generator is automatically initialized with a maximum of 34 clock pulses. The request inputs, as the IM6100 is powered on, must span at least 58 clock pulses to be recognized, 34 clocks for the counter to initialize and a maximum of two IM6100 cycles (20 to 24 clocks) for the state generator to sample the request lines. A positive transition on RUN/HALT should occur at least 10 clock pulses after RESET for it to be recognized.

The internal priority is RESET, CPREQ, RUN/HLT, DMAREQ, INTREQ, and IFETCH.

IFETCH

If no external requests are pending, the IM6100 fetches the next instruction pointed to by the contents of the PC. The IFETCH line is active during the cycle in which the instruction is fetched. External devices can monitor DX, 0-2, during IFETCH-XT_A to determine the functional class of the current instruction. For example, the external memory extension hardware must know when JMP or JMS instructions are fetched to implement the Extended Memory Control. The IM6102 does this to implement extended memory addressing.

The Programmable Logic Array, PLA, in the IM6100 sequences the IM6100 to execute the fetched instruction. All INDIRECT and AUTOINDEX Memory Reference Instructions go through a common state sequence to generate the Effective Address, EA, of the operand. The subsequent sequence, referred to as the EXECUTE phase, is controlled by the functional class of the instruction. The EXECUTE phase of AND, TAD, DCA, JMS, JMP and OPR Group 3 Microinstructions consists of only one cycle. ISZ and IOT have a 2-cycle EXECUTE phase. OPR Group 1 and Group 2 Microinstructions have an optional second cycle, depending on the microcoding of the OPR instructions. An IM6100 cycle consists of 5 states, T_1, T_2, T_3, T_4 and T_5, with an optional sixth state, T_6, for Output Transfers (WRITE).

The state sequence for internal (processor) and external IOT instructions are identical. The Device Address and Control bits are available in the External Address Register for internal IOT instructions. External hardware, for example Extended Memory Control, can control the C-lines for data transfers to implement Get Flags (GTF), Return Flags (RTF), and Clear All Flags (CAF) instructions. External Control of the C-lines is necessary to implement these internal IOT instructions since the flag bits may be distributed both inside and outside the IM6100.

Figure 18: Major Processor States and Number of Clock Cycles in Each State

RESET

The Reset initializes all internal IM6100 flags and clears the AC and the LINK. The machine is halted.

As long as the RESET line is low, the IM6100 remains in the reset state and the DX lines are three stated. The IM6100 continues to provide the external timing signals XT_A, XT_B and XT_C, all SEL lines are high, and the PC is set to 7777_8. In most applications, the higher memory locations utilize P/ROM's or ROM's. Therefore, a power-up routine starting at the highest memory location can be used to initialize the system. It is also possible to force entry into control panel memory on power-up.

① REQUESTS SAMPLED AT T1 OF THE FINAL EXECUTE PHASE
② EXECUTE MAY BE 5/6 STATES
③ PC IS SET TO 7777_8
④ CPU HALTS

Figure 19: Reset Timing

RUN/HALT

RUN/HLT changes the state of the IM6100's RUN/HLT flip-flop. Pulsing the line low causes the IM6100 to alternately run and halt. The RUN/HLT line is normally high. The IM6100 recognizes the positive transition of the signal.

The RUN/HLT flip-flop can be put in the halt state under program control by executing the HLT, 7402_8, instruction. When the IM6100 is halted, RUN/HLT is functionally identical to the CONTINUE switch of the PDP-8/e control panel and the RUN signal is low. The RUN signal can be used to power down external circuitry for a low power system.

The RUN/HLT can also be used to make the IM6100 execute one instruction at a time as shown in Figure 21. The RUN/HLT combines the functional features of STOP, CONTINUE, and SINGLE INSTRUCTION as defined by the PDP-8/e Control Panel.

Figure 20: Run/Halt Timing

① RUN/HLT PULSE FOR "SINGLE STEP"
② DMAGNT ON FOR 1 CYCLE FOR HALT TO RUN TRANSITION
③ TRIGGER RUN/HLT WITH IFETCH
④ RUN FF SAMPLED IN THE LAST EXECUTE CYCLE

Figure 21: "Single Step" With Run/Hlt

WAIT

The IM6100 samples the WAIT line during input-output data transfers (Figure 22). The WAIT line, if low, controls the transfer duration. If WAIT is active during input transfers (READ), the CPU waits in the T2 state. For an output transfer (WRITE), WAIT controls the time for which the write data is maintained on the DX lines by extending the T6 state. The wait duration is an integral multiple of the oscillator time period — 250nsec at 4MHz.

The WAIT mechanism is an ideal way of providing for slower memory and peripheral devices in the system without significant degradation in system performance. For example, if one waits for all reads and writes for one delay unit (250nsec at 4MHz), the system throughput is reduced by less than 3%.

Figure 22: Wait Line Sampling Timing

Figure 23: Memory And Input Transfer Wait Circuit

The circuit shown in Figure 23 will make the IM6100 wait during main memory and device input (READ) transfers. MEMSEL or DEVSEL, being low, will assert WAIT low. When XTA becomes active high, the WAIT line is asserted high after a delay. The wait duration is controlled by the delay in the XTA-WAIT path (t_{L1}).

The following conditions must be satisfied to obtain x units of delay during READ's:

$$t_{SL(max)} + t_{L2(max)} + t_{WS} < T_S$$

$$t_{XT(min)} + t_{L1(min)} - t_{WH} \geq x \frac{T_S}{2}$$

$$t_{XT(max)} + t_{L1(max)} + t_{WS} < (x + 1) \frac{T_S}{2}$$

For example, for an IM6100 I device operating at 4MHz, 5.0V and 25°C, the constraints to be met to obtain 1 unit of delay (250nsec) are as follows:

$t_{L2(max)} < T_S - t_{SL(max)} - t_{WS}$

$< 500 - 300 - 30$

< 170nsec

$$t_{L1(min)} \geq \frac{T_S}{2} - t_{XT(min)} + t_{WH}$$

$\geq 250 - 100 + 30$

≥ 180nsec

$t_{L1(max)} < T_S - t_{XT(max)} - t_{WS}$

$< 500 - 250 - 30$

< 220nsec

Note that the delay circuit can be as simple as an R-C network in conjunction with CMOS logic. Note also that the WAIT can be made selective on main memory, device, control panel memory or switch register select line.

Figure 24: Write Transfer Wait Circuit

Figure 24 shows a logic implementation to wait during WRITE's only.

The rising edge of MEMSEL (or CPSEL or DEVSEL) during READ clocks in a zero on the WAIT line. XTB, after a delay, releases the WAIT line. Every WRITE pulse is preceded by a READ pulse, and if no write operation is performed in a cycle, the T6 state is not entered and the WAIT line is not sampled.

For x units of delay, the following conditions must be met:

$$t_{XT(min)} + t_{L3(min)} - t_{WH} \geq x \frac{T_S}{2} \text{ and}$$

$$t_{XT(max)} + t_{L3(max)} + t_{WS} < (x + 1) \frac{T_S}{2}$$

In the circuit shown in Figure 25, the WAIT signal is normally asserted low and it is released by XTA during READ's and XTB during WRITE's. Note that WAIT is active for all data transfers. Since XTA and XTB have identical timing relative to the WAIT sample point, the constraints to be satisfied are as follows:

$$t_{XT(min)} + t_{L4(min)} - t_{WH} \geq x \frac{T_S}{2} \text{ and}$$

$$t_{XT(max)} + t_{L4(max)} + t_{WS} < (x + 1) \frac{T_S}{2}$$

Figure 25: Data Transfer Wait Circuit

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IM6100

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6100 ..... −45°C to +85°C
Storage Temperature ..... −65°C to +150°C
Operating Voltage ..... +4.0V to +11.0V
Supply Voltage ..... +12.0V
Voltage On Any Input or
Output Pin ..... −0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ±10%, T_A = −40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}−2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	−1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = −0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OL}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}	−1.0		1.0	μA
7	I_{CC}	Power Supply Current-Standby	V_{IN} = GND or V_{CC}			800	μA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 2.5MHz			1.8	mA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS (See Figure 2 and 22)

TEST CONDITIONS: V_{CC} = 5.0V ±10%, C_L = 50pF, T_A −40°C to +85°C, f_C = 2.5MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	FREQ	Operating Frequency			2.5	MHz
2	t_S	Major State Time	800			ns
3	t_{LXMAR}	LXMAR Pulse Width	335			ns
4	t_{AS}	Address Setup Time : DX-LXMAR (↓)	120			ns
5	t_{AH}	Address Hold Time : LXMAR (↓)-DX	175			ns
8	t_{END}	Data Output Enable Time: DEVSEL (↓)-DX			575	ns
6	t_{AL}	Access Time from LXMAR			650	ns
7	t_{EN}	Output Enable Time (MEM, CP, DEVSEL)			400	ns
9	t_{WP}	Pulse Width (MEMSEL, CPSEL)	320			ns
10	t_{WPD}	Pulse Width (DEVSEL)	320			ns
11	t_{DS}	Data Setup Time (DX- ↑ MEMSEL/CPSEL)	240			ns
12	t_{DH}	Data Hold Time (↑ MEMSEL/CPSEL-DX)	175			ns
13	t_{DSD}	Data Setup Time (DX-↑ DEVSEL)	275			ns
14	t_{DHD}	Data Hold Time (↑ DEVSEL-DX)	175			ns
15	t_{SL}	Logic Delay to MEM/DEV/CP/SWSEL	75		440	ns
16	t_{XT}	Logic Delay to LXMAR, XTA, XTB, XTC	65		380	ns
17	t_{ST}	Logic Delay to DATAF, RUN, DMAGNT, INTGNT, LINK, IFETCH			475	ns
18	t_{RS}	Set up Time for CP/INT/DMAREQ	0			ns
19	t_{RH}	Hold Time for CP/INT/DMAREQ, RESET, RUN-HALT	300			ns
20	t_{RHP}	RUN-HALT Pulse Width	110			ns
21	t_{WS}	Set up Time for Wait	100			ns
22	t_{WH}	Hold Time for Wait	35			ns

Note: For capacitance greater than 50pF, the AC parameters will have a delay factor of 0.5ns/pF.

IM6100-1

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6100-1I ..... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Operating Voltage ..... +4.0V to +11.0V
Supply Voltage ..... +12.0V
Voltage On Any Input or
Output Pin ..... −0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ±10%, T_A = −40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC} −2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	−1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = −0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OL}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}	−1.0		1.0	μA
7	I_{CC}	Power Supply Current-Standby	V_{IN} = GND or V_{CC}			800	μA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 3.33MHz			2.0	mA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS (Ref. Fig. 2 and 22)

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, C_L = 50pF, T_A = −40°C to +85°C, f_C = 3.33MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	FREQ	Operating Frequency			3.33	MHz
2	t_S	Major State Time	600			ns
3	t_{LXMAR}	LXMAR Pulse Width	260			ns
4	t_{AS}	Address Setup Time: DX-LXMAR (↓)	85			ns
5	t_{AH}	Address Hold Time : LXMAR (↓)-DX	125			ns
8	t_{END}	Data Output Enable Time: DEVSEL (↓)-DX			470	ns
6	t_{AL}	Access Time from LXMAR			520	ns
7	t_{EN}	Output Enable Time (MEM, CP, DEVSEL)			300	ns
9	t_{WP}	Pulse Width (MEMSEL, CPSEL)	235			ns
10	t_{WPD}	Pulse Width (DEVSEL)	235			ns
11	t_{DS}	Data Setup Time (DX-↑ MEMSEL/CPSEL)	135			ns
12	t_{DH}	Data Hold Time (↑ MEMSEL/CPSEL-DX)	125			ns
13	t_{DSD}	Data Setup Time (DX-↑ DEVSEL)	225			ns
14	t_{DHD}	Data Hold Time (↑ DEVSEL-DX)	125			ns
15	t_{SL}	Logic Delay to MEM/DEV/CP/SWSEL	75		380	ns
16	t_{XT}	Logic Delay to LXMAR, XTA, XTB, XTC	65		270	ns
17	t_{ST}	Logic Delay to DATAF, RUN, DMAGNT, INTGNT, LINK, IFETCH			340	ns
18	t_{RS}	Set up Time for CP/INT/DMAREQ	0			ns
19	t_{RH}	Hold Time for CP/INT/DMAREQ, RESET, RUN-HALT	200			ns
20	t_{RHP}	RUN-HALT Pulse Width	80			ns
21	t_{WS}	Set up Time for Wait	100			ns
22	t_{WH}	Hold Time for Wait	20			ns

Note: For capacitance greater than 50pF, the AC parameters will have a delay factor of 0.5ns/pF.

IM6100A
ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6100AI ..... −40°C to +85°C
Storage Temperature ..... −65°C to +150°C
Operating Voltage ..... +4.0V to +11.0V
Supply Voltage ..... +12.0V
Voltage On Any Input or
Output Pin ..... −0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ±5%, T_A = −40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	−1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = 0.0mA	V_{CC} −0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0.0mA			GND +0.01	V
6	I_{OL}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}	−1.0		1.0	μA
7	I_{CC}	Power Supply Current-Standby	V_{IN} = GND or V_{CC}			900	μA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 5.71MHz			4.0	mA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS (Ref: Figures 2 and 22)

TEST CONDITIONS: V_{CC} = 10V ±5%, C_L = 50pF, T_A = −40°C to +85°C, f_C = 5.71MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	FREQ	Operating Frequency			5.71	MHz
2	t_S	Major State Time	350			ns
3	t_{LXMAR}	LXMAR Pulse Width	150			ns
4	t_{AS}	Address Setup Time : DX-LXMAR (↓)	55			ns
5	t_{AH}	Address Hold Time : LXMAR (↓)-DX	60			ns
8	t_{END}	Data Output Enable Time: DEVSEL (↓)-DX			250	ns
6	t_{AL}	Access Time from LXMAR			295	ns
7	t_{EN}	Output Enable Time (MEM, CP, DEVSEL)			185	ns
9	t_{WP}	Pulse Width (MEMSEL, CPSEL)	140			ns
10	t_{WPD}	Pulse Width (DEVSEL)	140			ns
11	t_{DS}	Data Setup Time (DX- ↑ MEMSEL/CPSEL)	115			ns
12	t_{DH}	Data Hold Time (↑ MEMSEL/CPSEL-DX)	60			ns
13	t_{DSD}	Data Setup Time (DX- ↑ DEVSEL)	110			ns
14	t_{DHD}	Data Hold Time (↑ DEVSEL-DX)	60			ns
15	t_{SL}	Logic Delay to MEM/DEV/CP/SWSEL	35		180	ns
16	t_{XT}	Logic Delay to LXMAR, XTA, XTB, XTC	35		155	ns
17	t_{ST}	Logic Delay to DATAF, RUN, DMAGNT, INTGNT, LINK, IFETCH			190	ns
18	t_{RS}	Set up Time for CP/INT/DMAREQ	0			ns
19	t_{RH}	Hold Time for CP/INT/DMAREQ, RESET, RUN-HALT	125			ns
20	t_{RHP}	RUN-HALT Pulse Width	45			ns
21	t_{WS}	Set up Time for Wait	45			ns
22	t_{WH}	Hold Time for Wait	15			ns

Note: For capacitance greater than 50pF, the AC parameters will have a delay factor of 0.5ns/pF.

IM6100-1M (Military)

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6100-1M ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Operating Voltage ..... +4.0V to +11.0V
Supply Voltage ..... +12.0V
Voltage On Any Input or
Output Pin ..... −0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = −55°C to +125°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC} −2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	−1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = −0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OL}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}	−1.0		1.0	μA
7	I_{CC}	Power Supply Current-Standby	V_{IN} = GND or V_{CC}			800	μA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 2.5MHz			2.0	mA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS (Ref. Fig. 2 and 22)

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, C_L = 50pF, T_A = −55°C to +125°C, f_C = 2.5MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	FREQ	Operating Frequency			2.5	MHz
2	t_S	Major State Time	800			ns
3	t_{LXMAR}	LXMAR Pulse Width	355			ns
4	t_{AS}	Address Setup Time : DX-LXMAR (↓)	200			ns
5	t_{AH}	Address Hold Time : LXMAR (↓)-DX	175			ns
8	t_{END}	Data Output Enable Time: DEVSEL (↓)-DX			655	ns
6	t_{AL}	Access Time from LXMAR			745	ns
7	t_{EN}	Output Enable Time (MEM, CP, DEVSEL)			470	ns
9	t_{WP}	Pulse Width (MEMSEL, CPSEL)	330			ns
10	t_{WPD}	Pulse Width (DEVSEL)	330			ns
11	t_{DS}	Data Setup Time (DX- ↑ MEMSEL/CPSEL)	250			ns
12	t_{DH}	Data Hold Time (↑ MEMSEL/CPSEL-DX)	170			ns
13	t_{DSD}	Data Setup Time (DX- ↑ DEVSEL)	350			ns
14	t_{DHD}	Data Hold Time (↑ DEVSEL-DX)	170			ns
15	t_{SL}	Logic Delay to MEM/DEV/CP/SWSEL	75		420	ns
16	t_{XT}	Logic Delay to LXMAR, XTA, XTB, XTC	65		300	ns
17	t_{ST}	Logic Delay to DATAF, RUN, DMAGNT, INTGNT, LINK, IFETCH			375	ns
18	t_{RS}	Set up Time for CP/INT/DMAREQ	0			ns
19	t_{RH}	Hold Time for CP/INT/DMAREQ, RESET, RUN-HALT	220			ns
20	t_{RHP}	RUN-HALT Pulse Width	90			ns
21	t_{WS}	Set up Time for Wait	110			ns
22	t_{WH}	Hold Time for Wait	20			ns

Note: For capacitance of greater than 50pF, the AC parameters all have delay factor of 0.5ns/pF.

IM6100AM (Military)

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6100AM ..... −55°C to +125°C
Storage Temperature ..... −65°C to +150°C
Operating Voltage ..... +4.0V to +11.0V
Supply Voltage ..... +12.0V
Voltage On Any Input or
Output Pin ..... −0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ±5%, T_A = −55°C to +125°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage	GND ≤ V_{IN} ≤ V_{CC}	−1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = 0.0mA	V_{CC} −0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0.0mA			GND +0.01	V
6	I_{OL}	Output Leakage	GND ≤ V_{OUT} ≤ V_{CC}	−1.0		1.0	μA
7	I_{CC}	Power Supply Current-Standby	V_{IN} = GND or V_{CC}			900	μA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 5.0MHz			4.0	mA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS (Ref.: Figures 2 and 22)

TEST CONDITIONS: V_{CC} = 10V ± 5%, C_L = 50pF, T_A = −55°C to +125°C, f_C = 5.0MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	FREQ	Operating Frequency			5.0	MHz
2	t_S	Major State Time	400			ns
3	t_{LXMAR}	LXMAR Pulse Width	170			ns
4	t_{AS}	Address Setup Time : DX-LMAR (↓)	70			ns
5	t_{AH}	Address Hold Time : LXMAR (↓)-DX	70			ns
8	t_{END}	Data Output Enable Time: DEVSEL (↓)-DX			290	ns
6	t_{AL}	Access Time from LXMAR			340	ns
7	t_{EN}	Output Enable Time (MEM, CP, DEVSEL)			220	ns
9	t_{WP}	Pulse Width (MEMSEL, CPSEL)	160			ns
10	t_{WPD}	Pulse Width (DEVSEL)	160			ns
11	t_{DS}	Data Setup Time (DX- ↑ MEMSEL/CPSEL)	140			ns
12	t_{DH}	Data Hold Time (↑ MEMSEL/CPSEL-DX)	70			ns
13	t_{DSD}	Data Setup Time (DX- ↑ DEVSEL)	140			ns
14	t_{DHD}	Data Hold Time (↑ DEVSEL-DX)	70			ns
15	t_{SL}	Logic Delay to MEM/DEV/CP/SWSEL	35		210	ns
16	t_{XT}	Logic Delay to LXMAR, XTA, XTB, XTC	35		170	ns
17	t_{ST}	Logic Delay to DATAF, RUN, DMAGNT, INTGNT, LINK, IFETCH			210	ns
18	t_{RS}	Set up Time for CP/INT/DMAREQ	0			ns
19	t_{RH}	Hold Time for CP/INT/DMAREQ, RESET, RUN-HALT	140			ns
20	t_{RHP}	RUN-HALT Pulse Width	50			ns
21	t_{WS}	Set up Time for Wait	50			ns
22	t_{WH}	Hold Time for Wait	20			ns

Note: For capacitance of greater than 50pF, the AC parameters will have a delay factor of 0.5ns/pF.

7

INTERSIL

6801 CMOS Microcomputer Family Sampler Kit

6960 — Sampler PC Board

FEATURES

- **Provides fast and simple exposure to the IM6100 Microcomputer Family**
- **Very inexpensive**
- **Interfaces to any ASCII RS-232 or 20mA terminal**
- **Includes ODT monitor in ROM — Includes tape punch and load routines in ROM**
- **All CMOS components**
- **Executes PDP®-8/E instruction set**
- **Sampler PC board available — easy to use and inexpensive**

GENERAL DESCRIPTION

The 6801 CMOS Microcomputer Family Sampler Kit is a complete set of LSI components necessary to build a general purpose microcomputer. The heart of the Sampler Kit is the IM6100 Microprocessor. The IM6100 Microprocessor executes the PDP-8/E instruction set. The Sampler Kit also includes the ODT (Octal Debugging Technique) monitor ROM (1K x 12), three RAM's (each with 256 x 4 bits to form 256 x 12 bit words), the Programmable Interface Element (IM6101) and a UART (IM6403). A significant cost savings is realized through purchase of the Sampler Kit over the single quantity purchase price of all the included components.

A printed circuit board is also available to simplify construction of the Sampler system (part number 6960). The Sampler board is laid out so that it may interface with both RS-232C and 20mA current loop. The user may enhance the capability of the Sampler system with the addition of sixteen optional SSI packages, assorted switches, and LEDs (optional parts not included). The added capabilities include:

- Address/Bus Display
- Status Display
- Single Instruction Step
- Single Cycle Step
- 12-Bit Input Port
- 12-Bit Output Port

Any of these options can easily be added when desired, but are not required for operation.

The Sampler system, when teamed with any ASCII terminal, gives the user an easy to understand, yet powerful IM6100 Microcomputer system. The ODT Monitor program provides the control necessary to display and alter memory contents, start execution at a particular address, set a breakpoint, manipulate the registers, or search memory for a value. If the terminal has tape punch/read capability, built-in routines allow loading and saving of programs.

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BLOCK DIAGRAM

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System Hookup Diagram

ODT MONITOR COMMANDS

ODT commands consist of a control character or an octal number followed by a control character. The commands may be typed in any time the terminal is idle and are executed as soon as the control character is typed.

BINARY LOAD COMMAND

L — Load from the tape reader

Typing an L will load binary tape from a reader. The checksum will be printed out on the terminal following the end of the load. Printed out checksum should be 0000 for a proper load.

EXAMINE/MODIFY COMMANDS

/ (slash) — Opens a location

Typing an octal number nnnn followed by a slash causes the location whose address is nnnn to be opened. When a location is opened, its content is printed out as an octal number. Typing a slash not preceded by a number causes the most recently opened location to be reopened.

(carriage return) — Closes a location

When a location is open, typing an octal number, nnnn, followed by a carriage return causes the contents of the location to be changed to the number nnnn and closes the location. Typing a carriage return not preceded by a number causes the location to be closed without modifying its contents.

(line feed) — Closes and opens next

When a location is open, typing a line feed causes the location to be closed and the next memory location (that with an address one higher than the current location) to be opened. The address of the new location will be typed out, followed by a slash, followed by the contents of the new location. Typing an octal number, nnnn, before typing the line feed causes the contents of the old location to be changed to nnnn.

← (back arrow) — Closes location and opens indirect reference

When a location is open, typing a back arrow causes the location to be closed. The contents of the location are then treated as an indirect reference. That is, the content of the old location is taken as an address, and the new location is opened. If while a location is open, an octal number, nnnn, is typed followed by a back arrow, the content of the open location is changed to nnnn and proceeds as above.

↑ (up arrow) — Closes location and opens memory reference

This command behaves identically to the back arrow command except that the contents of the location are treated as a memory reference instruction, and it is the location referenced by that instruction that is opened. The location opened is that immediately referenced by the instruction. If the instruction is indirect (bit 3 is set to 1), then typing the up arrow only opens the location containing the pointer to the operand of the instruction. To open the effective location referred to by an indirect instruction, type an up arrow (memory reference) followed by a back arrow (indirection).

PROGRAM CONTROL AND BREAKPOINT COMMANDS

G — Go to

Typing an octal number, nnnn, followed by a G causes ODT to begin executing the program stored in memory, starting at location nnnn.

B — Breakpoint

Typing an octal number, nnnn, followed by a B causes ODT to set a breakpoint at location nnnn. Typing a B without preceding it by a number causes the current breakpoint to be cleared.

C — Continue

After a breakpoint causes control to return to ODT from a user program, typing C causes the program to resume execution where it left off.

A — Examine/modify accumulator, link, MQ

Three consecutive ODT RAM locations are reserved for storing the contents of the AC, link and MQ registers when a breakpoint occurs. When execution of the user's program resumes (via the G or C command), the contents of these registers are restored from these locations. Typing A causes the first of these locations, containing the contents of the AC, to be opened.

WORD SEARCH COMMANDS

M — Open search mask, lower bound, upper bound

The mask, lower bound and upper bound for word searches are kept in that order in three consecutive reserved ODT locations. The first of these locations, the mask, can be opened by typing M.

W — Word search command

Typing an octal number, nnnn, followed by a W causes a word search to occur. The search proceeds as follows: The number, nnnn, that was typed is masked and remembered as the quantity which is being searched for. (The operation of masking is to take the bitwise boolean AND of the given word with the contents of the mask word.) Then each location, beginning with the location whose address is stored in the lower bound word, is masked and compared with the quantity being searched for. If the two are equal, then the address of the word, followed by a slash and the (unmasked) contents of the word are printed out. Then the next location is examined and so on until (and including) the location whose address is stored in the upper bound word is reached. The word search command does not change the contents of any word in the user's programs.

TAPE PUNCHING COMMANDS

The following commands can be used to punch out paper tapes that can be read in by the BIN loader.

T — Punch leader/trailer

Typing a T will cause about four inches of leader/trailer tape (tape punched with 200 octal) to be punched. The T command also causes the accumulated checksum to be set to zero (cleared).

P — Punch tape

Typing an octal number, nnnn, followed by a semicolon (;) followed by a second octal number, mmmm, followed by a P, causes a tape corresponding to the contents of the block of memory beginning at location nnnn and ending at location mmmm to be punched. No checksum is punched at the end of the block so that several blocks can be punched together with one inclusive checksum.

E — Punch checksum and trailer

Typing an E will cause the accumulated checksum to be punched, followed by about four inches of leader/trailer tape. The checksum is also reset to zero (cleared).

SAMPLER ODT EXAMPLE

Say that the simple program

```
300  7001  START, IAC
301  7440         SZA
302  5300         JMP START
303  7402         HLT
```

is stored in memory. Then the following might be the result of a session with ODT. (Note: The underlined portion is typed by the user, and the remainder is typed by the computer. The symbol CR stands for carriage return, and LF stands for line feed.)

300/7001 LF	LIST THE PROGRAM IN OCTAL
301/7440 LF	LF MEANS — SHOW NEXT LOCATION
302/5300 LF	
303/7400 7402 CR	LOCATION 303 IS WRONG — CHANGE AND VERIFY
/ 7402 CR	
A1764 0LF	ACCUMULATOR CONTAINS GARBAGE, MAKE IT ZERO
0050/0001 0CR	SAME FOR LINK
302B	SET BREAKPOINT AT JMP START
300G	EXECUTE PROGRAM (GO)
0302 (0001	BREAKPOINT OCCURS; ACCUMULATOR HAS BEEN INCREMENTED
7774C	CONTINUE PAST BREAKPOINT 1 + 7774 TIMES
0302 (7776	BREAKPOINT OCCURS; AC=7776
303B	RESET BREAKPOINT TO HLT INSTRUCTION
C	CONTINUE
0303 (0000	PROGRAM STOPS WHEN AC REACHES 0 AGAIN
A0000LF	EXAMINE AC AND LINK
0050/0001 CR	LINK HAS BEEN CHANGED BY OVERFLOW
B	CLEAR ALL BREAKPOINTS

6960 — SAMPLER PC BOARD LAYOUT

INTERSIL

Preliminary

IM87C48 CMOS Single-Chip Microcomputer

FEATURES

- **8-bit CPU, EPROM, RAM and I/O in single package**
- **Pin-for-pin replacement for the industry standard 8748 NMOS single-chip microcomputer**
- **CMOS/LSI for low power dissipation — less than 50mW at 5V, 6MHz**
- **High noise immunity**
- **Extended temperature operation: -40°C to +85°C**
- **Single +5V volt supply**
- **Over 90 instructions**
- **1024 bytes of on-chip EPROM**
- **64 bytes of on-chip RAM**
- **27 I/O lines**
- **On-chip counter/timer for real-time applications**

PIN CONFIGURATION

ORDERING INFORMATION

PART NO.	PACKAGE
IM87C48IDL	40 PIN CERAMIC
IM87C48IJL	40 PIN CERDIP

GENERAL DESCRIPTION

The IM87C48 CMOS single-chip microcomputer from Intersil provides the user with a complete microcomputer in a single device. The CPU, EPROM, RAM, a set of I/O lines as well as a counter/timer are all combined in one 40-pin package. Intersil's high performance CMOS/LSI process is used to fabricate a device with equivalent performance to the NMOS 8748 while greatly decreasing the power dissipation. In addition, high noise immunity and an extended temperature range, -40°C to +85°C, make the device ideal for battery operated and hostile environment applications.

The IM87C48 microcomputer features a CPU with a repertoire of over 90 instructions. Included are versatile bit set/reset functions as well as instructions dealing directly with the on-chip counter/timer which are ideal for real-time controller applications. In addition, an eight-level subroutine stack and sixteen general purpose registers ease data flow, provide direct and indirect addressing modes, and implement subroutine calls.

The 27 I/O lines serve as static bidirectional ports, or interfaces to external memories and I/O Expander circuits. Three of the input lines can be "tested" with instructions by the CPU to perform conditional jumps. By combining the microcomputer with external memory devices, compact systems up to 4096 bytes of program memory and 256 bytes of data memory can be constructed. Even larger systems are possible by using bank-switching techniques.

The IM87C48 has been configured to assist the user in debugging his software and hardware prototypes. A single-step pin allows the user to step through the program, instruction by instruction. The EPROM program memory allows the user to try his software without commiting it to ROM. The device also allows external memories to be substituted for the on-chip program memory. This allows simple prototyping aids to be constructed that use RAM in place of EPROM for easy program changes. Additionally, the Intersil Intercept microcomputer development system and EPROM programmer are available to support the software and hardware development of IM87C48 microcomputer based systems.

7

BLOCK DIAGRAM

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FUNCTIONAL PIN DESCRIPTION

DESIGNATOR	PIN #	FUNCTION
V_{CC}	40	Main power supply.
V_{DD}	26	+5V normally, also low power standby.
V_{SS}	20	Circuit GND potential.
PROG	25	This output pin provides timing pulses to the Intersil IM82C43 I/O Expander devices.
OSC 1 OSC 2	2 3	Crystal inputs for generating the internal clock.
$\overline{RESET}$	4	Active low input used to reset the microcomputer. A capacitor from this pin to ground will automatically reset the device on power-up.
EA	7	External Access input used to force all program memory accesses to occur out of external memory.
$\overline{PSEN}$	9	Program Store Enable. This output, active low, occurs only during accesses to external program memory. The system uses this signal together with the address bits to access external program memory.
ALE	11	Address Latch Enable. This output, active high, occurs once during each cycle. The falling edge of this timing signal is used to strobe the address bits appearing on the data bus.
$\overline{RD}$	8	This output, active low, is used by external devices to place data onto the bus during a bus read operation.
$\overline{WR}$	10	This output, active low, is used to strobe data into external devices during a bus write operation.
$\overline{SS}$	5	Single-Step input, active low, that can be used in conjunction with ALE to single-step the processor through each instruction.
T0	1	An input pin that can be tested by the conditional jump instructions. This pin can be programmed as an output by the ENT0 CLK instruction which then causes an internal clock to be output on this pin. The frequency of the system clock is the clock crystal frequency divided by three.
T1	39	An input pin that can be tested by the conditional jump instructions. The pin can also be programmed as the input to counter/timer.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if external interrupt is enabled.
P10-P17	27-34	Port 1. An 8-bit quasi bidirectional port. The I/O structure on these eight lines allows each to be used separately as either an input or an output.
P20-P27	21-24, 35-38	Port 2. Identical to Port 1 except that P20-P23 contain the four high order program counter bits during an external program memory fetch. If IM82C43 I/O Expanders are being used in the system, they communicate with the IM87C48 through these four lines.
DB0-DB7 (BUS)	12-19	Data Bus. These eight lines form a true bidirectional port which can store data as a latched output port or serve as a non-latching input port.

7

ABSOLUTE MAXIMUM RATINGS

Operating Temperature ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Supply Voltage ..... +7.0V
Voltage on Any Input or
Output Pin ..... V_{SS} - 0.3V to V_{CC} + 0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = V_{DD} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $T_A = -40°C$ to $+85°C$

	SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
1	V_{IL}	Input Low Voltage		-0.3		0.8	V
2	V_{IH}	Input High Voltage (All except OSC1, $\overline{RESET}$, and T1)		V_{CC}-2		V_{CC}	V
3	V_{IH}	Input High Voltage (OSC1, $\overline{RESET}$, and T1)		V_{CC}-1		V_{CC}	V
4	V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA			0.45	V
5	V_{OH}	Output High Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	I_{OH} = -100 μA	2.4			V
6	V_{OH1}	Output High Voltage (All other outputs)	I_{OH} = -50 μA	2.4			V
7	I_{IL}	Input Leakage Current (All except $\overline{RESET}$, $\overline{SS}$, Port 1 and Port 2)	$V_{SS} \le V_{IN} \le V_{CC}$		±1		μA
8	I_{ILP}	Input Current Port 1, Port 2	$V_{IN} \le V_{IL}$		-160		μA
9	I_{ILC}	Input Current $\overline{SS}$, $\overline{RESET}$	$V_{IN} \le V_{IL}$		-40		μA
10	I_{OL}	Output Leakage Current	$V_{SS} \le V_O \le V_{CC}$		±1		μA
11	I_{CC}	V_{CC} Supply Current	f_{XTAL} = 6 MHz			10	mA
12	$I_{DD} + I_{CC}$	Total Supply Current				10	mA

A.C. CHARACTERISTICS[1]

TEST CONDITIONS: $V_{CC} = V_{DD} = 5.0V \pm 5\%$, $T_A = -40°C$ to $+85°C$

	SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
1	t_{CY}	Cycle Time	f_{XTAL} = 6 MHz	2.5			μs
2	t_{LL}	ALE Pulse Width		400			ns
3	t_{AL}	Address Setup to ALE		150			ns
4	t_{LA}	Address Hold from ALE		80			ns
5	t_{CC}	Control Pulse Width $\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$		700			ns
6	t_{DW}	Data Setup Before $\overline{WR}$		500			ns
7	t_{WD}	Data Hold After $\overline{WR}$		120			ns
8	t_{DR}	Data Hold		0		200	ns
9	t_{RD}	$\overline{PSEN}$, $\overline{RD}$ to Data In				500	ns
10	t_{AW}	Address Setup to $\overline{WR}$		230			ns
11	t_{AD}	Address Setup to Data In				950	ns
12	t_{AFC}	Address Float to $\overline{RD}$, $\overline{PSEN}$		0			ns

NOTE:
1. Control outputs are loaded with C_L = 80pF and BUS outputs with C_L = 150pF. t_{CY} is assumed to be 2.5 μs.

A.C. CHARACTERISTICS (PORT 2 TIMING)

TEST CONDITIONS: $V_{CC} = V_{DD} = 5.0V \pm 5\%$, $T_A = -40°C$ to $+85°C$

	SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
1	t_{CP}	Port Control Setup Before Falling Edge of $\overline{PROG}$		110			ns
2	t_{PC}	Port Control Hold After Falling Edge of $\overline{PROG}$		100			ns
3	t_{PR}	PROG to Time P2 Input Must be Valid				810	ns
4	t_{DP}	Output Data Setup Time		250			ns
5	t_{PD}	Output Data Hold Time		65			ns
6	t_{PF}	Input Data Hold Time		0		150	ns
7	t_{PP}	$\overline{PROG}$ Pulse Width		1200			ns
8	t_{PL}	Port 2 I/O Data Setup		350			ns
9	t_{LP}	Port 2 I/O Data Hold		150			ns

WAVEFORMS

INSTRUCTION FETCH FROM EXTERNAL PROGRAM MEMORY

WRITE TO EXTERNAL DATA MEMORY

READ FROM EXTERNAL DATA MEMORY

PORT 2 TIMING

7

APPLICATIONS

SINGLE-CHIP MICROCOMPUTER SYSTEM

USING IM6654 CMOS EPROM TO EXTEND PROGRAM MEMORY

USING IM82C43 I/O EXPANDERS, THIS FIVE CHIP SYSTEM HAS 80 I/O LINES.

PACKAGE DIMENSIONS

40 PIN CERAMIC DIP

NOTE: Dimensions in parenthesis are metric.

7

NOTES

7

INTERSIL

Preliminary

IM80C49 CMOS Single-Chip Microcomputer

FEATURES

- **8-bit CPU, ROM, RAM and I/O in single package**
- **Pin-for-pin replacement for the industry standard 8049 NMOS single-chip microcomputer**
- **CMOS/LSI for low power dissipation — less than 50mW at 5V, 6MHz**
- **High noise immunity**
- **Extended temperature operation: -40°C to +85°C**
- **Single +5V volt supply**
- **Over 90 instructions**
- **2048 bytes of on-chip ROM**
- **128 bytes of on-chip RAM**
- **27 I/O lines**
- **On-chip counter/timer for real-time applications**

GENERAL DESCRIPTION

The IM80C49 CMOS single-chip microcomputer from Intersil provides the user with a complete microcomputer in a single device. The CPU, ROM, RAM, a set of I/O lines as well as a counter/timer are all combined in one 40-pin package. Intersil's high performance CMOS/LSI process is used to fabricate a device with equivalent performance to the NMOS 8049 while greatly decreasing the power dissipation. In addition, high noise immunity and an extended temperature range, -40°C to +85°C, make the device ideal for battery operated and hostile environment applications.

The IM80C49 microcomputer features a CPU with a repertoire of over 90 instructions. Included are versatile bit set/reset functions as well as instructions dealing directly with the on-chip counter/timer which are ideal for real-time controller applications. In addition, an eight-level stack and sixteen general purpose registers ease data flow, provide direct and indirect addressing modes, and implement subroutine calls.

The 27 I/O lines serve as static bidirectional ports, or interfaces to external memories and I/O Expander circuits. Three of the input lines can be "tested" with instructions by the CPU to perform conditional jumps. By combining the microcomputer with external memory devices, compact systems up to 4096 bytes of program memory and 256 bytes of data memory can be constructed. Even larger systems are possible by using bank-switching techniques.

PIN CONFIGURATION

ORDERING INFORMATION

PART NO.	PACKAGE
IM80C49IDL	40 PIN CERAMIC
IM80C49IJL	40 PIN CERDIP

7

BLOCK DIAGRAM

FUNCTIONAL PIN DESCRIPTION

DESIGNATOR	PIN #	FUNCTION
V_{CC}	40	Main power supply.
V_{DD}	26	+5V normally, also low power standby.
V_{SS}	20	Circuit GND potential.
PROG	25	This output pin provides timing pulses to the Intersil IM82C43 I/O Expander devices.
OSC 1 OSC 2	2 3	Crystal inputs for generating the internal clock.
$\overline{RESET}$	4	Active low input used to reset the microcomputer. A capacitor from this pin to ground will automatically reset the device on power-up.
EA	7	External Access input used to force all program memory accesses to occur out of external memory.
$\overline{PSEN}$	9	Program Store Enable. This output, active low, occurs only during accesses to external program memory. The system uses this signal together with the address bits to access external program memory.
ALE	11	Address Latch Enable. This output, active high, occurs once during each cycle. The falling edge of this timing signal is used to strobe the address bits appearing on the data bus.
$\overline{RD}$	8	This output, active low, is used by external devices to place data onto the bus during a bus read operation.
$\overline{WR}$	10	This output, active low, is used to strobe data into external devices during a bus write operation.
$\overline{SS}$	5	Single-Step input, active low, that can be used in conjunction with ALE to single-step the processor through each instruction.
T0	1	An input pin that can be tested by the conditional jump instructions. This pin can be programmed as an output by the ENT0 CLK instruction which then causes an internal clock to be output on this pin. The frequency of the system clock is the clock crystal frequency divided by three.
T1	39	An input pin that can be tested by the conditional jump instructions. The pin can also be programmed as the input to counter/timer.
$\overline{INT}$	6	Interrupt input. Initiates an interrupt if external interrupt is enabled.
P10-P17	27-34	Port 1: An 8-bit quasi bidirectional port. The I/O structure on these eight lines allows each to be used separately as either an input or an output.
P20-P27	21-24, 35-38	Port 2. Identical to Port 1 except that P20-P23 contain the four high order program counter bits during an external program memory fetch. If IM82C43 I/O Expanders are being used in the system, they communicate with the IM87C48 through these four lines.
DB0-DB7 (BUS)	12-19	Data Bus. These eight lines form a true bidirectional port which can store data as a latched output port or serve as a non-latching input port.

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ABSOLUTE MAXIMUM RATINGS

Operating Temperature ..... -40°C to +85°C
Storage Temperature ..... -65°C to +150°C
Supply Voltage ..... +7.0V
Voltage on Any Input or
Output Pin ..... V_{SS} - 0.3V to V_{CC} + 0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: $V_{CC} = V_{DD} = 5.0V \pm 5\%$, $V_{SS} = 0V$, $T_A = -40°C$ to $+85°C$

	SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
1	V_{IL}	Input Low Voltage		-0.3		0.8	V
2	V_{IH}	Input High Voltage (All except OSC1, $\overline{RESET}$, and T1)		V_{CC}-2		V_{CC}	V
3	V_{IH}	Input High Voltage (OSC1, $\overline{RESET}$, and T1)		V_{CC}-1		V_{CC}	V
4	V_{OL}	Output Low Voltage	I_{OL} = 2.0 mA			0.45	V
5	V_{OH}	Output High Voltage (BUS, $\overline{RD}$, $\overline{WR}$, $\overline{PSEN}$, ALE)	I_{OH} = -100 μA	2.4			V
6	V_{OH1}	Output High Voltage (All other outputs)	I_{OH} = -50 μA	2.4			V
7	I_{IL}	Input Leakage Current (All except $\overline{RESET}$, $\overline{SS}$, Port 1 and Port 2)	$V_{SS} \le V_{IN} \le V_{CC}$		±1		μA
8	I_{ILP}	Input Current Port 1, Port 2	$V_{IN} \le V_{IL}$		-160		μA
9	I_{ILC}	Input Current $\overline{SS}$, $\overline{RESET}$	$V_{IN} \le V_{IL}$		-40		μA
10	I_{OL}	Output Leakage Current	$V_{SS} \le V_O \le V_{CC}$		±1		μA
11	I_{CC}	V_{CC} Supply Current	f_{XTAL} = 6 MHz			10	mA
12	$I_{DD} + I_{CC}$	Total Supply Current				10	mA

A.C. CHARACTERISTICS[1]

TEST CONDITIONS: $V_{CC} = V_{DD} = 5.0V \pm 5\%$, $T_A = -40°C$ to $+85°C$

	SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
1	t_{CY}	Cycle Time	f_{XTAL} = 6 MHz	2.5			μs
2	t_{LL}	ALE Pulse Width		400			ns
3	t_{AL}	Address Setup to ALE		150			ns
4	t_{LA}	Address Hold from ALE		80			ns
5	t_{CC}	Control Pulse Width $\overline{PSEN}$, $\overline{RD}$, $\overline{WR}$		700			ns
6	t_{DW}	Data Setup Before $\overline{WR}$		500			ns
7	t_{WD}	Data Hold After $\overline{WR}$		120			ns
8	t_{DR}	Data Hold		0		200	ns
9	t_{RD}	$\overline{PSEN}$, $\overline{RD}$ to Data In				500	ns
10	t_{AW}	Address Setup to $\overline{WR}$		230			ns
11	t_{AD}	Address Setup to Data In				950	ns
12	t_{AFC}	Address Float to $\overline{RD}$, $\overline{PSEN}$		0			ns

NOTE:
1. Control outputs are loaded with C_L = 80pF and BUS outputs with C_L = 150pF, t_{CY} is assumed to be 2.5 μs.

A.C. CHARACTERISTICS (PORT 2 TIMING)

TEST CONDITIONS: $V_{CC} = V_{DD} = 5.0V \pm 5\%$, $T_A = -40°C$ to $+85°C$

	SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNITS
1	t_{CP}	Port Control Setup Before Falling Edge of $\overline{PROG}$		110			ns
2	t_{PC}	Port Control Hold After Falling Edge of $\overline{PROG}$		100			ns
3	t_{PR}	PROG to Time P2 Input Must be Valid				810	ns
4	t_{DP}	Output Data Setup Time		250			ns
5	t_{PD}	Output Data Hold Time		65			ns
6	t_{PF}	Input Data Hold Time		0		150	ns
7	t_{PP}	$\overline{PROG}$ Pulse Width		1200			ns
8	t_{PL}	Port 2 I/O Data Setup		350			ns
9	t_{LP}	Port 2 I/O Data Hold		150			ns

WAVEFORMS

INSTRUCTION FETCH FROM EXTERNAL PROGRAM MEMORY

WRITE TO EXTERNAL DATA MEMORY

READ FROM EXTERNAL DATA MEMORY

PORT 2 TIMING

APPLICATIONS

SINGLE-CHIP MICROCOMPUTER SYSTEM

USING IM6654 CMOS EPROM TO EXTEND PROGRAM MEMORY

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USING IM82C43 I/O EXPANDERS, THIS FIVE CHIP SYSTEM HAS 80 I/O LINES.

PACKAGE DIMENSIONS

40 PIN CERAMIC DIP

NOTE: Dimensions in parenthesis are metric.

INTERSIL

IM5200 Field Programmable Logic Array (FPLA)

FEATURES

- Avalanche Induced Migration (AIM) Programmability
- 48 Product Terms, 14 Inputs, 8 Outputs
- Output Active Level – High or Low
- Product Term Expandability
- Edit Flexibility
- DTL/TTL Compatible Inputs and Outputs
- tpd – typically 65 ns
- 5 Volt ± 5% Power Supply
- Passive Pullup Outputs

APPLICATIONS

- Random Combinatorial Logic
- Code Conversion
- Microprogramming
- Look-up Tables
- Control of Sequential Circuits, Counters, Registers, RAMs, etc.
- Character Generators
- Decoders or Encoders

GENERAL DESCRIPTION

The IM5200, field programmable logic array (FPLA), is useful in a wide variety of logic applications. The device has 14 inputs and 8 outputs. The FPLA may have up to 48 product terms. Each product term may have up to 14 variables and each one of the outputs provides a sum of the product terms. The FPLA is functionally equivalent to a collection of AND gates which may be OR'ed at any of its outputs. Since some functions are more easily represented in their inverted form, the output level is also programmable to either a high or low active level. The IM5200 is provided with passive pullup outputs. This output configuration is useful for product term expansion by wire-ANDing the outputs of different IM5200's.

LOGIC DIAGRAM

PACKAGE DIMENSIONS

CONNECTION DIAGRAM

ORDERING INFORMATION

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MAXIMUM RATINGS

Supply Voltage Rating	−0.5V to +7V
Input Voltage	−1.5V to +5.5V
Output Voltage (Operating)	−0.5V to +5.5V
Storage Temperature	−65°C to 150°C
Operating Temperature	0°C to +75°C

ELECTRICAL CHARACTERISTICS V_{CC} = 5.0V + 5%, T_A = 0°C to +75°C

SYMBOL	PARAMETERS	MIN	TYP	MAX	UNITS	CONDITIONS
I_{IL}	Low level input current		−0.63	−1.0	mA	V_{IL} = 0.4V
I_{IH}	High level input current		5	40	μA	V_{IH} = 4.5V
V_{IL}	Input low threshold voltage			0.8	V	
V_{IH}	Input high threshold voltage	2.0			V	
V_C	Input clamp voltage		−.9	−1.5	V	I_{IN} = −10 mA
BV_{in}	Input breakdown voltage	5.5	6.5		V	I_{IN} = 1.0 mA
V_{OH}	Output high voltage	2.4	3.25		V	I_{OH} = −250μA
I_{CEX}	Output leakage current		<1	50.	μA	V_O = 5.5V
I_{SC}	Output short circuit current	−0.7	−1.1	−1.7	mA	V_O = 0V
V_{OL}	Output low voltage		0.3	0.45	V	I_{OL} = 12 mA
I_{CC}	Power Supply Current		135		mA	Inputs either open or at ground (see note 3).
C_{in}	Input capacitance		5	10	pF	V_{in} = 2.0V, V_{CC} = 0V
C_{out}	Output capacitance		7	12	pF	V_O = 2.0V, V_{CC} = 0V
t_{pd}	Input to output switching delay (t_{+-}, t_{++}, t_{-+}, t_{--})	20	65	100	ns	See switching test circuit

NOTE 1: Conditions for all typical values are V_{CC} = 5V, T_A = 25°C.

NOTE 2: Conditions for all maximum and minimum specifications are the worst case for the complete range of V_{CC} and T_A.

NOTE 3: Power consumption will increase after programming. The increase will be typically 0.75 mA per product term programmed.

SWITCHING DELAY TEST CIRCUIT

FREQ = 1MHz
DUTY CYCLE = 50%
AMPLITUDE = 0V to 3V
$t_R = t_F$ = 5 ns

SWITCHING WAVEFORMS

ALL MEASUREMENTS MADE AT 1.5V LEVELS

PRODUCT DESCRIPTION

AVALANCHE INDUCED MIGRATION TECHNOLOGY

The AIM element is a minimum size, open base, NPN transistor. The emitter is contacted by an aluminum "column" line and the collector is common with the collectors of other elements and the "row" driver collector. A conventional gold doped TTL process is used to fabricate the AIM element and all other transistors, diodes and resistors on the chip. The programming technique is to force a high current through the element from emitter to collector. This forces the emitter-base junction beyond normal avalanche and into a second breakdown mode. In the second breakdown, the current constricts to a narrow high temperature filament. Aluminum then migrates down the filament to the emitter-base-junction and causes a short of that junction. The drop in power dissipation, as soon as the emitter-base short is achieved, causes a decrease in temperature. Since temperature is a driving force in the programming action, further advance of migrating aluminum is inhibited after programming is achieved. The action is thus self-limiting. The AIM programming technique assures superior reliability since the element junction where the programming action occurs is inherently hermetic.

GENERAL DESCRIPTION

The IM5200 Field Programmable Logic Array (FPLA) is a logic element designed to produce a sum of product terms, which may be programmed by the user, at each of eight outputs. The basic operating circuit is comprised of 56 input inverters, which generate the true and complement of the 14 inputs, 48 twenty-eight input AND gates, 8 forty-eight input NOR gates and 3 arrays of AIM programmable elements. Additional circuitry is dedicated to the functions of programming and testing before programming. All outputs have 4K resistor pull-ups which permit wire-ANDing. Inputs are DTL and TTL designs with 2 V_{BE} operating thresholds.

Product Term Array

The Product Term Array, consisting of a 48 x 28 element AND array, allows the desired true or complement inputs to be connected by programming to the 48 AND gates which form the product terms. Only the input variables included in the product terms are programmed. New variables may always be added to a previously programmed product-term until all 14 variables have been used.

Summing Array

A 48 x 8 element OR array allows any combination of as many as 48 product terms to be logically summed (OR'ed) at each output by programming.

Output Active Level Array

The Output Active Level Array consists of eight elements, one per output, which provide for changing the active level of any output from LOW to HIGH. Active LOW is the necessary active state when expanding product terms by the parallel connections of two (2) or more IM5200s. The programmable active HIGH feature may be used to advantage in nonexpanded applications to save inverters and/or product terms when system considerations so require.

LOGIC OPERATION

The operating logic and AIM programmable element arrays are shown in Figure 1. In logic equation form each output can be expressed in the SUM OF PRODUCTS form.

F_i or $\overline{F_i}$ = logical sum of any user programmed combination of 48 available product terms (PT_j)

where PT_j = any user programmed combination of the true or complement of the 14 available inputs (I_k).

NOTES

1. Programming Logic and Preprogramming Test Logic is not shown.
2. Active Level Inversion Elements (8 total)

Figure 1. FPLA Operating Logic.

Some examples of possible SUM-OF-PRODUCT-TERMS functions and individual PRODUCT TERMS are:

SUM OF PRODUCT TERMS

$\overline{F}_1 = PT_3 + PT_{28} + PT_{39} + PT_{47}$

$F_3 = PT_1 + PT_{33} + PT_{39} + PT_{45} + PT_{46} + PT_{47}$

$\overline{F}_7 = PT_2$

PRODUCT TERMS

$PT_3 = I_0 \overline{I}_2 \overline{I}_8 \overline{I}_{13}$

$PT_{46} = I_1 \overline{I}_6 I_9 I_{11} \overline{I}_{12} I_{13}$

$PT_2 = I_4$

A product term is not necessarily a minterm since a minterm contains *all* input variables. The unprogrammed inputs of a product term that is not a minterm are "don't care". For example, the product term $I_1 I_3 \overline{I}_{13}$ will activate any output to which it is programmed whenever the I_1 input is HIGH, I_3 is HIGH, and I_{13} is LOW, regardless of the logic state of the other inputs. A minterm expansion of $I_1 I_3 \overline{I}_{13}$ would produce 2^{11} miniterms which means there are 2^{11} out of 2^{14} possible combinations of all 14 input variables that will activate any output to which the product term is programmed.

Any minterm condition applied to the IM5200 inputs will select (1) no product terms, (2) one product term, or (3) more than one product term.

In the case of no product term selection all the outputs will be in the inactive state (opposite to the levels specified in the ACTIVE LEVEL DATA for each output).

When only one product term is selected, the outputs assume the active levels specified by the SUMMING DATA TRUTH TABLE entry for the selected product term. The outputs not specified as active will assume the inactive state (opposite state to that specified in the ACTIVE LEVEL DATA).

To determine the output status for a case of multiple product term selection, first all of the product terms selected must be identified. Each output state can then be determined by examining the SUMMING DATA for all of the multiply selected product terms.

If *any* of the product terms has an active level specified for the output, the output will assume the active state as specified by the ACTIVE LEVEL DATA. If *none* of the product terms have an active level specified for the output, the outputs will assume the inactive state (opposite state to that specified by the ACTIVE LEVEL DATA.

TESTING

Some circuitry is built into the IM5200 for test purposes only. On an unprogrammed part it allows for:

1. Testing the output in the LOW state
2. Sampling the switching delay time through a maximum delay path
3. Checking the accuracy of programming circuitry decoding
4. Checking the integrity of programming paths under programming conditions

This test capability assures high programming yield and data sheet electrical performance after programming of parts.

PRODUCT TERM MINIMIZATION TECHNIQUES

Standard two (2) level multi-output minimization techniques (e.g. Quine-McCluskey algorithm) can be used to realize a minimal sum of product terms. In certain cases, the number of product terms can be further reduced by sharing product terms and by inverting the output active level. These techniques are important in cases where the initial specification indicates a need for more than 48 product terms.

APPLICATION OF BOOLEAN REDUCTION

REALIZE: $F_1 = \overline{I}_2 \overline{I}_1 \overline{I}_0 + I_2 I_1 \overline{I}_0 + I_2 I_1 I_0$

Applying the distributive law, product terms $I_2 I_1 I_0$ and $I_2 I_1 \overline{I}_0$ can be expressed as $I_2 I_1 (I_0 + \overline{I}_0)$. By the law of complement, $I_0 + \overline{I}_0 = 1$ and the entire expression is reduced to:

$F_1 = \overline{I}_2 \overline{I}_1 \overline{I}_0 + I_2 I_1$

PRODUCT TERM SHARING

REALIZE: $F_1 = \overline{I}_2 \overline{I}_1 \overline{I}_0 + \overline{I}_2 I_1 \overline{I}_0$

$F_2 = \overline{I}_2 I_1 \overline{I}_0 + I_2 \overline{I}_1 \overline{I}_0$

Since $\overline{I}_2 I_1 \overline{I}_0$ is common to both F_1 and F_2, it may be shared so that only three product terms, rather than four, are required.

ACTIVE LEVEL INVERSION

REALIZE: $F_1 = \overline{I}_2 \overline{I}_1 \overline{I}_0 + \overline{I}_2 I_1 I_0 + I_2 \overline{I}_1 I_0 + I_2 I_1$

To achieve a reduction in product terms, in this case, F_1 can be realized in its complement form using DeMorgan's Theorems. The true form required a HIGH active level and 4 product terms. The complement form requires a LOW active level and 3 product terms.

$\overline{F}_1 = \overline{I}_2 \overline{I}_1 I_0 + \overline{I}_2 I_1 \overline{I}_0 + I_2 \overline{I}_1 \overline{I}_0$

EDIT FLEXIBILITY

PRODUCT TERM DEACTIVATION

The true or the complement of any input may be connected to the AND gates by programming. However, if both the true *and* the complement of any variable are programmed in a product term, that product term will never be selected since $I_i \cdot \overline{I}_i = 0$. This feature may be used to deactivate permanently any previously programmed product term.

ADDITION OF NEW INPUT VARIABLES TO EXISTING PRODUCT TERMS

In the AIM technology only the active inputs are programmed. Unprogrammed inputs are "don't care." Therefore, additional input variables can be added to the "old" product terms at any time. For example,

Old Product Term

$I_0 I_1 \overline{I}_4$ ($I_2, I_3, I_5 \cdots I_{13}$ = don't care)

Adding input variable I_2 (true or complement) to the product term would yield:

New Product Term

$I_0 I_1 I_2 \overline{I}_4$ ($I_3, I_5 \cdots I_{13}$ = don't care)

EXPANDING A SUM OF PRODUCT TERMS BY ADDING NEW PRODUCT TERMS

New product terms may be added to the sum of product terms at any output by programming the AIM element that connects the product term AND gate to the output thereby enabling activation of the output when the product term is activated. The product term may be one already used in another output sum of product terms or it may be one that has not previously been used.

CHANGING AN OUTPUT ACTIVE LEVEL FROM LOW TO HIGH

Any outputs that are active LOW can be changed to active HIGH by programming the corresponding AIM element in the OUTPUT ACTIVE LEVEL ARRAY.

PROGRAMMING

GENERAL

Recommended Programmer is DATA I/O model 10.

Programming an IM5200 requires:

1. Two input pins, I_0 and I_9 corresponding to pins 21 and 7, respectively, to be forced to a voltage above normal TTL operating levels to establish the programming mode.
2. One input pin, I_3 corresponding to pin 1, to be switched between a high level and ground to select between the Summing Array (OR Array) or the Product Term Array (AND Array), respectively.

OUTPUT	PIN	SECTOR	LOCATION
F_0	13	1	0 – 15 Product Terms; AND/OR Arrays
F_1	14	2	16 – 31 Product Terms; AND/OR Arrays
F_2	15	3	32 – 47 Product Terms; AND/OR Arrays
F_3	16	4	Output Active Level Array

3. Four outputs, F_0, F_1, F_2, and F_3 corresponding to pins 13, 14, 15, and 16, respectively, for the routing of current into one of four sectors of the arrays.
4. Nine inputs, I_4, I_5, I_6, I_7, I_8, I_{10}, I_{11}, I_{12}, and I_{13} corresponding to pins 2, 3, 4, 5, 6, 8, 9, 10, and 11, respectively, to select a unique element within a sector.

Inputs I_1 and I_2, corresponding to pins 22 and 23, are used to enable testing of propagation delay, programming circuitry decoding and output low level characteristics before programming.

Programming current pulses are forced into the output pin, corresponding to a particular sector and routed to the element selected for programming. The elements are sensed at a reduced current level after each programming pulse to determine if programming has occurred.

After all necessary elements are programmed, the array is reverified by scanning the array and resensing all elements directly. Finally, a logical verification is conducted forcing all 2^{14} input states and checking the eight outputs for the correct logic levels.

EFFECTS OF PROGRAMMING (P) OR NOT PROGRAMMING (NP) AN ELEMENT IN EACH OF THE THREE ARRAYS

Output Active Level Array

AL_i	EFFECT ON AN OUTPUT
NP	Output active level will be a LOW for all product terms programmed to the output.
P	Output active level will be a HIGH for all product terms programmed to the output.

Product Term Array

I_k	$\overline{I}_k$	EFFECT ON A PRODUCT TERM
NP	NP	The logic state of the input cannot effect the product term. It is a "don't care" input.
NP	P	Low input becomes an active variable in the product term.
P	NP	High input becomes an active variable in the product term.
P	P	Disables the product term, preventing the product term from ever activating any output.

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Summing Array

PT_j	EFFECT ON AN OUTPUT
NP	Output is isolated from the product term unless programmed. Therefore, activation of the product term can not affect the output.
P	Activation of the product term will force the output to its active level.

DATA FORMATS FOR PROGRAMMING

Intersil Inc. can program the IM5200 from data inputs consisting of a truth table, or paper tape. Format specifics follow. If TWX data inputting is used, TWX 910-338-0171. If mailing data input, mail to:

INTERSIL, INCORPORATED
ATTEN: ORDER ENTRY
10710 N. Tantau Avenue
Cupertino, CA 95014

FORMAT INFORMATION SUMMARY

	HAND ENTRY IN TRUTH TABLE FORM	TWX – RCVD AS HARD COPY OR PAPER TAPE	PAPER TAPE
Heading Information	Enter at top of the form as indicated	Enter as per example preceding start of data (STX). The asterisk (*) character may not be used in any heading information	Enter as per example preceding the start of data (STX). The asterisk (*) character may not be used in any heading information
Start of Data	Not required	STX (Control B)	STX (Control B)
Active Level Data Identifier	Not required	*A	*A
Active Level Data Entry	H = High active level L = Low active level	H = High active level L = Low active level	H = High active level L = Low active level
Product Term Number Identifier	Not required	*P	*P
Product Term Number Entry	Preprinted	MSD = Decimal 0-4 LSD = Decimal 0-9	MSD = Decimal 0-4 LSD = Decimal 0-9
Product Term Input Data Identifier	Not required	*I	*I
Product Term Input Data Entry	H = Active high input L = Active low input BLANK = Don't care input	H = Active high input L = Active low input – = Don't care input	H = Active high input L = Active low input – = Don't care input
Summing Data Identifier	Not required	*F	*F
Summing Data Entry	A = Product term is summed by this output BLANK = Product term is not summed by this output	A = Product term is summed by this output – = Product term is not summed by this output	A = Product term is summed by this output – = Product term is not summed by this output
End of Data	Not required	ETX (Control C)	ETX (Control C)
Deactivating a Product Term	Enter D as any input entry for a product term to be deactivated	Enter D as any input entry for a product term to be deactivated	Enter D as any input entry for a product term to be deactivated
Spacing, Carriage Returns, Line Feeds	Not applicable	As needed to give an easily readable appearance in teletype printed form See TWX description for recommended format	Not required unless examination by printout on a teletype is desirable See Paper Tape description for recommended format
Rubouts	Not applicable	May be used to correct errors	May be used to correct errors

TRUTH TABLES

Truth tables can be submitted to Intersil Inc. by mail or by TWX (910-338-0171). A truth table format for mailing is presented as a part of this data sheet. Additional copies of this format are available upon request. The customer should complete all heading information on the format in order to assure that it will remain as a part of the purchase order which is entered.

When entering a truth table by TWX, the following format is recommended so that the data is compatible with the paper tape format. The TWX can, therefore, be received in punched paper tape form for direct processing by a programmer equipped with a paper tape reader input.

TWX FORMAT

```
ATTEN ORDER ENTRY

PO NUMBER 7-706574

BILL TO BRADY ELECTRONICS INC
        1074 SIXTH ST
        SYRACUSE NY 13206

SHIP TO BRADY ELECTRONICS INC
        764 EAST CARLTON
        SYRACUSE NY 13206

TELE (315) 463-5870

TWX 910-377-6402

BUYER HANK KENONE

SHIP AIR EXPRESS

ITEM 01 P/N 706475-001        12 PCS        DELIVERY ASAP


TRUTH TABLE P/N 706475-001
```

START OF DATA

```
                    ⑦
                 13        0
  ①              |         |   ②        ③
STX              |         |  *A LLLLLLLL
                 |12       |1
  ④  ⑤  ⑥        |         |   ⑧        ⑨
*P 00 *I LL---L--------H *F -----AA-
*P 01 *I LLLLLH-------- *F A----AAA
*P 02 *I HHLLLH-------- *F AA---AA-
*P 47 *I LHHHLHLLL-LLL *F --------
                                      ⑩
                                     ETX
```

EXPLANATION OF NUMBERS

1. STX "CONTROL B" ON TELETYPEWRITER
2. *A = ACTIVE LEVEL DATA IDENTIFIER CHARACTERS
3. ACTIVE LEVEL DATA (H OR L)
4. *P = PRODUCT TERM NUMBER IDENTIFIER CHARACTERS
5. PRODUCT TERM NUMBER
6. *I = PRODUCT TERM INPUT DATA IDENTIFIER CHARACTERS
7. PRODUCT TERM INPUT DATA (H, L, D OR –)
8. *F = SUMMING DATA IDENTIFIER CHARACTERS
9. SUMMING DATA (A OR –)
10. ETX = "CONTROL C" ON TELETYPEWRITER

TAPE FORMAT

PAPER TAPE

Teletype 8 level TWX tape can be mailed to Intersil, Inc., Attention: Order Entry. Heading information similar to that used for the TWX truth table format presented above, should be punched on the tape.

The recommended format for the data portion of a paper tape is shown above. Deviations in spacing, carriage returns, line feeds and rubouts are allowed but the start and end characters, the data identifiers, the data characters and the order of data must be strictly followed.

7

APPLICATIONS

CODE CONVERSION

The IM5200 can be used efficiently in code conversion applications where all possible combinations of a particular code are not used. The conversion from 12 level Hollerith to 8 level ASCII provides such an example. In the standard solution to this problem, the 12 level Hollerith code is first reduced to 8 levels, with logic, before it is presented to a 256 x 8 ROM. All non-existing input combinations must be decoded as "don't care" output states in the ROM.

The IM5200 can selectively decode 14 input variables; no precoding of the inputs is necessary. With the proper selection of output active levels, an invalid input combination will also automatically produce a unique "don't care" or error code.

MICROPROGRAMMING

In a microprogrammed computer, the microinstructions control the correct sequencing of the Central Processor Unit to execute appropriate macroinstructions. The microinstructions reside in the microprogram store. The addresses of the microroutine in the control store, which interpret external instructions, are the operation codes of the external instructions. Since the operation codes of various instructions in a processor may be of different lengths, some codes may have more bits than are necessary to address the control store. For example, a 16-bit microprocessor may have operation codes up to 16 bits long. However, the microprocessor store may have only 256 words of memory.

The IM5200 can be conveniently used to translate an arbitrary operation code to obtain the proper control store address. The IM5200 can also be used in the control store to minimize the size of the microprogram memory by utilizing the unique capability of the device to cope with special address combinations — "don't care" bits in addresses, a single address for multiple words and multiple addresses for single words.

SEQUENTIAL CONTROL

The IM5200 can be used effectively in sequencing applications to implement flow charts of state diagrams, condition driven look up tables or arbitrary state sequencers. The IM5200 input set could come from external control points ("qualifying inputs") or the IM5200 outputs coupled through feed-back latches ("current state inputs").

PERIPHERAL DEVICE CONTROL

For a Central Processor Unit to communicate with a peripheral device, the CPU must select the device and the mode of communication. During an Input-Output instruction, the CPU transmits the device address and control information to select a unique device in a specified mode. The IM5200 can be used to monitor the device address and control field bus to issue appropriate control signals to the devices.

PRIORITY ENCODING

An interesting application of the IM5200 is the priority encoding of interrupt request lines to generate a unique vector address which corresponds to the highest priority request line. The CPU can then use the vector address as a JUMP address to service the highest priority device without going through a software "polling" routine.

EXPANSION OF THE NUMBER PRODUCT TERMS BY WIRE-ANDING

The IM5200 can implement several simple functions by using only part of the structure for each function. Complex functions can be implemented by connecting several IM5200's in series or parallel.

The IM5200 has passive pull-up (4K) outputs. This output configuration is useful for product term expansion by wire-ANDing the outputs of different IM5200's. For EPLA applications, expansion by wire-ANDing is preferrable to the conventional chip select approach, since in many applications, it is difficult to generate the chip select signal, in view of the fact that "chip select" decision may itself be based on a random combination of the input variables.

Active LOW is the necessary active state for the outputs that must be wire-ANDed. It must be noted that the fan-out of the wire-ANDed outputs is reduced by approximately one standard TTL load for each IM5200 output that is tied together.

COMPANY _____

ADDRESS _____

_____

PHONE _____

DATE	Page of
CUSTOMER P.O. No.	
CUSTOMER PRINT OR I.D. No.	

IM5200 TRUTH TABLE

ACTIVE LEVEL DATA	H = High Active Level L = Low Active Level	PRODUCT TERM INPUT DATA	H = Active High Input L = Active Low Input Blank = Don't Care Input	SUMMING DATA	A = Product Term is Summed by This Output Blank - Product Term is Not Summed by this Output

ACTIVE LEVEL DATA							
F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0

	PRODUCT TERM INPUT DATA														SUMMING DATA							
	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0
	PIN 11	PIN 10	PIN 9	PIN 8	PIN 7	PIN 6	PIN 5	PIN 4	PIN 3	PIN 2	PIN 1	PIN 23	PIN 22	PIN 21	PIN 20	PIN 19	PIN 18	PIN 17	PIN 16	PIN 15	PIN 14	PIN 13
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ACTIVE LEVEL DATA	H = High Active Level L = Low Active Level	PRODUCT TERM INPUT DATA	H = Active High Input L = Active Low Input Blank = Don't Care Input	SUMMING DATA	A = Product Term is Summed by This Output Blank - Product Term is Not Summed by this Output

ACTIVE LEVEL DATA							
F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0

	PRODUCT TERM INPUT DATA														SUMMING DATA							
	I_{13}	I_{12}	I_{11}	I_{10}	I_9	I_8	I_7	I_6	I_5	I_4	I_3	I_2	I_1	I_0	F_7	F_6	F_5	F_4	F_3	F_2	F_1	F_0
	PIN 11	PIN 10	PIN 9	PIN 8	PIN 7	PIN 6	PIN 5	PIN 4	PIN 3	PIN 2	PIN 1	PIN 23	PIN 22	PIN 21	PIN 20	PIN 19	PIN 18	PIN 17	PIN 16	PIN 15	PIN 14	PIN 13
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INTERSIL

IM6101 Programmable Interface Element (PIE)

FEATURES

- **Compatible with IM6100 Microprocessor**
- **Four Separate SENSE Input Lines to Sense the Status of Peripheral Devices**
- **Four Programmable OPERATE Control Lines for READ/WRITE on Peripheral Devices**
- **Four General Purpose FLAGS each of which is Programmable**
- **Chained Vectored Priority Interrupt Structure Possible**
- **Low Power: Less than 1mW @ 5V**
- **TTL Compatible at +5V**

FUNCTIONAL BLOCK DIAGRAM

PIN CONFIGURATION

FIGURE 1.

GENERAL DESCRIPTION

The IM6101 is a Programmable Interface Element (PIE) device designed for interfacing various peripheral chips such as UART's, FIFO's, Keyboard Scanner's to IM6100 Microprocessor. In this way, the IM6101 eliminates the need for additional external logic between 6100 μP and its peripherals.

The IM6101 provides the control signals to peripheral devices for READING or WRITING on the DX bus by activating the WRITE CNTRL and READ CNTRL lines with IOT (Input Output Transfer) instructions.

Each IM6101 can sample 4 status lines from peripheral devices. It can also generate interrupt requests to the μP if the corresponding individual interrupt enable bits in the PIE are enabled and the respective status lines become active.

The four FLAG lines may be set or reset under program control to send control information to the peripheral devices or to send binary data.

ORDERING INFORMATION

ORDER CODE	IM6101-1	IM6101A	IM6101
PLASTIC PKG.	IM6101-1IPL	IM6101-AIPL	IM6101-IPL
CERAMIC PKG.	IM6101-1IDL	IM6101-AIDL	—
MILITARY TEMP.	IM6101-1MDL	IM6101-AMDL	—
MILITARY TEMP. WITH 883B	IM6101-1 MDL/883B	IM6101-AMDL/ 883B	—

PACKAGE DIMENSIONS

40 PIN PLASTIC DUAL-IN-LINE PACKAGE (PL)

40 PIN CERAMIC DUAL-IN-LINE PACKAGE (DL)

NOTE: DIMENSIONS IN PARENTHESIS ARE METRIC

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IM6101 FUNCTIONAL DESCRIPTION

Pin Number	Symbol	Input/ Output	Description
1	V_{CC}		+5 volts
2	INTGNT	I	A high level on INTERRUPT GRANT inhibits recognition of new interrupt requests and allows the priority chain time to uniquely specify a PIE.
3	PRIN	I	A high level ON PRIORITY IN and an interrupt request will select a PIE for vectored interrupt.
4	SENSE 4	I	The SENSE input is controlled by the SL (sense level) and SP (sense polarity) bits of control register B. A high SL level will cause the SKIP flip flop to be set by a level while a low SL level causes sense and interrupt flip flops to be set by an edge. A high SP level will cause the sense flip flop to set by a positive going edge or high level. A high IE (interrupt enable) level generates an interrupt request whenever the INT flip flop is set (by an edge).
5	SENSE 3	I	See pin 4 — SENSE 4
6	SENSE 2	I	See pin 4 — SENSE 4
7	SENSE 1	I	See pin 4 — SENSE 4
8	SEL 3	I	Matching SELECT(3-7) inputs with PIE addressing on DX(3-7) during IOTA selects a PIE for programmed input output transfers.
9	SEL 4	I	See pin 8 — SEL 3
10	LXMAR	I	A positive pulse on LOAD EXTERNAL ADDRESS REGISTER loads address and control data from DX(3-11) into the address register.
11	SEL 5	I	See Pin 8 — SEL 3
12	SEL 6	I	See Pin 8 — SEL 3
13	XTC	I	The XTC input is a timing signal produced by the microprocessor. When XTC is high a low going pulse on DEVSEL initiates a "read" operation. When XTC is low, a low going pulse on DEVSEL initiates a "write" operation.
14	SEL 7	I	See Pin 8 — SEL 3
15	DX 0	I/O	Data transfers between the microprocessor and PIE take place via these input/output pins.
16	DX 1	I/O	See Pin 15 — DX 0
17	DX 2	I/O	See Pin 15 — DX 0
18	DX 3	I/O	See Pin 15 — DX 0
19	DX 4	I/O	See Pin 15 — DX 0
20	DX 5	I/O	See Pin 15 — DX 0
21	DX 6	I/O	See Pin 15 — DX 0
22	DX 7	I/O	See Pin 15 — DX 0
23	DX 8	I/O	See Pin 15 — DX 0
24	DX 9	I/O	See Pin 15 — DX 0
25	DX 10	I/O	See Pin 15 — DX 0
26	DX 11	I/O	See Pin 15 — DX 0
27	GND		
28	$\overline{DEVSEL}$	I	The DEVSEL input is a timing signal produced by the microprocessor during IOT instructions. It is used by the PIE to generate timing for controlling PIE registers and "read" and "write" operations.
29	FLAG 4	O	The FLAG outputs reflect the data stored in control register A. Flags (1-4) can be set or reset by changing data in CRA via a WRA (write control register A) command. FLAG1 and FLAG3 can be controlled directly by PIE commands SFLAG1, CFLAG1, SFLAG3 and CFLAG3.
30	FLAG 3	O	See Pin 29 — FLAG 4
31	FLAG 2	O	See Pin 29 — FLAG 4
32	FLAG 1	O	See Pin 29 — FLAG 4
33	$\overline{C1}$	O	The PIE decodes address, control and priority information and asserts outputs C1 and C2 during the IOTA cycle to control the type of data transfer. These outputs are open drain for bussing and require pullup resistors to V_{CC}. C1(L), C2(L) - vectored interrupt C1(L), C2(H) - READ1, READ3 or RRA commands C1(H), C2(H) - all other instructions
34	C2	O	See Pin 33 — C1
35	READ1	O	Outputs READ1 and READ2 are used to gate data from peripheral devices onto the DX bus for input to the IM6100. Note the data does not pass through the PIE.
36	WRITE1	O	Outputs WRITE1 and WRITE2 are used to gate data from the IM6100 DX bus into peripheral devices. Data does not pass through the PIE.
37	READ2	O	See Pin 35 — READ1
38	WRITE2	O	See Pin 36 — WRITE1
39	$\overline{SKP/INT}$	O	The PIE asserts this line low to generate interrupt requests and to signal the IM6100 when sense flip flops are set during SKIP instructions. This output is open drain.
40	POUT	O	A high level on priority out indicates no higher priority PIE interrupt requests are outstanding. This output is tied to the PRIN input of the next lower priority PIE in the chain.

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TIMING DIAGRAM

Timing for a typical IOT transfer is shown in Figure 2. During the IFETCH cycle, the processor obtains from memory an IOT instruction of the form 6XXX. During the IOTA the processor places that instruction back on the DX lines ③ and pulses LXMAR transferring address and control information for the IOT transfer to all peripheral devices. A low going pulse on $\overline{DEVSEL}$ while XTC is high ④ is used by the addressed PIE along with decoded control information to generate $\overline{C1}$, $\overline{C2}$, $\overline{SKP}$ and controls for data transfers to the processor. Control outputs READ1 and READ2 are used to gate peripheral data to the DX lines during this time. A low going pulse on $\overline{DEVSEL}$ while XTC is low ⑤ is used to generate WRITE1 and WRITE2 controls. These signals are used to clock processor accumulator data into peripheral devices.

FIGURE 2. IM6101 PIE Timing Diagram.

All PIE timing is generated from IM6100 signals LXMAR, $\overline{DEVSEL}$, and XTC. No additional timing signals, clocks, or one shots are required. Propagation delays, pulse width, data setup and hold times are specified for direct interfacing with the IM6100.

PIE ADDRESS AND INSTRUCTIONS

The IM6100 communicates with the PIE and with peripherals through the PIE via IOT commands. During the IOTA cycle (See Figure 1) an instruction of the form 6XXX is loaded into all PIE instruction registers. The bits are interpreted as shown below.

The 5 address bits (3-7) are compared with the select inputs SEL3, SEL4, SEL5, SEL6, SEL7 to address 1 of 31 possible PIE's. Address zero is reserved for IOT's internal to the IM6100. The four control bits are decoded to select one of 16 instructions. Note also that the IOT instructions 66XX are reserved for the Parallel Input/Output Port (P10 - IM6103).

FIGURE 3. PIE Instruction Format.

CONTROL	MNEMONICS	DESCRIPTION
0000 1000	READ1 READ2	The READ instructions generate a pulse on the appropriate read outputs. This signal is used by the peripheral device to gate data onto the DX bus to be "OR'ed" with the IM6100 accumulator data.
0001 1001	WRITE1 WRITE2	The WRITE instructions generate a pulse on the appropriate write output. This signal is used by peripherals to load the IM6100 accumulator data on the DX lines into peripheral data registers.
0010 0011 1010 1011	SKIP1 SKIP2 SKIP3 SKIP4	The SKIP instructions test the state of the sense flip flops. If the input conditions have set the sense flip flop, the PIE will assert the SKP/INT output causing the IM6100 to skip the next program instruction. The sense flip flop is then cleared. If the sense flip flop is not set, the PIE does not assert the SKP/INT output and the IM6100 will execute the next instruction.
0100	RCRA	The Read Control Register A instruction gates the contents of CRA onto the DX lines during time ④ to be "OR" transferred to the IM6100 AC. (See Figure 2)
0101 1101 1100	WCRA WCRB WVR	The Write Control Register A, Write Control Register B and Write Vector Register instructions transfer IM6100 AC data on the DX lines during time ⑤ of IOTA into the appropriate register. (See Figure 2) Bits 10, 11 of the VR;5, 7 of CRA; 8-11 of CRB are don't care bits for these instructions.
0110 1110	SFLAG1 SFLAG3	The SET FLAG instructions set the bits FL1 and FL3 in control register A to a high level. PIE outputs FLAG1 and FLAG3 follow the data stored in bits FL1 and FL3 of CRA.
0111 1111	CFLAG1 CFLAG3	The CLEAR FLAG instructions clear the bits FL1 and FL3 in control register A to a low level.
$(6007)_8$	CAF	IM6100 internal IOT instruction CLEAR ALL FLAGS clears the interrupt requests by clearing the sense flip flops. It has no effect on control register output flags FL1, FL2, FL3, FL4. To clear these output flags, bits 0-3 of CRA must be cleared using WCRA with bits 0-3 of AC cleared.

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PRIORITY FOR VECTORED INTERRUPT

A hardware priority network uniquely selects a PIE to provide a vectored address. *The first IOT command of any type,* after the IM6100 signal INTERRUPT GRANT goes high, resets the line INTGNT to a low level. The signal INTGNT is used to freeze the priority network and enable vector generation. Within a given PIE, the internal priority is interrogated during every LXMAR.

The highest priority PIE has PRIN tied to V_{CC}. The lowest priority PIE is the last one on the chain. The vector address generated by the PIE consists of 10 bits from the vector register and two bits that indicate the sense input within the highest priority PIE that generated the interrupt.

A. Daisy-chaining of several PIE chips.

B. Interrupt Vector Register Format.

0	1	2	3	4	5	6	7	8	9	10	11
INTERRUPT VECTOR										SPRI	

SPRI: Sense Priority

SPRI	Conditions*
00	SENSE1
01	SENSE2 and not SENSE1
10	SENSE3 and not (SENSE2 or SENSE1)
11	SENSE4 and not (SENSE3 or SENSE2 or SENSE1)

*All sense input lines are enabled for interrupts.

FIGURE 4. IM6101 Priority for Vectored Interrupt.

I/O CONTROL LINES (C1 AND C2)

The type of input-output transfer is controlled by the selected PIE by activating the $\overline{C1}$, $\overline{C2}$ lines as shown below. These outputs are open drain.

$\overline{C1}$	$\overline{C2}$	
H	H	DEV/PIE ← AC Write
L	H	AC ← AC + DEV/PIE "OR" Read
L	L	PC ← VECTOR ADDRESS Vectored Interrupt

INTERRUPT/SKIP (INT/SKP)

Interrupt and skip information are time multiplexed on the same lines. Since the IM6100 samples skip and interrupt data at separate times (see Figure 1) there is no degradation in system performance. The PIE samples the sense flip flops and generates an interrupt request for enabled bits on the rising edge of LXMAR. Interrupt requests are asserted by driving the $\overline{INT/SKP}$ line low. During IOTA of SKIP instructions the INT/SKP reflects the SENSE flip flop data.

If the SENSE flip flop is set, the INT/SKP line is driven low to cause the IM6100 to skip the next instruction. This output is open drain.

CONTROL REGISTER A (CRA)

The CRA can be read and written by the IM6100 via the RCRA and WCRA commands. The format and meaning of control bits are shown below.

0	1	2	3	4	5	6	7	8	9	10	11
FL4	FL3	FL2	FL1	WP2	*	WP1	*	IE4	IE3	IE2	IE1

* Don't care for WCRA, 0 for RCRA

FIGURE 5. Format for Control Register A.

FL(1-4)

Data on FLAG outputs corresponds to data in FL (1-4). Changing the FL bits in CRA changes the corresponding FLAG output.

WP(1,2)

A high level on WRITE POLARITY bits causes positive pulses at the WRITE outputs (see Figure 1).

IE(1-4)

A high level on INTERRUPT ENABLE enables interrupts.

CONTROL REGISTER B

The CRB can be written by the IM6100 via the WCRB instruction. It has no read back capability. The format and meaning of control bits are shown below. Bits 8-11 are don't care bits.

0	1	2	3	4	5	6	7
SL4	SL3	SL2	SL1	SP4	SP3	SP2	SP1

FIGURE 6. Format for Control Register B.

SL(1-4)

A high level on the SENSE LEVEL bits causes the SENSE inputs to be level sensitive. A low level on the SL bits causes the SENSE inputs to be edge sensitive. The INT FFs are set only if a sense line is set up to be edge sensitive.

SP(1-4)

A high level on the SENSE POLARITY bits causes the SKIP flip flop to be set by a high level or positive going edge. A low level causes the SKIP flip flop to be set by a low level or negative going edge.

PERIPHERAL INTERFACE LINES

SENSE(1-4)

The IM6101 has two latches associated with each sense input — a SKIP flip flop and an INTERRUPT flip flop.

For the Interrupt flip flop to be set, the corresponding interrupt enable bit must be set to 'one'. If the sense input is programmed to be edge sensitive, the flip flop is set when the edge occurs. If it was initially programmed to be level sensitive and then the mode is changed to be edge sensitive, the flip flop will be set if the polarity of sense input line corresponds to its SP bit.

All conditions that set the Interrupt flip flop also set the associated Skip flip flop. In addition, the Skip flip flop is set when the polarity of the sense input corresponds to its SP bit in the level sensitive mode.

The Skip flip flop is cleared at IOTA READ time by executing a CAF (6007) instruction or a SKIP instruction on the associated sense input that actually skips. In the level sensitive mode, whenever the polarity of sense input does not correspond to its SP bit, the sense FF is cleared.

The Interrupt flip flop is cleared whenever the sense flip flop is cleared. In addition, it is cleared if the associated sense logic actually creates a vector, the interrupt enable bit is cleared to a 'zero' or the sense input is programmed to be level sensitive. Detailed operation of resetting Interrupt and Skip flop flops are as shown in Figure 7.

Figure 7. IM6101 SKIP Flip Flop and INTERRUPT Flip Flop Input Diagram.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6101A ..... -40°C to +85°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... 4.0V to 11.0V
Supply Voltage ..... +12.0V
Voltage On Any Input or
Output Pin ..... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, T_A = -40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage	$GND \le V_{IN} \le V_{CC}$	-1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = 0mA	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0mA			GND+0.01	V
6	I_{OL}	Output Leakage	$GND \le V_{OUT} \le V_{CC}$	-1.0		1.0	μA
7	I_{CC}	Power Supply Current—Standby	V_{CC}=10V±5%		1.0	500	μA
8	I_{CC}	Power Supply Current—Dynamic	V_{CC}=10V±5% f=571 kHz			2.0	mA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ±5%, T_A = -40°C to +85°C, C_L = 50pF

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{DR}	Delay from DEVSEL to READ			150	ns
2	t_{DW}	Delay from DEVSEL to WRITE	50		150	ns
3	t_{DF}	Delay from DEVSEL to FLAG			200	ns
4	t_{DC}	Delay from DEVSEL to C1, C2			215	ns
5	t_{DI}	Delay from DEVSEL to SKP/INT			215	ns
6	t_{DA}	Delay from DEVSEL to DX			215	ns
7	t_{LXMAR}	LXMAR Pulse Width	120			ns
8	t_{AS}	Address Setup Time	40			ns
9	t_{AH}	Address Hold Time	50			ns
10	t_{DS}	Data Setup Time	65			ns
11	t_{DH}	Data Hold Time	50			ns

Note: See Figure 2 for an A.C. Timing Diagram.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6101-1I ..... -40°C to +85°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... 4.0V to 7.0V
Supply Voltage ..... +8.0V
Voltage On Any Input or
Output Pin ..... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage	GND≤V_{IN}≤V_{CC}	-1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = -0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OL}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	μA
7	I_{CC}	Power Supply Current—Standby	V_{CC} = 5V ± 10%		1.0	100	μA
8	I_{CC}	Power Supply Current—Dynamic	V_{CC}=5V±10% f=330 kHz			500	μA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -40°C to +85°C, C_L = 50pF

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{DR}	Delay from DEVSEL to READ			300	ns
2	t_{DW}	Delay from DEVSEL to WRITE	100		300	ns
3	t_{DF}	Delay from DEVSEL to FLAG			375	ns
4	t_{DC}	Delay from DEVSEL to C1, C2			460	ns
5	t_{DI}	Delay from DEVSEL to SKP/INT			460	ns
6	t_{DA}	Delay from DEVSEL to DX			460	ns
7	t_{LXMAR}	LXMAR Pulse Width	240			ns
8	t_{AS}	Address Setup Time	80			ns
9	t_{AH}	Address Hold Time	125			ns
10	t_{DS}	Data Setup Time	80			ns
11	t_{DH}	Data Hold Time	100			ns

Note: See Figure 2 for an A.C. Timing Diagram.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Military IM6101AM ..... -55°C to +125°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... 4.0V to 11.0V
Supply Voltage ..... +12.0V
Voltage On Any Input or
Output Pin ..... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, T_A = -55°C to +125°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage	$GND \le V_{IN} \le V_{CC}$	-1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = 0mA	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0mA			GND+0.01	V
6	I_{OL}	Output Leakage	$GND \le V_{OUT} \le V_{CC}$	-1.0		1.0	μA
7	I_{CC}	Power Supply Current—Standby	V_{CC}=10V±5%		1.0	500	μA
8	I_{CC}	Power Supply Current—Dynamic	V_{CC}=10V±5% f=571 kHz			2.0	mA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, T_A = -55°C to +125°C, C_L = 50pF

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{DR}	Delay from DEVSEL to READ			165	ns
2	t_{DW}	Delay from DEVSEL to WRITE	50		165	ns
3	t_{DF}	Delay from DEVSEL to FLAG			220	ns
4	t_{DC}	Delay from DEVSEL to C1, C2			240	ns
5	t_{DI}	Delay from DEVSEL to SKP/INT			240	ns
6	t_{DA}	Delay from DEVSEL to DX			240	ns
7	t_{LXMAR}	LXMAR Pulse Width	135			ns
8	t_{AS}	Address Setup Time	45			ns
9	t_{AH}	Address Hold Time	55			ns
10	t_{DS}	Data Setup Time	70			ns
11	t_{DH}	Data Hold Time	55			ns

Note: See Figure 2 for an A.C. Timing Diagram.

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Military IM6101-IM ..... -55°C to +125°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... 4.0V to 7.0V
Supply Voltage ..... +8.0V
Voltage On Any Input or
Output Pin ..... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage	$GND \leq V_{IN} \leq V_{CC}$	-1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = -0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OL}	Output Leakage	$GND \leq V_{OUT} \leq V_{CC}$	-1.0		1.0	μA
7	I_{CC}	Power Supply Current—Standby	V_{CC} = 5V ± 10%		1.0	100	μA
8	I_{CC}	Power Supply Current—Dynamic	V_{CC}=5V±10% f=330 kHz			500	μA
9	C_{IN}	Input Capacitance			7.0	8.0	pF
10	C_O	Output Capacitance			8.0	10.0	pF

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -55°C to +125°C, C_L = 50pF

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{DR}	Delay from DEVSEL to READ			330	ns
2	t_{DW}	Delay from DEVSEL to WRITE	100		330	ns
3	t_{DF}	Delay from DEVSEL to FLAG			415	ns
4	t_{DC}	Delay from DEVSEL to C1, C2			510	ns
5	t_{DI}	Delay from DEVSEL to SKP/INT			510	ns
6	t_{DA}	Delay from DEVSEL to DX			510	ns
7	t_{LXMAR}	LXMAR Pulse Width	265			ns
8	t_{AS}	Address Setup Time	90			ns
9	t_{AH}	Address Hold Time	140			ns
10	t_{DS}	Data Setup Time	80			ns
11	t_{DH}	Data Hold Time	110			ns

Note: See Figure 2 for an A.C. Timing Diagram.

APPLICATION

INTRODUCTION

The IM6101, Programmable Interface Element (PIE), provides a universal means of interfacing industry standard LSI devices and peripheral equipment controllers to the IM6100 Microprocessor.

The IM6100 configures each PIE for a specific interface during system initialization by programming the control registers within the PIE for write enable polarities, sense polarities, sense edges or levels, flag values and interrupt enables. On power-up, the registers will contain random bit patterns.

The data transfer between the IM6100 and the peripheral devices does not take place through the PIE. The programmable Interface Element provides the steering signals for data transfers. This approach was chosen since all the standard LSI elements such as Keyboard chips, UARTs, FIFOs, etc. have internal storage latches and they require only control signals to take data from the bus or to put data on the bus. If some user defined peripheral interfaces do not have these built-in storage elements, discrete CMOS or low power Schottky latches, or flip-flops, must be provided to store the data from the IM6100 until the peripheral device is ready to accept it and to latch data from the peripheral devices until the IM6100 asks for it.

INTERRUPT PROCESSING WITH PIE'S

The PIEs provide for a vectored priority interrupt scheme. Up to 31 PIEs may be chained to obtain 124 interrupt lines. The microprocessor will recognize, identify and start servicing the highest priority interrupt request within 36.6μs at 3.3MHz.

The INTREQ lines from all PIEs are wire-ANDed together. A PIE generates an interrupt request, if any one of its four sense lines, which are interrupt enabled, become active by driving the INTREQ line to the IM6100 low. If no higher priority requests are outstanding (RESET, CPREQ, HLT or DMAREQ), the IM6100 will grant the request at the end of the current instruction. The content of the Program Counter is deposited in location 0000_8 of the memory and the program fetches the next instruction from location 0001_8. The return address is hence available in location 0000_8. This address must be saved in a software stack if nested interrupts are allowed.

The IM6100 activates the INTGNT signal high when an INTREQ is acknowledged. The INTGNT is reset by executing any IOT instruction. The PIEs use the INTGNT signal to freeze the priority network and to uniquely specify the PIE with the highest priority interrupt request. The PIE with the highest priority request sends a unique vector address to the IM6100 when the processor executes the first IOT instruction after the INTGNT. The Interrupt II Prototyping System uses the IOT instruction VECT (6047) for Vectoring.

The 12-bit vector address generated by the PIE consists of 10 high order bits from the vector register, defined by the user during system initialization, and two low order bits which indicate the sense input that generated the interrupt. Therefore, if the instruction in location 0001_8 is VECT-6047_8, the processor will branch to 1 of 4 locations, depending on which of the sense lines within a PIE generated the request. Each one of these locations must contain a Jump instruction pointing to the specific service routine for the corresponding sense input. The 36.6μs interrupt acknowledge time at 3.3 MHz consists of 17μs (max) to recognize an interrupt request, 3.6μs to grant an interrupt request, 10μs to execute the VECT for vectoring and 6.0μs to execute a Jump instruction to a specific service routine.

Proper vectoring requires the following conditions:

1. The IM6100 must be enabled for interrupts with the ION command.
2. The INTGNT output of the IM6100 must be connected to the INTGNT of all the PIEs and the PRIN of the PIE with the highest priority must be connected to VCC and its PROUT should be connected to the PRIN of the PIE with the next highest priority and so on.
3. The IE bit of the sense line that is expected to generate the interrupt must be set to 1.
4. The sense line must be programmed to be edge sensitive. If a sense line is programmed to be level sensitive, it will not generate an INTREQ nor will it generate a vector.
5. The vector register of the PIE must be initialized with the proper vector. Note that the two least significant bits are generated by the PIE itself.
6. The $\overline{C1}$ and $\overline{C2}$ lines of all the PIEs must be wired together with the $\overline{C1}$ and $\overline{C2}$ of the IM6100 and pull up resistors must be provided on these lines since the PIE $\overline{C1}$ and $\overline{C2}$ outputs are open drain. The $\overline{SKP/INT}$ line of the PIE must be wired with the INT and SKP lines of the IM6100. If the PIE DX lines are buffered, the external bus must be enabled onto the PIE DX with the XTB being active high and the PIE DX bus must be enabled onto the external bus when the C1 line of a PIE is active low (during RCRA, READ1, READ2 or vector).
7. The vector address will be generated with the first IOT of any kind after the INTGNT.
8. Note also that a successful skip on a sense line will reset an interrupt request by the sense line, if any. One should not thus turn on the interrupt system after a successful skip on a sense line expecting that the sense line that was just tested will generate a request.

SKIP HANDLING WITH PIE'S

Each PIE provides for four SENSE lines. The active state of the SENSE inputs can be programmed to be a low level, high level, positive edge or negative edge. There is a SENSE FF in the PIE associated with each SENSE line. This FF is set when the SENSE line is "active"

The state of the SENSE FF can be tested by the SKP commands. When the IM6100 executes a SKIP instruction, it will skip the next sequential instruction if the SENSE FFi is set. If the skip is successful, the FF will be cleared.

If the sense line was set up to be edge sensitive, it can, therefore, be tested for the 'set' state only once. If the FF is set by a level, it will be cleared by the successful skip and then, set immediately by the active level.

If the SENSE FF was set by an edge, and the respective IE bit is enabled, the PIE will generate an INTREQ to the IM6100. Provided the priority conditions are met, the PIE will supply the vector address to the IM6100 when it executes the first IOT instruction of any kind, after the INTREQ has been granted. If the vector address is generated by FFi, one may still skip once on sense line i.

It should be noted that if priority vectoring is inhibited by grounding PRIN, an INTREQ will be cleared only if a SKIPi instruction is executed to test the FFi that generated the request. Note also that an INTREQ will not be generated if the sense line was set up to be level sensitive.

In certain instances, one may be interested in restoring the set state of a SENSE FF after it has been successfully tested and cleared and if the SENSE line has been programmed to be edge sensitive. For example, assume that SENSE1 is programmed to be positive edge sensitive (SL1 = 0, SP1 = 1). The transition from a 0 to 1 occurred; SENSE FF1 is set; SENSE1 is at a 1 level. SKIP1 instruction will clear SENSE FF1. The SENSE FF1 can be set, under program control, by creating an internal edge. This is accomplished, in this specific instance, by programming SP1 to a 0 and then back to a 1. Since SP1 is in CRB and it cannot be read from the PIE, the CRB constant must be stored in user memory, for example, location KCRB.

```
CLA
TAD KCRB     /Get CRB constant
AND K7740    /SP1 = 0
WCRB         /Write CRB to clear SP1
TAD K0020    /SP1 = 1
WCRB         /Write CRB to set SP1

KCRB, CRB    /CRB constant
K7740, 7740
K0020, 0020
```

Software systems employing Skip's on a Sense input while allowing the same input to create an Interrupt should pay attention to the fact that the Skip and Interrupt flip flops are synchronized by LXMAR from the IM6100. Since there is no LXMAR during IOTB of an I/O instruction, the following can occur. Assume that the following two instruction sequence is used:

```
SKIP SENSEX     /SENSE F/F SET?
JMP  -1         /NO: WAIT FOR IT
```

Where SENSEX is also Interupt enabled.

Now, assume that the appropriate 'Edge' occurs during the fetch state of the Skip instruction. The Edge causes both flip flops to be set and the LXMAR produced at IOTA time creates an Interrupt request. The Skip instruction execution causes a Skip and clears the Skip flop flop. However, the Interrupt flip flop will not reflect the fact that the Skip flip flop has been cleared until after the next LXMAR occurs. So, the Interrupt request remains active during IOTB time since the IOTB cycle does not have a LXMAR. The IM6100 honors the Interrupt request since the next LXMAR doesn't occur until after the IOT is finished. The Interrupt servicing routine will not Skip again if it tries to find the device that created the Interrupt. Note that the proper Vector Address will still be generated.

PIE INSTRUCTION FORMAT

The IM6100 communicates with the PIEs using the Input-Output Transfer (IOT) instructions. The first three bits, 0-2, are always set to 6_8 (110) to specify an IOT instruction. The standard PDP-8/E™ convention is to set the next 6 bits, 3-8, to specify 1 of 64 I/O devices and then to control the operation of the selected I/O device by using bits 9-11. However, the PDP-8/E interfaces are not standardized since a specific pattern of bits 9-11 could specify completely different operations in different I/O devices. For example, the pattern 000 in bits 9-11 could mean a read operation for Interface A, a write operation for Interface B, a skip instruction for Interface C and so on since the operation for any IOT instruction depends entirely upon the circuitry designed into the I/O device interface.

The IOT instruction format for the PIE is different from that used by PDP-8/E™ interfaces. The first three bits are, as usual, set to 6_8 to indicate an IOT instruction. The next 5 bits, 3-7, specify 1 of 31 PIEs and then the operation of the selected PIE is controlled by bits 8-11 in 16 uniquely specified ways. For example, the specific pattern 0000 in bits 8-11 means exactly the same operation for all PIEs, namely activate READ1 line.

Of the 32 possible combinations of bits 3-7, the pattern 00000 is reserved for internal Processor IOT instructions and hence not available as a PIE address.

Recommended address assignments for the IM6101-PIE (Programmable Interface Element) are as follows:

000	00	Internal IOT (600X) and DEC HS RDR (601X)
000	01	DEC HS PUNCH (602X) and DEC TTY Keyboard (603X)
000	10	DEC TTY PRINTER (604X)
000	11	INTERCEPT PIE-UART Serial Interface
001	00	INTERCEPT PIE-UART PRINTER Interface
001	01	IM6102-MEDIC REAL TIME CLOCK
001	10	Reserved for Intercept Option - 1
001	11	Reserved for Intercept Option - 2
010	00	IM6102-MEDIC EMC/DMA
010	01	IM6102-MEDIC EMC/DMA
010	10	IM6102-MEDIC EMC/DMA
010	11	IM6102-MEDIC EMC/DMA
011	00	IM6103-PIO
011	01	IN6103-PIO
011	10	IN6103-PIO
011	11	IN6103-PIO
100	00	USER
100	01	USER
100	10	USER
100	11	USER
101	00	USER
101	01	USER
101	10	USER
101	11	USER
110	00	USER
110	01	USER
110	10	USER
110	11	USER
111	00	Reserved for Intercept Option - 5
111	01	Reserved for Intercept Option - 4
111	10	Intercept FLOPPY DISK System (675X)
111	11	Reserved for Intercept Option - 3

PARAMETER	DEFINITION
Minimum Peripheral device write data setup time w.r.t. leading edge of WRITE	t_{WPD} (IM6100) + $t_{DW\ (MIN)}$ (IM6101) - t_{DSD} (IM6100)
Minimum Peripheral device write data hold time w.r.t. leading edge of WRITE	t_{DHD} (IM6100) + t_{WPD} (IM6100) - $t_{DW\ (MAX)}$ (IM6101)
Maximum Peripheral device read data enable time	t_{END} (IM6100) - t_{DR} (IM6101)

TIMING REQUIREMENTS ON PERIPHERAL DEVICES

The timing required on peripheral devices is affected by the combined delays of the IM6100 and IM6101 devices. The table above describes the peripheral device timing requirements with respect to the data given for the IM6100 and IM6101 AC characteristics.

The values at any operating frequency, temperature and/or power supply voltage can be evaluated by substituting the calculated values for the IM6100 and IM6101 parameters in the defining expressions.

ASYNCHRONOUS SERIAL INTERFACE WITH PIE AND UART

The IM6402/03 Universal Asynchronous Receiver/Transmitter is a general, purpose programmable serial device for interfacing an asynchronous serial data channel to a parallel synchronous data channel. The receiver converts a serial word with start, data, parity and stop bits to a parallel data word and checks for parity, framing and data overrun errors. The transmitter section converts a parallel data word into a serial word with start, data, parity and stop bits. The data word length may be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The number of stop bits may be 1 or 2 or 1 1/2 when transmitting a 5 bit code.

The IM6402/03 can be used in a wide variety of applications including interfacing modems, Teletype™ and remote data acquisition systems to the IM6100 microprocessor. The IM6403 makes provisions for a crystal oscillator and internal divider chain to specify the data transfer rate. In the IM6402 the data transfer rate is controlled by an external timing source, for example, a Baud Generator.

A functional block diagram of the PIE/UART/IM6100 interface is shown below. The UART is configured, in this specific example, to interface with an ASR-33 Teletype which has a data format that consists of 11 bits — a start bit, 8 data bits and 2 stop bits. The UART is clocked at 16X the data rate. For the 10 character per second ASR-33, the UART clock frequency would be 1.76 KHz.

An 8-bit data word from the IM6100 Accumulator is loaded into the Transmitter Buffer Register via inputs TBR8-TBR1 when the Transmit Buffer Register Load (TBRL) signal makes a zero to one transition. A high level on Transmit Buffer Register Empty (TBRE) indicates that the buffer is ready to accept a new character for transmission. The microprocessor checks the status of TBRE via SENSE2 before it transmits a new character to the UART by pulsing WRITE1. The start bit, data bits and stop bits appear serially at the Transmit Register Output (TRO).

A serial data stream on the Receiver Register Input (RRI) is clocked into the Receive Buffer Register. A high level on Data Received (DR) indicates that a character has been received. The contents of Receiver Buffer Register appear on the outputs RBR8-RBR1 when a low level is applied to Receiver Register Disable (RRD) input. The RBR outputs are tristated when RRD is high. A low level on Data Received Reset (DRR) clears the DR flag. RRD and DRR

PIE/UART/IM6100 INTERFACE

may be tied together to clear DR as the register data is being read. The microprocessor monitors the status of the DR flag via SENSE1 to see if a new character has been received before it reads the information stored in the buffer register by pulsing READ1 low.

The UART interface uses only the low order 8 bits of the IM6100 data bus (DX) to receive and transmit characters.

The NAND gate is used to load the UART with the leading edge of the WRITE pulse since the IM6100 data is valid only with respect to the leading edge at higher operating frequencies.

PIE CONTROL REGISTER ASSIGNMENTS FOR IM6402 UART INTERFACE:

	0	1	2	3	4	5	6	7	8	9	10	11
CRA	*	*	*	*	*	*	WP1	*	*	*	IE2	IE1

	0	1	2	3	4	5	6	7
CRB	*	*	SL2	SL1	*	*	SP2	SP1

WP1 = 0	Active low WRITE1 (TBRL)
IE2 = 1	Interrupt enable for SENSE2 (TBRE)
IE1 = 1	Interrupt enable for SENSE1 (DR)
	If vectored interrupts are used (PIN = 1 or is part of a priority chain) the Interrupt Vector Register must be loaded with the desired vector address.
SL2 = 0; SP2 = 1	SENSE2 (TBRE) active on 0 to 1 transition
SL1 = 0; SP1 = 1	SENSE1 (DR) active on 0 to 1 transition

PIE ADDRESS AND CONTROL ASSIGNMENTS:

EXTERNAL COMMANDS	OCTAL CODE	DESCRIPTION
0 1 2 3 4 5 6 7 8 9 10 11 1 1 0 | 0 1 1 1 0 | 0 0 0 0 IOT Address READ1	6340	Activate RRD low to transfer Receiver Register contents onto the DX lines and clear the Data Received Flag.
1 1 0 | 0 1 1 1 0 | 0 0 0 1 WRITE1	6341	Activate TBRL low to transfer data from the DX lines to the Transmit Buffer Register.
1 1 0 | 0 1 1 1 0 | 0 0 1 0 SKIP1	6342	Skip the next instruction if the internal SENSE FF1 was set by a positive transition on Data Received (DR) and then clear SENSE FF1.
1 1 0 | 0 1 1 1 0 | 0 0 1 1 SKIP2	6343	Skip the next instruction if the internal SENSE FF2 was set by a positive transition on Transmit Buffer Register Empty (TBRE) and then clear Sense FF2.

INTERNAL COMMANDS	OCTAL CODE	DESCRIPTION
0 1 2 3 4 5 6 7 8 9 10 11 1 1 0 | 0 1 1 1 0 | 0 1 0 0 IOT Address RCRA	6344	'OR' transfer Control Register A to the AC.
1 1 0 | 0 1 1 1 0 | 0 1 0 1 WCRA	6345	Transfer AC to Control Register A
1 1 0 | 0 1 1 1 0 | 1 1 0 1 WCRB	6355	Transfer AC to Control Register B
1 1 0 | 0 1 1 1 0 | 1 1 0 0 WVR	6354	Transfer AC (0-9) to Vector Register (0-9)

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PIE Address and Control Assignments:

EXTERNAL COMMANDS	OCTAL CODE	DESCRIPTION
0 1 2 3 4 5 6 7 8 9 10 11 1 1 0 | 1 0 1 0 0 | 0 0 1 0 IOT Address SKIP1	6502	Skip and clear if SENSE1 is low — used to detect the status of the receive line.
1 1 0 | 1 0 1 0 0 | 0 1 1 0 SFLAG1	6506	Set FLAG1 to put the transmit line high ("MARK")
1 1 0 | 1 0 1 0 0 | 0 1 1 1 CFLAG1	6507	Clear FLAG1 to put the transmit line low ("SPACE")
1 1 0 | 1 0 1 0 0 | 1 1 1 0 SFLAG3	6516	Set FLAG3 to enable the paper tape reader
1 1 0 | 1 0 1 0 0 | 1 1 1 1 CFLAG3	6517	Clear FLAG3 to disable the paper tape reader

INTERNAL COMMANDS	OCTAL CODE	DESCRIPTION
0 1 2 3 4 5 6 7 8 9 10 11 1 1 0 | 1 0 1 0 0 | 0 1 0 0 IOT Address RCRA	6504	'OR' transfer Control Register A to AC
1 1 0 | 1 0 1 0 0 | 0 1 0 1 WCRA	6505	Transfer AC to Control Register A
1 1 0 | 1 0 1 0 0 | 1 1 0 1 WCRB	6515	Transfer AC to Control Register B
1 1 0 | 1 0 1 0 0 | 1 1 0 0 WVR	6514	Transfer AC (0-9) to Vector Register (0-9)

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Subroutines for programmed IOT transfers:

Program Listing:

```
                        /REFER TO THE APPLICATION BULLETIN M008
                         /"ROM BASED SUBROUTINE CALLS WITH THE
                         /IM6100" FOR THE IMPLEMENTATION OF A
                         /SOFTWARE STACK. THE ROUTINES IN THIS
                         /NOTE ASSUME THAT THE SUBROUTINES
                         /ARE RESIDENT IN RAM AND ARE CALLED BY
                         /THE CONVENTIONAL JMS INSTRUCTION.

                        *3200

                        /INPUT-OUTPUT ROUTINES FOR UART
                         /INPUT ROUTINE READS AN 8-BIT CHAR
                         /FROM THE UART INTO THE AC RIGHT
                         /JUSIFIED. THE OUTPUT ROUTINE XMTS
                         /A CHAR FROM THE AC TO THE UART AND
                         /THEN CLEARS THE AC.
                                /USER DEFINED MNEMONICS
                                RUART=6340        /READ UART DATA
                                WUART=6341        /WRITE UART

                                SKPDR=6342        /SKP IF DATA RECD
                               SKPTBR=6343        /SKP IF XMT RDY

3200  0000  INPUT,  0                             /ENTRY FOR SUBROUTINE
3201  6342           SKPDR
3202  5201           JMP .-1                      /WAIT FOR DATA READY

3203  7200           CLA
3204  6340           RUART                        /AC<= UART
3205  0207           AND K0377                    /STRIP 0-3
3206  5600           JMP I INPUT                  /RETURN

3207  0377  K0377,   0377


3210  0000  OUTPUT,  0
3211  6343           SKPTBR
3212  5211           JMP .-1                      /WAIT FOR XMT RDY

3213  6341           WUART
3214  7200           CLA                          /WRITE UART & CLA
3215  5610           JMP I OUTPUT                 /RETURN
```

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TELETYPE INTERFACE WITH PIE

A simple economical program controlled serial interface for a Teletype can be built using only the Programmable Interface Element. The interface uses one Sense line to receive serial data, one Flag line to transmit serial data and one Flag line to control the Teletype paper tape reader, as shown below. Timing for proper transmit pulse widths, setting and clearing FLAG1, and proper receiver sampling times, testing SENSE1, is created via software timing loops.

PIE Control Register Assignments

	0	1	2	3	4	5	6	7	8	9	10	11
CRA	•	•	•	•	•	•	•	•	•	•	•	•

	0	1	2	3	4	5	6	7
CRB	•	•	•	SL1	•	•	•	SP1

SL1 = 1; SP1 = 0 SENSE1 is level sensitive and active low.

IM6100/PIE/TELETYPE INTERFACE

Subroutines for programmed IOT transfers:

Transmit character routine:

The transmit routine takes an 8-bit character from the Accumulator and transmits it to the Teletype via FLAG1. FLAG1 is initially set high or "mark". For each character, the program sends out a start bit ("space" - zero), 8 data bits with the least significant bit first and 2 stop bits ("mark" - one).

Program listing:

```
                        /TELETYPE XMT ROUTINE
                         /FLAG1 IS INITIALISED TO 1(MARK)
                         /CHAR TO BE XMTED IN AC4-11
                         /NOMINAL BIT TIME 9.09 MS
                         /4MHZ OPERATION FOR IM6100
                         /AC AND L CLEARED AFTER XMT

                                /USER DEFINED MNEMONICS

                                TMARK=6506        /XMT MARK (1)
                                TSPACE=6507       /XMT SPACE(0)

                        *3000

3000  0000  XMT,        0
3001  3160              DCA TEMP1         /SAVE AC
3002  1235              TAD M8
3003  3161              DCA TEMP2         /-8 IN TEMP2
3004  1160              TAD TEMP1         /RESTORE AC

3005  6507              TSPACE            /START BIT
3006  4225              JMS DELAY         /TIME OUT BIT

                                /XMT 8 DATA BITS LSB FIRST
3007  7010  LOOP,        RAR               /XMT BIT IN L
3010  7430              SZL
3011  5214              JMP .+3           /JMP IF 1

3012  6507              TSPACE            /XMT 0
3013  7410              SKP

3014  6506              TMARK             /XMT 1

3015  4225              JMS DELAY         /TIME OUT BIT
                                          /9.082 MS NOMINAL <.1% ERROR

3016  2161              ISZ TEMP2
3017  5207              JMP LOOP          /XMT 8 BITS

3020  6506              TMARK             /STOP BIT
3021  4225              JMS DELAY
3022  4225              JMS DELAY         /2 STOP BITS

3023  7300              CLA CLL
3024  5600              JMP I XMT         /RETURN

3025  0000  DELAY,       0000              /9.043 MS
3026  3160              DCA TEMP1         /SAVE AC
3027  1236              TAD M693
3030  3162              DCA TEMP3         /-693 IN TEMP3
3031  1160              TAD TEMP1         /RESTORE AC

3032  2162              ISZ TEMP3
3033  5232              JMP .-1           /TIME OUT LOOP
                                          /9.009 MS

3034  5625              JMP I DELAY       /RETURN

3035  7770  M8,         7770
3036  6513  M693,       6513

                        *160
0160  0000  TEMP1,      0000
0161  0000  TEMP2,      0000
0162  0000  TEMP3,      0000
```

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Receiver character routine:

The receive routine accepts a serial data string from the Teletype which consists of a start bit, 8 data bits with the least significant bit first and 2 stop bits and assembles them, right justified, into an 8-bit word in the Accumulator. Each bit is sampled in the middle of the bit interval. The user can read character by character from the Teletype reader by turning the reader off after receiving each character and then reenabling it under program control to fetch the next character in sequence The routine assumes that the program is waiting for a character from the Teletype.

Program listing:

```
                        *3100
                        /TELETYPE RECEIVE ROUTINE
                         /SENSEI IS INITIALISED TO BE LEVEL
                                /SENSITIVE AND ACTIVE LOW
                         /AC AND L ARE CLEARED. CHAR IN AC 4-11

                                /USER DEFINED MNEMONICS

                                SKPLOW=6502      /SKP IF TTY IN IS 0
                                RDRON=6516       /ENABLE RDR
                                RDROFF=6517      /RDR OFF

3100  0000  RCVE,   0000
3101  7300          CLA CLL
3102  1235          TAD M8
3103  3161          DCA TEMP2        /-8 IN TEMP2

3104  6516          RDRON            /ENABLE RDR

3105  6502  START,  SKPLOW
3106  5305          JMP .-1          /WAIT FOR START BIT

3107  1330          TAD M349
3110  3162          DCA TEMP3        /-349 IN TEMP3

3111  2162          ISZ TEMP3
3112  5311          JMP .-1          /1/2 BIT DELAY
                                     /4.532 MS

3113  6502          SKPLOW
3114  5305          JMP START        /FALSE START BIT

3115  6517          RDROFF           /GOOD START BIT
                                     /TURN OFF RDR
3116  4225  DATA,   JMS DELAY        /FULL BIT DELAY TO THE
                                     /MIDDLE OF NEXT BIT
                                     /<.15% ERROR

3117  7100          CLL
3120  6502          SKPLOW
3121  7020          CML              /L=1 IF MARK
3122  7010          RAR

3123  2161          ISZ TEMP2
3124  5316          JMP DATA         /RCVE 8 BITS

3125  7012          RTR
3126  7012          RTR              /RIGHT JUSIFY

3127  5700          JMP I RCVE       /RETURN

3130  7243  M349,   7243
```

7

INTERSIL

IM6102 Memory Extension/ DMA Controller/ Interval Timer (MEDIC)

FEATURES

- **Provides Extended Memory Address to 32K Words**
- **Simultaneous DMA — Provides Simultaneous DMA Channel that Uses DX Bus During Second Half of a Cycle to Access Memory**
- **DMA Channel Can be Used for Dynamic RAM Refresh**
- **12-Bit Programmable Interval Timer**
- **Direct Interface with IM6100 Microprocessor Via Bidirectional DX Bus and Handshake Lines**
- **Hardware Reset**
- **28 Different I/O Instructions**

GENERAL DESCRIPTION

The IM6102 is a multi-function peripheral controller chip incorporating functions such as memory extension, direct memory access control, and a programmable real time clock.

The IM6102 provides necessary control to address up to 32K words of memory, and its DMA channel can be used with Dynamic RAM Components for "transparent refresh". The programmable real time clock is 12-bit long, and its output frequency can be programmed for 5 decades.

It features a high degree of system integration, putting into one chip all the functions which are normally available in three or more LSI circuits. As a result of this large integration, the user can design and produce a compact microcomputer with minicomputer performance.

PIN CONFIGURATION

ORDERING INFORMATION

ORDER CODE	IM6102-1	IM6102A	IM6102
PLASTIC PKG.	IM6102-1IPL	IM6102-AIPL	IM6102-IPL
CERAMIC PKG	IM6102-1IDL	IM6102-AIDL	—
MILITARY TEMP.	IM6102-1MDL	IM6102-AMDL	—
MILITARY TEMP. WITH 883B	IM6102-1 MDL/883B	IM6102-AMDL/ 883B	—

PACKAGE DIMENSIONS

NOTE: DIMENSIONS IN PARENTHESIS ARE METRIC

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IM6102 FUNCTIONAL PIN DESCRIPTION

Pin Number	Symbol	Input/ Output	Description
1	V_{CC}		Supply voltage
2	$\overline{DMAEN}$	I	Enable the IM6102 DMA channel to transfer data
3	DMAGNT	I	Direct memory access grant from CPU
4	$\overline{MEMSEL}$	I	Memory select for read or write from CPU
5	IFETCH	I	CPU flag indicating instruction fetch cycle
6	$\overline{MEMSEL}$*	O	Memory select generated by the IM6102
7	$\overline{RESET}$	I	Asynchronous reset will clear Instruction Field to 0_8, disable all interrupts, initialize DMA port to READ/REFRESH, initialize timer to "stop", "divide by 2^{12} mode" and "enable divide counters"
8	$\overline{UP}$	O	User pulse (read or write)
9	XTA	I	CPU external minor cycle timing signal
10	LXMAR	I	A falling edge of LXMAR pulse from CPU will load external memory address register
11	LXMAR*	O	LXMAR generated by the IM6102
12	XTC*	O	XTC generated by the IM6102
13	XTC	I	CPU external minor cycle timing signal
14	CLOCK	I	Oscillator OUT pulses from CPU for timing the IM6102 DMA transfers.
15	$\overline{SKP}/\overline{INTX}$	I	Multiplexed SKP/INT line from lower priority devices
16	DX0	I/O	Most significant bit of the 12-bit multiplexed address and data I/O bus
17	DX1	I/O	See pin 16-DX0
18	DX2	I/O	See pin 16-DX0
19	DX3	I/O	See pin 16-DX0
20	DX4	I/O	See pin 16-DX0
21	DX5	I/O	See pin 16-DX0
22	DX6	I/O	See pin 16-DX0
23	DX7	I/O	See pin 16-DX0
24	DX8	I/O	See pin 16-DX0
25	DX9	I/O	See pin 16-DX0
26	GND	I/O	Power Supply
27	DX10	I/O	See pin 16-DX0
28	DX11	I/O	See pin 16-DX0
29	OSCIN	I	Crystal input for timer oscillator
30	$\overline{DEVSEL}$	I	Device select for read or write from CPU
31	OSC OUT	O	See pin 29
32	$\overline{C_0}$	O	Control lines to CPU determining type of peripheral data transfer
33	$\overline{C_1}$	O	See pin 32-C_0
34	$\overline{C_2}$	O	See pin 32-C_0
35	$\overline{SKP}/\overline{INT}$	O	Multiplexed SKP/INT input to the CPU
36	EMAO	O	Extended memory address field (most significant bit)
37	EMA1	O	Extended memory address field
38	EMA2	O	Extended memory address field
39	INTGNT	I	CPU interrupt grant
40	$\overline{PROUT}$	O	Priority out for vectored interrupt

NOTE: All DX lines are bidirectional with three-state outputs: Pins 6, 8, 11, 12, 35, 40 have active pullups; pins 32, 33, 34 have open drain outputs; pin 15 has a resistive input pullup; all inputs are protected with resistors and clamp diodes.

ARCHITECTURE

The IM6102 is composed of three distinct functions:

a) A DMA port that uses the bus during the second half of a cycle to read, write, or refresh memory. The DMA port logic includes a word count register WC, a current address register CA, an extended current address register ECA, and a DMA status register.

b) An extended memory address controller that augments the 12-bit addresses generated by the IM6100 microprocessor by supplying a 3-bit address field that may be decoded to select one of eight 4096 word memory fields. The memory extension controller logic consists of an instruction field register IF, a data field register DF, an instruction buffer register IB, and a save field register SF.

c) A realtime clock whose mode and time base rate may be programmed by the user. The clock logic includes a clock enable register CE, a clock buffer register CB, a clock counter register CC, and a time base multiplexer.

A block diagram of the IM6102 is shown in Figure 1.

The IM6102 registers are summarized as follows:

A. Simultaneous DMA Channel (Figure 3)

CURRENT ADDRESS (CA) REGISTER

This register is a 12-bit presettable binary counter. At the beginning of a SDMA transfer, the current address must be set to the first location to be accessed. The content of the CA register is incremented by 1 after a SDMA transfer, and the incremented value is used as the address of the memory location with which the next transfer will be performed.

EXTENDED CURRENT ADDRESS (ECA) REGISTER

This is a 3-bit presettable binary counter and if the carry enable bit of the DMA status register is set, the 12-bit CA register and the 3 ECA bits are treated as one 15-bit register with the ECA bits most significant. If memory field 7 (all 3 bits at logic one) is selected, the ECA cannot increment, but will wrap around in field 7 and an F7 error (F7E) will occur. The Interrupt Enable bit IE in SR11 must be set to enable F7E interrupts. If enabled the F7E will request an interrupt. If the carry enable bit CE in SR9 is not set, the ECA is not incremented when CA goes from 7777_8 to 0000_8.

WORD COUNT (WC) REGISTER

A 12-bit presettable binary counter is used as a word counter. At the beginning of a SDMA transfer, the two's complement of the number of 12-bit words to be transferred must be loaded into the WC. If enabled this will initiate the SDMA operation. The WC register is incremented by 1 after a SDMA transfer. If this value becomes zero, word count overflow has occurred and if the IE bit in SR11 is set, interrupts are enabled and an interrupt is requested. Unless instructed to be in the continuous run mode, a WC overflow inhibits further transfers. The WOF is set when the MSB of the WC register makes a "1" to "0" transition.

FIGURE 1: IM6102 MEMORY EXTENSION/DMA/INTERVAL TIMER CONTROLLER (MEDIC)

FIGURE 2: MEDIC TIMING FOR DCA I

DMA Status Register

This register consists of 5 control bits and 2 flag bits for the SDMA feature. For a description refer to the register bit assignments.

FIGURE 3: SDMA REGISTERS

OPERATION

The IM6102 SDMA channel augments the throughput of the IM6100 during DMA operations by transferring data between memory and peripheral devices simultaneously with normal processor bus usage. In other words, no memory cycles are "stolen" from the processor; but the DMA address and data are transferred on the bus during periods that the DX bus is inactive.

TABLE 3 SDMA INSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION
LCAR	6205_8	LOAD CURRENT ADDRESS REGISTER (CA) The contents of the AC replace the contents of the CA and the AC is cleared. DMA sequencing is stopped.
RCAR	6215_8	READ CURRENT ADDRESS REGISTER Description: Contents of CA transferred to AC.
LWCR	6225_8	LOAD WORD COUNT REGISTER (WC) Description: Contents of AC are transferred to the WORD COUNT REGISTER, the AC is cleared WORD COUNT OVERFLOW (WOF) is cleared and DMA operation started.
LEAR	$62N6_8$	LOAD IMMEDIATE TO EXTENDED CURRENT ADDRESS REGISTER (ECA) Description: Field N of the IOT instruction is transferred to the Extended current address register.
REAR	6235_8	READ EXTENDED CA Description: Extended current address register contents OR'd into bits 6, 7, 8, of AC.
LFSR	6245_8	LOAD DMA FLAGS and STATUS REGISTER Description: AC bits 7-11 are transferred to the DMA STATUS REGISTER and the AC is cleared.
RFSR	6255_8	READ DMA FLAGS and STATUS REGISTER Description: DMA Flags and Status Register bits are OR transferred into AC bits 5-11 and Field 7 wraparound error (F7E) is cleared.
SKOF	6265_8	SKIP ON OVERFLOW INTERRUPT Description: The PC is incremented by 1 if a word count register overflow interrupt condition is present causing next instruction to be skipped.
WRVR	6275_8	WRITE VECTOR REGISTER Description: AC bits 0-10 are transferred to the Vector Register and the AC is cleared.
CAF	6007_8	CLEAR ALL FLAGS—clears F7E and WOF (and also COF), Clock enable and clock buffer. The DMA process is initiated if the status register is not set to the "stop" mode.

TABLE 4 DMA FLAGS AND STATUS REGISTER BIT ASSIGNMENTS

0	1	2	3	4	5	6	7	8	9	10	11
*	*	*	*	*	F7E	WOF	SR7	SR8	CE	$\overline{R}$/W	IE

where* — don't care for write and zero for read.

F7E — Field 7 wrap around carry error; cleared by CAF, RFSR and RESET

WOF — Logic one indicates word counter overflow; clear by CAF, LWCR and RESET

CE — Carry enable from CA(0-11) to ECA; cleared by RESET

$\overline{R}$/W — Logic one indicates DMA write (Port to Memory transfer). Cleared (DMA Read) by RESET

IE — Enable interrupt when WC overflows or Field 7 error occurs; cleared by RESET

SR7, 8
- 00 — Refresh mode; WC is frozen, no UP, DMAEN is don't care
- 01 — Normal mode; DMAEN(H) freezes WC CA and no UP if WC has not overflowed; stop if WC overflows
- 10 — Burst mode; DMAEN(H) freezes WC, CA and no UP if WC has not overflowed; refresh condition if WC overflows
- 11 — Stops DMA

DMA MODES

$SR_7 = SR_8 = 0$ REFRESH MODE

This is the mode to which the 6102 reverts on RESET. The word count register clock input is disabled, the user pulse (DMA data strobe) is suppressed and the DMAEN input is ignored. However, provided valid DMA transfer conditions are met in a particular memory cycle, the DMA sequencer will be started, appropriate timing signals will be generated and the current address register will be clocked. Thus DMA read accesses will be performed continually with an essentially free-running current address register. Read accesses will refresh dynamic memory. No WOF is possible but an F7E is possible if bit SR9 is set, enabling a carry from the current address register to the extended current address register.

$SR_7 = 0; SR_8 = 1$ NORMAL MODE

This mode is used for normal SDMA operations with static memory. The following instruction sequence can be used:

```
CLA      /Clear AC
TAD CA   /Get starting address
LCAR     /Load into current address register and
         clear AC
```

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TAD SR	/Get DMA status Register Constant
LFSR	/Change status (from refresh to normal for example)
TAD WC	/Get two's complement of block length
LWCR	/Load word count register and start DMA TRANSFERS

Note that LWCR will start the sequencer so it should be the last instruction in the initialization sequence. The ECA register and vector register could also have been initialized in this sequence.

The SDMA sequencer samples DMAEN on the rising edge of every XTA and latches the condition of the enable line. If DMAEN is low, the sequencer is enabled, external timing signals XTC*, MSEL*, UP, LXMAR* are generated, the WC and CA registers are clocked. If DMAEN is high, at XTA (↑) time, the signal is sampled and latched and if the WC has not overflowed, the WC and CA registers are frozen, UP is suppressed. If the WOF condition comes up, the SDMA operation stops, regardless of DMAEN level.

The DMAEN and UP signals provide a simple interlocked handshaking method for transferring data one or more characters at a time (entire blocks) concurrently with processor operations on the bus. Of course, at all times, independent of DMAEN, the SDMA sequencer can proceed only if other bus usage conditions for DMA operations are met (not IOTA, IAUTOI, DCA, JMS, IJMS, ISZ, DMAGNT, or access of location $X0000_8$).

NOTE: IAUTOI is an indirect cycle of any autoindexed instruction; IJMS is indirect cycle of JMS. An autoindexed JMP* instruction may not be executed when the DMA mode is active.

$SR_7 = 1; SR_8 = 0$ BURST MODE

This mode is the same as the normal mode except when the word count register overflows. When this happens, the SDMA sequencer will set the WOF flag and revert to the refresh mode (ignoring DMAEN, freezing WC and suppressing UP). This mode is used when SDMA operations and dynamic memory refresh must be concurrently performed. The system designer must control the block lengths to be transferred, the refresh interval, and memory system design according to the application and performance desired.

$SR_7 = 1; SR_8 = 1$ STOP MODE

In this mode, no SDMA operations will take place. Naturally, cycle stealing DMA is still possible, and indeed may be used in any of the modes but the designer must be aware that cycle stealing may adversely affect dynamic memory refresh intervals. LWCR and LFSR may be executed in either order to change mode and start DMA.

B. Extended Memory Address Control

Figure 4 shows the EMA registers in more detail along with the register transfers caused by various instructions. The EMA function of the IM6102 is program compatible with the DEC PDP-8/E KM8-E Memory Extension option. The purpose of the EMA function is to extend the effective addressing space of the system from 4K to 32K words. To perform this function, the EXTENDED MEMORY CONTROLLER maintains a 3-bit extended address which is decoded by the memory modules to select 1 of 8 memory fields each containing 4096 words of storage. These 4K fields start with FIELD 0 and progress to FIELD 7 when 32K of memory is used. All software communication with the controller is via programmed IOT instructions for which a summary is included in Table 1.

Figure 4 shows two 3-bit field registers: the Instruction Field, which acts as an extension to the Instruction and directly obtained operand addresses and the Data Field, which augments indirectly obtained operand addresses. The program can, therefore, use one field for instructions and address pointers and another field for data. The selection between Instruction and Data Fields is signalled by the DATAF signal generated by the IM6100. A discussion of the various registers follows.

FIGURE 4: EMA REGISTERS

INSTRUCTION FIELD REGISTER (IF)

The IF is a 3-bit register that serves as an extension of the Program Counter (PC). The IF, however, is not incremented when the PC goes from 7777_8 to 0000_8. The contents of the IF determine the field from which all instructions are taken. Operands for all directly addressed memory reference instructions also come from the Instruction Field. The indirect pointer for all indirectly addressed memory reference instructions reside in the Instruction Field. The IF is cleared to 0_8 and the IM6100 Program Counter is set to 7777_8 by RESET.

DATA FIELD REGISTER (DF)

The DF is a 3-bit register which determines the memory field from which operands are fetched in indirectly addressed AND, TAD, ISZ or DCA instructions. However, the branch address for indirectly addressed JMS or JMP instructions is obtained from the Instruction Field. The Data Field register may be modified under program control. The DF is set to 0_8, on reset.

INSTRUCTION BUFFER REGISTER (IB)

The IB is a 3-bit register which serves as an input buffer for the Instruction Field (IF) register. All programmed modifications of the IF register are made through the IB

register. The transfer from IB to IF takes place at the beginning of the execute phase of the "next" JMP or JMS instruction or immediately upon execution of an LIF instruction. Using this feature, a program segment can execute an instruction to modify the IF and then "exit" the program segment before the actual modification of the IF takes place. If instructions could change the IF directly, it would be impossible to execute the "next" sequential instruction, followed by a Change IF instruction. The IB to IF transfer is inhibited if the JMP/JMS instruction is fetched from control panel memory, which is restricted to 4K, but the LIF instruction is used here to provide the ability to load the IF register from the IB register. This allows the control panel routines to be executed transparently while the IB and IF differ and also yields a method for the panel to extract or alter the status of the primary EMA registers. The IB is set to 0_8, on reset. The IB to IF transfer takes place during the second cycle of a JMP/JMS instruction when XTC makes a falling (↓) transition.

SAVE FIELD REGISTER (SF)

The SF is a 6-bit register in which the IB and DF registers are saved during an Interrupt Grant. When an Interrupt occurs, the contents of IB and DF are automatically stored in SF (0-2) and SF (3-5), respectively, and the IF, IB and DF registers are cleared. The INTGNT (Interrupt Grant) cycle stores the "current" Program Counter (PC) in location 0000_8 of Memory Field 0_8 and the CPU resumes operation in location 0001_8 of Memory Field 0_8. The Instruction Field and Data Field of the program segment being executed by the CPU before the interrupt was acknowledged are available in the SF register.

INTERRUPT INHIBIT FLIP-FLOP

The INTREQ (Interrupt Request) line to the IM6100 must be "gated" by the Interrupt Inhibit Flip-Flop so that, when the Instruction Field is changed under program control, all interrupts are disabled until a JMP or JMS instruction is executed. Since the actual modification of the Instruction Field takes place only after the "next" JMP/JMS, this inhibition of the INTREQ's ensures that the program sequence resumes operation in the "new" memory field before an Interrupt Request is granted.

Since Interrupt Requests are asynchronous in nature, a situation may arise in which an INTREQ is generated when the IF and IB bits are different. The Interrupt Inhibit FF guarantees the structural integrity of the program segment. The IIF is cleared on reset.

TABLE 5 EMA INSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION
GTF	6004_8	GET FLAGS Operation: AC (0) ← LINK AC (2) ← INTREQ Line AC (3) ← INT INHIBIT FF AC (4) ← INT ENABLE FF AC (6-11) ← SF (0-5) Description: LINK, INTREQ and INT ENABLE FF are internal to the CPU. The INT INHIBIT FF and SF are in the MEDIC.
RTF	6005_8	RETURN FLAGS Operation: LINK ← AC (0) IB ← AC (6-8) DF ← AC (9-11) Description: LINK is restored. All AC bits are available externally during IOTA T6 to restore other flag bits. The internal Interrupt System is enabled. However, the Interrupt Inhibit FF is made active until the "next" JMS/JMP/LIF. The IB is transferred to IF after the "next" JMS/JMP/LIF.
CDF	$62N1_8$	CHANGE DATA FIELD Operation: DF ← N_8 Description: Change DF register to N (0_8-7_8).

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TABLE 5, Continued

MNEMONIC	OCTAL CODE	OPERATION
CIF	$62N2_8$	CHANGE INSTRUCTION FIELD Operation: $IB \leftarrow N_8$ Description: Change IB to N (0_8-7_8). Transfer IB to IF after the "next" JMP/JMS/LIF. The Interrupt Inhibit FF is active until the "next" JMP/JMS/LIF.
CDF, CIF	$62N3_8$	CHANGE DF, IF Operation: $DF \leftarrow N_8$ $IB \leftarrow N_8$ Description: Combination of CDF and CIF.
RDF	6214_8	READ DATA FIELD Operation: AC (6-8) ← AC (6-8) + DF Description: OR's the contents of DF into bits 6-8 of the AC. All other bits are unaffected.
RIF	6224_8	READ INSTRUCTION FIELD Operation: AC (6-8) ← AC (6-8) + IF Description: OR's the contents of IF into bits 6-8 of the AC. All other bits of the AC are unaffected.
RIB	6234_8	READ INTERRUPT BUFFER READ SAVE FIELD Operation: AC (6-11) ← AC (6-11) + SF Description: OR's the contents of SF into bits 6-11 of the AC. All other bits are unaffected.
RMF	6244_8	RESTORE MEMORY FIELD Operation: IB ← SF (0-2) DF ← SF (3-5) Description: The SF register saves the contents of the IB and DF when an interrupt occurs. This command is used to restore IB and DF when "exiting" from the interrupt service routine in another field. Transfer IB to IF after the next JMP/JMS/LIF. The Interrupt Inhibit Flip-Flop is active until the next JMP/JMS/LIF.
LIF	6254_8	LOAD INSTRUCTION FIELD Operation: IF ← IB Description: Transfer IB to IF and clear the Interrupt Inhibit FF

+: "OR"
•: "AND"
←: "IS REPLACED BY"

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OPERAND FETCHING

Instructions are accessed from the currently assigned Instruction Field. For indirect AND, TAD, ISZ or DCA instructions, the operand address refers first to the Instruction Field to obtain an Effective Address which in turn refers to a location in the currently addressed Data Field. All instructions and operands are obtained from the field designated by the IF, except for indirectly addressed operands, which are specified by the DF.

Thus, DF is active only in the Execute phase of an AND, TAD, ISZ or DCA when it is directly preceded by an Indirect phase.

ADDRESS MODE	IF	DF	AND, TAD, ISZ or DCA
Direct	m	n	Operand in field m
Indirect	m	n	Absolute address of operand in field m; operand in field n

Each field of extended memory contains eight auto-index registers in addresses 10 through 17. For example, assume that a program in field 2 is running (IF = 2) and using operands in field 1 (DF = 1) when the instruction TAD I 10 is fetched. The indirect autoindex cycle is entered, and the contents of location 10 in field 2 are read, incremented, and rewritten. If address 10 in field 2 originally contained 0546, it now contains 0547. In the execute cycle, the operand is fetched from location 0547 of field 1.

Program control is transferred between memory fields by the CIF instruction. The instruction does not change the instruction field directly, as this would make it impossible to execute the next sequential instruction; instead, it loads the new instruction field in the IB for automatic transfer into the IF when either a JMP or JMS instruction is executed. The DF is unaffected by the JMP and JMS instructions.

The 12-bit program counter is set in the normal manner and, because the IF is an extension on the most significant end of the PC, the program sequence resumes in the new memory field following a JMP or JMS. Entry into a program interrupt is inhibited after the CIF instruction until a JMP or JMS is executed.

NOTE: The IF is not incremented if the PC goes from 7777_8 to 0000_8. This feature protects the user from accidentally entering a nonexistent field.

To call a subroutine that is out of the current field, the data field register is set to indicate the field of the calling JMS, which establishes the location of the operands as well as the identity of the return field. The instruction field is set to the field of the starting address of the subroutine. The following sequence returns program control to the main program from a subroutine that is out of the current field.

```
/PROGRAM OPERATIONS IN MEMORY FIELD 2
/INSTRUCTION FIELD = 2; DATA FIELD = 2
/CALL A SUBROUTINE IN MEMORY FIELD 1
/INDICATE CALLING FIELD LOCATION BY THE
/CONTENTS OF THE DATA FIELD
        CIF 10          /CHANGE TO INSTRUCTION
                        /FIELD 1 = 6212
        JMS I SUBRP     /SUBRP = ENTRY ADDRESS
        CDF 20          /RESTORE DATA FIELD
        .
        .
        .
SUBRP,  SUBR            /POINTER
                                        FIELD 2
-----------------------------------------------------
                                        FIELD 1
                        /CALLED SUBROUTINE,
                        /LOCATION IN FIELD 1
SUBR,   0               /RETURN ADDRESS
                        /STORED HERE
        CLA
        RDF             /READ DATA FIELD INTO AC
        TAD RETURN      /CONTENTS OF THE AC =
                        /6202 + DATA FIELD BITS
        DCA EXIT        /STORE CIF N INSTRUCTION
        .               /NOW CHANGE DATA FIELD
        .               /IF DESIRED
        .
EXIT,   0               /A CIF INSTRUCTION
        JMP I SUBR      /RETURN TO CALLING
                        /PROGRAM
RETURN, CIF             /USED TO FORM CIF N
                        /INSTRUCTION
```

When a program interrupt occurs, the current instruction and data field numbers are automatically stored in the 6-bit save field register, then the IF and DF are cleared. The 12-bit program counter is stored in location 0000_8 of field 0_8 and program control advances to location 0001_8 of field 0_8. At the end of the program interrupt subroutine, the RMF instruction restores the IF and DF from the contents of the SF. Alternatively, the GTF and RTF instructions may be used to handle the Save Field and Link information. The following instruction sequence at the end of the program interrupt subroutine continues the interrupted program after the interrupt has been processed:

```
        .
        .
        .
        .
        CLA
        TAD AC          /RESTORE AC
        RMF             /LOAD IB AND DF FROM SF
        ION             /TURN ON INTERRUPT
                        /SYSTEM
        JMP I 0         /RESTORE PC WITH
                        /CONTENTS OF LOCATION
                        /0000₈ AND LOAD
                        /IF FROM IB
```

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IM6100 control panel memory programs, if used must be careful in the manner that EMA register data is manipulated. Control panel interrupt requests bypass the device interrupt enable flip flop, and indeed, are granted even by a halted CPU. The interrupts from a control panel may occur at any time, and in particular when the IB and IF registers do not contain the same data. The EMA logic inhibits IB to IF transfers in control panel memory so that panel routines may execute transparently (in particular, JMP/JMS instructions). The panel routines may alter the IF by executing the LIF instruction.

Users should also note that the GTF and RIB instructions read the SF register, and only the RIF instruction reads the IF register. Note also that the SF saves the IB register rather than the IF during an interrupt. However, interrupts are inhibited until the IF and IB registers are the same.

The memory extension controller that we have discussed in this section shows three important design considerations involved in extending memory addressing space. The first is the concept of having separate instruction and data fields for program flexibility. The second is the importance of double buffering the instruction field register to maintain structural integrity of programs and the third is the provision for saving the current field status upon interrupts and disabling interrupts until a change of instruction field has been completely executed.

C. Programmable Real Time Clock

The programmable real time clock offers the 6100 user a number of ways to accurately measure and count intervals in order to implement real time data acquisition and data processing systems.

The crystal used should have the following characteristics:

$R_S \leqslant 150$ ohms

C_M = 3-30 mpF (10^{-15}F)

C_O = 10-50 pF

Static capacitance should be around 5pF; for the greatest stability, C_O should be around 12pF and the oscillator is parallel resonant.

TABLE 6 CLOCK ENABLE REGISTER BIT ASSIGNMENTS

0	1	2	3	4	5	6	7	8	9	10	11
EN0	*	EN2	EN3	EN4	EN5	*	EN7	*	*	*	*

* Don't care for write and zero for read.

Where EN0 — When set to 1, enables clock overflow (COF flag) to cause an interrupt. Cleared by RESET, CAF.

EN2 — When reset to a 0-counter runs at selected rate. Overflow occurs every 4096 (2^{12}) counts.COF flag remains set until cleared by IOT 6135 (CLSA), CAF, RESET. When set to a 1-counter runs at selected rate. If the COF flag is cleared, overflow causes clock buffer to be transferred to the clock counter which continues to run. COF flag remains set until cleared with IOT 6135 (CLSA). Also cleared by RESET, CAF.

EN3, 4, 5 — Assuming 2 MHz crystal oscillator cleared by RESET, CAF.

Bits 3,4,5	Octal	Interval Between Pulses	Frequency
000	0	Stop	0
001	1	Stop	0
010	2	20 msec	50 Hz
011	3	2 msec	500 Hz
100	4	200 μsec	5 KHz
101	5	20 μsec	50 KHz
110	6	2 μsec	500 KHz
111	7	Stop	0

EN7 — Inhibits clock prescaler when set to 1 cleared by RESET, CAF. EN3-5 and EN7 should not be changed simultaneously.

FIGURE 5 RTC REGISTERS

A discussion of the Real Time Clock registers as shown in Fig. 5 follows:

CLOCK ENABLE REGISTER

This register controls the mode of counting, whether clock interrupts are allowed, and the rate of the time base of the clock. For a description refer to the register bit assignments.

CLOCK BUFFER REGISTER (CB)

This 12-bit register stores data being transferred from the AC to the clock counter, or from the clock counter to the AC. It also permits presetting of the clock counter.

CLOCK COUNTER REGISTER (CC)

This register is a 12-bit binary counter that may load the clock buffer or be loaded from it. It is driven by a 2 MHz crystal oscillator with the proper predivision set by the time base selection. When an overflow occurs and if bit 0 of the clock enable register is a logic one, an interrupt is requested. If bit 2 is also 1, overflow causes the clock buffer to be transferred automatically into the clock counter.

TIME BASE MULTIPLEXER

The multiplexer provides count pulses to the clock counter according to the rate set by the clock enable register. Use of other than a 2 MHz crystal for the clock will result in proportionately different time bases.

CLOCK OVERFLOW FLAG

This flag is set by a clock counter overflow. It is cleared by CAF, CLSA and RESET. Its complement provides LSB (VR11) of interrupt vector. If ENO of clock enable counter is set, COF can cause an interrupt request. The COF is set when the MSB of the counter makes a "1" to "0" transition.

TABLE 7 RTC INSTRUCTIONS

MNEMONIC	OCTAL CODE	OPERATION
CLZE	6130_8	CLEAR ENABLE REGISTER PER AC Description: Clears the bits in the clock enable register corresponding to those bits set in the AC. The AC is not changed.
CLSK	6131_8	SKIP ON CLOCK INTERRUPT Description: Causes the program counter to be incremented by one if clock interrupt conditions exists, so that the next sequential instruction is skipped.
CLOE	6132_8	SET ENABLE REGISTER PER AC Description: Sets the bits in the clock enable register corresponding to those bits set in the AC. The AC is not changed.
CLAB	6133_8	TRANSFER AC TO CLOCK BUFFER Description: Causes the contents of the AC to be transferred to the Clock Buffer, then causes the contents of the Clock Buffer to be transferred to the Clock Counter. The AC is not changed.
CLEN	6134_8	READ CLOCK STATUS Description: Interrogates the clock overflow status flip flop by clearing AC, then transferring clock status into AC bit 0. COF is cleared.
CLSA	6135_8	READ CLOCK STATUS Description: Interrogates the clock overflow status flip flop by clearing AC, then transferring clock status into AC bit O. COF is cleared.
CLBA	6136_8	READ CLOCK BUFFER Description: Clears the AC, then transfers the contents of the Clock Buffer into the AC.
CLCA	6137_8	READ CLOCK COUNTER Description: Clears the AC, transfers the contents of the Clock Counter to the Clock Buffer, then transfers the contents of the Clock Buffer into the AC. If EN7 is set to 1 (clock prescaler is inhibited), the CLCA instruction increments the prescaler input by one. If the clock is in the "stop" mode but EN7 is not inhibited, the prescaler will not be clocked by the CLCA instruction.
CAF	6007_8	CLEAR ALL FLAGS Description: Clears COF flag (and also F7E, WOF flags), clock enable and clock buffer registers.

SYSTEM CONSIDERATIONS

The IM6102 is the highest priority device in a priority interrupt scheme. It provides an active low signal on pin 40, POUT, to signal the next lower priority device in the chain (thus, a high level on POUT indicates that the 6102 is not requesting an interrupt) via its "priority-in", PRIN, input.

The IM6102 when requesting an interrupt activates the SKP/INT line low on pin 35 and the POUT line low on pin 40 if its interrupt inhibit flip-flop is not set.

The IOT instructions used by the IM6102 preclude the use of certain device addresses when the system uses IM6101 PIEs. The addresses that may not be used are those given by bits 3 through 7 of the IOT instructions that are used with the IM6102. These addresses are 00101, 01000, 01001, 01010, 01011 corresponding to IOT instructions 612X, 613X, 620X, 621X, 622X, 623X, 624X, 625X, 626X and 627X.

The IM6102 does not generate DMAREQ signals to the 6100 because of its simultaneous use of the DX bus. It monitors the DMAGNT signal in order to place the EMA 0, 1, 2 lines on pins 36, 37, 38 in a high impedance state while DMAGNT is high.

If the application requires other peripherals requiring direct memory access on a cycle stealing basis, for example, bus contention problems will be resolved by the IM6102 as it monitors the DMAGNT line and gets off the bus (by placing all lines in the high impedance state) when DMAGNT is active.

If interrupts are enabled and a request is pending, during the first INTGNT cycle, the IM6102 will detect the referencing of location 0000_8 by the IM6100 in order to save the PC and will suspend simultaneous DMA during that cycle. The logic will in fact suspend simultaneous DMA in any cycle that location 0000_8 is referenced, either in main memory or control panel memory.

This makes it possible to disable automatic interrupt vectoring by grounding the INTGNT line to the IM6102. This will not affect the generation of INTREQ so the IM6100 will have to poll peripheral devices (skip on flag instructions) to determine the interrupting source.

Grounding INTGNT is not possible in extended memory applications since the INTGNT signal is used to save the Instruction Buffer and Data Field Register and clear the IF, IB and DF registers. (All peripheral device interrupt service routines have their entry point at location 0001_8 of Memory Field 0_8).

If no interrupt requests are pending in the 6102 (COF, F7E or WOF) from the DMA or RTC functions, the IM6102 interrupt request flip-flop is clear and POUT, the priority out signal, is high, enabling interrupt requests downstream in the priority chain. In the event that interrupts are enabled (DMA status bit SR11 is set and/or clock enable bit ENO is set) and an interrupting condition occurs (F7E, WOF, COF), the POUT signal goes low asynchronously disabling interrupt vectors downstream.

If the Interrupt Inhibit Flip-Flop is not set, the SKP/INT line is driven low by the interrupt request. If the IIFF is set, the SKP/INT line stays high until the IIFF is cleared (by RESET or an IB to IF transfer) at which time SKP/INT may be driven low. Skip requests will always propagate independently of IIFF during IOTA •$\overline{\text{DEVSEL}}$• XTC.

Interrupt requests from devices downstream of the IM6102 must also be channeled via the IM6102 in order that the IIFF may condition the request timing. The IM6102 provides a built in pull-up on the SKP/INTX line coming in from devices downstream in the priority chain. At 5v, the pull-up looks like a 10K resistor; at 10V, it looks like 5K.

The execution of any IOT instruction will reset INTGNT to a low level at the end of IOTA time. This IOT instruction will be the first instruction in the interrupt service routine after saving status. If hardware vectoring is being used, any IOT instruction when INTGNT is high will cause the IM6102 to place a vector address on the bus if it requested an interrupt and pull the C1 and C2 lines low, thus placing the vector in PC and forcing a branch to the service routine. If the C2 line is left unconnected, the vector address will not be forced into the PC, but will be OR'ed into the AC. The interrupt service routine would have to execute a CLA after its first IOT instruction in order to clear the AC. Note that the LSB of the vector address is determined by the complement of the COF flag and that a DMA interrupt service routine must distinguish between the two possible interrupting conditions, a word count overflow or a field 7 wraparound error. The programmer may read the DMA status register with an RFSR instruction and also test the WOF flag with a skip instruction, SKOF. The COF flag may also be tested with the CLSK skip instruction. The flag may be read (and cleared) with the CLSA instruction. The skip instructions cause the SKP/INT line to go low during IOTA • XTC time if the flag being tested is set. At all other times, the SKP/INT line carries interrupt requests as modified by the IM6102 interrupt inhibit logic. The flags must always be explicitly cleared by the interrupt service routine.

The DMA transfer rate depends on the program. The minimum rate would be obtained if the processor was executing an autoindexed DCA or an indirect JMS (even if non-autoindexed, DMA is suppressed during indirect phase of JMS). Continuously executing these instructions would cause DMA transfers to occur only every third memory cycle (IFETCH). The maximum rate could be obtained by executing a JMP• loop (JMP to itself); data would be transferred on every cycle and the interrupt routine entered when word count overflows could bump the return address out of the loop.

In dynamic memory systems it should be noted that the MEMSEL* signal narrows when the mode changes from write to refresh (burst mode). RESET signals may need to be limited in duration to prevent loss of memory data in dynamic memory systems.

The accuracy of the clock counter in the programmable real time clock section of the IM6102 is as follows:

CASE 1: Counter running; CC loaded from AC via CB using instruction CLAB (IOT 6133) accuracy is 0 to +1 count.

CASE 2: CC loaded from CB automatically on overflow; the accuracy of counting is then only dependent on accuracy of oscillator.

IM6102 users who do not need all the capabilities of the device may improve systems performance by not using some of the features. To do this properly, certain pins on the device will become unused. The following table summarizes what may be done with certain pins when using only part of the IM6102 functions. All unlisted pins must be used when implementing any of the three basic features.

PIN NUMBER	PIN NAME	RTC ONLY	SDMA ONLY	EMC ONLY	EMC & DYNAMIC REFRESH
2	DMAEN	GND	USED	GND	GND
3	DMAGNT	USED	USED	USED	USED
6	MEMSEL*	N/C	USED	N/C	USED
8	UP	N/C	USED	N/C	N/C
11	LXMAR*	N/C	USED	N/C	USED
12	XTC*	N/C	USED	N/C	USED
15	SKP/INTX	VCC	VCC	USED	USED
29	OSCIN	USED	GND	GND	GND
31	OSC OUT	USED	N/C	N/C	N/C
34	C2	USED	USED	N/C	N/C
36	EMAO	N/C	N/C	USED	USED
37	EMA 1	N/C	N/C	USED	USED
38	EMA 2	N/C	N/C	USED	USED
40	PROUT	USED	USED	N/C	N/C

TABLE 1 SUMMARY OF IM6102 INSTRUCTIONS

MNEMONIC	OCTAL CODE	I/O CONTROL LINES			OPERATION
		C0	C1	C2	
GTF	6004	0	0	1	① Get flags, INT INH FF → AC(3), SF (0-5) → AC(6-11)
RTF	6005	1	1	1	② Return flags, AC(6-8) → IB, AC(9-11) → DF
CDF	62N1	1	1	1	Change Data Field, N → DF
CIF	62N2	1	1	1	Change IF, N → IB
CDF, CIF	62N3	1	1	1	Combination of CDF, CIF
RDF	6214	1	0	1	Read DF, DF + AC(6-8) → AC(6-8)
RIF	6224	1	0	1	Read IF, IF + AC(6-8) →AC(6-8)
RIB	6234	1	0	1	Read Save Field, SF + AC(6-11) → AC(6-11)
RMF	6244	1	1	1	Restore Mem. Field, SF(0-2) → IB, SF(3-5) → DF
LIF	6254	1	1	1	Load IF, IB → IF
CLZE	6130	1	1	1	Clear Clock Enable Register if corresponding AC bit is set AC not changed
CLSK	6131	1	1	1	Skip on Clock Overflow Interrupt condition
CLOE	6132	1	1	1	Set Clock Enable Register if corresponding AC bit is set AC not changed
CLAB	6133	1	1	1	AC → Clock Buffer; Clock Buffer → Clock Counter; AC not changed
CLEN	6134	0	0	1	Clock Enable Register → AC
CLSA	6135	0	0	1	COF → AC(0), Clear COF Status bit
CLBA	6136	0	0	1	Clock Buffer → AC
CLCA	6137	0	0	1	Clock Counter → Clock Buffer; Clock Buffer → AC
LCAR	6205	0	1	1	AC → Current Address Register, 0 → AC
RCAR	6215	0	0	1	Current Address Register → AC
LWCR	6225	0	1	1	AC → Word Count Register, Start DMA, 0 → AC; clears word count overflow (WOF)
LEAR	62N6	1	1	1	N → Extended Current Address Register (ECA)
REAR	6235	1	0	1	Read ECA, ECA + AC(6-8) → AC(6-8)
LFSR	6245	0	1	1	AC(7-11) → Status Register, 0 → AC
RFSR	6255	1	0	1	DMA Status Register + AC(5-11) → AC(5-11); clears Field 7 Wraparound error (F7E)
SKOF	6265	1	1	1	Skip on Word Count Overflow
WRVR	6275	0	1	1	AC(0-10) → Vector Register, 0 → AC
CAF	6007	1	1	1	③ Clear all flags (F7E, W0F, COF) Clear clock Enable register, clock buffer

NOTES:

1. The internal flags of the IM6100 are defined as follows: LINK → AC (0), INTREQ → AC (2) and INTERRUPT ENABLE FF → AC (4).
2. When RTF is executed, the LINK is restored from AC (0) and the Interrupt System is enabled after the next sequential instruction is executed. The Interrupt Inhibit FF is set preventing interrupts until the next JMP, JMS or LIF instruction is executed.
3. A hardware RESET clears F7E, W0F, 11FF and COF. The IF and DF are cleared to O_8. The DMA status register is cleared. (Read; refresh; disable F7E and W0F interrupts; no carry from CAO to ECA2). The clock Enable register is cleared (Disable COF interrupt; disable clock buffer to clock counter transfer on COF; disable counter). Counter/buffer is cleared.

TABLE 2 SUMMARY OF IM6102 REGISTER BIT ASSIGNMENTS

	DX0	DX1	DX2	DX3	DX4	DX5	DX6	DX7	DX8	DX9	DX10	DX11
Current Address	CA0	CA1	CA2	CA3	CA4	CA5	CA6	CA7	CA8	CA9	CA10	CA11
Extended Current Address							ECA0	ECA1	ECA2			
Word Count	WC0	WC1	WC2	WC3	WC4	WC5	WC6	WC7	WC8	WC9	WC10	WC11
DMA Status (1)						SR5	SR6	SR7	SR8	SR9	SR10	SR11
Interrupt Vector (2)	VR0	VR1	VR2	VR3	VR4	VR5	VR6	VR7	VR8	VR9	VR10	VR11
RIF Instruction (3)							IF0	IF1	IF2			
RTF, CIF Instruction							IB0	IB1	IB2			
GTF, RIB Instruction				IIFF(4)			SF0	SF1	SF2	SF3	SF4	SF5
CDF, RDF Instruction							DF0	DF1	DF2			
RTF Instruction										DF0	DF1	DF2
Clock Enable (5)	EN0		EN2	EN3	EN4	EN5		EN7				
Clock Buffer	CB0	CB1	CB2	CB3	CB4	CB5	CB6	CB7	CB8	CB9	CB10	CB11
Clock Overflow (6)	COF											

(1) DMA STATUS

SR5 Set if Field 7 wraparound carry error — F7E; cleared by CAF, RFSR (at IOTA · $\overline{XTC}$ time), RESET } READ ONLY BITS

SR6 Set if DMA Word Counter Overflow — W0F; cleared by CAF, LWCR, RESET } READ ONLY BITS

SR7 Mode Bit 7 } ; Cleared by RESET (REFRESH MODE)

SR8 Mode Bit 8 } See below

SR9 Carry enable from CA0-11 to ECA2 if set — CE

SR10 DMA Write if set

SR11 Enable F7E or W0F interrupt if set — IE

(2) VR0-VR10 loaded from AC. VR11 is equivalent to $\overline{COF}$

(3) IF — Instruction Field; cleared to 0_8 by RESET AND INTGNT

(4) IIFF — Interrupt Inhibit Flip-Flop; set whenever IB ≠ IF; (CIF, CDF/CIF, RMF, RTF) cleared by RESET and IB → IF transfer

(5) EN0 — Enable Clock Overflow (COF) interrupt; cleared (interrupt disable) by RESET, CAF

EN2 — When set causes clock buffer to be transferred to clock counter on COF. Counter runs at selected rate; COF remains set until cleared with CLSA. When cleared to 0, counter runs at selected rate, overflow occurs every 2^{12} counts and COF remains set. EN2 is cleared by RESET, CAF

EN3, EN4, EN5 — Select interval between pulses. Cleared to 000 by RESET (counter disabled), CAF See below.

EN7 — Inhibits clock prescaler when set. Cleared by RESET, CAF

(6) COF — Clock Overflow status bit; cleared by CAF, RESET and CLSA; complement provides LSB of interrupt vector.

SR 7, 8	00	Refresh mode; WC is frozen, no UP, DMAEN don't care
	01	Normal mode; DMAEN(H) freezes WC, CA and no UP if WC has not overflowed; stop if WC overflows
	10	Burst mode; DMAEN (H) freezes WC, CA and no UP if WC has not overflowed; reverts to refresh mode if WC overflows.
	11	Stops SDMA

EN 3, 4,5	with	2 MHz clock
000		STOP
001		STOP
010		20 ms interval
011		2 ms interval
100		200 μs interval
101		20 μs interval
110		2 μs interval
111		STOP

NOTES:

1. Bits SR 7 and 8 do not change when the DMA controller stops or reverts to refresh mode as a result of WC overflow.
2. The "overflow" status is defined as set when the most significant bit of a counter makes a "1" to "0" transition.

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SDMA OPERATIONS TIMING

A. IM6100 Signals

B. DMA Read

C. DMA Read/Refresh

D. DMA Write

E. DMA Write/Refresh

7

TIMING DIAGRAM

IM6102A

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6102A ..... -40°C to +85°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... +4.0V to +11.0V
Supply Voltage ..... +12.0V
Voltage On Any Input or
Output Pin ..... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, T_A = -40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage[1]	GND≤V_{IN}≤V_{CC}	-1.0		1.0	μA
4	V_{OH}	Output Voltage High[2]	I_{OH} = 0mA	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0mA			GND+0.01	V
6	I_{OL}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	μA
7	I_{CC}	Power Supply Current-Standby	V_{IN}=GND or V_{CC}			900	μA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 5.71MHz			4.0	mA
9	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
10	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE: 1. Except pins 15, 29, 31 2. Except pins 32, 33, 34.

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, C_L = 50pF, T_A = -40°C to +85°C, f_C = 5.71MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{LIN}	LXMAR Pulse Width IN	125			ns
2	t_{AIS}	Address Setup Time IN: DX-LXMAR (↓)	50			ns
3	t_{AIH}	Address Hold Time IN: LXMAR(↓)-DX	50			ns
4	t_{DEN}	Data Output Enable Time: DEVSEL(↓)-DX			240	ns
5	t_{CEN}	Controls Output Enable Time: DEVSEL(↓)-lines C0,C1,C2,S/I			240	ns
6	t_{DIS}	Data Input Setup Time: DX-DEVSEL(↑)	50			ns
7	T_{DIH}	Data Input Hold Time: DEVSEL(↑)-DX	50			ns
8	t_{RST}	RESET Input Pulse Width	250			ns
9	t_{SID}	SKP/INTX to SKP/INT Propagation Delay			100	ns
10	t_{DMLX}	DMA Control Signals Delay: XTC-XTC*; MEMSEL-MEMSEL*, LXMAR-LXMAR*			100	ns
11	t_{DEM}	Enable/Disable Time from DMAGNT to EMA Lines			50	ns
12	t_{MDR}	MEMSEL* Pulse Width READ	300			ns
13	t_{MDW}	MEMSEL* Pulse Width WRITE	380			ns
14	t_{MDWR}	MEMSEL* Pulse Width WRITE/REFSH	240			ns
15	t_{LD}	LXMAR* Pulse Width	150			ns
16	t_{DRAT}	DMA READ Access Time: LXMAR*(↓)-UP(↑)	300			ns
17	t_{DXAS}	DX & EMA Address Setup Time Wrt LXMAR*(↓)	150			ns
18	t_{DXAH}	DX & EMA Address Hold Time Wrt LXMAR*(↓)	55			ns
19	t_{DREN}	DMA READ Enable Time: MEMSEL* (↓)-UP(↑)	210			ns
20	t_{RUP}	UP Pulse Width DMA READ	150			ns
21	t_{DWAT}	DMA WRITE Access Time: LXMAR*(↓)-MEMSEL*(↑)	300			ns
22	t_{DWEN}	DMA WRITE Enable Time: UP (↓)-MEMSEL*(↑)	210			ns
23	t_{MWS}	MEMSEL* Setup Time DMA WRITE MEMSEL*(↓)-LXMAR*(↓)	50			ns
24	t_{DMS}	DMAEN Setup Time Wrt XTA (↑)	50			ns
25	t_{DMH}	DMAEN Hold Time Wrt XTA (↑)	50			ns
26	t_{WUP}	UP Pulse Width DMA WRITE	300			ns

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6102-1I ..... -40°C to +85°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... +4.0V to +7.0V
Supply Voltage ..... +8.0V
Voltage On Any Input or
Output Pin ..... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, T_A = -40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage[1]	GND≤V_{IN}≤V_{CC}	-1.0		1.0	μA
4	V_{OH}	Output Voltage High[2]	I_{OH} = -0.2mA	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			GND+0.01	V
6	I_{OL}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	μA
7	I_{CC}	Power Supply Current-Standby	V_{IN}=GND or V_{CC}			800	μA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 3.33MHz			2.0	mA
9	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
10	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE: 1. Except pins 15, 29, 31 2. Except pins 32, 33, 34.

A.C. CHARACTERISTICS

TEST CONDITIONS: 5.0V ± 10%, C_L = 50pF, T_A = -40°C to +85°C, f_C = 3.33MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{LIN}	LXMAR Pulse Width IN	250			ns
2	t_{AIS}	Address Setup Time IN: DX-LXMAR (↓)	70			ns
3	t_{AIH}	Address Hold Time IN: LXMAR(↓)-DX	100			ns
4	t_{DEN}	Data Output Enable Time: DEVSEL(↓)-DX			350	ns
5	t_{CEN}	Controls Output Enable Time: DEVSEL(↓)-lines C0,C1,C2,S/I			350	ns
6	t_{DIS}	Data Input Setup Time: DX-DEVSEL(↑)	100			ns
7	T_{DIH}	Data Input Hold Time: DEVSEL(↑)-DX	100			ns
8	t_{RST}	RESET Input Pulse Width	500			ns
9	t_{SID}	SKP/INTX to SKP/INT Propagation Delay			120	ns
10	t_{DMLX}	DMA Control Signals Delay: XTC-XTC*; MEMSEL-MEMSEL*, LXMAR-LXMAR*			120	ns
11	t_{DEM}	Enable/Disable Time from DMAGNT to EMA Lines			80	ns
12	t_{MDR}	MEMSEL* Pulse Width READ	550			ns
13	t_{MDW}	MEMSEL* Pulse Width WRITE	700			ns
14	t_{MDWR}	MEMSEL* Pulse Width WRITE/REFSH	400			ns
15	t_{LD}	LXMAR* Pulse Width	260			ns
16	t_{DRAT}	DMA READ Access Time: LXMAR*(↓)-UP(↑)	85			ns
17	t_{DXAS}	DX & EMA Address Setup Time Wrt LXMAR*(↓)	125			ns
18	t_{DXAH}	DX & EMA Address Hold Time Wrt LXMAR*(↓)	125			ns
19	t_{DREN}	DMA READ Enable Time: MEMSEL* (↓)-UP(↑)	400			ns
20	t_{RUP}	UP Pulse Width DMA READ	260			ns
21	t_{DWAT}	DMA WRITE Access Time: LXMAR*(↓)-MEMSEL*(↑)	550			ns
22	t_{DWEN}	DMA WRITE Enable Time: UP (↓)-MEMSEL*(↑)	400			ns
23	t_{MWS}	MEMSEL* Setup Time DMA WRITE MEMSEL*(↓)-LXMAR*(↓)	100			ns
24	t_{DMS}	DMAEN Setup Time Wrt XTA (↑)	100			ns
25	t_{DMH}	DMAEN Hold Time Wrt XTA (↑)	100			ns
26	t_{WUP}	UP Pulse Width DMA WRITE	550			ns

IM6102

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM6102 ..... -40°C to +85°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... +4.0V to +7.0V
Supply Voltage ..... +8.0V
Voltage On Any Input or
Output Pin ..... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, T_A = -40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage 1	$GND \le V_{IN} \le V_{CC}$	-1.0		1.0	μA
4	V_{OH}	Output Voltage High 2	I_{OH} = -0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OL}	Output Leakage	$GND \le V_{OUT} \le V_{CC}$	-1.0		1.0	μA
7	I_{CC}	Power Supply Current-Standby	V_{IN}=GND or V_{CC}		1.0	800	μA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 2.5MHz			1.8	mA
9	C_{IN}	Input Capacitance 1			7.0	8.0	pF
10	C_O	Output Capacitance 1			8.0	10.0	pF

NOTE: 1. Except pins 15, 29, 31 2. Except pins 32, 33, 34.

A.C. CHARACTERISTICS

TEST CONDITIONS: 5.0V ± 10%, C_L = 50pF, T_A = -40°C to +85°C, f_C = 2.5MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{LIN}	LXMAR Pulse Width IN	300			ns
2	t_{AIS}	Address Setup Time IN: DX-LXMAR (↓)	80			ns
3	t_{AIH}	Address Hold Time IN: LXMAR(↓)-DX	120			ns
4	t_{DEN}	Data Output Enable Time: DEVSEL(↓)-DX			400	ns
5	t_{CEN}	Controls Output Enable Time: DEVSEL(↓)-lines C0,C1,C2,S/I			400	ns
6	t_{DIS}	Data Input Setup Time: DX-DEVSEL(↑)	100			ns
7	T_{DIH}	Data Input Hold Time: DEVSEL(↑)-DX	100			ns
8	t_{RST}	RESET Input Pulse Width	500			ns
9	t_{SID}	SKP/INTX to SKP/INT Propagation Delay			150	ns
10	t_{DMLX}	DMA Control Signals Delay: XTC-XTC*; MEMSEL-MEMSEL*, LXMAR-LXMAR*			150	ns
11	t_{DEM}	Enable/Disable Time from DMAGNT to EMA Lines			100	ns
12	t_{MDR}	MEMSEL* Pulse Width READ	750			ns
13	t_{MDW}	MEMSEL* Pulse Width WRITE	950			ns
14	t_{MDWR}	MEMSEL* Pulse Width WRITE/REFSH	550			ns
15	t_{LD}	LXMAR* Pulse Width	350			ns
16	t_{DRAT}	DMA READ Access Time: LXMAR*(↓)-UP(↑)	750			ns
17	t_{DXAS}	DX & EMA Address Setup Time Wrt LXMAR*(↓)	120			ns
18	t_{DXAH}	DX & EMA Address Hold Time Wrt LXMAR*(↓)	175			ns
19	t_{DREN}	DMA READ Enable Time: MEMSEL* (↓)-UP(↑)	550			ns
20	t_{RUP}	UP Pulse Width DMA READ	350			ns
21	t_{DWAT}	DMA WRITE Access Time: LXMAR*(↓)-MEMSEL*(↑)	750			ns
22	t_{DWEN}	DMA WRITE Enable Time: UP (↓)-MEMSEL*(↑)	550			ns
23	t_{MWS}	MEMSEL* Setup Time DMA WRITE MEMSEL*(↓)-LXMAR*(↓)	100			ns
24	t_{DMS}	DMAEN Setup Time Wrt XTA (↑)	100			ns
25	t_{DMH}	DMAEN Hold Time Wrt XTA (↑)	100			ns
26	t_{WUP}	UP Pulse Width DMA WRITE	750			ns

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IM6102AM (Military)

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Military IM6102AM ..... -55°C to +125°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... +4.0V to +11.0V
Supply Voltage ..... +12.0V
Voltage On Any Input or
Output Pin ..... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, T_A = -55°C to +125°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage[1]	GND≤V_{IN}≤V_{CC}	-1.0		1.0	μA
4	V_{OH}	Output Voltage High[2]	I_{OH} = 0mA	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0mA			GND+0.01	V
6	I_{OL}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	μA
7	I_{CC}	Power Supply Current-Standby	V_{IN}=GND or V_{CC}			900	μA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 5.0MHz			4.0	mA
9	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
10	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE: 1. Except pins 15, 29, 31 . 2. Except pins 32, 33, 34.

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, C_L = 50pF, T_A = -55°C to +125°C, f_C = 5.0MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{LIN}	LXMAR Pulse Width IN	135			ns
2	t_{AIS}	Address Setup Time IN: DX-LXMAR (↓)	60			ns
3	t_{AIH}	Address Hold Time IN: LXMAR(↓)-DX	60			ns
4	t_{DEN}	Data Output Enable Time: DEVSEL(↓)-DX			260	ns
5	t_{CEN}	Controls Output Enable Time: DEVSEL(↓)-lines C0,C1,C2,S/I			260	ns
6	t_{DIS}	Data Input Setup Time: DX-DEVSEL(↑)	60			ns
7	T_{DIH}	Data Input Hold Time: DEVSEL(↑)-DX	60			ns
8	t_{RST}	RESET Input Pulse Width	250			ns
9	t_{SID}	SKP/INTX to SKP/INT Propagation Delay			120	ns
10	t_{DMLX}	DMA Control Signals Delay: XTC-XTC*; MEMSEL-MEMSEL*, LXMAR-LXMAR*			120	ns
11	t_{DEM}	Enable/Disable Time from DMAGNT to EMA Lines			60	ns
12	t_{MDR}	MEMSEL* Pulse Width READ	375			ns
13	t_{MDW}	MEMSEL* Pulse Width WRITE	475			ns
14	t_{MDWR}	MEMSEL* Pulse Width WRITE/REFSH	275			ns
15	t_{LD}	LXMAR* Pulse Width	175			ns
16	t_{DRAT}	DMA READ Access Time: LXMAR*(↓)-UP(↑)	375			ns
17	t_{DXAS}	DX & EMA Address Setup Time Wrt LXMAR*(↓)	70			ns
18	t_{DXAH}	DX & EMA Address Hold Time Wrt LXMAR*(↓)	70			ns
19	t_{DREN}	DMA READ Enable Time: MEMSEL* (↓)-UP(↑)	275			ns
20	t_{RUP}	UP Pulse Width DMA READ	175			ns
21	t_{DWAT}	DMA WRITE Access Time: LXMAR*(↓)-MEMSEL*(↑)	375			ns
22	t_{DWEN}	DMA WRITE Enable Time: UP (↓)-MEMSEL*(↑)	275			ns
23	t_{MWS}	MEMSEL* Setup Time DMA WRITE MEMSEL*(↓)-LXMAR*(↓)	50			ns
24	t_{DMS}	DMAEN Setup Time Wrt XTA (↑)	50			ns
25	t_{DMH}	DMAEN Hold Time Wrt XTA (↑)	50			ns
26	t_{WUP}	UP Pulse Width DMA WRITE	375			ns

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IM6102-1M (Military)

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Military IM6102-1M ..... -55°C to +125°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... +4.0V to +7.0V
Supply Voltage ..... +8.0V
Voltage On Any Input or
Output Pin ..... -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, C_L = 50pF, T_A = -55°C to +125°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC} -2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage[1]	$GND \le V_{IN} \le V_{CC}$	-1.0		1.0	μA
4	V_{OH}	Output Voltage High[2]	I_{OH} = 0mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0mA			0.45	V
6	I_{OL}	Output Leakage	$GND \le V_{OUT} \le V_{CC}$	-1.0		1.0	μA
7	I_{CC}	Power Supply Current-Standby	V_{IN}=GND or V_{CC}			800	μA
8	I_{CC}	Power Supply Current-Dynamic	f_C = 2.5MHz			2.0	mA
9	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
10	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE: 1. Except pins 15, 29, 31 2. Except pins 32, 33, 34.

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, T_A = -55°C to +125°C, f_C = 2.5MHz

	SYMBOL	PARAMETER	MIN	TYP	MAX	UNITS
1	t_{LIN}	LXMAR Pulse Width IN	300			ns
2	t_{AIS}	Address Setup Time IN: DX-LXMAR ↓	80			ns
3	t_{AIH}	Address Hold Time IN: LXMAR↓-DX	120			ns
4	t_{DEN}	Data Output Enable Time: DEVSEL↓-DX			400	ns
5	t_{CEN}	Controls Output Enable Time: DEVSEL↓-lines C0,C1,C2,S/I			400	ns
6	t_{DIS}	Data Input Setup Time: DX-DEVSEL↑	100			ns
7	T_{DIH}	Data Input Hold Time: DEVSEL↑-DX	100			ns
8	t_{RST}	RESET Input Pulse Width	500			ns
9	t_{SID}	SKP/INTX to SKP/INT Propagation Delay			130	ns
10	t_{DMLX}	DMA Control Signals Delay: XTC-XTC*; MEMSEL-MEMSEL*, LXMAR-LXMAR*			130	ns
11	t_{DEM}	Enable/Disable Time from DMAGNT to EMA Lines			100	ns
12	t_{MDR}	MEMSEL* Pulse Width READ	750			ns
13	t_{MDW}	MEMSEL* Pulse Width WRITE	950			ns
14	t_{MDWR}	MEMSEL* Pulse Width WRITE/REFSH	550			ns
15	t_{LD}	LXMAR* Pulse Width	350			ns
16	t_{DRAT}	DMA READ Access Time: LXMAR*↓-UP↓	750			ns
17	t_{DXAS}	DX & EMA Address Setup Time Wrt LXMAR*↓	120			ns
18	t_{DXAH}	DX & EMA Address Hold Time Wrt LXMAR*↓	175			ns
19	t_{DREN}	DMA READ Enable Time: MEMSEL*↓-UP↓	550			ns
20	t_{RUP}	UP Pulse Width DMA READ	350			ns
21	t_{DWAT}	DMA WRITE Access Time: LXMAR*↓-MEMSEL*↑	750			ns
22	t_{DWEN}	DMA WRITE Enable Time: UP↓-MEMSEL*↑	550			ns
23	t_{MWS}	MEMSEL* Setup Time DMA WRITE MEMSEL*↓-LXMAR*↓	100			ns
24	t_{DMS}	DMAEN Setup Time Wrt XTA ↑	100			ns
25	t_{DMH}	DMAEN Hold Time Wrt XTA ↑	100			ns
26	t_{WUP}	UP Pulse Width DMA WRITE	750			ns

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APPLICATION

IM6100-IM6102 Interface in a Buffered System.

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INTERSIL

IM6103 CMOS Parallel Input-Output Port (PIO)

FEATURES

- 20 Programmable I/O Pins
- TTL Compatible Inputs and Outputs
- Compatible with IM6100 Microprocessor Family
- Low Power Dissipation < 10 mW
- Extended Temperature Range, -40°C to +85°C
- Single Power Supply

GENERAL DESCRIPTION

The IM6103 is a Parallel Input-Output Port (PIO) device designed for use in IM6100 microcomputer systems. Its function is to provide a general purpose parallel I/O component to interface peripheral equipment to the IM6100 system bus. The functional configuration of the IM6103 is programmed by the user software so that normally no external logic is necessary to interface a wide variety of peripheral devices such as displays, printers, keyboards, etc. to an IM6100 microcomputer system.

A general purpose all-CMOS microcomputer system with 64 x 12 RAM, 1k x 12 ROM and 20 I/O lines can be built with just four CMOS LSI devices – IM6100 microprocessor, IM6512 (64 x 12) RAM, IM6312 (1k x 12) ROM and IM6103 PIO.

FUNCTIONAL BLOCK DIAGRAM

PIN CONFIGURATION

PACKAGE DIMENSIONS

ORDERING INFORMATION

PART NO.	TEMPERATURE RANGE	OPERATING VOLTAGE RANGE	PACKAGE
IM6103 AMDL	-55°C to +125°C	4-11V	40 Pin Ceramic
IM6103 AIDL	-40°C to +85°C	4-11V	40 Pin Ceramic
IM6103 AIPL	-40°C to +85°C	4-11V	40 Pin Plastic
IM6103 IPL	-40°C to +85°C	4-7V	40 Pin Plastic
IM6103 CPL	0°C to +70°C	4-7V	40 Pin Plastic
IM6103 MDL	-55°C to +125°C	4-7V	40 Pin Ceramic
IM6103 IDL	-40°C to +85°C	4-7V	40 Pin Ceramic

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ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IM61031 . . . . . -40°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Supply Voltage . . . . . +12V
Voltage on Any Input or Output Pin With Respect to GND . . . . . -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = Industrial

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Logical "1" Input Voltage		V_{CC}–1.7			V
2	V_{IL}	Logical "0" Input Voltage				0.8	
3	I_{IL}	Input Leakage	$0V \leqslant V_{IN} \leqslant V_{CC}$	-1.0		1.0	μA
4	V_{OH}	Logical "1" Output Voltage	I_{OUT} = 0 except pins 6, 9	V_{CC}–1.0			V
5	V_{OL}	Logical "0" Output Voltage	I_{OUT} = 0			0.45	
6	I_O	Output Leakage	$0V \leqslant V_O \leqslant V_{CC}$	-1.0		1.0	μA
7	I_{CC}	Supply Current	V_{CC} = 5V C_L = 50 pF; T_A = 25°C F_{CLOCK} = Operating Frequency			2.5	mA
8	C_{IN}	Input Capacitance			7.0	8.0	pF
9	C_O	Output Capacitance			8.0	10.0	

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -40°C to +85°C, C_L = 50pF, All times in ns.

	SYMBOL	PARAMETER		MIN	MAX	UNITS
1	t_{ADDS}	Address Set-Up Time	DX–LXMAR↓	110		ns
2	t_{ADDH}	Address Hold Time	LXMAR↓–DX	150		
3	t_{DEN}	Output Enable Time	DEVSEL↓–DX		550	
4	t_{DC}	Output Enable Time	DEVSEL↓–C_1		550	
5	t_{DI}	Output Enable Time	DEVSEL↓–SKP		400	
6	t_{DS}	Data Set-Up Time	DX–DEVSEL↑	200		
7	t_{DH}	Data Hold Time	DEVSEL↑–DX	150		
8	t_{PS}	Data In Set-Up Time	Port Data In–LXMAR↓	200		
9	t_{PH}	Data In Hold Time	LXMAR↓–Port Data In	225		
10	t_{D1}	Delay Time	DEVSEL↑–Port Data Out		550	
11	t_{BS}	Data In Set-Up Time	Port B In–IRS↓	200		
12	t_{BH}	Data In Hold Time	IRS↓–Port B In	150		
13	t_{D2}	Output Enable Time	ORS↑–Port B Out		550	
14	t_{D2}	Output Disable Time	ORS↓–Port B Out		200	
15	t_{D3}	Delay Time	IRS↓–IRE↓ ORS↓–ORF↓ DEVSEL↑–IRE↑ DEVSEL↑–ORF↑		550	

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ABSOLUTE MAXIMUM RATINGS

Operating Temperature
Industrial IMM6103I. . . . . -40°C to +85°C
Storage Temperature . . . . . -65°C to +150°C
Supply Voltage . . . . . +8V
Voltage on Any Input or Output Pin With Respect to GND . . . . . -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

DC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = Industrial

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Logical "1" Input Voltage		V_{CC}-1.7			V
2	V_{IL}	Logical "0" Input Voltage				0.8	V
3	I_{IL}	Input Leakage	$0V \leqslant V_{IN} \leqslant V_{CC}$	-1.0		1.0	μA
4	V_{OH}	Logical "1" Output Voltage	I_{OH} = -0.2 mA except pins 6,9	V_{CC}-1.0			V
5	V_{OL}	Logical "0" Output Voltage	I_{OL} = 2.0 mA			0.45	V
6	I_O	Output Leakage	$0V \leqslant V_O \leqslant V_{CC}$	-1.0		1.0	μA
7	I_{CC}	Supply Current	V_{CC} = 5.0V C_L = 50 pF; T_A = 25°C F_{CLOCK} = Operating Frequency			2.5	mA
8	C_{IN}	Input Capacitance			7.0	8.0	pF
9	C_O	Output Capacitance			8.0	10.0	pF

AC CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5V ± 10%, T_A = -40°C to +85°C, C_L = 50pF, All times in ns.

	SYMBOL	PARAMETER		MIN	MAX	UNITS
1	t_{ADDS}	Address Set-Up Time	DX–LXMAR↓	80		ns
2	t_{ADDH}	Address Hold Time	LXMAR↓–DX	100		ns
3	t_{DEN}	Output Enable Time	DEVSEL↓–DX		450	ns
4	t_{DC}	Output Enable Time	DEVSEL↓–C_1		450	ns
5	t_{DI}	Output Enable Time	DEVSEL↓–SKP		330	ns
6	t_{DS}	Data Set-Up Time	DX–DEVSEL↑	150		ns
7	t_{DH}	Data Hold Time	DEVSEL↑–DX	100		ns
8	t_{PS}	Data In Set-Up Time	Port Data In–LXMAR↓	150		ns
9	t_{PH}	Data In Hold Time	LXMAR↓–Port Data In	175		ns
10	t_{D1}	Delay Time	DEVSEL↑–Port Data Out		450	ns
11	t_{BS}	Data In Set-Up Time	Port B in–IRS↓	150		ns
12	t_{BH}	Data In Hold Time	IRS↓–Port B In	100		ns
13	t_{D2}	Output Enable Time	ORS↑–Port B Out		450	ns
14	t_{D2}	Output Disable Time	ORS↓–Port B Out		200	ns
15	t_{D3}	Delay Time	IRS↓–IRE↓ ORS↓–ORF↓ DEVSEL↑–IRE↑ DEVSEL↑–ORF↑		450	ns

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FIGURE 1: Functional Block Diagram.

IM6103 FUNCTIONAL PIN DEFINITION

PIN NUMBER	SYMBOL	INPUT/ OUTPUT	DESCRIPTION
1	V_{CC}		Positive Power Supply
2	PA_7	I/O	Port A I/O Line (4). Most Significant Bit of Port A in Mode 10.
	PC_{11}	I/O	Port C I/O Line (8) in Mode 11/OX—Most Significant Bit.
3 ~ 5	$PA_6 \sim PA_4$	I/O	Port $A_5 \sim A_7$ (Mode 10).
	$PC_{10} \sim PC_8$	I/O	Port $C_9 \sim C_{11}$ (Mode 11/OX).
6	SKP/INT	O	Time Multiplexed SKP and INTREQ lines to the IM6100 Microprocessor – Active Low.
7	PA_8	I/O	Port A I/O Line in Mode 11/10 – Most Significant Bit of Port A in Mode 11.
	IRS	O	Input Register Strobe to clock data into Port B in Handshake Mode (Mode OX). Port B Latches in the data on the falling edge of IRS (IRS↓).
8	PA_9	I/O	Port A_9 (Mode 11/10).
	IRE	O	Input Register Empty output goes high when Port B input buffer has been read by the IM6100 microprocessor. It goes low when Port B input buffers are strobed in by IRS↓. (Mode OX). PIO may be programmed to generate an INTREQ on IRE↓.

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IM6103 FUNCTIONAL PIN DEFINITION (Continued)

PIN NUMBER	SYMBOL	INPUT/ OUTPUT	DESCRIPTION
9	C_1	O	C_1 output goes low upon completion of PIO Port data transfer to the IM6100 Accumulator (AC). This output is an open-drain output to be wire-OR'D with C_1 Lines from other IM6100 peripheral controllers.
10	LXMAR	I	Address Latch enable signal from the IM6100. PIO clocks in address and control information from the IM6100 on the falling edge of LXMAR (LXMAR↓). All Port inputs are sampled at LXMAR↓.
11	PA_{10}	I/O	Port A_{10} (Mode 11/10).
	ORS	I	Output Register Strobe input to enable Port B output buffers in Mode OX. Port B is tristated when ORS is low.
12	DEVSEL	I	Input-Output Device Select control line from the IM6100. It performs both the read and write function. The first negative transition after LXMAR↓, enables the DX output buffers of the selected PIO for a 'read' operation. When DEVSEL returns high, the 'read' operation is terminated. The second negative-going pulse on DEVSEL serves as a 'write' pulse to the selected PIO and the IM6100 AC data is written into the selected PIO register or port on the rising edge.
13	PA_{11}	I/O	Port A_{11} (Mode 11/10)—Least Significant bit of Port A.
	ORF	O	Output Register Full output goes high when the IM6100 writes into Port B in a handshake mode. It goes low when the peripheral device reads Port B by enabling ORS high. The PIO may be programmed to generate an INTREQ on ORF↓ (Mode OX).
14	SEL_6	I	A Chip Select Input. PIO has two chip selects, SEL_6 and SEL_7, thereby enabling up to four PIO chips in a system.
15	SEL_7	I	A Chip Select Input.
16 ~ 25	$DX_0 \sim DX_9$	I/O	The IM6100 System bus (Data and Address).
26	GND		Ground
27 ~ 28	$DX_{10} \sim DX_{11}$	I/O	IM6100 System bus (Data and Address).
29 ~ 40	$PB_0 \sim PB_{11}$	I/O	I/O Port Pin. PB_0 is the most significant bit, and PB_{11} is the least significant bit.

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IM6100 SYSTEM TIMING

The tristate bidirectional 12-bit DX bus is used to transfer data and control information (Figure 3) between the IM6103 and the IM6100 microprocessor. The IM6100 transmits the device address and control information on the DX bus during the 'execute' phase of an Input-Output Transfer (IOT) instruction. The IM6103 accepts this information on the falling edge of the LXMAR (Address Latch Enable) Signal.

The address bits (6-7) are compared with the chip select inputs (SEL_6 and SEL_7) to address 1 of 4 PIO's. The IOT address bits (3-5) are programmed internally to respond to the bit pattern 011. The SEL_6 and SEL_7 inputs should be externally hard-wired to match the DX_6 and DX_7 chip select bits. As shown in Fig. 3, DEVSEL goes low, during the first half of an IOT execute machine cycle for a read operation and it goes low again in the second half for a write operation. The IM6103 responds to a 'read' instruction by putting data on the DX bus and C_1 output (of IM6103) low when DEVSEL (from IM6100) input is low. C_1 line goes low to indicate an input transfer cycle to the IM6100. All PIO data transfers to the IM6100 Accumulator (AC) is an 'OR' transfer, (i.e., PIO data is OR'ed into the contents of the AC).

During the write operation into PIO, the PIO accepts data from the IM6100 Accumulator on the rising edge of the DEVSEL. During and after the PIO write, the contents of the accumulator are not cleared.

SKP/INT line goes low during the 'read' DEVSEL if the IM6103 is responding to a 'skip' instruction, and the 'skip' condition is met, therefore causing the IM6100 to skip the next sequential instruction. SKP/INT line reflects the interrupt request status of the IM6100 at all times except during the 'read' DEVSEL. The SKP/INT line goes low if an active interrupt request is pending. During read DEVSEL mode, the SKP/INT indicates the current skip condition. The bits are interpreted as shown below:

FIGURE 2: PIO instruction format.

FIGURE 3: IM6103 system timing diagram.

OPERATION OF PORT BUFFERS

The IM6103 has 20 I/O pins which can be individually programmed in groups of 4, 8 or 12 bits in three different modes of operation.

In Mode 11, the 20 I/O lines are divided into three ports:
–Port A with 4 bits (PA_8-PA_{11})
–Port B with 12 bits (PB_0-PB_{11})
–Port C with 4 bits (PC_8-PC_{11})

In Mode 10, the 20 I/O lines are grouped into 2 ports–
–Port A with 8 bits (PA_4-PA_{11})
–Port B with 12 bits (PB_0-PB_{11})
–The four I/O lines associated with Port C in Mode 11 (PC_8-PC_{11}) are allocated to Port A as PA_4-PA_7.

In Mode OX, there are two ports—Port B with 12 bits and Port C with 4 bits and four lines for handshake control logic. Four lines of Port A in Mode 11 (PA_8-PA_{11}) are reassigned as handshake control lines. They are:
—Input Register Strobe (IRS)
—Input Register Empty (IRE)
—Output Register Strobe (ORS)
—Output Register Empty (ORE)
The handshake logic controls the data transfer for the Port B. Port C operation remains the same as in Mode 11.

For an 'input' transfer in OX Mode, the input register empty (IRE) output goes high to indicate to the peripheral device that the input register is empty (as shown in Fig. 4). The peripheral device may then strobe in the new data into Port B with Input Register Strobe (IRS). At this time, IRE goes low to indicate to the peripheral device that the input buffer is full, and remains low until Port B has been read by the IM6100 microprocessor. IRE then goes high after the IM6100 executes a Read Port B (RPB) instruction to initiate another input sequence. The data into Port B should be valid only for a short duration before and after IRS makes the 1 to 0 transition.

FIGURE 4: Input data transfer (peripheral device to PIO).

For an 'output' transfer in OX mode, the IM6100 microprocessor writes the data into Port B and its timing is shown in Figure 5. ORF line from the PIO goes high, signaling the peripheral device that the output register is full. The peripheral device may then strobe in the new data from Port B with ORS. Port B stays in the high impedance mode until ORS is activated by the peripheral device. ORF line goes low and remains low until Port B has been written into by the IM6100 microprocessor. ORF then goes high, initiating another output sequence.

FIGURE 5: Output data transfer (PIO to peripheral device).

The IM6100 monitors the status of ORF (Output Register Full). If it is low (i.e., output register is empty), IM6100 may load data into Port B output buffer with SPB/CPB/WPB instruction. ORF goes high a delay time after the rising edge of the 'write' DEVSEL, signaling the peripheral device that output buffer has new data. During this time, Port B output buffers remain tristated. The peripheral device may then enable and read out Port B output latches by activating ORS (Output Register Strobe) high. The falling edge of ORS (from high to low) signals the PIO that the peripheral device no longer needs the valid current information. Port B is tristated and ORF then goes low, thereafter, to indicate another output sequence.

ORF should be set to 0 and IRE to 1 with a 'write' command in Mode OX, to initiate the handshaking sequence.

The IM6100 microprocessor should not write into Port B until ORF is low for an 'output' transfer and should not read Port B until IRE is low for an 'input' transfer. The peripheral device reads Port B if ORF is high and writes into Port B if IRE is high.

The PIO may be programmed to generate an INTREQ (Interrupt Request) to the microprocessor when ORF or IRE goes low by setting the respective Interrupt enable bits, OREN and IREN.

The IM6100 may poll the status of ORF or IRE by executing the respective skip instructions SKPOR and SKPIR, by reading the status register or by reading "Port A".

In Mode 11 and 10, when handshaking control is not in effect, the execution of SKPOR and SKPIR Instructions depend on the state of the Port A lines PA_{11} and PA_9, respectively. The Interrupt feature is available only in Mode OX.

The mode of operation — 11, 10 or OX, is selected by programming the Status Register (SR).

All ports are bidirectional. The execution of a 'write' instruction caused a port to be automatically programmed to be an 'output'. The output data may be changed by using the 'set', 'clear' or 'write' instructions. The output remains valid until the port bit lines are reset to be inputs.

Execution of a 'read' instruction causes a port to be automatically set as an 'input' port — i.e., it presents a very high impedance to the I/O lines. Data appearing on the I/O lines will be sampled into the port input latch at every LXMAR pulse and may be read by the IM6100 microprocessor by the 'read' instruction.

In Mode OX, Port B acts as a tristate bidirectional buffer which is controlled by an external peripheral device. ORF and IRE lines are outputs and ORS and IRS lines are inputs.

At power-on, all ports are defined to be input ports and the PIO is initialized to be in Mode 10. With 20 I/O lines partitioned into the 8/12 (i.e., Port A = 8 bits, Port B = 12 bits) format.

STATUS REGISTER

The Status Register (SR) has 2 mode bits, M_8 and M_9 which can be modified by the WSR (Write Status Register) instruction. These two bits define the mode of operation for the IM6103 as shown in Figure 8.

M_8	M_9	MODE	PORT OPERATION
0	*	Mode OX	PB_{0-11}, PC_{8-11}, IRS, IRE, ORS, ORF
1	0	Mode 10	PB_{0-11}, PA_{4-11}
1	1	Mode 11	PB_{0-11}, PC_{8-11}, PA_{8-11}

FIGURE 8: Mode bit assignments.

The Mode and Interrupt status bits, ORINT (Output Register empty Interrupt) and IRINT (Input Register empty Interrupt), may be read with the RSR (Read Status Register) instruction. The interrupt status bits are set to 0 if the corresponding flag is requesting an interrupt.

In Mode 11/10 the current value of PA_{11} and PA_9 can be interrogated. In this mode, Port A can be either an input or an output. M_8 and M_9 are initialized to "11" at power-on.

DX_8	DX_9	DX_{10}	DX_{11}	DX	BUS
M_8	M_9	ORINT	IRINT	SR	MODE OX READ
M_8	M_9	PA_{10}	PA_9	SR	MODE 11/10 READ
M_8	M_9			SR	MODE 11/10/OX WRITE

FIGURE 9: Status register bit assignments.

SKIP OPERATION

The IM6100 may poll the status of ORF or IRE in Mode OX, by executing a skip instruction, SKPOR or SKPIR. The IM6103 will assert the SKP/INT line low if the corresponding status line (ORF or IRE) is low, causing the next sequential instruction to be skipped. During this cycle, ORF and IRE remain unchanged.

In Mode 11/10, SKPOR and SKPIR instruction executions depend on the state of PA_{11} and PA_9, respectively. Port A may be an input or output port.

If ORF is reset to 0 by executing a CLRPA or WPA instruction to initiate the handshaking sequence, the next SKPOR instruction will cause the next sequential instruction to be skipped.

INTERRUPT OPERATION

The IM6103 may be programmed to generate an interrupt request input (INTREQ) when ORF or IRE goes low, by setting the corresponding interrupt enable bits, OREN or IREN, to 1. If the IM6100 interrupt system has been previously enabled, the microprocessor will acknowledge the INTREQ input. If the IM6100 μP does not see the higher priority INTREQ's, inputs from other peripheral controllers such as IM6102 Memory Extender/Direct Memory Access/Internal Timer Controller (MEDIC) or IM6101 Parallel Interface Elements (PIE) in the system, the interrupt service routine should initiate a software poll of the PIO's in the system to identify the particular PIO that generated the INTREQ. In Mode OX, the interrupt request status of ORF and IRE may be identified by reading the Status Register. ORINT or IRINT will be set to 0 if ORF (being low) or IRE (being low) is generating an INTREQ. Note that IM6102 MEDIC and IM6101 PIE provide an automatic priority vectoring.

The interrupt feature of IM6103 is available only in Mode OX. An ORF INTREQ may be removed by one of the following methods:

- executing a SPB/CPB/WPB Instruction (ORF goes high if Port B is written into), or
- setting ORF to 1 with SPA/WPA Instruction, or
- by resetting OREN to 0 with a CPA/WPA Instruction, or
- by changing to Mode 11/10.

An IRE INTREQ may be removed by:

- executing a RPB Instruction (IRE goes high after Port B is read), or
- setting IRE to 1 with SPA/WPA Instructions, or
- resetting IREN to 0 with a CPA/WPA Instruction, or
- changing to Mode 11/10.

PIO may be software programmed to generate an INTREQ to the IM6100 by resetting ORF or IRE to 0 with a CPA/WPA Instruction and by setting the corresponding enable bit, OREN or IREN, with a SPA/WPA Instruction in Mode OX.

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PIO INSTRUCTION

NOTE: Symbol Definition – "•" - AND
"+" - OR
"=" - Is Replaced By

PIO CONTROL	MNEMONICS	DESCRIPTION
0 0 0 0	SETPA (Set Port A)	Set PA_i to 1 if AC_i is 1. AC is not cleared. Mode 11: $PA_i=PA_i+AC_i$, $8 \leq i \leq 11$ Mode 10: $PA_i=PA_i+AC_i$, $4 \leq i \leq 11$ Mode OX: IREN = IREN + AC_8 IRE = IRE + AC_9 OREN = OREN + AC_{10} ORF = ORF + AC_{11}
0 0 0 1	CLRPA	Clear Port A. Clear PA_i to 0 if AC_i is 1. AC is not cleared. Mode 11: $PA_i=PA_i \bullet \overline{AC_i}$, $8 \leq i \leq 11$ Mode 10: $PA_i=PA_i \bullet \overline{AC_i}$, $4 \leq i \leq 11$ Mode OX: IREN = IREN $\bullet \overline{AC_8}$ IRE = IRE $\bullet \overline{AC_9}$ OREN = OREN $\bullet \overline{AC_{10}}$ ORF = ORF $\bullet \overline{AC_{11}}$
0 0 1 0	WPA	Write Port A. Set PA_i equal to AC_i. AC is not cleared. Mode 11: $PA_i=AC_i$, $8 \leq i \leq 11$ Mode 10: $PA_i=AC_i$, $4 \leq i \leq 11$ Mode OX: IREN = AC_8 IRE = AC_9 OREN = AC_{10} ORF = AC_{11}
0 0 1 1	RPA	Read Port A. 'OR' transfer PA to AC. Mode 11: $AC_i=AC_i+PA_i$, $8 \leq i \leq 11$ $AC_i=AC_i$, $0 \leq i \leq 7$ Mode 10: $AC_i=AC_i+PA_i$, $4 \leq i \leq 11$ $AC_i=AC_i$, $0 \leq i \leq 3$ Mode OX: $AC_8=AC_8+$ IRS $AC_9=AC_9+$IRE $AC_{10}=AC_{10}+$ORS $AC_{11}=AC_{11}+$ORF $AC_i=AC_i$, $0 \leq i \leq 7$
0 1 0 0	SETPB	Set Port B. Set PB_i to 1 if AC_i is 1. AC is not cleared. $PB_i=PB_i+AC_i$, $0 \leq i \leq 11$
0 1 0 1	CLRPB	Clear Port B. Clear PB_i to 0 if AC_i is 1. AC is not cleared. $PB_i=PB_i \bullet \overline{AC_i}$, $0 \leq i \leq 11$
0 1 1 0	WPB	Write Port B. Set PB_i equal to AC_i. AC is not cleared. $PB_i=AC_i$, $0 \leq i \leq 11$

PIO CONTROL	MNEMONICS	DESCRIPTION
0 1 1 1	RPB	Read Port B. 'OR' transfer PB to AC. $AC_i=AC_i+PB_i$, $0 \leq i \leq 11$
1 0 0 0	SETPC	Set Port C. Set PC_i to 1 if AC_i is 1. AC is not cleared. Mode 11 and OX: $PC_i=PC_i+AC_i$ $8 \leq i \leq 11$ Mode 10: No operation
1 0 0 1	CLRPC	Clear Port C. Clear PC_i to 0 if AC_i is 1. AC is not cleared. Mode 11 and OX: $PC_i=PC_i \bullet \overline{AC_i}$ $8 \leq i \leq 11$ Mode 10: No operation
1 0 1 0	WPC	Write Port C. Set PC_i equal to AC_i. AC is not cleared. Mode 11 and OX: $PC_i=AC_i$ $8 \leq i \leq 11$ Mode 10: No operation
1 0 1 1	RPC	Read Port C. 'OR' transfer PC to AC. Mode 11 and OX: $AC_i=AC_i+PC_i$ $8 \leq i \leq 11$ Mode 10: No operation
1 1 0 0	SKPOR	Skip the next sequential instruction if PA_{11}/ORF is low. Mode 11 and 10: Skip if PA_{11} is low. Mode OX: Skip if ORF is low.
1 1 0 1	SKPIR	Skip the next sequential instruction if PA_9/IRE is low. Mode 11 and 10: Skip if PA_9 is low. Mode OX: Skip if IRE is low.
1 1 1 0	WSR	Write Status Register. AC is not cleared. $M_8 = AC_8$ $M_9 = AC_9$
1 1 1 1	RSR	Read Status Register. 'OR' transfer Status register to AC. $AC_8 = AC_8 + M_8$ $AC_9 = AC_9 + M_9$ $AC_i = AC_i$, $0 \leq i \leq 7$ Mode 11 and 10: $AC_{10}=AC_{10}+PA_{11}$ $AC_{11}=AC_{11}+PA_9$ Mode OX: $AC_{10}=AC_{10}+$ORINT $AC_{11}=AC_{11}+$IRINT

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DX_0	DX_1	DX_2	DX_3	DX_4	DX_5	DX_6	DX_7	DX_8	DX_9	DX_{10}	DX_{11}	DX BUS
1	1	0	0	1	1	SEL_6	SEL_7	I_8	I_9	I_{10}	I_{11}	PIO INSTRUCTION
0	0	0	0	0	0	0	0	PA_8	PA_9	PA_{10}	PA_{11}	PORT A MODE 11 READ
								PA_8	PA_9	PA_{10}	PA_{11}	PORT A MODE 11 WRITE
0	0	0	0	PA_4	PA_5	PA_6	PA_7	PA_8	PA_9	PA_{10}	PA_{11}	PORT A MODE 10 READ
				PA_4	PA_5	PA_6	PA_7	PA_8	PA_9	PA_{10}	PA_{11}	PORT A MODE 10 WRITE
0	0	0	0	0	0	0	0	IRS	IRE	ORS	ORF	PORT A MODE OX READ
								IREN	IRE	OREN	ORF	PORT A MODE OX WRITE
PB_0	PB_1	PB_2	PB_3	PB_4	PB_5	PB_6	PB_7	PB_8	PB_9	PB_{10}	PB_{11}	PORT B MODE 11/10/OX READ/WRITE
0	0	0	0	0	0	0	0	PC_8	PC_9	PC_{10}	PC_{11}	PORT C MODE 11/OX READ
								PC_8	PC_9	PC_{10}	PC_{11}	PORT C MODE 11/OX WRITE
0	0	0	0	0	0	0	0	M_8	M_9	PA_{11}	PA_9	STATUS REG MODE 11/10 READ
0	0	0	0	0	0	0	0	M_8	M_9	ORINT	IRINT	STATUS REG MODE OX READ
								M_8	M_9			STATUS REG MODE 11/10/OX WRITE

FIGURE 6: IM6103 PIO register bit assignments.

PINS	2	3	4	5	7	8	11	13	29	30	31	32	33	34	35	36	37	38	39	40
MODE 10	PA_7	PA_6	PA_5	PA_4	PA_8	PA_9	PA_{10}	PA11	PB_0	PB_1	PB_2	PB_3	PB_4	PB_5	PB_6	PB_6	PB_8	PB_9	PB_{10}	PB_{11}
MODE 11	PC_{11}	PC_{10}	PC_9	PC_8	PA_8	PA_9	PA_{10}	PA_{11}	PB_0	PB_1	PB_2	PB_3	PB_4	PB_5	PB_6	PB_7	PB_8	PB_9	PB_{10}	PB_{11}
MODE OX	PC_{11}	PC_{10}	PC_9	PC_8	IRS	IRE	ORS	ORF	PB_0	PB_1	PB_2	PB_3	PB_4	PB_5	PB_6	PB_7	PB_8	PB_9	PB_{10}	PB_{11}

FIGURE 7: IM6103 PIO port pin assignments.

FIGURE 10: IM6103 PIO timing diagram.

FIGURE 11: Input data transfer (peripheral device to PIO).

FIGURE 12: Output data transfer (PIO to peripheral device).

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APPLICATION OF IM6103

Figure 13 illustrates a microcomputer system block diagram using IM6103 in a dual processor system.

FIGURE 13: Dual processor system with shared memory.

INTERSIL

IM6402/IM6403 Universal Asynchronous Receiver Transmitter (UART)

FEATURES

- **Low Power — Less Than 10mW Typ. at 2MHz**
- **Operation Up to 4MHz Clock — IM6402A**
- **Programmable Word Length, Stop Bits and Parity**
- **Automatic Data Formatting and Status Generation**
- **Compatible with Industry Standard UART's — IM6402**
- **On-Chip Oscillator with External Crystal — IM6403**
- **Operating Voltage —**
  - **— IM6402-1/03-1: 4-7V**
  - **— IM6402A/03A: 4-11V**
  - **— IM6402/03: 4-7V**

GENERAL DESCRIPTION

The IM6402 and IM6403 are CMOS/LSI UART's for interfacing computers or microprocessors to asynchronous serial data channels. The receiver converts serial start, data, parity and stop bits to parallel data verifying proper code transmission, parity, and stop bits. The transmitter converts parallel data into serial form and automatically adds start, parity, and stop bits.

The data word length can be 5, 6, 7 or 8 bits. Parity may be odd or even. Parity checking and generation can be inhibited. The stop bits may be one or two (or one and one-half when transmitting 5 bit code). Serial data format is shown in Figure 7.

The IM6402 and IM6403 can be used in a wide range of applications including modems, printers, peripherals and remote data acquisition systems. CMOS/LSI technology permits operating clock frequencies up to 4.0MHz (250K Baud) an improvement of 10 to 1 over previous PMOS UART designs. Power requirements, by comparison, are reduced from 670mW to 10mW. Status logic increases flexibility and simplifies the user interface.

The IM6402 differs from the IM6403 on pins 2, 17, 19, 22, and 40 as shown in Figure 5. The IM6403 utilizes pin 2 as a crystal divide control and pins 17 and 40 for an inexpensive crystal oscillator. TBREmpty and DReady are always active. All other input and output functions of the IM6402 and IM6403 are identical.

PIN CONFIGURATION

*See Table 1

TABLE 1

PIN	IM6402	IM6403 w/XTAL	IM6403 w/EXT CLOCK
2	N/C	DIVIDE CONTROL	DIVIDE CONTROL
17	RRC	XTAL	EXTERNAL CLOCK INPUT
40	TRC	XTAL	GND

ORDERING INFORMATION

ORDER CODE	IM6402-1/03-1	IM6402A/03A	IM6402/03
PLASTIC PKG	IM6402-1/03-1IPL	IM6402/03-AIPL	IM6402/03-IPL
CERAMIC PKG	IM6402-1/03-1IDL	IM6402/03-AIDL	—
MILITARY TEMP.	IM6402-1/03-1MDL	IM6402/03-AMDL	—
MILITARY TEMP. WITH 883B	IM6402-1/03-1 MDL/883B	IM6402/03-AMDL/ 883B	—

PACKAGE DIMENSIONS

40 PIN PLASTIC DUAL-IN-LINE PACKAGE (PL)

40 PIN CERAMIC DUAL-IN-LINE PACKAGE (DL)

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*DIFFERS BETWEEN IM6402 AND IM6403.

FIGURE 1. Pin Configuration

IM6403 FUNCTIONAL PIN DEFINITION

PIN	SYMBOL	DESCRIPTION
1	V_{CC}	Positive Power Supply
2	IM6402-N/C IM6403-Control	No Connection Divide Control High: 2^4 (16) Divider Low: 2^{11} (2048) Divider
3	GND	Ground
4	RRD	A high level on RECEIVER REGISTER DISABLE forces the receiver holding register outputs RBR1-RBR8 to a high impedance state.
5	RBR8	The contents of the RECEIVER BUFFER REGISTER appear on these three-state outputs. Word formats less than 8 characters are right justified to RBR1.
6	RBR7	See Pin 5 — RBR8
7	RBR6	See Pin 5 — RBR8
8	RBR5	See Pin 5 — RBR8
9	RBR4	See Pin 5 — RBR8
10	RBR3	See Pin 5 — RBR8
11	RBR2	See Pin 5 — RBR8
12	RBR1	See Pin 5 — RBR8
13	PE	A high level on PARITY ERROR indicates that the received parity does not match parity programmed by control bits. The output is active until parity matches on a succeeding character. When parity is inhibited, this output is low.

IM6403 FUNCTIONAL PIN DEFINITION (Continued)

PIN	SYMBOL	DESCRIPTION
14	FE	A high level on FRAMING ERROR indicates the first stop bit was invalid. FE will stay active until the next valid character's stop bit is received.
15	OE	A high level on OVERRUN ERROR indicates the data received flag was not cleared before the last character was transferred to the receiver buffer register. The Error is reset at the next character's stop bit if $\overline{DRR}$ has been performed (i.e., $\overline{DRR}$: active low).
16	SFD	A high level on STATUS FLAGS DISABLE forces the outputs PE, FE, OE, DR,* TBRE* to a high impedance state. See Figure 4 and Figure 5. *IM6402 only.
17	IM6402-RRC IM6403-XTAL or EXT CLK IN	The RECEIVER REGISTER CLOCK is 16X the receiver data rate.
18	$\overline{DRR}$	A low level on DATA RECEIVED RESET clears the data received output (DR), to a low level.
19	DR	A high level on DATA RECEIVED indicates a character has been received and transferred to the receiver buffer register.
20	RRI	Serial data on RECEIVER REGISTER INPUT is clocked into the receiver register.
21	MR	A high level on MASTER RESET (MR) clears PE, FE, OE, DR, TRE and sets TBRE, TRO high. Less than 18 clocks after MR goes low, TRE returns high. MR does not clear the receiver buffer register, and is required after power-up.
22	TBRE	A high level on TRANSMITTER BUFFER REGISTER EMPTY indicates the transmitter buffer register has transferred its data to the transmitter register and is ready for new data.
23	$\overline{TBRL}$	A low level on TRANSMITTER BUFFER REGISTER LOAD transfers data from inputs TBR1-TBR8 into the transmitter buffer register. A low to high transition on $\overline{TBRL}$ requests data transfer to the transmitter register. If the transmitter register is busy, transfer is automatically delayed so that the two characters are transmitted end to end. See Figure 2.
24	TRE	A high level on TRANSMITTER REGISTER EMPTY indicates completed transmission of a character including stop bits.
25	TRO	Character data, start data and stop bits appear serially at the TRANSMITTER REGISTER OUTPUT.

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IM6403 FUNCTIONAL PIN DEFINITION (Continued)

PIN	SYMBOL	DESCRIPTION
26	TBR1	Character data is loaded into the TRANSMITTER BUFFER REGISTER via inputs TBR1-TBR8. For character formats less than 8-bits, the TBR8, 7, and 6 Inputs are ignored corresponding to the programmed word length.
27	TBR2	See Pin 26 — TBR1
28	TBR3	See Pin 26 — TBR1
29	TBR4	See Pin 26 — TBR1
30	TBR5	See Pin 26 — TBR1
31	TBR6	See Pin 26 — TBR1
32	TBR7	See Pin 26 — TBR1
33	TBR8	See Pin 26 — TBR1
34	CRL	A high level on CONTROL REGISTER LOAD loads the control register. See Figure 3.

IM6403 FUNCTIONAL PIN DEFINITION (Continued)

PIN	SYMBOL	DESCRIPTION
35	PI*	A high level on PARITY INHIBIT inhibits parity generation, parity checking and forces PE output low.
36	SBS*	A high level on STOP BIT SELECT selects 1.5 stop bits for a 5 character format and 2 stop bits for other lengths.
37	CLS2*	These inputs program the CHARACTER LENGTH SELECTED. (CLS1 low CLS2 low 5-bits) (CLS1 high CLS2 low 6-bits) (CLS1 low CLS2 high 7-bits) (CLS1 high CLS2 high 8-bits)
38	CLS1*	See Pin 37 — CLS2
39	EPE*	When PI is low, a high level on EVEN PARITY ENABLE generates and checks even parity. A low level selects odd parity.
40	IM6402-TRC IM6403-XTAL or GND	The TRANSMITTER REGISTER CLOCK is 16X the transmit data rate.

*See Table 2 (Control Word Function)

TABLE 2. Control Word Function

CONTROL WORD					DATA BITS	PARITY BIT	STOP BIT(S)
CLS2	CLS1	PI	EPE	SBS			
L	L	L	L	L	5	ODD	1
L	L	L	L	H	5	ODD	1.5
L	L	L	H	L	5	EVEN	1
L	L	L	H	H	5	EVEN	1.5
L	L	H	X	L	5	DISABLED	1
L	L	H	X	H	5	DISABLED	1.5
L	H	L	L	L	6	ODD	1
L	H	L	L	H	6	ODD	2
L	H	L	H	L	6	EVEN	1
L	H	L	H	H	6	EVEN	2
L	H	H	X	L	6	DISABLED	1
L	H	H	X	H	6	DISABLED	2
H	L	L	L	L	7	ODD	1
H	L	L	L	H	7	ODD	2
H	L	L	H	L	7	EVEN	1
H	L	L	H	H	7	EVEN	2
H	L	H	X	L	7	DISABLED	1
H	L	H	X	H	7	DISABLED	2
H	H	L	L	L	8	ODD	1
H	H	L	L	H	8	ODD	2
H	H	L	H	L	8	EVEN	1
H	H	L	H	H	8	EVEN	2
H	H	H	X	L	8	DISABLED	1
H	H	H	X	H	8	DISABLED	2

X = Don't Care

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
- Industrial IM6402AI/03AI ..... -40°C to +85°C
- Military IM6402AM/03AM ..... -55°C to +125°C

Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... 4.0V to 11.0V
Supply Voltage ..... +12.0V
Voltage On Any Input or Output Pin .. -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 4V to 11V, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	V_{IH}	Input Voltage High		70% V_{CC}			V
2	V_{IL}	Input Voltage Low				20% V_{CC}	V
3	I_{IL}	Input Leakage[1]	$GND \leq V_{IN} \leq V_{CC}$	-1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = 0mA	V_{CC}-0.01			V
5	V_{OL}	Output Voltage Low	I_{OL} = 0mA			GND+0.01	V
6	I_{OL}	Output Leakage	$GND \leq V_{OUT} \leq V_{CC}$	-1.0		1.0	μA
7	I_{CC}	Power Supply Current Standby	V_{IN}=GND or V_{CC}		5.0	500	μA
8	I_{CC}	Power Supply Current IM6402A Dynamic	f_C = 4MHz			9.0	mA
9	I_{CC}	Power Supply Current IM6403A Dynamic	$f_{CRYSTAL}$=3.58MHz			13.0	mA
10	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
11	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE 1: Except IM6403 XTAL input pins (i.e. pins 17 and 40).
NOTE 2: V_{CC} = 5V, T_A = 25°C.

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 10V ± 5%, C_L = 50pF, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	f_C	Clock Frequency IM6402A	See Timing Diagrams (Figures 2,3,4)	D.C.	6.0	4.0	MHz
2	$f_{CRYSTAL}$	Crystal Frequency IM6403A			8.0	6.0	MHz
3	t_{PW}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		100	40		ns
4	t_{MR}	Pulse Width MR		400	200		ns
5	t_{DS}	Input Data Setup Time		40	0		ns
6	t_{DH}	Input Data Hold Time		30	30		ns
7	t_{EN}	Output Enable Time			40	70	ns

TIMING DIAGRAMS

FIGURE 2. Data Input Cycle

FIGURE 3. Control Register Load Cycle

FIGURE 4. Status Flag Enable Time or Data Output Enable Time

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ABSOLUTE MAXIMUM RATINGS

Operating Temperature
- Industrial IM6402-1I/03-1I ..... -40°C to +85°C
- Military IM6402-1M/03-1M ..... -55°C to +125°C

Storage Temperature ..... -65°C to +150°C
Operating Voltage ..... 4.0V to 7.0V
Supply Voltage ..... +8.0V
Voltage On Any Input or Output Pin .. -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0 ± 10%, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage[1]	GND≤V_{IN}≤V_{CC}	-1.0		1.0	μA
4	V_{OH}	Output Voltage High	I_{OH}=-0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL} = 2.0mA			0.45	V
6	I_{OL}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-1.0		1.0	μA
7	I_{CC}	Power Supply Current Standby	V_{IN}=GND or V_{CC}		1.0	100	μA
8	I_{CC}	Power Supply Current IM6402 Dynamic	f_C = 2MHz			1.9	mA
9	I_{CC}	Power Supply Current IM6403 Dynamic	$f_{CRYSTAL}$=3.58MHz			5.5	mA
10	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
11	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE 1: Except IM6403 XTAL input pins (i.e. pins 17 and 40).
NOTE 2: V_{CC} = 5V, T_A = 25°C.

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, C_L = 50pF, T_A = Industrial or Military

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP[2]	MAX	UNITS
1	f_C	Clock Frequency IM6402	See Timing Diagrams (Figures 2,3,4)	D.C.	3.0	2.0	MHz
2	$f_{CRYSTAL}$	Crystal Frequency IM6403			4.0	3.58	MHz
3	t_{PW}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		150	50		ns
4	t_{MR}	Pulse Width MR		400	200		ns
5	t_{DS}	Input Data Setup Time		50	20		ns
6	t_{DH}	Input Data Hold Time		60	40		ns
7	t_{EN}	Output Enable Time			80	160	ns

FIGURE 5. Functional Difference Between IM6402 and IM6403 UART (6403 has On-Chip 4/11 Stage Divider)

The IM6403 differs from the IM6402 on three Inputs (RRC, TRC, pin 2) as shown in Figure 5. Two outputs (TBRE, DR) are not three-state as on the IM6402, but are always active. The on-chip divider and oscillator allow an inexpensive crystal to be used as a timing source rather than additional circuitry such as baud rate generators. For example, a color TV crystal at 3.579545MHz results in a baud rate of 109.2Hz for an easy teletype interface (Figure 11). A 9600 baud interface may be implemented using a 2.4576MHz crystal with the divider set to divide by 16.

INTERSIL

ABSOLUTE MAXIMUM RATINGS

Operating Temperature
IM6402/03 ..... -40°C to +85°C
Storage Temperature ..... -65°C to 150°C
Operating Voltage ..... 4.0V to 7.0V
Supply Voltage ..... +8.0V
Voltage On Any Input or Output Pin .. -0.3V to V_{CC} +0.3V

NOTE: Stresses above those listed under "Absolute Maximum Ratings" may cause permanent device failure. These are stress ratings only and functional operation of the devices at these or any other conditions above those indicated in the operation sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may cause device failures.

D.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0 ± 10%, T_A = -40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	V_{IH}	Input Voltage High		V_{CC}-2.0			V
2	V_{IL}	Input Voltage Low				0.8	V
3	I_{IL}	Input Leakage[1]	GND≤V_{IN}≤V_{CC}	-5.0		5.0	μA
4	V_{OH}	Output Voltage High	I_{OH} = -0.2mA	2.4			V
5	V_{OL}	Output Voltage Low	I_{OL}=1.6mA			0.45	V
6	I_{OL}	Output Leakage	GND≤V_{OUT}≤V_{CC}	-5.0		5.0	μA
7	I_{CC}	Power Supply Current Standby	V_{IN}=GND or V_{CC}		1.0	800	μA
8	I_{CC}	Power Supply Current IM6402 Dynamic	f_C = 500 KHz			1.2	mA
9	I_{CC}	Power Supply Current IM6403 Dynamic	$f_{CRYSTAL}$=2.46MHz			3.7	mA
10	C_{IN}	Input Capacitance[1]			7.0	8.0	pF
11	C_O	Output Capacitance[1]			8.0	10.0	pF

NOTE 1: Except IM6403 XTAL input pins (i.e. pins 17 and 40).
NOTE 2: V_{CC} = 5V, T_A = 25°C.

A.C. CHARACTERISTICS

TEST CONDITIONS: V_{CC} = 5.0V ± 10%, C_L = 50pF, T_A = -40°C to +85°C

	SYMBOL	PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
1	f_C	Clock Frequency IM6402	See Timing Diagrams (Figures 2,3,4)	D.C.	3.0	1.0	MHz
2	$f_{CRYSTAL}$	Crystal Frequency IM6403			4.0	2.46	MHz
3	t_{PW}	Pulse Widths CRL, $\overline{DRR}$, $\overline{TBRL}$		225	50		ns
4	t_{MR}	Pulse Width MR		600	200		ns
5	t_{DS}	Input Data Setup Time		75	20		ns
6	t_{DH}	Input Data Hold Time		90	40		ns
7	t_{EN}	Output Enable Time			80	190	ns

* These outputs are three state (IM6402) or always active (IM6403)

FIGURE 6. IM6402/03 Functional Block Diagram

TRANSMITTER OPERATION

The transmitter section accepts parallel data, formats it and transmits it in serial form (Figure 7) on the TROutput terminal.

FIGURE 7. Serial Data Format

Transmitter timing is shown in Figure 8. Ⓐ Data is loaded into the transmitter buffer register from the inputs TBR1 through TBR8 by a logic low on the $\overline{\text{TBRL}}$oad input. Valid data must be present at least t_{DS} prior to and t_{DH} following the rising edge of $\overline{\text{TBRL}}$. If words less than 8 bits are used, only the least significant bits are used. The character is right justified into the least significant bit, TBR1. Ⓑ The rising edge of $\overline{\text{TBRL}}$ clears TBREmpty. 0 to 1 clock cycles later data is transferred to the transmitter register and TREmpty is cleared and transmission starts. TBREmpty is reset to a logic high. Output data is clocked by TRClock. The clock rate is 16 times the data rate. Ⓒ A second pulse on TBRLoad loads data into the transmitter buffer register. Data transfer to the transmitter register is delayed until transmission of the current character is complete. Ⓓ Data is automatically transferred to the transmitter register and transmission of that character begins.

FIGURE 8. Transmitter Timing (Not to Scale)

RECEIVER OPERATION

Data is received in serial form at the RI input. When no data is being received, RI input must remain high. The data is clocked through the RRClock. The clock rate is 16 times the data rate. Receiver timing is shown in Figure 9.

Ⓐ A low level on $\overline{\text{DRR}}$eset clears the DReady line. Ⓑ During the first stop bit data is transferred from the receiver register to the RBRegister. If the word is less than 8 bits, the unused most significant bits will be a logic low. The output character is right justified to the least significant bit RBR1. A logic high on OError indicates overruns. An overrun occurs when DReady has not been cleared before the present character was transfered to the RBRegister. A logic high on PError indicates a parity error. Ⓒ 1/2 clock cycle later DReady is set to a logic high and FError is evaluated. A logic high on FError indicates an invalid stop bit was received. The receiver will not begin searching for the next start bit until a stop bit is received.

FIGURE 9. Receiver Timing (Not to Scale)

START BIT DETECTION

The receiver uses a 16X clock for timing (see Figure 10.) The start bit Ⓐ could have occurred as much as one clock cycle before it was detected, as indicated by the shaded portion. The center of the start bit is defined as clock count 7½. If the receiver clock is a symmetrical square wave, the center of the start bit will be located within ±1/2 clock cycle, ±1/32 bit or ±3.125%. The receiver begins searching for the next start bit at the center of the first stop bit.

FIGURE 10. Start Bit Timing

TYPICAL APPLICATION

Microprocessor systems, which are inherently parallel in nature, often require an asynchronous serial interface. This function can be performed easily with the IM6402/03 UART. Figure 11 shows how the IM6403 can be interfaced to an IM6100 microcomputer system with the aid of an IM6101 Programmable Interface Element (PIE). The PIE interprets Input/Output transfer (IOT) instructions from the processor and generates read and write pulses to the UART. The SENSE lines on the PIE are also employed to allow the processor to detect UART status. In particular, the processor must know when the Receive Buffer Register has accumulated a character (DR active), and when the Transmit Buffer Register can accept another character to be transmitted.

In this example the characters to be received or transmitted will be eight bits long (CLS 1 and 2: both HIGH) and transmitted with no parity (PI:HIGH) and two stop bits (SBS:HIGH). Since these control bits will not be changed during operation, Control Register Load (CRL) can be tied high. Remember, since the IM6402/03 is a CMOS device, all unused inputs should be committed.

The baud rate at which the transmitter and receiver will operate is determined by the external crystal and DIVIDE CONTROL pin on the IM6403. The internal divider can be set to reduce the crystal frequency by either 16 (PIN 2:HIGH) or 2048 (PIN 2:LOW) times. The frequency out of the internal divider

should be 16 times the desired baud rate. To generate 110 baud, this example will use a 3.579545MHz color TV crystal and DIVIDE CONTROL set low. The IM6402 may use different receive (RRC) and transmit (TRC) clock rates, but requires an external clock generator.

To assure consistent and correct operation, the IM6402/03 must be reset after power-up. The Master Reset (MR) pin is active high, and could be driven reliably from a Schmitt trigger inverter and R-C delay. In this example, the IM6100 is reset through still another inverter. The Schmitt trigger between the processor and R-C network is needed to assure that a slow rising capacitor voltage does not re-trigger RESET. A long reset pulse after power-up (~100ms) is required by the processor to assure that the on-board crystal oscillator has sufficient time to start.

The IM6402 supports the processor's bi-directional data bus quite easily by tying the TBR and RBR buses together. A read command from the processor will enable the RECEIVER BUFFER REGISTER onto the bus by using the RECEIVER REGISTER DISABLE (RRD) pin. A write command from the processor clocks data from the bus into the TRANSMITTER BUFFER REGISTER using $\overline{TBRL}$. Figure 11 shows a NAND gate driving $\overline{TBRL}$ from the $\overline{WRITE_2}$ pin on the PIE. This gate is used to generate a rising edge to $\overline{TBRL}$ at the point where data is stable on the bus, and to hold $\overline{TBRL}$ high until the UART actually transfers the data to it's internal buffer. If $\overline{TBRL}$ were allowed to return low before TBRE went high, the intended output data would be overwritten, since the TBR is a transparent latch.

Although not shown in this example, the error flags (PE, FE, OE) could be read by the processor using the other READ line from the PIE. Since an IM6403 is used, TBRE and DR are not affected by the STATUS FLAGS DISABLE pin. Thus, the three error flags can be tied to the data bus and gated by connecting SFD to $\overline{READ_2}$.

If parity is not inhibited, a parity error will cause the PE pin to go high until the next valid character is received.

A framing error is generated when an expected stop bit is not received. FE will stay high after the error until the next complete character's stop bit is received.

The overrun error flag is set if a received character is transferred to the RECEIVER BUFFER REGISTER when the previous character has not been read. The OE pin will stay high until the next received stop bit after a $\overline{DRR}$ is performed.

FIGURE 11. 110 Baud Serial Interface for IM6100 System

INTERSIL

IM87C41 CMOS Single-Chip Programmable Peripheral Interface Microcomputer

PRELIMINARY
Notice: This is a general specification. Some parametric limits are subject to change.

FEATURES

- 8-bit CPU plus EPROM, RAM, I/O, Timer/Counter, and Clock in a single package
- CMOS pin-for-pin replacement for standard NMOS 8741
- Low power dissipation — maximum 50mW @ 5V, 6MHz
- Extended temperature range: -40°C to +85°C
- Completely static — no minimum operating frequency
- Compatible with Intersil's CMOS IM80C48 family
- 1K x 8 EPROM, 64 x 8 RAM, 18 programmable I/O lines
- Asynchronous double-buffered data register for master processor interface
- On-chip Timer/Counter ideal for real-time applications
- Expandable I/O
- Alternative to custom LSI
- Compatible ROM versions (IM80C41/C42)
- High noise immunity — typically 33%
- Single +5V supply

PIN CONFIGURATION

ORDERING INFORMATION

PART NO.	PACKAGE
IM87C41IDL	40 PIN CERAMIC
IM87C41IJL	40 PIN CERDIP

GENERAL DESCRIPTION

The Intersil IM87C41 is a general-purpose programmable peripheral interface device, optimized for use as a slave to many common 8-bit processors. Intersil's high-performance silicon-gate CMOS/LSI process is used to fabricate a device which is pinout, function, software, and throughput compatible with the NMOS 8741, while offering significantly decreased power consumption. In addition, the IM87C41's extended operating temperature range (-40°C to +85°C) and high noise immunity make it ideal for battery operated equipment and hostile environments. The IM87C41 contains an 8-bit CPU, program and data memory, two I/O ports, clock, and timer/counter. An interface-status register and double-buffered data register facilitate communication with a master processor, such as the IM87C48 or 8085.

The IM87C41 CPU has a repertoire of over 90 instructions, most of which execute in one cycle. Included are versatile bit set/reset and test operations, as well as instructions dealing directly with the on-chip timer/counter. 1024 bytes of UV-erasable EPROM program memory and 64 bytes of data memory are provided on chip. The EPROM program memory is ideal for prototypes and low-volume applications. It also conveniently allows for program modifications before the user commits to masked-ROM (IM80C41 or IM80C42). Included in the data memory area are an eight-level subroutine stack, and sixteen general purpose registers. Register direct, indirect, and unique accumulator-indirect addressing modes are implemented for ease of data manipulation.

The IM87C41 has two general-purpose TTL-compatible 8-bit I/O ports; individual port lines may be programmed to function as either inputs or outputs. Two additional inputs are testable using conditional-jump instructions. The compatible CMOS IM82C43 I/O expander is supported by the IM87C41 instruction set and extends I/O capability in increments of 16 I/O lines.

For debugging purposes, a single-step input allows instructions to be executed one at a time. Since the IM87C41 is completely static (in contrast to the dynamic NMOS 8741), the device may also be single-clocked.

Intersil's Intercept microcomputer development systems provide full IM87C41 support. The efficient IFDOS operating system supports a text editor, assembler, EPROM programmer, and a hardware in-circuit emulator.

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INTERSIL

IM82C43 CMOS Input/Output Expander

PRELIMINARY
Notice: This is not a final specification. Some parametric limits are subject

FEATURES

- IM87C48/C41 — compatible I/O expander
- CMOS pin-for-pin replacement for standard NMOS 8243
- Low power dissipation — typically 25mW active
- Extended temperature range: -40°C to +85°C
- Four 4-bit I/O ports in 24-pin DIP
- Logical AND/OR directly to ports
- High output drive
- High noise immunity — typically 33%
- Single +5V supply

DESCRIPTION

The Intersil IM82C43 is a CMOS input/output expander compatible with the NMOS 8243. It is designed to provide low-cost I/O expansion for the CMOS IM87C48 and IM87C41 single-chip microcomputers.

The 24-pin IM82C43 provides four 4-bit I/O ports; IM87C48/C41 instructions implement accumulator/IM82C43 port transfers, as well as logical AND/OR operations. P20-P23 on the IM87C48/C41 serves as a 4-bit bus for transfer of control and data to the IM82C43.

PIN CONFIGURATION

LOGICAL BLOCK DIAGRAM

ORDERING INFORMATION

PART NO.	PACKAGE
IM82C43IDG	24 PIN CERAMIC
IM82C43IJG	24 PIN CERDIP
IM82C43IPG	24 PIN PLASTIC

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INTERSIL

6950 INTERCEPT JR. MICROCOMPUTER TUTORIAL SYSTEM

FEATURES

- **Battery operation**
- **Executes PDP®-8/E instruction set**
- **Keyboard monitor program in ROM**
- **8 seven-segment displays for address and data**
- **256 words of non-volatile RAM**
- **3 expansion sockets for optional modules**
- **Fully assembled and tested**
- **Low cost**
- **Tutorial manual included**

®Registered trademark of Digital Equipment Corp.

GENERAL DESCRIPTION

A practical exposure to the Intersil IM6100 microprocessor, RAMs, P/ROMs, and Input/Output interfacing can be achieved with the INTERCEPT JR. TUTORIAL SYSTEM and the owners handbook supplied.

This fully assembled and factory tested system is battery operated. Moreover, it executes the same instruction set as the popular PDP®-8E minicomputer, thus providing a rich supply of proven software. The INTERCEPT JR. is designed with a modular concept to enable the user to purchase only those modules which meet his requirements. Or, if the user wishes, custom interface boards can be designed using the documentation supplied. The INTERCEPT JR. system is a valuable tool for the evaluation of custom circuits interfaced to an IM6100 microcomputer system.

With its simplicity of design, broad capabilities, and low cost, the INTERCEPT JR. TUTORIAL SYSTEM is ideal as an educational tool for the student, hobbiest, or system designer.

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6950-INTERCEPT JR. MODULE

INTERCEPT JR. provides an all CMOS computer on a 10" × 11" double sided PC board. A multiple function calculator type keypad in concert with a 1024 × 12 CMOS ROM (IM6312) monitor provides control functions, a serial bootstrap loader, as well as the INTERCEPT JR. MICROINTERPRETER. Memory addresses and data are displayed in octal on two four-digit LED displays. The IM6100 CMOS microprocessor interfaces via a three-state address/data bus to 256 × 12 CMOS RAM. Four D-cell batteries allow for non-volatile RAM and battery operation of the entire system. External terminals permit the user to provide a 5 volt power source. A socket is provided for evaluation of a user generated CMOS ROM (IM6312/12A). Three edge connectors with 44 pins on 0.156" pin-to-pin spacing are provided for expansion using the optional boards available.

6951-M1KX12
JR. RAM MODULE

The JR. RAM MODULE, utilizing twelve (12) IM6518 1024 x 1 CMOS RAMS on a 4½" x 6½" PC board, provides a convenient memory extension module. Non-volatility is assured by two (2) penlight batteries which are provided.

6952-P2KX12
JR. PROGRAMMABLE ROM-P/ROM MODULE

The JR. P/ROM MODULE provides the user with twelve (12) sockets organized on a 4½" x 6½" PC board. The user has the option of utilizing the IM5623, 256 x 4, or IM5624, 512 x 4 three-state-output Avalanche Induced Migration (AIM) programmable bipolar P/ROMs to obtain from 256 to 2048 words of program. Each of the four (4) rows of sockets are power strobed to permit 0.75 watts average when the P/ROMs are accessed.

6953-PIEART
JR. SERIAL I/O MODULE

The JR. SERIAL I/O MODULE featuring the IM6101 CMOS Parallel Interface Element (PIE) and the IM6403 CMOS Universal Asynchronous Receiver Transmitter (UART) provides the user with serial I/O capability with both RS232 and 20 mA current loop interfaces. The IM6100 controls the UART via the PIE. The CMOS ROM monitor contains a bootstrap routine for loading programs from the 6953-PIEART using BIN** formatted media.

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**Digital Equipment Corporation Binary Format

6954-ACI
JR. AUDIO CASSETTE INTERFACE MODULE

The INTERCEPT JR. AUDIO CASSETTE INTERFACE MODULE allows the user to store and retrieve programs on an inexpensive cassette tape recorder. The module transfers data at 30 characters per second. Thus, approximately 200,000 characters may be recorded on a standard two hour cassette. The module employs the IM6101 PIE and IM6402 UART to accomplish serial/parallel conversion, as well as two phaselock loops and a digital sinewave generator for the analog interface.

6957-AUDVIS
JR. AUDIO VISUAL MODULE

The JR. AUDIO VISUAL MODULE provides the user with an excellent tutorial device. A switch register, acting as an input, can be loaded into two LED display registers providing both binary and seven segment octal readout. A volume controlled speaker can be "clicked" or used to produce tones by controlling the rate at which the speaker is pulsed. A display control on-off switch is provided for power conservation.

MICROINTERPRETER SIMPLIFIES PROGRAM ENTRY

The INTERCEPT JR. MICROINTERPRETER provides an assembler-like method of entering programs. The user needn't remember opcodes! The MICROINTERPRETER converts assembler mnemonics into machine language opcodes.

EXAMPLE:

Add 7_{10} (0007_8) which is stored in memory location 22_{10} (0026_8), to 15_{10} (0017_8), which is stored in memory location 23_{10} (0027_8), and store the result in 21_{10} (0025_8).

PROGRAM

```
0020   CLA       /Clear Accumulator
0021   TAD 0026  /Read Location 0026
0022   TAD 0027  /Add Location 0027
0023   DCA 0025  /Deposit Result in 0025
0024   HLT       /Halt
```

SYSTEM BLOCK DIAGRAM

INTERSIL

6910/6911 Intercept I/II Microcomputer Development System

HARDWARE FEATURES:

- 4K Words of Resident Memory (RAM) for Program and Data Storage
- Expandable to 32K Words of Memory: Intercept II
- Resident Control Panel Memory (2K Words ROM and 256 Words RAM)
  - Transparent to User Programs
  - Floppy Disk Operating System Bootstrap
  - Up to 8 Simultaneous Breakpoints
  - Highly Interactive Debugging Facilities
- Two High Speed Serial I/O Ports with Multiple Baud Rates (14 Different Baud Rates)
  - User Selectable
  - RS232C Standard on Both I/O Ports
  - Either Port May be Strapped for 20mA Current Loop
- Compact Size
  - Intercept I (8.3cm x 40.8cm x 27.9cm)
  - Intercept II (21.6cm x 50.8cm x 47.6cm)
- Extensive Hardware Options
  - Memory Module
  - Wirewrap Module
  - Extender Module
  - Teletype Relay Module
  - Dual Floppy Disk System
- Intercept II: 6910
- Intercept I: 6911

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Intercept I/II

INTERSIL

GENERAL DESCRIPTION

Intercept I/II is a general purpose microcomputer development system for Intersil's IM6100 Microprocessor component. It consists of two PC boards, a Central Processor Module Board, and a Memory Module Board. The Central Processor Module Board includes the IM6100 CPU, resident memory (2K words ROM and 256 words RAM) for firmware storage, memory extension capability and two channels of serial I/O ports. The Memory Module Board includes 4K words (4K x 12) of CMOS RAM for the user's PROGRAM/DATA storage.

All of the system control features, such as an extended memory control (for memory expansion up to 32K words); a real time clock, and DMA control functions are resident in the system. The resident firmware eliminates the need for the hardware control panel.

The Intercept I has an ultra compact enclosure size of 8.3cm x 40.8cm x 27.9cm (HxWxD) and it can accommodate a total of four PC Boards. Two boards, a processor card and a memory card, are supplied with the Intercept I system, and thus, the user can add up to two additional cards.

The Intercept II has a compact enclosure size of 21.6cm x 50.8cm x 47.6cm (HxWxD), and it allows a total of eleven PC boards in the system. Because two cards come with the system, the user may add up to nine additional cards to Intercept II.

Standardized board sizes and uniform bus definitions ensure compatibility with previous Intercept designs. Intersil offers hardware and software support including 4K memory modules, floppy disk hardware, Intercept Floppy Disk Operating System, etc.

HARDWARE SPECIFICATIONS

Word Size

Host Processor: Intersil IM6100
Data: 12-bits
Instruction: 12 or 24-bits

Memory Size

Main Memory

RAM: 4K expandable to 32K (CMOS with battery backup standard)

Control Panel Memory (2K words x 12)

RAM: 256 words (not expandable — monitor uses 128 words)
ROM: 2K (not expandable — used by monitor)

System Clock

Crystal Controlled: 3.3MHz typical

Serial I/O Interfaces

(RS232C is standard on both I/O ports; either port may be strapped for 20mA current loop operation)

Primary Port

Baud Rates: 50/75/110/134.5/150/200/300/600/1200/1800/2400/4800/9600/19200

Any of these 14 different baud rates is switch selectable.

Code Format: 10 level code

Parity: None

Secondary Port

Same as Primary Port except: Baud Rate is console controlled or software programmable (50/75/110/134.5/150/200/300/600/1200/1800/2400/4800/9600/38400.)

Includes four RS232C supervisory signals (two inputs and two outputs)

Interrupt

Single level, maskable, prioritized, vectored or polled.

Direct Memory Access

Standard IM6102 DMA, bus control implemented on CPU module — transfer rate user controlled (direct memory interface) — typically greater than 2MHz.

Physical Characteristics

Dimensions: (HxWxD) 8.3cm x 40.8cm x 27.9cm*
21.6cm x 50.8cm x 47.6cm**

Weight: 18 lbs.*
35 lbs.**

Electrical Characteristics

DC Power Supply	Power Supply Current	Basic System Current Requirements (Typ.)
**+5V ± 5%	6 A	.8 A
*+5V ± 5%	1.5 A	.9 A
**+12V ± 5%	.8 A	.1 A
**-12V ± 5%	.8 A	.1 A

*Applies to Intercept I Only. **Applies to Intercept II Only.

AC Power Requirements

Frequency: 50 or 60 Hz
Voltage: 115 or 230V AC
Power: Intercept I: 70W max.
Intercept II: 175W max.

Environmental Characteristics

Operating Temperature: 0°C to 50°C

Humidity: 10% to 90% (no condensation)

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Equipment Supplied (Basic System)

- 6912 Central Processor Module
- 6901 4K CMOS RAM Module
- Finished Cabinet with Power Supplies, Card Cage and Fan**
- Intercept User's Manual
- IM6100 CMOS Microcomputer User's Manual
- Two RS232C and One 20mA Current Loop Cable
- AC Power Line Cord

**Intercept II Only.

Hardware Options

6901 — M4K x 12
4K Nonvolatile CMOS Memory Module
- 4K Words (4Kx12) CMOS Static RAM
- 100 mAH Rechargeable Ni-Cd Battery Back-Up Included
- Data Retention of Up to 40 Days
- Ni-Cd Batteries Automatically Recharged in a System Under Normal Power
- Input Protect Switch (For Write Inhibit into RAM's)
- 15.2cm x 21.6cm x 1.9cm

6905 — WIREWP
Wirewrap Module for User Interfaces to Intercept
- Direct Interface to Intercept System
- Universal Wirewrap Board

6906 — EXTEND
Extender Module
- Extend any Intercept Module for Servicing, Testing, Trouble-Shooting, and Debugging

6909 — RELAY
Teletype Paper Tape Reader Remote Control Module
- Remote Control of Teletype Model ASR33 Paper Tape Reader
- 6.4cm x 9.5cm
- Protection Against Noise Induced by Line Surges when Interfacing to Teletype ASR33

6970 — IFDOS
Dual Floppy Disk System with Single Board Interface to Intercept Bus
- IBM 3740 Compatible Media with Multiple Sources
- Disc Drive/Controller/Formatter/Intercept Interface Included
- Powerful Operating System
- Editor, Assembler
- Binary Loader, Octal Debugger
- Numerous Utility Programs for File Copying, Dumping, System Data Handling, and System Program Cataloging

SOFTWARE/FIRMWARE SPECIFICATIONS

Resident Control Panel Firmware Monitor

Capabilities
- Accumulator, Link, Program Counter, Instruction/Data Fields, MQ, Switch Register-examine/modify
- Control Panel and Main Memory-examine/modify
- Single Instruction, Breakpoint, Snapshot and Trace-debugging and modify
- IFDOS (FLOPPY DISK) Operating System Bootstrap
- Memory Bit Pattern/Word Search
- Binary Paper Tape Input/Output Commands (Loader/Punch)
- DEC PDP-8/E Console Terminal, HLT, OSR Emulation
- Up to 8 Simultaneous Breakpoints

Features
- High Speed Resident Operation
- Highly Interactive Debugging Facilities
- Completely Transparent to User Programs

SOFTWARE OPTIONS

6980 — Intercept Floppy Disk Operating System (IFDOS)

Components
- File System Controls Floppy Disk Input/Output Operation
- Keyboard Monitor for Communication Between User and IFDOS
- Text Editor Creates and Modifies ASCII Text at the Terminal
- PAL Assembler translates IM6100 assembly language to machine language in one or two passes. About 400 symbols can be created in standard system of 4K word memory. 1024 more symbols can be created with each 4K additional RAM with maximum symbol limit of up to 4095 symbols.
- Numerous Switch Options and Pseudo-operations for Assembly and Listing Control
- Numerous Utility Programs for File Manipulation and Disk Dumping and Copying
- Disk Diagnostic Programs
- Supplied with IFDOS in a Standard Floppy Diskette and Listing
- Required Hardware:
  — Intercept System
  — ASCII Terminal
  — 6970-IFDOS Dual Floppy Disk Unit

6981 — FOPAL III
PAL III Fortran Cross Assembler
- Written in Standard Fortran IV
- Card Deck Based
- Can Use with Any Fortran Compiler and a Card Reader (such as 029 Reader)

6982 — PDP®-8/E Extended Paper Tape Software Kit
(Order No. 6982-QF081-AC) — See Note 1

Components
- Text Editor Creates and Modifies ASCII Text at the Terminal
- PAL III Assembler Translates the IM6100 Assembly Language to Machine Language in Two or Three Passes
- 23-Bit Floating Point Arithmetic Package Performs Basic Arithmetic, Trigonometric, and Exponential Function Using Floating Point Numbers
- Supplied with programs in Paper Tapes and Documentation

6982 — FOCAL®8
(Order No. 6982-IS-LFOCA) — See Note 1
- Interactive Algebraic Language
- Extensive Math. Functions
- Easy to Learn High Level Language
- Needs only 4K Words of RAM
- Paper Tape Based

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Note:
1. This is redistributed Digital Equipment Corporation Software. It is copyrighted and non-licensed Digital Equipment Corporation software, which means that it cannot be copied although it may be distributed to third parties. Digital Equipment Corporation assumes no responsibility for any software distributed by Intersil, Inc. nor for the performance of any of Intersil's products.

INTERSIL

6970-IFDOS Intercept Floppy Disc Operating System

DESCRIPTION

The 6970-IFDOS Floppy Disc Operating System is designed to facilitate development of software for an IM6100 microprocessor-based system. An ASCII terminal such as the ASR33 is required, as well as at least 4K words of memory (included with the INTERCEPT prototyping system).

HARDWARE

The hardware components of 6970-IFDOS consist of two completely interfaced floppy disc drive mechanisms with all electronics, power supplies, and cables necessary to add over four (4) million bits of "on line" mass storage capability to the INTERCEPT prototyping system. All components are contained in a single covered enclosure which is rack mountable or can be placed on any flat surface. The interface module is inserted directly into the INTERCEPT bus and is connected to the disc system via a multi-conductor ribbon cable.

Features:

- IBM 3740 compatible media with multiple sources
- Software compatible with DEC RX8 for the PDP-8 minicomputers
- Intelligent disc drive/controller formatter/interface communications which provide the ability to:
  - Detect, identify, and correct errors resulting from mechanical, electrical, media or human malfunction
  - Completely format a diskette within industry standards
- Automatic transparent self tests on disc related equipment are performed at times when system throughput is least affected
- Flexible Programmed Input/Output for applications that require direct communications between user programs and the storage system

SOFTWARE

Features:

- A file system which maintains a catalog of user files on floppy disc and performs file handling and input/output operations as specified by user

Features (con't):

- A keyboard monitor which provides communication between the user and the operating system thereby enabling simple commands to enter and delete files in the user catalog, transfer files between memory and mass storage, print the user file catalog, and call system programs
- An easy to learn text editor which allows the user to create and modify ASCII text at the console terminal
- An extremely fast and flexible assembler which accepts source programs created by the editor and produces binary output for subsequent loading and execution
- A binary loader which loads and executes assembler output files and facilitates loading of existing binary paper tapes
- An octal debugger which allows the user to examine, modify, and control execution of programs from the terminal
- Numerous utility programs for absolute block copying and dumping of floppy discs, system data handling, control of system parameters, and printing of system program catalogs

DIAGNOSTIC SOFTWARE

- Binary programs to test the floppy disc system and interface
- A listing of the programs

PHYSICAL SPECIFICATIONS

- DIMENSIONS Height 10.5 inches
  Width 19 inches
  Depth 22.5 inches
- WEIGHT 54 lbs
- POWER REQUIREMENTS
  110 volts @ 60 Hz (2.0 Amps) or
  200 volts @ 50 Hz (1.5 Amps)

The listing for 6980-ISOFT can be ordered separately by specifying 6980-ILIST.

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INTERSIL

ADVANCE INFORMATION
Characteristics are subject to change without notice.

6920 CMOS EPROM Programmer

FEATURES

- **Programs Intersil's IM6653/54 and IM87C48/C41 families of CMOS EPROM products**
- **Software controlled for ease of expandability**
- **IM6100 microprocessor based**
  - **— 16K bit buffer memory**
- **Serial data communication**
  - **— 20 mA current loop**
  - **— RS232C**
  - **— 110 to 9600 selectable baud rate**
- **Three operating modes**
  - **— Master with CRT terminal or Teletype®**
  - **— Slave with development system**
  - **— Stand-alone for duplicating EPROMS**
- **Self contained D/A controlled power supplies**
- **Check sum error detection**

®Teletype is a registered trademark of Teletype Corp.

DESCRIPTION

Intersil's 6920 CMOS EPROM programmer is a multi-mode, cost effective solution to programming Intersil's IM6653/54 family of CMOS EPROMs and the IM87C48/C41 family of CMOS EPROM based, single chip, 8-bit microcomputers.

The 6920 is microprocessor controlled, allowing the programmer to operate as a stand-alone unit, for duplicating EPROMS; a master, for operation with CRT terminals or Teletype®; or a slave, for operation with a software development system or minicomputer.

Serial data communication is used for all command and data transfers with a 20 mA current loop and an RS232C interface provided. Check sum error detection is employed for data validation.

REAR PANEL VIEW

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Appendix

Application Note Summary B-2

High Reliability Processing B-4

Chip Ordering Information B-10

Intersil Part Numbering System B-16

Sales Offices, Distributors, and Representatives B-18

B

APPLICATION NOTE SUMMARY

The following brief descriptions of current Intersil application notes will provide a quick review of available applications literature.

A003 UNDERSTANDING AND APPLYING THE ANALOG SWITCH

Introduces analog switches and compares them to relays. Describes CMOS, hybrid (FET + driver), J-FET "virtual ground" and J-FET "positive signal" types. Applications information included.

A004 IH5009 LOW COST ANALOG SWITCH SERIES

Compares the members of the IH5009 "virtual ground" analog switches and provides suggested applications.

A005 THE 8007 – A HIGH PERFORMANCE FET INPUT OP AMP

Compares the 8007 with the 741, which is (pin compatible), and suggests applications such as log-antilog amplifier, sample and hold circuit, photometer, peak detector, etc.

A006 A NEW CMOS ANALOG GATE TECHNOLOGY

Introduces Intersils' "Floating Body" process for manufacturing CMOS analog gate and multiplexer devices. This process virtually eliminates destructive latch up.

A007 USING THE 8048/8049 MONOLITHIC LOG-ANTILOG AMPLIFIER

Describes in detail the operation of the 8048 logarithmic amplifier, and its counterpart, the 8049 antilog amp.

A008 A LOW COST DUAL FET-INPUT OP AMP: THE ICL8043

Covers sample and hold, instrumentation amplifier, staircase generator, and automatic offset suppression circuits.

A010 DIGITAL TO ANALOG CONVERTER CIRCUITS USING THE 8018A

Describes, in detail, the operation of the 8018 D/A converter switch network.

A011 A PRECISION FOUR QUADRANT MULTIPLIER THE 8013

Describes, in detail, the operation of the 8013 analog multiplier. Included are multiplication, division, and square root applications.

A012 A PRECISION WAVEFORM GENERATOR AND VOLTAGE CONTROLLED OSCILLATOR – THE 8038

Describes, in detail, the operation of the 8038 and includes the generation of sine, square, triangular, sawtooth, and pulse waveshapes. Frequency control from 1/100 Hz to 500 kHz is possible. See also A013.

A013 EVERYTHING YOU ALWAYS WANTED TO KNOW ABOUT THE 8038

A companion to A012, this note includes 17 of the most asked questions regarding the use of the 8038.

A016 SELECTING A/D CONVERTERS

Describes the differences between integrating converters and successive approximation converters. Includes a checklist for decision making, and a note on multiplexed data systems.

A017 THE INTEGRATING A/D CONVERTER

Explanation of integrating A/D converters, together with a detailed error analysis.

A018 DO'S AND DONT'S OF APPLYING A/D CONVERTERS

An analysis of proper design techniques using D/A converters.

A019 4½ DIGIT PANEL METER DEMONSTRATION/ INSTRUMENTATION BOARDS

Describes two typical PC board layouts using the 8052A/7103A 4½ digit A/D pair. Includes schematics, parts layout, list of materials, etc. Also see A028.

A021 POWER D/A CONVERTERS USING THE ICH 8510

Detailed analysis of the 8510. Included are a section describing the linearity of the device and application notes for driving servo motors, linear and rotary actuators, etc.

A022 A NEW J-FET STRUCTURE – THE VARAFET

Describes in detail the operation of the varafet, a standard J-FET with the analog gate interfacing components monolithically built in.

A023 LOW COST DIGITAL PANEL METER DESIGNS

Provides a detailed explanation of the 7106 and 7107 3½ digit panel meter IC's, and describes the two evaluation kits available from Intersil.

A026 DC SERVO MOTOR SYSTEMS USING THE ICH8510

This companion note to A021 explains the design techniques utilized in using the ICH8510 family to drive closed loop servo motor systems.

A027 POWER SUPPLY DESIGN USING THE ICL8211 AND ICL8212

Explains the operation of the ICL8211/12 and describes various power supply configurations. Included are positive and negative voltage regulators, constant current source, programmable current source, current limiting, voltage crowbarring, power supply window detector, etc.

A028 BUILDING AN AUTO RANGING DMM WITH THE ICL7103A/8052A CONVERTER PAIR

This companion app note to A019 explains the use of the 8052A/7103A converter pair to build a ±4½ digit auto ranging digital multimeter. Included are schematics, circuit descriptions, tips and hints, etc.

A029 POWER OP AMP HEAT SINK KIT

Describes the heat sinks for the ICH8510 family. These heat sinks may be ordered from the factory.

A030 THE ICL7104: A BINARY OUTPUT A/D CONVERTER FOR MICROPROCESSORS

Describes in detail the operation of the 7104. Includes digital interfacing, handshake mode, buffer gain, auto-zero and external zero. Appendix includes detailed discussion of auto-zero loop residual errors in dual slope A/D conversion.

H001 ULTRA LOW BIAS CURRENT OPERATIONAL AMPLIFIER

Introduces the ICH8500 op amp, and suggests applications, such as: picoammeter, sample and hold circuit, and gated integrator.

HIGH RELIABILITY PROCESSING

100% INTEGRATED CIRCUIT PROCESSING

Intersil is committed to build and process integrated circuits for the Military/High-Rel market segments in conformance with MIL-STD-883 and MIL-M-38510. Any customer drawing which specifies testing as set forth in these documents will be automatically processed to the latest revisions of MIL-STD-883 and MIL-M-38510, unless specific requests are made to the contrary.

The latest significant changes in MIL-STD-883, Rev. B, and MIL-M-38510, Rev. D, concerned the change of Class A to Class S, the addition of 100% PIND for Class S, and revisions of certain Group B and Group D quality conformance requirements.

DISCRETE DEVICE PROCESSING

Intersil also offers several QPL-approved discrete products carrying the JANTX designation, which are screened and qualified to the latest revisions of MIL-STD-750 and MIL-S-19500.

MIL-STD-883B SCREENING AND QUALITY CONFORMANCE PROGRAMS, METHODS 5004 AND 5005

The following flow chart details screening activities as carried out by Intersil for Class S, B and C requirements.

*Method 2017, Hybrid

B

QUALITY CONFORMANCE INSPECTION, CLASSES B AND C

The following diagram presents quality conformance inspection methods for Classes B and C as performed at Intersil.

*Sample must have had temp/time exposure specified for burn-in. LTPD of 15 applies to number of leads inspected except that in no case shall less than 3 devices be used.

**Required only when a package contains a dessicant.

NOTES:

1. Group A and B inspections are required on individual inspection lots as a condition for acceptance for delivery.
2. Samples shall be randomly selected from the assembled inspection lot in accordance with appendix B of MIL-M-38510. Specified screen requirements of method 5004 are not required to have been completed for Intersil's standard generic data program, but will be performed when required by customer drawing. Where use of electrical rejects is permitted, and unless otherwise specified, they need not have been subjected to the temperature/time exposure of burn-in.
3. Group C (chip-related test) shall be performed periodically at 3 month intervals.
4. Group D (package related tests) shall be performed periodically at 6 month intervals.
5. Where end point measurements are required but no parameters have been identified, the critical final electrical parameters specified for 100% screening shall be used as end point measurements.
6. Subgroups within a group may be performed in any order but individual tests within a subgroup shall be performed in the sequence indicated.

B

QUALITY CONFORMANCE

The following steps are carried out when quality conformance testing is performed on a lot from which samples are taken.

QUALITY CONFORMANCE – CLASSES B & C

	STANDARD SAMPLE SIZE	ALLOWABLE REJECTS	TIME ALLOWANCE
Group A (Electrical Acceptance)	45	0	3-5 days
Group B (Package Related)	19 Electrical Rejects	0	1 week
Group C (Die Related)	102 Good Electrical (Note 1)	1 from Subgroup 1 1 from Subgroup 2	8-10 weeks
Group D (Package Related)	50 Good Electrical (Note 2) 75 Electrical Rejects	1 from each of 5 Subgroups	4 weeks

NOTE 1: Non-destructive, shippable samples (102 units).

NOTE 2: Destructive tests:

Moisture resistance. Subgroup 3 sample size	25 units
Variable-frequency vibration. Subgroup 4 sample size	25 units
Total Destroyed	50 units

QUALIFICATION TESTING

When qualification testing is required, it will be equivalent to quality conformance testing, with the exception that Group A must be read and recorded on all applicable subgroups for the number of electrically-good units which will be required for samples for Groups C and D.

QUALIFICATION TESTING – GROUPS B & C

	STANDARD SAMPLE SIZE	ALLOWABLE REJECTS	TIME ALLOWANCE
Group A (Electrical Acceptance)	184 (Read & Record)	5	5 days
Group B (Package Related)	19 Electrical Rejects	0	1 week
Group C (Die Related)	102 Good Electrical (Note 1)	1 from Subgroup 1 1 from Subgroup 2	10-12 weeks
Group D (Package Related)	50 Good Electrical (Note 2) 75 Electrical Rejects	1 from each of 5 Subgroups	4 weeks

NOTE 1: Shippable samples.

NOTE 2: 50 destroyed samples, subgroups 3 and 4.

LIMITED USAGE QUALIFICATION

A customer may elect to take advantage of a "Limited Usage" qualification per MIL-M-38510, in order to reduce the number of samples required. The following conditions must be met for eligibility for the "Limited Usage" qualification:

1. A maximum quantity of 500 microcircuits is included in a single order.
2. A maximum quantity of 2000 microcircuits is included in a given equipment-acquisition contract or program.
3. A maximum quantity of 2000 microcircuits is to be procured during a 12-month period for a given circuit type and vendor.

Microcircuits which qualify for limited usage cannot be assigned a JAN part number. Variable data will be taken only when specified in a customer drawing.

LIMITED USAGE QUALIFICATION – CLASS B (1)

	SAMPLE SIZE	ALLOWABLE REJECTS	TIME ALLOWANCE
Group A (Electrical Acceptance)	45	0	5 days
Group B (Package Related)	19 Electrical Rejects	0	1 week
Group C (Die Related, Non-Destructive)	10 Good Electrical Parts	0	8-10 weeks
Group D (Package Related, Destructive)	25 (15 Good, 10 Electrical Rejects)	0	4 weeks

(1) Mil-M-38510, Paragraph 4.4.4; MIL-STD-883, Method 5005.

B

GLOSSARY OF MILITARY/AEROSPACE HIGH-REL DEFINITIONS/TERMINOLOGY

ACCELERATED BURN-IN – Same as "Burn-In", except that testing is carried out at an increased temperature (nominally 150° C) for reduced dwell time. Accelerated testing is not permissible for Class S devices.

ATTRIBUTES DATA – Go-No-Go data. Strictly pass/fail and number of rejects recorded. A typical requirement for post burn-in electrical tests on Class B devices.

BASELINE – Technique used to define manufacturing and test processes at time of order placement. Baselining usually involves development of a Program Plan and an Acceptance Test Plan which include flow charts, specification identification/revision letters, QA procedures, and actual specimens of certain important specifications. During subsequent manufacture and testing of parts, it is not permissible to make revisions or changes to any of the identified specifications, unless prior notification and possible customer approval occurs. Other terminology associated with baselining include "Critical Process Changes", "Minor Process Changes", and "Major Process Changes".

BURN-IN – A screening operation. Devices are subjected to high temperature (typically 125° C) and normal power/operation for 160 hours (Class B devices) or 240 hours (Class S devices).

CLASS S, B AND C INTEGRATED CIRCUITS – These classes set forth the screening, sampling and document control requirements for IC testing. Terminology is defined in MIL-M-38510 and in Test Methods 5004 and 5005 of MIL-M-38510. Classes, S, B and C are sometimes referred to as "Levels S, B and C." The Classes cover:

CLASS S – For space and satellite programs. Includes Condition A Precap, SEM, 240 hour burn-in, PIND test and elaborate qualification and quality conformance testing. Normally requires extensive data, documentation, and program planning. Formerly referred to as Class A. Class S devices are quite expensive.

CLASS B – For manned flight, and includes most frequently-procured military integrated circuits. Used for all but highest reliability requirements. Class B uses burn-in, pre-cap, visual, etc.

CLASS C – For ground support equipment. Contains only environmental screening requirements with pre-cap visual. No burn-in required.

In all classes, LTPD (Lot Tolerance Percent Defective) is the sampling plan measurement criteria.

CORRECTIVE ACTION – Those actions which a given supplier (or user) agrees to perform so that a detected problem does not reoccur.

DESC – Defense Electronic Supply Center, located in Dayton, Ohio. The command includes two major subgroups, with functions as follows:

DESC-ECS – This group performs specification engineering work. After the original specifications are created at RADC, DESC-ECS implements and monitors the specifications. DESC-ECS is the industry's main interface on existing specifications.

DESC-EQE – The group which supervises supplier certifications and qualifications. The group to which the industry submits applications when desiring to have devices qualified (QPL'd) on an existing JAN slash sheet. DESC-EQE surveys supplier facilities and grants line certification as various requirements are met. Also reviews manufacturer's qualification test data and issues JAN QPL's accordingly.

DESC LINE CERTIFICATION – The document which approves a supplier's facilities as an appropriate site to manufacture JAN parts.

DIE SHEAR TESTS – A sample test. Mounted chips are exercised to destruction. Degree of die adherence to lead frame is observed. Corrective action taken if required.

DPA – Destructive Physical Analysis. Finished products are opened and analyzed, in accordance with customer or MIL Spec criteria.

GENERIC DATA – Data pertaining to a device family; not necessarily the specific part number ordered by the customer, but representative of parts in the family. Group B, C and D generic data is frequently requested in lieu of the performance of special qual tests on a given order. Generic data tends to be inexpensive.

GROUP A – Sample electrical tests which are performed on each lot. Group A is defined in Test Method 5005 for integrated circuits and in MIL-S-19500 for diodes and transistors.

GROUP B – A collection of package-related environmental and "wear-and-tear" tests. Defined in Test Method 5005 for integrated circuits. For Class S screening, additional life tests are required, and are performed on every lot per MIL-M-38510. For diodes and transistors, Group B consists of both environmental and life tests.

GROUP C – For Class B and C integrated circuits, only Group C includes life testing and temperature cycling/constant acceleration die-related sample tests. Defined in Test Method 5005 and performed every three months per MIL-M-38510.

GROUP D – A collection of additional environmental package-related sample tests as defined in Test Method 5005. Performed every six months per MIL-M-38510.

JAN — "Joint Army Navy", a registered trademark of the U.S. Government. The JAN marking denotes a device which is in full compliance to MIL-M-38510 or MIL-S-19500.

JAN TX — A JAN-qualified diode or transistor which has been subjected to additional screening (burn-in) tests.

JAN TXV — A JAN-qualified diode or transistor which, in additional to burn-in testing, has been subjected to additional screening including pre-cap visual inspection, as witnessed by a government source inspector. Equivalent to Class B screening for integrated circuits.

"M38510" CIRCUITS — Until a recent revision to MIL-M-38510, it was a common practice for users and suppliers alike to specify or offer integrated circuits marked "M38510/XXX" without a J or JAN prefix. This part numbering system indicated a device which was "near-JAN", "quasi-JAN" or "non-JAN". The practice tended to cause confusion between these devices and parts in full conformance to JAN levels. MIL-M-38510 now prohibits such marking with the exception of two special instances:

- When JAN QPL supplier for a given product does not exist, the government will permit "M38510/XXX" marking. While a customer may specify such marking, the supplier must furnish the government with evidence that the parts meet all applicable requirements.
- For certain parts destined for use in F-16 aircraft, "M38510/XXX" marking is permissible, but orders for such parts must be accompanied by appropriate DESC certification letter.

M38510/XXX — Detail specifications (or "slash sheets") for integrated circuits. For example, the 101 specification covers Operational Amplifiers, with electrical requirements for the 741, LM101, 108, 747 types, etc.

MIL-M-38510 — The general military specification for integrated circuits.

MIL-S-19500 — The general military specifications for diodes and transistors.

MIL-S-19500/XXX — Detail specifications (or "slash sheets" for diodes and transistors.

MIL-STD-750 — Specifies Test Methods for diodes and transistors, such as burn-in, pre-cap, temperature cycling, etc.

MIL-STD-883 — Specifies Test Methods for integrated circuits, such as pre-cap, burn-in, hermeticity, storage life, etc.

NPFC — Naval Publications and Forms Center, Philadelphia. Printing and distribution source for military specifications.

NON-STANDARD PARTS — In government terminology, refers to non-JAN devices. Non-standard parts are typically covered by user Source Control Drawings (SCD).

NON-STANDARD PARTS APPROVAL — Approval by the government (frequently RADC) of non-JAN parts, typically on source control drawings, for use in a military system or program. This approval is essentially a waiver which permits non-JAN 38510 parts in a system which otherwise mandatorially requires JAN parts only.

OPERATING LIFE TEST — Same conditions as burn-in, but duration is usually 1000 hours. This is a sample test (Qualification and Quality Conformance).

PCA — Parts Configuration Analysis. A new term which has much the same meaning as "Baseline".

PDA — Percent Defective Allowable. Criteria sometimes applied to burn-in screening. A 10% PDA (the most common type) means that if more than 10% of that lot fails as a result of burn-in (as determined by pre- and post-burn-in electrical tests) the entire lot is considered to have failed.

PDS — Parameter Drift Screening. Measures the changes (Δs) in electrical parameters through burn-in. Common for Class S devices.

PIND — Particle Impact Noise Detection. This is an audio screening test to locate and elminate those parts which have loose internal particles. The test can isolate a high percentage of defectives, even in otherwise good lots. Repeatability of the tests is questionable. This test is one of the screening items for Class S integrated circuits.

PREPARING ACTIVITY — The organizational element of the government which writes specifications, frequently RADC.

PRESEAL VISUAL — A screening inspection which involves observation of a die through a microscope.

PROCURING ACTIVITY — Per MIL-M-38510, this is the organizational element in the government which contracts for articles or services. The Procuring Activity can be a subcontractor (OEM), providing that the government delegates this responsibility. In such a case, the subcontractor does not have the power to grant waivers, unless this authority has been approved by the government.

PRODUCT RELIABLIITY — Pertains to the level of quality of a product over a period of time. Reliability is usually measured or expressed in terms of Failure Rate (such as "0.002% per 1000 hours at a 60% confidence level at 25°C") or MTBF (mean time between failure in hours). MTBF is the reciprocal of Failure Rate.

QPL — Qualified Products List. In the case of JAN products, QPLs are identified as QPL-38510 for integrated circuits and QPL-19500 for diodes and transistors. QPL-38510 revisions occur approximately quarterly and QPL-19500 revisions occur approximately annually. In the interim, the government will notify suppliers via letter of any new device qualifications which may have been granted. Two types of QPLs exist:

PART II QPL – This is an interim or temporary QPL which is granted on the basis of having obtained line certification and approval of an Application to Conduct Qualification Testing. A PART II QPL is automatically voided whenever any one supplier is granted a PART I QPL; thus, a sole-source situation is condoned.

PART I QPL – A "permanent" QPL, granted after all qualification testing is completed and test data is approved by the government.

QPLTT – Qualified Product List Throughput Time. That period which required to obtain device qualification. QPLTT is a function of (1) whether a JAN slash sheet exists; (2) whether a competitor already holds a Part I QPL; and (3) whether the applicant's production line is certified by DESC.

Following is a worst-case example, where a JAN slash sheet does not exist and government line certification has not been granted. QPLTT will be approximately 39.5 months, if the JAN slash sheet already exists, QPLTT will be cut to about 10.5 months. If the applicant already has line certification, QPLTT will be about 2 months to obtain Part II status.

Total time required to obtain a Part I QPL adds about 7 months to QPLTT; in a worst-case example, about 46 months will be required.

QUALIFYING ACTIVITY – Per MIL-M-38510, the organizational element in the government which designates certification (i.e., DESC).

QUALIFICATION TESTING – Initial one-time sample tests which are performed to determine whether device types and processes are good. For integrated circuits, this usually means testing to Groups A, B, C and D. For diodes and transistors, this usually means testing to Groups A, B and C.

QUALITY CONFORMANCE TESTING – These are sample tests which must be performed at prescribed intervals per MIL-M-38510 or MIL-S-19500, assuring that processes remain in control and that individual lots are passed.

RADC – Rome Air Development Command, Griffiss AFB, New York. This is the government organization which created semiconductor specifications; MIL-M-38510 and MIL-STD-883 were developed at RADC. This Air Force unit develops specifications for all U.S. military services. RADC is frequently involved in granting waivers for non-standard parts for Air Force systems.

READ AND RECORD DATA – Same as variable data.

REWORK PROVISION – For semiconductor devices, permissible rework of parts is usually limited to re-testing (screening), lead straightening or bending, re-marking, and cleaning.

S & V – Survivability and Vulnerability. Pertains to the ability of a device to resist radiation dosage.

SCREENING – Operations which are performed on devices on a 100% basis (not sampling). Examples include pre-cap visual, burn-in hermeticity, 100% electrical test, etc. For integrated circuits, Test Method 5004 defines screening flow.

SEM INSPECTION – Inspection by Scanning Electron Microscope. Die samples are examined at very high magnification for metallization defects. A common inspection for Class S devices.

SERIALIZATION – The marking of a unique part number on each part, with assigned numbers marked sequentially/consecutively.

SCDs – Source Control Drawings. Typically user-generated drawings which require development of internal IC vendor sheets. Although each drawing may be slightly different, all will be modelled around MIL-M-38510, MIL-S-19500, MIL-STD-883, or MIL-STD-750.

SOURCE INSPECTION – Can be either Customer Source Inspection (CSI) or Government Source Inspection (GSI). Source Inspection is initiated via purchase order, and can occur at one or more of the following points:

- Pre-cap Visual. Expensive and adds to throughput time.
- Final Inspection. Simple and inexpensive; little delivery impact.
- Throughout. Very expensive and time-consuming.

STANDARD PARTS – In government terminology, JAN parts.

TRACEABILITY – A production and manufacturing control system which includes:

- Wafer run identification number.
- Date pre-cap visual inspection was performed, identity of inspector, and specification number and revision.
- Lot number and inspection history.
- QA Group A electrical results.

VARIABLE DATA – Read and recorded electrical measurements (parametric values). Usually required for pre- and post-burn-in electrical tests. Also common for Group C and D testing.

WIRE PULL TESTS – Bond wire pull tests will be specified in two modes:

DESTRUCTIVE WIRE PULL – Generally performed periodically in assembly on a sample basis. Wires are pulled to destruction and the break point force is recorded. Corrective action is taken as required.

B

CHIP ORDERING INFORMATION

FET, MOSFET, AND DUAL TRANSISTOR CHIPS

INTRODUCTION

Intersil recognizes the increasing need for transistors and FETs in die form. To fulfill this need, Intersil offers a full line of JFETs, MOSFETs, and dual transistors in die form.

Die sales do, however, present some unique problems. In many cases the chips cannot be guaranteed to the same electrical specifications as the packaged part. This is due to the fact that leakage, noise, AC parameters and temperature testing cannot be tested to the same degree of accuracy for dice as it can for packaged devices. This is due to equipment limitations and handling problems.

PURCHASE OPTIONS

Intersil offers dice which are delivered in a number of forms:

- Chips which have been electrically probed, inked, visually inspected and diced.
- Wafers which have been electrically probed, inked, visually inspected and scribed only.
- Wafers which have been electrically probed, inked, and visually inspected only.

GENERAL PHYSICAL INFORMATION

- Chips are available with exact length X width dimensions plus tolerance (see individual data sheets). Chip height ranges from .003" to .006".
- To facilitate die attaching, chips are gold backed. Approximate thickness is 1000 angstroms. In general, dice should be attached to gold, platinum, or palladium metallization. Thin-film gold, moly-gold and most of the thick-film metallization materials are compatible.
- Consult individual product information sheets for dimensions. Except for the aluminum bonding pads, the chips are completely covered with vapox (silicon dioxide). This minimizes damage to the chip caused by handling problems.
- All chips have aluminum metallization and aluminum bonding pads. Typical aluminum thickness is 12,000 angstroms.
- Die are 100% tested to electrical specifications, then visually inspected. When wafers are ordered, dice which fail the electrical test are inked out.
- Generally the minimum size of the die-attaching pad metallization should be at least 5 mils larger (on every edge) than the chip dimensions. For example, a 15 mil chip should be attached on at least a 25 mil pad.

CHIP AND WAFER PROCESSING FLOW CHART

B

RECOMMENDED DICE ASSEMBLY PROCEDURE

CLEANING

Dice supplied in die form do not require cleaning prior to assembly. Dice supplied in wafer form should be cleaned after scribing and breaking. Freon TF in a vapor degreaser is the preferred cleaning method. However, an alternative is to boil the die in TCE for five minutes with a rinse in isopropyl alcohol for 1-2 minutes.

DIE ATTACH:

The die attach operation should be done under a gaseous nitrogen ambient atmosphere to prevent oxidation. A preform should be used if the mounting surface has less than 50 microinches of gold and the die should be handled on the edges with tweezers. Die attach temperature should be between 385° C and 400° C with eutectic visible on three sides of the die after attachment.

BONDING:

Thermocompression gold ball or aluminum ultrasonic bonding may be used. The gold ball should be about 3 times the diameter of the gold wire. The ball should cover the bonding pad, but not excessively, or it may short out surrounding metallization. 1-mil aluminum wire may be used on most dice, but should not be used if the assembled unit will be plastic encapsulated.

HANDLING OF DICE:

All dice shown in this catalog are passivated devices and Intersil warrants that they will meet or exceed published specifications when handled with the following precautions:

- Dice should be stored in a dry inert-gas atmosphere.
- Dice should be assembled using normal semiconductor techniques.
- Dice should be attached in a gaseous nitrogen spray at a temperature less than 430° C.

ELECTRICAL TEST LIMITATIONS

DUAL BIPOLAR TRANSISTORS

LV_{ceo}	100V max. @ ≤1 mA
BV_{cbo}	100V max. @ ≥1 μA
BV_{ebo}	100V max. @ ≤10 mA
H_{fe}	≤1000 @ ≥10 μA
$V_{ce(SAT)}$	≥10 mV @ ≤10 mA
I_{cbo}	≥100 pA @ ≤100V
$V_{be1}-V_{be2}$	≥1 mV @ ≥10 μA
$I_{b1}-I_{b2}$	≥2 nA

FETS

Breakdown voltage	100V max. @ 1 μA
Pinch-off voltage	0-20V @ ≥1 nA
$V_{GS(TH)}$	0-20V @ ≥ 10 μA
$R_{DS(on)}$	20 Ω min. @ V_{GS} = 0 (V_{GS} = 30 MOSFETs)
I_{DSS} & $I_{D(on)}$	100 mA max.
gf_s	10,000 μMHOS max. @ I_D ≤ 10 mA
$I_{D(off)}$, $I_{S(off)}$, I_{GSS}	100 pA min.
$V_{GS1} - V_{GS2}$ (Duals)	10 mV min.

Electrical testing is guaranteed to a 10% LTPD. AC parameters such as capacitance and switching time cannot be tested in wafer or dice form.

STANDARD DIE CARRIER PACKAGE

- Easy to handle, store and inventory.
- 100% electrically probed dice with electrical rejects removed.
- 100% visually sorted with mechanical and visual rejects removed.
- Easy visual inspection — dice in carriers, geometry side up.
- Individual compartment for each die.
- Carriers usuable in customer production area.
- Carrier may be storage container for unused dice.
- Carriers hold 25, 100, or 400 dice, depending on die size and quantity ordered.
- Part numbers shown in this catalog are for carrier packaging.

B

OPTIONAL VIAL PACKAGE

- 100% electrically probed dice with rejects inked but included in vial. Bulk shipment.
- 10% extra good dice included (no charge) to cover possible breakage and/or visual rejects.
- Preferred for production quantities.
- Lower cost.
- For vial package – replace "D" in catalog number with "V", e.g.: 2N4416/D (2N4416 dice in carrier) becomes 2N4416/V (2N4416 dice in vial).

OPTIONAL WAFER PACKAGE

- 100% electrically probed – rejects inked.
- 10% extra good dice included (no charge) to cover possible breakage and/or visual rejects.
- Preferred for production quantities.
- Lowest cost.
- Wafer is supplied unscribed.
- For wafer package – replace "D" in catalog number with "W", e.g.: 2N4416/D (2N4416 dice in carrier) becomes 2N4416/W (2N4416 dice in wafer).

B

NOTE:

Intersil reserves the right to improve device geometries and manufacturing processes as required. These improvements may result in slight geometry changes. However, they will not affect the electrical limits, basic pad layouts or maximum die sizes in this catalog.

ELECTRICAL TEST CAPABILITY

As an example of how to use the capability chart to see what Intersil actually guarantees and tests for, on a 100% basis, compare the 2N4391 in a TO-18 package to the 2N4391 delivered as a chip.

Electrical Test Spec.	2N4391 in a TO-18	2N4391 Chip
I_{GSS} @ 25C	100 pA max.	100 pA max.
BV_{GSS}	40V min.	40V min.
$I_{D(off)}$ @ 25C	100 pA max.	100 pA max.
$V_{GS(forward)}$	1V max.	See note 1
$V_{GS(off)}$ or V_P	4V to 10V	4V to 10V
I_{DSS}	50 to 150 mA	50 to 100 mA
$V_{DS(on)}$	0.4V max.	0.4V max.
$r_{DS(on)}$	30Ω max.	30Ω max.
C_{iss}	14 pF max.	Guaranteed by Design
C_{rss}	3.5 pF max.	Guaranteed by Design
t_d	15ns max.	Guaranteed by Design
t_r	5ns max.	Guaranteed by Design
t_{off}	20ns max.	Guaranteed by Design
t_f	15 ns max.	Guaranteed by Design

NOTE 1: This parameter is very dependent upon quality of metallization surface to which chip is attached.

SUMMARY

Of the 14 items specified for the package part, only 7 can be tested and guaranteed in die form. It is to be noted that those specifications which cannot be tested in die form can be sample tested in package form as an indicator of lot performance. Many of the tests, however, such as capacitance tests, are design parameters.

The above electrical testing is guaranteed to a 10% LTPD. However, there are occasions where customer requirements cannot be satisfied by wafer sort testing alone. While the previously described tests will be done on a 100% basis, Intersil recognizes the need for additional testing to obtain confidence that a particular customer's needs can be met with a reasonably high yield. Toward this end Intersil has instituted a dice sampling plan which is two-fold. First, random samples of the dice are packaged and tested to assure adherence to the electrical specification. When required, wafers are identified and wafer identity is tied to the samples. This tests both the electrical character of the die and its ability to perform electrically after going through the high temperature dice attachment stage. Second, more severe testing can be performed on the packaged devices per individual customer needs. When testing is required other than that called out in the data sheet, Intersil issues an ITS number to describe the part. Examples of tighter testing which can be performed on packaged samples is shown as follows:

FET & DUAL FET PAIRS

1. Leakages to 1 pA (I_{gss})
2. $r_{DS\ (on)}$ to as low as 4 ohms
3. $I_{D\ (off)}$ to 10 pA
4. I_{DSS} to 1 amp (pulsed)
5. G_{FS} to 10,000 μmho
6. G_{os} to 1 μmho
7. e_n noise to 5 nV/$\sqrt{Hz}$ at frequencies of 10 Hz to 100 Hz
8. CMRR to 100 dB
9. $\Delta(V_{gs1}-V_{gs2})/\Delta T$ down to 10 μV/°C to an LTPD of 20%
10. g_m match to 5%
11. I_{DSS} match to 5%

TRANSISTOR PAIRS

1. Leakages to as low as 1 pA
2. Beta with collector current up to 50 mA and as low as 100 nA
3. f_T up to 500 MHz with collector currents in the range of 10 μA to 10 mA
4. Noise measurements as low as 5 nV/$\sqrt{Hz}$ from 10 Hz to 100 kc
5. $\Delta(V_{be1}-V_{be2})/\Delta T$ to 10 μV/°C to an LTPD of 20%

VISUAL INSPECTION

Individual chips are 100% inspected to MIL-STD-750, Method 2072 or, as an option, MIL-STD-883, Level B. Inspection is done to an LTPD of 20%. As an option, Intersil offers S.E.M. capability on all wafers.

B

CMOS INTEGRATED CIRCUIT CHIPS

INTRODUCTION

In addition to discrete device chips, Intersil also offers a full line of metal gate CMOS integrated circuits in die form. Die sales, however, present some unique problems. In many cases, chips cannot be guaranteed to the same electrical specifications as can the packaged parts. This is because leakage, noise, AC parameters and temperature testing cannot be guaranteed to the same degree of accuracy for dice as for packaged devices.

GENERAL PHYSICAL INFORMATION

- Chips are available with precise length and width dimensions, ±2 mils in either dimension.
- Chip thickness is 15 mils ±1 mil.
- Bonding pad and interconnect material is aluminum, 10K to 15K Å thick.
- Each die surface is protected by planar passivation and additional surface glassivation except for bonding pads and scribe lines. The surface passivation is removed from the bonding pad areas by an HF etchant; bonding pads may appear discolored at low magnification due to surface roughness of the aluminum caused by the etchant.
- Die are 100% inspected to electrical specifications, then visually inspected according to MIL-STD-883, Method 2010.2, Condition B, with modifications reflecting CMOS requirements.
- Bonding pad dimensions are 4.0 x 4.0 mils minimum.
- Storage temperature is -40°C to +150°C.
- Operating temperature is -20°C to +70°C.
- Guaranteed AQL Levels:

Visual	2.0%
Functional electrical testing	1.0%
Parametric DC testing	4.0%
Untested parameters	10.0%

CMOS INTEGRATED CIRCUIT CHIP PROCESSING FLOW CHART

B

RECOMMENDED DICE ASSEMBLY PROCEDURES

CLEANING

Dice supplied in die form do not require cleaning prior to assembly. However, if cleaning is desired, dice should be subjected to freon TF in a vapor degreaser and then vapor-dried.

RECOMMENDED HANDLING

Intersil recommends that dice be stored in the vacuum-sealed plastic bags which hold the dice carriers. Once removed from the sealed bags, the dice should be stored in a dry, inert-gas atmosphere.

Extreme care should be used when handling dice. Both electrical and visual damage can occur as the result of an unclean environment or harsh handling techniques.

DIE ATTACH

The die attach operation should be done under a gaseous nitrogen ambient atmosphere to prevent oxidization. If a eutectic die attach is used, it is recommended that a 98% gold/2% silicon preform be used at a die attach temperature between 385°C and 435°C. If an epoxy die attach is used, the epoxy cure temperature should not exceed 150°C. If hermetic packages are used, epoxy die attach should be carried out with caution so that there will be no "outgassing" of the epoxy.

BONDING

Thermocompression gold ball or aluminum ultrasonic bonding may be used. The wire should be 99.99% pure gold and the aluminum wire should be 99% aluminum/1% silicon. In either case, it is recommended that 1.0 mil wire be used for normal power circuits.

STANDARD DIE CARRIER PACKAGE

- Easy to handle, store and inventory.
- 100% electrically probed with electrical rejects removed.
- 100% visually sorted with mechanical and visual rejects removed.
- Easy visual inspection — dice are in carriers, geometry side up.
- Individual compartment for each die.
- Carriers usable in customer production area.
- Carrier may be used as storage contained for unused dice.
- Carriers hold 25, 100 or 400 dice, depending on die size and quantity ordered.
- Packaging of integrated circuit dice in carriers is identical to illustration shown earlier for discrete device, except that IC chips are not available in vial packs or in wafer form.

CHANGES

Intersil reserves the right in improve device geometries and manufacturing processes without prior notice. Although these improvements may result in slight geometry changes, they will not affect dice electrical limits, pad layouts, or maximum die sizes.

USER RESPONSIBILITY

Written notification of any non-conformance by Intersil of Intersil's dice specifications must be made within 75 days of the shipment date of the die to the user. Intersil assumes no responsibility for the dice after 75 days or after further user processing such as, but not limited to, chip mounting or wire bonding.

PART NUMBERS AND ORDER INFORMATION

Example of Intersil Part Number:

BASIC	SELECTION	TEMP	PKG	PIN	
ICH8500	A	C	T	V	ICH8500ACTV
ICL8038	C	C	P	D	ICL8038CCPD
IH5040		M	D	E	IH5040MDE

ON ALL INTERSIL IC PART NUMBERS. THE LAST THREE LETTERS ARE TEMPERATURE, PACKAGE, AND PIN NUMBER, RESPECTIVELY.

TEMPERATURE:
- C — Commercial
- I — Industrial
- M — Military

PACKAGE:
- D — Ceramic Dual-In-Line
- E — Small TO-8 Type
- F — Ceramic Flat Pack
- I — 16 Pin Dip (0.6 X 0.7) Lead Space
- J — Cerdip Dual-In-Line
- K — 8 Lead TO-3 Metal Can
- L — Leadless, Ceramic
- P — Epoxy Dual-In-Line
- Q — 2 Lead Metal Can
- T — TO-5 Type
- DR — TO-72 with No. 4 Lead Connected to Case

NUMBER OF PINS:
- A — 8
- B — 10
- C — 12
- D — 14
- E — 16
- N — 18
- F — 22
- G — 24
- I — 28
- J — 32
- K — 36
- L — 40
- M — 48
- V — 8, 0.230 in. Pin Circle
- W — 10, 0.230 in. Pin Circle
- Y — 8, No. 4 Lead Connected to Case
- Z — 10, No. 5 Lead Connected to Case.

LINEAR:

HYBRIDS:

WATCH AND CLOCK:

B

BIPOLAR MEMORY:

IM 5 6 00 C J E

- E — Number of Pins
- J — Package
- C — Temperature
  - M — −55°C to +125°C
  - C — 0°C to + 75°C
- 00 — Specific Chip Type
- 6 — General Type
  - 2 — Field Programmable Logic Array (FPLA)
  - 6 — Programmable Read Only Memory (PROM)
- 5 — Bipolar Process
- IM — Intersil Memory Circuit

MOS MEMORY:

IM 7 114 L 2 C J N

- N — Number of Pins
- J — Package
- C — Temperature Range
  - M — −55°C to +125°C
  - I — −40°C to + 85°C
  - C — 0°C to + 75°C
- 2 — Speed Selection
- L — Power Selection
- 114 — Device Chip Type
- 7 — MOS Process
- IM — Intersil Memory

C/MOS MEMORY:

IM 6 5 08 A −1 M D E

- E — Number of Pins
- D — Package
- M — Temperature
  - M — −55°C to +125°C
  - I — −40°C to + 85°C
  - C — 0°C to + 75°C
- −1 — Improved Speed, Reduced Current (optional)
- A — Operating Voltage (optional)
- 08 — Specific Chip Type
- 5 — General Type
  - 1 — Processing Elements
  - 3 — Read Only Memories (ROM)
  - 4 — Interface Elements
  - 5 — Random Access Memories (RAM)
  - 6 — Programmable Read Only Memory (PROM)
- 6 — C/MOS Process
- IM — Intersil Memory Circuit

VMOS PART NUMBERING (PROPRIETARY PARTS)

I V N 5 2 00 X Y Z

- Z — Breakdown Voltage
- Y — Z if Zener, N if None
- X — Package Code
- 00 — Selection
- 2 — Basic Type
- N — N or P
- I V — Intersil VMOS

BREAKDOWN VOLTAGE

A	20
B	30
C	35
D	40
E	60
F	80
G	90
H	100
J	125
K	150
L	175
M	200
N	225
P	250
Q	300
R	350
S	400
T	450
U	500

PACKAGE CODES

TO-237 (92+)	A
TO-202	B
TO-220	C
DICE	D
TO-66	H
TO-3	K
TO-52	S
TO-39	T

FOR INDIVIDUAL PART AVAILABILITY, PLEASE REFER TO A CURRENT INTERSIL PRICE LIST OR CONTACT YOUR NEAREST INTERSIL SALES OFFICE.

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Livonia, MI 48150
Tel: (313) 525-8100

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5251 W. 73rd St.
Edina, MN 55435
Tel: (612) 830-1800
TWX: 910-576-3125

Schweber Electronics
7402 Washington Avenue South
Eden Prairie, MN 55343
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Kansas City, MO 64120
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Tel: (314) 291-6200
TWX: 910-762-0632

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Tel: (603) 668-6968

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Pleasant Valley Avenue
Moorestown, NJ 08057
Tel: (609) 235-1900
TWX: 710-897-0829

Arrow Electronics
285 Midland Avenue
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Tel: (201) 797-5800
TWX: 710-988-2206

Diplomat Electronics, Inc.
490 South River Drive
Totowa, NJ 07512
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Albuquerque, NM 87123
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Bell Industries
Century Electronics Div.
11728 Linn NE
Albuquerque, NM 87123
Tel: (505) 292-2700
TWX: 910-989-0625

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Arrow Electronics
900 Broad Hollow Road
Farmingdale, NY 11735
Tel: (516) 694-6800
TWX: 510-224-6494

Arrow Electronics
399 Conklin Avenue
Farmingdale, NY 11735
Tel: (516) 694-1359

Components Plus
40 Oser Avenue
Hauppauge, NY 11787
Tel: (516) 231-9200
TWX: 510-227-9869

Harvey Federal Electronics
P.O. Box 1208
Binghamton, NY 13902
Tel: (607) 748-8211
TWX: 510-252-0893

Harvey Federal Electronics
10 Riverton Way
West Henrietta, NY 14586
Tel: (716) 334-5920
TWX: 510-253-7001

Schweber Electronics
2 Townline Circle
Rochester, NY 14623
Tel: (716) 424-2222

Schweber Electronics
Jericho Turnpike
Westbury, NY 11590
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Summit Distributors, Inc.
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P.O. Box 989
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RESCO/Raleigh
Rt. 8 Box 116-B
Highway 70 West
Raleigh, NC 27612
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TWX: 510-928-0590

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Solon, OH 44139
Tel: (216) 248-3990

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Schweber Electronics
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Tel: (513) 761-5432
TWX: 810-461-2670

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Component Specialties
7920 E. 40th Street
Tulsa, OK 74145
Tel: (918) 664-2820

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Parrott Electronics
8058 S.W. Nimbus Dr.
Beaverton, OR 97005
Tel: (503) 641-3355

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Schweber Electronics
101 Rock Road
Horsham, PA 19044
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Sheridan Associates
4297 Greensburgh Pike
Suite #3114
Pittsburgh, PA 15221
Tel: (412) 351-4000

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Arrow Electronics
13715 Gamma Road
Dallas, TX 75234
Tel: (214) 386-7500

Arrow Electronics
10700 Corporate Drive
Stafford, TX 77477
Tel: (713) 491-4100

Component Specialties inc.
8222 Jamestown Drive
Suite 115
Austin, TX 78758
Tel: (512) 837-8922

Component Specialties
10907 Shady Trail
Dallas, TX 75220
Tel: (214) 357-6511

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Houston, TX 77036
Tel: (713) 771-7237

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14177 Proton Street
Dallas, TX 75240
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TWX: 910-860-5493

Schweber Electronics
7420 Harwin Drive
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TWX: 910-881-1109

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Salt Lake City, UT 84119
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TWX: 910-925-5698

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3695 West 1987 South
Salt Lake City, UT 84104
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1005 Andover Park East
Tukwila, WA 98188
Tel: (206) 575-4420

Wyle Distribution Group
1750 132nd Ave., N.E.
Bellevue, WA 98005
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Arrow Electronics
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Oak Creek, WI 53514
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Waukesha, WI 53186

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