# **Complementary Silicon Plastic Power Transistors**

These devices are designed for use in general–purpose amplifier and switching applications.

#### **Features**

- High DC Current Gain
- High Current Gain Bandwidth Product
- TO-220 Compact Package
- These Devices are Pb-Free and are RoHS Compliant\*

#### MAXIMUM RATINGS (Note 1)

Rating	Symbol	Value	Unit
Collector–Emitter Voltage 2N6111, 2N6288 2N6109 2N6107, 2N6292	V <sub>CEO</sub>	30 50 70	Vdc
Collector-Base Voltage 2N6111, 2N6288 2N6109 2N6107, 2N6292	V <sub>CB</sub>	40 60 80	Vdc
Emitter-Base Voltage	V <sub>EB</sub>	5.0	Vdc
Collector Current - Continuous	I <sub>C</sub>	7.0	Adc
Collector Current – Peak	I <sub>CM</sub>	10	Adc
Base Current	Ι <sub>Β</sub>	3.0	Adc
Total Power Dissipation @ T <sub>C</sub> = 25°C Derate above 25°C	P <sub>D</sub>	40 0.32	W W/°C
Operating and Storage Junction Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	-65 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

Indicates JEĎEC Registered Data.
 THERMAL CHARACTERISTICS

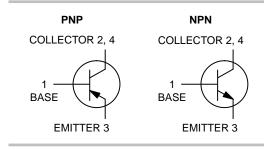
I	Characteristics	Symbol	Max	Unit
	Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	3.125	°C/W

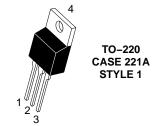


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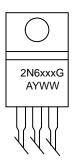
www.onsemi.com

# 7 AMPERE POWER TRANSISTORS COMPLEMENTARY SILICON 30 – 50 – 70 VOLTS, 40 WATTS





#### MARKING DIAGRAM



2N6xxx = Specific Device Code xxx = See Table on Page 4 G = Pb-Free Package A = Assembly Location

Y = Year WW = Work Week

#### **ORDERING INFORMATION**

See detailed ordering, marking, and shipping information in the package dimensions section on page 4 of this data sheet.

<sup>\*</sup>For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# **ELECTRICAL CHARACTERISTICS** ( $T_C = 25^{\circ}C$ unless otherwise noted) (Note 2)

Characteristic	Symbol	Min	Max	Unit
OFF CHARACTERISTICS			•	•
Collector–Emitter Sustaining Voltage (Note 3) $ \begin{pmatrix} I_C = 100 \text{ mAdc, } I_B = 0 \end{pmatrix} $ $ 2N6111, 2N6288 $ $ 2N6109 $ $ 2N6107, 2N6292 $	V <sub>CEO(sus)</sub>	30 50 70	- - -	Vdc
Collector Cutoff Current (V <sub>CE</sub> = 20 Vdc, I <sub>B</sub> = 0) 2N6111, 2N6288	I <sub>CEO</sub>	-	1.0	mAdc
(V <sub>CE</sub> = 40 Vdc, I <sub>B</sub> = 0) 2N6109 (V <sub>CE</sub> = 60 Vdc, I <sub>B</sub> = 0) 2N6107, 2N6292		-	1.0 1.0	
Collector Cutoff Current (V <sub>CE</sub> = 40 Vdc, V <sub>EB(off)</sub> = 1.5 Vdc) 2N6111, 2N6288	ICEX	-	100	μAdc
(V <sub>CE</sub> = 60 Vdc, V <sub>EB(off)</sub> = 1.5 Vdc) 2N6109 (V <sub>CE</sub> = 80 Vdc, V <sub>EB(off)</sub> = 1.5 Vdc) 2N6107, 2N6292		-	100 100	
(V <sub>CE</sub> = 30 Vdc, V <sub>EB(off)</sub> = 1.5 Vdc, T <sub>C</sub> = 150°C) 2N6111, 2N6288 (V <sub>CE</sub> = 50 Vdc, V <sub>EB(off)</sub> = 1.5 Vdc, T <sub>C</sub> = 150°C)		-	2.0	mAdc
2N6109 (V <sub>CE</sub> = 70 Vdc, V <sub>EB(off)</sub> = 1.5 Vdc, T <sub>C</sub> = 150°C) 2N6107, 2N6292		-	2.0	
Emitter Cutoff Current (V <sub>BE</sub> = 5.0 Vdc, I <sub>C</sub> = 0)	I <sub>EBO</sub>	-	1.0	mAdc
ON CHARACTERISTICS (Note 3)				
DC Current Gain $ \begin{aligned} &(I_C = 2.0 \text{ Adc, } V_{CE} = 4.0 \text{ Vdc}) \\ &2N6107, 2N6292 \\ &(I_C = 2.5 \text{ Adc, } V_{CE} = 4.0 \text{ Vdc}) \\ &2N6109 \\ &(I_C = 3.0 \text{ Adc, } V_{CE} = 4.0 \text{ Vdc}) \\ &2N6111, 2N6288 \\ &(I_C = 7.0 \text{ Adc, } V_{CE} = 4.0 \text{ Vdc}) \\ &All \text{ Devices} \end{aligned} $	h <sub>FE</sub>	30 30 30 2.3	150 150 150 –	-
Collector–Emitter Saturation Voltage (I <sub>C</sub> = 7.0 Adc, I <sub>B</sub> = 3.0 Adc)	V <sub>CE(sat)</sub>	-	3.5	Vdc
Base–Emitter On Voltage $(I_C = 7.0 \text{ Adc}, V_{CE} = 4.0 \text{ Vdc})$	V <sub>BE(on)</sub>	-	3.0	Vdc
DYNAMIC CHARACTERISTICS				
Current Gain – Bandwidth Product (Note 4) ( $I_C = 500 \text{ mAdc}$ , $V_{CE} = 4.0 \text{ Vdc}$ , $f_{test} = 1.0 \text{ MHz}$ ) 2N6288, 2N6292 2N6107, 2N6109, 2N6111	f⊤	4.0 10	<u>-</u>	MHz
Output Capacitance (V <sub>CB</sub> = 10 Vdc, I <sub>E</sub> = 0, f = 1.0 MHz)	C <sub>ob</sub>	-	250	pF
Small–Signal Current Gain ( $I_C = 0.5 \text{ Adc}$ , $V_{CE} = 4.0 \text{ Vdc}$ , $f = 50 \text{ kHz}$ )	h <sub>fe</sub>	20	-	_

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. Indicates JEDEC Registered Data.

3. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

<sup>4.</sup>  $f_T = |h_{fe}| \cdot f_{test}$ 

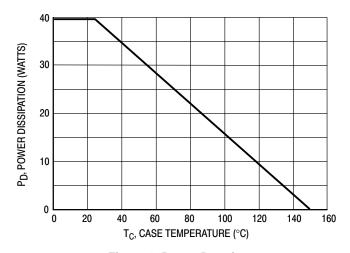
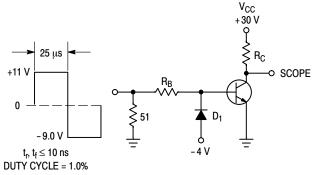


Figure 1. Power Derating



R<sub>B</sub> and R<sub>C</sub> ARE VARIED TO OBTAIN DESIRED CURRENT LEVELS

D1 MUST BE FAST RECOVERY TYPE, eg: 1N5825 USED ABOVE IB  $\approx$  100 mA MSD6100 USED BELOW IB  $\approx$  100 mA

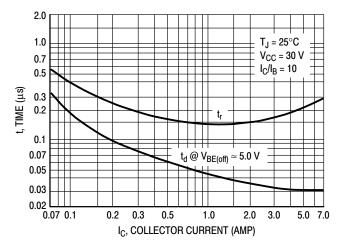


Figure 2. Switching Time Test Circuit

Figure 3. Turn-On Time

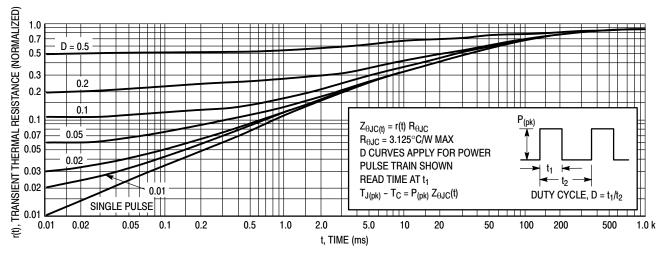


Figure 4. Thermal Response

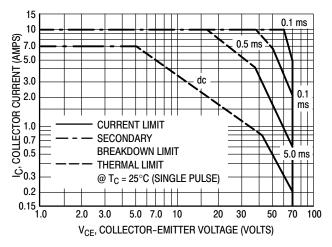


Figure 5. Active-Region Safe Operating Area

There are two limitations on the power handling ability of a transistor: average junction temperature and second breakdown. Safe operating area curves indicate  $I_C - V_{CE}$  limits of the transistor that must be observed for reliable operation; i.e., the transistor must not be subjected to greater dissipation than the curves indicate.

The data of Figure 5 is based on  $T_{J(pk)} = 150^{\circ}C$ ;  $T_{C}$  is variable depending on conditions. Second breakdown pulse limits are valid for duty cycles to 10% provided  $T_{J(pk)} \leq 150^{\circ}C$ .  $T_{J(pk)}$  may be calculated from the data in Figure 4. At high case temperatures, thermal limitations will reduce the power that can be handled to values less than the limitations imposed by second breakdown.

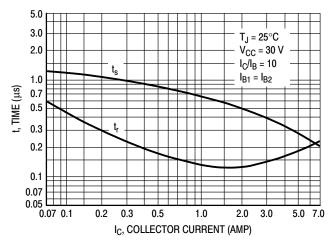


Figure 6. Turn-Off Time

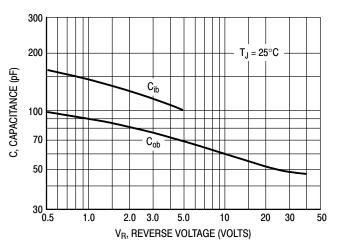


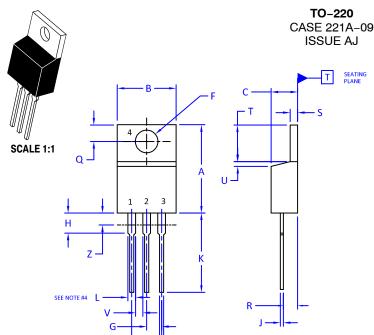
Figure 7. Capacitance

#### **ORDERING INFORMATION**

Device	Device Marking	Package	Shipping
2N6107G	2N6107	TO-220 (Pb-Free)	50 Units / Rail
2N6109G	2N6109	TO-220 (Pb-Free)	50 Units / Rail
2N6111G	2N6111	TO-220 (Pb-Free)	50 Units / Rail
2N6288G	2N6288	TO-220 (Pb-Free)	50 Units / Rail
2N6292G	2N6292	TO-220 (Pb-Free)	50 Units / Rail

# **MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS**





### **DATE 05 NOV 2019**

- 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 2009.
- 2. CONTROLLING DIMENSION: INCHES

NOTES:

3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

#### 4. MAX WIDTH FOR F102 DEVICE = 1.35MM

	INCHES		MILLIMETERS		
DIM	MIN.	MAX.	MIN.	MAX.	
Α	0.570	0.620	14.48	15.75	
В	0.380	0.415	9.66	10.53	
С	0.160	0.190	4.07	4.83	
D	0.025	0.038	0.64	0.96	
F	0.142	0.161	3.60	4.09	
G	0.095	0.105	2.42	2.66	
Н	0.110	0.161	2.80	4.10	
J	0.014	0.024	0.36	0.61	
К	0.500	0.562	12.70	14.27	
L	0.045	0.060	1.15	1.52	
N	0.190	0.210	4.83	5.33	
Q	0.100	0.120	2.54	3.04	
R	0.080	0.110	2.04	2.79	
S	0.045	0.055	1.15	1.41	
Т	0.235	0.255	5.97	6.47	
U	0.000	0.050	0.00	1.27	
V	0.045		1.15		
Z		0.080		2.04	

STYLE 1:		STYLE 2:		STYLE 3:		STYLE 4:	
PIN 1.	BASE	PIN 1.	BASE	PIN 1.	CATHODE	PIN 1.	MAIN TERMINAL 1
2.	COLLECTOR	2.	EMITTER	2.	ANODE	2.	MAIN TERMINAL 2
3.	EMITTER	3.	COLLECTOR	3.	GATE	3.	GATE
4.	COLLECTOR	4.	EMITTER	4.	ANODE	4.	MAIN TERMINAL 2
STYLE 5:		STYLE 6:		STYLE 7:		STYLE 8:	
PIN 1.	GATE	PIN 1.	ANODE	PIN 1.	CATHODE	PIN 1.	CATHODE
2.	DRAIN	2.	CATHODE	2.	ANODE	2.	ANODE
3.	SOURCE	3.	ANODE	3.	CATHODE	3.	EXTERNAL TRIP/DELA
4.	DRAIN	4.	CATHODE	4.	ANODE	4.	ANODE
STYLE 9:		STYLE 10:		STYLE 11:		STYLE 12	:
PIN 1.	GATE	PIN 1.	GATE	PIN 1.	DRAIN	PIN 1.	MAIN TERMINAL 1
2.	COLLECTOR	2.	SOURCE	2.	SOURCE	2.	MAIN TERMINAL 2
3.	EMITTER	3.	DRAIN	3.	GATE	3.	GATE
4.	COLLECTOR	4.	SOURCE	4.	SOURCE	4.	NOT CONNECTED

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