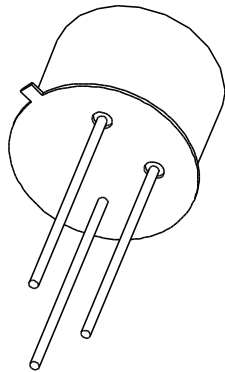


# DATA SHEET



## **BFY50; BFY51; BFY52** NPN medium power transistors

Product specification  
Supersedes data of September 1994  
File under Discrete Semiconductors, SC04

1997 Apr 22

NPN medium power transistors

BFY50; BFY51; BFY52

FEATURES

- High current (max. 1 A)
- Low voltage (max. 35 V).

APPLICATIONS

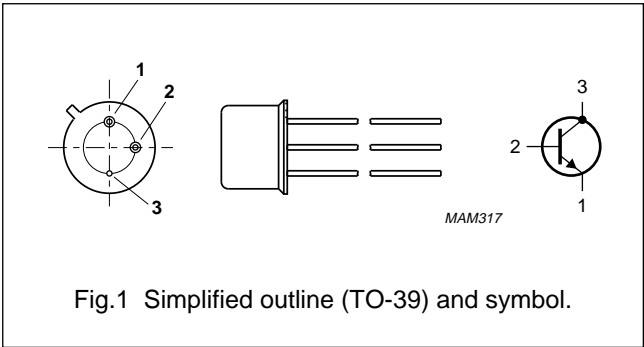
- General purpose industrial applications.

DESCRIPTION

NPN medium power transistor in a TO-39 metal package.

PINNING

PIN	DESCRIPTION
1	emitter
2	base
3	collector, connected to case



QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter				
	BFY50		—	—	80	V
	BFY51		—	—	60	V
	BFY52		—	—	40	V
$V_{CEO}$	collector-emitter voltage	open base				
	BFY50		—	—	35	V
	BFY51		—	—	30	V
	BFY52		—	—	20	V
$I_{CM}$	peak collector current		—	—	1	A
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ }^{\circ}\text{C}$	—	—	800	mW
		$T_{case} \leq 100\text{ }^{\circ}\text{C}$	—	—	2.86	W
$h_{FE}$	DC current gain	$I_C = 150\text{ mA}; V_{CE} = 10\text{ V}$				
	BFY50		30	112	—	
	BFY51		40	123	—	
	BFY52		60	142	—	
$f_T$	transition frequency	$I_C = 50\text{ mA}; V_{CE} = 10\text{ V}; f = 100\text{ MHz}$				
	BFY50		60	—	—	MHz
	BFY51; BFY52		50	—	—	MHz

## NPN medium power transistors

## BFY50; BFY51; BFY52

**LIMITING VALUES**

In accordance with the Absolute Maximum Rating System (IEC 134).

SYMBOL	PARAMETER	CONDITIONS	MIN.	MAX.	UNIT
$V_{CBO}$	collector-base voltage	open emitter			
	BFY50		–	80	V
	BFY51		–	60	V
	BFY52		–	40	V
$V_{CEO}$	collector-emitter voltage	open base			
	BFY50		–	35	V
	BFY51		–	30	V
	BFY52		–	20	V
$V_{EBO}$	emitter-base voltage	open collector	–	6	V
$I_C$	collector current (DC)		–	1	A
$I_{CM}$	peak collector current		–	1	A
$I_{BM}$	peak base current		–	100	mA
$P_{tot}$	total power dissipation	$T_{amb} \leq 25\text{ °C}$	–	800	mW
		$T_{case} \leq 25\text{ °C}$	–	5	W
		$25\text{ °C} < T_{case} < 100\text{ °C}$	–	2.86	W
$T_{stg}$	storage temperature		–65	+150	°C
$T_j$	junction temperature		–	200	°C
$T_{amb}$	operating ambient temperature		–65	+150	°C

**THERMAL CHARACTERISTICS**

SYMBOL	PARAMETER	CONDITIONS	VALUE	UNIT
$R_{th\ j-a}$	thermal resistance from junction to ambient	in free air	220	K/W
$R_{th\ j-c}$	thermal resistance from junction to case		35	K/W

## NPN medium power transistors

## BFY50; BFY51; BFY52

**CHARACTERISTICS** $T_j = 25\text{ °C}$  unless otherwise specified.

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$I_{CBO}$	collector cut-off current BFY50	$I_E = 0; V_{CB} = 60\text{ V}$	–	–	50	nA
		$I_E = 0; V_{CB} = 60\text{ V}; T_j = 100\text{ °C}$	–	–	2.5	$\mu\text{A}$
		$I_E = 0; V_{CB} = 80\text{ V}$	–	–	500	nA
		$I_E = 0; V_{CB} = 80\text{ V}; T_j = 100\text{ °C}$	–	–	30	$\mu\text{A}$
$I_{CBO}$	collector cut-off current BFY51	$I_E = 0; V_{CB} = 40\text{ V}$	–	–	50	nA
		$I_E = 0; V_{CB} = 40\text{ V}; T_j = 100\text{ °C}$	–	–	2.5	$\mu\text{A}$
		$I_E = 0; V_{CB} = 60\text{ V}$	–	–	500	nA
		$I_E = 0; V_{CB} = 60\text{ V}; T_j = 100\text{ °C}$	–	–	30	$\mu\text{A}$
$I_{CBO}$	collector cut-off current BFY52	$I_E = 0; V_{CB} = 30\text{ V}$	–	–	50	nA
		$I_E = 0; V_{CB} = 30\text{ V}; T_j = 100\text{ °C}$	–	–	2.5	$\mu\text{A}$
		$I_E = 0; V_{CB} = 40\text{ V}$	–	–	500	nA
		$I_E = 0; V_{CB} = 40\text{ V}; T_j = 100\text{ °C}$	–	–	30	$\mu\text{A}$
$I_{EBO}$	emitter cut-off current	$I_C = 0; V_{EB} = 5\text{ V}$	–	–	50	nA
		$I_C = 0; V_{EB} = 5\text{ V}; T_j = 100\text{ °C}$	–	–	2.5	$\mu\text{A}$
		$I_C = 0; V_{EB} = 6\text{ V}$	–	–	500	nA
$h_{FE}$	DC current gain BFY50	$I_C = 10\text{ mA}; V_{CE} = 10\text{ V}$	20	–	–	
		$I_C = 150\text{ mA}; V_{CE} = 10\text{ V}$	30	–	–	
		$I_C = 500\text{ mA}; V_{CE} = 10\text{ V}$	20	–	–	
		$I_C = 1\text{ A}; V_{CE} = 10\text{ V}$	15	–	–	
$h_{FE}$	DC current gain BFY51	$I_C = 10\text{ mA}; V_{CE} = 10\text{ V}$	30	–	–	
		$I_C = 150\text{ mA}; V_{CE} = 10\text{ V}$	40	–	–	
		$I_C = 500\text{ mA}; V_{CE} = 10\text{ V}$	25	–	–	
		$I_C = 1\text{ A}; V_{CE} = 10\text{ V}$	15	–	–	
$h_{FE}$	DC current gain BFY52	$I_C = 10\text{ mA}; V_{CE} = 10\text{ V}$	30	–	–	
		$I_C = 150\text{ mA}; V_{CE} = 10\text{ V}$	60	–	–	
		$I_C = 500\text{ mA}; V_{CE} = 10\text{ V}$	30	–	–	
		$I_C = 1\text{ A}; V_{CE} = 10\text{ V}$	15	–	–	

## NPN medium power transistors

## BFY50; BFY51; BFY52

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
V <sub>CEsat</sub>	collector-emitter saturation voltage BFY50	I <sub>C</sub> = 10 mA; I <sub>B</sub> = 1 mA	–	–	200	mV
		I <sub>C</sub> = 150 mA; I <sub>B</sub> = 15 mA	–	–	200	mV
		I <sub>C</sub> = 500 mA; I <sub>B</sub> = 50 mA	–	–	700	mV
		I <sub>C</sub> = 1 A; I <sub>B</sub> = 100 mA	–	–	1	V
V <sub>CEsat</sub>	collector-emitter saturation voltage BFY51; BFY52	I <sub>C</sub> = 10 mA; I <sub>B</sub> = 1 mA	–	–	200	mV
		I <sub>C</sub> = 150 mA; I <sub>B</sub> = 15 mA	–	–	350	mV
		I <sub>C</sub> = 500 mA; I <sub>B</sub> = 50 mA	–	–	1	V
		I <sub>C</sub> = 1 A; I <sub>B</sub> = 100 mA	–	–	1.6	V
V <sub>BEsat</sub>	base-emitter saturation voltage	I <sub>C</sub> = 10 mA; I <sub>B</sub> = 1 mA	–	–	1.2	V
		I <sub>C</sub> = 150 mA; I <sub>B</sub> = 15 mA	–	–	1.3	V
		I <sub>C</sub> = 500 mA; I <sub>B</sub> = 50 mA	–	–	1.5	V
		I <sub>C</sub> = 1 A; I <sub>B</sub> = 100 mA	–	–	2	V
C <sub>c</sub>	collector capacitance	I <sub>E</sub> = i <sub>e</sub> = 0; V <sub>CB</sub> = 10 V; f = 1 MHz	–	7	12	pF
f <sub>T</sub>	transition frequency BFY50	I <sub>C</sub> = 50 mA; V <sub>CE</sub> = 10 V; f = 100 MHz; T <sub>amb</sub> = 25 °C	60	140	–	MHz
	BFY51; BFY52		50	–	–	MHz
Switching times (between 10% and 90% levels)						
t <sub>on</sub>	turn-on time	I <sub>Con</sub> = 150 mA; I <sub>Bon</sub> = 15 mA; I <sub>Boff</sub> = –15 mA	–	55	–	ns
t <sub>d</sub>	delay time		–	15	–	ns
t <sub>r</sub>	rise time		–	40	–	ns
t <sub>off</sub>	turn-off time		–	360	–	ns
t <sub>s</sub>	storage time		–	300	–	ns
t <sub>f</sub>	fall time		–	60	–	ns

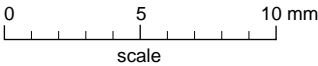
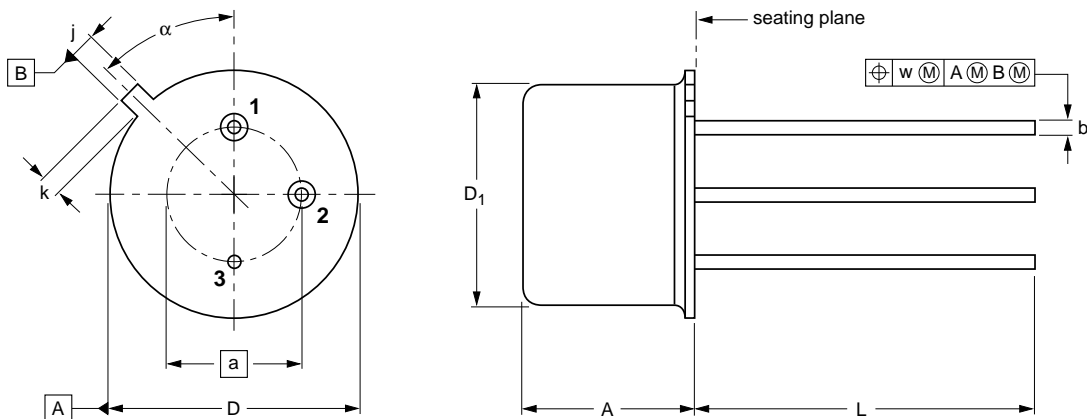
NPN medium power transistors

BFY50; BFY51; BFY52

PACKAGE OUTLINE

Metal-can cylindrical single-ended package; 3 leads

SOT5/11



DIMENSIONS (mm are the original dimensions)

UNIT	A	a	b	D	D <sub>1</sub>	j	k	L	w	α
mm	6.60 6.35	5.08	0.48 0.41	9.39 9.08	8.33 8.18	0.85 0.75	0.95 0.75	14.2 12.7	0.2	45°

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT5/11		TO-39				97-04-11

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**NPN medium power transistors****BFY50; BFY51; BFY52**

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**DEFINITIONS**

<b>Data Sheet Status</b>	
Objective specification	This data sheet contains target or goal specifications for product development.
Preliminary specification	This data sheet contains preliminary data; supplementary data may be published later.
Product specification	This data sheet contains final product specifications.
<b>Limiting values</b>	
Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.	
<b>Application information</b>	
Where application information is given, it is advisory and does not form part of the specification.	

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