CURTIS ELECTROMUSIC SPECIALTIES

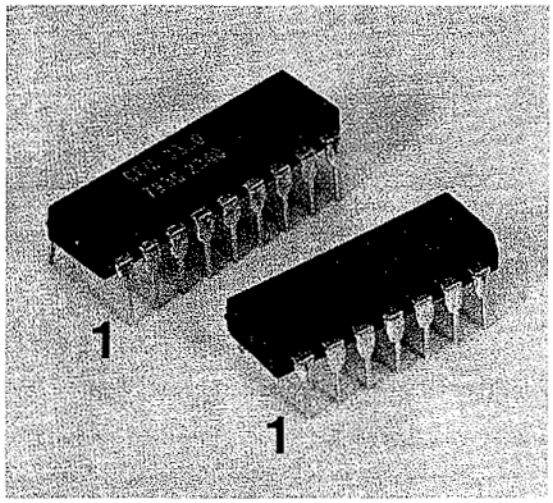
CEM 3330 / 3335

Dual Voltage Controlled Amplifier

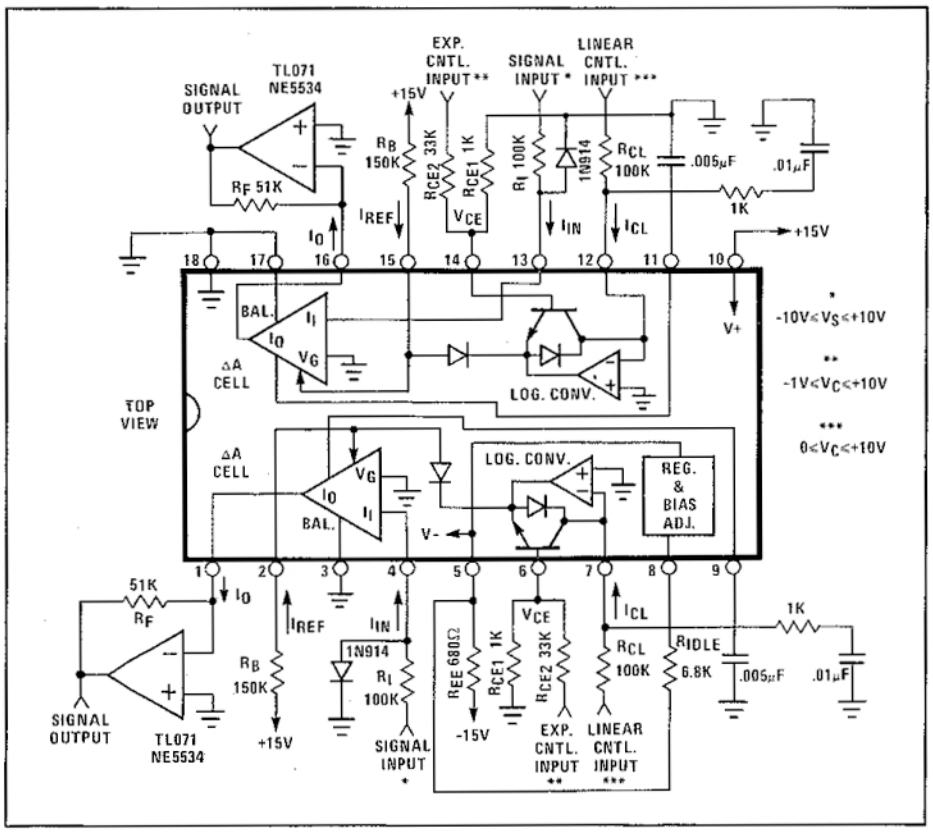
The CEM 3330 and CEM 3335 are dual, high performance, voltage controlled amplifiers intended for electronic musical instrument and professional audio applications. For the 3330, each amplifier includes complete circuitry for simultaneous linear and exponential control of gain. In addition, the operating point of the amplifiers may be set anywhere from Class B to Class A, allowing the user to optimize those parameters critical to the particular application. Also featured are virtual ground summing nodes for both the signal and linear control inputs, so that signal and control mixing may be accomplished within the device itself. Finally, the VCA outputs are signal currents, allowing the device to be conveniently used in two-pole voltage controlled filters, as well as dual voltage controlled amplifiers.

The 3335 is the same device as the 3330 but without the linear control circuitry, and is intended for those applications which require only the exponential control of gain.

The devices include an on-chip 6.5 volt Zener, allowing them to operate off ±15 volt supplies as well as +15, -5 volt supplies.



CEM 3330 Circuit Block and Connection Diagram



Features

- Low Cost
- Two Independent Voltage Controlled Amplifiers in a Single Package
- Simultaneous Linear and Exponential Control Inputs
- Wide Control Range: 120dB min.
- Very Accurate Control Scales for Excellent Gain Tracking
- Exceptionally Low Control Voltage Feedthrough: -60dB minimum without trim, better than -80dB with trim
- Low Distortion: Less than 0.1%
- Exceptionally Low Noise: Better than -100dB
- Class B to Class A Operation
- Summing Signal and Linear Control Inputs
- Current Outputs for Ease of Use in Voltage Controlled 2-Pole Filters
- Can Be Used in VCO and VCF Control Paths Without Causing Shift
- ±15 Volt Supplies

Electrical Characteristics

V_{CC} = +15V		T_A = 25°C			
Parameter	Conditions	Min	Typ	Max	Units
Exponential Control Range		120	150	–	dB
Linear Control Range		100	130		dB
Peak Cell Current, I_{CP} (input plus output)	Class B	±400	±600	–	μA
	Class A	±800	±1400	–	μA
Exponential Control Scale Sensitivity		2.8	3.0	3.2	mV/dB
Tempco of Exponential Control Scale		+3000	+3300	+3600	ppm
Tempco of Linear Control Scale		–	±100	±300	ppm
Exponential Control Scale Error[1]		–	0.3	1	dB
Linear Control Scale Error[1]	$0<I_{CL}<100\mu A$	–	0.3	1.5	%
Cell Current Gain	V_G = 0	.83	1	1.2	
Current Gain Tempco	V_G = 0	–	±100	±300	ppm
Log Converter Output	$I_{CL} = I_{REF}$	-5	0	+5	mV
Output Voltage Compliance		-.3	–	+13.5	V
Untrimmed Distortion[2]	Class B	–	1.5	5	%
	Class A	–	0.3	1	%
Trimmed Distortion[2]	Class B	–	0.2	0.8	%
	Class A	–	.05	0.2	%
Untrimmed Control Feedthrough[3]	Class B	–	0.2	0.8	μA
	Class A	–	7	25	μA
Trimmed Control Feedthrough[3]	Class B	–	.01	.08	μA
	Class A	–	1	5	μA
Output Noise Current in 20KHz Bandwidth (V_G = 0)	Class B	–	1.2	3.5	nARMS
	Class A	–	3.5	12	nARMS
Signal Current Bandwidth[4]	Class B	30	100	–	KHz
	Class A	100	350	–	KHz
Signal Current Slew Rate	Class B	60	150	–	μA/μS
	Class A	400	750	–	μA/μS
Crosstalk Between VCAs	F = 10KHz	-60	-70	–	dB
Internal Bias Current at Signal & Linear Control Inputs	Class B	80	175	350	nA
	Class A	130	300	600	nA
Exponential Control Input Current	I_{CL} = 100μA	.4	0.8	1.3	μA
Linear Control Input Offset Voltage		-7	+3	+15	mV
Signal Input Offset Voltage		-15	-5	+5	mV
Positive Supply Current	Class B	0.8	1.3	2.1	mA
	Class A	2.1	2.7	3.7	mA
Positive Supply Range		+9	–	+18	V
Negative Supply Range[5]		-4.5	–	-18	V

Note 1: From current gains of +20dB to -80dB. Peak cell current is less than 100μA.
Note 2: Output signal is 10dB below clipping and is at a frequency of 1KHz. V_G = 0
Note 3: Current gain varies from unity to maximum attenuation (>110dB).
Note 4: Peak Output Current is ±200μA.
Note 5: Current limiting resistor required for negative voltages greater than –6 volts.
Note 6: Class B is defined at an idle current of 1μA; Class A is at an idle current of 100μA.

Application Hints

Supplies

Since the device can withstand no more than 24 volts between its supply pins, an internal 6.5 volt ±10% Zener diode has been provided to allow the chip to run off virtually any negative supply voltage. If the negative supply is between -4.5 and -6.0 volts, it may be connected directly to the negative supply pin (pin 5). For voltages greater than -7.5 volts, a series current limiting resistor must be added between pin 5 and the supply. Its value is calculated as follows:

$$R_{EE} = (V_{EE} - 7.2)/I_{EE}$$

where I_{EE} is .010 for idle currents less than 10μA, .012 for idle currents between 10μA and 50μA, and .014 for idle currents between 50μA and 200μA. (See Selection of Quiescent Operating Current).

Although the circuit was designed for a positive supply voltage of +15 volts, it may be operated from any voltage between +9 and +18 volts with little effect on performance.

Basic Operation

Each of the two voltage controlled amplifiers consists of a variable gain cell and, in the case of the 3330, a log converter as well (see Block Diagrams). The gain cell is the current-in, current-out type, accepting a bipolar input current, I_{IN}, and providing a bipolar output current, I_O, with the following relationship:

$$I_O = -I_{IN} e^{-V_G/V_T} \qquad V_T = KT/q$$

where V_G is the voltage applied to the direct control input of each gain cell (pin 2 and pin 15 on the 3330, pin 2 and pin 11 on the 3335).

For the 3330, the log converter generates the logarithm of the linear control input current,

I_{CL}, (pin 7 and pin 12) while transmitting the exponential control input, V_{CE}, (pins 6 and 14) unchanged to its output. The transfer function for each log converter is:

$$V_{OLC} = -V_T \ln \frac{I_{CL}}{I_{REF}} + V_{CE} = V_G$$

where I_{REF} is the current sourced into the direct control input. Since the output of the log converter internally connects to the direct control input of the gain cell, the overall current gain of the gain cell is given by:

$$I_O = -I_{IN} \cdot \frac{I_{CL}}{I_{REF}} \cdot e^{-V_{CE}/V_T}$$

For proper operation, the linear control current, I_{CL}, and reference current, I_{REF}, are positive in polarity; that is, they flow into the device. A negative input current for I_{CL} will simply shut the gain completely off, while a negative reference current should be avoided. The signal input current may, of course, be either polarity.

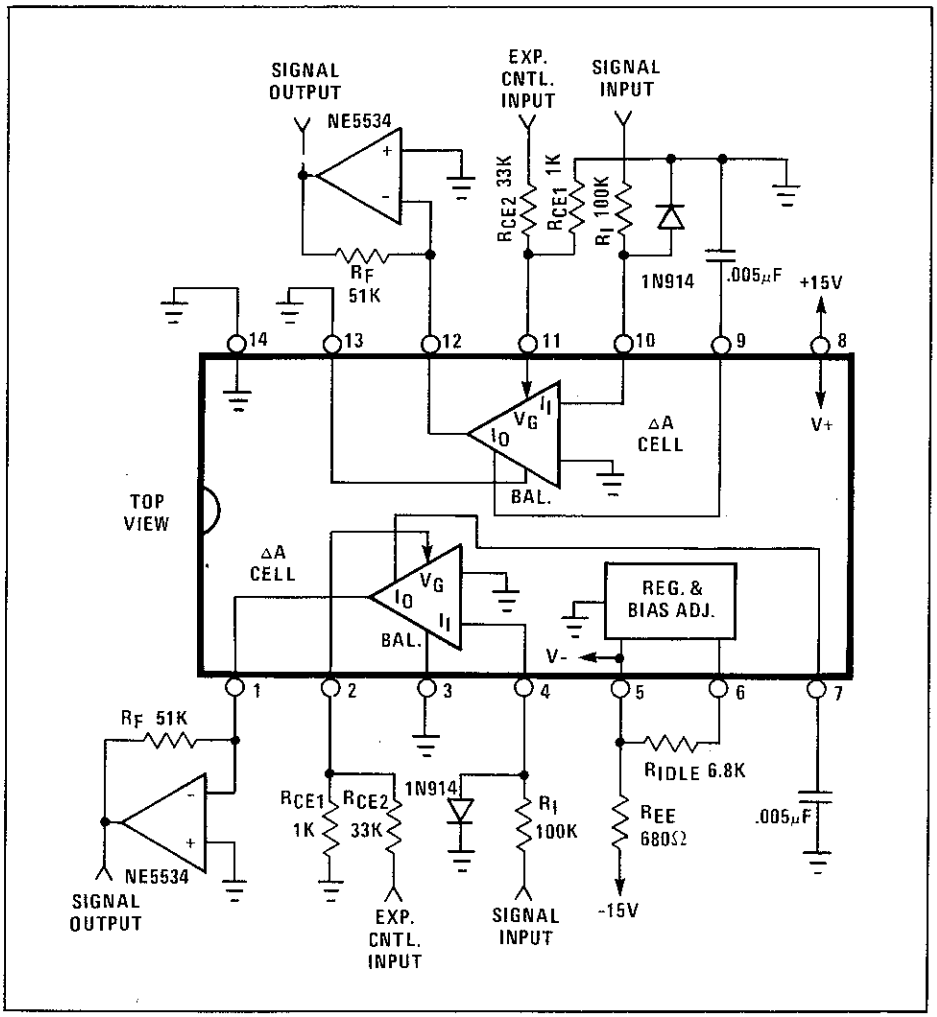
The Block Diagrams show typical external components connections to the devices. The signal inputs and the linear control inputs are virtual ground summing nodes; therefore, the signal input currents and linear control currents may be accurately generated from their respective voltages simply with resistors terminating at these nodes. Note that these virtual ground inputs also allow multiple input voltages to be mixed (linearly added) on-chip by merely adding more input resistors.

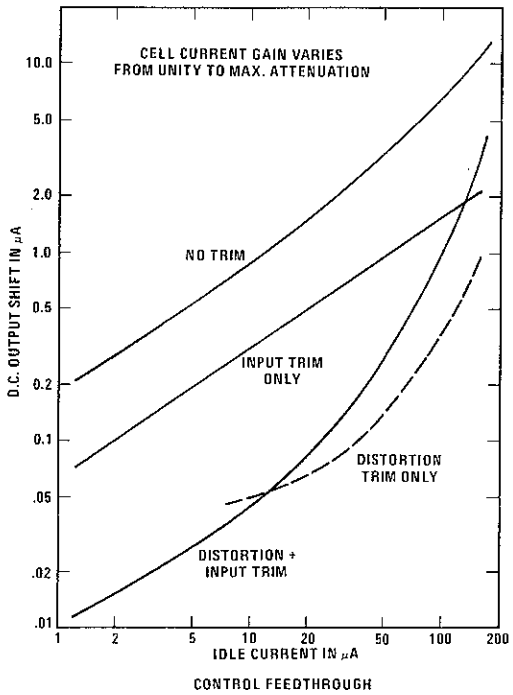
Although the voltage compliance of the gain cell outputs ranges from -0.3V to V_{CC} - 1.5V, best results are obtained by feeding the outputs into virtual ground inputs. Thus, in the Block Diagrams, the output currents are converted to voltages with external op amps.

Absolute Maximum Ratings

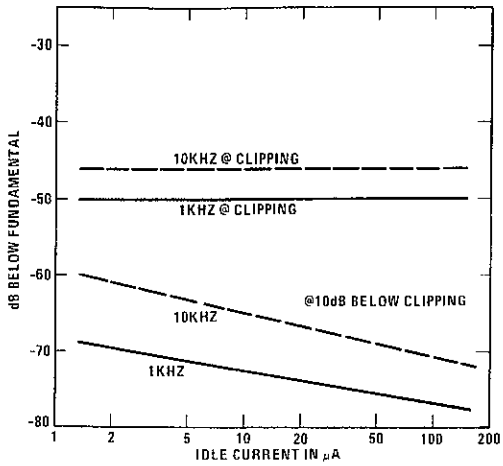
Voltage Between V_{CC} and V_{EE} Pins	+24V,-0.5V
Voltage Between V_{CC} and Ground Pins	+18V,-0.5V
Voltage Between V_{EE} and Ground Pins	-6.0V,+0.5V
Voltage Between Output and Distortion Trim or Ground Pins	+18V,-0.5V
Voltage Between All Other Pins and Ground Pin	±6.0V
Current Through Any Pin	±40mA
Storage Temperature Range	-55°C to +150°C
Operating Temperature Range	-25°C to +75°C

CEM 3335 Circuit Block and Connection Diagram

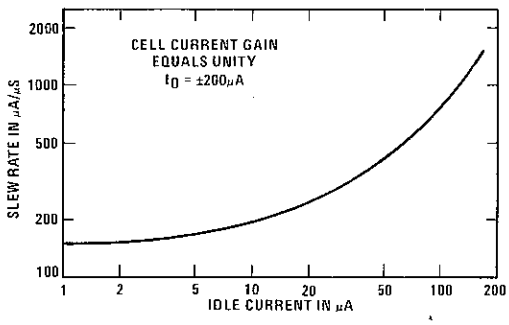




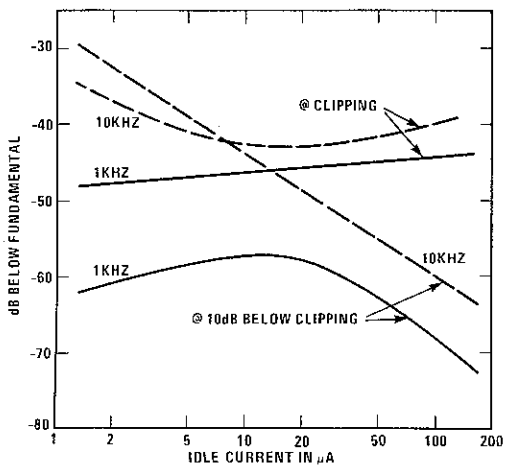
CONTROL FEEDTHROUGH



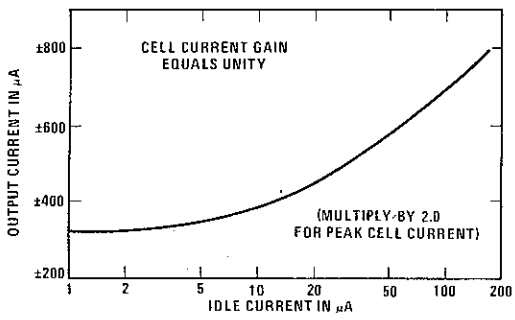
EVEN HARMONIC DISTORTION



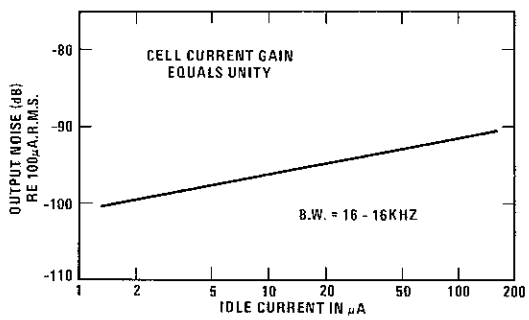
OUTPUT CURRENT SLEW RATE



ODD HARMONIC DISTORTION



PEAK OUTPUT CURRENT BEFORE CLIPPING



NOISE OUTPUT

FIGURE 1: VCA PERFORMANCE V.S. IDLE CURRENT

Selection of Component Values

Selection of the input and output resistor values requires consideration of the preferred and maximum operating current levels of the device as well as the available input voltages and desired output voltage. In general, the input signal current should be made as large as possible to obtain the best signal to noise ratio. However, for either peak inputs currents or peak output currents greater than several hundred microamperes, distortion begins to increase significantly, until the total cell current (input peak current plus output peak current) exceeds the maximum value specified in the specifications for I_{CP}. At this point, clipping occurs, resulting in severe distortion.

For optimum noise performance, it is recommended that the input resistor, R_I, be selected so that the maximum *peak* input signal voltage causes ½ the peak cell current to flow in the input:

$$R_I = V_{IN\ MAX}/½\ I_{CP}$$

Note that the input could handle up to 6dB more current, but the cell current gain would have to be reduced so significantly to prevent clipping, that the signal to noise ratio would actually be degraded. (Output noise increases roughly by the square root of an increase in cell current gain). If more than one signal is being summed in the input, then the total of all peak input currents should be no greater than ½ I_{CP}. Next, the output resistor, R_F, is selected so that the desired maximum for the peak output voltage before clipping is produced with the maximum input signal. Thus,

$$R_F = V_{O\ MAX}/½\ I_{CP}$$

Note that the cell current gain for these conditions is unity, but the voltage gain for the circuit is R_F/R_I and may be greater or less than unity. Note also that the current gain may be made greater than unity for inputs less than $V_{IN\ MAX}$.

Although R_I and R_F have been selected using maximum input and output conditions, the device should nominally operate at least 6 to 20 dB below these maximum levels (corresponding to 100μA or less input and output currents) for best distortion performance.

With the values of R_I and R_F selected, the maximum linear control current, I_{CL}, and most negative exponential control voltage, V_{CE} (V_G in the case of the 3335), are selected to give the maximum desired voltage gain in accordance to the following equations:

$$A_{V\ 3330} = \frac{R_F}{R_I} \cdot \frac{I_{CL}}{I_{REF}} \cdot e^{-V_{CE}/V_T}$$

or

$$A_{V\ 3335} = \frac{R_F}{R_I} \cdot e^{-V_G/V_T}$$

The maximum gain is only limited by either the total cell current exceeding I_{CP}, or excessive noise and DC output shift with cell current gains much greater than unity (>+40dB).

For greatest linear scale accuracy, the maximum value of I_{CL} should be restricted to 100μA or less, although currents up to 300μA can be used with increasing error. For best distortion performance, the reference current, I_{REF}, should also be set between 50μA and 200μA; it may be generated simply with a resistor to V_{CC}. The linear control input resistor, R_{CL}, is thus selected so that the maximum available linear control voltage produces the desired maximum value for I_{CL}.

Finally, the selected value of I_{REF} together with $I_{CL\ MAX}$ determines the most negative value of V_{CE} required to generate the maximum voltage gain. If the exponential input is not used, then it may be grounded (V_{CE} = 0), and only the values of $I_{CL\ MAX}$ and I_{REF} juggled to obtain the maximum gain factor.

Selection of the Quiescent Operating Current

A unique feature of the device is that the quiescent standby, or idle, current of the signal-carrying transistors can be set anywhere between one and several hundred microamperes, thus effectively allowing the user to set the operation of the gain cells anywhere between Class B and Class A. Since the quiescent operating point affects all VCA characteristics, improving some while worsening others, the idle current is selected to optimize those parameters important to the particular application.

As shown in the graphs of Figure 1, increasing the idle current decreases distortion, improves slew rate, and increases available output current, but all at the expense of increased noise and greater control voltage feedthrough. Thus, if the application is to control the level of low frequency control signals where control voltage rejection is critical, then the VCA is best operated Class B. For the processing of audio signals, however, the VCA should be operated Class AB to Class A, with the best compromise between distortion, noise and bandwidth.

The quiescent idle current is set the same for both VCAs by placing a resistor between the idle adjust pin (pin 8 on the 3330, pin 6 on the 3335) and the I_{EE} pin (pin 5). Figure 2 shows the idle current versus the value of this resistor. With

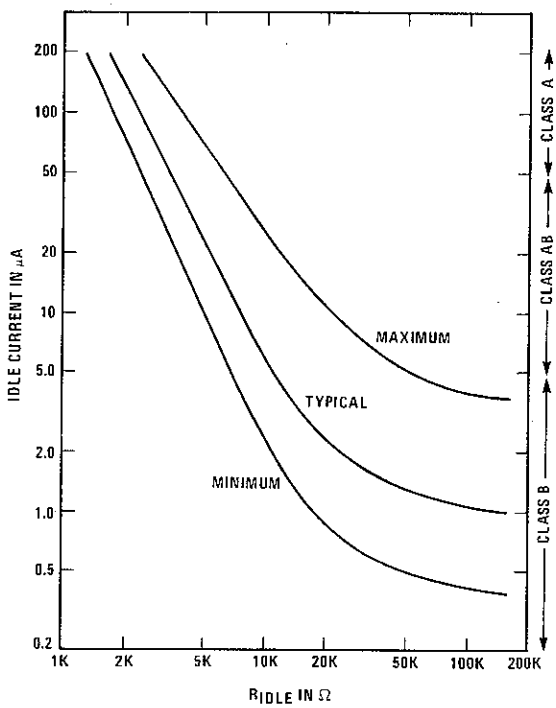


FIGURE 2: IDLE CURRENT V.S. IDLE ADJUST RESISTOR

no resistor ($R_{IDLE} = \infty$) the idle current is typically at 1μA and the VCAs will operate Class B.

As can be seen from Figure 2, the idle current may vary significantly from device to device for any given value of R_{IDLE}, due to the ±25% tolerance of the internal resistors. In most cases, this idle current tolerance is acceptable because the VCA parameters will vary to a much lesser extent. However, the idle current may be set more precisely by measuring the idle current and adjusting the value of R_{IDLE} with a trim pot until the desired value is obtained. The idle current is measured by measuring the output current with no signal input and at a current gain of unity while putting roughly -0.5 to -1.5 volt on the distortion trim pin (pins 3 and 17 on the 3330, pins 3 and 13 on the 3335).

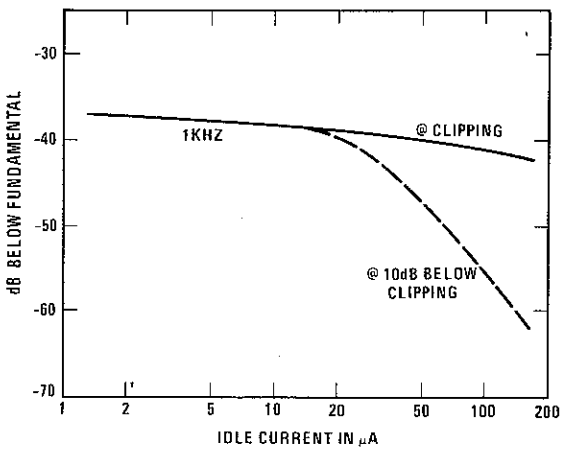


FIGURE 3: SECOND HARMONIC DISTORTION, UNTRIMMED

Trimming of the Second Harmonic Distortion

When operating the VCAs less than Class A, internal transistor mismatches will cause the gain during the positive portion of the input signal to differ from that during the negative portion, thus introducing even harmonic distortion (predominantly second). In Figure 3 is shown a graph of typical untrimmed second harmonic distortion (distortion trim pins connected to ground) versus the idle current. This distortion may be acceptable in some applications, but will have to be trimmed out in others. Trimming is accomplished by adjusting the voltage on the distortion trim pins (pins 3 and 17 on the 3330, pins 3 and 13 on the 3335) somewhere between ±10mV, as shown in Figure 4.

The even harmonic distortion may be trimmed to near minimum with the following simple procedure: The signal input is alternately switched between ground, a positive voltage source (such as a battery) and a negative voltage source of the *exact* same magnitude (best accomplished by simply reversing the leads to the positive voltage source). The value of the voltage source is selected to be equal to the peak signal level at which it is desired to trim the distortion. The output voltage is measured to four digits with a DVM for each of the three input conditions, and the trim adjusted so that the output voltage change is the same going from the grounded to positive input as it is going from the grounded to negative input.

Although the second harmonic may be trimmed out to better than 80dB at almost any gain setting and input signal level, it is best to perform the trimming at a current gain of zero and input signal level around 10dB below the clipping point. This procedure will yield, in general, the best distortion performance at all input levels and gain settings except at the very highest (last 10 to 6dB before clipping at the output). And since in the case of the music and speech signals, the last 15 to 20dB should be reserved for headroom, this result is acceptable.

As most of the odd order harmonic distortion is due to crossover distortion, there is no way to trim it out; it may be reduced only by increasing the idle current.

Optimizing the Bandwidth

As can be seen from the Block Diagrams, the log converters are stabilized with a series 1K resistor and .01μF capacitor compensation network from the linear control input to ground, while each of the gain cells may be compensated with a .005μF capacitor from the compensation pins (pins 9 and 11 on the 3330, pins 7 and 9 on the 3335) to ground. This gain cell compensation is good for low frequency control applications, but may result in inadequate large signal bandwidth for quality audio applications.

Figure 5 shows an improved compensation technique for

greater bandwidths and slew rate: By placing a series 1K resistor and .01μF capacitor network from the signal input to ground, the .005μF compensation capacitors may be reduced to 150 pF, resulting in the bandwidths and slew rate shown in Figure 1.

Control Inputs

As was discussed earlier, the linear control input resistor, R_{CL}, should be selected so that the linear control current reaches a maximum of 50μA to 200μA. This level is low enough so as not to cause significant control scale non-linearity, but high enough to swamp out the effects of the internal input bias current. Since the actual current controlling the linear gain is the input control current minus this bias current, the input control voltage at which the gain becomes zero is given by:

$$V_{CLO} = I_B R_{CL} + V_{OS}$$

This cut-off point may be increased by injecting a small constant negative current into the control input, or decreased by injecting a small positive current into the input.

As the scale sensitivity of the exponential control inputs on both the 3330 and 3335 are 18mV/-6dB, an attenuation network will in most cases by required. An increasing positive control voltage decreases the gain.

The basic gain cell is fully temperature compensated. The only first order temperature effect is the exponential control factor tempco ($1/V_T$). This effect may be substantially reduced by using a +3300ppm tempco resistor (Tel Labs Q81) for R_{CE1}, shown in the Block Diagrams. If only the linear control input is to be used, then the exponential input is grounded and no temperature compensation is necessary.

To use the 3330 for exponential gain control only, the entire log converter may be bypassed, reducing the number of external components and potential errors introduced by the log converter. This is accomplished by simply leaving the linear and exponential control inputs open, and applying the exponential control voltage directly to the I_{REF} pin (which is also the direct input, V_G, to the gain cell) as shown in Figure 6. The scale sensitivity is the same as that of the exponential input to the log converter, and therefore requires the same considerations as discussed above.

For best distortion performance, it is recommended that the impedance at both the distortion adjust inputs and direct control inputs (3330 or 3335) be kept below several hundred ohms.

Trimming of the Control Voltage Feedthrough

The shift in the quiescent DC output voltage as the gain is changed is due to several factors. One cause is the internal bias current at the signal current input, being only of concern at idle currents less than 10μA. The other cause is the same potential imbalance between the two signal processing halves which also is responsible for even order harmonic distortion.

Thus, there are two methods for minimizing the control voltage feedthrough: One is to inject an adjustable DC current into the signal current input pin, as shown in Figure 7. The range of this current should be roughly equal to plus and minus the idle current. (For idle currents less than 5μA, it is not necessary that this current be adjustable to negative values.) The best technique for adjusting this trim for maximum control voltage rejection is to simply set the gain to maximum and adjust the pot for zero DC quiescent output current. (The DC output current at zero gain is always zero.)

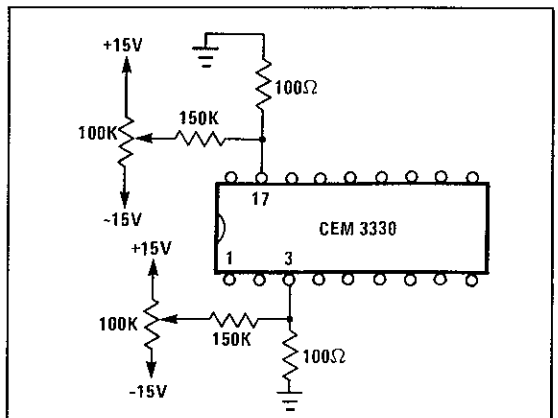


FIGURE 4: DISTORTION TRIM

The other method for minimizing control voltage feedthrough is to balance the two circuit halves by adjusting the second harmonic distortion trim discussed above. This method, although usually reducing the distortion below that of the untrimmed value, will not adjust

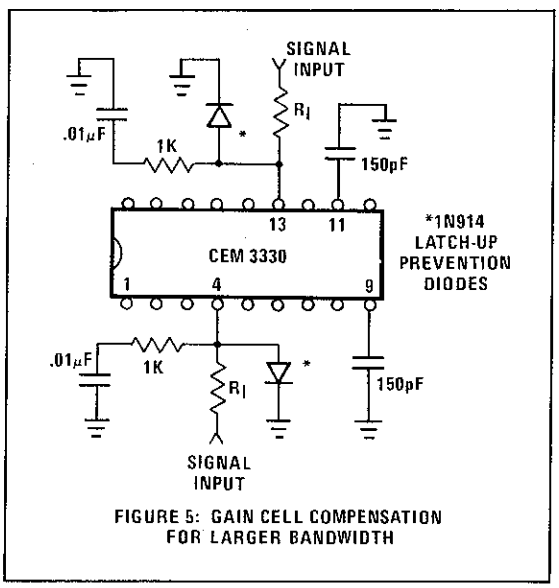


FIGURE 5: GAIN CELL COMPENSATION FOR LARGER BANDWIDTH

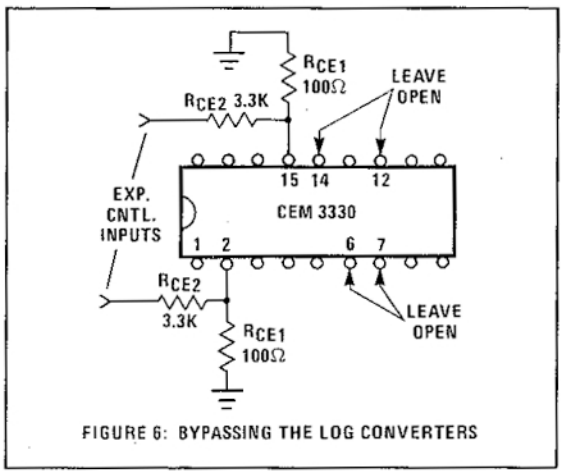


FIGURE 6: BYPASSING THE LOG CONVERTERS

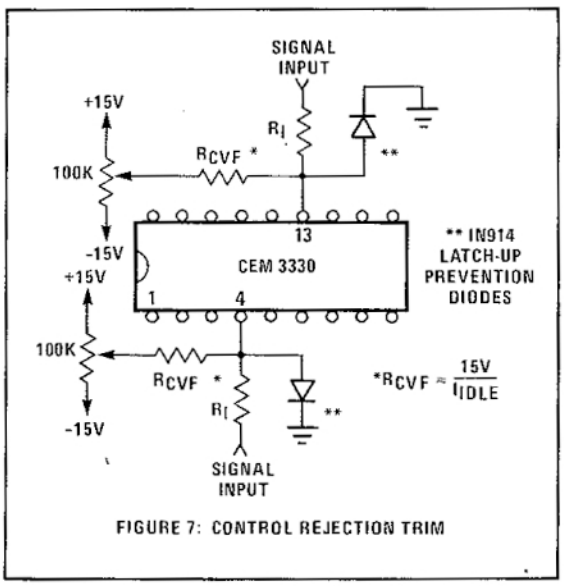


FIGURE 7: CONTROL REJECTION TRIM

the distortion to its potential minimum. Conversely, minimizing the distortion with this trim does not necessarily minimize the control voltage feedthrough. (At high values of idle current, it may even increase it.) The technique for using this trim to maximize the control rejection is the same as before: the pot is adjusted for zero DC current output at maximum gain.

At idle currents less than 10μA, it is recommended that the input trim of Figure 7 be used rather than the distortion trim, as the distortion trim tends to increase the distortion above the untrimmed value when feedthrough has been minimized. At higher idle currents, however, it is recommended that the distortion trim be used to minimize feedthrough, since it will also tend to reduce distortion below the untrimmed value. In fact, this is a good method for improving (but not necessarily optimizing) both distortion and control rejection with only a single trim. For absolute best control voltage rejection, where the distortion is not as critical as control rejection, it is recommended that both the input current adjust of Figure 7 and the distortion trim be simultaneously adjusted to produce minimum feedthrough.

Shown in Figure 1 are typical values of control feedthrough versus idle current for untrimmed, trimmed with the input current adjust only, trimmed with the distortion adjust only, and trimmed with the input adjust after the distortion has been trimmed for minimum.

For best overall VCA performance at any idle current, where both distortion and feedthrough are important, it is recommended that the second harmonic distortion is first trimmed for minimum, and then the control voltage feedthrough trimmed with the technique of Figure 7.

Layout Considerations

In the usual case where the outputs connect to the summing inputs of op amps, these output traces should be kept short to prevent their high impedance from picking up extraneous signals.

Since capacitance greater than 50pF at the idle adjust pin may cause high frequency oscillation, care should be exercised in the layout to minimize stray capacitance at this pin.

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