ESP-PSRAM64 & ESP-PSRAM64H Datasheet

Version 1.0

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About This Document

This document introduces the specifications of ESP-PSRAM64 and ESP-PSRAM64H.

Release Notes

Date	Version	Release notes
2018.06	V1.0	First release.

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1. Introduction

ESP-PSRAM64 and ESP-PSRAM64H are 64 Mbit serial pseudo SRAM devices that are organized in 8Mx8 bits. They are fabricated using the high-performance and high-reliability CMOS technology. ESP-PSRAM64 operates at 1.8V and can offer high data bandwidth at 144 MHz clock rate, while ESP-PSRAM64H operates at 3.3V and can support up to 133 MHz clock rate. Note, however, that burst operations which cross page boundaries have a lower max input clock frequency at 84 MHz.

Both of the PSRAM devices can be accessed via the Serial Peripheral Interface (SPI). Additionally, a Quad Peripheral Interface (QPI) is supported if the application needs faster data rates. The devices also support unlimited reads and writes to the memory array.

Note that the information in this data sheet is applicable to both PSRAM devices. Any differences between them will be clearly specified in the course of this document.

Table 1-1. Ordering Information of ESP-PSRAM64 and ESP-PSRAM64H

Part number	Product density	Package type	Maximum Clock rate	Operating temperature	Product carrier	Green code	Operating voltage	Read/Write operation mode	SPI mode
ESP-PSRAM64	64 Mbit	SOP8-150 mil	144 MHz	–40°C ~ 85°C	Tape & Reel	RoHS Compliant Package and Green/Reach Package	1.8V	1 KB Pages	Standard/ Quad SPI
ESP-PSRAM64H			133 MHz				3.3V		

2. Pin Description

Figure 2-1 shows the pin layout of ESP-PSRAM64 and ESP-PSRAM64H.

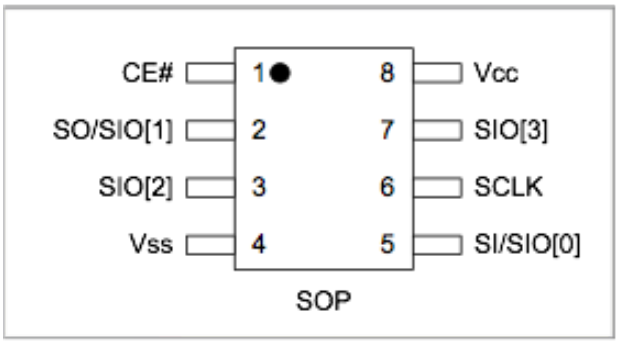


Figure 2-1. Pin Layout of ESP-PSRAM64 and ESP-PSRAM64H

Table 2-1. Signals Table

Pin	Signal Type	SPI Mode Function	QPI Mode Function
V_{CC}	Power	Core supply, 1.8V for ESP-PSRAM64, 3.3V for ESP-PSRAM64H.	
Vss	Ground	Core supply ground	
CE#	Input	Chip select signal, active low. When CE#=1, the chip is in standby state.	
CLK	Input	Clock signal	
SI/SIO[0]	I/O	Serial input	I/O[0]
SO/SIO[1]	I/O	Serial output	I/O[1]
SIO[2]	I/O	-	I/O[2]
SIO[3]	I/O	-	I/O[3]

3. Power-up Initialization

SPI/QPI products include an on-chip voltage sensor which activates the self-initialization process. When Vcc reaches a stable level at or above the minimum Vcc, the device will need 150 µs and a user-issued reset operation (see Section 8) to complete its self-initialization process. From the beginning of power ramp to the end of the 150-µs period, CLK should remain low, CE# should remain high (to track Vcc within 200 mV) and SI/SO/SIO[3:0] should remain low.

After the 150-µs period, the device will be ready for normal operation.

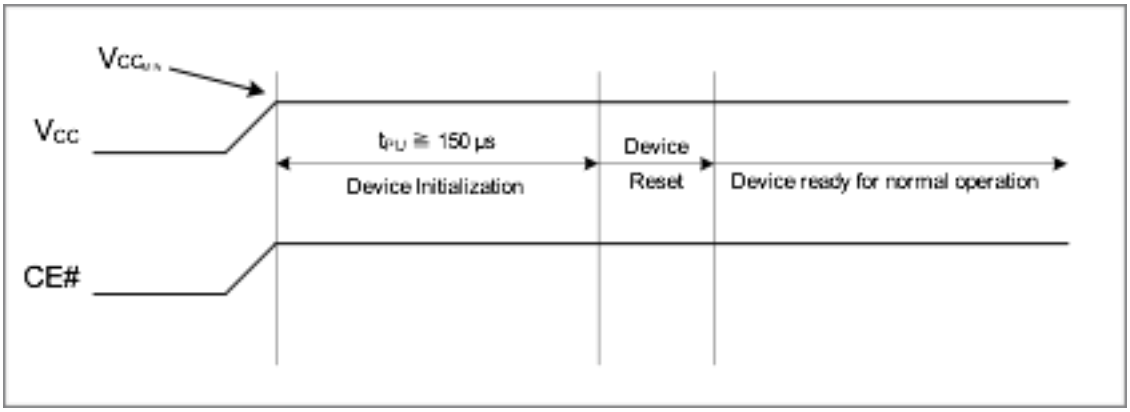


Figure 3-1. Power-up Initialization Timing

4. Wrap Boundary Toggle Operation

The Wrap Boundary Toggle Operation allows the device to switch between the linear burst mode (CA[9:0]) and the 32-byte wrap mode (CA[4:0]). The default setting is Linear Burst.

A Linear Burst allows the device to cross page boundaries . Page boundary crossing is invisible to the memory controller and limited to the max CLK frequency of 84 MHz. Table 4-1 shows an example of the byte sequence in both modes.

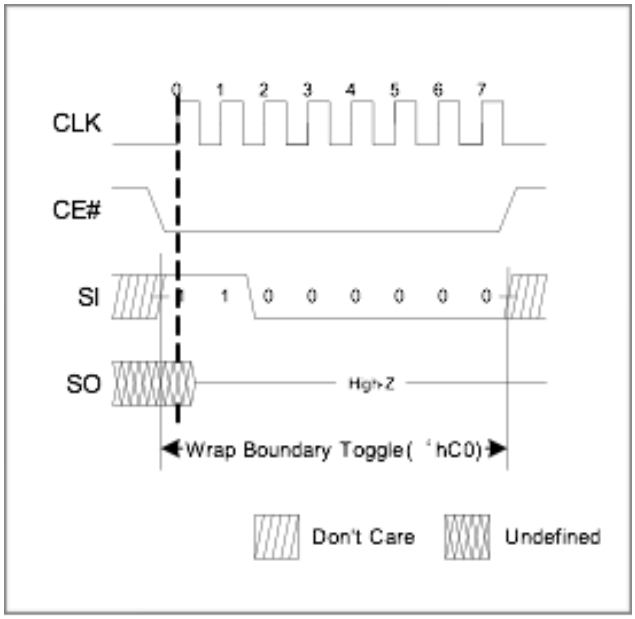


Figure 4-1. SPI Wrap Boundary Toggle 'hC0

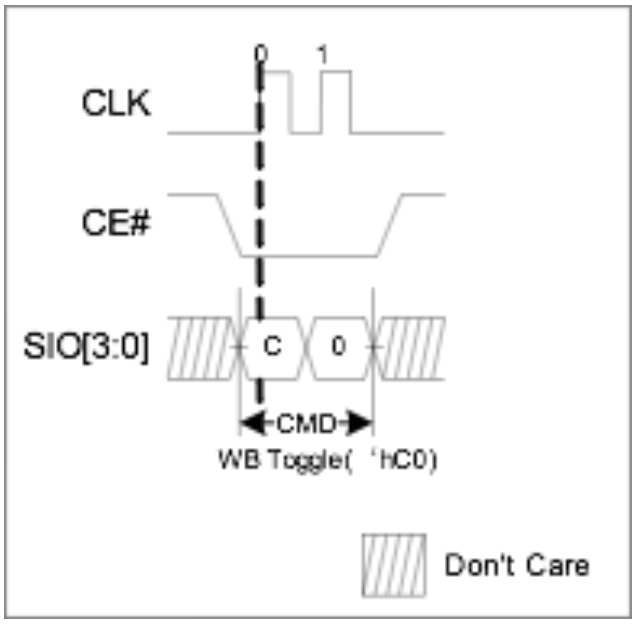


Figure 4-2. QPI Wrap Boundary Toggle 'hC0

Table 4-1. Burst Type/Length

Burst Type/Length	Starting Address	Byte Sequence
Linear Burst	4	[4,5,6,...1023,1024,1025,1026,...]
Wrap 32	4	[4,5,6,...31,0,1,2,...]

5. Interface Description

5.1. Address Space

The SPI/QPI PSRAM device is byte-addressable. The address of the 64 Mbit device is A[22:0].

5.2. Page Size

The page size is 1K (CA[9:0]). The default setting is a linear burst that crosses page boundaries in a continuous manner. Note, however, that the maximum input clock frequency for burst operations which cross page boundaries is 84 MHz. Optionally, the device can also be set to the 32-byte wrap (CA[4:0]) mode, using the Wrap Boundary Toggle command, but the device cannot cross page boundaries in this case.

5.3. Power-on Status

The device powers up in SPI Mode. It is required to have CE# high before beginning any operations.

5.4. Truth Table

The device recognizes the following commands specified by the various input methods.

Command	Code	SPI Mode (QE=0)					QPI Mode (QE=1)				
		Cmd	Addr	Wait Cycle	DIO	MAX Freq.	Cmd	Addr	Wait Cycle	DIO	MAX Freq.
Read	'h03	S*note1	S	0	S	33	N/A				
Fast Read	'h0B	S	S	8	S	133/144	N/A				
Fast Read Quad	'hEB	S	Q	6	Q*note 1	133/144	Q	Q	6	Q	133/144*note2
Write	'h02	S	S	0	S	133/144	Q	Q	0	Q	133/144*note2
Quad Write	'h38	S	Q	0	Q	133/144	Same as 'h02				
Enter Quad Mode	'h35	S	-	-	-	133/144	N/A				
Exit Quad Mode	'hF5	N/A					Q	-	-	-	133/144
Reset Enable	'h66	S	-	-	-	133/144	Q	-	-	-	133/144
Reset	'h99	S	-	-	-	133/144	Q	-	-	-	133/144

Command	Code	SPI Mode (QE=0)					QPI Mode (QE=1)				
		Cmd	Addr	Wait Cycle	DIO	MAX Freq.	Cmd	Addr	Wait Cycle	DIO	MAX Freq.
Set Burst Length	'hC0	S	-	-	-	133/144	Q	-	-	-	133/144
Read ID	'h9F	S	S	0	S	133/144	N/A				

📖 ***Notes*:***

1. S=Serial I/O; Q=Quad I/O.
2. 133/144 MHz max without crossing page boundaries, and 84 MHz max when burst commands cross page boundaries.
3. For ESP-PSRAM64, the maximum frequency is 144 MHz, while for ESP-PSRAM64H it is 133 MHz.

5.5. Command Termination

In order to terminate ongoing read and write operations and put the chip into standby mode, CE# must be pulled high immediately after all read/write operations. Not doing so will block internal refresh operations and cause memory failure.

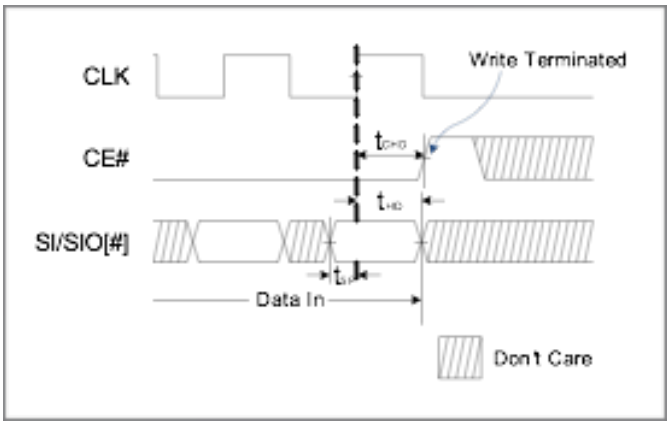


Figure 5-1. Write Command Termination

For a memory controller to correctly latch the last piece of data prior to read-termination, it is recommended that a longer CE# hold time ($t_{CHD} > t_{ACLK} + t_{CLK}$) be provided, allowing for a sufficient data window.

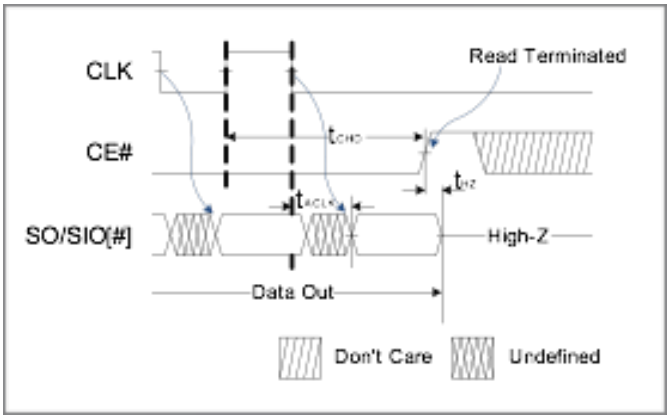


Figure 5-2. Read Command Termination

6. SPI Mode Operations

The device enters SPI mode on power-up by default, but this can also be switched into QPI mode.

6.1. SPI Read Operations

For all reads, data will be available after t_{ACLK} following the falling edge of CLK. SPI reads can be done in three ways:

- 'h03: Serial CMD, Serial I/O, low frequency, configurable in linear or burst 32-byte wrap mode.
- 'h0B: Serial CMD, Serial I/O, high frequency, configurable in 32/1K-byte burst wrap mode.
- 'hEB: Serial CMD, Quad I/O, high frequency, configurable in 32/1K-byte burst wrap mode.

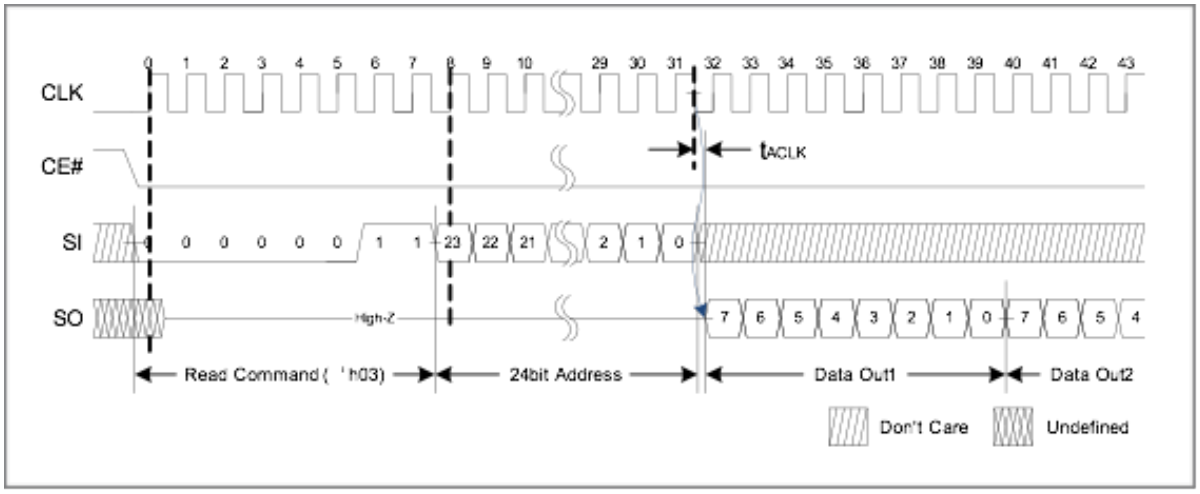


Figure 6-1. SPI Read 'h03 (Max frequency: 33 MHz)

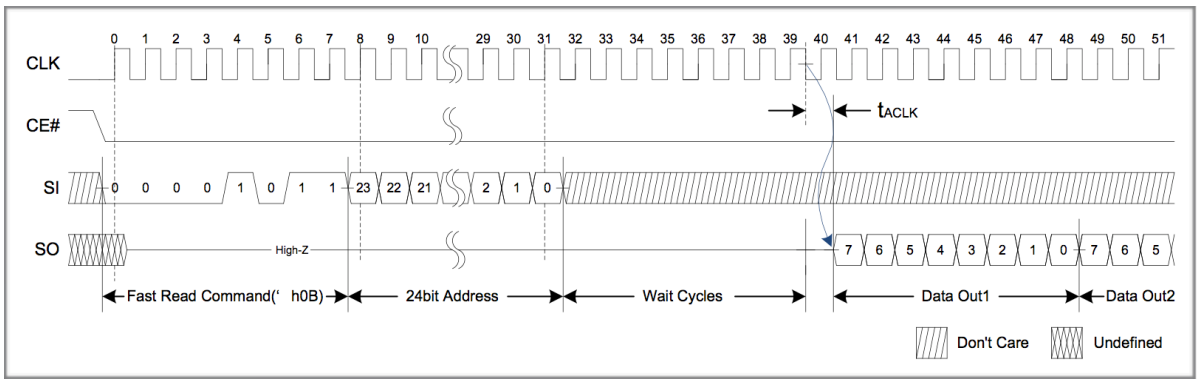


Figure 6-2. SPI Fast Read 'h0B (Max frequency: 104 MHz)

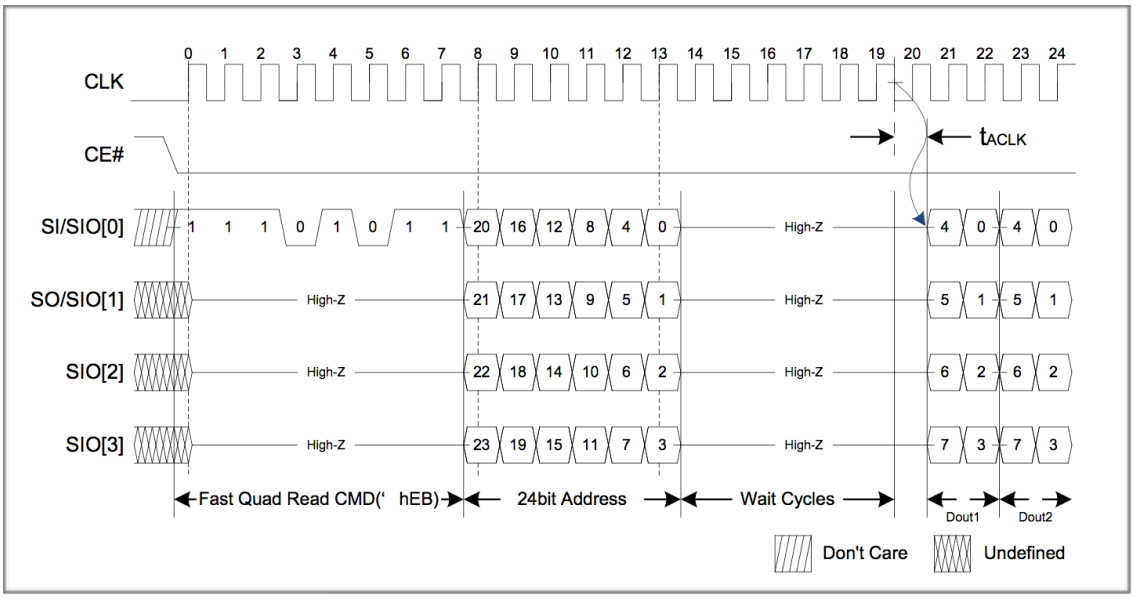


Figure 6-3. SPI Fast Quad Read ‘hEB
(Max frequency: 144 MHz for ESP-PSRAM64, 133 MHz for ESP-PSRAM64H)

6.2. SPI Write Operations

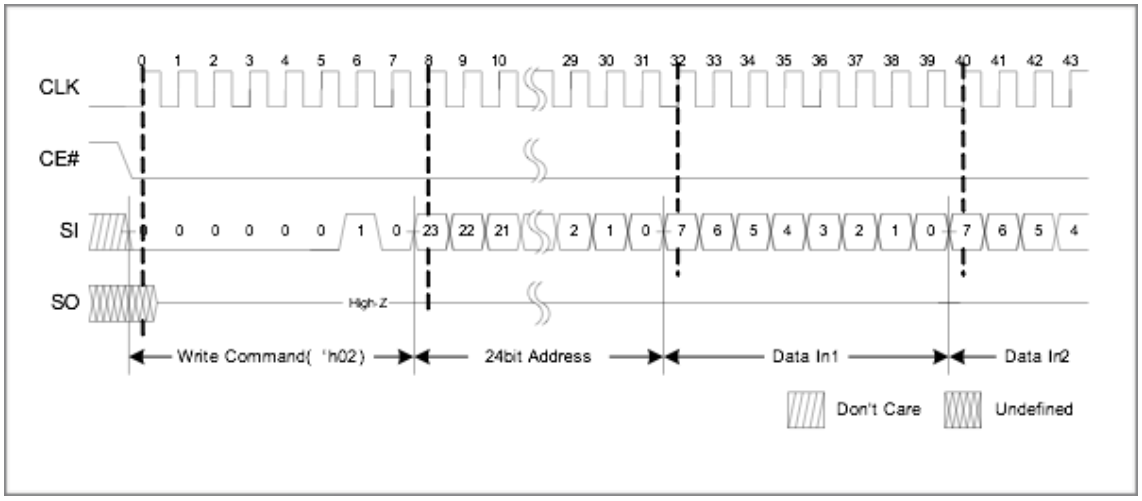


Figure 6-4. SPI Write ‘h02

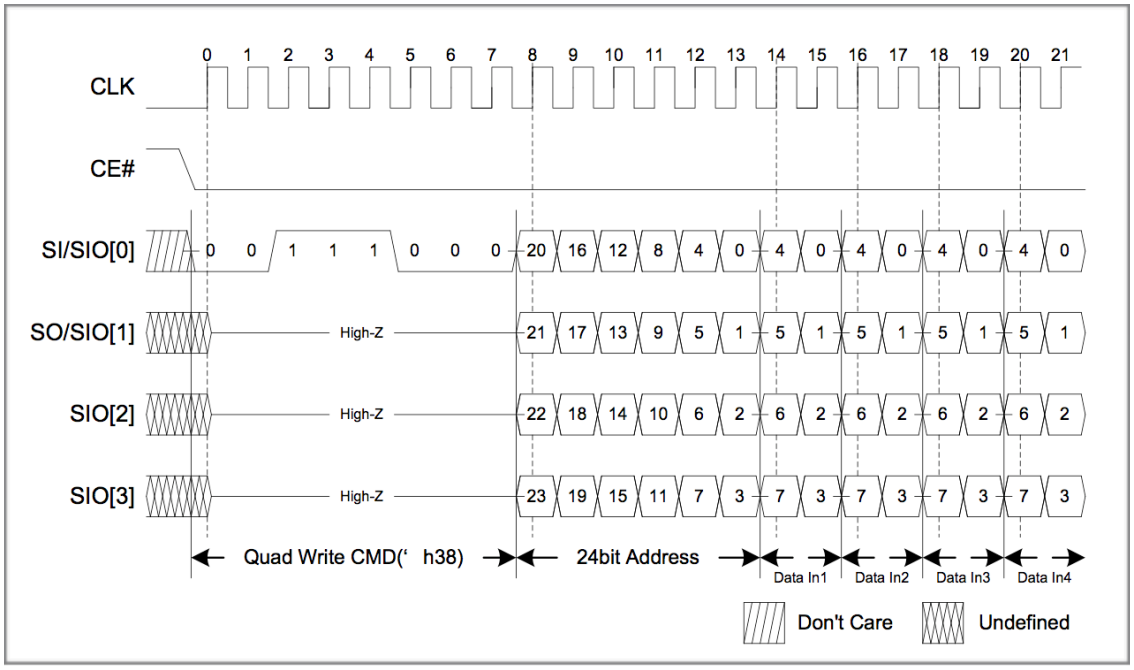


Figure 6-5. SPI Quad Write 'h38

6.3. SPI Quad Mode Enable Operation

This command switches the device's mode into quad I/O.

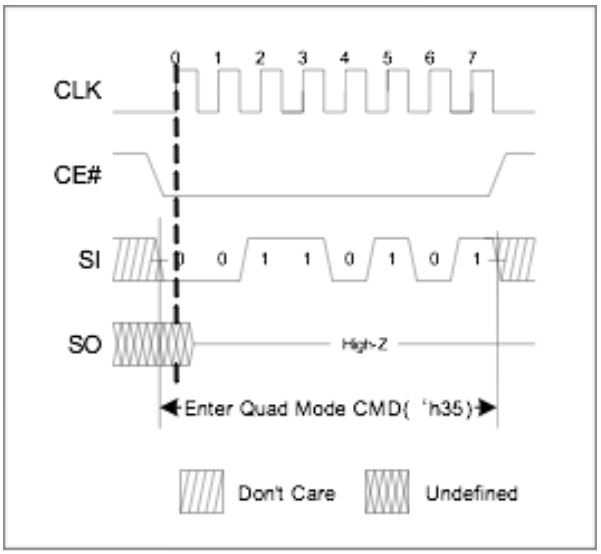


Figure 6-6. Quad Mode Enable 'h35 (available only in SPI mode)

6.4. SPI Read ID Operation

This command is similar to Fast Read, but there are no wait cycles and the device outputs EID value instead of data.

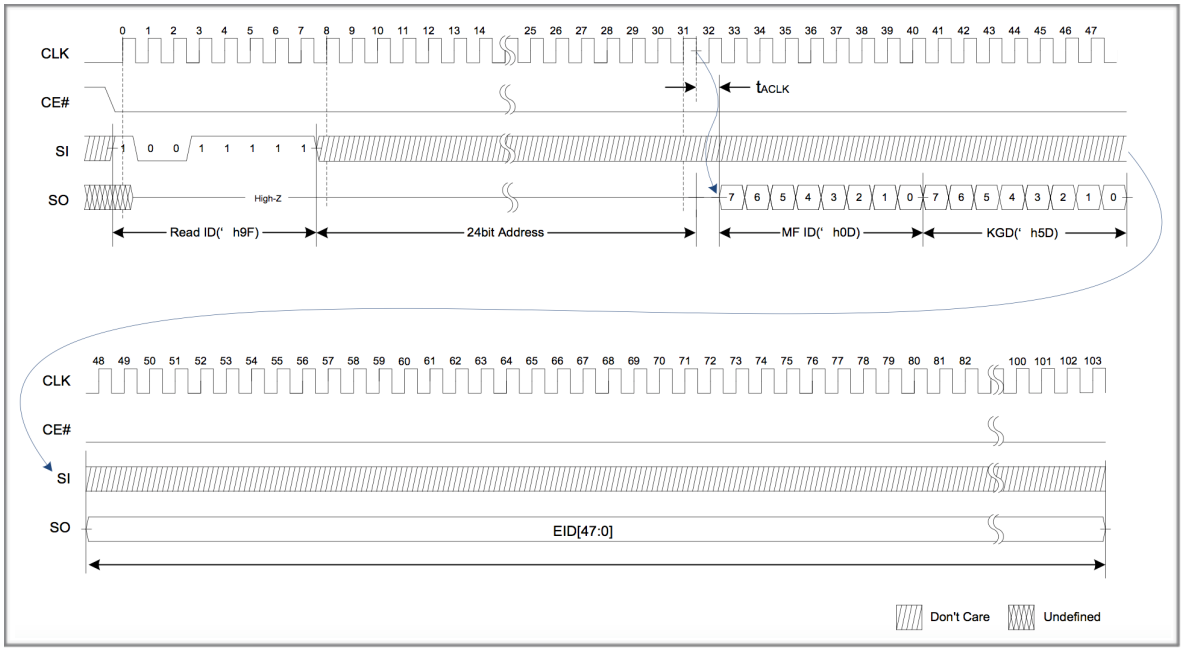


Figure 6-7. SPI Read ID 'h9F (Available Only in SPI Mode)

Table 6-1. Known Good Die (KGD)

KDG[7:0]	Known Good Die
'b0101_0101	Fail
'b0101_1101	Pass

> 📖 ***Note:***
>
> The default is "FAIL", which is changed to PASS only after all tests are passed.

7. QPI Mode Operations

7.1. QPI Read Operations

For all reads, data will be available after t_{ACLK} following the falling edge of CLK.

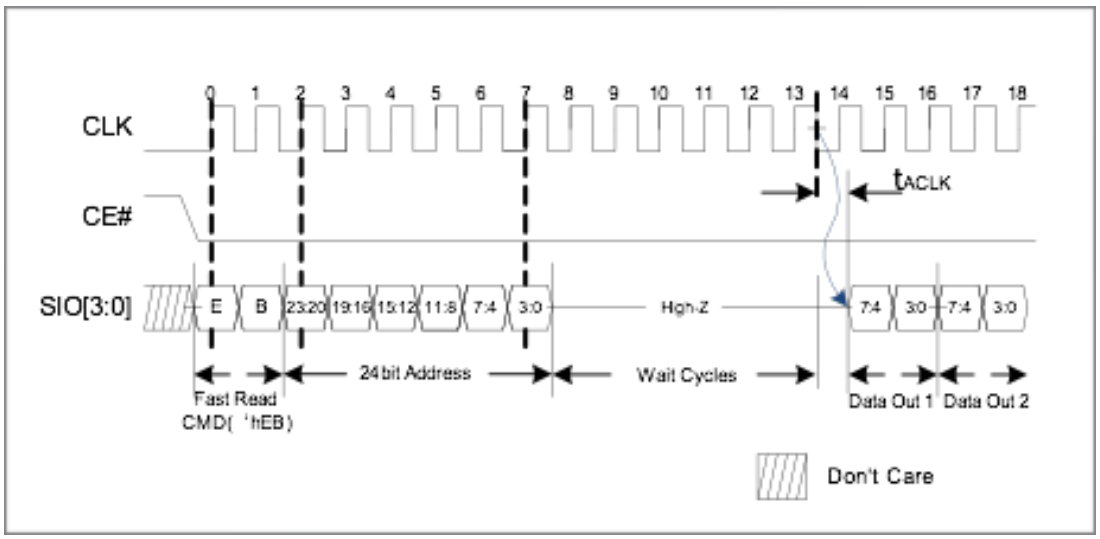


Figure 7-1. QPI Fast Read 'hEB
(Max frequency: 144 MHz for ESP-PSRAM64, 133 MHz for ESP-PSRAM64H)

7.2. QPI Write Operations

QPI write command can be input as 'h02 or 'h38.

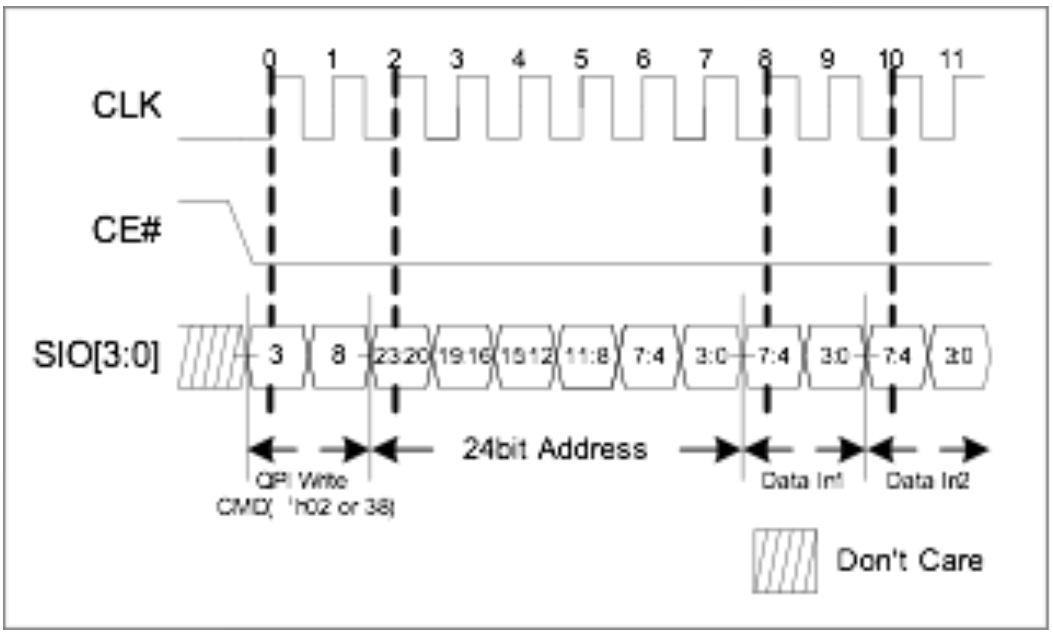


Figure 7-2. QPI Write 'h02 or 'h38

7.3. QPI Quad Mode Exit Operation

This command will switch the device's mode back into serial I/O.

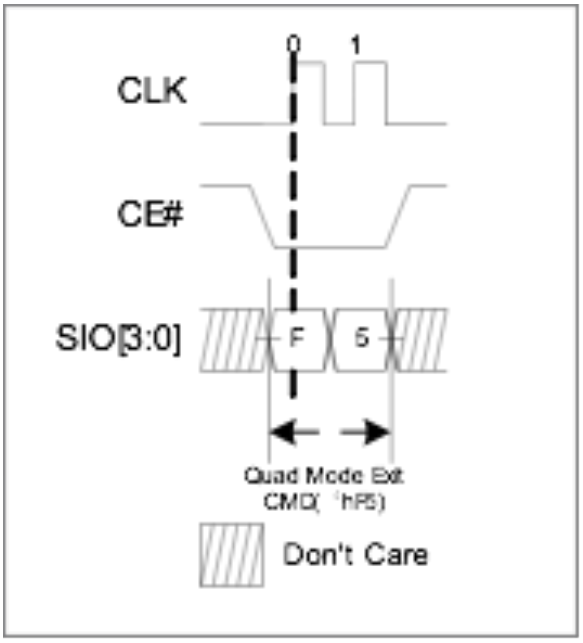


Figure 7-3. Quad Mode Exit 'hF5 (Only Available in QPI Mode)

8. Reset Operation

The reset operation is used as a system (software) reset that puts the device in SPI standby mode, which is also the default mode after power-up. This operation is based on two commands: Reset-Enable (RSTEN) and Reset (RST).

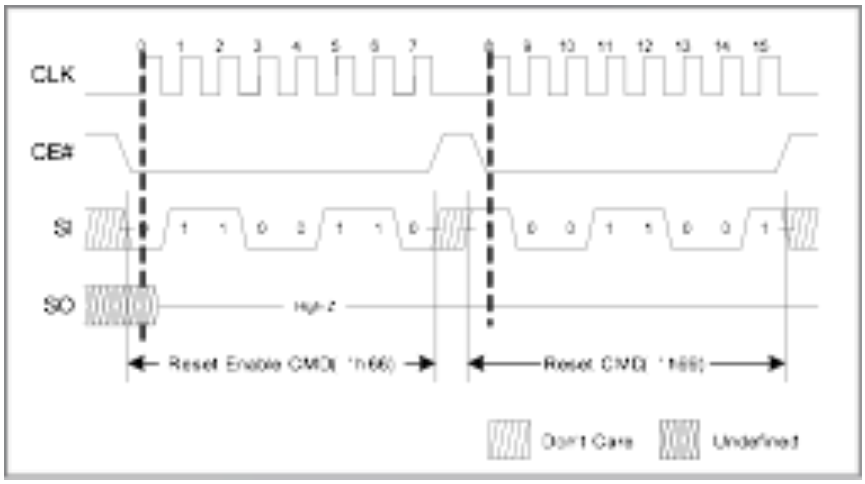


Figure 8-1. SPI Reset

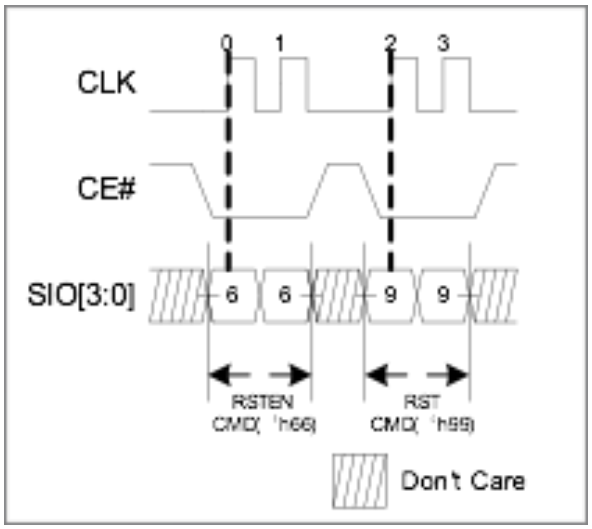


Figure 8-2. QPI Reset

The Reset command has to immediately follow the Reset-Enable command in order for the reset operation to take effect. Any other command after Reset-Enable will prompt the device to exit the Reset-Enable state and abandon the reset operation.

9. Input/Output Timing

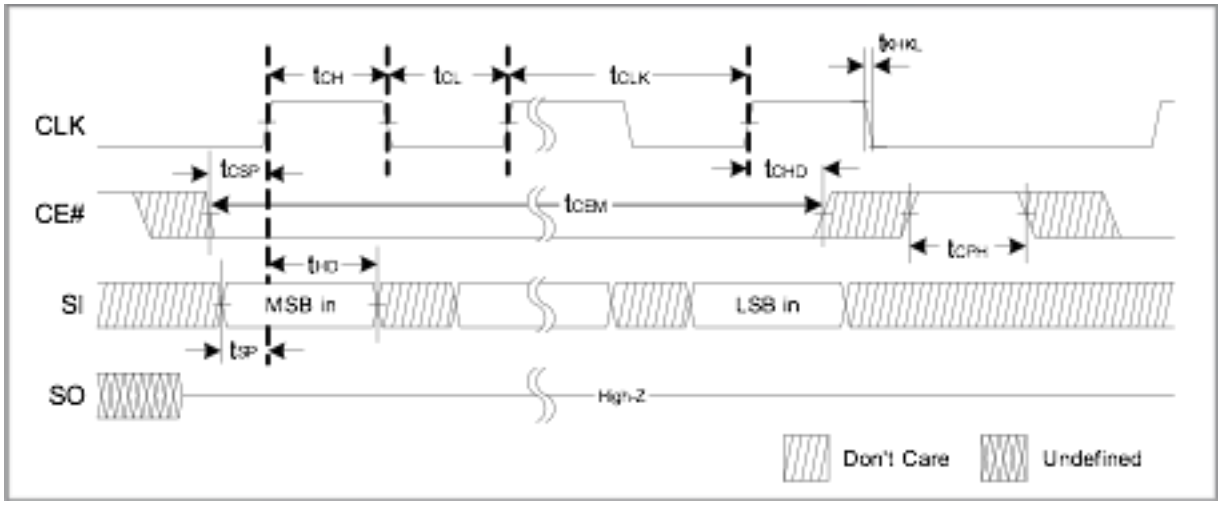


Figure 10-1. Input Timing

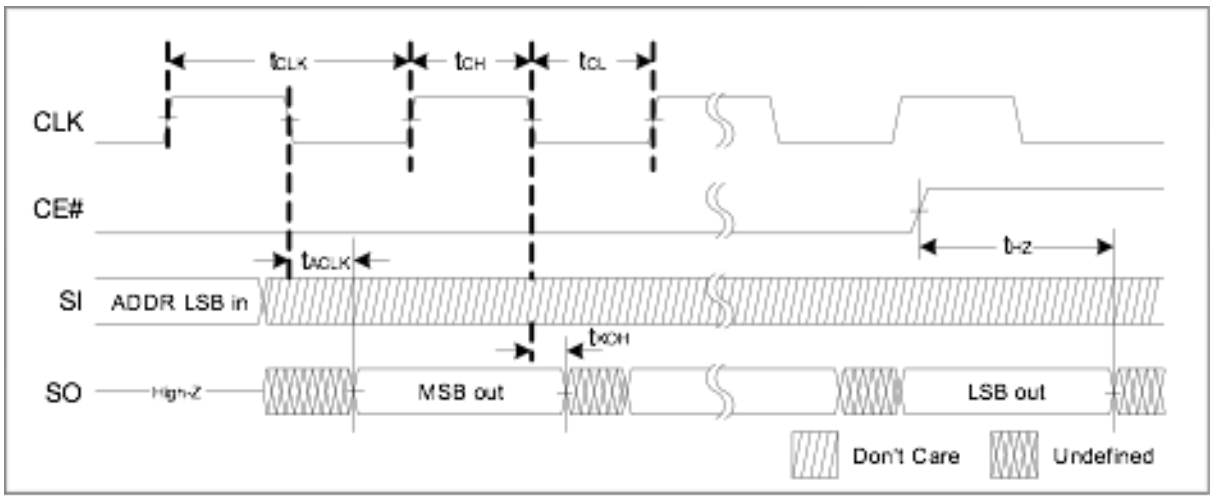


Figure 10-2. Output Timing

10. Electrical Specifications

10.1. Absolute Maximum Ratings

Table 10-1. Absolute Maximum Ratings

Symbol	Parameter	Rating	Unit
VT	Voltage to any pad, except for Vcc, relative to Vss	–0.3 ~ Vcc +0.3	V
V_{CC}	Voltage on Vcc, relative to Vss	ESP-PSRAM64: –0.2 ~ +2.45 ESP-PSRAM64H: –0.2 ~ +4.2	V
T_{STG}	Storage Temperature*	–55 ~ +150	°C

📖 ***Note:***

**Storage temperature refers to the surface temperature of the case at the center of the PSRAM's top side.*

⚠ ***Notice:***

Exposing the device to greater stress than what is listed as absolute maximum ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits specified in this document. Exposure to Absolute Maximum Rating conditions for extended periods may affect the device's reliability.

10.2. Operating Conditions

Table 10-2. Operating Characteristics

Parameter	Min	Max	Unit
Operating Temperature	–40	85	°C

10.3. Pin Capacitance

Table 10-3. Package Pin Capacitance

Symbol	Parameter	Min	Max	Unit	Notes
C_{IN}	Input Pin Capacitance	-	6	pF	V_{IN} = 0V
C_{OUT}	Output Pin Capacitance	-	8	pF	V_{OUT} = 0V

10.4. DC Electrical Characteristics

Table 10-4. DC Characteristics

Symbol	Parameter	Min	Max	Unit
Vcc	Supply voltage	ESP-PSRAM64: 1.62 ESP-PSRAM64H: 2.7	ESP-PSRAM64: 1.98 ESP-PSRAM64H: 3.6	V
V_{IH}	Input high voltage	Vcc – 0.4	Vcc + 0.2	V
V_{IL}	Input low voltage	–0.2	0.4	V
V_{OH}	Output high voltage (I_{OH} = –0.2 mA)	0.8 Vcc	-	V
V_{OL}	Output low voltage (I_{OL} = +0.2 mA)	-	0.2 Vcc	V
I_{LI}	Input leakage current	-	1	µA
I_{LO}	Output leakage current	-	1	µA
I_{CC}	Read/Write	-	ESP-PSRAM64: 25 ESP-PSRAM64H: 40	mA
I_{SB}	Standby current*	-	200	µA

📖 ***Note:***

**Standby current is measured when CLK is at a low DC level.*

10.5. AC Electrical Characteristics

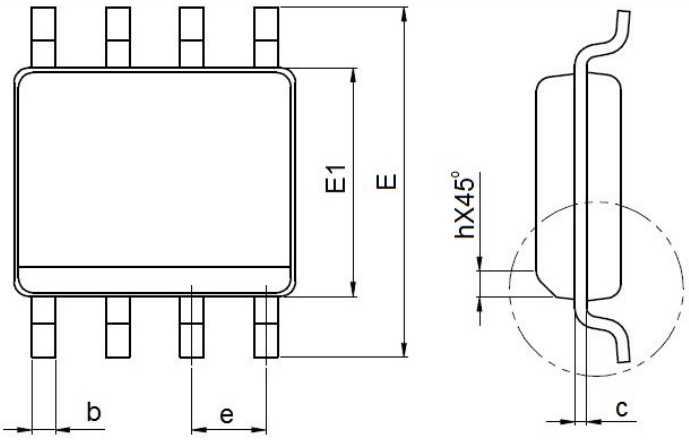
Table 10-5. Read/Write Timing

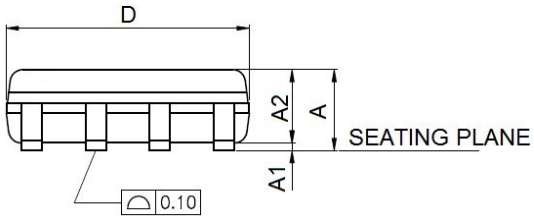
Symbol	Parameter	Min	Max	Unit	Notes
t_{CLK}	CLK period—SPI Read ('h03)	30.3	-	ns	33 MHz
	CLK period—all other operations	7			133/144 MHz*
t_{CH}/t_{CL}	Clock high/low width	0.45	0.55	t_{CLK} (min)	-
t_{KHKL}	Clock rise or fall time	-	1.5	ns	-
t_{CPH}	CE# HIGH between subsequent burst operations	50	-	ns	-
t_{CEM}	CE# low pulse width	-	8	µs	-
t_{CSP}	CE# setup time to CLK rising edge	2.5	-	ns	-
t_{CHD}	CE# hold time from CLK rising edge	20	-		-
t_{SP}	Setup time to active CLK edge	2	-		-
t_{HD}	Hold time from active CLK edge	2	-		-
t_{HZ}	Chip disable to DQ output height-Z	-	6		-
t_{ACLK}	CLK to output delay	2	6		-
t_{KOH}	Data hold time from clock falling edge	1.5	-		-

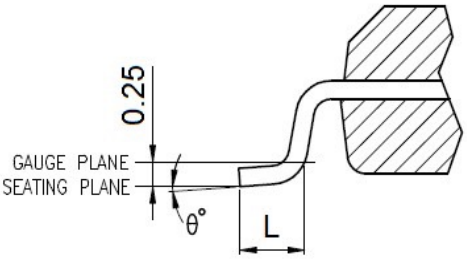
📖 ***Note*:***

1. *Only Linear Burst allows page boundary crossing. Frequency limits are therefore*
   - *133/144 MHz MAX. without crossing page boundaries, and*
   - *84 MHz MAX. when burst commands cross page boundaries.*
2. For ESP-PSRAM64, the maximum frequency is 144 MHz, while for ESP-PSRAM64H, it is 133 MHz.
3. *For operating frequencies > 84 MHz, refer to JEDEC JESD84-B50 for data sampling training.*

11. Product Dimensions







VARIATIONS (ALL DIMENSIONS SHOWN IN MM)

SYMBOLS	STANDARD	
	MIN.	MAX.
A	—	1.75
A1	0.10	0.25
A2	1.25	—
b	0.31	0.51
c	0.10	0.25
D	4.90 BSC	
E	6.00 BSC	
E1	3.90 BSC	
e	1.27 BSC	
L	0.40	1.27
h	0.25	0.50
θ°	0	8

NOTES:

1. JEDEC OUTLINE : MS-012 AA REV.F (STANDARD)
   MS-012 BA REV.F (THERMAL)
2. DIMENSIONS "D" DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH, PROTRUSIONS AND GATE BURRS SHALL NOT EXCEED 0.15mm. PER SIDE.
3. DIMENSIONS "E1" DOES NOT INCLUDE INTER-LEAD FLASH, OR PROTRUSIONS. INTER-LEAD FLASH AND PROTRUSIONS SHALL NOT EXCEED 0.25mm PER SIDE.

A. Appendix: Device Marking Conventions

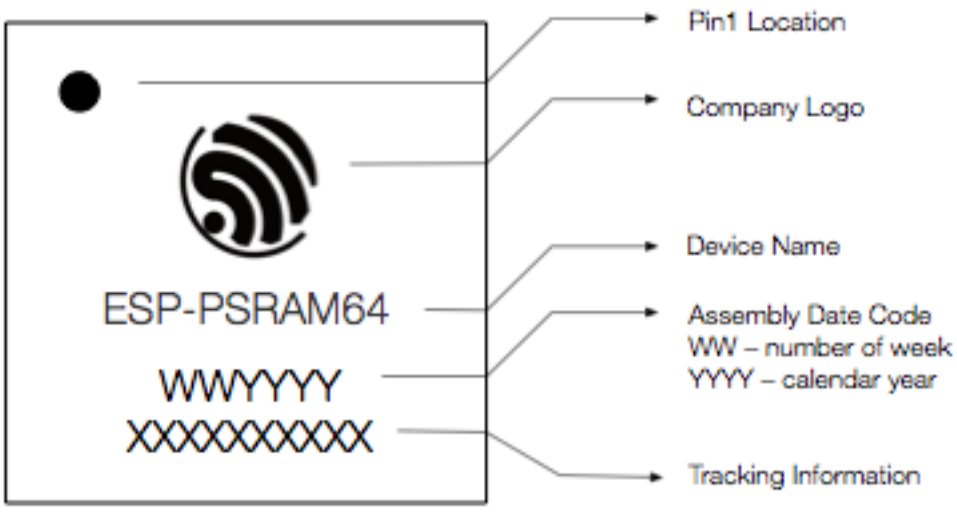


Figure A-1. Device Marking of ESP-PSRAM64

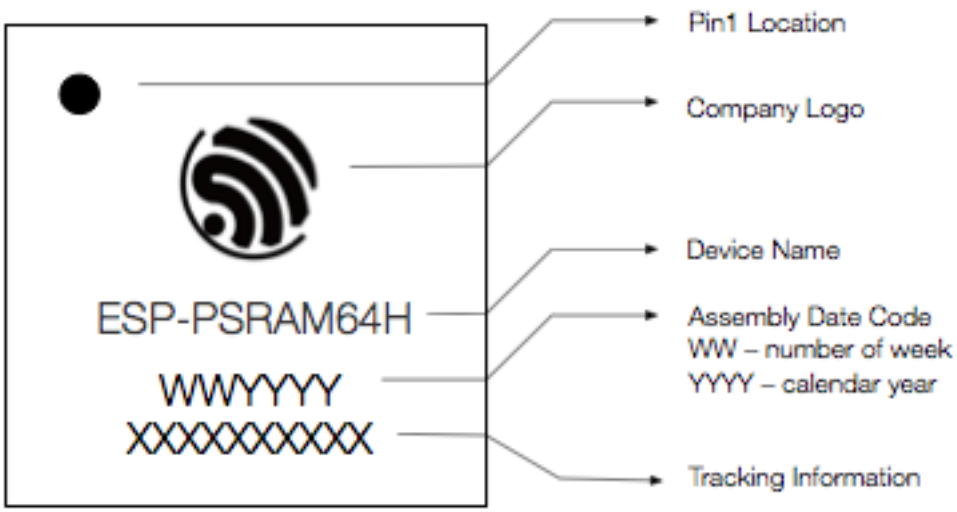


Figure A-2. Device Marking of ESP-PSRAM64H

> 📖 ***Note:***
>
> The content and the number of digits in the tracking Information are subject to change.

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