

## ADC0844/ADC0848 8-Bit $\mu$ P Compatible A/D Converters with Multiplexer Options

Check for Samples: [ADC0844](#), [ADC0848](#)

### FEATURES

- Easy Interface to All Microprocessors
- Operates Ratiometrically or with 5 V<sub>DC</sub> Voltage Reference
- No Zero or Full-Scale Adjust Required
- 4-Channel or 8-Channel Multiplexer with Address Logic
- Internal Clock
- 0V to 5V Input Range with Single 5V Power Supply
- Standard Width 20-Pin or 24-Pin PDIP
- 28 Pin PLCC Package

### KEY SPECIFICATIONS

- Resolution: 8 Bits
- Total Unadjusted Error:  $\pm 1/2$  LSB and  $\pm 1$  LSB
- Single Supply: 5 V<sub>DC</sub>
- Low Power: 15 mW
- Conversion Time: 40  $\mu$ s

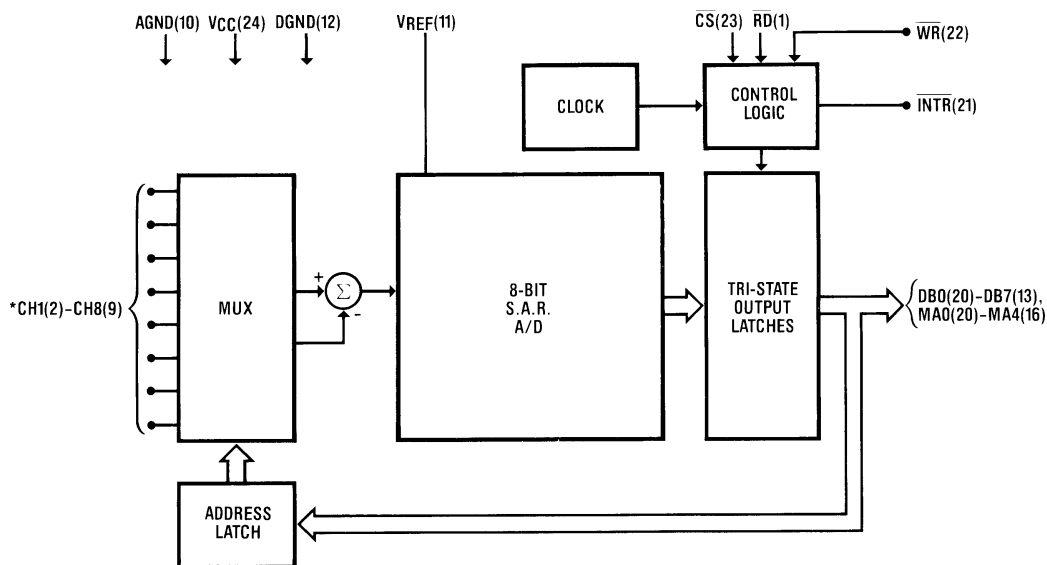
### DESCRIPTION

The ADC0844 and ADC0848 are CMOS 8-bit successive approximation A/D converters with versatile analog input multiplexers. The 4-channel or 8-channel multiplexers can be software configured for single-ended, differential or pseudo-differential modes of operation.

The differential mode provides low frequency input common mode rejection and allows offsetting the analog range of the converter. In addition, the A/D's reference can be adjusted enabling the conversion of reduced analog ranges with 8-bit resolution.

The A/Ds are designed to operate from the control bus of a wide variety of microprocessors. TRI-STATE output latches that directly drive the data bus permit the A/Ds to be configured as memory locations or I/O devices to the microprocessor with no interface logic necessary.

### Block Diagram



\* ADC0848 shown in PDIP Package CH5-CH8 not included on the ADC0844



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

All trademarks are the property of their respective owners.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 1999–2013, Texas Instruments Incorporated

## Connection Diagram

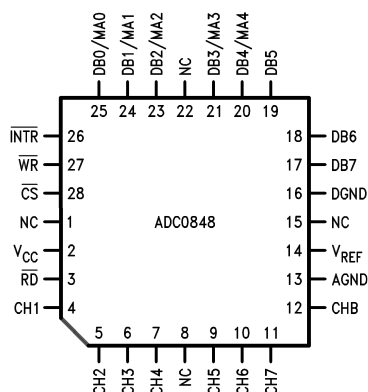


Figure 1. PLCC Package (Top View)

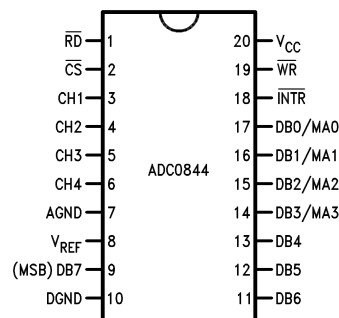


Figure 2. 20-Pin PDIP (Top View)

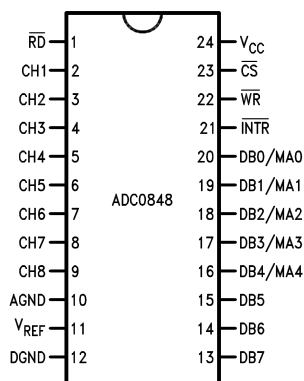


Figure 3. 28-Pin PDIP (Top View)



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## Absolute Maximum Ratings<sup>(1)(2)(3)</sup>

Supply Voltage ( $V_{CC}$ )		6.5V
Voltage	Logic Control Inputs	-0.3V to +15V
	At Other Inputs and Outputs	-0.3V to $V_{CC}+0.3V$
Input Current at Any Pin <sup>(4)</sup>		5 mA
Package Input Current <sup>(4)</sup>		20 mA
Storage Temperature		-65°C to +150°C
Package Dissipation at $T_A=25^\circ\text{C}$		875 mW
ESD Susceptibility <sup>(5)</sup>		800V
Lead Temperature (Soldering, 10 seconds)	PDIP Package	260°C
	PLCC Package	Vapor Phase (60 seconds)
		Infrared (15 seconds)
		215°C
		220°C

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.
- (2) All voltages are measured with respect to the ground pins.
- (3) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/Distributors for availability and specifications.
- (4) When the input voltage ( $V_{IN}$ ) at any pin exceeds the power supply rails ( $V_{IN} < V^-$  or  $V_{IN} > V^+$ ) the absolute value of the current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with a 5 mA current limit to four.
- (5) Human body model, 100 pF discharged through a 1.5 kΩ resistor.

## Operating Conditions<sup>(1)(2)</sup>

Supply Voltage ( $V_{CC}$ )		4.5 $V_{DC}$ to 6.0 $V_{DC}$
Temperature Range ( $T_{MIN} \leq T_A \leq T_{MAX}$ )	ADC0844CCN, ADC0848BCN, ADC0848CCN	$0^\circ\text{C} \leq T_A \leq 70^\circ\text{C}$
	ADC0844BCJ <sup>(3)</sup> , ADC0844CCJ <sup>(3)</sup> , ADC0848BCV, ADC0848CCV	$-40^\circ\text{C} \leq T_A \leq 85^\circ\text{C}$

- (1) Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. DC and AC electrical specifications do not apply when operating the device beyond its specified operating conditions.
- (2) All voltages are measured with respect to the ground pins.
- (3) Product/package combination obsolete; shown for reference only.

## Electrical Characteristics

The following specifications apply for  $V_{CC} = 5 V_{DC}$  unless otherwise specified. **Boldface limits apply from  $T_{MIN}$  to  $T_{MAX}$** ; all other limits  $T_A = T_J = 25^\circ\text{C}$ .

Parameter		Conditions	ADC0844BCJ <sup>(1)</sup> ADC0844CCJ <sup>(1)</sup>			ADC0844CCN, ADC0848BCN, ADC0848CCN, ADC0848BCV, ADC0848CCV			Limit Units
			Typ <sup>(2)</sup>	Tested Limit <sup>(3)</sup>	Design Limit <sup>(4)</sup>	Typ <sup>(2)</sup>	Tested Limit <sup>(3)</sup>	Design Limit <sup>(4)</sup>	
CONVERTER AND MULTIPLEXER CHARACTERISTICS									
Maximum Total		V <sub>REF</sub> = 5.00 V <sub>DC</sub> <sup>(5)</sup>							
Unadjusted Error	ADC0844BCN, ADC0848BCN, BCV						±½	±½	LSB
	ADC0844CCN, ADC0848CCN, CCV						±1	±1	LSB
	ADC0844CCJ <sup>(1)</sup>			±1					LSB
Minimum Reference Input Resistance			2.4	1.1		2.4	1.2	1.1	kΩ
Maximum Reference Input Resistance			2.4	5.9		2.4	5.4	5.9	kΩ
Maximum Common-Mode Input Voltage		See <sup>(6)</sup>		V <sub>CC</sub> + 0.05			V <sub>CC</sub> + 0.05	V <sub>CC</sub> + 0.05	V
Minimum Common-Mode Input Voltage		See <sup>(6)</sup>		GND – 0.05			GND – 0.05	GND – 0.05	V
DC Common-Mode Error		Differential Mode	±1/16	±¼		±1/16	±¼	±¼	LSB
Power Supply Sensitivity		V <sub>CC</sub> = 5V±5%	±1/16	±⅙		±1/16	±⅙	±⅙	LSB
Off Channel Leakage Current		On Channel = 5V, Off Channel = 0V <sup>(7)</sup>		–1			–0.1	–1	μA
		On Channel = 0V, Off Channel = 5V		1			0.1	1	μA
DIGITAL AND DC CHARACTERISTICS									
V <sub>IN(1)</sub> , Logical “1” Input Voltage (Min)		V <sub>CC</sub> = 5.25V		2.0			2.0	2.0	V
V <sub>IN(0)</sub> , Logical “0” Input Voltage (Max)		V <sub>CC</sub> = 4.75V		0.8			0.8	0.8	V
I <sub>IN(1)</sub> , Logical “1” Input Current (Max)		V <sub>IN</sub> = 5.0V	0.005	1		0.005		1	μA
I <sub>IN(0)</sub> , Logical “0” Input Current (Max)		V <sub>IN</sub> = 0V	–0.005	–1		–0.005		–1	μA

- (1) This product/package combination is obsolete. Shown for reference only.
- (2) Typical figures are at  $25^\circ\text{C}$  and represent most likely parametric norm.
- (3) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).
- (4) Design limits are specified by not 100% tested. These limits are not used to calculate outgoing quality levels.
- (5) Total unadjusted error includes offset, full-scale, linearity, and multiplexer error.
- (6) For  $V_{IN(-)} \geq V_{IN(+)}$  the digital output code will be 0000 0000. Two on-chip diodes are tied to each analog input, which will forward-conduct for analog input voltages one diode drop below ground or one diode drop greater than  $V_{CC}$  supply. Be careful during testing at low  $V_{CC}$  levels (4.5V), as high level analog inputs (5V) can cause this input diode to conduct, especially at elevated temperatures, and cause errors for analog inputs near full-scale. The spec allows 50 mV forward bias of either diode. This means that as long as the analog  $V_{IN}$  does not exceed the supply voltage by more than 50 mV, the output code will be correct. To achieve an absolute 0  $V_{DC}$  to 5  $V_{DC}$  input voltage range will therefore require a minimum supply voltage of 4.950  $V_{DC}$  over temperature variations, initial tolerance and loading.
- (7) Off channel leakage current is measured after the channel selection.

## Electrical Characteristics (continued)

The following specifications apply for  $V_{CC} = 5 V_{DC}$  unless otherwise specified. **Boldface limits apply from  $T_{MIN}$  to  $T_{MAX}$** ; all other limits  $T_A = T_J = 25^\circ C$ .

Parameter	Conditions	ADC0844BCJ <sup>(1)</sup> ADC0844CCJ <sup>(1)</sup>			ADC0844CCN, ADC0848BCN, ADC0848CCN, ADC0848BCV, ADC0848CCV			Limit Units
		Typ <sup>(2)</sup>	Tested Limit <sup>(3)</sup>	Design Limit <sup>(4)</sup>	Typ <sup>(2)</sup>	Tested Limit <sup>(3)</sup>	Design Limit <sup>(4)</sup>	
$V_{OUT(1)}$ , Logical "1" Output Voltage (Min)	$V_{CC} = 4.75V$ , $I_{OUT} = -360 \mu A$		<b>2.4</b>			2.8	<b>2.4</b>	V
	$I_{OUT} = -10 \mu A$		<b>4.5</b>			4.6	<b>4.5</b>	V
$V_{OUT(0)}$ , Logical "0" Output Voltage (Max)	$V_{CC} = 4.75V$ , $I_{OUT} = 1.6 mA$		<b>0.4</b>			0.34	<b>0.4</b>	V
$I_{OUT}$ , TRI-STATE Output Current (Max)	$V_{OUT} = 0V$	-0.01	<b>-3</b>		-0.01	-0.3	<b>-3</b>	$\mu A$
	$V_{OUT} = 5V$	0.01	<b>3</b>		0.01	0.3	<b>3</b>	$\mu A$
$I_{SOURCE}$ , Output Source Current (Min)	$V_{OUT} = 0V$	-14	<b>-6.5</b>		-14	-7.5	<b>-6.5</b>	mA
$I_{SINK}$ , Output Sink Current (Min)	$V_{OUT} = V_{CC}$	16	<b>8.0</b>		16	9.0	<b>8.0</b>	mA
$I_{CC}$ , Supply Current (Max)	$\overline{CS} = 1$ , $V_{REF}$ Open	1	<b>2.5</b>		1	2.3	<b>2.5</b>	mA

## AC Electrical Characteristics

The following specifications apply for  $V_{CC} = 5V_{DC}$ ,  $t_r = t_f = 10 ns$  unless otherwise specified. **Boldface limits apply from  $T_{MIN}$  to  $T_{MAX}$** ; all other limits  $T_A = T_J = 25^\circ C$ .

Parameter	Conditions	Typ <sup>(1)</sup>	Tested Limit <sup>(2)</sup>	Design Limit <sup>(3)</sup>	Units
$t_C$ , Maximum Conversion Time (See <a href="#">Figure 7</a> )		30	40	<b>60</b>	$\mu s$
$t_{W(\overline{WR})}$ , Minimum $\overline{WR}$ Pulse Width	See <sup>(4)</sup>	50	150		ns
$t_{ACC}$ , Maximum Access Time (Delay from Falling Edge of $\overline{RD}$ to Output Data Valid)	$C_L = 100 pF^{(4)}$	145		225	ns
$t_{1H}$ , $t_{0H}$ , TRI-STATE Control (Maximum Delay from Rising Edge of $\overline{RD}$ to Hi-Z State)	$C_L = 10 pF$ , $R_L = 10k^{(4)}$	125		200	ns
$t_{WL}$ , $t_{RL}$ , Maximum Delay from Falling Edge of $\overline{WR}$ or $\overline{RD}$ to Reset of INTR	See <sup>(4)</sup>	200	400		ns
$t_{DS}$ , Minimum Data Set-Up Time		50	100		ns
$t_{DH}$ , Minimum Data Hold Time		0	50		ns
$C_{IN}$ , Capacitance of Logic Inputs		5			pF
$C_{OUT}$ , Capacitance of Logic Outputs		5			pF

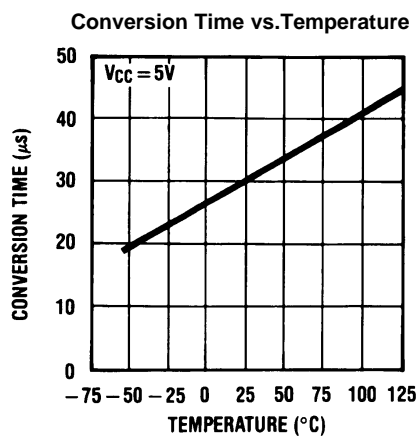
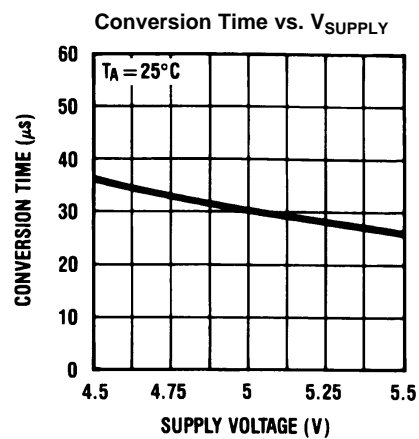
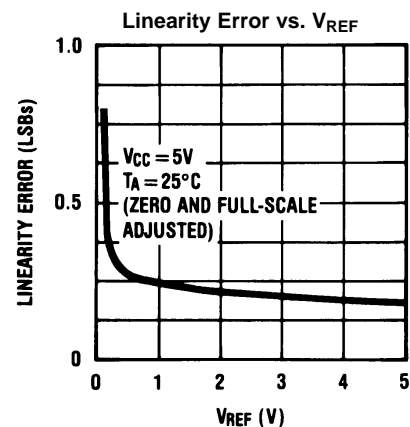
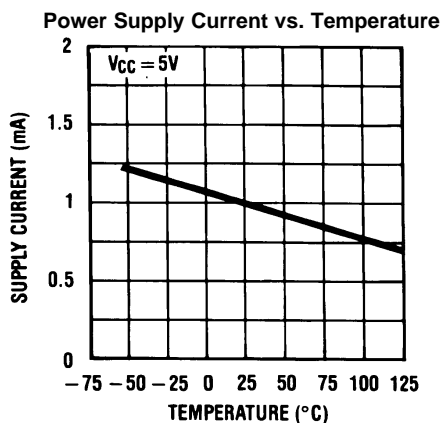
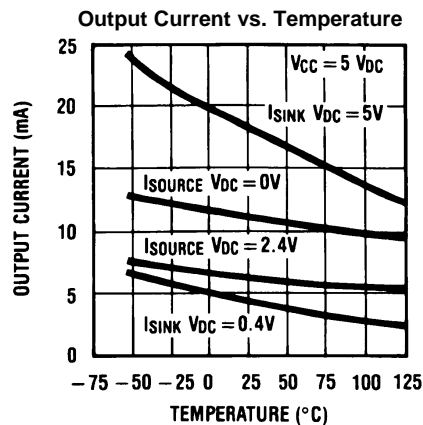
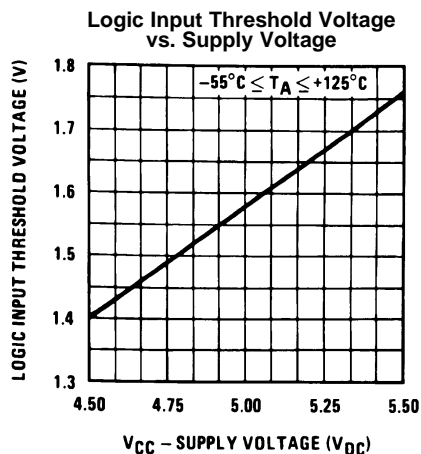
(1) Typical figures are at  $25^\circ C$  and represent most likely parametric norm.

(2) Tested limits are specified to TI's AOQL (Average Outgoing Quality Level).

(3) Design limits are specified by not 100% tested. These limits are not used to calculate outgoing quality levels.

(4) The temperature coefficient is  $0.3\%/^\circ C$ .

## Typical Performance Characteristics



## Typical Performance Characteristics (continued)

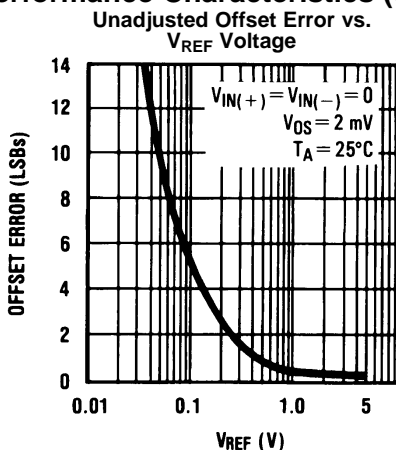
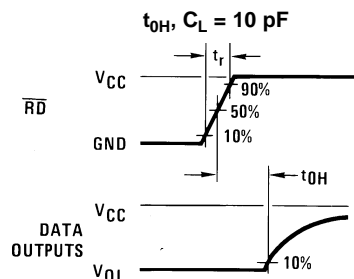
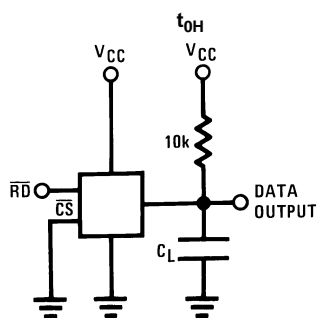
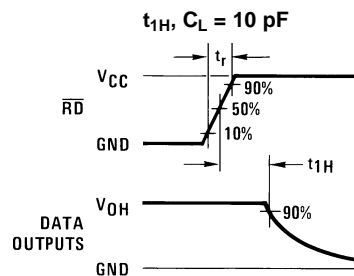
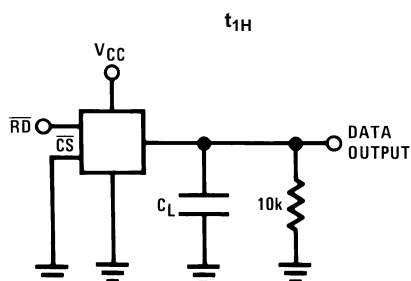
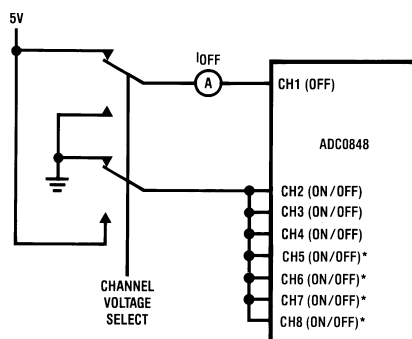


Figure 10.

## TRI-STATE Test Circuits and Waveforms

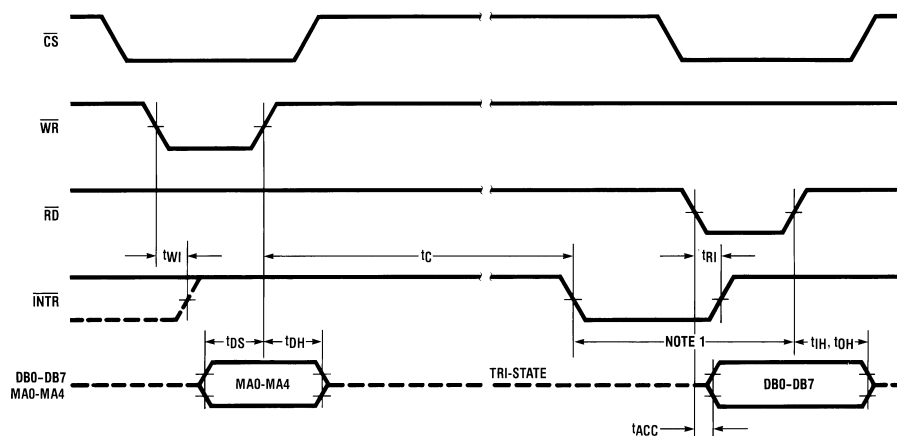
 $t_r = 20 \text{ ns}$ 

## Leakage Current Test Circuit



\*NOT INCLUDED ON ADC0844

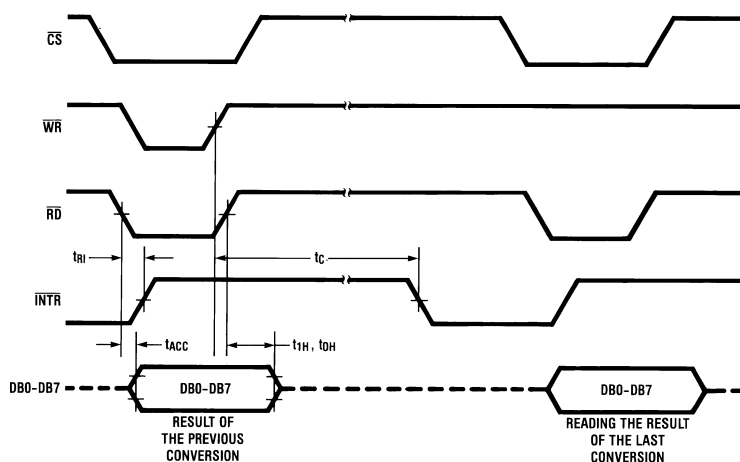
## Timing Diagrams



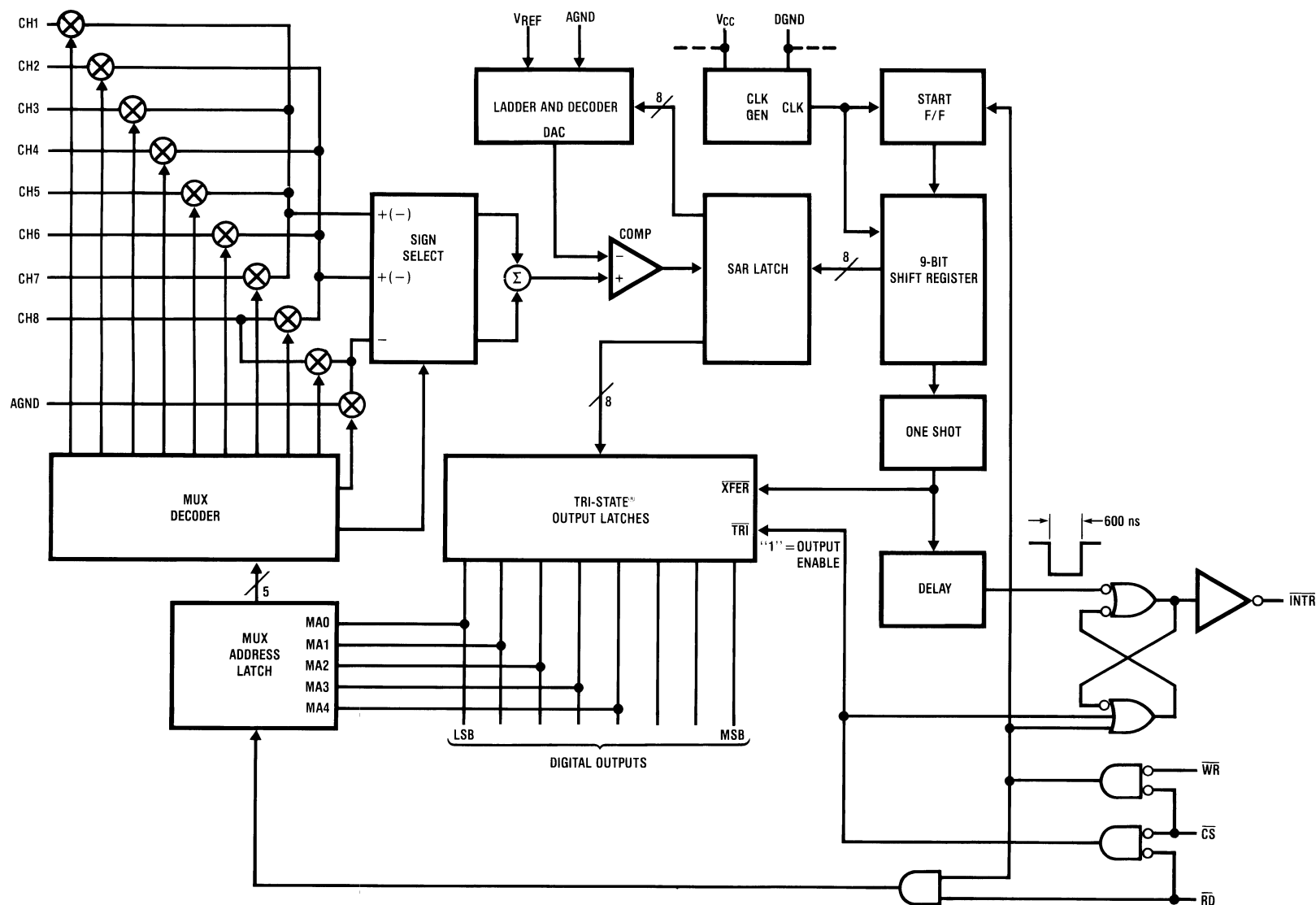
Read strobe must occur at least 600 ns after the assertion of interrupt to ensure reset of  $\overline{INTR}$ .

MA stands for MUX address.

**Figure 11. Using the Previously Selected Channel Configuration and Starting a Conversion**



## ADC0848 Functional Block Diagram





## Functional Description

The ADC0844 and ADC0848 contain a 4-channel and 8-channel analog input multiplexer (MUX) respectively. Each MUX can be configured into one of three modes of operation differential, pseudo-differential, and single ended. These modes are discussed in [Applications Information](#). The specific mode is selected by loading the MUX address latch with the proper address (see [Table 1](#) and [Table 2](#)). Inputs to the MUX address latch (MA0-MA4) are common with data bus lines (DB0-DB4) and are enabled when the  $\overline{RD}$  line is high. A conversion is initiated via the  $\overline{CS}$  and  $\overline{WR}$  lines. If the data from a previous conversion is not read, the  $\overline{INTR}$  line will be low. The falling edge of  $\overline{WR}$  will reset the  $\overline{INTR}$  line high and ready the A/D for a conversion cycle. The rising edge of  $\overline{WR}$ , with  $\overline{RD}$  high, strobes the data on the MA0/DB0-MA4/DB4 inputs into the MUX address latch to select a new input configuration and start a conversion. If the  $\overline{RD}$  line is held low during the entire low period of  $\overline{WR}$  the previous MUX configuration is retained, and the data of the previous conversion is the output on lines DB0-DB7. After the conversion cycle ( $t_C \leq 40 \mu s$ ), which is set by the internal clock frequency, the digital data is transferred to the output latch and the  $\overline{INTR}$  is asserted low. Taking  $\overline{CS}$  and  $\overline{RD}$  low resets  $\overline{INTR}$  output high and outputs the conversion result on the data lines (DB0-DB7).

## APPLICATIONS INFORMATION

### MULTIPLEXER CONFIGURATION

The design of these converters utilizes a sampled-data comparator structure which allows a differential analog input to be converted by a successive approximation routine.

The actual voltage converted is always the difference between an assigned “+” input terminal and a “-” input terminal. The polarity of each input terminal of the pair being converted indicates which line the converter expects to be the most positive. If the assigned “+” input is less than the “-” input the converter responds with an all zeros output code.

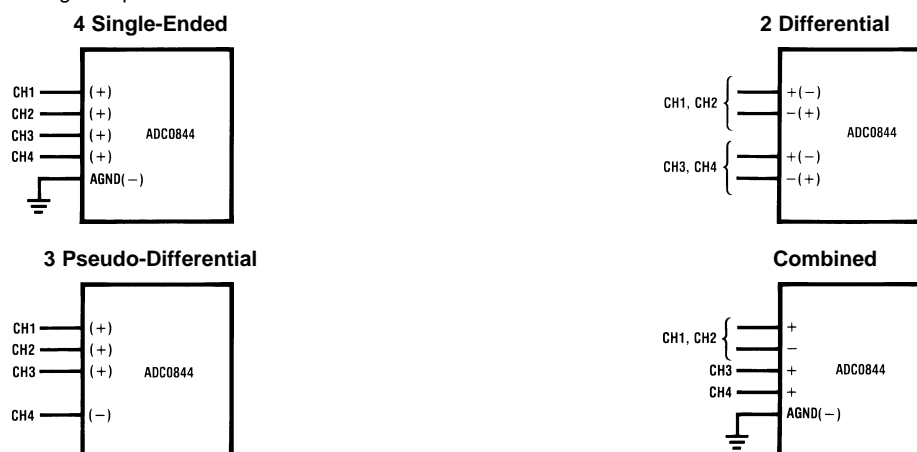
A unique input multiplexing scheme has been utilized to provide multiple analog channels. The input channels can be software configured into three modes: differential, single ended, or pseudo-differential. [Figure 12](#) shows the three modes using the 4-channel MUX ADC0844. The eight inputs of the ADC0848 can also be configured in any of the three modes. In the differential mode, the ADC0844 channel inputs are grouped in pairs, CH1 with CH2 and CH3 with CH4. The polarity assignment of each channel in the pair is interchangeable. The single-ended mode has CH1-CH4 assigned as the positive input with the negative input being the analog ground (AGND) of the device. Finally, in the pseudo-differential mode CH1-CH3 are positive inputs referenced to CH4 which is now a pseudo-ground. This pseudo-ground input can be set to any potential within the input common-mode range of the converter. The analog signal conditioning required in transducer-based data acquisition systems is significantly simplified with this type of input flexibility. One converter package can now handle ground referenced inputs and true differential inputs as well as signals with some arbitrary reference voltage.

The analog input voltages for each channel can range from 50 mV below ground to 50 mV above  $V_{CC}$  (typically 5V) without degrading conversion accuracy.

**Table 1. ADC0844 MUX ADDRESSING<sup>(1)</sup>**

MUX Address				$\overline{\text{CS}}$	$\overline{\text{WR}}$	$\overline{\text{RD}}$	Channel#					MUX Mode	
MA3	MA2	MA1	MA0				CH1	CH2	CH3	CH4	AGND		
X	L	L	L	L	NP	H	+	−				Differential	
X	L	L	H	L		H	−	+					
X	L	H	L	L		H			+	−			
X	L	H	H	L		H			−	+			
L	H	L	L	L	NP	H	+				−	Single-Ended	
L	H	L	H	L		H		+			−		
L	H	H	L	L		H			+		−		
L	H	H	H	L		H				+	−		
H	H	L	L	L	NP	H	+			−		Pseudo- Differential	
H	H	L	H	L		H		+		−			
H	H	H	L	L		H			+	−			
X	X	X	X	L	NP	L	Previous Channel Configuration						

(1) X = don't care, NP = negative pulse

**Figure 12. Analog Input Multiplexer Options**

## REFERENCE CONSIDERATIONS

The voltage applied to the reference input of these converters defines the voltage span of the analog input (the difference between  $V_{IN(MAX)}$  and  $V_{IN(MIN)}$ ) over which the 256 possible output codes apply. The devices can be used in either ratiometric applications or in systems requiring absolute accuracy. The reference pin must be connected to a voltage source capable of driving the minimum reference input resistance of 1.1 k $\Omega$ . This pin is the top of a resistor divider string used for the successive approximation conversion.

In a ratiometric system (Figure 13), the analog input voltage is proportional to the voltage used for the A/D reference. This voltage is typically the system power supply, so the  $V_{REF}$  pin can be tied to  $V_{CC}$ . This technique relaxes the stability requirements of the system reference as the analog input and A/D reference move together maintaining the same output code for a given input condition. For absolute accuracy (Figure 14), where the analog input varies between very specific voltage limits, the reference pin can be biased with a time and temperature stable voltage source. The LM385 and LM336 reference diodes are good low current devices to use with these converters.

The maximum value of the reference is limited to the  $V_{CC}$  supply voltage. The minimum value, however, can be quite small (see Typical Performance Characteristics) to allow direct conversions of transducer outputs providing less than a 5V output span. Particular care must be taken with regard to noise pickup, circuit layout and system error voltage sources when operating with a reduced span due to the increased sensitivity of the converter (1 LSB equals  $V_{REF}/256$ ).

## THE ANALOG INPUTS

### Analog Differential Voltage Inputs and Common-Mode Rejection

The differential input of these converters actually reduces the effects of common-mode input noise, a signal common to both selected “+” and “–” inputs for a conversion (60 Hz is most typical). The time interval between sampling the “+” input and then the “–” inputs is ½ of a clock period. The change in the common-mode voltage during this short time interval can cause conversion errors. For a sinusoidal common-mode signal this error is:

$$V_{\text{ERROR(MAX)}} = V_{\text{peak}} (2\pi f_{\text{CM}}) \times 0.5 \times \left( \frac{t_{\text{C}}}{8} \right)$$

where

- $f_{\text{CM}}$  is the frequency of the common-mode signal
- $V_{\text{peak}}$  is its peak voltage value
- $t_{\text{C}}$  is the conversion time

For a 60 Hz common-mode signal to generate a ¼ LSB error ( $\approx 5$  mV) with the converter running at 40  $\mu\text{s}$ , its peak value would have to be 5.43V. This large a common-mode signal is much greater than that generally found in a well designed data acquisition system.

**Table 2. ADC0848 MUX Addressing<sup>(1)</sup>**

MUX Address					$\overline{\text{CS}}$	$\overline{\text{WR}}$	$\overline{\text{RD}}$	Channel									MUX Mode
MA4	MA3	MA2	MA1	MA0				CH1	CH2	CH3	CH4	CH5	CH6	CH7	CH8	AGND	
X	L	L	L	L	L	NP	H	+	–								Differential
X	L	L	L	H	L		H	–	+								
X	L	L	H	L	L		H			+	–						
X	L	L	H	H	L		H			–	+						
X	L	H	L	L	L		H					+	–				
X	L	H	L	H	L		H					–	+				
X	L	H	H	L	L		H							+	–		
X	L	H	H	H	L		H							–	+		
L	H	L	L	L	L	NP	H	+								–	Single-Ended
L	H	L	L	H	L		H		+							–	
L	H	L	H	L	L		H			+						–	
L	H	L	H	H	L		H				+					–	
L	H	H	L	L	L		H					+				–	
L	H	H	L	H	L		H						+			–	
L	H	H	H	L	L		H							+		–	
L	H	H	H	H	L		H								+	–	
H	H	L	L	L	L	NP	H	+							–		Pseudo-Differential
H	H	L	L	H	L		H		+						–		
H	H	L	H	L	L		H			+					–		
H	H	L	H	H	L		H				+				–		
H	H	H	L	L	L		H					+			–		
H	H	H	L	H	L		H						+		–		
H	H	H	H	L	L		H							+	–		
H	H	H	H	H	L		H								–		
X	X	X	X	X	L		L	Previous Channel Configuration									

(1) X = don't care, NP = negative pulse

## Input Current

Due to the sampling nature of the analog inputs, short duration spikes of current enter the “+” input and exit the “–” input at the clock edges during the actual conversion. These currents decay rapidly and do not cause errors as the internal comparator is strobed at the end of a clock period. Bypass capacitors at the inputs will average these currents and cause an effective DC current to flow through the output resistance of the analog signal source. Bypass capacitors should not be used if the source resistance is greater than 1 k $\Omega$ .

## Input Source Resistance

The limitation of the input source resistance due to the DC leakage currents of the input multiplexer is important. A worst-case leakage current of  $\pm 1 \mu\text{A}$  over temperature will create a 1 mV input error with a 1 k $\Omega$  source resistance. An op amp RC active low pass filter can provide both impedance buffering and noise filtering should a high impedance signal source be required.

## OPTIONAL ADJUSTMENTS

### Zero Error

The zero of the A/D does not require adjustment. If the minimum analog input voltage value,  $V_{\text{IN(MIN)}}$ , is not ground, a zero offset can be done. The converter can be made to output 0000 0000 digital code for this minimum input voltage by biasing any  $V_{\text{IN}}(-)$  input at this  $V_{\text{IN(MIN)}}$  value. This is useful for either differential or pseudo-differential modes of input channel configuration.

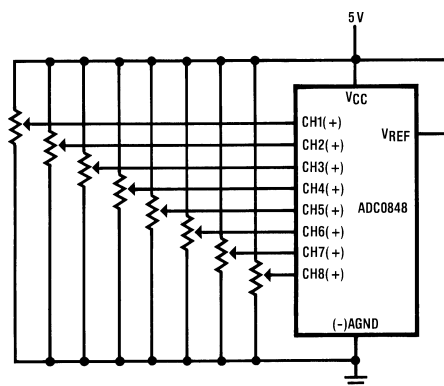
The zero error of the A/D converter relates to the location of the first riser of the transfer function and can be measured by grounding the  $V^-$  input and applying a small magnitude positive voltage to the  $V^+$  input. Zero error is the difference between actual DC input voltage which is necessary to just cause an output digital code transition from 0000 0000 to 0000 0001 and the ideal  $\frac{1}{2}$  LSB value ( $\frac{1}{2}$  LSB = 9.8 mV for  $V_{\text{REF}} = 5.000 V_{\text{DC}}$ ).

### Full-Scale

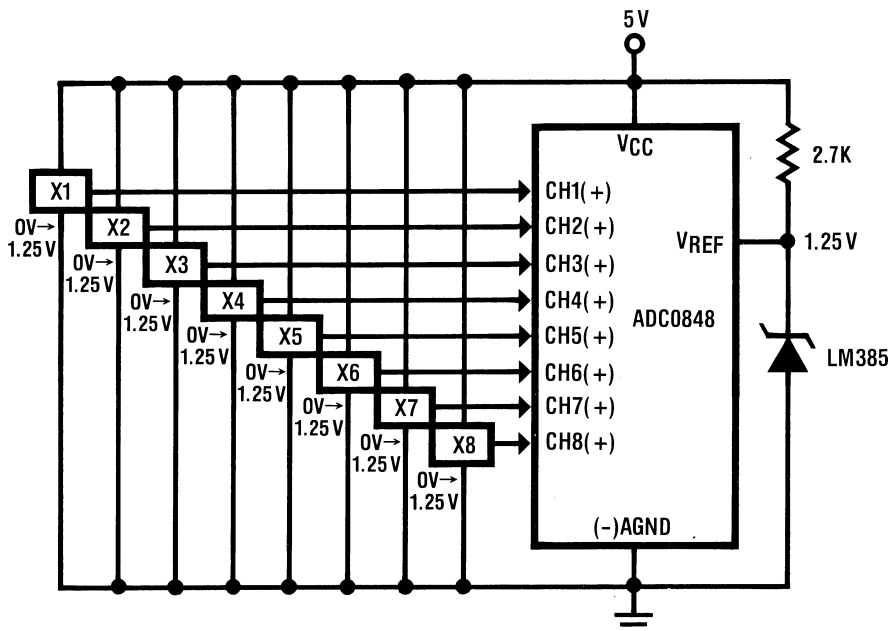
The full-scale adjustment can be made by applying a differential input voltage which is  $1 \frac{1}{2}$  LSB down from the desired analog full-scale voltage range and then adjusting the magnitude of the  $V_{\text{REF}}$  input for a digital output code changing from 1111 1110 to 1111 1111.

### Adjusting for an Arbitrary Analog Input Voltage Range

If the analog zero voltage of the A/D is shifted away from ground (for example, to accommodate an analog input signal which does not go to ground), this new zero reference should be properly adjusted first. A  $V_{\text{IN}}(+)$  voltage which equals this desired zero reference plus  $\frac{1}{2}$  LSB (where the LSB is calculated for the desired analog span,  $1 \text{ LSB} = \text{analog span}/256$ ) is applied to selected “+” input and the zero reference voltage at the corresponding “–” input should then be adjusted to just obtain the 00<sub>HEX</sub> to 01<sub>HEX</sub> code transition.



**Figure 13. Referencing Examples - Ratiometric**



### Figure 14. Referencing Examples - Absolute with a Reduced Span

The full-scale adjustment should be made [with the proper  $V_{IN}$  (-) voltage applied] by forcing a voltage to the  $V_{IN}$  (+) input which is given by:

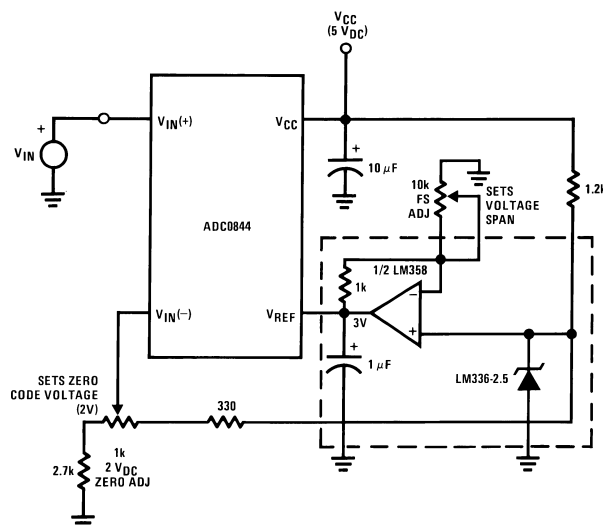
$$V_{IN} (+) \text{ fs adj} = V_{MAX} - 1.5 \left[ \frac{(V_{MAX} - V_{MIN})}{256} \right]$$

where

- $V_{MAX}$  = the high end of the analog input range
  - $V_{MIN}$  = the low end (the offset zero) of the analog range. (Both are ground referenced.)
- (1)

The  $V_{REF}$  (or  $V_{CC}$ ) voltage is then adjusted to provide a code change from  $FE_{HEX}$  to  $FF_{HEX}$ . This completes the adjustment procedure.

For an example see the Zero-Shift and Span Adjust circuit below.



**Figure 15. Zero-Shift and Span Adjust ( $2V \leq V_{IN} \leq 5V$ )**

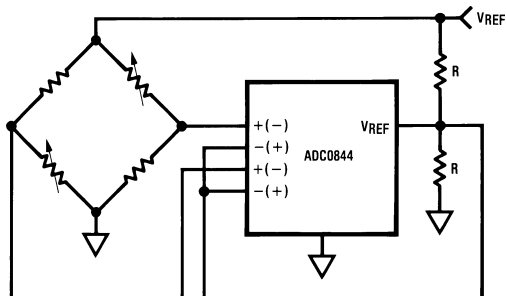


Figure 16. Differential Voltage Input 9-Bit A/D

Diodes are 1N914

DO = all 1s if  $V_{IN(+)} > V_{IN(-)}$   
DO = all 0s if  $V_{IN(+)} < V_{IN(-)}$

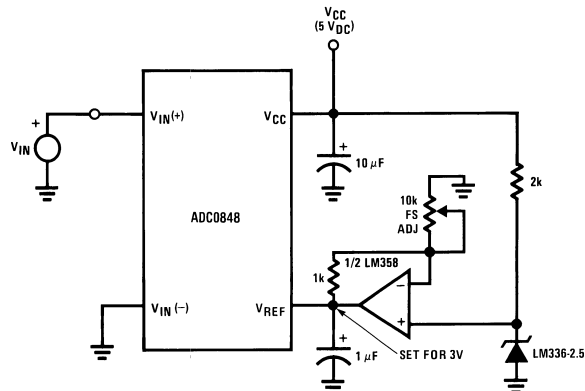


Figure 17. Span Adjust ( $0V \leq V_{IN} \leq 3V$ )

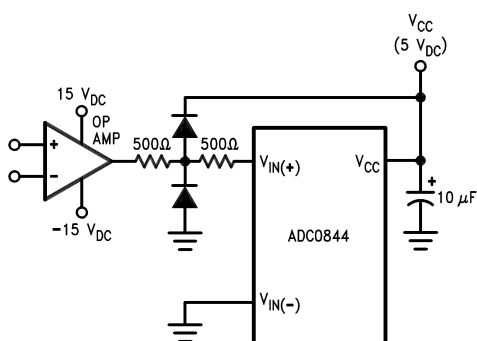


Figure 18. Protecting the Input

\*  $V_{IN(-)} = 0.15 V_{CC}$   
 $15\% \text{ of } V_{CC} \leq V_{XDR} \leq 85\% \text{ of } V_{CC}$

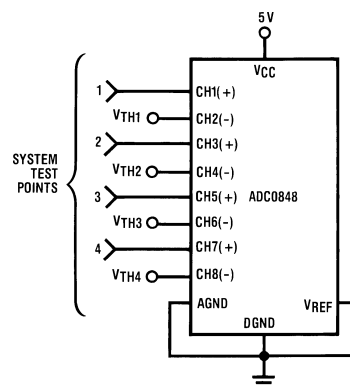


Figure 19. High Accuracy Comparators

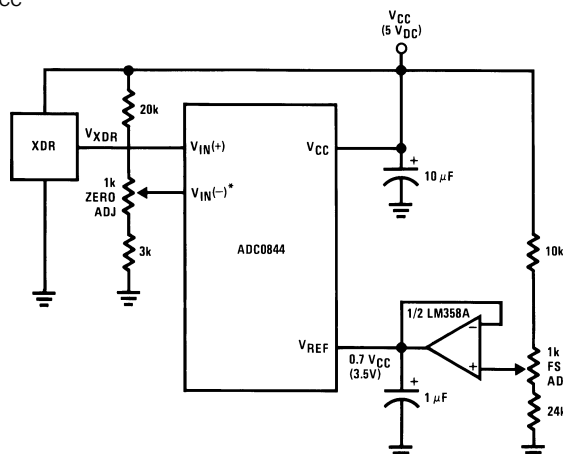
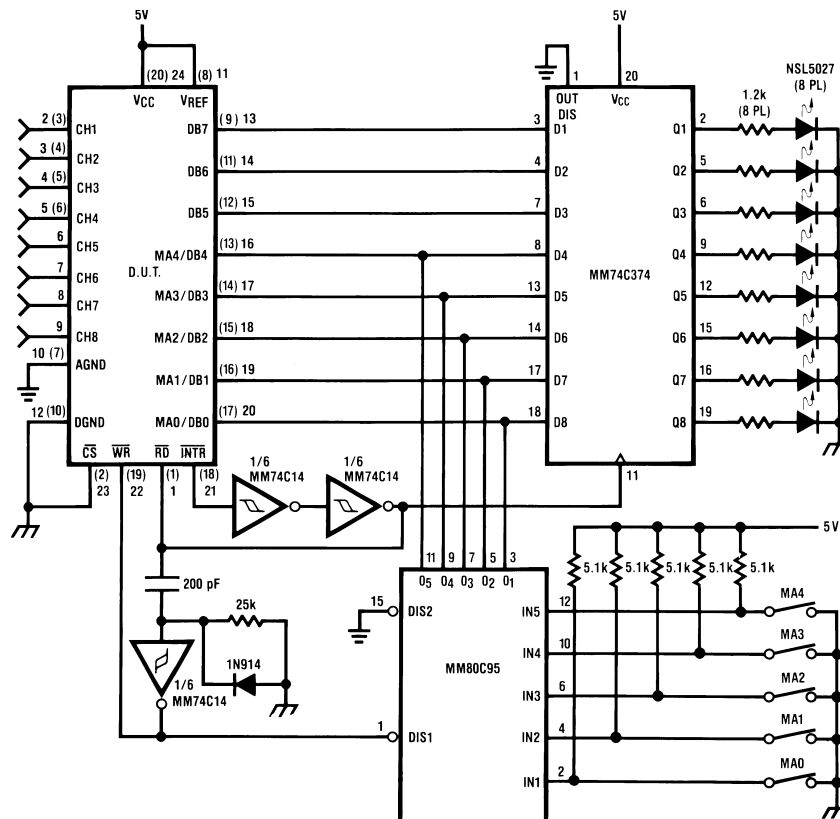
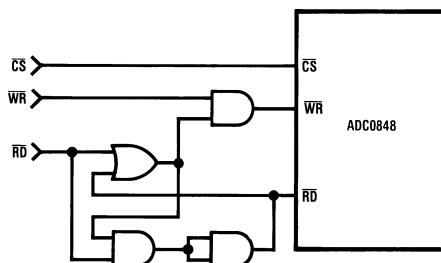


Figure 20. Operating with Automotive Ratiometric Transducers



Note: DUT pin numbers in parentheses are for ADC0844, others are for ADC0848.

Figure 21. A Stand Alone Circuit



$\overline{CS} \cdot \overline{WR}$  will update the channel configuration and start a conversion.

$\overline{CS} \cdot \overline{RD}$  will read the conversion data and start a new conversion without updating the channel configuration.

Waiting for the end of this conversion is not necessary. A  $\overline{CS} \cdot \overline{WR}$  can immediately follow the  $\overline{CS} \cdot \overline{RD}$ .

Figure 22. Start a Conversion without Updating the Channel Configuration

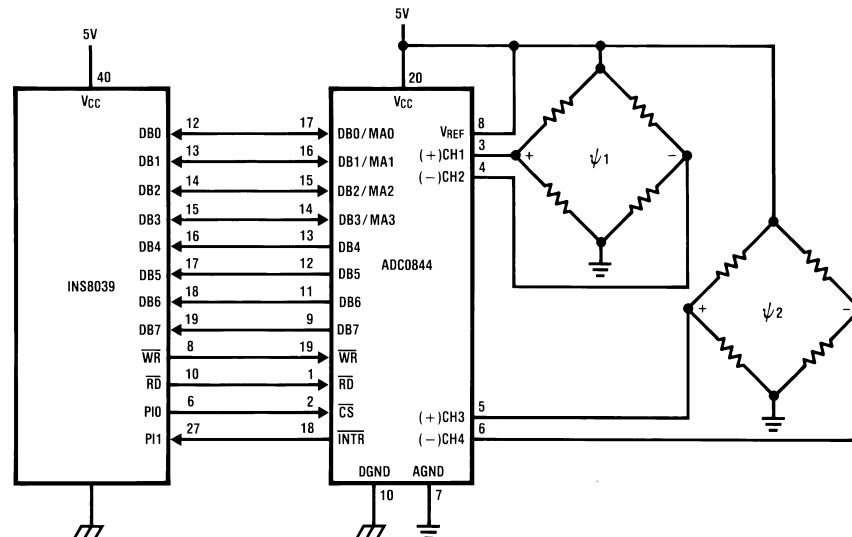


Figure 23. ADC0844—INS8039 Interface

### Sample Program for ADC0844 - INS8039 Interface Converting Two Ratiometric Differential Signals

```

0000 04 10      ORG      0H
                JMP      BEGIN          ;START PROGRAM AT ADDR 10
0010 B9 FF      BEGIN:  MOV      R1,#0FFH      ;MAIN PROGRAM
                                ;LOAD R1 WITH AN UNUSED ADDR
                                ;LOCATION
0012 B8 20      MOV      R0,#20H          ;A/D DATA ADDRESS
0014 89 FF      ORL      P1,#0FFH        ;SET PORT 1 OUTPUTS HIGH
0016 23 00      MOV      A,00H          ;LOAD THE ACC WITH A/D MUX DATA
                                ;CH1 AND CH2 DIFFERENTIAL
0018 14 50      CALL     CONV            ;CALL THE CONVERSION SUBROUTINE
001A 23 02      MOV      A,#02H          ;LOAD THE ACC WITH A/D MUX DATA
                                ;CH3 AND CH4 DIFFERENTIAL
001C 18         INC      R0              ;INCREMENT THE A/D DATA ADDRESS
001D 14 50      CALL     CONV            ;CALL THE CONVERSION SUBROUTINE

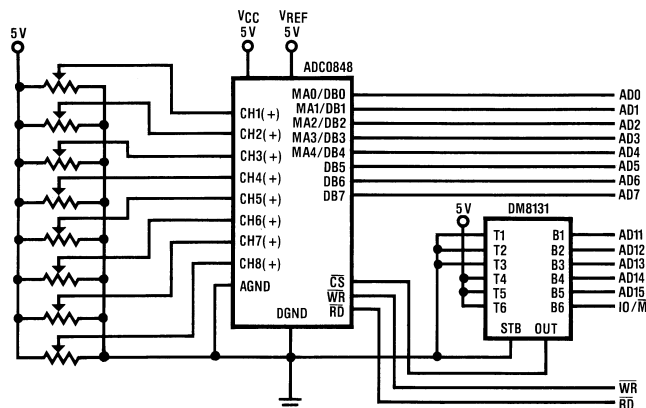
                ;CONTINUE MAIN PROGRAM

                ;CONVERSION SUBROUTINE
                ;ENTRY:ACC-A/D MUX DATA
                ;EXIT:ACC-CONVERTED DATA

0050 99 FE      CONV:   ORG      50H
0052 91         ANL      P1#0FEH        ;CHIP SELECT THE A/D
0053 09         MOVX    @R1,A           ;LOAD A/D MUX & START CONVERSION
                                ;INPUT INTR STATE
0054 32 53      LOOP:   IN      A,P1
                                ;IF INTR = 1 GOTO LOOP
0056 81         JB1     LOOP            ;IF INTR = 0 INPUT A/D DATA
0057 89 01      MOVX    A,@R1          ;IF INTR = 0 INPUT A/D DATA
                                ;CLEAR THE A/D CHIP SELECT
0059 A0         ORL      P1,&01H        ;CLEAR THE A/D CHIP SELECT
005A 83         MOV     @R0,A          ;STORE THE A/D DATA
                                ;RETURN TO MAIN PROGRAM

```





**Figure 24. I/O Interface to NSC800**

### Sample Program for ADC0848 - NSC800 Interface

```

0008          NCONV      EQU      16
000F          DEL        EQU      15          ;DELAY 50 μSEC CONVERSION
001F          CS         EQU      1FH          ;THE BOARD ADDRESS
3C00          ADDTA       EQU      003CH       ;START OF RAM FOR A/D
                                         ;DATA

0000'         08 09 0A 0B MUXDTA: DB      08H,09H,0AH,0BH ;MUX DATA
0004'         0C 0D 0E 0F          DB      0CH,0DH,0EH,0FH
0008'         0E 1F          START: LD      C,CS
000A'         06 16          LD      B,NCONV
000C'         21 0000'       LD      HL,MUXDTA
000F'         11 003C       LD      DE,ADDTA
0012'         ED A3          STCONV: OUTI          ;LOAD A/D'S MUX DATA
                                         ;AND START A CONVERSION
0014'         EB          EX      DE,HL          ;HL=RAM ADDRESS FOR THE
                                         ;A/D DATA

0015'         3E 0F          LD      A,DEL
0017'         3D          WAIT: DEC      A          ;WAIT 50 μSEC FOR THE
0018'         C2 0013'       JP      NZ,WAIT       ;CONVERSION TO FINISH
001B'         ED A2          INI          ;STORE THE A/D'S DATA
                                         ;CONVERTED ALL INPUTS?

001D'         EB          EX      DE,HL
001E'         C2 000E'       JP      NZ,STCONV       ;IF NOT GOTO STCONV

          END

```

Note: This routine sequentially programs the MUX data latch in the signal-ended mode. For CH1-CH8 a conversion is started, then a 50 μs wait for the A/D to complete a conversion and the data is stored at address ADDTA for CH1, ADDTA + 1 for CH2, etc.

## REVISION HISTORY

### Changes from Revision C (March 2013) to Revision D

### Page

- Changed layout of National Data Sheet to TI format ..... [17](#)

## PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
ADC0848BCV/NOPB	ACTIVE	PLCC	FN	28	35	Green (RoHS & no Sb/Br)	SN	Level-2A-245C-4 WEEK	-40 to 85	ADC0848 BCV	<a href="#">Samples</a>
ADC0848BCVX/NOPB	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	SN	Level-2A-245C-4 WEEK	-40 to 85	ADC0848 BCV	<a href="#">Samples</a>
ADC0848CCV/NOPB	ACTIVE	PLCC	FN	28	35	Green (RoHS & no Sb/Br)	SN	Level-2A-245C-4 WEEK	-40 to 85	ADC0848 CCV	<a href="#">Samples</a>
ADC0848CCVX/NOPB	ACTIVE	PLCC	FN	28	750	Green (RoHS & no Sb/Br)	SN	Level-2A-245C-4 WEEK	-40 to 85	ADC0848 CCV	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and

---

continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

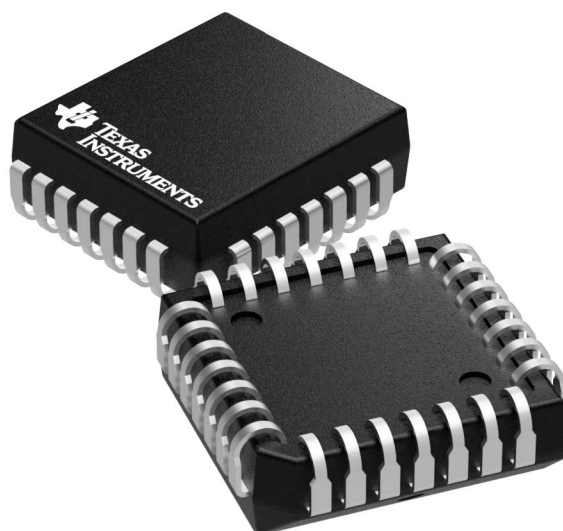
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**FN 28**

**GENERIC PACKAGE VIEW**

**PLCC - 4.57 mm max height**

PLASTIC CHIP CARRIER



Images above are just a representation of the package family, actual package may vary.  
Refer to the product data sheet for package details.

4040005-3/C

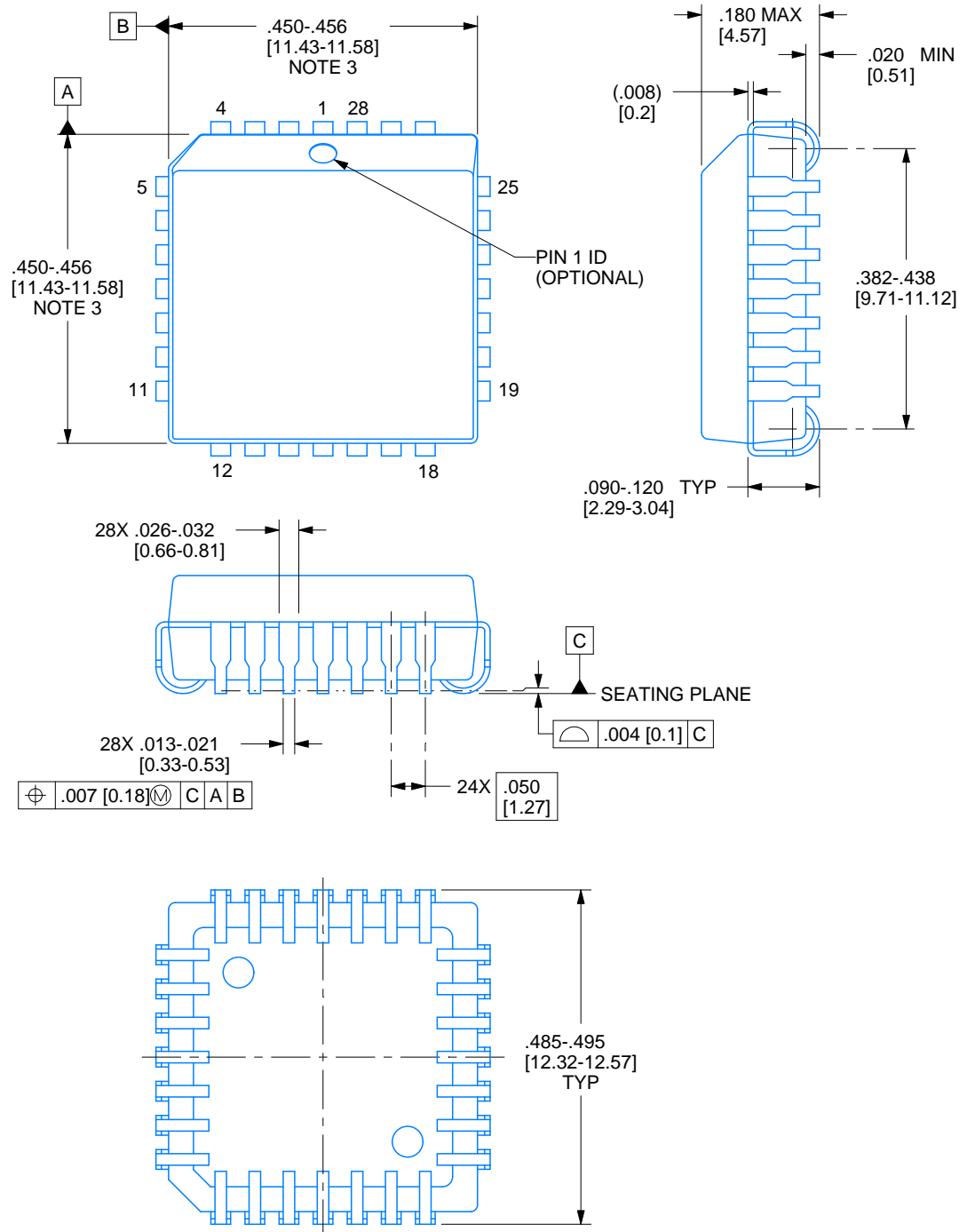
**FN0028A**



# PACKAGE OUTLINE

## PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



4215153/B 05/2017

### NOTES:

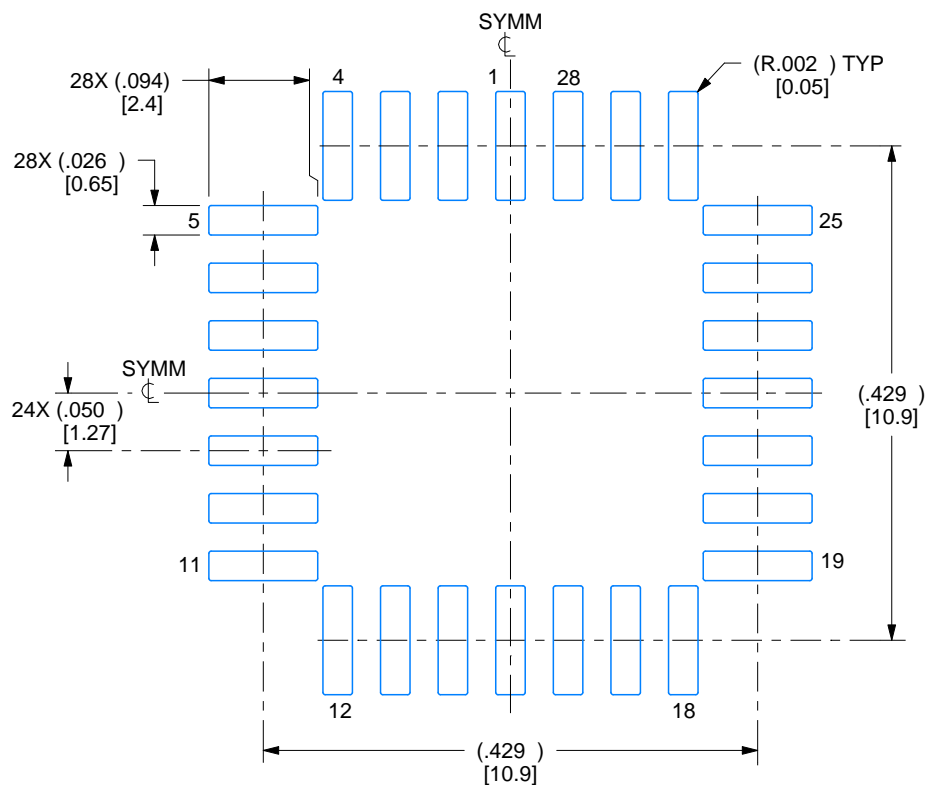
1. All linear dimensions are in inches. Any dimensions in brackets are in millimeters. Any dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Dimension does not include mold protrusion. Maximum allowable mold protrusion .01 in [0.25 mm] per side.
4. Reference JEDEC registration MS-018.

# EXAMPLE BOARD LAYOUT

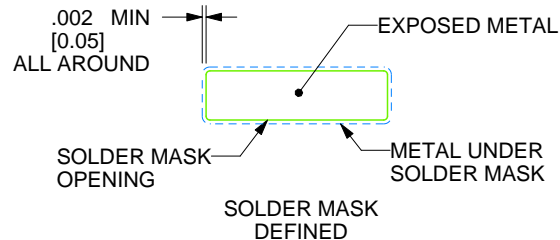
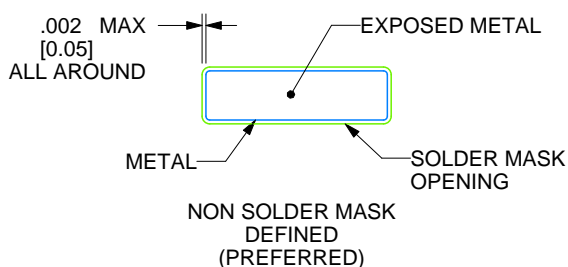
FN0028A

PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:6X



SOLDER MASK DETAILS

4215153/B 05/2017

NOTES: (continued)

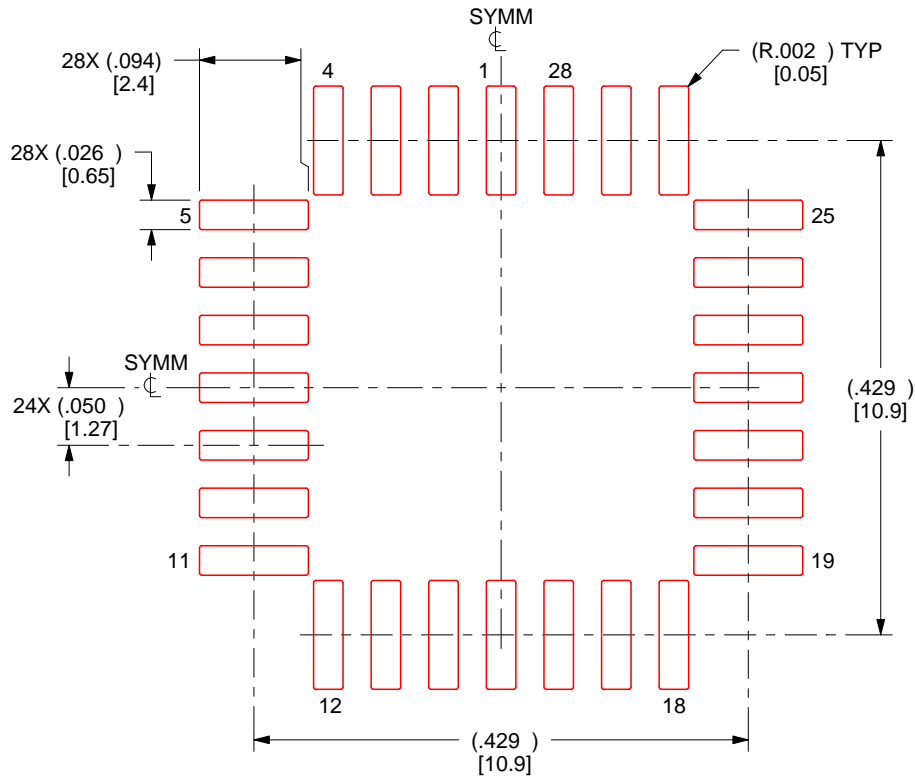
5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

FN0028A

PLCC - 4.57 mm max height

PLASTIC CHIP CARRIER



**SOLDER PASTE EXAMPLE**  
 BASED ON 0.125 mm THICK STENCIL  
 SCALE:6X

4215153/B 05/2017

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.



## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale ([www.ti.com/legal/termsofsale.html](http://www.ti.com/legal/termsofsale.html)) or other applicable terms available either on [ti.com](http://ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2020, Texas Instruments Incorporated