

## 14 W hi-fi audio amplifier

### Features

- Wide-range supply voltage, up to 36 V
- Single or split power supply
- Short-circuit protection to ground
- Thermal shutdown

### Description

The TDA2030 is a monolithic integrated circuit in the Pentawatt® package, intended for use as a low frequency class-AB amplifier. Typically it provides 14 W output power ( $d = 0.5\%$ ) at 14 V/4  $\Omega$ . At  $\pm 14$  V or 28 V, the guaranteed output power is 12 W on a 4  $\Omega$  load and 8 W on an 8  $\Omega$  (DIN45500).

The TDA2030 provides high output current and has very low harmonic and crossover distortion.

Furthermore, the device incorporates an original (and patented) short-circuit protection system comprising an arrangement for automatically limiting the dissipated power so as to keep the operating point of the output transistors within their safe operating range. A conventional thermal shutdown system is also included.

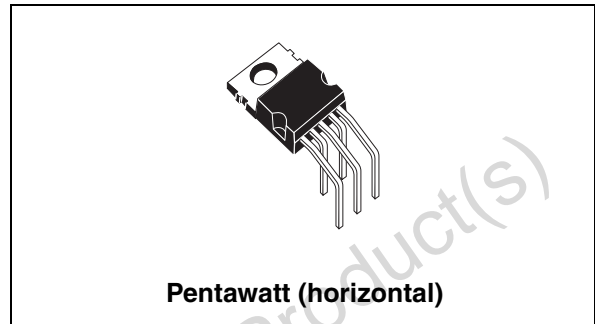
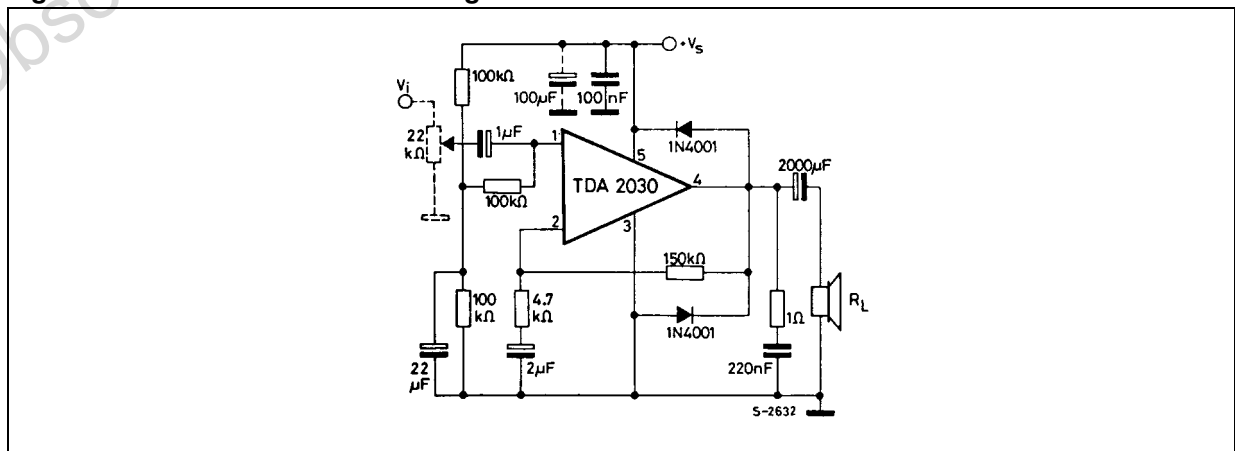


Table 1. Device summary

Order code	Package
TDA2030H	Pentawatt horizontal

Figure 1. Ex: Functional block diagram



# 1 Device overview

Figure 2. Pin connections (top view)

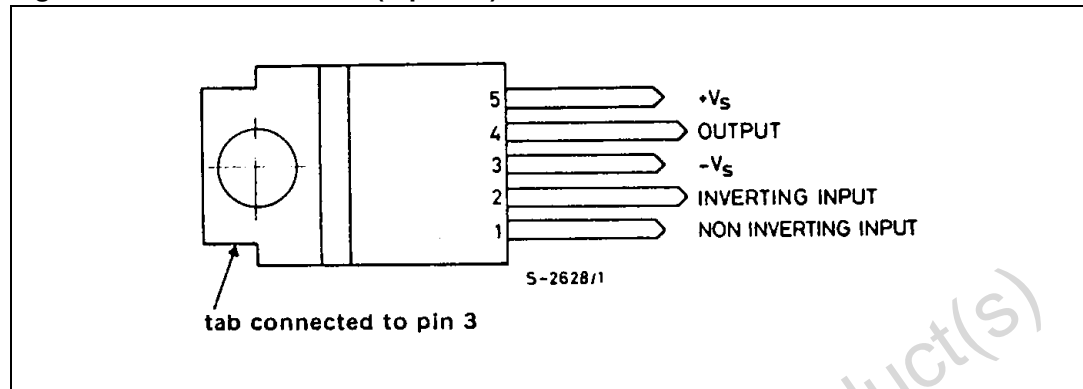
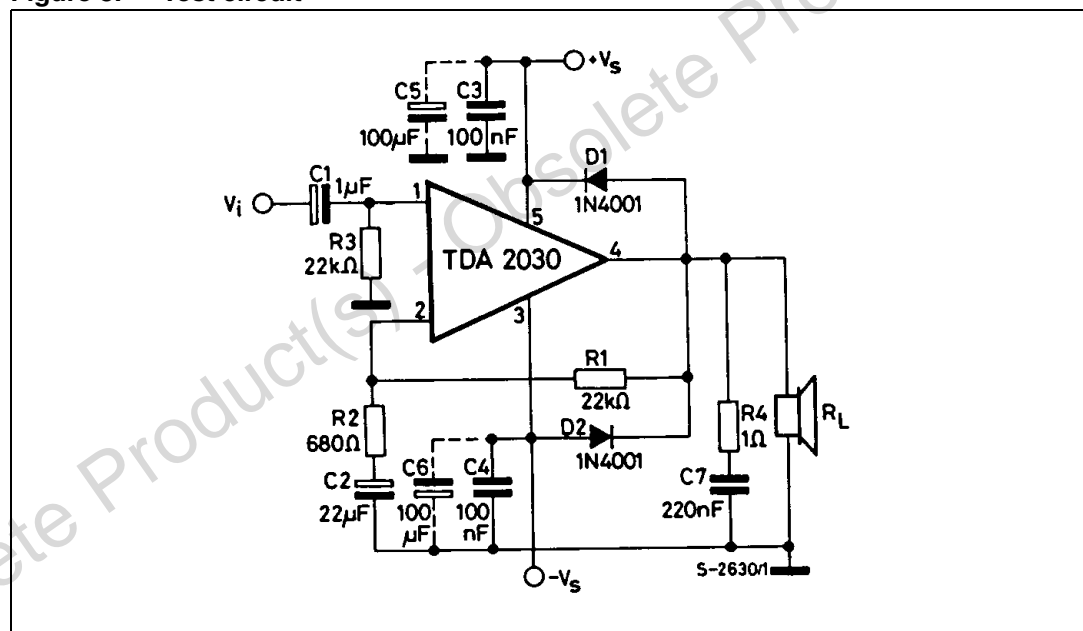


Figure 3. Test circuit



## 2 Electrical specifications

### 2.1 Absolute maximum ratings

Table 2. Absolute maximum ratings

Symbol	Parameter	Value	Unit
$V_s$	Supply voltage	$\pm 18$ (36)	V
$V_i$	Input voltage	$V_s$	
$V_i$	Differential input voltage	$\pm 15$	V
$I_o$	Output peak current internally limited)	3.5	A
$P_{tot}$	Power dissipation at $T_{case} = 90^\circ\text{C}$	20	W
$T_{stg}, T_j$	Storage and junction temperature	-40 to 150	$^\circ\text{C}$

### 2.2 Thermal data

Table 3. Thermal data

Symbol	Parameter	Value	Unit
$R_{th\ j-case}$	Thermal resistance junction-case	max 3	$^\circ\text{C}$

### 2.3 Electrical characteristics

Refer to the test circuit in [Figure 3](#);  $V_s = \pm 14\text{ V}$ ,  $T_{amb} = 25^\circ\text{C}$  unless otherwise specified.

Table 4. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_s$	Supply voltage		$\pm 6$ 12		$\pm 18$ 36	V
$I_d$	Quiescent drain current	$V_s = \pm 18$ ( $V_s = 36$ )		40	60	mA
$I_b$	Input bias current			0.2	2	$\mu\text{A}$
$V_{OS}$	Input offset voltage			$\pm 2$	$\pm 20$	mV
$I_{OS}$	Input offset current			$\pm 20$	$\pm 200$	nA
$P_o$	Output power	$d = 0.5\%$ , $f = 40$ to $15,000\text{ Hz}$ ; $G_V = 30\text{ dB}$ $R_L = 4\ \Omega$ $R_L = 8\ \Omega$	12 8	14 9		W W
		$d = 10\%$ , $f = 1\text{ kHz}$ ; $G_V = 30\text{ dB}$ $R_L = 4\ \Omega$ $R_L = 8\ \Omega$	12 8	14 9		W W

Table 4. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
d	Distortion	$P_o = 0.1$ to $12$ W, $R_L = 4\ \Omega$ , $G_V = 30$ dB $f = 40$ to $15.000$ Hz		0.2	0.5	%
		$P_o = 0.1$ to $8$ W, $R_L = 8\ \Omega$ , $G_V = 30$ dB $f = 40$ to $15.000$ Hz		0.1	0.5	%
B	Frequency response (-3 dB)	$P_o = 12$ W, $R_L = 4\ \Omega$ ; $G_V = 30$ dB	10 Hz to 140			Hz
$R_i$	Input resistance (pin 1)		0.5	5		M $\Omega$
$G_V$	Voltage gain (open loop)			90		dB
$G_V$	Voltage gain (closed loop)	$f = 1$ kHz	29.5	30	30.5	dB
$e_N$	Input noise voltage	B = 22 Hz to 22 kHz		3	10	$\mu$ V
$i_N$	Input noise current			80	200	pA
SVR	Supply voltage rejection	$G_V = 30$ dB; $R_L = 4\ \Omega$ , $R_g = 22$ k $\Omega$ , $f_{\text{ripple}} = 100$ Hz; $V_{\text{ripple}} = 0.5$ V <sub>eff</sub>	40	50		dB
$I_d$	Drain current	$P_o = 14$ W, $R_L = 4\ \Omega$ $P_o = 9$ W, $R_L = 8\ \Omega$		900 500		mA
$T_j$	Thermal shutdown junction temperature				145	$^{\circ}$ C

## 2.4 Characterizations

Figure 4. Output power vs. supply voltage

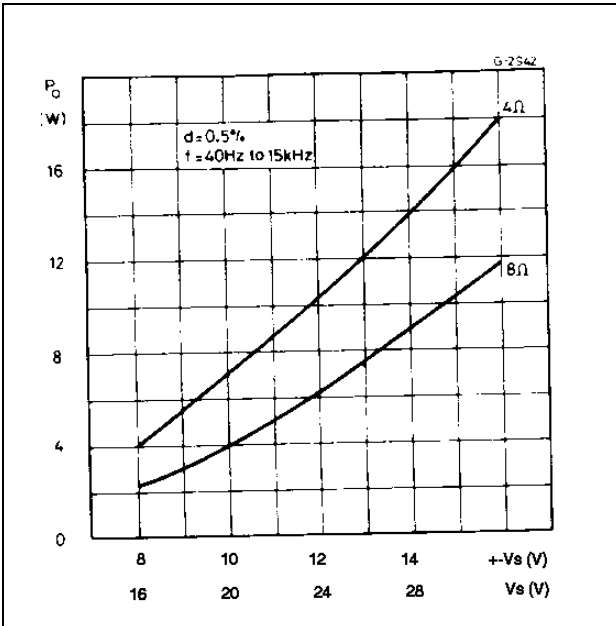


Figure 5. Output power vs. supply voltage

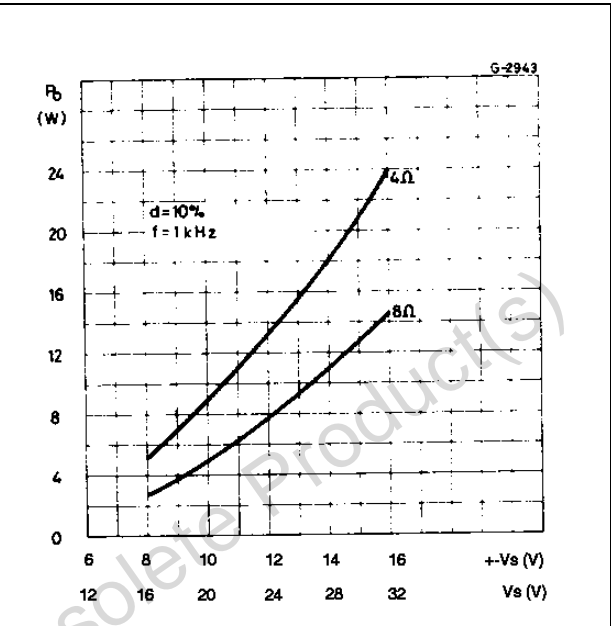


Figure 6. Distortion vs. output power

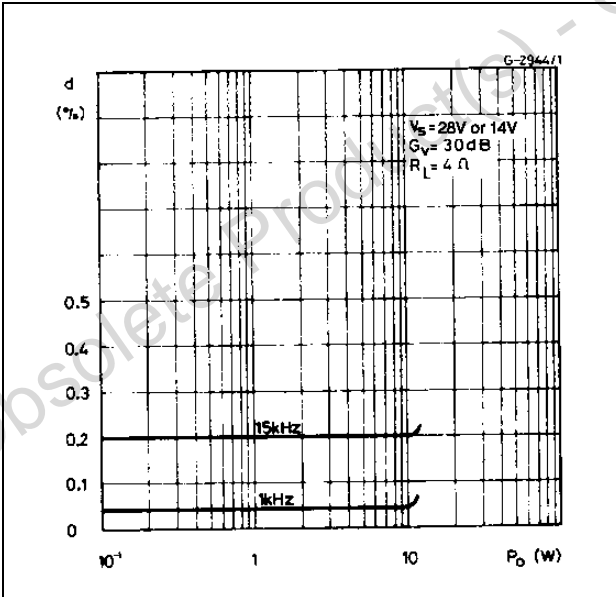


Figure 7. Distortion vs. output power

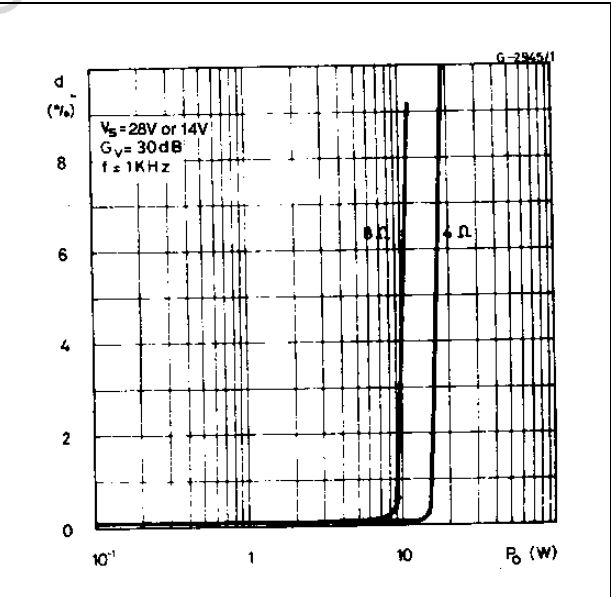


Figure 8. Distortion vs. output power

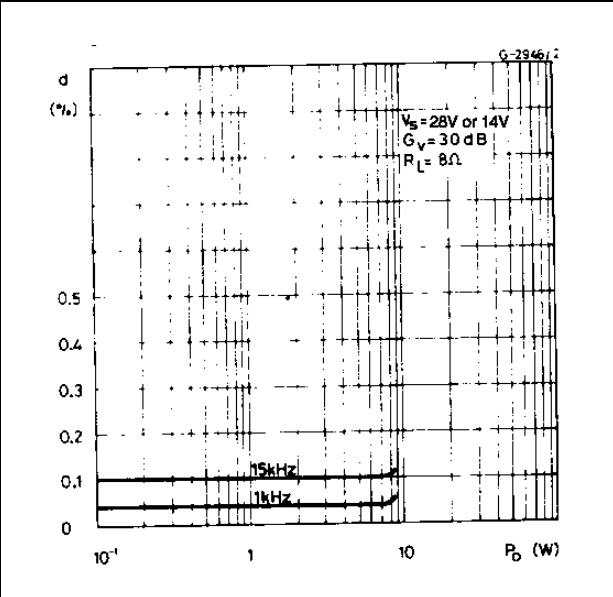


Figure 9. Distortion vs. frequency

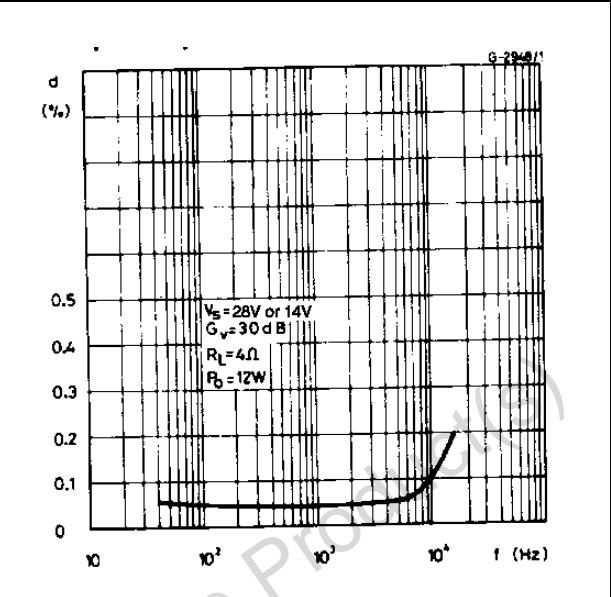


Figure 10. Distortion vs. frequency

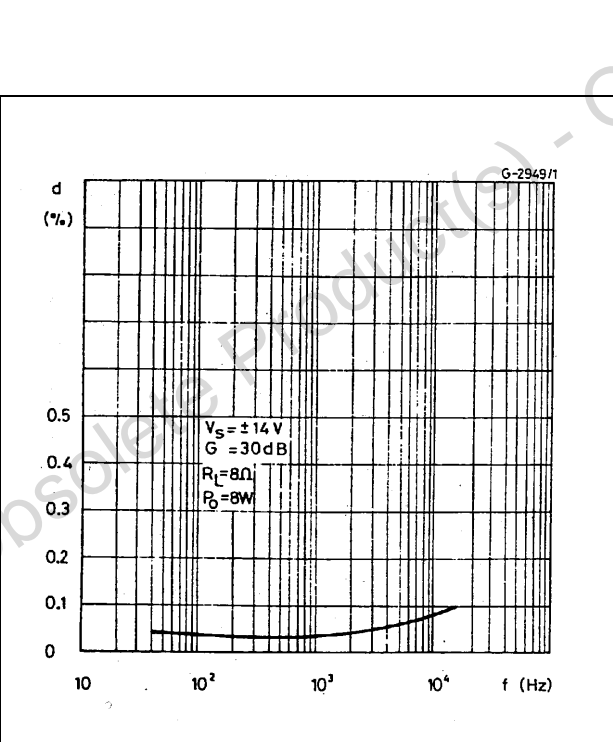


Figure 11. Frequency response with different values of the rolloff capacitor C8 (see typical amplifier with split power supply)

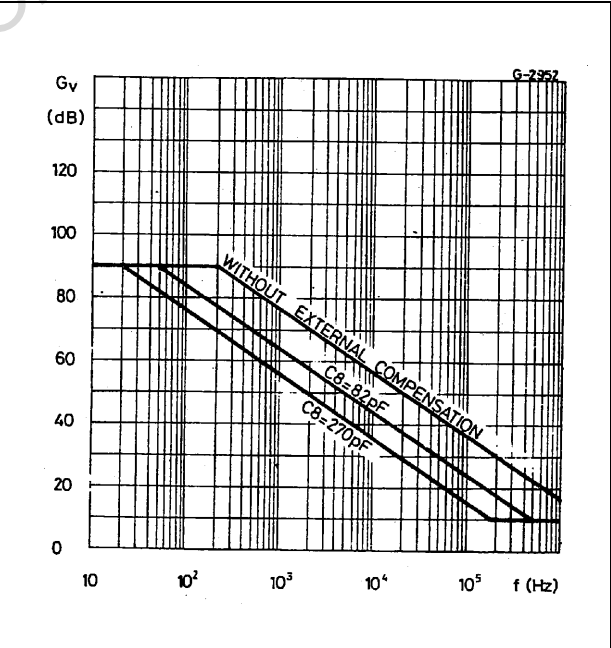


Figure 12. Quiescent current vs. supply voltage

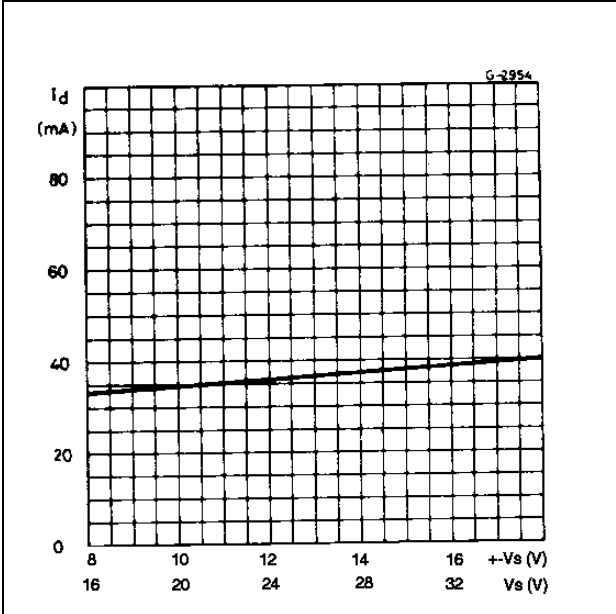


Figure 13. Supply voltage rejection vs. voltage gain

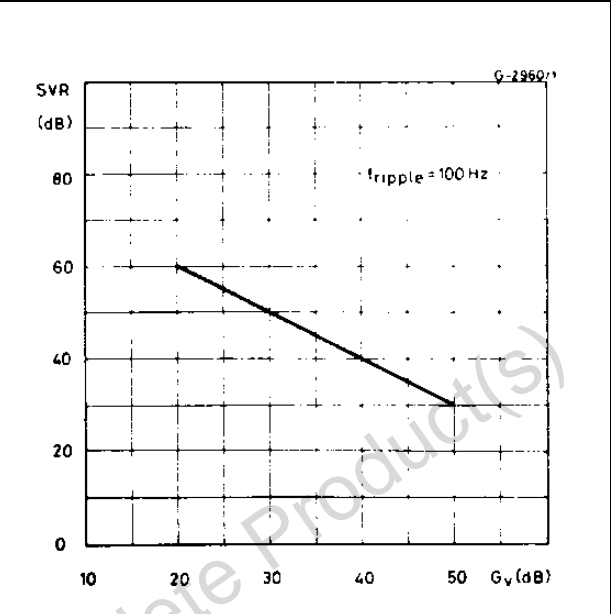


Figure 14. Power dissipation and efficiency vs. output power

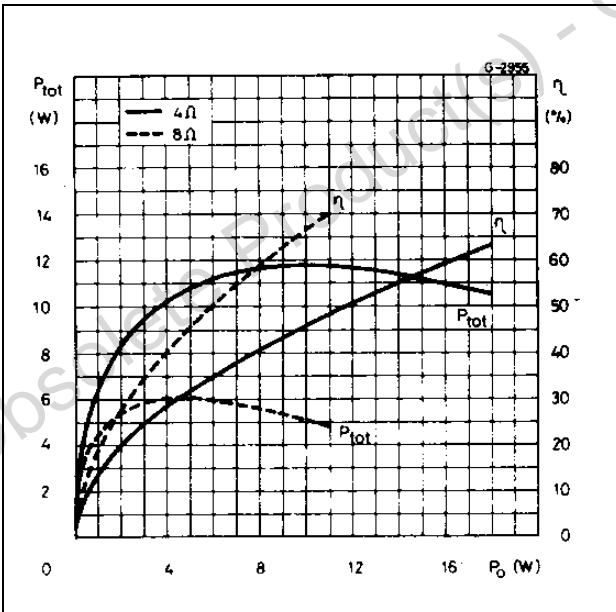
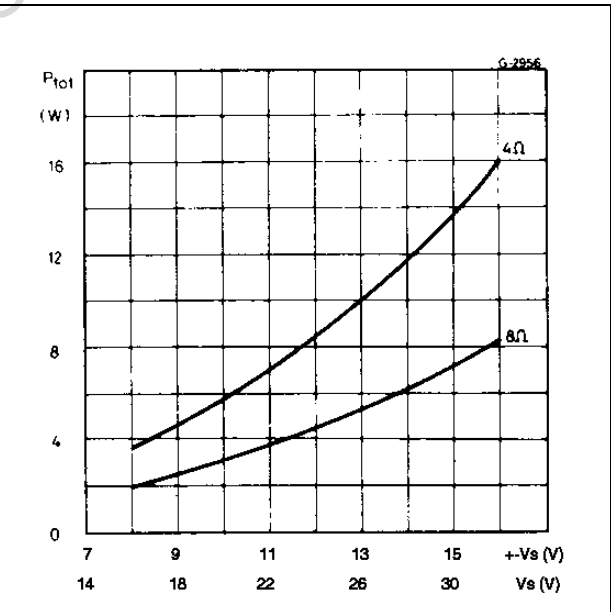


Figure 15. Maximum power dissipation vs. supply voltage (sine wave operation)



### 3 Applications

Figure 16. Typical amplifier with split power supply

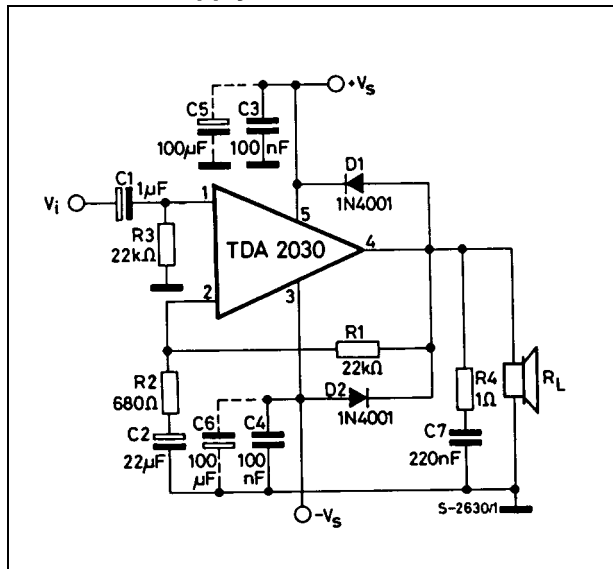


Figure 17. Typical amplifier with single power supply

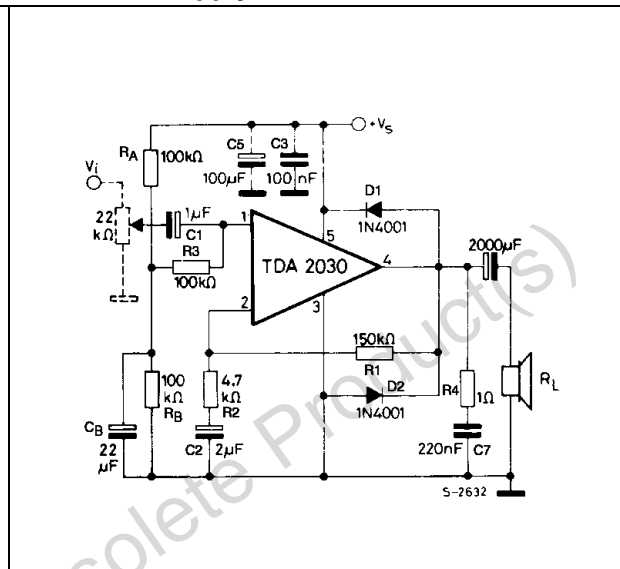


Figure 18. PC board and component layout for a typical amplifier with split power supply

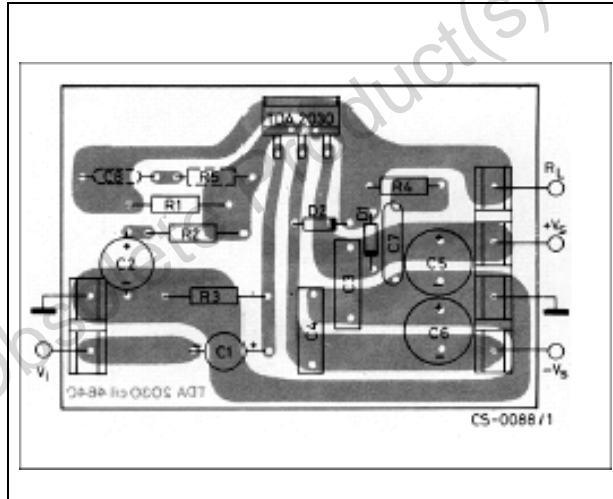


Figure 19. PC board and component layout for a typical amplifier with single power supply

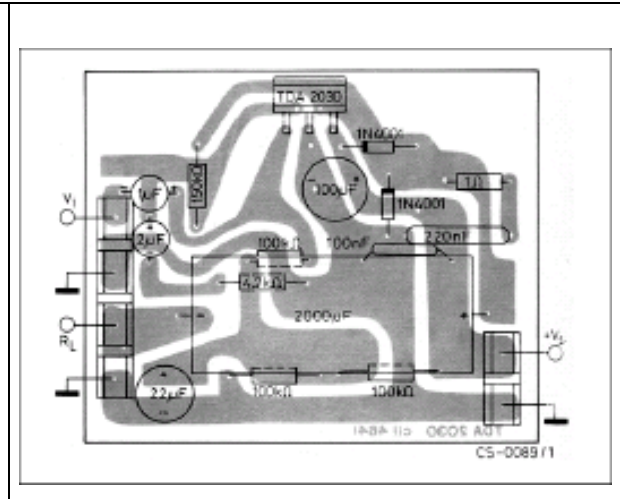
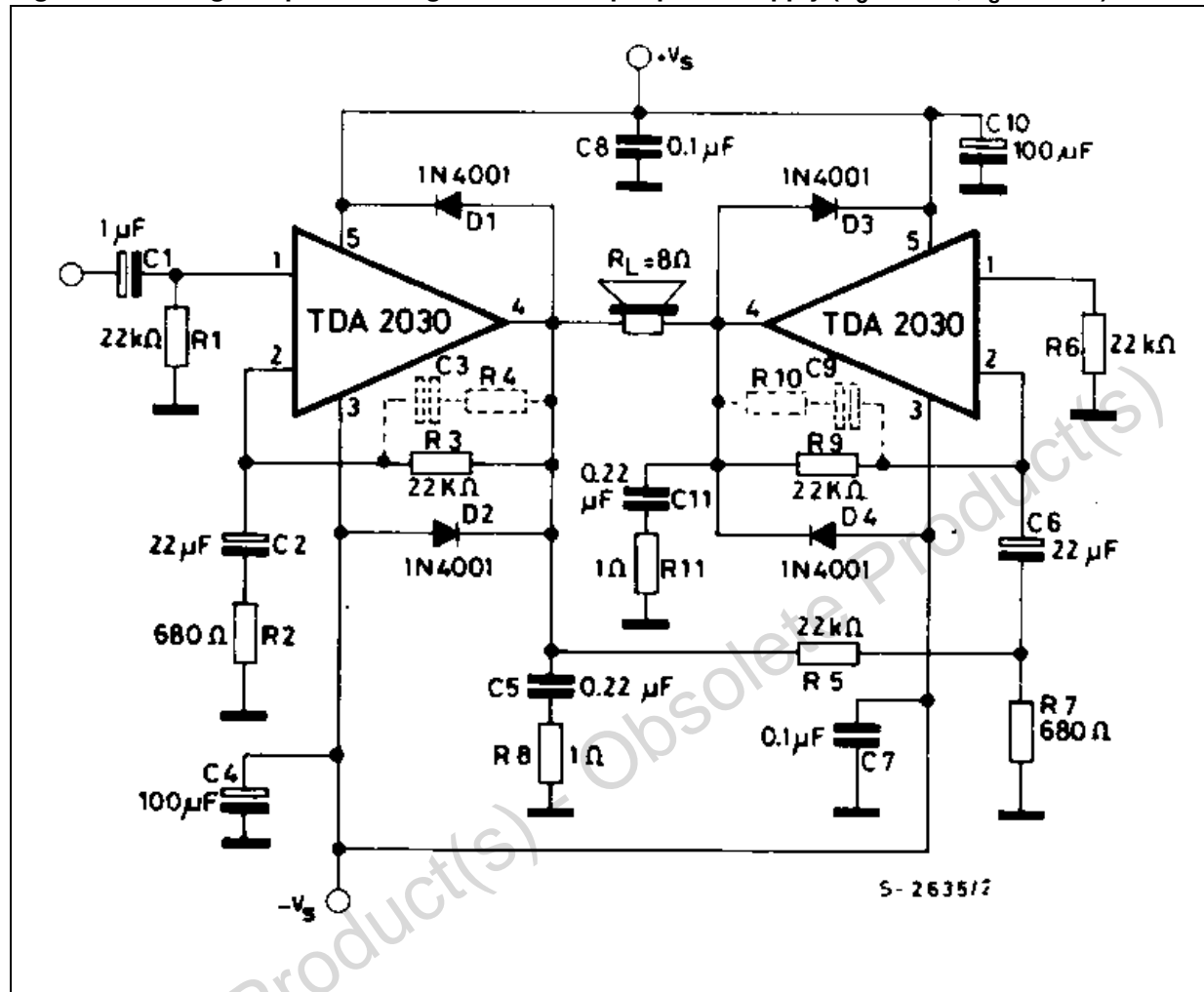




Figure 20. Bridge amplifier configuration with split power supply ( $P_o = 28\text{ W}$ ,  $V_s = \pm 14\text{ V}$ )

## 4 Practical considerations

### 4.1 Printed circuit board

The layout shown in [Figure 19](#) should be adopted by the designers. If different layouts are used, the ground points of input 1 and input 2 must be well decoupled from the ground return of the output in which a high current flows.

### 4.2 Assembly suggestion

No electrical isolation is needed between the package and the heatsink with single supply voltage configuration.

### 4.3 Application suggestions

The recommended values of the components are those shown on application circuit of [Figure 16](#). However, if different values are chosen, then the following table can be helpful.

**Table 5. Variations from recommended values**

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
R <sub>1</sub>	22 kΩ	Closed loop gain setting	Increase of gain	Decrease in gain <sup>(1)</sup>
R <sub>2</sub>	680 Ω	Closed loop gain setting	Decrease of gain <sup>(1)</sup>	Increase in gain
R <sub>3</sub>	22 kΩ	Non-inverting input biasing	Increase of input impedance	Decrease in input impedance
R <sub>4</sub>	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R <sub>5</sub>	3 R <sub>2</sub>	Upper frequency cutoff	Poor high-frequency attenuation	Danger of oscillation
C <sub>1</sub>	1 μF	Input DC decoupling		Increase in low-frequency cutoff
C <sub>2</sub>	22 μF	Inverting input DC decoupling		Increase in low-frequency cutoff
C <sub>3</sub> C <sub>4</sub>	0.1 μF	Supply voltage bypass		Danger of oscillation
C <sub>5</sub> C <sub>6</sub>	100 μF	Supply voltage bypass		Danger of oscillation
C <sub>7</sub>	0.22 μF	Frequency stability		Danger of oscillation
C <sub>8</sub>	$\frac{1}{2\pi BR_1}$	Upper frequency cutoff	Smaller bandwidth	Larger bandwidth
D <sub>1</sub> D <sub>2</sub>	1N4001	To protect the device against output voltage spikes		

1. Closed loop gain must be higher than 24 dB

Table 6. Single supply application

Component	Recommended value	Purpose	Larger than recommended value	Smaller than recommended value
R <sub>1</sub>	150 kΩ	Closed loop gain setting	Increase in gain	Decrease in gain <sup>(1)</sup>
R <sub>2</sub>	4.7 kΩ	Closed loop gain setting	Decrease in gain <sup>(1)</sup>	Increase in gain
R <sub>3</sub>	100 kΩ	Non-inverting input biasing	Increase of input impedance	Decrease in input Impedance
R <sub>4</sub>	1 Ω	Frequency stability	Danger of oscillation at high frequencies with inductive loads	
R <sub>A</sub> /R <sub>B</sub>	100 kΩ	Non-inverting input biasing	Poor high-frequency attenuation	Danger of oscillation
C <sub>1</sub>	1 μF	Input DC decoupling		Increase in low-frequency cutoff
C <sub>2</sub>	22 μF	Inverting DC decoupling		Increase in low-frequency cutoff
C <sub>3</sub>	0.1 μF	Supply voltage bypass		Danger of oscillation
C <sub>5</sub>	100 μF	Supply voltage bypass		Danger of oscillation
C <sub>7</sub>	0.22 μF	Frequency stability		Danger of oscillation
C <sub>8</sub>	$\frac{1}{2\pi BR_1}$	Upper frequency cutoff	Smaller bandwidth	Larger bandwidth
D <sub>1</sub> D <sub>2</sub>	1N4001	To protect the device against output voltage spikes.		

1. Closed loop gain must be higher than 24 dB

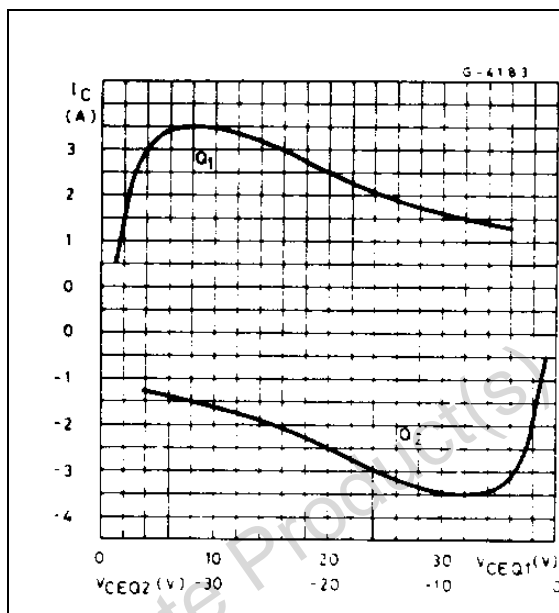
## 5 Short-circuit protection

The TDA2030 has an original circuit which limits the current of the output transistors. [Figure 21](#) shows that the maximum output current is a function of the collector emitter voltage; hence the output transistors work within their safe operating area ([Figure 5](#)).

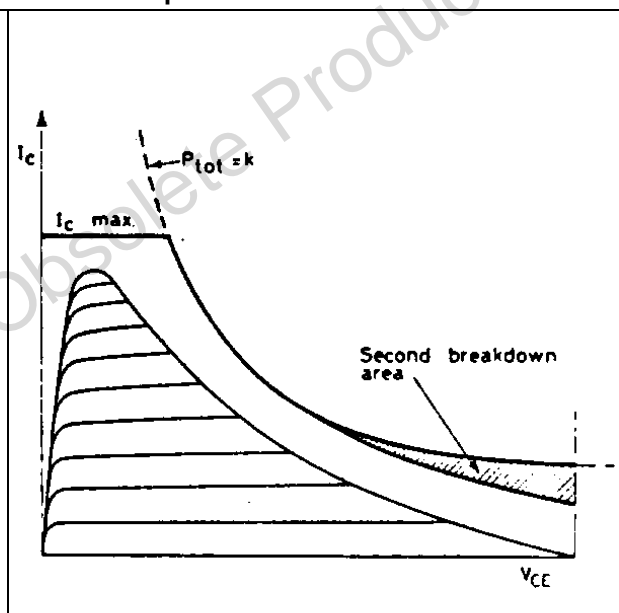
This function can therefore be considered as being peak power limiting rather than simple current limiting.

It reduces the possibility that the device gets damaged during an accidental short-circuit from AC output to ground.

**Figure 21. Maximum output current vs. voltage [ $V_{CEsat}$ ] across each output transistor**



**Figure 22. Safe operating area and collector characteristics of the protected power transistor**



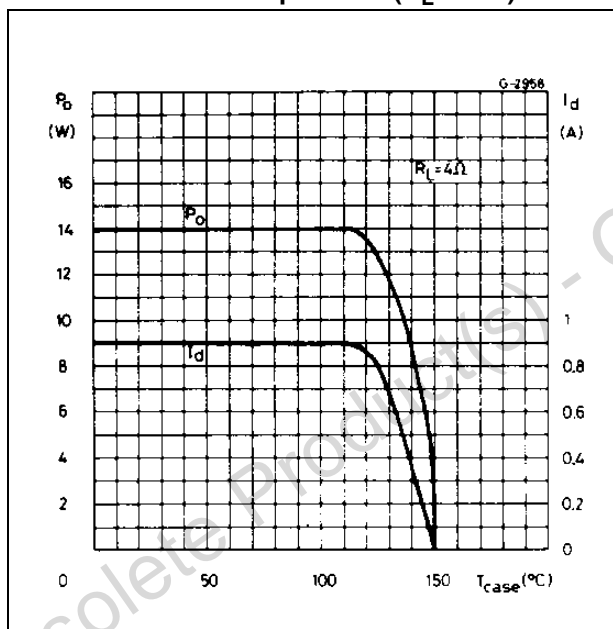
## 6 Thermal shutdown

The presence of a thermal limiting circuit offers the following advantages:

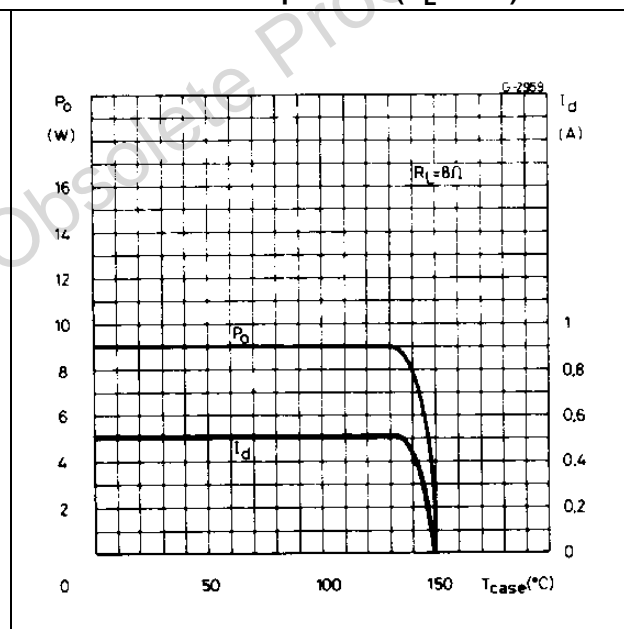
1. An overload on the output (even if it is permanent), or an above limit ambient temperature can be easily supported since  $T_j$  cannot be higher than  $150^\circ\text{C}$ .
2. The heatsink can have a smaller factor of safety compared with that of a conventional circuit. There is no possibility of device damage due to high junction temperature. If for any reason, the junction temperature increases to  $150^\circ\text{C}$ , the thermal shutdown simply reduces the power dissipation at the current consumption.

The maximum allowable power dissipation depends upon the size of the external heatsink (i.e. its thermal resistance); [Figure 25](#) shows this power dissipation as a function of ambient temperature for different thermal resistances.

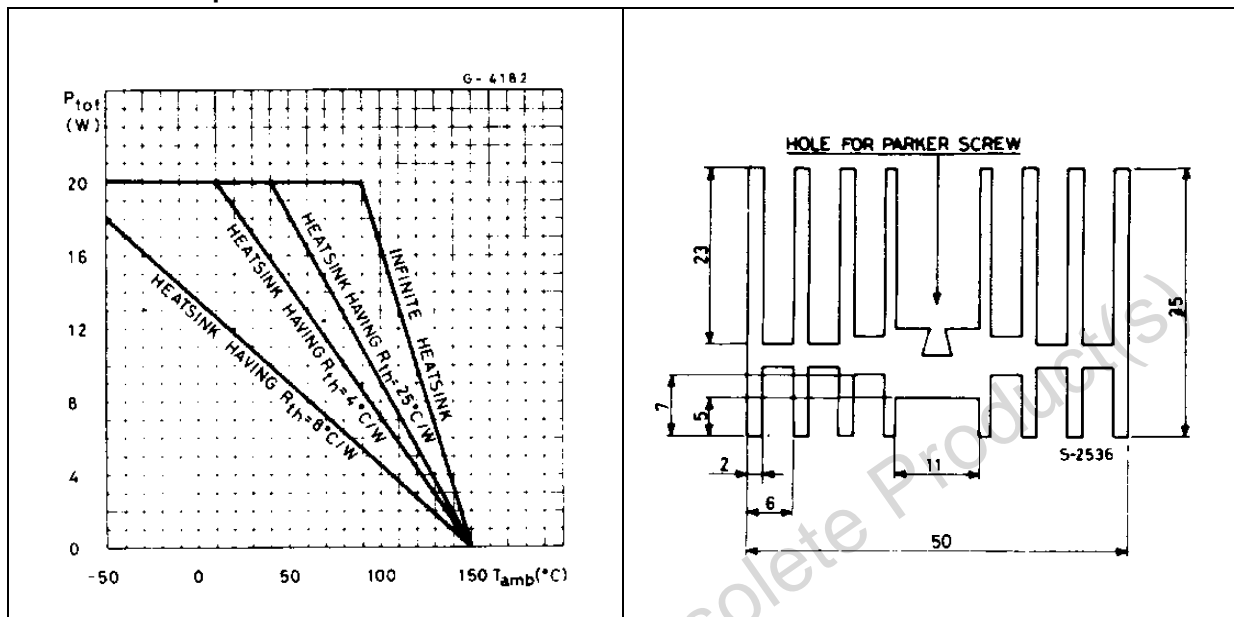
**Figure 23. Output power and drain current vs. case temperature ( $R_L = 4\ \Omega$ )**



**Figure 24. Output power and drain current vs. case temperature ( $R_L = 8\ \Omega$ )**



**Figure 26. Example of heatsink**



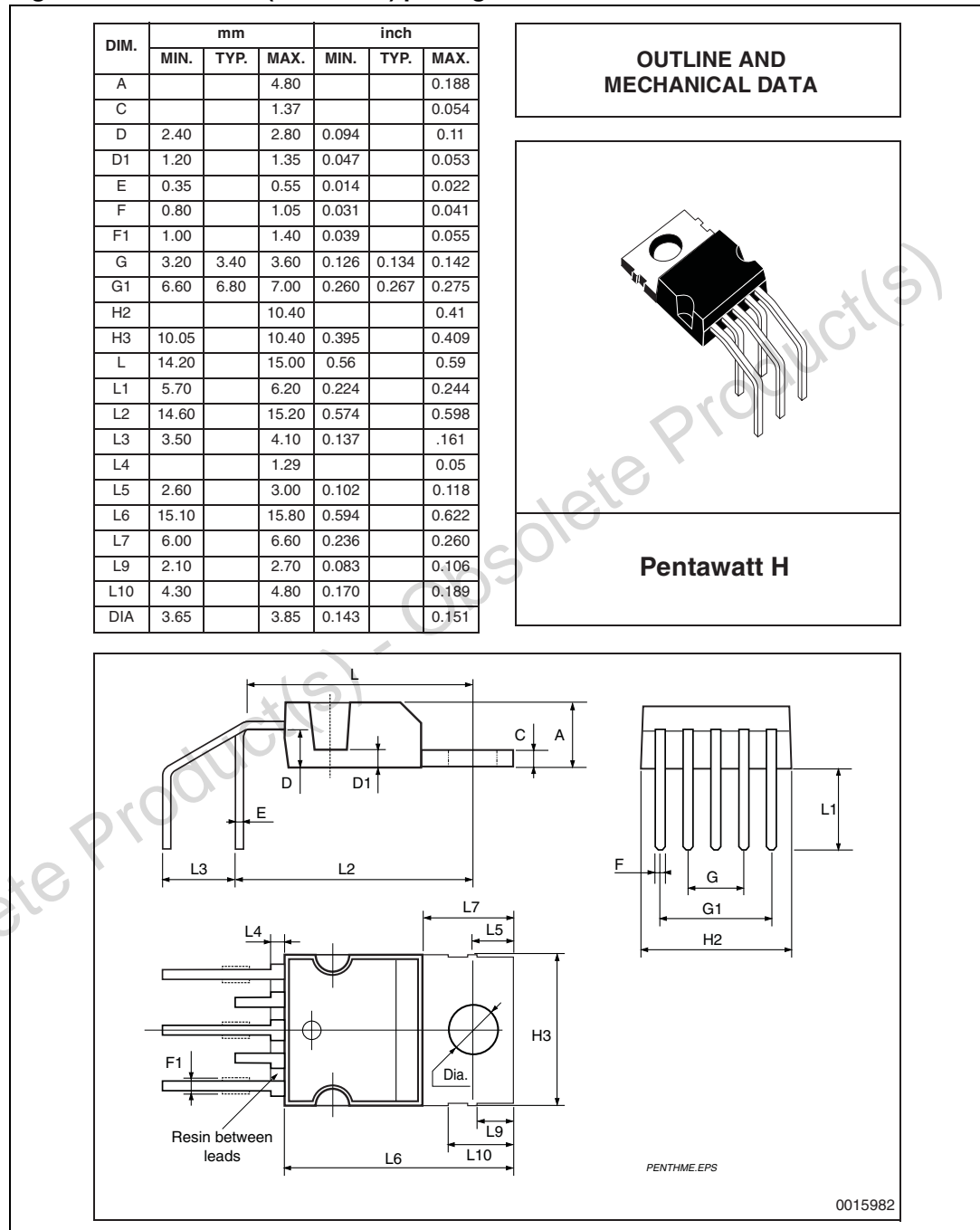
The following table shows the length that the heatsink in [Figure 26](#) must have for several values of  $P_{\text{tot}}$  and  $R_{\text{th}}$ .

**Table 7. Recommended values of heatsink**

Dimension	Recommended values			Unit
P <sub>tot</sub>	12	8	6	W
Length of heatsink	60	40	30	mm
R <sub>th</sub> of heatsink	4.2	6.2	8.3	°C/W

## 7 Package mechanical data

Figure 27. Pentawatt (horizontal) package outline and dimensions



In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK<sup>®</sup> is an ST trademark.

## 8 Revision history

**Table 8. Document revision history**

Date	Revision	Changes
June 1998	2	Second issue
21-Jun-2011	3	Added <i>Features on page 1</i> Removed Pentawatt (vertical) package option Replaced <i>Figure 27</i> with Pentawatt (horizontal) package data Updated presentation of document, minor textual changes



**Please Read Carefully:**

Information in this document is provided solely in connection with ST products. STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, modifications or improvements, to this document, and the products and services described herein at any time, without notice.

All ST products are sold pursuant to ST's terms and conditions of sale.

Purchasers are solely responsible for the choice, selection and use of the ST products and services described herein, and ST assumes no liability whatsoever relating to the choice, selection or use of the ST products and services described herein.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted under this document. If any part of this document refers to any third party products or services it shall not be deemed a license grant by ST for the use of such third party products or services, or any intellectual property contained therein or considered as a warranty covering the use in any manner whatsoever of such third party products or services or any intellectual property contained therein.

**UNLESS OTHERWISE SET FORTH IN ST'S TERMS AND CONDITIONS OF SALE ST DISCLAIMS ANY EXPRESS OR IMPLIED WARRANTY WITH RESPECT TO THE USE AND/OR SALE OF ST PRODUCTS INCLUDING WITHOUT LIMITATION IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE (AND THEIR EQUIVALENTS UNDER THE LAWS OF ANY JURISDICTION), OR INFRINGEMENT OF ANY PATENT, COPYRIGHT OR OTHER INTELLECTUAL PROPERTY RIGHT.**

**UNLESS EXPRESSLY APPROVED IN WRITING BY AN AUTHORIZED ST REPRESENTATIVE, ST PRODUCTS ARE NOT RECOMMENDED, AUTHORIZED OR WARRANTED FOR USE IN MILITARY, AIR CRAFT, SPACE, LIFE SAVING, OR LIFE SUSTAINING APPLICATIONS, NOR IN PRODUCTS OR SYSTEMS WHERE FAILURE OR MALFUNCTION MAY RESULT IN PERSONAL INJURY, DEATH, OR SEVERE PROPERTY OR ENVIRONMENTAL DAMAGE. ST PRODUCTS WHICH ARE NOT SPECIFIED AS "AUTOMOTIVE GRADE" MAY ONLY BE USED IN AUTOMOTIVE APPLICATIONS AT USER'S OWN RISK.**

Resale of ST products with provisions different from the statements and/or technical features set forth in this document shall immediately void any warranty granted by ST for the ST product or service described herein and shall not create or extend in any manner whatsoever, any liability of ST.

ST and the ST logo are trademarks or registered trademarks of ST in various countries.

Information in this document supersedes and replaces all information previously supplied.

The ST logo is a registered trademark of STMicroelectronics. All other names are the property of their respective owners.

© 2011 STMicroelectronics - All rights reserved

STMicroelectronics group of companies

Australia - Belgium - Brazil - Canada - China - Czech Republic - Finland - France - Germany - Hong Kong - India - Israel - Italy - Japan - Malaysia - Malta - Morocco - Philippines - Singapore - Spain - Sweden - Switzerland - United Kingdom - United States of America

[www.st.com](http://www.st.com)