National Semiconductor

May 1996

LMF60 High Performance 6th-Order Switched Capacitor Butterworth Lowpass Filter

General Description

The LMF60 is a high performance, precision, 6th-order Butterworth lowpass active filter. It is fabricated using National's LMCMOS process, an improved silicon-gate CMOS process specifically designed for analog products. Switched-capacitor techniques eliminate external component requirements and allow a clock-tunable cutoff frequency. The ratio of the clock frequency to the low-pass cutoff frequency is internally set to 50:1 (LMF60-50) or 100:1 (LMF60-100). A Schmitt trigger clock input stage allows two clocking options, either self-clocking (via an external resistor and capacitor) for stand-alone applications, or for tighter cutoff frequency control, a TTL or CMOS logic compatible clock can be directly applied. The maximally flat passband frequency response together with a DC gain of 1V/V allows cascading LMF60 sections for higher-order filtering. In addition to the filter, two independent CMOS op amps are included on the die and are useful for any general signal conditioning applications. The LMF60 is pin- and functionally-compatible with the MF6, but provides improved performance.

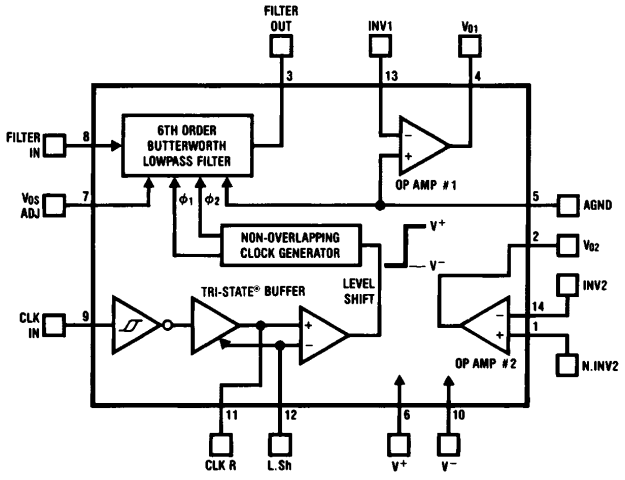
Features

- Cutoff frequency range of 0.1 Hz to 30 kHz
- Cutoff frequency accuracy of ±1.0%, maximum
- Low offset voltage ±100 mV, maximum, ±5V supply
- Low clock feedthrough of 10 mV_{p-p}, typical
- Dynamic range of 88 dB, typical
- Two uncommitted op amps available
- No external components required
- 14-pin DIP or 14-pin wide-body S.O. package
- Single/Dual Supply Operation: +4V to +14V (±2V to ±7V)
- Cutoff frequency set by external or internal clock
- Pin-compatible with the MF6

Applications

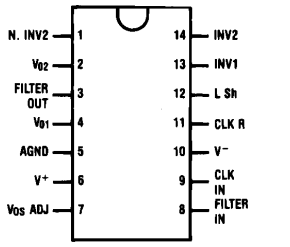
- Communication systems
- Audio filtering
- Anti-alias filtering
- Data acquisition noise filtering
- Instrumentation
- High-order tracking filters

Block and Connection Diagrams



TL/H/9294–1

All Packages



TL/H/9294–2

Top View

Order Number LMF60CMJ-50, (5962-9096 701MCA or LMF60CMJ50/883), LMF60CMJ-100, or (5962-9096 702MCA or LMF60CMJ100/883)
See NS Package Number J14A

Order Number LMF60CIWM-50 or LMF60CIWM-100
See NS Package Number M14B

Order Number LMF60CIN-50 or LMF60CIN-100
See NS Package Number N14A

TRI-STATE® is a registered trademark of National Semiconductor Corporation.

  RRD-B30M56/Printed in U. S. A.

Absolute Maximum Ratings (Note 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/Distributors for availability and specifications.

Supply Voltage ($V^+ - V^-$) (Note 2)	15V
Voltage at Any Pin	$V^+ + 0.2V$ $V^- - 0.2V$
Input Current at Any Pin (Note 3)	5 mA
Package Input Current (Note 3)	20 mA
Power Dissipation (Note 4)	500 mW
Storage Temperature	−65°C to +150°C
ESD Susceptibility (Note 5)	2000V
CLK IN Pin	1700V

Soldering Information:

• N Package: 10 sec.	260°C
• J Package: 10 sec.	300°C
• SO Package: Vapor Phase (60 sec.)	215°C
Infrared (15 sec.) (Note 6)	220°C

Operating Ratings (Note 1)

Temperature Range	$T_{Min} \le T_A \le T_{Max}$
LMF60CIN-50, LMF60CIN-100 LMF60CIJ-50, LMF60CIJ-100, LMF60CIWM-50, LMF60CIWM-100	$-40°C \le T_A \le +85°C$
LMF60CMJ-50, LMF60CMJ-100, LMF60CMJ50/883, LMF60CMJ100/883	$-55°C \le T_A \le +125°C$
Supply Voltage ($V^+ - V^-$)	4V to 14V

Filter Electrical Characteristics

The following specifications apply for f_{CLK} = 500 kHz (Note 7) unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter		Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
$V^+ = +5V, V^- = -5V$						
f_{CLK}	Clock Frequency Range (Note 16)			5	**1.5**	Hz (Min) MHz (Max)
I_S	Total Supply Current				7.0 / **12.0**	mA (Max)
	Clock Feedthrough		V_{IN} = 0V Filter Opamp	10 5		mVp-p mVp-p
H_o	DC Gain		$R_{Source} \le 2 k\Omega$		0.10 / **0.10** −0.26 / **−0.30**	dB (Max) dB (Min)
f_{CLK}/f_C	Clock to Cutoff Frequency Ratio (Note 10)	LMF60-50			49.00 ±0.8% / **49.00 ±1.0%**	(Max)
		LMF60-100			98.10 ±0.8% / **98.10 ±1.0%**	(Max)
	Temperature Coefficient of f_{CLK}/f_C			4		ppm/°C
A_{MIN}	Stopband Attenuation		At 2 × f_C		**36**	dB (Min)
V_{OS}	DC Offset Voltage	LMF60-50			**±100**	mV (Max)
		LMF60-100			**±150**	mV (Max)
V_{OUT}	Output Voltage Swing (Note 2)				+3.9 / **+3.7** −4.2 / **−4.0**	V (Min) V (Max)
I_{SC}	Output Short Circuit Current (Note 11)		Source Sink	90 2.2		mA mA
	Dynamic Range (Note 12)			88		dB
	Additional Magnitude Response Test Points (Note 13)	LMF60-50	f_{IN} = 12 kHz		−9.45 ±0.46 / **−9.45 ±0.50**	dB
			f_{IN} = 9 kHz		−0.87 ±0.16 / **−0.87 ±0.20**	dB
		LMF60-100	f_{IN} = 6 kHz		−9.30 ±0.46 / **−9.30 ±0.50**	dB
			f_{IN} = 4.5 kHz		−0.87 ±0.16 / **−0.87 ±0.20**	dB

Filter Electrical Characteristics (Continued)

The following specifications apply for f_{CLK} = 250 kHz (Note 7) unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J$ = 25°C.

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
V^+ = +2.5V, V^- = −2.5V					
f_{CLK}	Clock Frequency Range (Note 16)		5	**750**	Hz (Min) kHz (Max)
I_S	Total Supply Current			5.0 / **6.5**	mA (Max)
	Clock Feedthrough (Peak to Peak)	V_{IN} = 0V Filter Opamp	6 3		mV mV
H_o	DC Gain (with $R_{Source} \leq 2\ k\Omega$)	f_{CLK} = 250 kHz		0.10 / **0.10** −0.26 / **−0.30**	dB (Max) dB (Min)
		f_{CLK} = 500 kHz	−0.08		dB
f_{CLK}/f_C	Clock to Cutoff Frequency Ratio (Note 10) LMF60-50	f_{CLK} = 250 kHz		49.00 ±0.8% / **49.00 ± 1.0%**	(Max)
		f_{CLK} = 500 kHz	49.00 ±0.6%		
	LMF60-100	f_{CLK} = 250 kHz		98.10 ±0.8% / **98.10 ± 1.0%**	(Max)
		f_{CLK} = 500 kHz	98.10 ±0.6%		
	Temperature Coefficient of f_{CLK}/f_C		4		ppm/°C
A_{MIN}	Stopband Attenuation	At 2 × f_C		**36**	dB (Min)
V_{OS}	DC Offset Voltage LMF60-50			**±60**	mV (Max)
	LMF60-100			**±90**	mV (Max)
V_{OUT}	Output Voltage Swing (Note 2)	R_L = 5 kΩ		+1.4 / **+1.2** −2.0 / **−1.8**	V (Min) V (Max)
I_{SC}	Output Short Circuit Current (Note 11)	Source Sink	42 0.9		mA mA
	Dynamic Range (Note 12)		81		dB
	Additional Magnitude Response Test Points (Note 13) LMF60-50	f_{IN} = 6 kHz		−9.45 ±0.46 / **−9.45 ±0.50**	dB
		f_{IN} = 4.5 kHz		−0.87 ±0.16 / **−0.87 ±0.20**	dB
	LMF60-100	f_{IN} = 3 kHz		−9.30 ±0.46 / **−9.30 ±0.50**	dB
		f_{IN} = 2.25 kHz		−0.87 ±0.16 / **−0.87 ±0.20**	dB

Op Amp Electrical Characteristics

Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX}; all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
$V^+ = +5V, V^- = -5V$					
V_{OS}	Input Offset Voltage			**±20**	mV (Max)
I_B	Input Bias Current		10		pA
CMRR	Common Mode Rejection Ratio (Op Amp #2 Only)	Test Input Range = −2.2V to +1.8V		**55**	dB
V_O	Output Voltage Swing	$R_L = 5\ k\Omega$		3.8 / **3.6** −4.2 / **−4.0**	V (Min) V (Max)
I_{SC}	Output Short Circuit Current (Note 13)	Source Sink	90 2.1		mA mA
SR	Slew Rate		4		V/μs
A_{VOL}	DC Open Loop Gain		80		dB (Min)
GBW	Gain Bandwidth Product		2.0		MHz
$V^+ = +2.5V, V^- = -2.5V$					
V_{OS}	Input Offset Voltage			**±20**	mV (Max)
I_B	Input Bias Current		10		pA
CMRR	Common Mode Rejection Ratio (Op Amp #2 Only)	Test Input Range = −0.9V to +0.5V		**55**	dB
V_O	Output Voltage Swing	$R_L = 5\ k\Omega$		1.3 / **1.1** −1.8 / **−1.6**	V (Min) V (Max)
I_{SC}	Output Short Circuit Current (Note 13)	Source Sink	42 0.9		mA mA
SR	Slew Rate		3		V/μs
A_{VOL}	DC Open Loop Gain		74		dB (Min)
GBW	Gain Bandwidth Product		2.0		MHz

Logic Input-Output Characteristics

The following specifications apply for $V^- = 0V$ (Note 15), L.Sh = 0V unless otherwise specified. **Boldface limits apply for $T_A = T_J = T_{MIN}$ to T_{MAX};** all other limits $T_A = T_J = 25°C$.

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
TTL CLOCK INPUT, CLK R PIN (NOTE 14)					
V_{IH} V_{IL}	TTL Input Voltage Logical "1" Logical "0"	$V^+ = +5V, V^- = -5V$		**2.0** **0.8**	V (Min) V (Max)
V_{IH} V_{IL}	CLK R Input Voltage Logical "1" Logical "0"	$V^+ = +2.5V, V^- = -2.5V$		**2.0** 0.6 / **0.4**	V (Min) V (Max)
	Maximum Leakage Current at CLK R		2.0		μA

Logic Input-Output Characteristics (Continued)

The following specifications apply for V^- = 0V (Note 15), L.Sh = 0V unless otherwise specified. **Boldface limits apply for T_A = T_J = T_{MIN} to T_{MAX};** all other limits T_A = T_J = 25°C.

Symbol	Parameter	Conditions	Typical (Note 8)	Limits (Note 9)	Units (Limits)
SCHMITT TRIGGER					
V_{T+}	Positive Going Input Threshold Voltage	V^+ = 10V		6.1 / **6.0** 8.8 / **8.9**	V (Min) V (Max)
		V^+ = 5V		3.0 / **2.9** 4.3 / **4.4**	V (Min) V (Max)
V_{T-}	Negative Going Input Threshold Voltage	V^+ = 10V		1.4 / **1.3** 3.8 / **3.9**	V (Min) V (Max)
		V^+ = 5V		0.7 / **0.6** 1.9 / **2.0**	V (Min) V (Max)
$V_{T+} - V_{T-}$	Hysteresis	V^+ = 10V		2.3 / **2.1** 7.4 / **7.6**	V (Min) V (Max)
		V^+ = 5V		1.1 / **0.9** 3.6 / **3.8**	V (Min) V (Max)
V_{OH}	Logical "1" Voltage I_O = −10 μA, Pin 11	V^+ = +10V V^+ = +5V		9.1 / **9.0** 4.6 / **4.5**	V (Min) V (Min)
V_{OL}	Logical "0" Voltage I_O = −10 μA, Pin 11	V^+ = +10V V^+ = +5V		0.9 / **1.0** 0.4 / **0.5**	V (Max) V (Max)
I_{SOURCE}	Output Source Current, Pin 11	CLK R to V^- V^+ = +10V V^+ = +5V		 4.9 / **3.7** 1.6 / **1.2**	 mA (Min) mA (Min)
I_{SINK}	Output Sink Current, Pin 11	CLK R to V^+ V^+ = +10V V^+ = +5V		 4.9 / **3.7** 1.6 / **1.2**	 mA (Min) mA (Min)

Note 1: Absolute Maximum Ratings indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional. Specified Electrical Characteristics do not apply when operating the device outside its specified conditions.

Note 2: All voltages are measured with respect to AGND, unless otherwise specified.

Note 3: When the input voltage (V_{IN}) at any pin exceeds the power supply rails ($V_{IN} < V^-$ or $V_{IN} > V^+$) the absolute value of current at that pin should be limited to 5 mA or less. The 20 mA package input current limits the number of pins that can exceed the power supply boundaries with 5 mA to four.

Note 4: The Maximum power dissipation must be derated at elevated temperatures and is dictated by $T_{J\,Max}$, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is PD = $(T_{J\,Max} - T_A)/\theta_{JA}$ or the number given in the absolute ratings, whichever is lower. For this device, $T_{J\,Max}$ = 125°C, and the typical junction-to-ambient thermal resistance of the LMF60CCN when board mounted is 67°C/W. For the LMF60CIJ this number decreases to 62°C/W. For the LMF60CIWM, θ_{JA} = 78°C/W.

Note 5: Human body model: 100 pF discharged through a 1.5 kΩ resistor.

Note 6: See AN450 "Surface Mounting Methods and Their Effect on Product Reliability" or the section titled "Surface Mount" found in any current Linear Databook for other methods of soldering surface mount devices.

Note 7: The specifications given are for a clock frequency (f_{CLK}) of 500 kHz at +5V and 250 kHz at ±2.5V. Above this frequency, the cutoff frequency begins to deviate from the specified error band over the temperature range but the filter still maintains its amplitude characteristics. See application hints.

Note 8: Typicals are at 25°C and represent the most likely parametric norm.

Note 9: Guaranteed to National's Average Outgoing Quality Level (AOQL).

Note 10: The cutoff frequency of the filter is defined as the frequency where the magnitude response is 3.01 dB less than the DC gain of the filter.

Note 11: The short circuit source current is measured by forcing the output to its maximum positive swing and then shorting that output to the negative supply. The short circuit sink current is measured by forcing the output being tested to its maximum negative voltage and then shorting that output to the positive supply. These are worst case conditions.

Note 12: For ±5V supplies the dynamic range is referenced to 2.62 V_{rms} (3.7V peak), where the wideband noise over a 20 kHz bandwidth is typically 100 μV. For ±2.5V supplies the dynamic range is referenced to 0.849 V_{rms} (1.2V peak), where the wideband noise over a 20 kHz bandwidth is typically 75 μV_{rms}.

Note 13: The filter's magnitude response is tested at the cutoff frequency, f_C, at $f_{IN} = 2\,f_C$, and at these two additional frequencies.

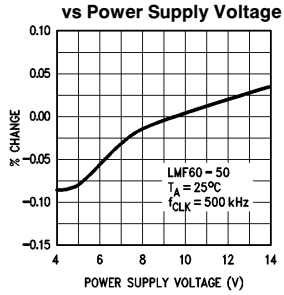
Note 14: The LMF60 is operated with symmetrical supplies and L.Sh is tied to GND.

Note 15: For simplicity all the logic levels (except for the TTL input logic levels) have been referenced to V^- = 0V. The logic levels will scale accordingly for ±5V and ±2.5V supplies.

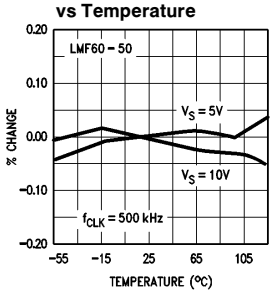
Note 16: The nominal ratio of the clock frequency to the low-pass cutoff frequency is internally set to 50-to-1 (LMF60-50) or 100-to-1 (LMF60-100).

Typical Performance Characteristics

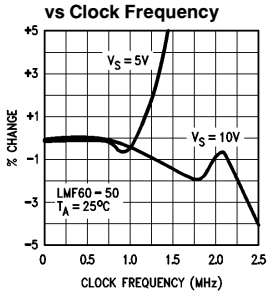
f_{CLK}/f_C Deviation vs Power Supply Voltage



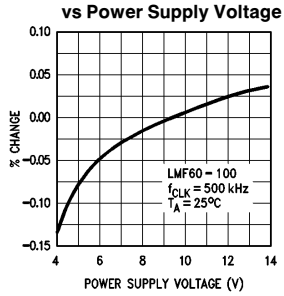
f_{CLK}/f_C Deviation vs Temperature



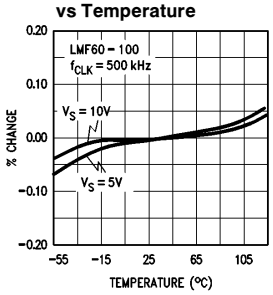
f_{CLK}/f_C Deviation vs Clock Frequency



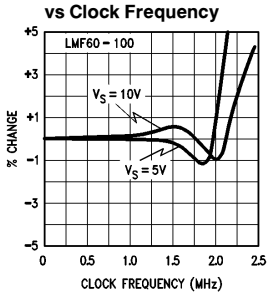
f_{CLK}/f_C Deviation vs Power Supply Voltage



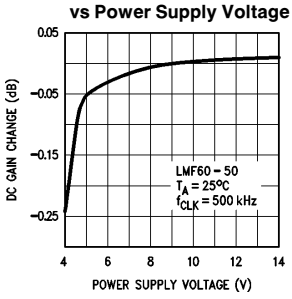
f_{CLK}/f_C Deviation vs Temperature



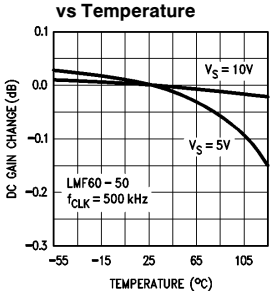
f_{CLK}/f_C Deviation vs Clock Frequency



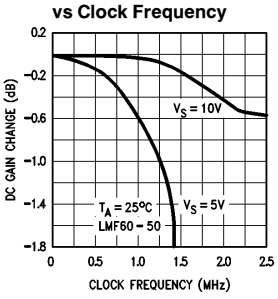
DC Gain Deviation vs Power Supply Voltage



DC Gain Deviation vs Temperature



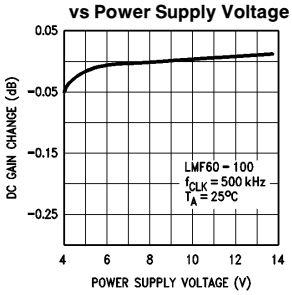
DC Gain Deviation vs Clock Frequency



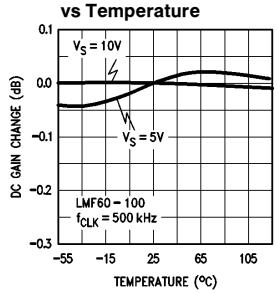
TL/H/9294–3

Typical Performance Characteristics (Continued)

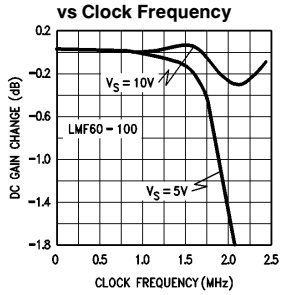
DC Gain Deviation vs Power Supply Voltage



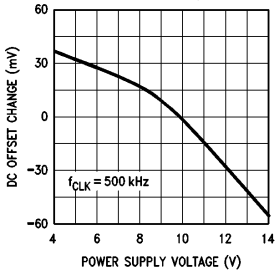
DC Gain Deviation vs Temperature



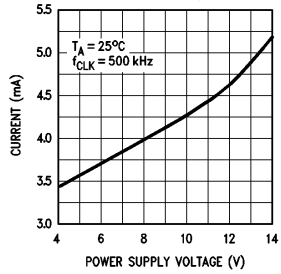
DC Gain Deviation vs Clock Frequency



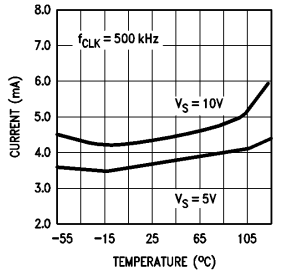
DC Offset Voltage Deviation vs Power Supply Voltage



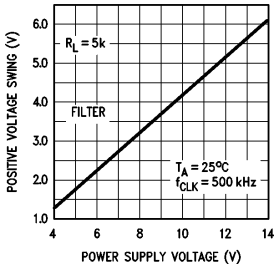
Power Supply Current vs Power Supply Voltage



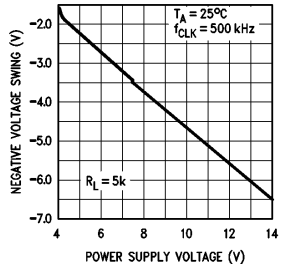
Power Supply Current vs Temperature



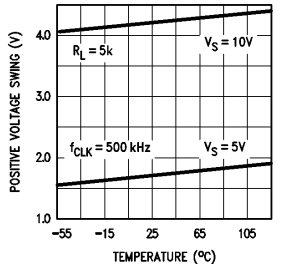
Positive Voltage Swing vs Power Supply Voltage



Negative Voltage Swing vs Power Supply Voltage



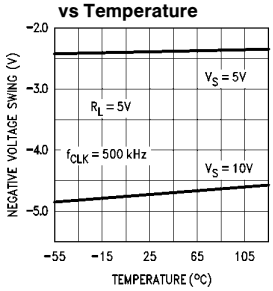
Positive Voltage Swing vs Temperature



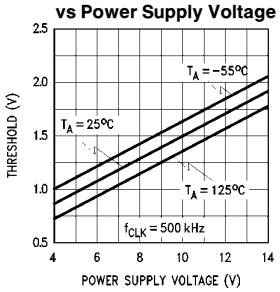
TL/H/9294–4

Typical Performance Characteristics (Continued)

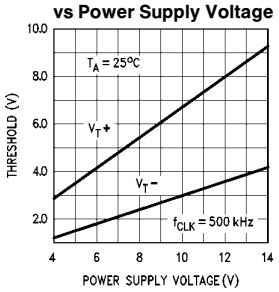
Negative Voltage Swing vs Temperature



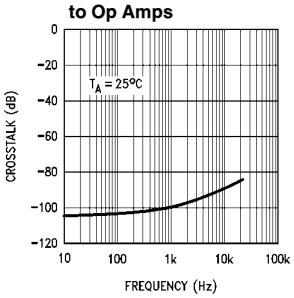
CLK R Trigger Threshold vs Power Supply Voltage



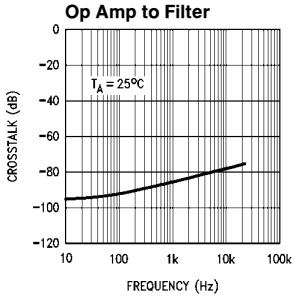
Schmitt Trigger Threshold vs Power Supply Voltage



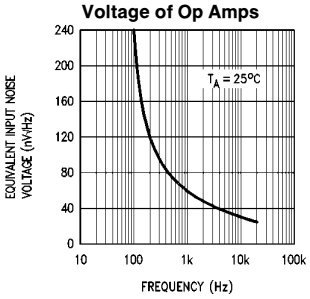
Crosstalk from Filter to Op Amps



Crosstalk from Either Op Amp to Filter



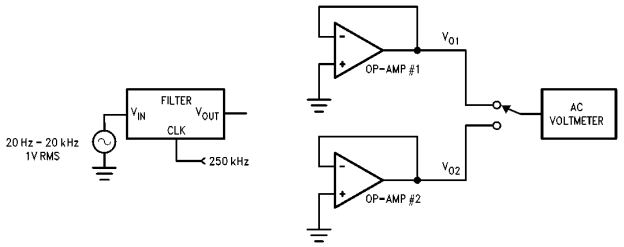
Equivalent Input Noise Voltage of Op Amps



TL/H/9294–5

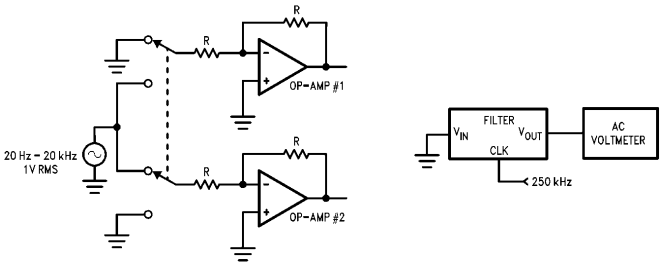
Crosstalk Test Circuits

From Filter to Op-Amps



TL/H/9294–6

From Either Op-Amp to Filter Output



TL/H/9294–7

Pin Description (Pin Numbers)

Pin	Description
FILTER OUT (3)	The output of the lowpass filter will typically swing to within 1V of each supply rail.
FILTER IN (8)	The input to the lowpass filter. To minimize gain errors the source impedance that drives this input should be less than 2k (See Section 1.4). For single supply operation the input signal must be biased to mid-supply or AC coupled.
V_{OS}ADJ (7)	This pin is used to adjust the DC offset of the filter output; if not used it must be tied to the AGND potential. (See Section 1.3)
AGND (5)	The analog ground pin. This pin sets the DC bias level for the filter section and the noninverting input of Op-Amp #1 and must be tied to the system ground for split supply operation or to mid-supply for single supply operation (See Section 1.2). When tied to mid-supply this pin should be well bypassed.
V_{O1}(4), INV1 (13)	V_{O1} is the output and INV1 is the inverting input of Op-Amp #1. The non-inverting input of this Op-Amp is internally connected to the AGND pin.
V_{O2}(2), INV2 (14), NINV2 (1)	V_{O2} is the output, INV2 is the inverting input, and NINV2 is the non-inverting input of Op-Amp #2.
V^+ (6), V^- (10)	The positive and negative supply pins. The total power supply range is 4V to 14V. Decoupling these pins with 0.1 μF capacitors is highly recommended.
CLK IN (9)	A CMOS Schmitt-trigger input to be used with an external CMOS logic level clock. Also used for self-clocking Schmitt-trigger oscillator (See Section 1.1).
CLK R (11)	A TTL logic level clock input when in split supply operation ($\pm$2V to $\pm$7V) and L. Sh tied to system ground. This pin becomes a low impedance output when L.Sh is tied to V^-. Also used in conjunction with the CLK IN pin for self clocking Schmitt-trigger oscillator (See Section 1.1).
L.Sh (12)	Level shift pin, selects the logic threshold levels for the desired clock. When tied to V^- it enables an internal TRI-STATE® buffer stage between the Schmitt trigger and the internal clock level shift stage thus enabling the CLK IN Schmitt-trigger input and making the CLK R pin a low impedance output. When the voltage level at this input exceeds [25% ($V^+ - V^-$) + V^-] the internal TRI-STATE® buffer is disabled allowing the CLK R pin to become the clock input for the internal clock level shift stage. The CLK R threshold level is now 2V above the voltage applied to the L.Sh pin. Driving the CLK R pin with TTL logic levels can be accomplished through the use of split supplies and by tying the L.Sh pin to system ground.

1.0 LMF60 Application Hints

The LMF60 is comprised of a non-inverting unity gain lowpass sixth-order Butterworth switched capacitor filter section and two undedicated CMOS Op-Amps. The switched-capacitor topology makes the cutoff frequency (where the gain drops 3.01 dB below the DC gain) a direct ratio (100:1 or 50:1) of the clock frequency supplied to the lowpass filter. Internal integrator time constants set the filter's cutoff frequency. The resistive element of these integrators is actually a capacitor which is ''switched'' at the clock frequency (for a detailed discussion see Input Impedance section). Varying the clock frequency changes the value of this resistive element and thus the time constant of the integrators. The clock to cutoff frequency ratio (f_{CLK}/f_C) is set by the ratio of the input and feedback capacitors in the integrators. The higher the clock to cutoff frequency ratio (or the sampling rate) the closer the approximation is to the theoretical Butterworth response. The LMF60 is available in f_{CLK}/f_C ratios of 50:1 (LMF60-50) or 100:1 (LMF60-100).

1.1 CLOCK INPUTS

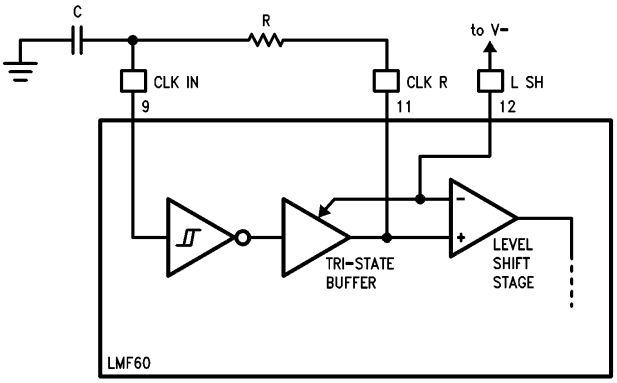
The LMF60 has a Schmitt-trigger inverting buffer which can be used to construct a simple R/C oscillator. The oscillator frequency is dependent on the buffer's threshold levels as well as on the resistor/capacitor tolerance (See *Figure 1*).

Schmitt-trigger threshold voltage levels can vary significantly causing the R/C oscillator's frequency to vary greatly from part to part.

Where accuracy in f_C is required an external clock can be used to drive the CLK R input of the LMF60. This input is TTL logic level compatible and also presents a very light load to the external clock source ($\sim 2\ \mu A$) with split supplies and L.Sh tied to system ground. The logic level is programmed by the voltage applied to level shift (L.Sh) pin (See the Pin Description for L.Sh pin).

1.2 POWER SUPPLY BIASING

The LMF60 can be biased from a single supply or dual split supplies. The split supply mode shown in *Figures 2* and *3* is the most flexible and easiest to implement. As discussed earlier split supplies, $\pm 2V$ to $\pm 7V$, will enable the use of TTL or CMOS clock logic levels. *Figure 4* shows two schemes for single supply biasing. In this mode only CMOS clock logic levels can be used.



TL/H/9294–8

FIGURE 1. Schmitt Trigger R/C Oscillator

$$f_{CLK} = \frac{1}{RC \ln\left[\left(\frac{V_{CC} - V_{T-}}{V_{CC} - V_{T+}}\right)\frac{V_{T+}}{V_{T-}}\right]}$$

Typically for $V_{CC} = V^+ - V^- = 10V$:

$$f_{CLK} = \frac{1}{1.37\ RC}$$

1.0 LMF60 Application Hints (Continued)

If the LMF60-50 or the LMF60-100 were set up for a cutoff frequency of 10 kHz the input impedance would be:

$$R_{IN} = \frac{1 \times 10^{10}}{10\ \text{kHz}} = 1\ \text{M}\Omega$$

In this example with a source impedance of 10k the overall gain, if the LMF60 had an ideal gain of 1 (0 dB) would be:

$$A_V = \frac{1\ \text{M}\Omega}{10\ \text{k}\Omega + 1\ \text{M}\Omega} = 0.99009\ (-86.4\ \text{mdB})$$

Since the maximum overall gain error for the LMF60 is +0.1 dB, −0.3 dB with a $R_S \leq 2\ \text{k}\Omega$ the actual gain error for this case would be +0.21 dB to −0.39 dB.

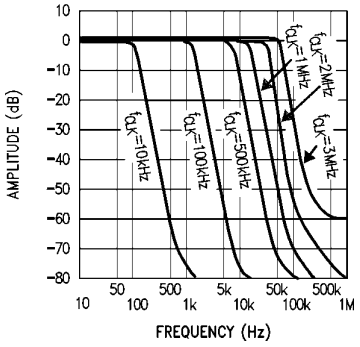
1.5 CUTOFF FREQUENCY RANGE

The filter's cutoff frequency (f_C) has a lower limit caused by leakage currents through the internal switches discharging the stored charge on the capacitors. At lower clock frequencies these leakage currents can cause millivolts of error, for example:

$$f_{CLK} = 100\ \text{Hz},\ I_{LEAKAGE} = 1\ \text{pA},\ C = 1\ \text{pF}$$

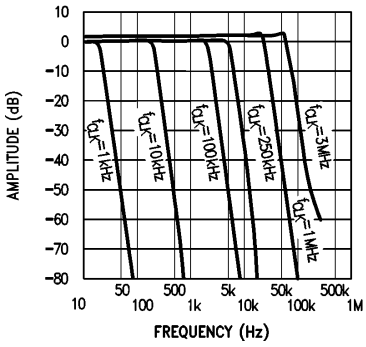
$$V = \frac{1\ \text{pA}}{1\ \text{pF (100 Hz)}} = 10\ \text{mV}$$

The propagation delay in the logic and the settling time required to acquire a new voltage level on the capacitors increases as the LMF60 power supply voltage decreases. This causes a shift in the f_{CLK}/f_C ratio which will become noticeable when the clock frequency exceeds 500 kHz. The amplitude characteristic will stay within tolerance until f_{CLK} exceeds 750 kHz and will peak at about 0.4 dB at the cutoff frequency with a 2 MHz clock. The response of the LMF60 is still a reasonable approximation of the ideal Butterworth lowpass characteristic as can be seen in *Figure 7*.



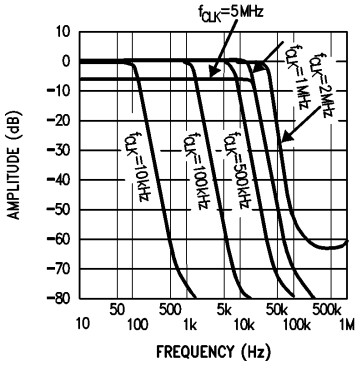
TL/H/9294–17

FIGURE 7a. LMF60-100 ±5V Supplies Amplitude Response



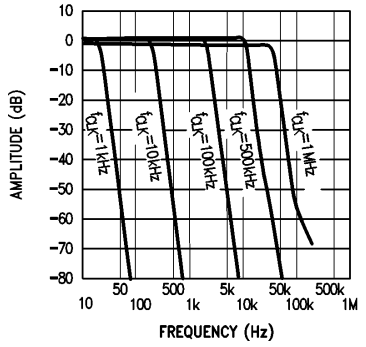
TL/H/9294–18

FIGURE 7b. LMF60-50 ±5V Supplies Amplitude Response



TL/H/9294–19

FIGURE 7c. LMF60-100 ±2.5V Supplies Amplitude Response



TL/H/9294–20

FIGURE 7d. LMF60-50 ±2.5V Supplies Amplitude Response

1.0 LMF60 Application Hints (Continued)

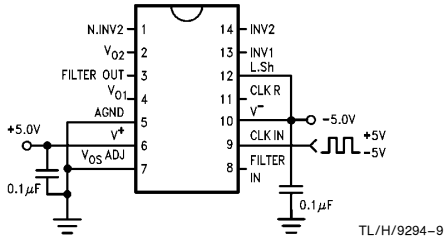


FIGURE 2. Dual Supply Operation LMF60 Driven with CMOS Logic Level Clock ($V_{IH} \geq V^+ - 0.3\ V_S$ and $V_{IL} \leq V^- + 0.3\ V_S$ where $V_S = V^+ - V^-$)

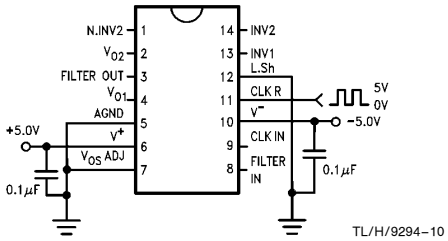
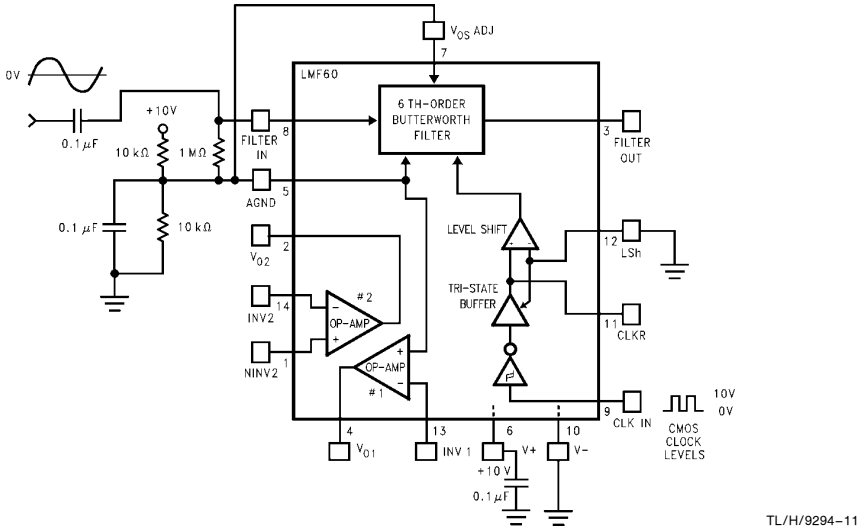
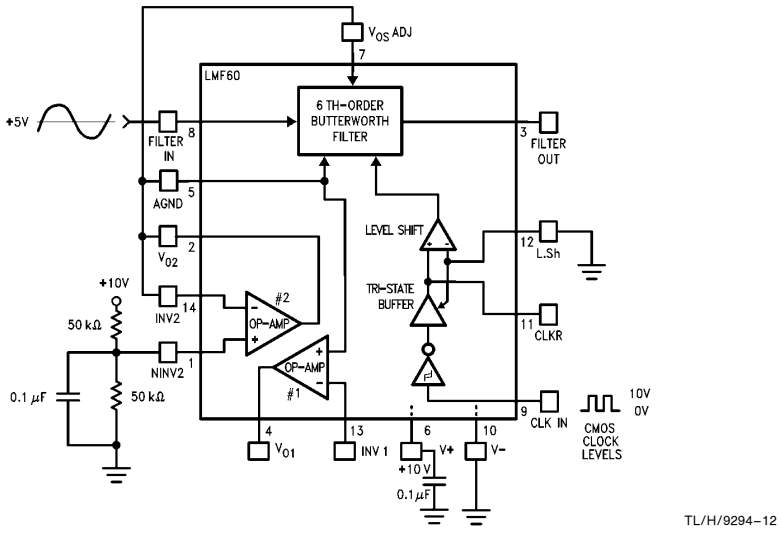


FIGURE 3. Dual Supply Operation LMF60 Driven with TTL Logic Level Clock



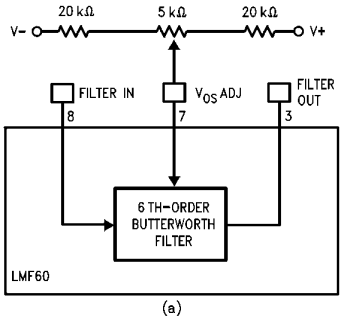
a) Resistor Biasing of AGND



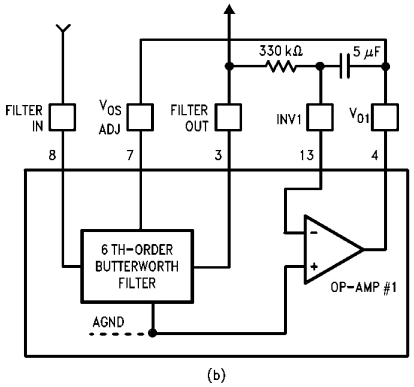
b) Using Op-Amp 2 to Buffer AGND

FIGURE 4. Single Supply Operation

1.0 LMF60 Application Hints (Continued)



TL/H/9294–13



TL/H/9294–14

FIGURE 5. V_{OS} Adjust Schemes

1.3 OFFSET ADJUST

The V_{OS}ADJ pin is used in adjusting the output offset level of the filter section. If this pin is not used it must be tied to the analog ground (AGND) level, either mid-supply for single ended supply operation or ground for split supply operation. This pin sets the zero reference for the output of the filter. The implementation of this pin can be seen in *Figure 5*. In *5(a)* DC offset is adjusted using a potentiometer; in *5(b)* the Op-Amp integrator circuit keeps the average DC output level at AGND. The circuit in *5(b)* is therefore appropriate only for AC-coupled signals and signals biased at AGND.

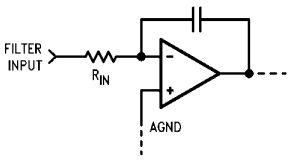
1.4 INPUT IMPEDANCE

The LMF60 lowpass filter input (FILTER IN pin) is not a high impedance buffer input. This input is a switched capacitor resistor equivalent, and its effective impedance is inversely proportional to the clock frequency. The equivalent circuit of the input to the filter can be seen in *Figure 6*. The input capacitor charges to the input voltage (V_{IN}) during one half of the clock period, during the second half the charge is transferred to the feedback capacitor. The total transfer of charge in one clock cycle is therefore $Q = C_{IN}V_{IN}$, and since current is defined as the flow of charge per unit time the average input current becomes

$$I_{IN} = Q/T$$

(where T equals one clock period) or

$$I_{IN} = \frac{C_{IN}V_{IN}}{T} = C_{IN}V_{IN}f_{CLK}$$



TL/H/9294–15

a) Equivalent Circuit for LMF60 Filter Input

The equivalent input resistor (R_{IN}) then can be defined as

$$R_{IN} = V_{IN}/I_{IN} = \frac{1}{C_{IN}f_{CLK}}$$

The input capacitor is 2 pF for the LMF60-50 and 1 pF for the LMF60-100, so for the LMF60-100

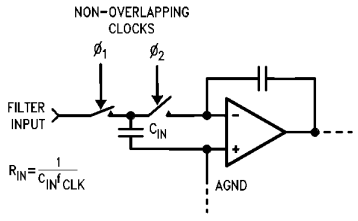
$$R_{IN} = \frac{1 \times 10^{12}}{f_{CLK}} = \frac{1 \times 10^{12}}{f_C \times 100} = \frac{1 \times 10^{10}}{f_C}$$

and

$$R_{IN} = \frac{5 \times 10^{11}}{f_{CLK}} = \frac{5 \times 10^{11}}{f_C \times 50} = \frac{1 \times 10^{10}}{f_C}$$

for the LMF60-50. As shown in the above equations, for a given cutoff frequency (f_C) the input impedance remains the same for the LMF60-50 and the LMF60-100. The higher the clock to cutoff frequency ratio, the greater equivalent input resistance for a given clock frequency. As the cutoff frequency increases the equivalent input impedance decreases. This input resistance will form a voltage divider with the source impedance (R_{SOURCE}). Since R_{IN} is inversely proportional to the cutoff frequency, operation at higher cutoff frequencies will be more likely to load the input signal which would appear as an overall decrease in gain at the output of the filter. Since the filter's ideal gain is unity, its overall gain is given by:

$$A_V = \frac{R_{IN}}{R_{IN} + R_{SOURCE}}$$



TL/H/9294–16

b) Actual Circuit for LMF60 Filter Input

FIGURE 6. LMF60 Filter Input

2.0 Designing with the LMF60

Given any lowpass filter specification, two equations will come in handy in trying to determine whether the LMF60 will do the job. The first equation determines the order of the lowpass filter required:

$$n = \frac{\log\left(10^{0.1A_{Min}} - 1\right) - \log\left(10^{0.1A_{Max}} - 1\right)}{2\log\left(f_s/f_b\right)} \quad (1)$$

where n is the order of the filter, A_{Min} is the minimum stopband attenuation (in dB) desired at frequency f_s, and A_{Max} is the passband ripple or attenuation (in dB) at frequency f_b. If the result of this equation is greater than 6, then more than a single LMF60 is required.

The attenuation at any frequency can be found by the following equation:

$$\text{Attn}(f) = 10\log\left[1 + \left(10^{0.1A_{Max}} - 1\right)(f/f_b)^{2n}\right]\text{dB} \quad (2)$$

where $n = 6$ (the order of the filter).

2.1 A LOWPASS DESIGN EXAMPLE

Suppose the amplitude response specification in *Figure 8* is given. Can the LMF60 be used? The order of the Butterworth approximation will have to be determined using eq. 1:

$A_{Min} = 30$ dB, $A_{Max} = 1.0$ dB, $f_s = 2$ kHz, and $f_b = 1$ kHz

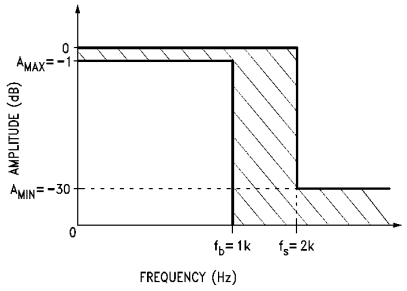
$$n = \frac{\log(10^3 - 1) - \log(10^{0.1} - 1)}{2\log(2)} = 5.96$$

Since n can only take on integer values, $n = 6$. Therefore the LMF60 can be used. In general, if n is 6 or less a single LMF60 stage can be utilized.

Likewise, the attenuation at f_s can be found using equation 2 with the above values and $n = 6$ giving:

$$\text{Atten (2 kHz)} = 10\log\left[1 + \left(10^{0.1} - 1\right)(2/1)^{12}\right]$$
$$= 30.26\text{ dB}$$

This result also meets the design specification given in *Figure 8* again verifying that a single LMF60 section will be adequate.



TL/H/9294–21

FIGURE 8. Design Example Magnitude Response Specification Where the Response of the Filter Design Must Fall Within the Shaded Area of the Specification

Since the LMF60's cutoff freqency f_C, which corresponds to a gain attenuation of −3.01 dB, was not specified in this example it needs to be calculated. Solving equation 2 where $f = f_C$ as follows:

$$f_c = f_b\left[\frac{10^{0.1(3.01\text{ dB})} - 1)}{(10^{0.1A_{Max}} - 1)}\right]^{1/(2n)}$$
$$= 1\left(\frac{10^{0.301} - 1}{10^{0.1} - 1}\right)^{1/12}$$
$$= 1.119\text{ kHz}$$

where $f_C = f_{CLK}/50$ or $f_{CLK}/100$.

To implement this example for the LMF60-50 the clock frequency will have to be set to $f_{CLK} = 50(1.119\text{ kHz}) = 55.95$ kHz or for the LMF60-100 $f_{CLK} = 100(1.119\text{ kHz}) = 111.9$ kHz

2.2 CASCADING LMF60s

In the case where a steeper stopband attenuation rate is required two LMF60's can be cascaded *(Figure 9)* yielding a 12th order slope of 72 dB per octave. Because the LMF60 is a Butterworth filter and therefore has no ripple in its passband, when LMF60's are cascaded the resulting filter also has no ripple in its passband. Likewise the DC and passband gains will remain at 1V/V. The resulting response is shown in *Figure 10*.

In determining whether the cascaded LMF60's will yield a filter that will meet a particular amplitude response specification, as above, equations 3 and 4 can be used, shown below.

$$n = \frac{\log\left(10^{0.05\,A_{min}} - 1\right) - \log\left(10^{0.05\,A_{Max}} - 1\right)}{2\log\left(f_s/f_b\right)} \quad (3)$$

$$\text{Attn}(f) = 10\log\left[1 + \left(10^{0.05\,A_{Max}} - 1\right)(f/f_b)^{2n}\right]\text{ dB} \quad (4)$$

where $n = 6$ (the order of each filter).

Equation 3 will determine whether the order of the filter is adequate ($n \leq 6$) while equation 4 can determine if the required stopband attenuation is met and what actual cutoff frequency (f_C) is required to obtain the particular frequency response desired. The design procedure would be identical to the one shown in Section 2.1.

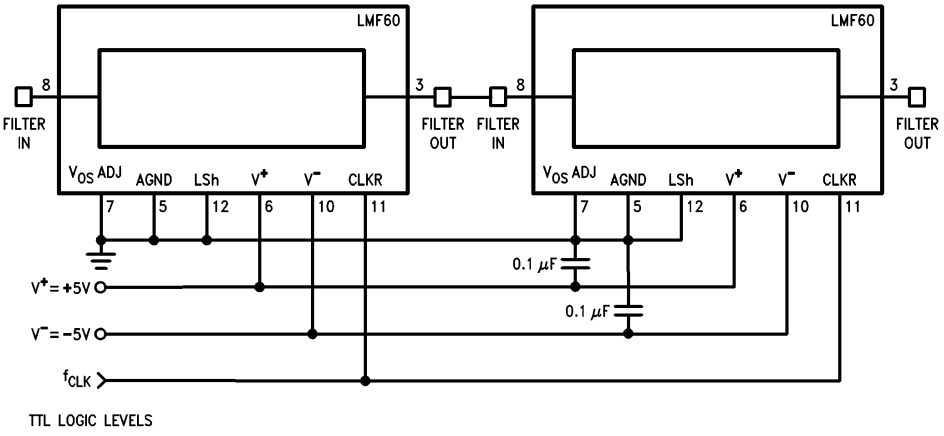
2.3 IMPLEMENTING A "NOTCH" FILTER WITH THE LMF60

A "notch" filter with 60 dB of attenuation can be obtained by using one of the Op-Amps available in the LMF60 and three external resistors. The circuit and amplitude response are shown in *Figure 11*.

The frequency where the "notch" will occur is equal to the frequency at which the output signal of the LMF60 will have the same magnitude but be 180 degrees out of phase with its input signal. For a sixth order Butterworth filter 180° phase shift occurs where $f = f_n = 0.742\ f_C$. The attenuation at this frequency is 0.12 dB which must be compensated for by making $R_1 = 1.014 \times R_2$.

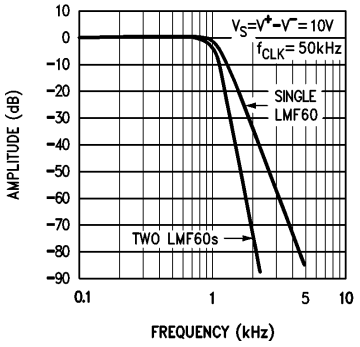
Since R_1 does not equal R_2 there will be a gain inequality above and below the notch frequency. At frequencies below the notch frequency ($f \ll f_n$), the signal through the filter has a gain of one and is non-inverting. Summing this with the input signal through the Op-Amp yields an overall gain of two or +6 dB. For $f \gg f_n$, the signal at the output of the filter is greatly attenuated thus only the input signal will appear at the output of the Op-Amp. With $R_3 = R_1 = 1.014\ R_2$ the overall gain is 0.986 or −0.12 dB at frequencies above the notch.

2.0 Designing with the LMF60 (Continued)



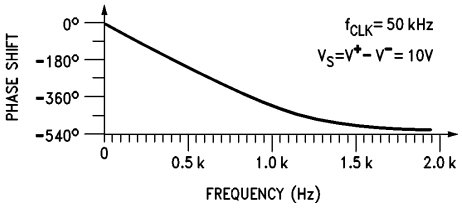
TL/H/9294–22

FIGURE 9. Cascading Two LMF60s



TL/H/9294–23

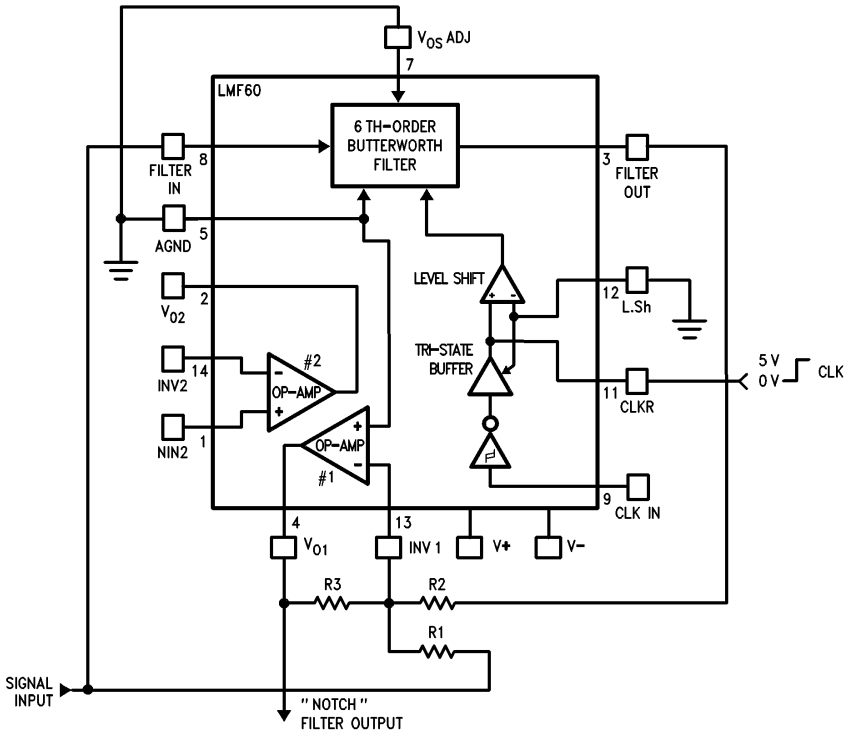
FIGURE 10a. One LMF60-50 vs. Two LMF60-50s Cascaded



TL/H/9294–24

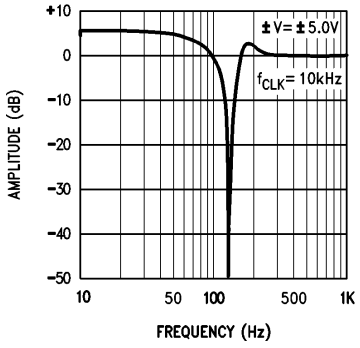
FIGURE 10b. Phase Response of Two Cascaded LMF60-50s

2.0 Designing with the LMF60 (Continued)



TL/H/9294–25

FIGURE 11a. "Notch" Filter



TL/H/9294–26

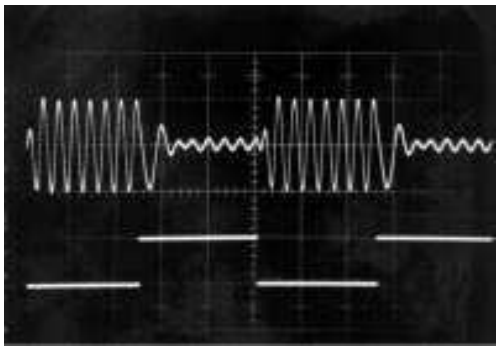
FIGURE 11b. LMF60-50 "Notch" Filter Amplitude Response

2.0 Designing with the LMF60 (Continued)

2.4 CHANGING CLOCK FREQUENCY INSTANTANEOUSLY

The LMF60 will respond well to a sudden change in clock frequency. Distortion in the output signal occurs at the transition of the clock frequency and lasts approximately three cutoff frequency (f_C) cycles. As shown in *Figure 12*, if the control signal is low the LMF60-50 has a 100 kHz clock making $f_C = 2$ kHz; when this signal goes high the clock frequency changes to 50 kHz yielding 1 kHz f_C.

The transient response of the LMF60 seen in *Figure 13* is also dependent on the f_c and thus the f_{CLK} applied to the filter. The LMF60 responds as a classical sixth order Butterworth lowpass filter.



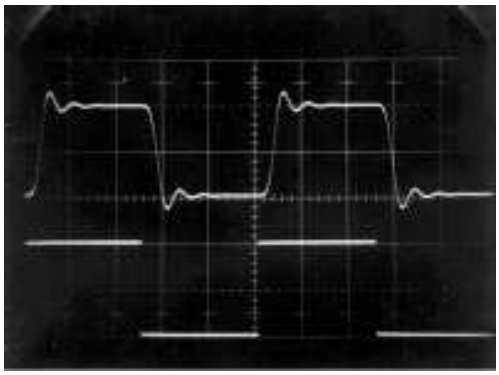
TL/H/9294–27

f_{IN} = 1.5 kHz (Scope Time Base = 2 ms/Div)

FIGURE 12. LMF60-50 Abrupt Clock Frequency Change

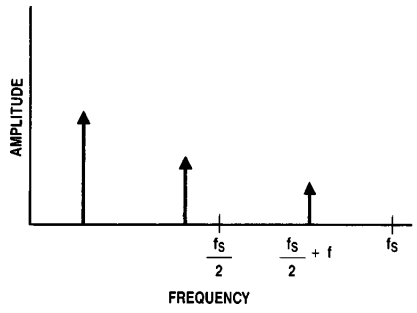
2.5 ALIASING CONSIDERATIONS

Aliasing effects have to be taken into consideration when input signal frequencies exceed half the sampling rate. For the LMF60 this equals half the clock frequency (f_{CLK}). When the input signal contains a component at a frequency higher than half the clock frequency, as in *Figure 14a*, that component will be ''reflected'' about $f_{CLK}/2$ into the frequency range *below* $f_{CLK}/2$ as in *Figure 14b*. If this component is within the passband of the filter and of large enough amplitude it can cause problems. Therefore if frequency components in the input signal exceed $f_{CLK}/2$ they must be attenuated before being applied to the LMF60 input. The necessary amount of attenuation will vary depending on system requirements. In critical applications the signal components above $f_{CLK}/2$ will have to be attenuated at least to the filter's residual noise level. An example circuit is shown in *Figure 15* using one of the uncommitted Op-Amps available in the LMF60.



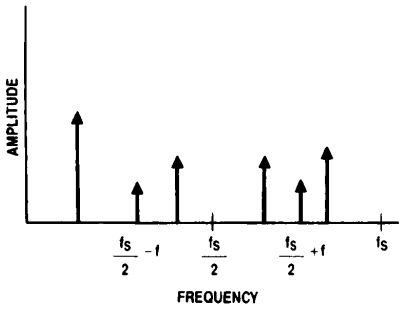
TL/H/9294–28

FIGURE 13. LMF60-50 Step Input Response, Vertical = 2V/Div., Horizontal = 1 ms/Div., f_{CLK} = 100 kHz



TL/H/9294–29

(a) Input Signal Spectrum

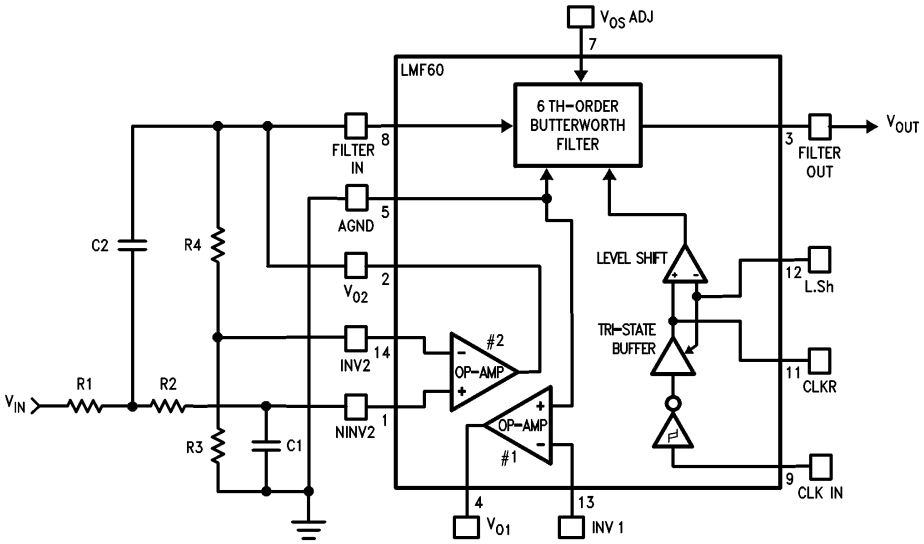


TL/H/9294–30

(b) Output Signal Spectrum. Note that the input signal at $f_S/2 + f$ causes an output signal to appear at $f_S/2 - f$.

FIGURE 14. The phenomenon of aliasing in sampled-data systems. An input signal whose frequency is greater than one-half the sampling frequency will cause an output to appear at a frequency lower than one-half the sampling frequency. In the LMF60, $f_S = f_{CLK}$.

2.0 Designing with the LMF60 (Continued)



TL/H/9294–31

$$f_0 = \frac{1}{2\pi\sqrt{R_1R_2C_1C_2}}$$

$H_0 = R_4/R_3$ ($H_0 = 1$ when R_3 and R_4 are omitted and V_{O2} is directly tied to INV2).

Design Procedure:
pick C_1

$$R_2 = \frac{1}{2QC_1\omega_0}$$

for a 2nd Order Butterworth $Q = 0.707$

$$R_2 = \frac{0.113}{C_1 f_0}$$

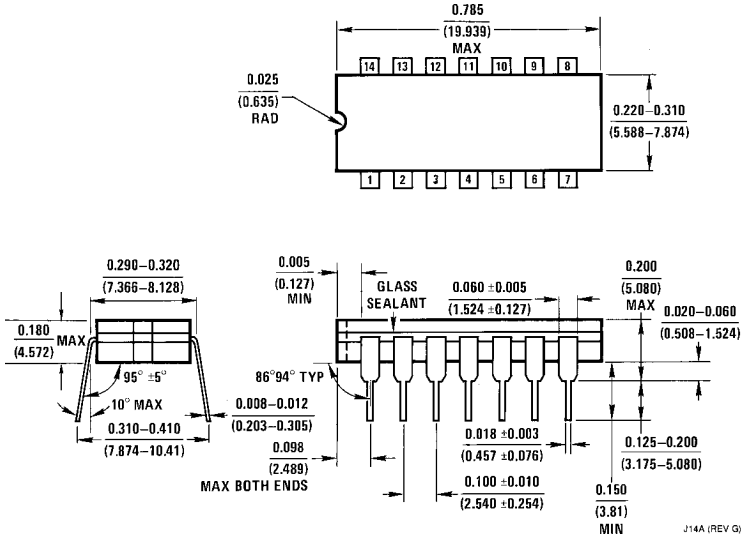
make $R_1 = R_2$
and

$$C_2 = \frac{1}{(2\pi f_0 R_1)^2 C_1}$$

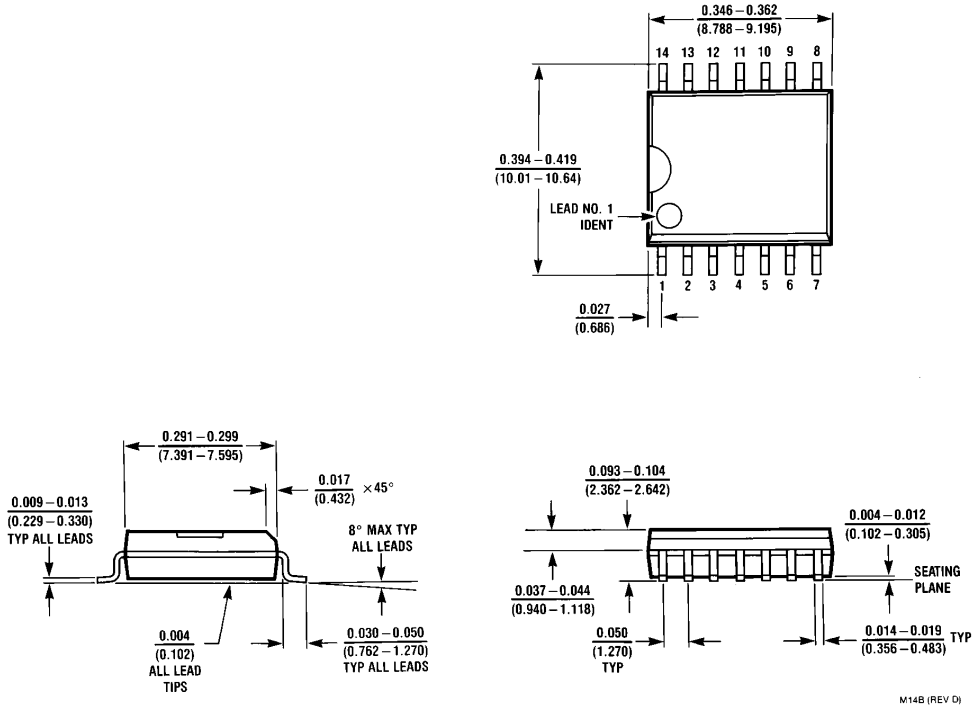
Note: The parallel combination of R_4 (if used), R_1 and R_2 should be $\geq$ 10 kΩ in order not to load Op-Amp #2.

FIGURE 15. Second Order Butterworth Anti-Aliasing Filter Using Uncommitted Op-Amp #2

Physical Dimensions inches (millimeters) unless otherwise noted



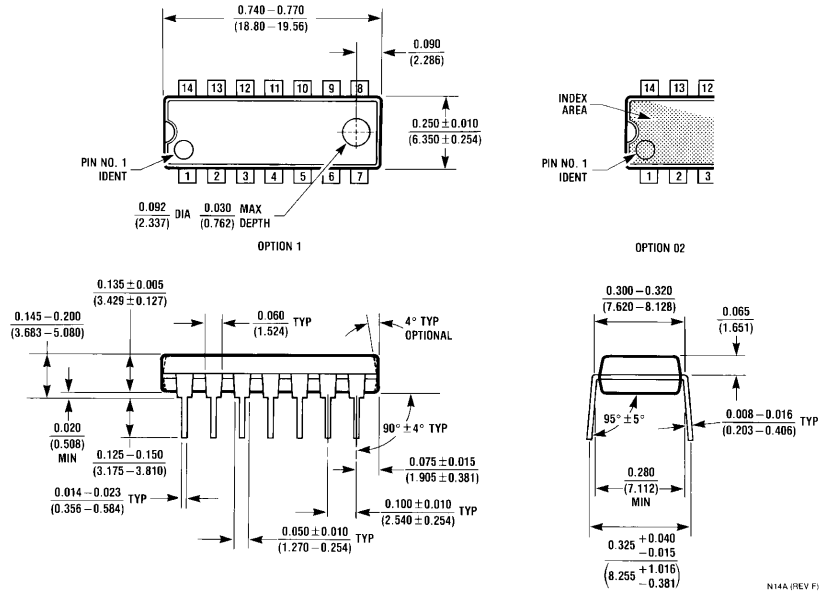
Cavity Dual-In-Line Package (J)
Order Number LMF60CMJ-50, LMF60CMJ50/883,
LMF60CMJ-100 or LMF60CMJ100/883
NS Package Number J14A



Small Outline Wide Body (M)
Order Number LMF60CIWM-50 or LMF60CIWM-100
NS Package Number M14B

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

Lit. # 108461



Molded Dual-In-Line Package (N)
Order Number LMF60CIN-50 or LMF60CIN-100
NS Package Number N14A

LIFE SUPPORT POLICY

NATIONAL'S PRODUCTS ARE NOT AUTHORIZED FOR USE AS CRITICAL COMPONENTS IN LIFE SUPPORT DEVICES OR SYSTEMS WITHOUT THE EXPRESS WRITTEN APPROVAL OF THE PRESIDENT OF NATIONAL SEMICONDUCTOR CORPORATION. As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, and whose failure to perform, when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in a significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

National Semiconductor Corporation
1111 West Bardin Road
Arlington, TX 76017
Tel: 1(800) 272-9959
Fax: 1(800) 737-7018

http://www.national.com

National Semiconductor Europe
Fax: +49 (0) 180-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 180-530 85 85
English Tel: +49 (0) 180-532 78 32
Français Tel: +49 (0) 180-532 93 58
Italiano Tel: +49 (0) 180-534 16 80

National Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: (852) 2737-1600
Fax: (852) 2736-9960

National Semiconductor Japan Ltd.
Tel: 81-043-299-2308
Fax: 81-043-299-2408