DATA SHEET

For a complete data sheet, please also download:

- The IC04 LOCMOS HE4000B Logic Family Specifications HEF, HEC
- The IC04 LOCMOS HE4000B Logic Package Outlines/Information HEF, HEC

HEF40245B
buffers
Octal bus transceiver with 3-state outputs

Product specification
File under Integrated Circuits, IC04

January 1995

Philips Semiconductors

PHILIPS

Octal bus transceiver with 3-state outputs

HEF40245B buffers

DESCRIPTION

The HEF40245B is an octal bus transmitter/receiver designed for 8-line asynchronous, 2-way data communication between data buses. It features output stages with high current output capability suitable for driving highly capacitive loads.

The direction input (DR) controls transmission of data from bus A to bus B, or bus B to bus A, depending on its logic level. The 3-state outputs are controlled by the enable input $\overline{EO}$. A HIGH on $\overline{EO}$ causes the outputs to assume a high impedance OFF-state. The device also features hysteresis on all inputs to improve noise immunity.

Schmitt-trigger action in the inputs makes the circuit highly tolerant to slower input rise and fall times.

The HEF40245B is pin and functionally compatible with the TTL '245' device.

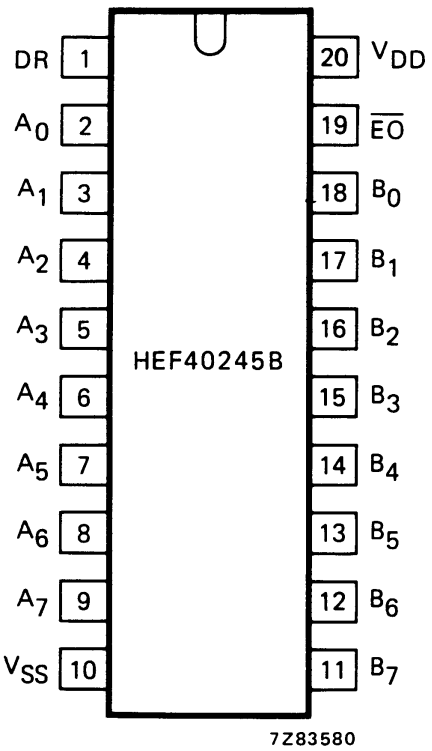


Fig.1 Pinning diagram.

PINNING

A_0 to A_7	data input/output
B_0 to B_7	data input/output
DR	direction input
$\overline{EO}$	output enable input (active LOW)

HEF40245BP(N): 20-lead DIL; plastic (SOT146-1)
HEF40245BD(F): 20-lead DIL; ceramic (cerdip) (SOT152)
HEF40245BT(D): 20-lead SO; plastic (SOT163-1)
( ): Package Designator North America

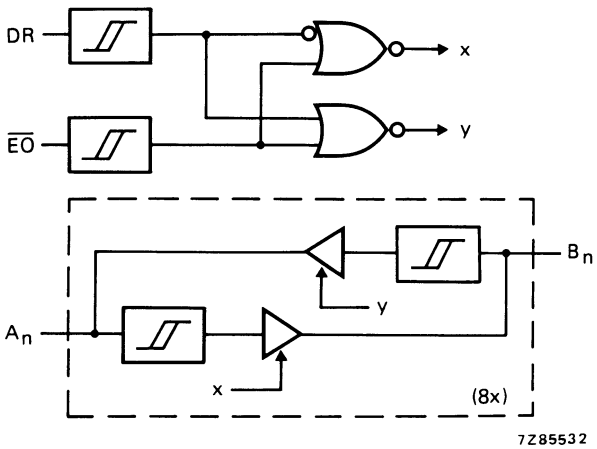


Fig.2 Logic diagram; for functional diagram see Fig.3.

FAMILY DATA, I_{DD} LIMITS category buffers

See Family Specifications.

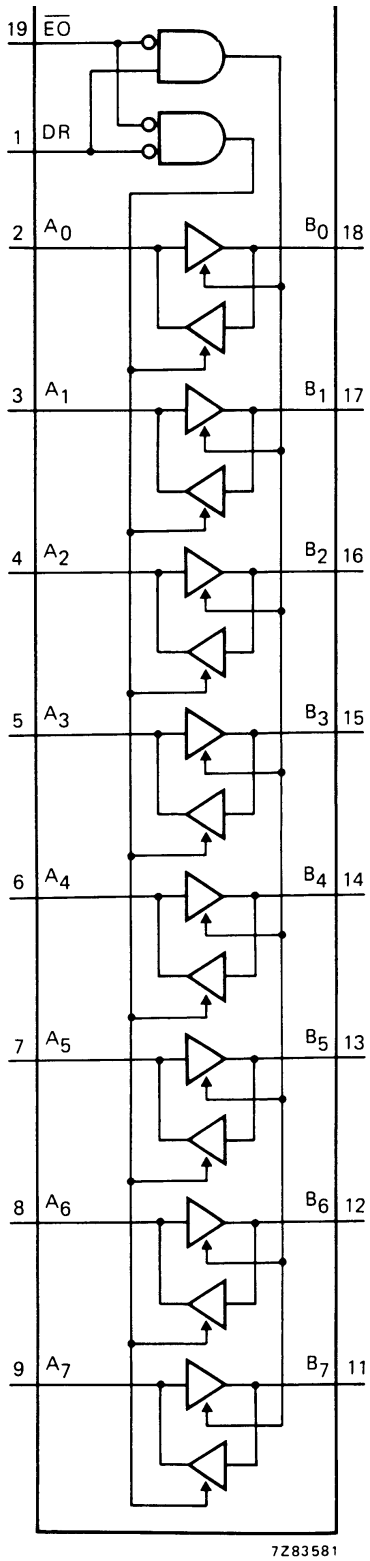


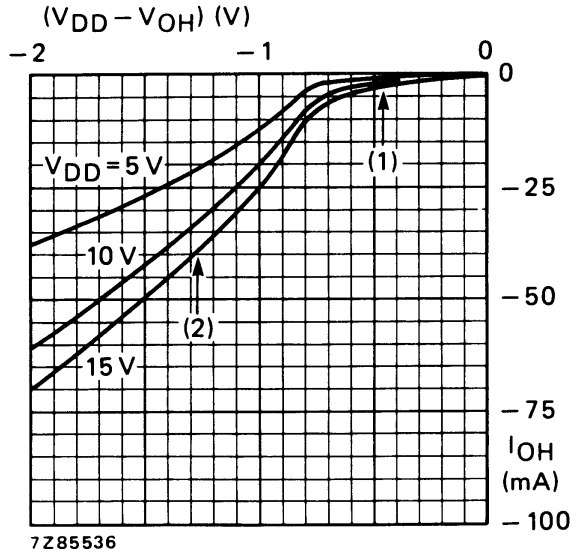
Fig.3 Functional diagram.

FUNCTION TABLE

INPUTS		INPUTS/OUTPUTS	
$\overline{EO}$	DR	A_n	B_n
L	L	A = B	input
L	H	input	B = A
H	X	Z	Z

Notes

1. H = HIGH state (the more positive voltage)
   L = LOW state (the less positive voltage)
   X = state is immaterial
   Z = high impedance OFF-state



(1) P-channel MOS transistor conducting.
(2) P-channel MOS transistor and bipolar n-p-n transistor conducting.

Fig.4 Typical output source current characteristic.

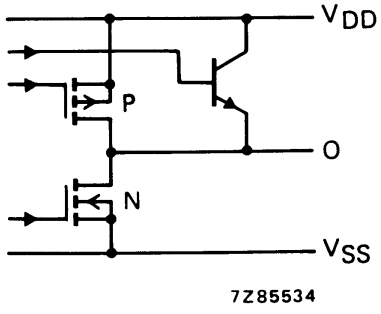


Fig.5 Schematic diagram of output stage.

RATINGS

Limiting values in accordance with the Absolute Maximum System (IEC 134)
See Family Specifications, except for:

D.C. current into any input	$\pm I_I$	max.	10	mA
D.C. source or sink current into any output	$\pm I_O$	max.	25	mA
D.C. current into the supply terminals	$\pm I$	max.	100	mA

DC CHARACTERISTICS

V_{SS} = 0 V

	V_{DD} V	V_{OH} V	V_{OL} V	SYMBOL	T_{amb} (°C)						
					−40		+ 25			+ 85		
					MIN.	MAX.	MIN.	TYP.	MAX.	MIN.	MAX.	
Output current	5	4,6			0,75		0,6	1,2		0,45		mA
HIGH	10	9,5		$-I_{OH}$	1,85		1,5	3,0		1,1		mA
	15	13,5			14,5		15	50		15,5		mA
Output current	5	3,6			9,3		10	24		10,7		mA
HIGH	10	8,4		$-I_{OH}$	14,4		15	46		15,0		mA
	15	13,2			19,5		20	62		19,8		mA
Output current	5		0,4		2,9		2,3	5,4		1,75		mA
LOW	10		0,5	I_{OL}	9,5		7,6	17		5,50		mA
	15		1,5		30,0		25	45		19,0		mA
Hysteresis	5							220				mV
voltage	10			V_H				250				mV
(any input)	15							320				mV
3-state input/output leakage current pins A_n or B_n	15			I_{OZ}[1]	–	1,6	–	–	1,6	–	12	µA

Note

1. Relevant output in OFF-state; A_n at V_{SS} or V_{DD}; B_n at V_{SS} or V_{DD}.

AC CHARACTERISTICS

V_{SS} = 0 V; T_{amb} = 25 °C; C_L = 50 pF; input transition times ≤ 20 ns

	V_{DD} V	SYMBOL	MIN.	TYP.	MAX.		TYPICAL EXTRAPOLATION FORMULA
Propagation delays							
$A_n \rightarrow B_n$	5			95	190	ns	83 ns + (0,24 ns/pF) C_L
HIGH to LOW	10	t_{PHL}		40	80	ns	35 ns + (0,10 ns/pF) C_L
	15			30	60	ns	26 ns + (0,07 ns/pF) C_L
$A_n \rightarrow B_n$	5			85	170	ns	82 ns + (0,06 ns/pF) C_L
LOW to HIGH	10	t_{PLH}		40	80	ns	38 ns + (0,03 ns/pF) C_L
	15			30	60	ns	29 ns + (0,02 ns/pF) C_L
Output transition	5			40	80	ns	
times	10	t_{THL}		20	40	ns	
HIGH to LOW	15			15	30	ns	see Fig.6
	5			30	60	ns	
LOW to HIGH	10	t_{TLH}		20	40	ns	
	15			15	30	ns	
3-state propagation delays							
Output disable times							
$\overline{EO} \rightarrow A_n, B_n$	5			100	200	ns	
HIGH	10	t_{PHZ}		50	100	ns	
	15			40	80	ns	
	5			100	200	ns	
LOW	10	t_{PLZ}		60	120	ns	
	15			50	100	ns	
Output enable times							
$\overline{EO} \rightarrow A_n, B_n$	5			100	200	ns	
HIGH	10	t_{PZH}		45	90	ns	
	15			35	70	ns	
	5			115	230	ns	
LOW	10	t_{PZL}		55	110	ns	
	15			45	90	ns	

ALL BUFFERS SWITCHING	V_{DD} V	TYPICAL FORMULA FOR P (μW)	
Dynamic power	5	$4\,250\ f_i + \sum (f_o C_L) \times V_{DD}^2$	where
dissipation per	10	$17\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_i = input freq. (MHz)
package (P)	15	$46\,000\ f_i + \sum (f_o C_L) \times V_{DD}^2$	f_o = output freq. (MHz)
			C_L = load capacitance (pF)
			$\sum (f_o C_L)$ = sum of outputs
			V_{DD} = supply voltage (V)

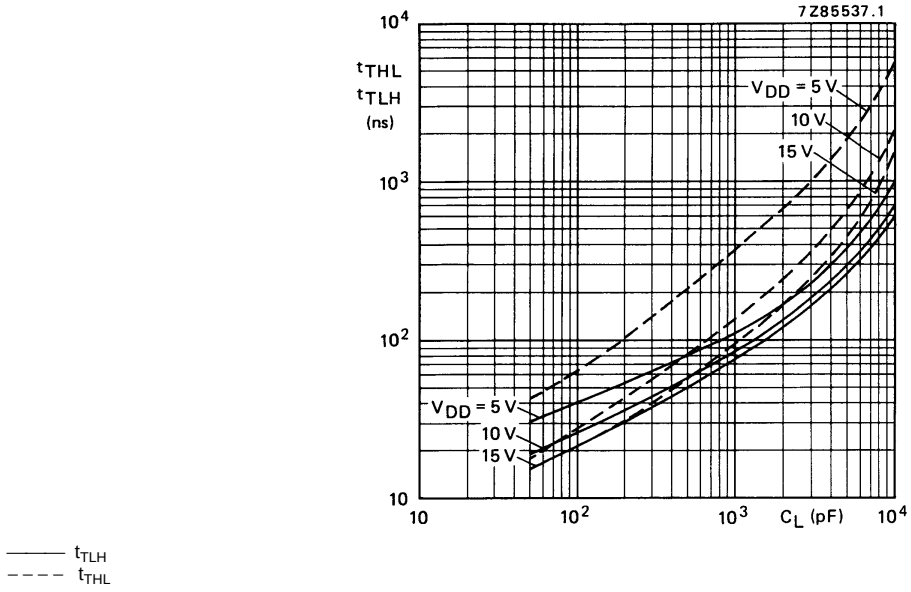


Fig.6 Output transition times as a function of the load capacitance.