MC68008

Technical Summary

16-Bit Microprocessor With 8-Bit Data Bus

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This document contains both a summary of the MC68008 as well as a detailed set of parametrics. For detailed information on the MC68008 refer to M68000 UM/AD, *M68000 8-/16-/32-Bit Microprocessor User's Manual*.

The MC68008 is a member of the M68000 Family of advanced microprocessors. This device allows the design of cost-effective systems using 8-bit data buses while providing the benefits of a 32-bit microprocessor architecture. The performance of the MC68008 is greater than any 8-bit microprocessor and superior to several 16-bit microprocessors.

The following resources are available to the MC68008 user:

- 17 32-Bit Data and Address Registers
- 56 Basic Instruction Types
- Extensive Exception Processing
- Memory-Mapped I/O
- 14 Addressing Modes
- Complete Code Compatibility with the MC68000

This document contains information on a new product. Specifications and information herein are subject to change without notice.

INTRODUCTION

A system implementation based on an 8-bit data bus reduces system cost in comparison to 16-bit systems due to a more effective use of components and byte-wide memories and peripherals. In addition, the nonmultiplexed address and data buses eliminate the need for external demultiplexers, further simplifying the system.

The MC68008 has full code compatibility (source and object) with the MC68000, which allows programs to be run on either MPU, depending on performance requirements and cost objectives.

The MC68000 is available as a 48-pin dual-in-line package (in plastic or ceramic) and 52-pin quad plastic package. Among the four additional pins of the 52-pin package, two additional address lines are included beyond the 20 address lines of the 48-pin package. The address lines reach of the MC68008 is 1 of 4 Mbytes with the 48- or 52-pin package, respectively.

The large nonsegmented linear address space of the MC68008 allows large modular programs to be developed and executed efficiently. A large linear address space allows program segment sizes to be determined by the application rather than forcing the designer to adopt an arbitrary segment size without regard to the application's individual requirements.

The programmer's model is identical to that of the MC68000 (see Figure 1), with 17 32-bit registers, a 32-bit program counter (PC), and a 16-bit status register (SR). The first eight registers (D0–D7) are used as data registers for byte (8-bit), word (16-bit), and long word (32-bit) operations. The second set of seven registers (A0–A6), the user stack pointer (A7), and the system stack pointer (A7′) can be used as software stack pointers and base address registers. In addition, the registers can be used for some simple word and long-word data operations. All 17 registers can be used as index registers.

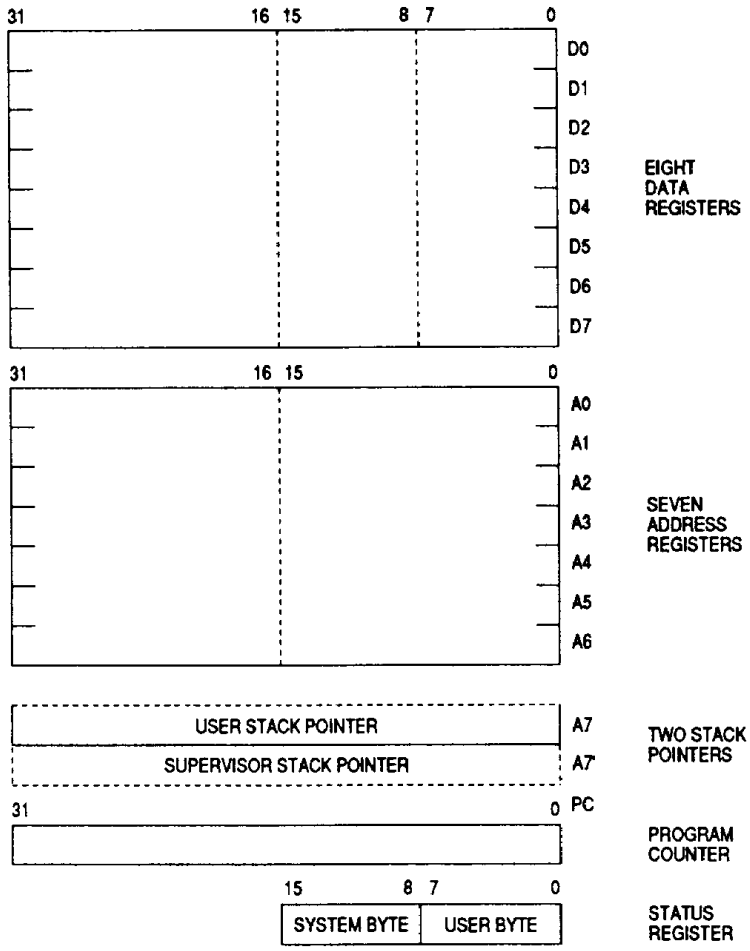

Figure 1. Programming Model

The system stack is used by many instructions. The 14 addressing modes allow the creation of user stacks and queues. Although all address registers can be used to create stacks and queues, the A7 register, by convention, is used as the system stack pointer. Supplementing this convention is another address register, A7', also referred to as the system stack pointer. This powerful concept allows the supervisor mode and user mode of the MC68008 to have their own system stack pointer (SP) without needing to move pointers for each context of use when the mode is switched.

The SP is either the supervisor stack pointer (A7'—SSP) or the user stack pointer (A7—USP), depending on the state of the S bit in the SR. If the S bit is set, indicating that the processor is in the supervisor state, then the SSP is the active system stack pointer and the USP is not used. If the S bit is clear, indicating that the processor is in the user state, then the USP is the active system stack pointer and the SSP is protected from user modification.

The SR (see Figure 2) can be considered as two bytes, the user byte and the system byte. The user byte contains five bits defining the overflow (V), zero (Z), negative (N), carry (C), and extended (X) condition codes. The system byte contains five defined bits. Three bits are used to define the current interrupt priority; and any interrupt level higher than the current mask level will be recognized. (Note that level 7 interrupts are nonmaskable — that is, level 7 interrupts are always processed.) Two additional bits indicate whether the processor is in the trace (T) mode and/or in the supevisor (S) state.

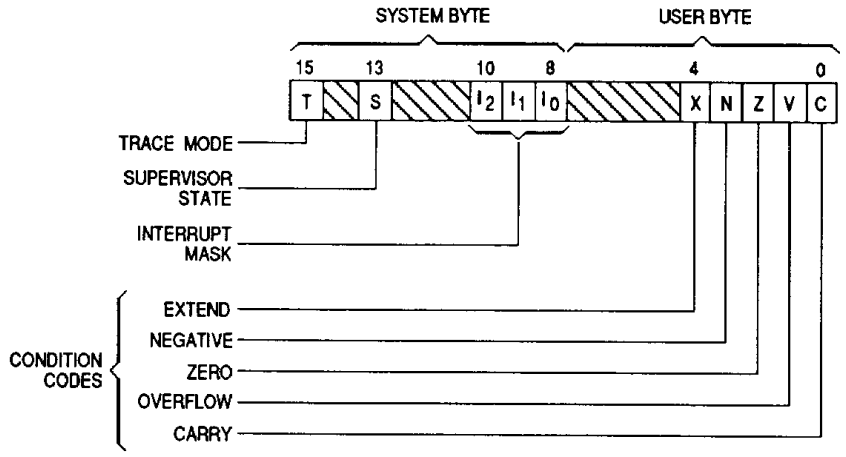

Figure 2. Status Register

DATA TYPES AND ADDRESSING MODES

Five basic data types are supported:

1. Bits
2. BCD Digits (4 bits)
3. Bytes (8 bits)
4. Words (16 bits)
5. Long Words (32 bits)

In addition, operations on other data types, such as memory addresses, status word data, etc., are provided in the instruction set.

Most instructions can use any of the 14 addressing modes listed in Table 1. These addressing modes consist of six basic types:

1. Register Direct
2. Register Indirect
3. Absolute
4. Program Counter Relative
5. Immediate
6. Implied

The register indirect addressing modes also have the capability to perform postincrementing, predecrementing, offsetting, and indexing. The program counter relative mode can be used in combination with indexing and offsetting for writing relocatable programs.

Table 1. Addressing Modes

Addressing Modes	Syntax
Register Direct Addressing	
Data Register Direct	Dn
Address Register Direct	An
Absolute Data Addressing	
Absolute Short	xxx.W
Absolute Long	xxx.L
Program Counter Relative Addressing	
Relative with Offset	d_{16}(PC)
Relative with Index Offset	d_8(PC,Xn)
Register Indirect Addressing	
Register Indirect	(An)
Postincrement Register Indirect	(An)+
Predecrement Register Indirect	-(An)
Register Indirect with Offset	d_{16}(An)
Indexed Register Indirect with Offset	d_8(An,Xn)
Immediate Data Addressing	
Immediate	#xxx
Quick Immediate	#1r#8
Implied Addressing	
Implied Register	SR/USP/SP/PC

NOTES:
Dn = Data Register
An = Address Register
Xn = Address of Data Register Used as Index Register
SR = Status Register
PC = Program Counter
SP = Stack Pointer
USP = User Stack Pointer
( ) = Contents of
d_8 = 8-Bit Offset (Displacement)
d_{16} = 16-Bit Offset (Displacement)
#xxx = Immediate Data

INSTRUCTION SET OVERVIEW

The MC68008 is completely code compatible with the MC68000. This applies equally to either source code or object code. For detailed information on the MC68008 instruction set, refer to M68000 PM/AD, *M68000 Programmer's Reference Manual.*

The instruction set was designed to minimize the number of mnemonics remembered by the programmer. To further reduce the programmer's burden, the addressing modes are orthogonal.

The instruction set, shown in Table 2, forms a set of programming tools that include all processor functions to perform data movement, integer arithmetic, logical operations, shift and rotate operations, bit manipulation, BCD operations, and both program and system control. Some additional instructions, which are variations or subsets of these instructions, are listed in Table 3.

Table 2. Instruction Set Summary

Mnemonic	Description
ABCD	Add Decimal with Extend
ADD	Add
AND	Logical AND
ASL	Arithmetic Shift Left
ASR	Arithmetic Shift Right
Bcc	Branch Conditionally
BCHG	Bit Test and Change
BCLR	Bit Test and Clear
BRA	Branch Always
BSET	Bit Test and Set
BSR	Branch to Subroutine
BTST	Bit Test
CHK	Check Register against Bounds
CLR	Clear Operand
CMP	Compare
DBcc	Test Condition, Decrement and Branch
DIVS	Signed Divide
DIVU	Unsigned Divide
EOR	Exclusive OR
EXG	Exchange Registers
EXT	Sign Extend
JMP	Jump
JSR	Jump to Subroutine
LEA	Load Effective Address
LINK	Link Stack
LSL	Logical Shift Left
LSR	Logical Shift Right
MOVE	Move
MULS	Signed Multiply
MULU	Unsigned Multiply
NBCD	Negate Decimal with Extend
NEG	Negate
NOP	No Operation
NOT	Ones Complement
OR	Logical OR
PEA	Push Effective Address
RESET	Reset External Devices
ROL	Rotate Left without Extend
ROR	Rotate Right without Extend
ROXL	Rotate Left with Extend
ROXR	Rotate Right with Extend
RTE	Return from Exception
RTR	Return and Restore
RTS	Return from Subroutine
SBCD	Subtract Decimal with Extend
Scc	Set Conditional
STOP	Stop
SUB	Subtract
SWAP	Swap Data Register Halves
TAS	Test and Set Operand
TRAP	Trap
TRAPV	Trap on Overflow
TST	Test
UNLK	Unlink

Table 3. Variations of Instruction Types

Instruction Type	Variation	Description
ADD	ADD	Add
	ADDA	Add Address
	ADDQ	Add Quick
	ADDI	Add Immediate
	ADDX	Add with Extend
AND	AND*	Logical AND
	ANDI	AND Immediate
	ANDI to CCR	AND Immediate to Condition Codes
	ANDI to SR	AND Immediate to Status Register
CMP	CMP	Compare
	CMPA	Compare Address
	CMPM	Compare Memory
	CMPI	Compare Immediate
EOR	EOR	Exclusive OR
	EORI	Exclusive OR Immediate
	EORI to CCR	Exclusive OR Immediate to Condition Codes
	EORI to SR	Exclusive OR Immediate to Status Register
MOVE	MOVE	Move Source to Destination
	MOVEA	Move Address
	MOVEC	Move Control Register
	MOVEM	Move Multiple Registers
	MOVEP	Move Peripheral Data
	MOVEQ	Move Quick
	MOVES	Move Alternate Address Space
	MOVE from SR	Move from Status Register
	MOVE to SR	Move to Status Register
	MOVE from CCR	Move from Condition Codes
	MOVE to CCR	Move to Condition Codes
	MOVE USP	Move User Stack Pointer
NEG	NEG	Negate
	NEGX	Negate with Extend
OR	OR	Logical OR
	ORI	OR Immediate
	ORI to CCR	OR Immediate to Condition Codes
	ORI to SR	OR Immediate to Status Register
SUB	SUB	Subtract
	SUBA	Subtract Address
	SUBI	Subtract Immediate
	SUBQ	Subtract Quick
	SUBX	Subtract with Extend

SIGNAL DESCRIPTION

The MC68008 is available in two package sizes (48-pin and 52-pin). The additional four pins of the 52-pin quad package allow for additional signals: A20, A21, $\overline{\text{BGACK}}$, and $\overline{\text{IPL2}}$.

The input and output signals can be functionally organized into the groups shown in Figure 3(a) for the 48-pin version and in Figure 3(b) for the 52-pin version. The following paragraphs provide a brief description of the signals and a reference (if applicable) to other paragraphs that contain more information about the function being performed.

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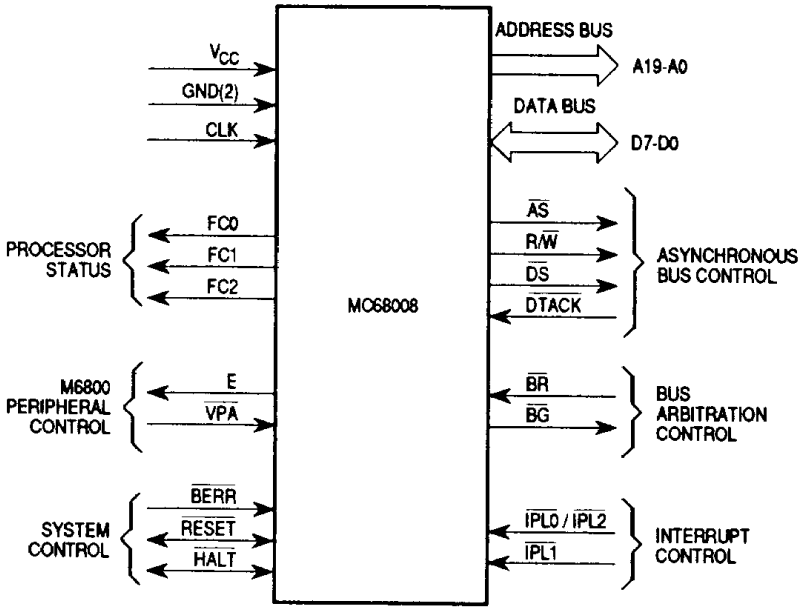
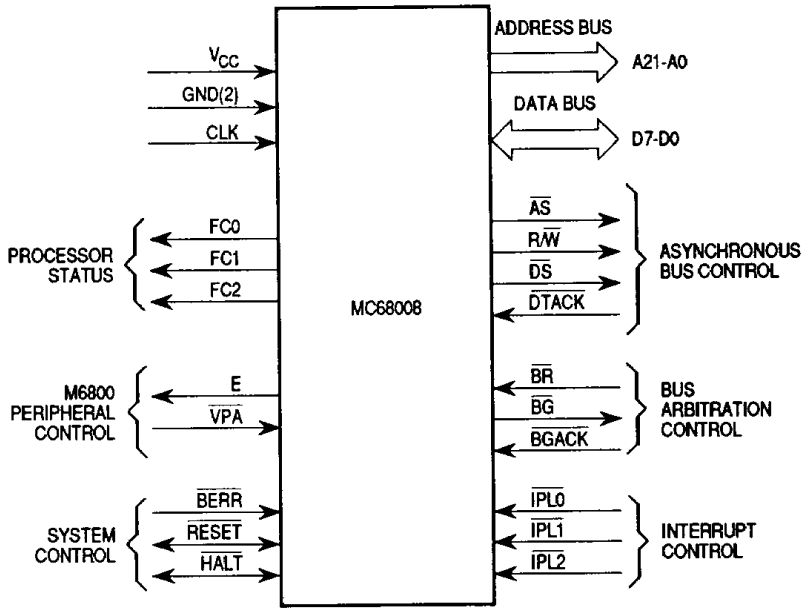


(a) 48-Pin Version



(b) 52-Pin Version

Figure 3. Functional Signal Groups

ADDRESS BUS (48-Pin: A0–A19; 52-Pin: A0–A21)

This unidirectional three-state bus provides the address for bus operation during all cycles except interrupt acknowledge cycles. During interrupt acknowledge cycles, address lines A1, A2, and A3 provide information about what level interrupt is being serviced while address lines A0 and A4–A19 (A21) are all driven high.

DATA BUS (D0–D7)

This 8-bit, bidirectional, three-state bus is the general-purpose data path. During an interrupt acknowledge cycle, the external device supplies the vector number on data lines D0–D7.

ASYNCHRONOUS BUS CONTROL

Asynchronous data transfers are handled using the following control signals: address strobe, read/write, data strobe, and data transfer acknowledge.

Address Strobe ($\overline{AS}$)

This three-state signal indicates a valid address on the address bus. It is also used to "lock" the bus during the read-modify-write cycle used by the test and set (TAS) instruction.

Read/Write (R/$\overline{W}$)

This three-state signal defines the data bus transfer as a read or write cycle. R/$\overline{W}$ also works in conjunction with the data strobe as explained in the following paragraph.

Data Strobe ($\overline{DS}$)

This three-state signal controls the flow of data on the data bus as listed in Table 4. When R/$\overline{W}$ is high, the processor will read from the data bus as indicated. When R/$\overline{W}$ is low, the processor will write to the data bus as shown.

Table 4. Data Strobe Control of Data Bus

$\overline{DS}$	R/$\overline{W}$	D0–D7
1	—	No Valid Data
0	1	Valid Data Bits 0–7 (Read Cycle)
0	0	Valid Data Bits 0–7 (Write Cycle)

Data Transfer Acknowledge ($\overline{DTACK}$)

This input indicates that the data transfer is complete. When the processor recognizes $\overline{DTACK}$ during a read cycle, data is latched and the bus cycle is terminated. When $\overline{DTACK}$ is recognized during a write cycle, the bus cycle is terminated.

BUS ARBITRATION CONTROL

The 48-pin MC68008 contains a simple two-wire arbitration circuit; the 52-pin MC68008 contains a full three-wire MC68000 bus arbitration control. Both versions are designed to work with daisy-chained networks, priority encoded networks, or a combination of these techniques. This circuit is used in determining which device will be the bus master.

Bus Request ($\overline{BR}$)

This input is wire-ORed with all other devices that could be bus masters. This input indicates to the processor that some other device desires to become the bus master. Bus requests may be issued at any time in the cycle or even if no cycle is being performed.

Bus Grant ($\overline{BG}$)

This output indicates to all other potential bus master devices that the processor will release bus control at the end of the current bus cycle.

Bus Grant Acknowledge ($\overline{BGACK}$)

This input, available on the 52-pin version only, indicates that some other device has become the bus master. This signal should not be asserted until the following four conditions are met:

1. A bus grant has been received.
2. Address strobe is inactive, which indicates that the microprocessor is not using the bus.
3. Data transfer acknowledge is inactive, which indicates that neither memory nor peripherals are using the bus.
4. Bus grant acknowledge is inactive, which indicates that no other device is claiming bus mastership.

NOTES

1. There is a two-clock interval straddling the transition of $\overline{AS}$ from the inactive state to the active state during which $\overline{BG}$ can not be issued.
2. If an existing MC68000 system is retrofitted to use the MC68008 48-pin version (using $\overline{BR}$ and $\overline{BG}$ only), the existing $\overline{BR}$ and $\overline{BGACK}$ signals should be ANDed and the resultant signal connected to the MC68008 $\overline{BR}$.

INTERRUPT CONTROL (48-Pin: $\overline{IPL0}/\overline{IPL2}$, $\overline{IPL1}$; 52-Pin: $\overline{IPL0}$, $\overline{IPL1}$, $\overline{IPL2}$)

These input pins indicate the encoded priority level of the device requesting an interrupt. The MC68000 and the 52-pin MC68008 MPUs use three pins to encode a range of 0–7 but, for the 48-pin MC68008, only two pins are available. By connecting the $\overline{IPL0}/\overline{IPL2}$ pin to both the $\overline{IPL0}$ and $\overline{IPL2}$ inputs internally, the

48-pin version encodes values of 0, 2, 5, and 7. Level 0 is used to indicate that there are no interrupts pending and level 7 is a nonmaskable edge-triggered interrupt. Except for level 7, the requesting level must be greater than the interrupt mask level contained in the processor status register before the processor will acknowledge the request.

The level presented to these inputs is continually monitored to allow for the case of a requesting level that is less than or equal to the processor status register level to be followed by a request that is greater than the processor status register level. A satisfactory interrupt condition must exist for two successive clocks before triggering an internal interrupt request. An interrupt acknowledge sequence is indicated by the function codes.

SYSTEM CONTROL

The three system control inputs are used to either reset or halt the processor and to indicate to the processor that bus errors have occurred.

Bus Error ($\overline{BERR}$)

This input informs the processor that there is a problem with the cycle currently being executed. Problems may be a result of:

1. Nonresponding devices
2. Interrupt vector number acquisition failure
3. Illegal access request as determined by a memory management unit
4. Various other application-dependent errors

The bus error signal interacts with the halt signal to determine if the current bus cycles should be re-executed or if exception processing should be performed. A summarization of the interaction is shown in Table 5:

Table 5. Interaction of $\overline{BERR}$ and $\overline{HALT}$

$\overline{BERR}$	$\overline{HALT}$	Resulting Operation
1	1	Normal Operation
1	0	Single Bus Cycle Operation
0	1	Bus Error — Exception Processing
0	0	Bus Error — Rerun Current Cycle

Reset ($\overline{\text{RESET}}$)

This bidirectional signal resets (starts a system initialization sequence) the processor in response to an external $\overline{\text{RESET}}$ signal. An internally generated reset (result of a RESET instruction) causes all external devices to be reset, but the internal state of the processor is not affected. A total system reset (processor and external devices) is the result of external $\overline{\text{HALT}}$ and $\overline{\text{RESET}}$ signals applied simultaneously.

Halt ($\overline{\text{HALT}}$)

When this bidirectional signal is driven by an external device, it causes the processor to stop at the completion of the current bus cycle. When the processor is halted using this input, all control signals are inactive, and all three-state lines are put in their high-impedance state.

When the processor stops executing instructions, such as in a double bus fault condition, the halt line is driven by the processor to indicate to external devices that the processor has stopped.

M6800 PERIPHERAL CONTROL

These control signals are used to interface synchronous M6800 peripheral devices with the asynchronous MC68008.

The MC68008 does not supply a valid memory address ($\overline{\text{VMA}}$) signal like that of the MC68000. $\overline{\text{VMA}}$ indicates to the M6800 peripheral devices that there is a valid address on the address bus and that the processor is synchronized to the enable clock. This signal can be produced by a TTL circuit (see a sample circuit in Figure 4). $\overline{\text{VMA}}$ only responds to a valid peripheral address ($\overline{\text{VPA}}$) input, which indicates that the peripheral is an M68000 Family device.

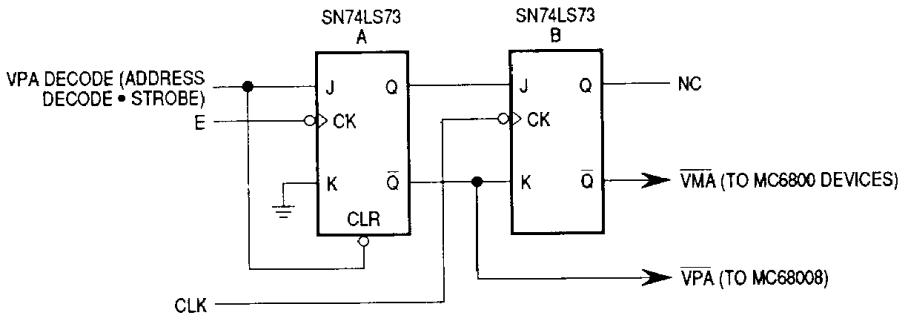


Figure 4. External $\overline{\text{VMA}}$ Generation

The $\overline{VPA}$ decode shown in Figure 4 is an active-high decode, indicating that $\overline{AS}$ has been asserted and the address bus is addressing an M6800 peripheral. The $\overline{VPA}$ output is used to indicate to the MC68008 that the data transfer should be synchronized with the enable (E) signal.

Enable (E)

This signal is the standard enable signal common to all M6800-type peripheral devices. The period for this output is 10 MC68008 clock periods (six clocks low, four clocks high).

Valid Peripheral Address ($\overline{VPA}$)

This input indicates that the device or region addressed is an M6800 Family device and that data transfer should be synchronized with E. This input also indicates that the processor should use automatic vectoring for an interrupt.

PROCESSOR STATUS (FC0, FC1, FC2)

These function code outputs indicate the state (user or supervisor) and the cycle type currently being executed (see Table 6). The information indicated by the function code output is valid whenever $\overline{AS}$ is active.

Table 6. Function Code Outputs

Function Code Output			Address Space
FC2	FC1	FC0	
0	0	0	(Undefined, Reserved)
0	0	1	User Data
0	1	0	User Program
0	1	1	(Undefined, Reserved)
1	0	0	(Undefined, Reserved)
1	0	1	Supervisor Data
1	1	0	Supervisor Program
1	1	1	Interrupt Acknowledge

CLOCK (CLK)

The clock input is a TTL-compatible signal that is internally buffered for development of the internal clocks needed by the processor. The clock input should be a constant frequency.

V_{CC} AND GND

Power is supplied to the processor using these two signals.

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SIGNAL SUMMARY

Table 7 summarizes the signals discussed in the previous paragraphs.

Table 7. Signal Summary

Signal Name	Mnemonic	Input/Output	Active State	Hi-Z	
				On $\overline{HALT}$	On $\overline{BGACK}$
Address Bus	A0–A19 (A21)	Output	High	Yes	Yes
Data Bus	D0–D7	Input/Output	High	Yes	Yes
Address Strobe	$\overline{AS}$	Output	Low	No	Yes
Read/Write	R/$\overline{W}$	Output	Read—High Write—Low	No No	Yes Yes
Data Strobe	$\overline{DS}$	Output	Low	No	Yes
Data Transfer Acknowledge	$\overline{DTACK}$	Input	Low	No	No
Bus Request	$\overline{BR}$	Input	Low	No	No
Bus Grant	$\overline{BG}$	Output	Low	No	No
Bus Grant Acknowledge**	$\overline{BGACK}$	Input	Low	No	No
Interrupt Priority Level	$\overline{IPLx}$	Input	Low	No	No
Bus Error	$\overline{BERR}$	Input	Low	No	No
Reset	$\overline{RESET}$	Input/Output	Low	No*	No*
Halt	$\overline{HALT}$	Input/Output	Low	No*	No*
Enable	E	Output	High	No	No
Valid Peripheral Address	$\overline{VPA}$	Input	Low	No	No
Function Code Output	FC0, FC1, FC2	Output	High	No	Yes
Clock	CLK	Input	High	No	No
Power Input	V_{CC}	Input	—	—	—
Ground	GND	Input	—	—	—

*Open Drain
**52-Pin Version Only

DATA TRANSFER OPERATIONS

Transfer of data between devices involves the following signals:

1. Address bus A0–A21
2. Data bus D0–D7
3. Control signals

The address and data buses are separated nonmultiplexed parallel buses. Data transfer is accomplished with an asynchronous bus structure that uses handshakes to ensure the correct movement of data. In all cycles, the bus master assumes responsibility for deskewing all signals it issues at both the start and end of a cycle. In addition, the bus master is responsible for deskewing the acknowledge and data signals from the slave device.

The following paragraphs explain the read, write, and read-modify-write cycles. The indivisible read-modify-write cycle is the method used by the MC68008 for interlocked multiprocessor communications.

READ CYCLE

During a read cycle, the processor receives data from the memory or a peripheral device. The processor reads bytes of data in all cases. If the instruction specifies a word (or double word) operation, the processor reads both bytes in a two-cycle read operation. When the instruction specifies byte operation, the processor uses A0 to determine which byte to read and then issues data strobe.

WRITE CYCLE

During a write cycle, the processor sends data to either the memory or a peripheral device. The processor writes bytes of data in all cases. If the instruction specifies a word operation, the processor writes both bytes in a two-cycle write operation. When the instruction specifies a byte operation, the processor uses A0 to determine which byte to write and then activates $\overline{DS}$.

READ-MODIFY-WRITE CYCLE

The read-modify-write cycle performs a byte read, modifies the data in the arithmetic logic unit, and writes the data back to the same address. In the MC68008, this cycle is indivisible in that the address strobe is asserted throughout the entire cycle. The TAS instruction uses the cycle to provide meaningful communication between processors in a multiple processor environment. TAS is the only instruction that uses the read-modify-write cycle; since TAS only operates on bytes, all read-modify-write cycles are byte operations.

PROCESSING STATES

The MC68008 is always in one of three processing states: normal, exception, or halted.

NORMAL PROCESSING

The normal processing state is that associated with instruction execution; the memory references are to fetch instructions and operands and to store results. A special case of the normal state is the stopped state which the processor enters when a STOP instruction is executed. In this state, no further memory references are made.

EXCEPTION PROCESSING

The exception processing state is associated with interrupts, trap instructions, tracing, and other exceptional conditions. The exception may be internally generated by an instruction or by an unusual condition arising during the execution of an instruction. Externally, exception processing can be forced by an interrupt, a bus error, or a reset. Exception processing is designed to provide an efficient context switch so that the processor may handle unusual conditions.

HALTED PROCESSING

The halted processing state is an indication of catastrophic hardware failure. For example, if, during the exception processing of a bus error, another bus error occurs, the processor assumes that the system is unusable and halts. Only an external reset can restart a halted processor. Note that a processor in the stopped state is not in the halted state, nor vice versa.

INTERFACE WITH M6800 PERIPHERALS

Motorola's extensive line of M6800 peripherals are compatible with the MC68008. Some devices that are particularly useful are as follows:

MC6821 Peripheral Interface Adapter
MC6840 Programmable Timer Module
MC6845 CRT Controller
MC6850 Asynchronous Communications Interface Adapter
MC6852 Synchronous Serial Data Adapter
MC6854 Advanced Data Link Controller

To interface the synchronous M6800 peripherals with the asynchronous MC68008, the processor modifies its bus cycle to meet the M6800 cycle requirements whenever an M6800 device address is detected. This modification is possible since both processors use memory-mapped I/O.

ELECTRICAL SPECIFICATIONS

MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Supply Voltage	V_{CC}	0.3 to + 7.0	V
Input Voltage	V_{in}	−0.3 to + 7.0	V
Operating Temperature Range MC68008 MC68008C	T_A	T_L to T_H 0 to 70 - 40 to 85	°C
Storage Temperature	T_{stg}	- 55 to 150	°C

The device contains circuitry to protect the inputs against damage due to high static voltages or electric fields; however, normal precautions should be taken to avoid application of voltages higher than maximum-rated voltages to these high-impedance circuits. Tying unused inputs to the appropriate logic voltage level (e.g., either GND or V_{CC}) enhances reliability of operation.

THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Symbol	Value	Rating
Thermal Resistance (Still Air) Ceramic, Type LC Plastic, Type P Plastic, Type FN	θ_{JA}	 40 40 50	θ_{JC}	 15* 20* 30*	°C/W

*Estimated

POWER CONSIDERATIONS

The average die-junction temperature, T_J, in °C can be obtained from:

$$T_J = T_A + (P_D \cdot \theta_{JA}) \quad (1)$$

where:

T_A = Ambient Temperature, °C
θ_{JA} = Package Thermal Resistance, Junction-to-Ambient, °C/W
P_D = $P_{INT} + P_{I/O}$
P_{INT} = $I_{CC} \times V_{CC}$, Watts — Chip Internal Power
$P_{I/O}$ = Power Dissipation on Input and Output Pins — User Determined

For most applications, $P_{I/O} < P_{INT}$ and can be neglected.

An appropriate relationship between P_D and T_J (if $P_{I/O}$ is neglected) is:

$$P_D = K \div (T_J + 273\ °C) \quad (2)$$

Solving equations (1) and (2) for K gives:

$$K = P_D \cdot (T_A + 273°C) + \theta_{JA} \cdot P_D^2 \quad (3)$$

where K is a constant pertaining to the particular part. K can be determined from equation (3) by measuring P_D (at thermal equilibrium) for a known T_A. Using this value of K, the values of P_D and T_J can be obtained by solving equations (1) and (2) iteratively for any value of T_A.

The curve shown in Figure 5 gives the graphic solution to the above equations for the specified power dissipation of 1.5 watts over the ambient temperature range of −55°C to 125°C using a maximum θJA of 45°C/W. Ambient temperature is that of the still air surrounding the device. Lower values of θJA cause the curve to shift downward slightly; for instance, for θJA of 40°/W, the curve is just below 1.4 watts at 25°C.

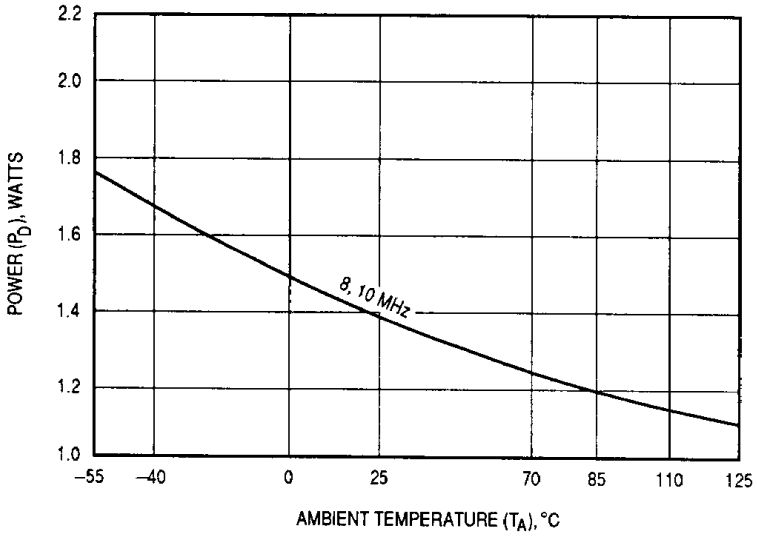


Figure 5. Power Dissipation (P_D) vs Ambient Temperature(T_A)

The total thermal resistance of a package (θJA) can be separated into two components, θJC and θCA, representing the barrier to heat flow from the semiconductor junction to the package (case) surface (θJC) and from the case to the outside ambient air (θCA). These terms are related by the equation:

$$\theta JA = \theta JC + \theta CA \quad (4)$$

θJC is device related and cannot be influenced by the user. However, θCA is user dependent and can be minimized by such thermal management techniques as heat sinks, ambient air cooling, and thermal convection. Thus, good thermal management on the part of the user can significantly reduce θCA so that θJA approximately equals θJC. Substitution of θJC for θJA in equation (1) results in a lower semiconductor junction temperature.

Table 8 summarizes maximum power dissipation and average junction temperature for the curve drawn in Figure 5, using the minimum and maximum

values of ambient temperature for different packages and substituting θ_{JC} for θ_{JA} (assuming good thermal management). Table 9 provides the maximum power dissipation and average junction temperature for the MC68000 assuming that no thermal management is applied (i.e., still air).

NOTE

Since the power dissipation curve shown in Figure 5 is negatively sloped, power dissipation declines as ambient temperature increases. Therefore, maximum power dissipation occurs at the lowest rated ambient temperature where *power dissipation is lowest.*

Values for thermal resistance presented in this manual, unless estimated, were derived using the procedure described in Motorola Reliability Report 7843, *Thermal Resistance Measurement Method for MC68XXX Microcomponent Devices*, and are provided for design purposes only. Thermal measurements are complex and dependent on procedure and setup. User-derived values for thermal resistance may differ.

Table 8. Power Dissipation and Junction Temperature vs Temperature ($\theta_{JC} = \theta_{JA}$)

Package	T_A Range	θ_{JC} (°C/W)	P_D (W) @ T_A Min.	T_J (°C) @ T_A Min.	P_D (W) @ T_A Max.	T_J (°C) @ T_A Max.
LC	0°C to 70°C	15	1.5	23	1.2	88
	−40°C to 85°C	15	1.7	−14	1.2	103
	0°C to 85°C	15	1.5	23	1.2	103
P	0°C to 70°C	20	1.5	30	1.2	95
FN	0°C to 70°C	30	1.5	45	1.3	108

Table 9. Power Dissipation and Junction Temperature vs Temperature ($\theta_{JA} \neq \theta_{JC}$)

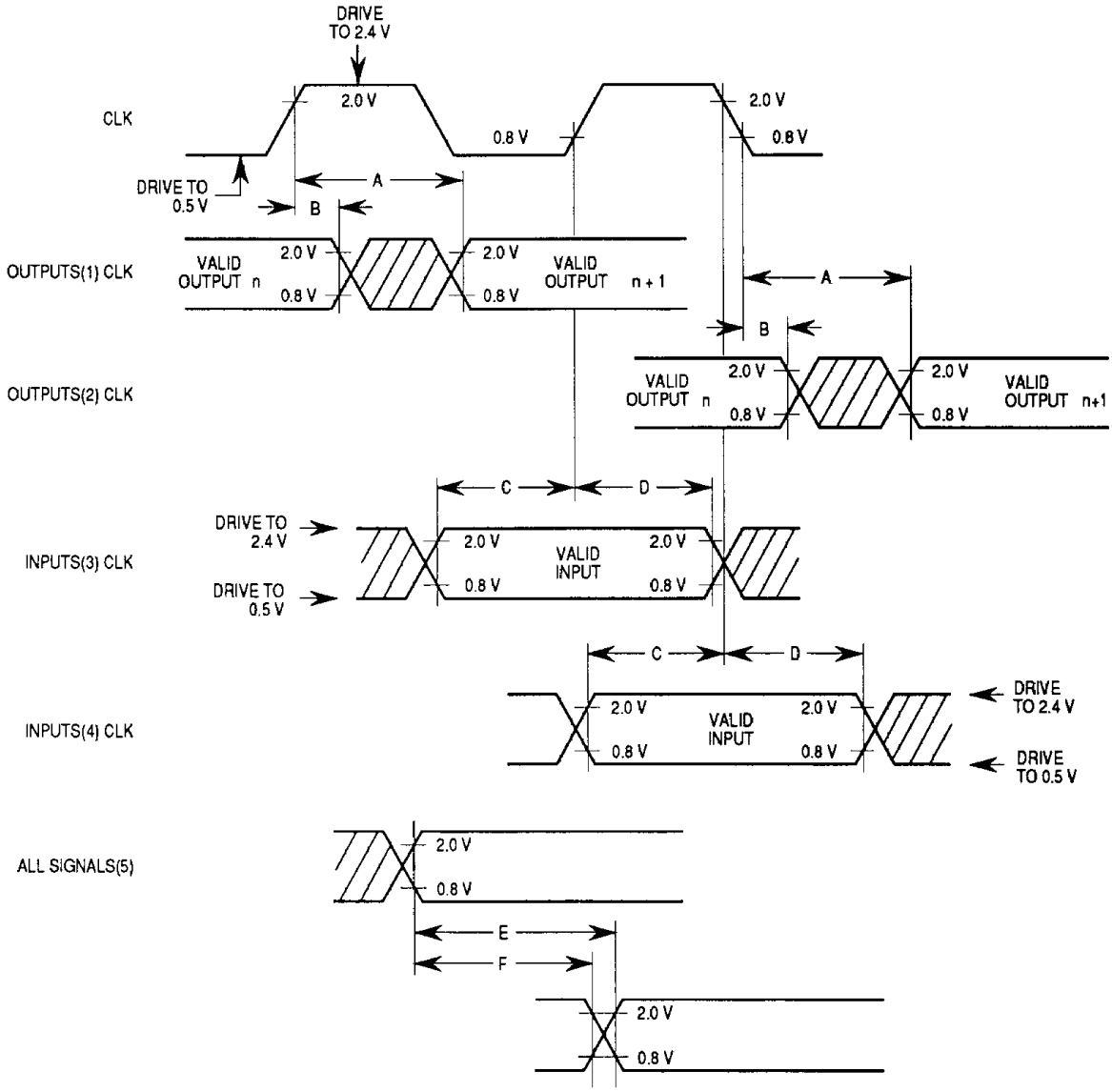
Package	T_A Range	θ_{JA} (°C/W)	P_D (W) @ T_A Min.	T_J (°C) @ T_A Min.	P_D (W) @ T_A Max.	T_J (°C) @ T_A Max.
LC	0°C to 70°C	40	1.5	60	1.2	121
	−40°C to 85°C	40	1.7	−27	1.2	134
	0°C to 85°C	40	1.5	60	1.2	134
P	0°C to 70°C	40	1.5	60	1.2	121
FN	0°C to 70°C	50	1.5	75	1.3	134

AC ELECTRICAL SPECIFICATIONS DEFINITIONS

The AC specifications presented consist of output delays, input setup and hold times, and signal skew times. All signals are specified relative to an appropriate edge of the clock and possibly to one or more other signals.

The measurement of the AC specifications is defined by the waveforms shown in Figure 6. To test the parameters guaranteed by Motorola, inputs must be driven to the voltage levels specified in this figure. Outputs are specified with minimum and/or maximum limits, as appropriate, and are measured as shown in Figure 6. Inputs are specified with minimum setup and hold times, and are measured as shown. Finally, the measurement for signal-to-signal specifications is also shown.

Note that the testing levels used to verify conformance to the AC specifications does not affect the guaranteed DC operation of the device as specified in the DC electrical specifications.



NOTES:
1. This output timing is applicable to all parameters specified relative to the rising edge of the clock.
2. This output timing is applicable to all parameters specified relative to the falling edge of the clock.
3. This input timing is applicable to all parameters specified relative to the rising edge of the clock.
4. This input timing is applicable to all parameters specified relative to the falling edge of the clock.
5. This timing is applicable to all parameters specified relative to the assertion/negation of another signal.

LEGEND:
- A. Maximum output delay specification.
- B. Minimum output hold time.
- C. Minimum input setup time specification.
- D. Minimum input hold time specification.
- E. Signal valid to signal valid specification (maximum or minimum).
- F. Signal valid to signal invalid specification (maximum or minimum).

Figure 6. Drive Levels and Test Points for AC Specifications

DC ELECTRICAL SPECIFICATIONS (V_{CC} = 5.0 Vdc ± 5%; GND = 0 Vdc; $T_A = T_L$ to T_H)

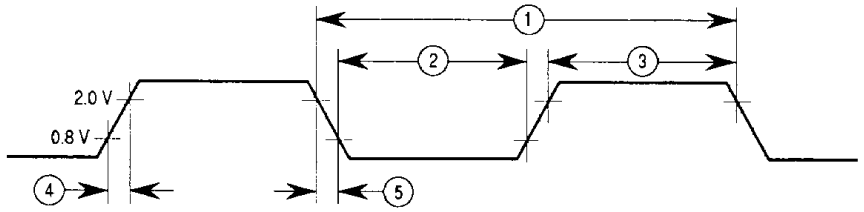
Characteristic		Symbol	Min	Max	Unit
Input High Voltage		V_{IH}	2.0	V_{CC}	V
Input Low Voltage		V_{IL}	GND 0.3	0.8	V
Input Leakage Current @ 5.25 V	$\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, CLK, $\overline{IPL0}$ $\overline{IPL2}$, $\overline{VPA}$ $\overline{HALT}$, $\overline{RESET}$	I_{IN}	— —	2.5 20	μA
Three-State (Off State) Input Current @ 2.4 V/0.4 V	$\overline{AS}$, A0–A18, A20, A21, D0–D7, FC0–FC2, $\overline{DS}$, R/$\overline{W}$, $\overline{VMA}$	I_{TSI}	—	20	μA
Output High Voltage (I_{OH} = −400 μA) (I_{OH} = −400 μA)	E* E, $\overline{AS}$, A0–A19, A20, A21, $\overline{BG}$, D0–D7, FC0–FC2, $\overline{DS}$, R/$\overline{W}$, $\overline{VMA}$	V_{OH}	V_{CC} − 0.75 2.4	— 2.4	V
Output Low Voltage (I_{OL} = 1.6 mA) (I_{OL} = 3.2 mA) (I_{OL} = 5.0 mA) (I_{OL} = 5.3 mA)	 $\overline{HALT}$ A0–A19, A20, A21, FC0–FC2 $\overline{RESET}$ E, $\overline{AS}$, D0–D7, $\overline{DS}$, R/$\overline{W}$, $\overline{VMA}$	V_{OL}	 — — — —	 0.5 0.5 0.5 0.5	V
Power Dissipation (see **POWER CONSIDERATIONS**)		P_D***	—	—	W
Capacitance (V_{in} = 0 V, T_A = 25°C, Frequency = 1 MHz)**		C_{in}	—	20.0	pF
Load Capacitance	$\overline{HALT}$ All Others	C_L	— —	70 130	pF

*With external pullup resistor of 1.1 Ω.
**Capacitance is periodically sampled rather than 100% tested.
***During normal operation, instantaneous V_{CC} current requirements may be as high as 1.5 A.

AC ELECTRICAL SPECIFICATIONS — CLOCK TIMING (see Figure 7)

Num.	Characteristic	Symbol	8 MHz*		10 MHz*		Unit
			Min	Max	Min	Max	
	Frequency of Operation	f	2.0	8.0	2.0	10.0	MHz
1	Clock Period	t_{cyc}	125	500	100	500	ns
2,3	Clock Pulse Width	t_{CL}, t_{CH}	55	250	45	250	ns
4,5	Clock Rise and Fall Times	t_{Cr}, t_{Cf}	—	10	—	10	ns

*These specifications represent an improvement over previously published specifications for the 8- and 10-MHz MC68008 and are valid only for product bearing date codes of 8827 and later.



NOTE: Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall will be linear between 0.8 V and 2.0 V.

Figure 7. Clock Input Timing Diagram

AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES

(V_{CC} = 5.0 Vdc ± 5%; GND = 0 Vdc; $T_A = T_L$ to T_H; see Figures 8 and 9)

Num.	Characteristic	Symbol	8 MHz*		10 MHz*		Unit
			Min	Max	Min	Max	
6	Clock Low to Address Valid	t_{CLAV}	—	62	—	50	ns
6A	Clock High to FC Valid	t_{CHFCV}	—	62	—	50	ns
7	Clock High to Address, Data Bus High Impedance (Maximum)	t_{CHADZ}	—	80	—	70	ns
8	Clock High to Address, FC Invalid (Minimum)	t_{CHAFI}	0	—	0	—	ns
9[1]	Clock High to $\overline{AS}$, $\overline{DS}$ Asserted	t_{CHSL}	3	60	3	50	ns
11[2]	Address Valid to $\overline{AS}$, $\overline{DS}$ Asserted (Read)/$\overline{AS}$ Asserted (Write)	t_{AVSL}	30	—	20	—	ns
11A[2]	FC Valid to $\overline{AS}$, $\overline{DS}$ Asserted (Read)/$\overline{AS}$ Asserted (Write)	t_{FCVSL}	90	—	70	—	ns
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ Negated	t_{CLSH}	—	62	—	50	ns
13[2]	$\overline{AS}$, $\overline{DS}$ Negated to Address, FC Invalid	t_{SHAFI}	40	—	30	—	ns
14[2]	$\overline{AS}$ (and $\overline{DS}$ Read) Width Asserted	t_{SL}	270	—	195	—	ns
14A[2]	$\overline{DS}$ Width Asserted (Write)	t_{DSL}	140	—	95	—	ns
15[2]	$\overline{AS}$, $\overline{DS}$ Width Negated	t_{SH}	150	—	105	—	ns
16	Clock High to Control Bus High Impedance	t_{CHCZ}	—	80	—	70	ns
17[2]	$\overline{AS}$, $\overline{DS}$ Negated to R/$\overline{W}$ Invalid	t_{SHRH}	40	—	30	—	ns
18[1]	Clock High to R/$\overline{W}$ High (Read)	t_{CHRH}	0	55	0	45	ns
20[1]	Clock High to R/$\overline{W}$ Low (Write)	t_{CHRL}	0	55	0	45	ns
20A[2, 6]	$\overline{AS}$ Asserted to R/$\overline{W}$ Valid (Write)	t_{ASRV}	—	10	—	10	ns
21[2]	Address Valid to R/$\overline{W}$ Low (Write)	t_{AVRL}	20	—	0	—	ns
21A[2]	FC Valid to R/$\overline{W}$ Low (Write)	t_{FCVRL}	60	—	50	—	ns
22[2]	R/$\overline{W}$ Low to $\overline{DS}$ Asserted (Write)	t_{RLSL}	80	—	50	—	ns
23	Clock Low to Data-Out Valid (Write)	t_{CLDO}	—	62	—	50	ns
25[2]	$\overline{AS}$, $\overline{DS}$ Negated to Data-Out Invalid (Write)	t_{SHDOI}	50	—	30	—	ns
26[2]	Data-Out Valid to $\overline{DS}$ Asserted (Write)	t_{DOSL}	40	—	30	—	ns
27[5]	Data-In Valid to Clock Low (Setup Time of Read)	t_{DICL}	10	—	10	—	ns
28[2]	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{DTACK}$ Negated (Asynchronous Hold)	t_{SHDAH}	0	245	0	190	ns
29	$\overline{AS}$, $\overline{DS}$ Negated to Data-In Invalid (Hold Time on Read)	t_{SHDII}	0	—	0	—	ns
29A	$\overline{AS}$, $\overline{DS}$ Negated to Data In High Impedance	t_{SHDZ}	—	187	—	150	ns
30	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{BERR}$ Negated	t_{SHBEH}	0	—	0	—	ns
31[2, 5]	$\overline{DTACK}$ Asserted to Data In Valid (Setup Time)	t_{DALDI}	—	90	—	65	ns
32	$\overline{HALT}$ and $\overline{RESET}$ Input Transition Time	$t_{RHr,f}$	0	200	0	200	ns
33	Clock High to $\overline{BG}$ Asserted	t_{CHGL}	—	62	—	50	ns
34	Clock High to $\overline{BG}$ Negated	t_{CHGH}	—	62	—	50	ns
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted	t_{BRLGL}	1.5	3.5	1.5	3.5	Clks
36[7]	$\overline{BR}$ Negated to $\overline{BG}$ Negated	t_{BRHGH}	1.5	3.5	1.5	3.5	Clks
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated (52-Pin Version Only)	t_{GALGH}	1.5	3.5	1.5	3.5	Clks
37A[8]	$\overline{BGACK}$ Asserted to $\overline{BR}$ Negated (52-Pin Version Only)	t_{GALBRH}	20	1.5 Clks	20	1.5 Clks	ns
38	$\overline{BG}$ Asserted to Control, Address, Data Bus High Impedance ($\overline{AS}$ Negated)	t_{GLZ}	—	80	—	70	ns
39	$\overline{BG}$ Width Negated	t_{GH}	1.5	—	1.5	—	Clks
41	Clock Low to E Transition	t_{CLET}	—	50	—	45	ns
42	E Output Rise and Fall Time	$t_{Er,f}$	—	15	—	15	ns
44	$\overline{AS}$, $\overline{DS}$ Negated to $\overline{VPA}$ Negated	t_{SHVPH}	0	120	0	90	ns

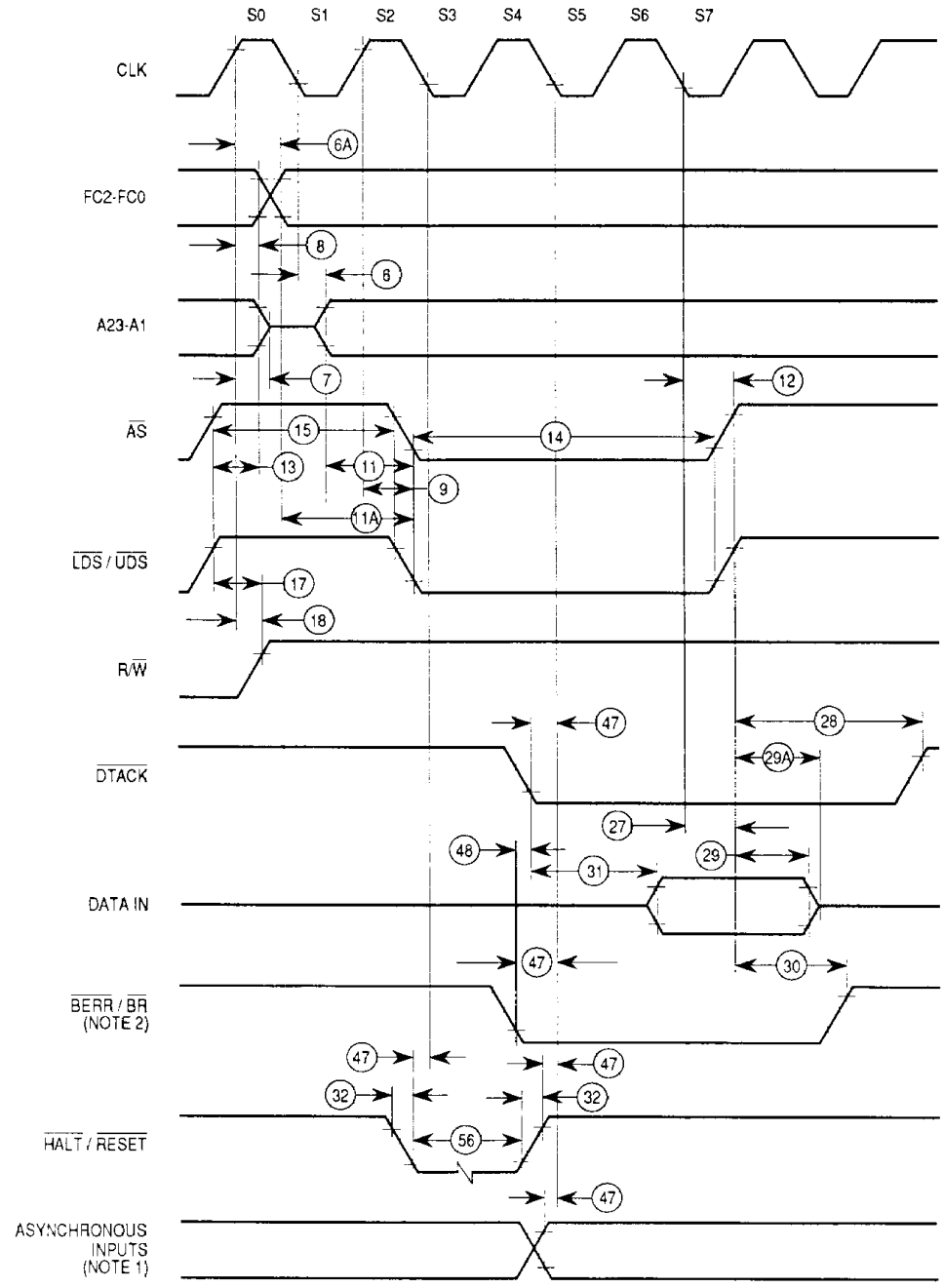
AC ELECTRICAL SPECIFICATIONS — READ AND WRITE CYCLES
(Continued)

Num.	Characteristic	Symbol	8 MHz*		10 MHz*		Unit
			Min	Max	Min	Max	
45	E Low to Control, Address Bus Invalid (Address Hold Time)	t_{ELCAI}	30	—	10	—	ns
46	$\overline{BGACK}$ Width Low (52-Pin Version Only)	t_{GAL}	1.5	—	1.5	—	Clks
47[5]	Asynchronous Input Setup Time	t_{ASI}	10	—	10	—	ns
48[2, 3]	$\overline{DTACK}$ Asserted to $\overline{BERR}$ Asserted	t_{BELDAL}	20	—	20	—	ns
49[9]	$\overline{AS}$, $\overline{DS}$, Negated to E Low	t_{SHEL}	70	70	55	55	ns
50	E Width High	t_{EH}	450	—	350	—	ns
51	E Width Low	t_{EL}	700	—	550	—	ns
53	Data-Out Hold from Clock High	t_{CHDOI}	0	—	0	—	ns
54	E Low to Data-Out Invalid	t_{ELDOI}	30	—	20	—	ns
55	R/$\overline{W}$ Asserted to Data Bus Impedance Change	t_{RLDBD}	30	—	20	—	ns
56[4]	$\overline{HALT}$/$\overline{RESET}$ Pulse Width	t_{HRPW}	10	—	10	—	Clks
57	$\overline{BGACK}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven (52-Pin Version Only)	t_{GASD}	1.5	—	1.5	—	Clks
57A	$\overline{BGACK}$ Negated to FC, $\overline{VMA}$ Driven (52-Pin Version Only)	t_{GAFD}	1	—	1	—	Clks
58[7]	$\overline{BR}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	t_{RHSD}	1.5	—	1.5	—	Clks
58A[7]	$\overline{BR}$ Negated to FC, $\overline{VMA}$ Driven	t_{RHFD}	1	—	1	—	Clks

*These specifications represent an improvement over previously published specifications for the 8- and 10-MHz MC68008 and are valid only for product bearing date codes of 8827 and later.

NOTES:

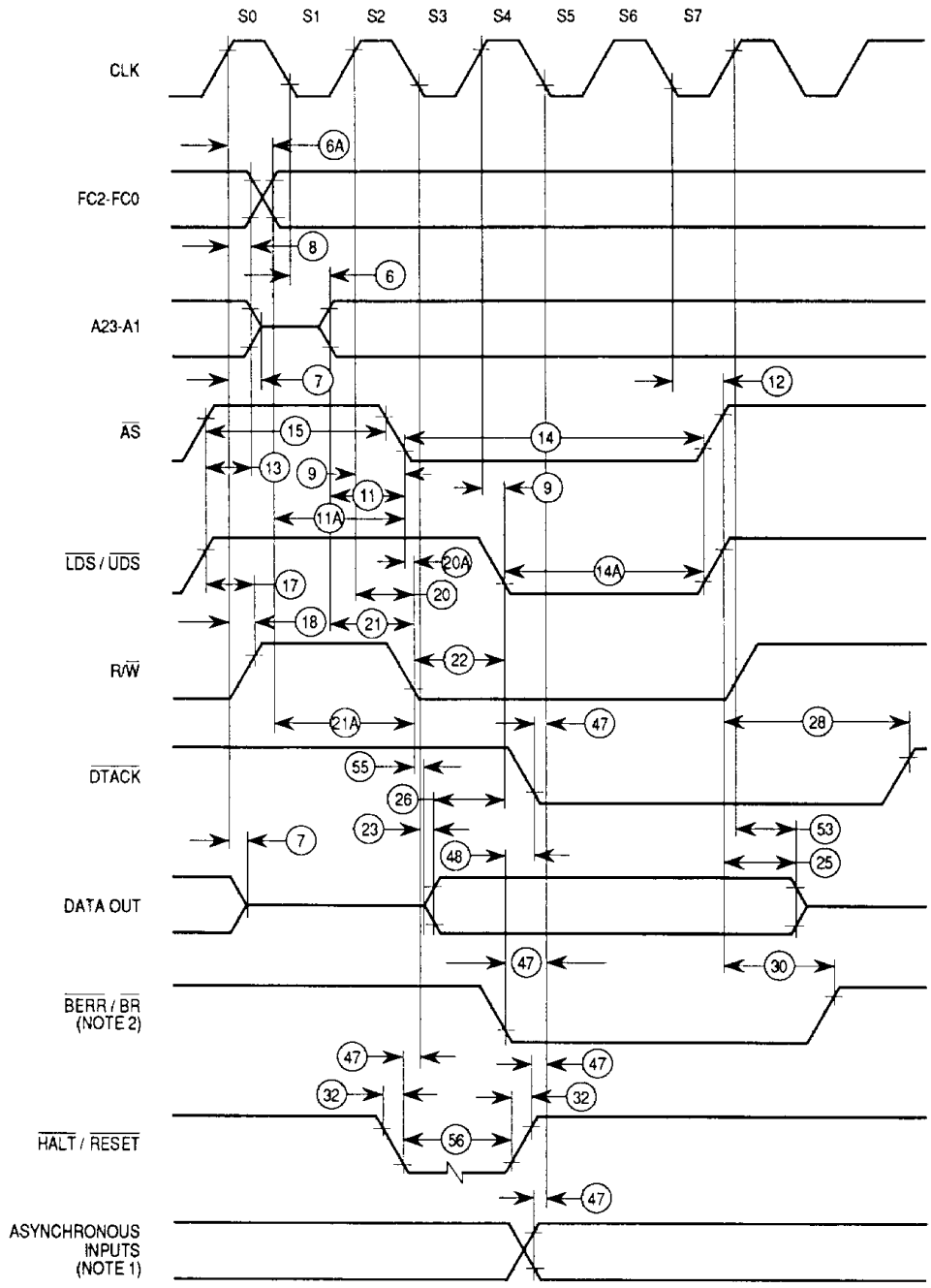
1. For a loading capacitance of less than or equal to 50 pF, subtract 5 ns from the value given in the maximum columns.
2. Actual value depends on clock period.
3. If #47 is satisfied for both $\overline{DTACK}$ and $\overline{BERR}$, #48 may be ignored. In the absence of $\overline{DTACK}$, $\overline{BERR}$ is an asynchronous input using the asynchronous input setup time (#47).
4. For power-up, the MC68008 must be held in the $\overline{RESET}$ state for 100 ms to allow stabilization of on-chip circuitry. After the system is powered up, #56 refers to the minimum pulse width required to reset the processor.
5. If the asynchronous input setup time (#47) requirement is satisfied for $\overline{DTACK}$, the $\overline{DTACK}$-asserted to data setup time (#31) requirement can be ignored. The data must only satisfy the data-in to clock low setup time (#27) for the following clock cycle.
6. When $\overline{AS}$ and R/$\overline{W}$ are equally loaded (±20%), subtract 5 ns from the values given in these columns.
7. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
8. The minimum value must be met to guarantee power operation. If the maximum value is exceeded, $\overline{BG}$ may be reasserted.
9. The falling edge of S6 triggers both the negation of the strobes ($\overline{AS}$ and $\overline{xDS}$) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal. Specification #49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of E.



NOTES:

1. Setup time for the asynchronous inputs $\overline{IPL2}$ / $\overline{IPL0}$, $\overline{IPL2}$, and VPA (#47) guarantees their recognition at the next falling edge of the clock.
2. $\overline{BR}$ need fall at this time only to ensure being recognized at the end of the bus cycle.
3. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.

Figure 8. Read Cycle Timing Diagram



NOTES:

1. Timing measurements are referenced to and from a low voltage of 0.8 V and a high voltage of 2.0 V, unless otherwise noted. The voltage swing through this range should start outside and pass through the range such that the rise or fall is linear between 0.8 V and 2.0 V.
2. Because of loading variations, R/$\overline{W}$ may be valid after $\overline{AS}$ even though both are initiated by the rising edge of S2 (specification #20A).

Figure 9. Write Cycle Timing Diagram

AC ELECTRICAL SPECIFICATIONS — PERIPHERAL CYCLES TO M6800

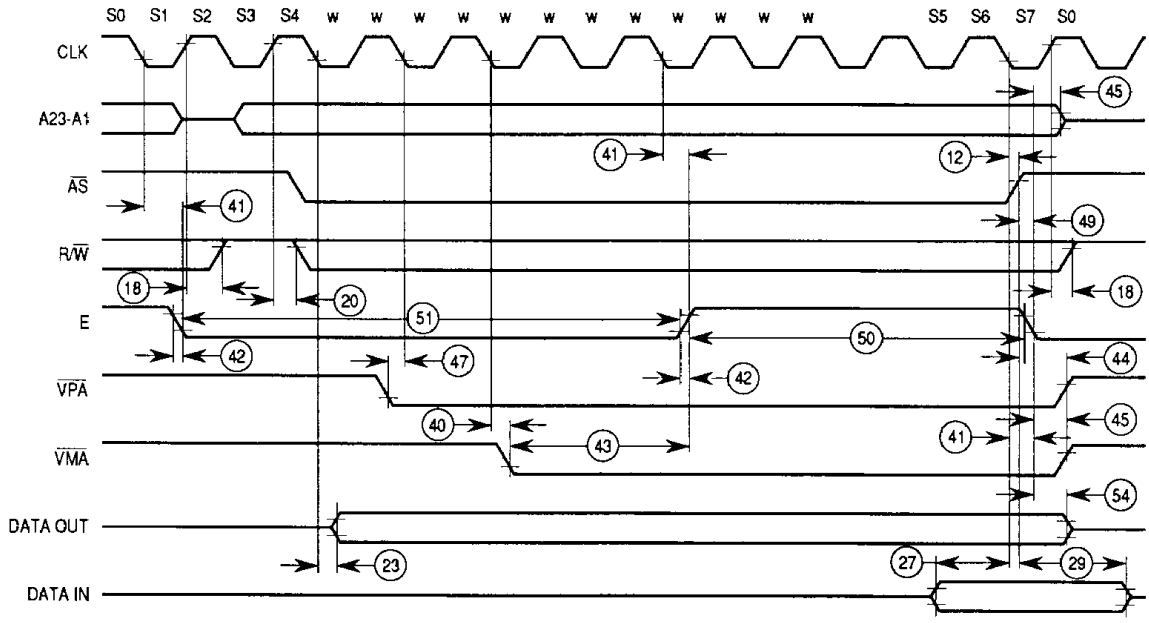
(V_{CC} = 5.0 Vdc ± 5%; GND = 0 Vdc; $T_A = T_L$ to T_H; see Figures 10 and 11)

Num.	Characteristic	Symbol	8 MHz*		10 MHz*		Unit
			Min	Max	Min	Max	
12[1]	Clock Low to $\overline{AS}$, $\overline{DS}$ Negated	t_{CLSH}	—	62	—	50	ns
18[1]	Clock High to R/$\overline{W}$ High (Read)	t_{CHRH}	0	55	0	45	ns
20[1]	Clock High to R/$\overline{W}$ Low (Write)	t_{CHRL}	0	55	0	45	ns
23	Clock Low to Data-Out Valid (Write)	t_{CLDO}	—	62	—	50	ns
27	Data-In Valid to Clock Low (Setup Time of Read)	t_{DICL}	10	—	10	—	ns
29	$\overline{AS}$, $\overline{DS}$ Negated to Data-In Invalid (Hold Time on Read)	t_{SHDII}	0	—	0	—	ns
41	Clock Low to E Transition	t_{CLET}	—	55	—	45	ns
42	E Output Rise and Fall Time	$t_{Er,f}$	—	15	—	15	ns
44	$\overline{AS}$, $\overline{DS}$ Negated to VPA Negated	t_{SHVPH}	0	120	0	90	ns
45	E Low to Control, Address Bus Invalid (Address Hold Time)	t_{ELCAI}	30	—	10	—	ns
47	Asynchronous Input Setup Time	t_{ASI}	10	—	10	—	ns
49[2]	$\overline{AS}$, $\overline{DS}$, Negated to E Low	t_{SHEL}	− 70	70	− 55	55	ns
50	E Width High	t_{EH}	450	—	350	—	ns
51	E Width Low	t_{EL}	700	—	550	—	ns
54	E Low to Data-Out Invalid	t_{ELDOI}	30	—	20	—	ns

*These specifications represent an improvement over previously published specifications for the 8- and 10-MHz MC68008 and are valid only for product bearing date codes of 8827 and later.

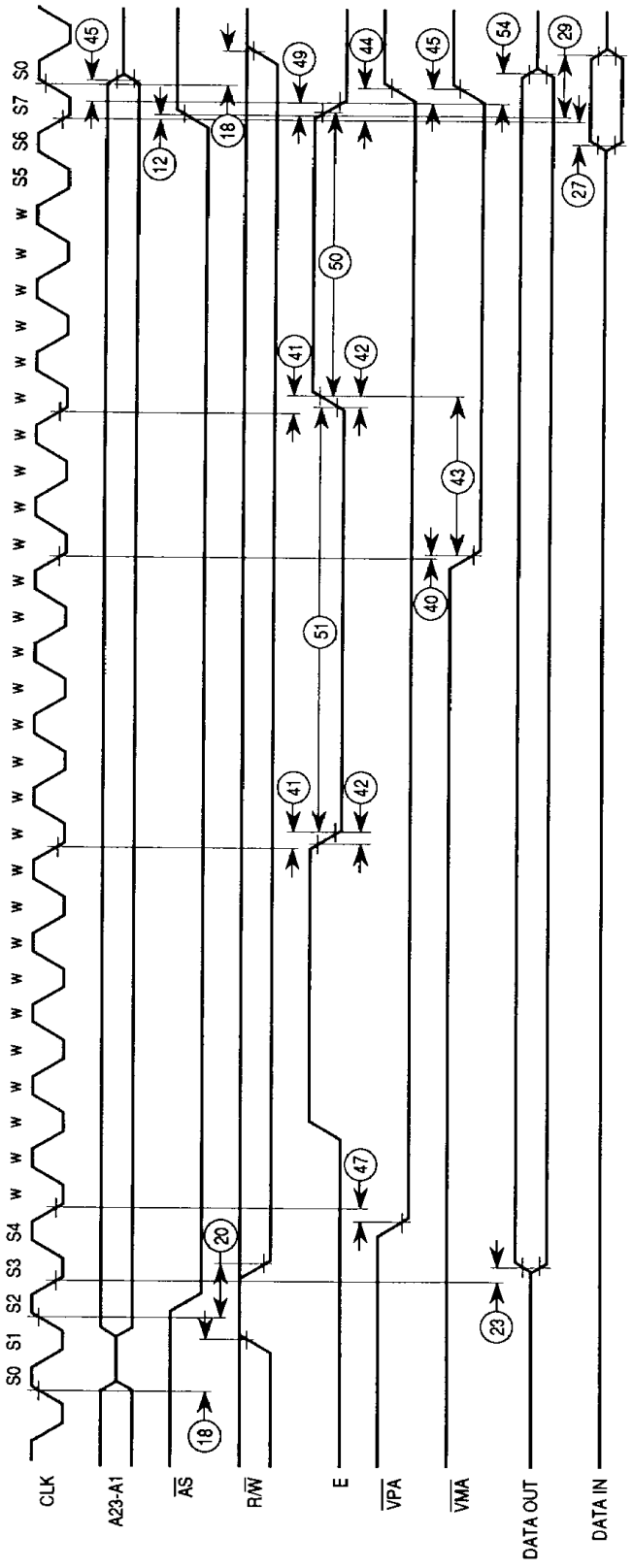
NOTES:

1. For a loading capacitance of less than or equal to 50 pF, subtract 5 ns from the value given in the maximum columns.
2. The falling edge of S6 triggers both the negation of the strobes ($\overline{AS}$ and $\overline{DS}$) and the falling edge of E. Either of these events can occur first, depending upon the loading on each signal. Specification #49 indicates the absolute maximum skew that will occur between the rising edge of the strobes and the falling edge of E.



NOTE: This timing diagram is included for those who wish to design their own circuit to generate $\overline{VMA}$. It shows the best case possibly attainable.

Figure 10. MC68008 to M6800 Peripheral Timing Diagram (Best Case)



NOTE: This timing diagram is included for those who wish to design their own circuit to generate VMA. It shows the worst case possibly attainable.

Figure 11. MC68008 to M6800 Peripheral Timing Diagram (Worst Case)

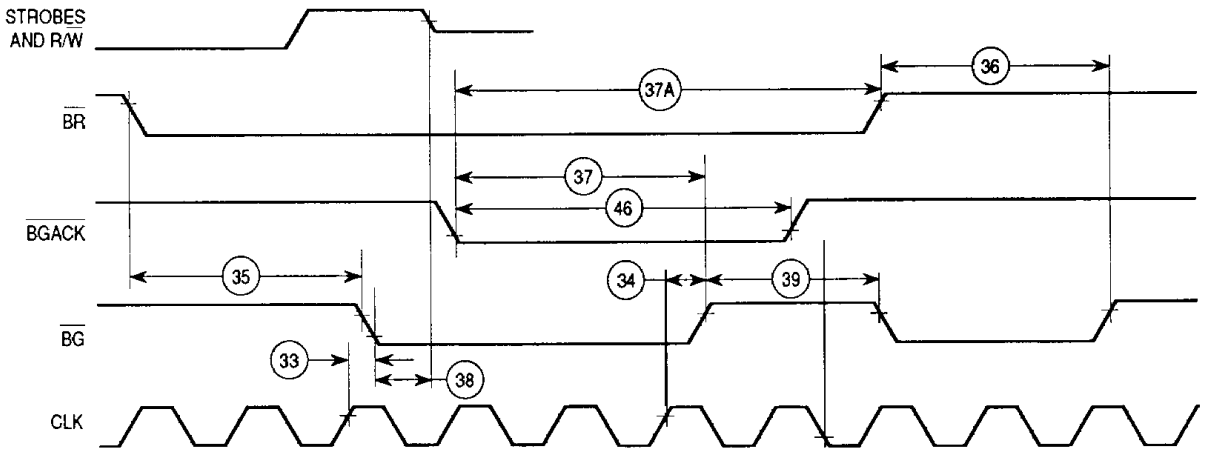
3

AC ELECTRICAL SPECIFICATIONS — BUS ARBITRATION (V_{CC} = 5.0 Vdc ± 5%; GND = 0 Vdc; $T_A = T_L$ to T_H; see Figures 12, 13, 14, and 15)

Num	Characteristic	Symbol	8 MHz*		10 MHz*		Unit
			Min	Max	Min	Max	
7	Clock High to Address, Data Bus High Impedance (Maximum)	t_{CHADZ}	—	80	—	70	ns
16	Clock High to Control Bus High Impedance	t_{CHCZ}	—	80	—	70	ns
33	Clock High to $\overline{BG}$ Asserted	t_{CHGL}	—	62	—	50	ns
34	Clock High to $\overline{BG}$ Negated	t_{CHGH}	—	62	—	50	ns
35	$\overline{BR}$ Asserted to $\overline{BG}$ Asserted	t_{BRLGL}	1.5	3.5	1.5	3.5	Clks
36[1]	$\overline{BR}$ Negated to $\overline{BG}$ Negated	t_{BRHGH}	1.5	3.5	1.5	3.5	Clks
37	$\overline{BGACK}$ Asserted to $\overline{BG}$ Negated	t_{GALGH}	1.5	3.5	1.5	3.5	Clks
37A[2]	$\overline{BGACK}$ Asserted to $\overline{BR}$ Negated	t_{GALBRH}	20	1.5 Clks	20	1.5 Clks	ns
38	$\overline{BG}$ Asserted to Control, Address, Data Bus High Impedance ($\overline{AS}$ Negated)	t_{GLZ}	—	80	—	70	ns
39	$\overline{BG}$ Width Negated	t_{GH}	1.5	—	1.5	—	Clks
46	$\overline{BGACK}$ Width Low	t_{GAL}	1.5	—	1.5	—	Clks
47	Asynchronous Input Setup Time	t_{ASI}	10	—	10	—	ns
57	$\overline{BGACK}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	t_{GASD}	1.5	—	1.5	—	Clks
57A	$\overline{BGACK}$ Negated to FC, $\overline{VMA}$ Driven	t_{GAFD}	1	—	1	—	Clks
58[1]	$\overline{BR}$ Negated to $\overline{AS}$, $\overline{DS}$, R/$\overline{W}$ Driven	t_{RHSD}	1.5	—	1.5	—	Clks
58A[1]	$\overline{BR}$ Negated to FC, $\overline{VMA}$ Driven	t_{RHFD}	1	—	1	—	Clks

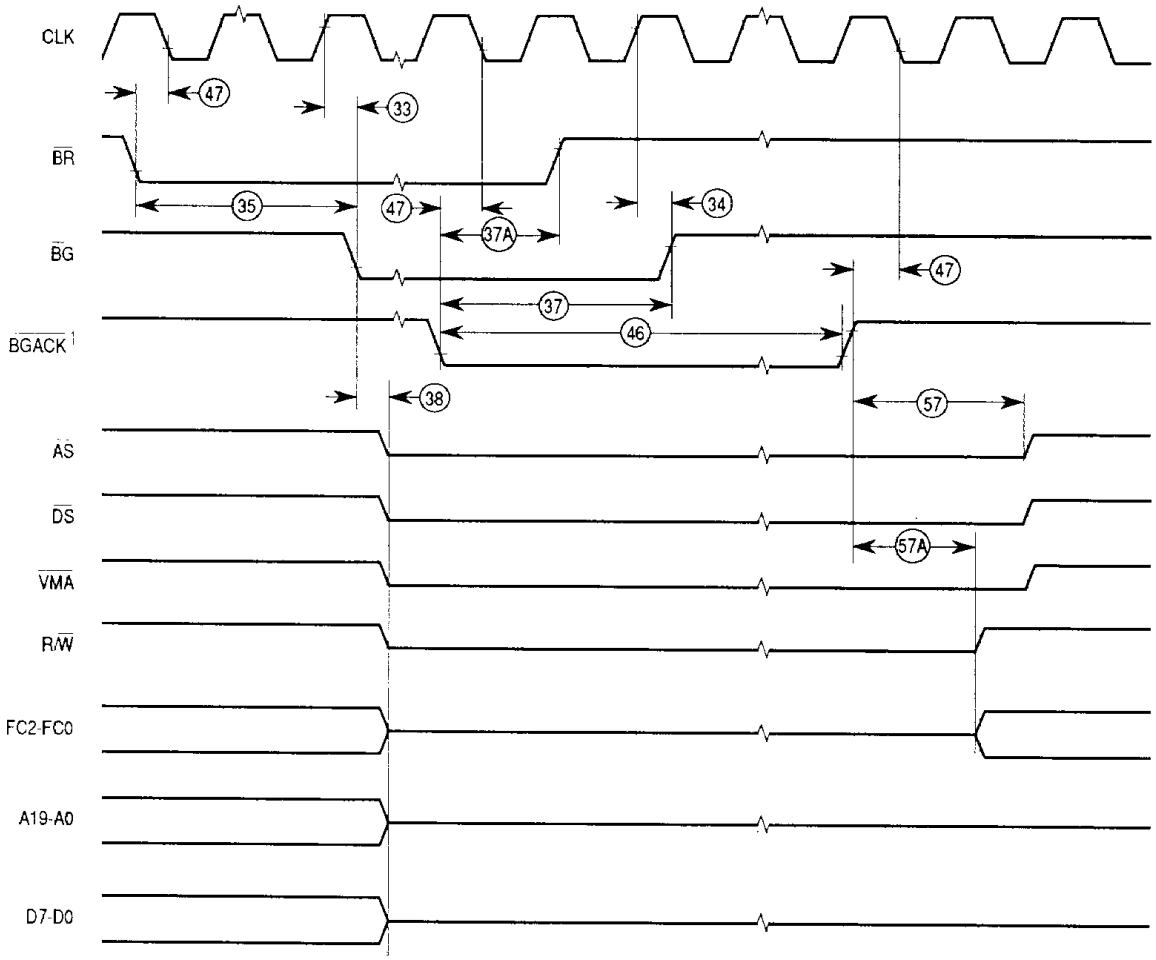
*These specifications represent an improvement over previously published specifications for the 8- and 10-MHz MC68008 and are valid only for product bearing date codes of 8827 and later.

NOTES:
1. The processor will negate $\overline{BG}$ and begin driving the bus again if external arbitration logic negates $\overline{BR}$ before asserting $\overline{BGACK}$.
2. The minimum value must be met to guarantee proper operation. If the maximum value is exceeded, $\overline{BG}$ may be reasserted.



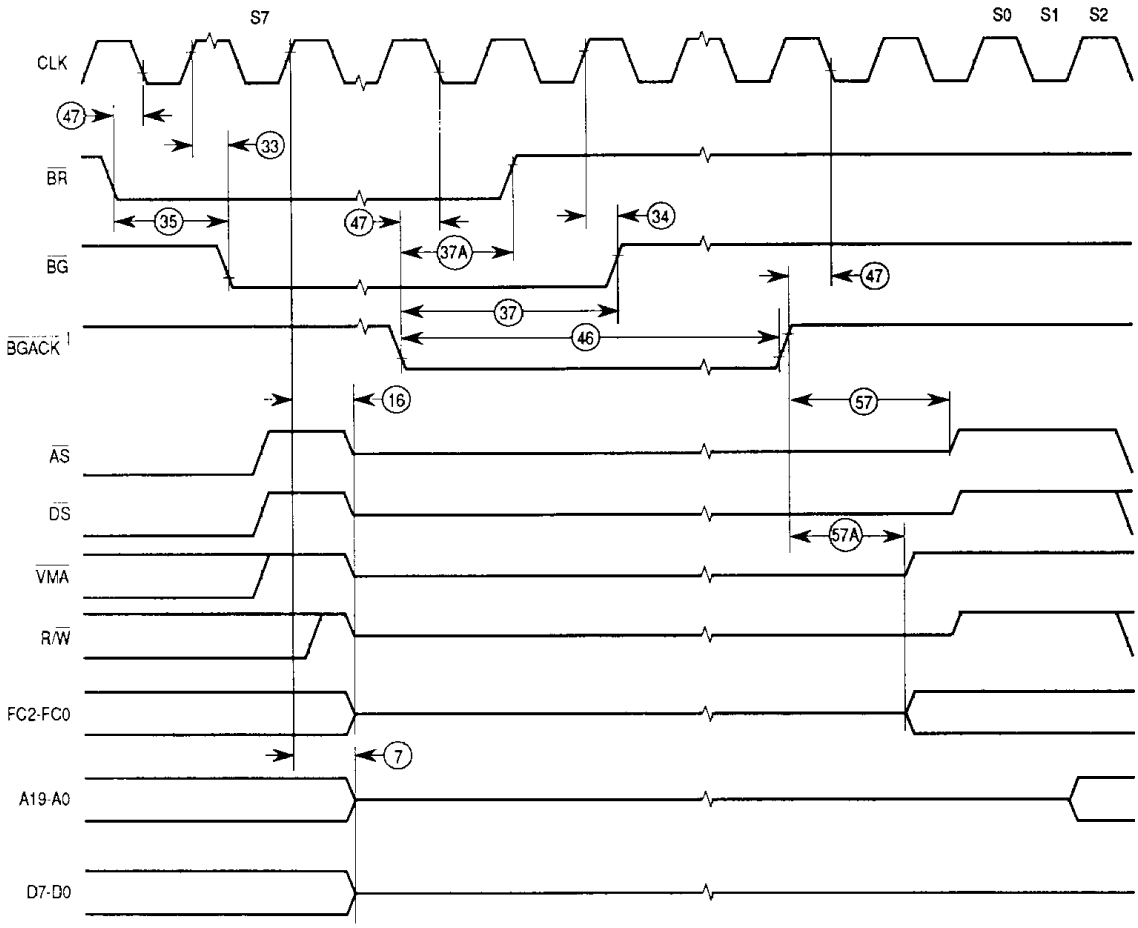
NOTE: Setup time to the clock (#47) for the asynchronous inputs $\overline{BERR}$, $\overline{BGACK}$, $\overline{BR}$, $\overline{DTACK}$, $\overline{IPL2}$-$\overline{IPL0}$, and $\overline{VPA}$ guarantees their recognition at the next falling edge of the clock.

Figure 12. Bus Arbitration Timing



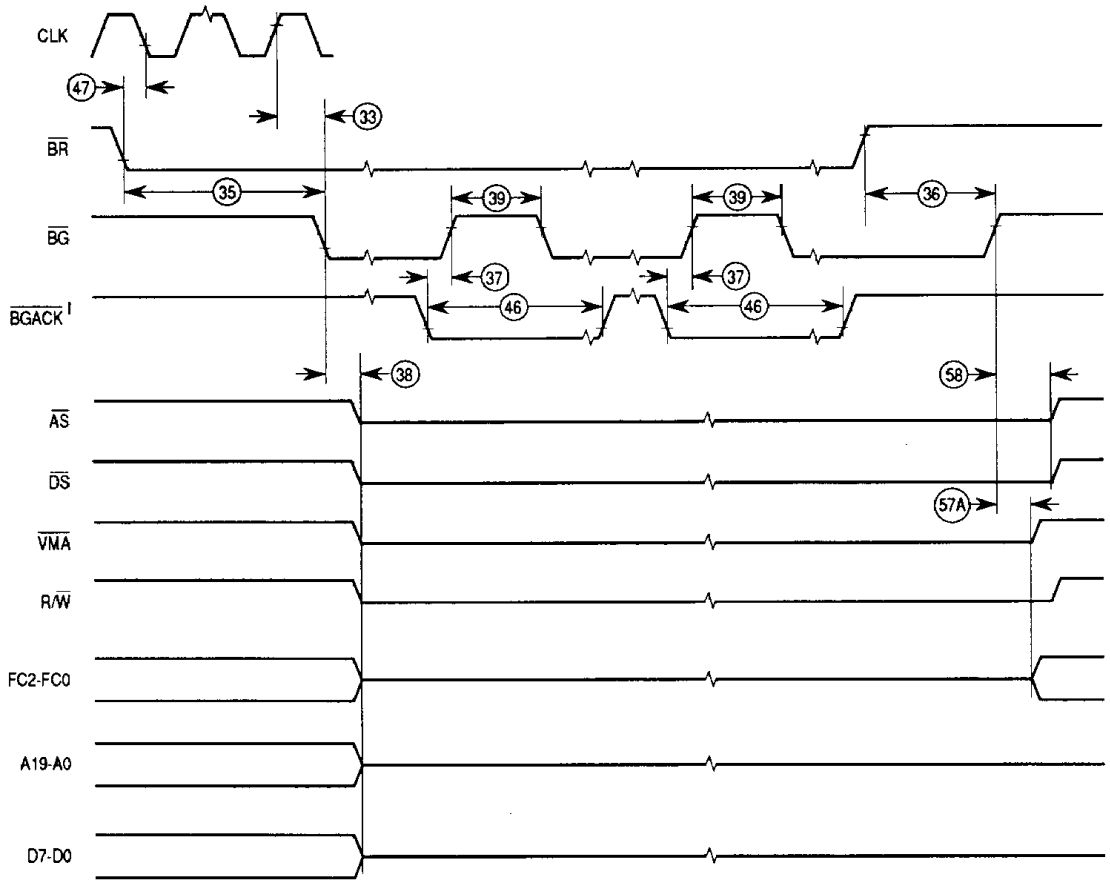
NOTES:
1. Setup time for the asynchronous inputs $\overline{BGACK}$ and $\overline{BR}$ (#47) guarantees their recognition at the next falling edge of the clock (52-pin version only).
2. Waveform measurements for all inputs and outputs are specified at: logic high 2.0 V, logic low = 0.8 V.

Figure 13. Bus Arbitration Timing — Idle Bus Case



NOTES:
1. Setup time for the asynchronous inputs BGACK and BR (#47) guarantees their recognition at the next falling edge of the clock (52 pin version only).
2. Waveform measurements for all inputs and outputs are specified at: logic high 2.0 V, logic low = 0.8 V.

Figure 14. Bus Arbitration Timing — Active Bus Case

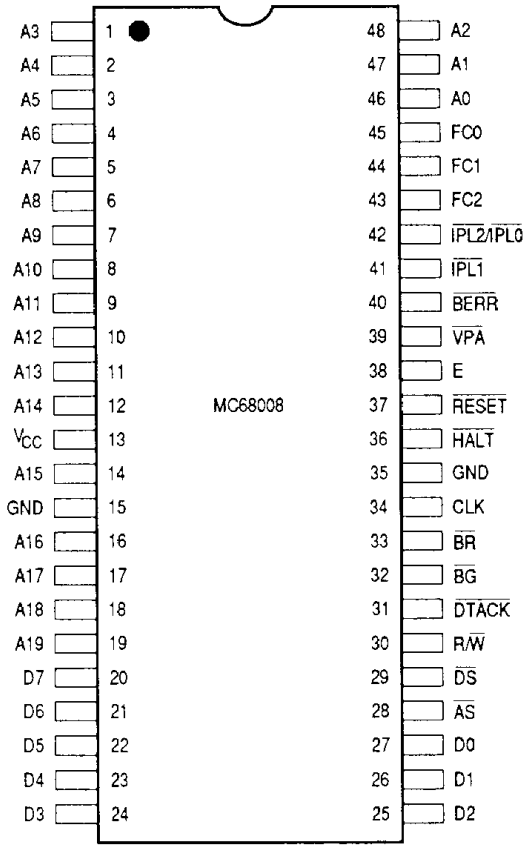


NOTES:
1. Setup time for the asynchronous inputs BGACK and BR (#47) guarantees their recognition at the next falling edge of the clock (52-pin version only).
2. Waveform measurements for all inputs and outputs are specified at: logic high 2.0 V, logic low = 0.8 V.

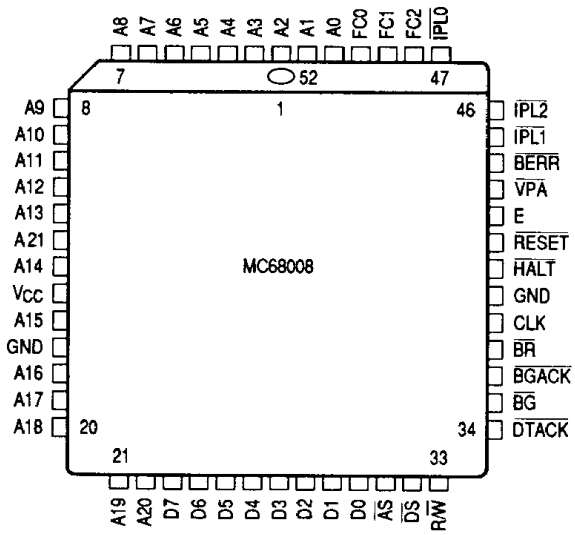
Figure 15. Bus Arbitration Timing — Multiple Bus Requests

PIN ASSIGNMENTS

48-LEAD DUAL-IN-LINE PACKAGE



52-LEAD QUAD PACKAGE



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