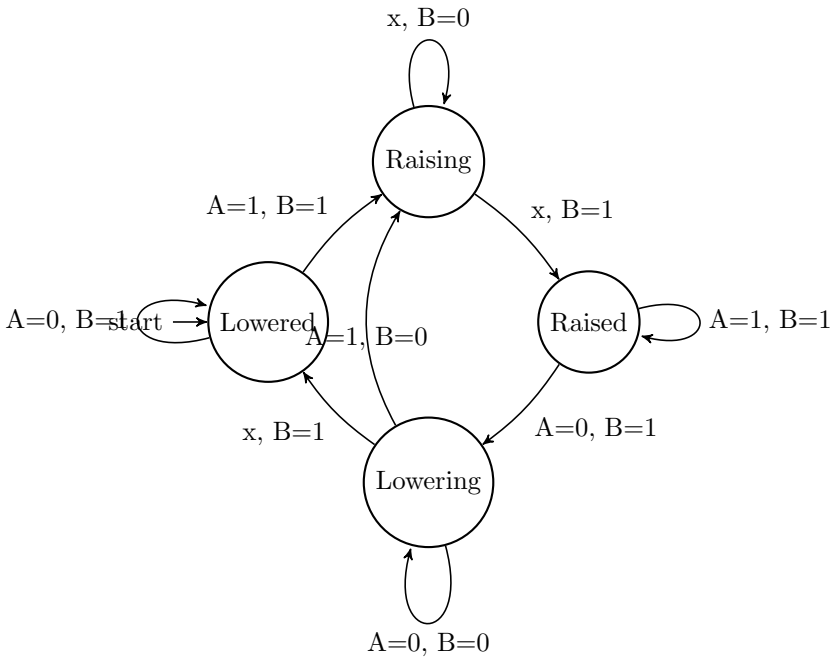
Part A: FSM State Diagram



FSM State Table for Gate Control System

Current State	Input A	Input B	New State
Lowered	0	1	Lowered
Lowered	1	1	Raising
Raising	x	0	Raising
Raising	x	1	Raised
Raised	0	1	Lowering
Raised	1	1	Raised
Lowering	0	0	Lowering
Lowering	1	0	Raising
Lowering	x	1	Lowered

FSM State Table with Flip-Flop Assignments and Ouput

State		Input		NextState			Output	
F1	**F0**	**A**	**B**	**NewF1**	**NewF0**	**State**	**R**	**L**
0	0	0	1	0	0	Lowered	0	0
0	0	1	1	0	1	Raising	1	0
0	1	x	0	0	1	Raising	1	0
0	1	x	1	1	0	Raised	0	0
1	0	0	1	1	1	Lowering	0	1
1	0	1	1	1	0	Raised	0	0
1	1	0	0	1	1	Lowering	0	1
1	1	0	1	0	0	Lowered	0	0
1	1	1	0	0	1	Raising	1	0

Complete truth table

$F1F0[1..0]$		A	B	$NewF1NewF0[1..0]$		R	L
0	0	0	0	0	1	1	0
0	0	0	1	0	0	0	0
0	0	1	0	0	1	1	0
0	0	1	1	0	1	1	0
0	1	0	0	0	1	1	0
0	1	0	1	1	0	0	0
0	1	1	0	0	1	1	0
0	1	1	1	1	0	0	0
1	0	0	0	1	1	0	1
1	0	0	1	1	1	0	1
1	0	1	0	1	1	1	0
1	0	1	1	1	0	0	0
1	1	0	0	1	1	0	1
1	1	0	1	0	0	0	0
1	1	1	0	0	1	1	0
1	1	1	1	0	0	0	0

This is a Mealy machine since its output depends on both current state and current input.

Part B

Table 1: Full State Transition Table with Inputs and Outputs

Step	**R1mul**	**R1en**	**R2mul**	**R2en**	**InSel**	**ASel**	**BSel**	**Done**	**NextStep**
000	0	1	x	0	01	11	00	0	001
001	1	1	0	0	00	11	01	0	010
010	1	1	0	0	00	11	01	0	011
011	x	0	0	1	10	11	00	0	100
100	x	0	1	1	00	11	10	0	101
101	0	1	x	0	xx	10	01	0	110
110	0	1	x	0	11	11	01	0	111
111	0	0	x	0	xx	xx	xx	1	111