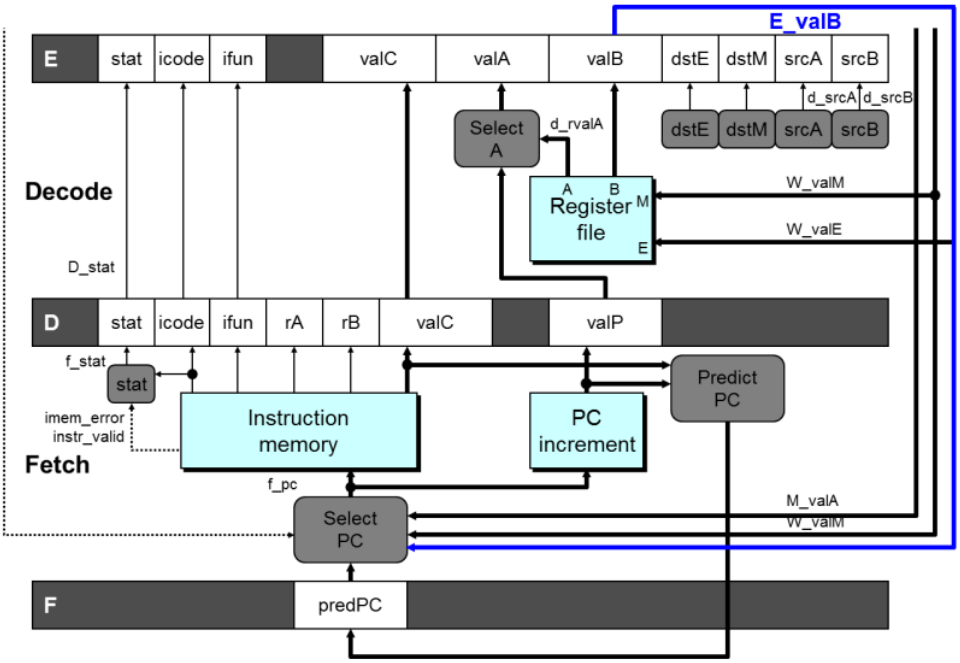
Homework 9

Pipeline

1. please write down the HCL code for the following signals in PIPE implementation. NOTE: You should refer to Chapter 4.5 of CSAPP book.
   a. d_valB
   b. D_stall
   c. E_bubble
2. What's the difference between signal e_dstE and E_dstE? When are they updated?
3. Suppose we add a new instruction rjmp rB to Y86 instruction sets. It will jmp to the address stored in rB.
   a. Fill in the function of each stage for rjmp rB instruction in Y86 sequential implementation. (NOTE: use valB to update PC)

Stage	rjmp rB
F	
D	
E	
M	
W	
P	

   b. As shown in the new PIPE logic figure, we add a forwarding logic from E_valB to f_pc to support rjmp instruction, since the target address require read from register file. Please describe all possible hazards due to new instruction rjmp. You need provide detail explanation and list detection conditions like Figure 4.64 and control action like Figure 4.66. (Do not consider the hazard combinations here.)



c. Please list all hazard combinations (arise simultaneously) including rjmp instruction. You need draw pipeline states figures like Figure 4.67 and list pipeline control action like tables after Figure 4.67 for each combination.

d. The original PIPE implementation of Y86 should be modified to support the rjmp instruction. Please describe the modification and provide HCL of f_pc and D_bubble logic. (NOTE: Only need to write the code about rjmp instruction)