1.

Field	rcall rB valC	rret rB
Fetch	icode:ifun ← M1[PC] rA:rB ← M1[PC+1]= F:rB valC ← M8[PC+2] valP ← PC + 10	icode:ifun ← M1[PC] rA:rB ← M1[PC+1]= F:rB valP ← PC + 2
Decode	--	valB ← R[rB]
Execute	--	valE ← 0 + valB
Memory	--	--
Write Back	R[rB] ← valP	--
PC update	PC ← valC	PC ← valE

2.

Condition	Trigger
Target-addr Hazard	IRRET in { D_icode,E_icode,M_icode }

Condition	Pipeline register				
	F	D	E	M	W
Target-addr Hazard	S	B	-	-	-

3.

Condition	Trigger
Target-addr Hazard	IRRET in { D_icode }

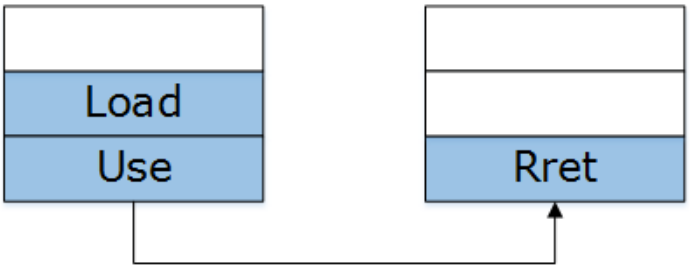
Condition	Pipeline register				
	F	D	E	M	W
Target-addr Hazard	S	B	-	-	-

4.

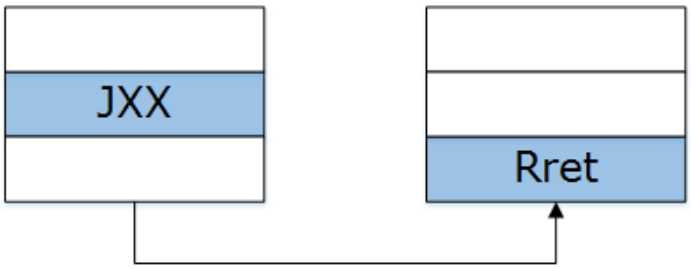
```
int f_pc = [
    E_icode == IRRET  : E_valB;
];

bool F_stall =
    #Stalling at fetch before ret forwarding the E_valB
    D_icode == IRRET

bool D_stall = (nothing need to be add)
```

```
bool D_bubble =

    # Stalling at fetch while ret forwarding the E_valB
    IRET in { D_icode,}
```

5.



Condition	F	D	E	M	W
Load	Stall	Stall	Bubble	Normal	Normal
RRET	Stall	Bubble	Normal	Normal	Normal
Combination	Stall	B+S	Bubble	Normal	Normal
Desired	Stall	Stall	Bubble	Normal	Normal



Condition	F	D	E	M	W
Mispredicted branch	Normal	Bubble	Bubble	Normal	Normal
RRET	Stall	Bubble	Normal	Normal	Normal
Combination	Stall	Bubble	Bubble	Normal	Normal

6. 25/8 21/4

7. 不能正确 forwarding。

Decode 阶段，需要一段时间才能读取寄存器的值，而在 fetch 阶段一开始便需要 select pc，无法等到 decode 读完寄存器后再 forward 过来。