NC State University
Department of Electrical and Computer Engineering
ECE 463/521: Fall 2016
Project #3: Dynamic Instruction Scheduling

by

Zach Hannum

NCSU Honor Pledge: "I have neither given nor received unauthorized aid on this test or assignment."

Student’s electronic signature: Zach Hannum
(sign by typing your name)

Course number: 463
(463 or 521?)

Contents

1.1 Effects of IQ_SIZE with a large ROB

Plot

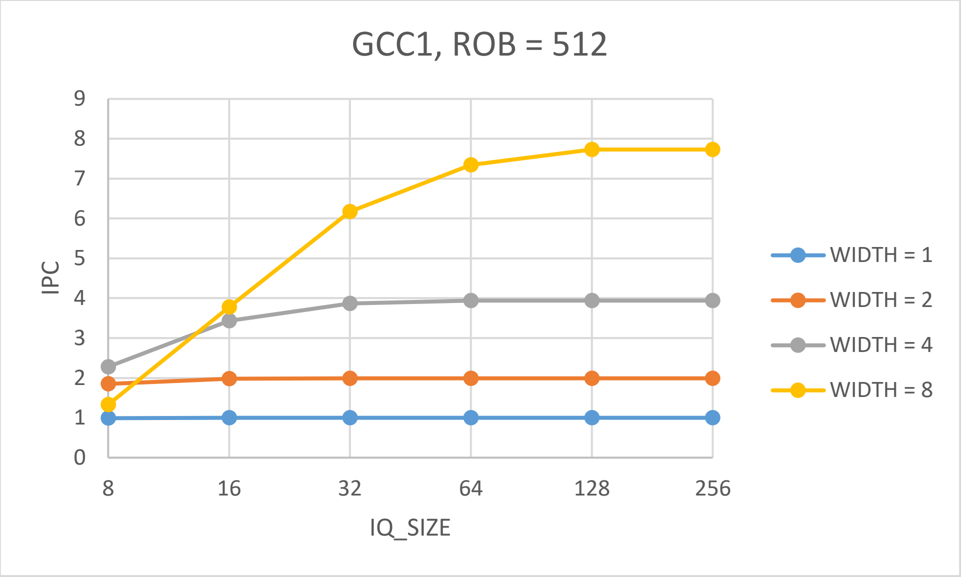

Figure 1: GCC benchmark, effects of IQ_SIZE

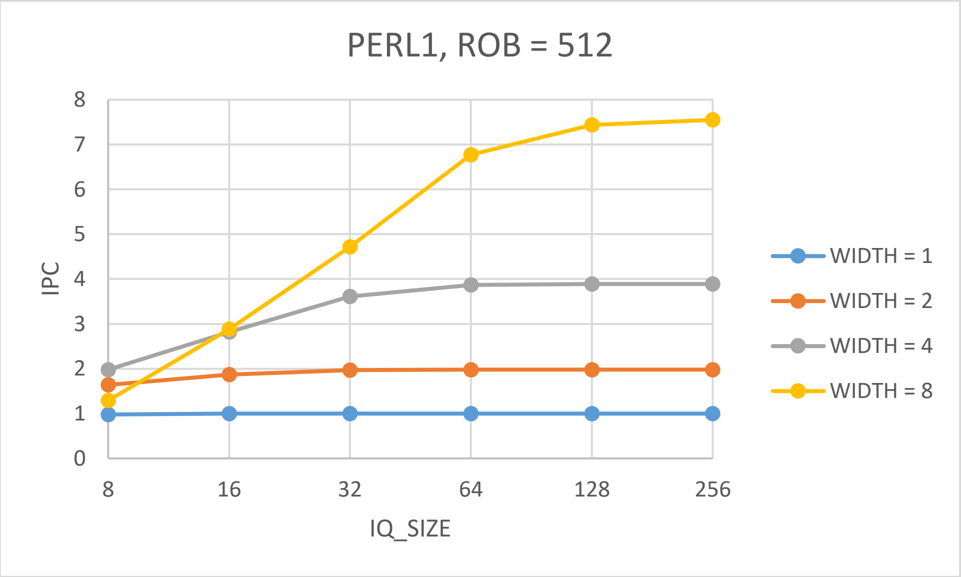

Figure 2: PERL benchmark, effects of IQ_SIZE

Analysis

Optimized IQ_SIZE per WIDTH
Minimum IQ_SIZE that still achieves within 5% of the IPC of the largest IQ_SIZE

	GCC	**PERL**
WIDTH = 1	IQ_SIZE = 8	IQ_SIZE = 8
WIDTH = 2	IQ_SIZE = 16	IQ_SIZE = 16
WIDTH = 4	IQ_SIZE = 32	IQ_SIZE = 64
WIDTH = 8	IQ_SIZE = 64	IQ_SIZE = 128

Discussion

If the goal of a superscalar processor is to achieve an IPC close to WIDTH of the machine, the relationship between WIDTH and IQ_SIZE, extrapolated from the table above, should be that as WIDTH gets larger, IQ_SIZE should as well. For the best performance/cost ratio, the IQ_SIZE should be ~8 times larger than WIDTH.

The GCC and PERL benchmarks end up with different IPCs. For instance, at WIDTH = 8, GCC's highest IPC reached is 7.73, while PERL's is only 7.55. This difference simply comes down to the actual instructions being processed through the pipeline. GCC's trace could be a more "ideal" case, while the PERL trace is more "challenging" for the pipeline, causing more stalls due to dependences.

1.2 Effect of ROB_SIZE

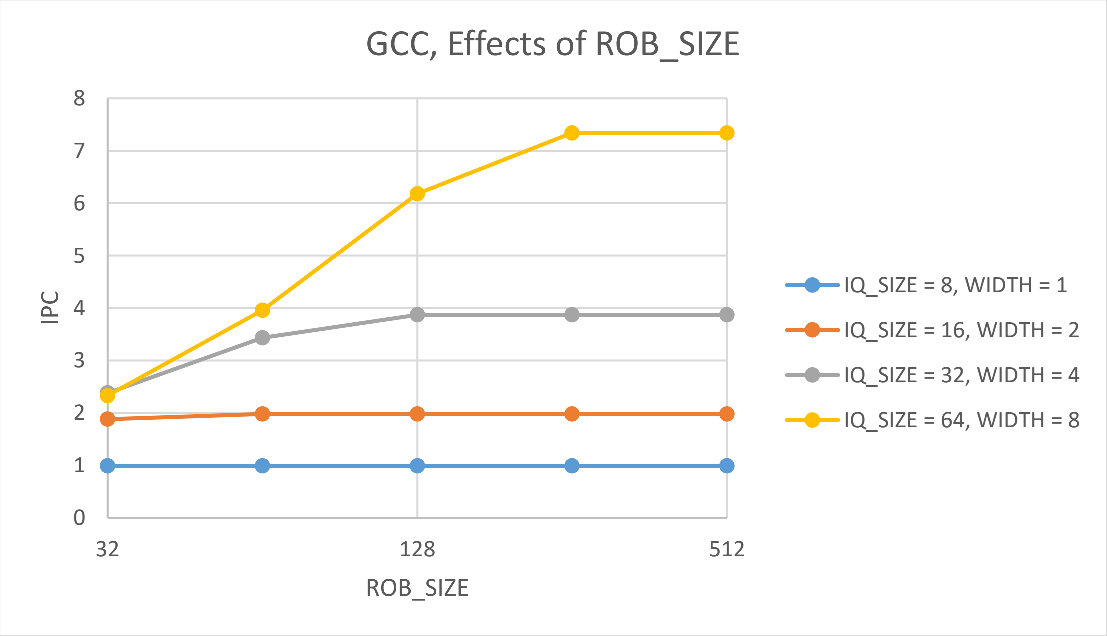

Figure 3: GCC benchmark, effects of ROB_SIZE

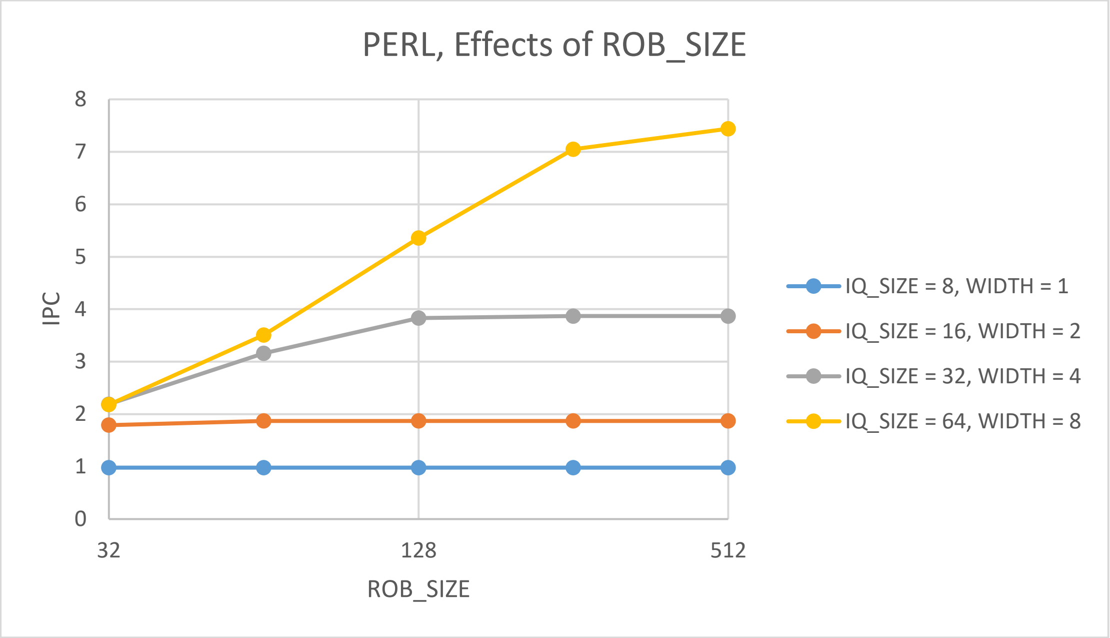

Figure 4: Perl benchmark, effects of ROB_SIZE

1.3 Effect of Instruction Cache

Plot

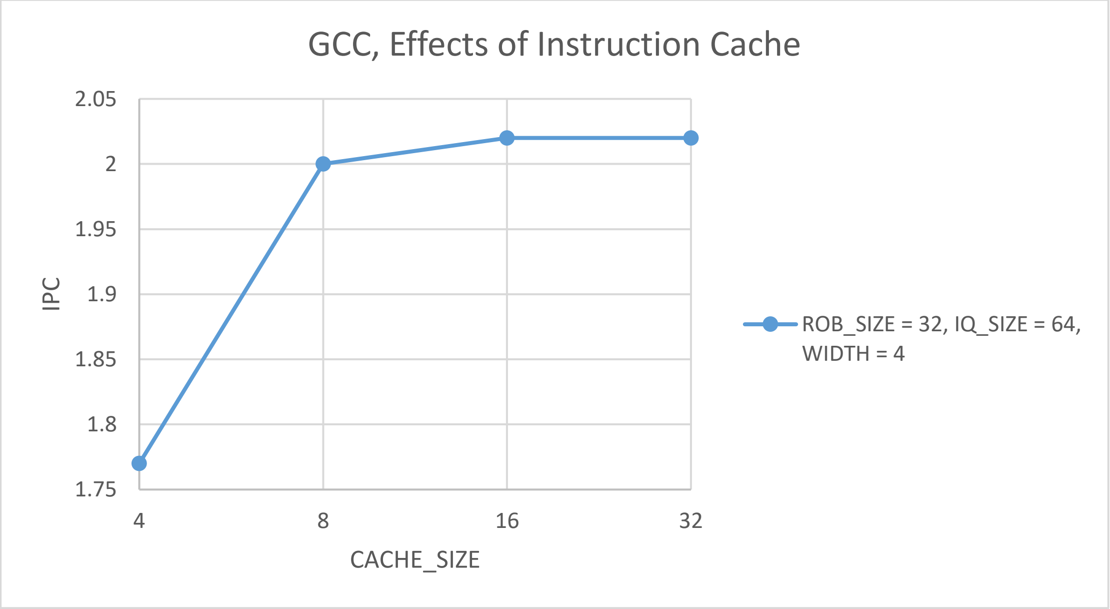

Figure 5: GCC benchmark, effects of instruction cache

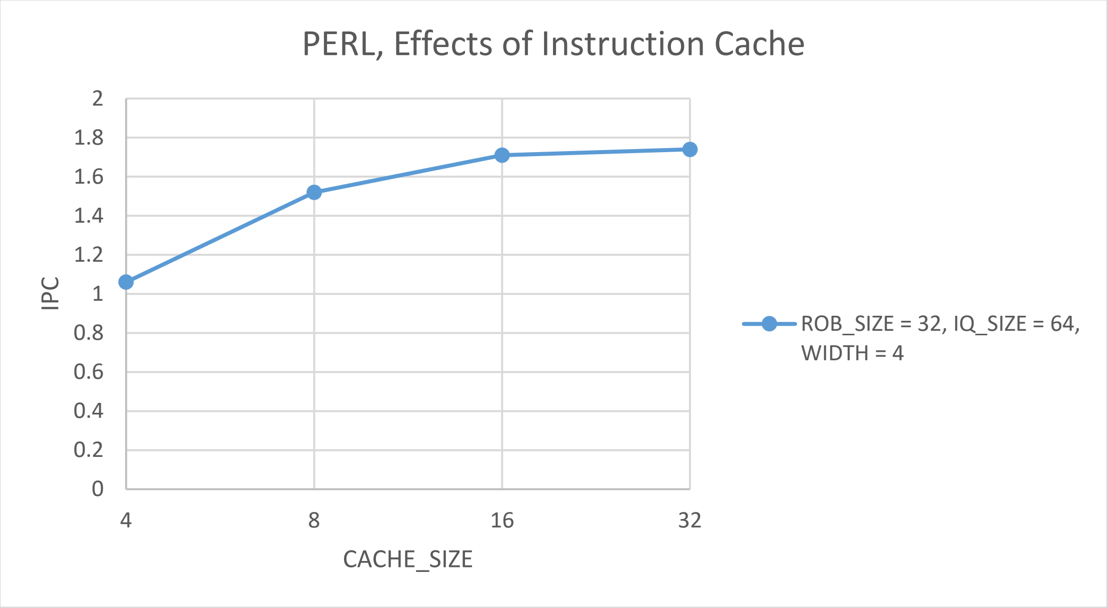

Figure 6: PERL benchmark, effects of instruction cache

Analysis

Overall, the inclusion of the instruction cache makes IPC worse. Without the instruction cache, the pipeline assumes a perfect cache hit rate, so the IPC in those cases (sections 1.1 and 1.2) are the most ideal. However, increasing the instruction cache size nearly doubles the IPC.

1.4 Effect of Prefetching

Plot

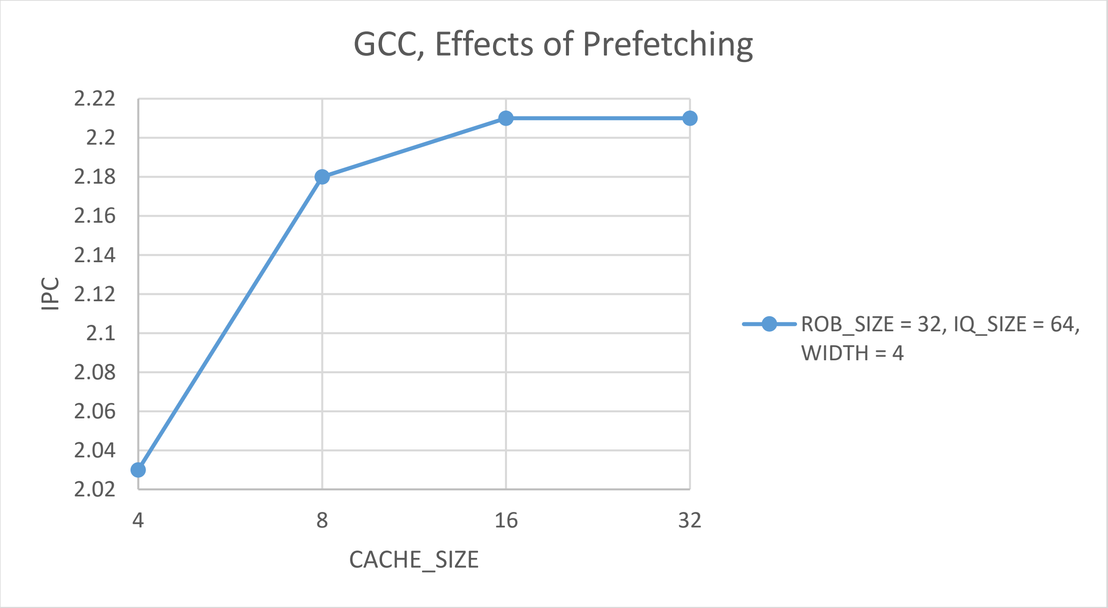

Figure 7: GCC benchmark, effects of prefetching

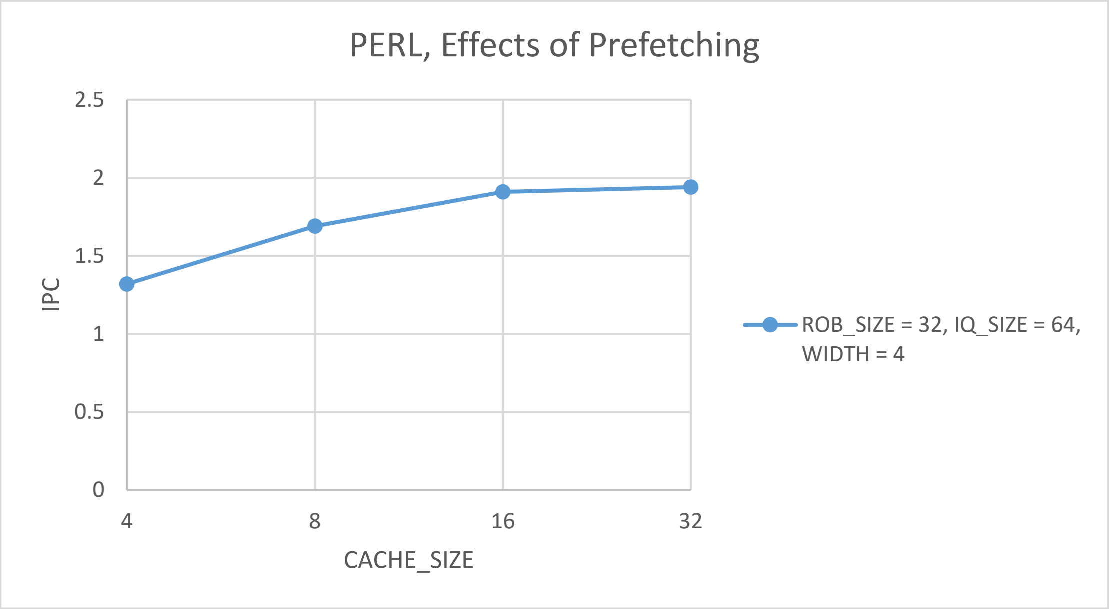

Figure 8: PERL benchmark, effects of prefetching

Analysis

With prefetching enabled, the IPC shows improvements. In both cases, the effects of prefetching are greatest with a smaller cache size. For instance, with the GCC benchmark, prefetching with CACHE_SIZE = 4 has nearly the same IPC as CACHE_SIZE = 32 without prefetching. In the case of the PERL benchmark, prefetching with a CACHE_SIZE = 8 yields close to the IPC of CACHE_SIZE = 32 without prefetching.