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Question: 4-5 The FET input voltmeter circuit in Figure 4-4 has the followi...

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4-5 The FET input voltmeter circuit in Figure 4-4 has the following components: $R_1 = 6.8 \text{ k}\Omega$, $R_2 = R_3 = 4.7 \text{ k}\Omega$, $R_4 = 1.5 \text{ k}\Omega$, $R_5 = 500 \Omega$, $R_6 = 3.3 \text{ k}\Omega$, $R_s + R_m = 20 \text{ k}\Omega$. The meter full-scale current is 50 μ A, the supply voltage is $\pm 10 \text{ V}$, the transistors

have $h_{FE} = 80$, and the FET gate-source voltage is $V_{GS} = -3$ V. Determine V_p , I_s , I_2 , I_3 , and I_4 when E = 0. Also, calculate the range of adjustment for V_p .

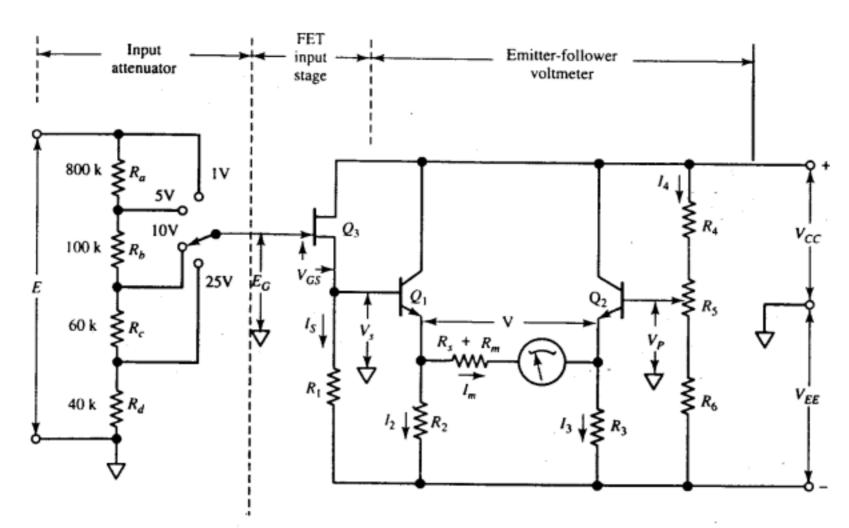
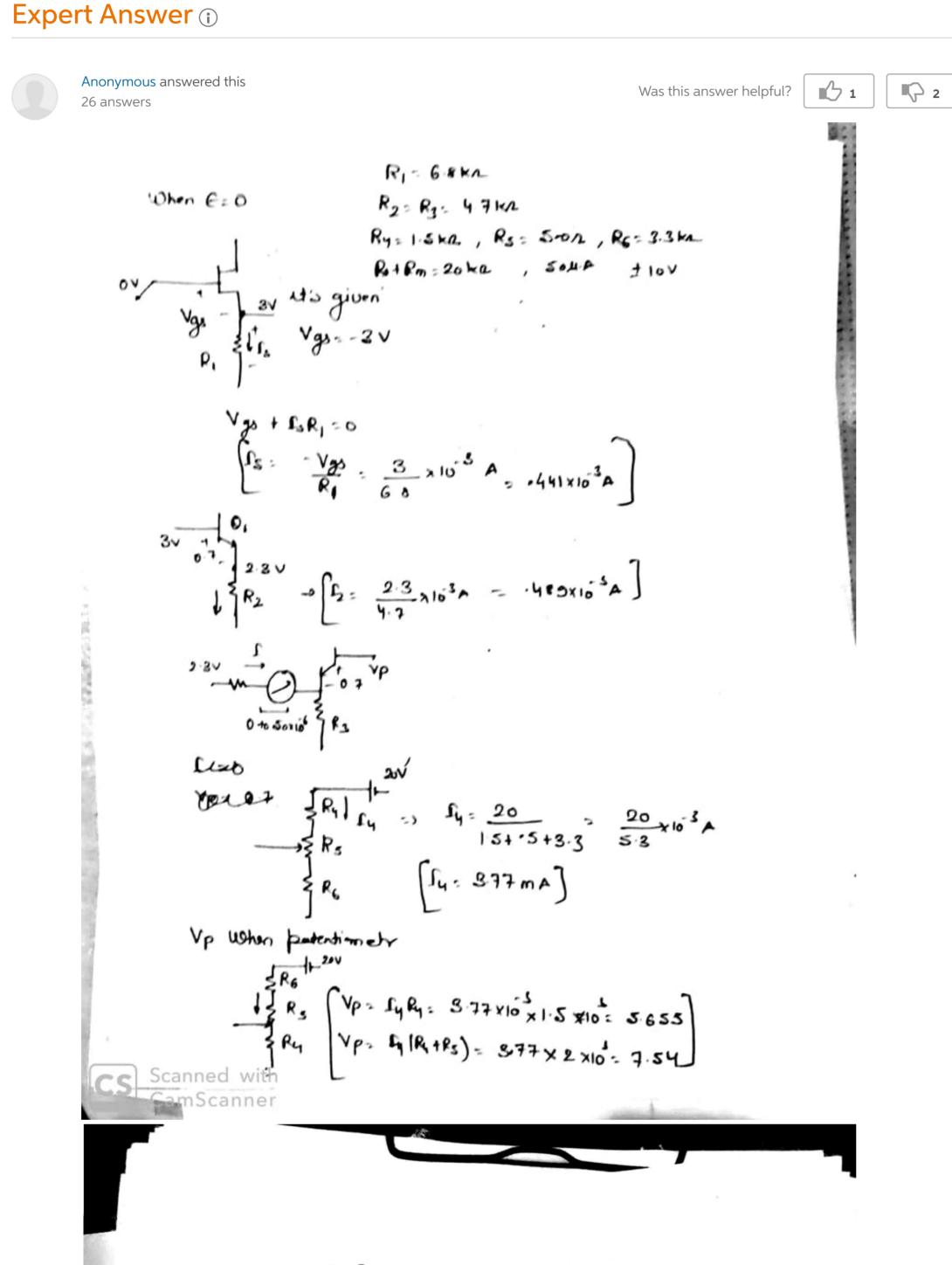


Figure 4-4 A voltmeter input attenuator is simply a potential divider that accurately divides the voltage to be measured. The FET input stage (Q_3) gives the emitter follower a very high input resist-

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A: See answer

Q: EE 303 solve all this problem please

A: See answer 100% (1 rating)

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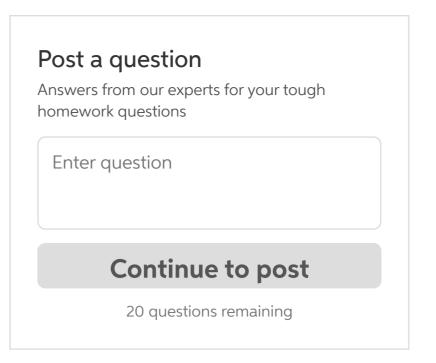
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