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Lab 5: The MIPS datapath in Verilog: The Write-Back stage

Introduction: This lab implements the final stage of the MIPS five stage pipeline. This stage consists of only one component: mux

mux:

The write-back stage consists of only one module: a multiplexer. Its output goes to reg.v as the input for write_data of I_DECODE.
The inputs are mem_Read_data, mem_ALU_result, and MemtoReg which are the outputs of the MEM/WB latch.

Timing Diagram for WB during the MIPS data_path testing of Lab 6