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Class: CSE 401
Term: Spring 2016

## Lab 3: The MIPS datapath in Verilog: The Execute stage

Introduction: This lab implements the third stage of the MIPS five stage pipeline. This stage consists of six components: adder, bottom_mux, alu_control, alu, top_mux, and ex_mem.

### adder:

Adds two 32-bit inputs to output a 32-bit value. Takes in npcout and s_extendout to output adder_out.

### bottom_mux:

Implements a multiplexer that selects from two inputs (5 bits), a and b, based on the sel input. Its inputs are instrout_1511 and instrout_2016 from ID/EX latch, and regdst. The output is muxout, which is sent to EX/MEM latch.

### alu_control:

Takes in 6 bit of s_extendout with alu_op and outputs select, which is the control. for alu.v. This bridges machine language with assembly language.

### alu:

Takes in rdata1 as its input as well as "b," which is the output of top_mux.
It outputs result, later known as aluout, and zero, which is then aluzero for ex_mem.v.
This handles the logical and arithmetic correspondence.

### top_mux:

Implements a multiplexer that selects from two inputs (32 bits), a and b, based on the sel input. Its inputs are rdata2 ID/EX latch and aluscr from alu_control.v
The output becomes the b input of alu.v

### ex_mem:

This is the latch that receives signals form all the modules of the execute stage. Its outputs go to MEM/WB and FETCH.

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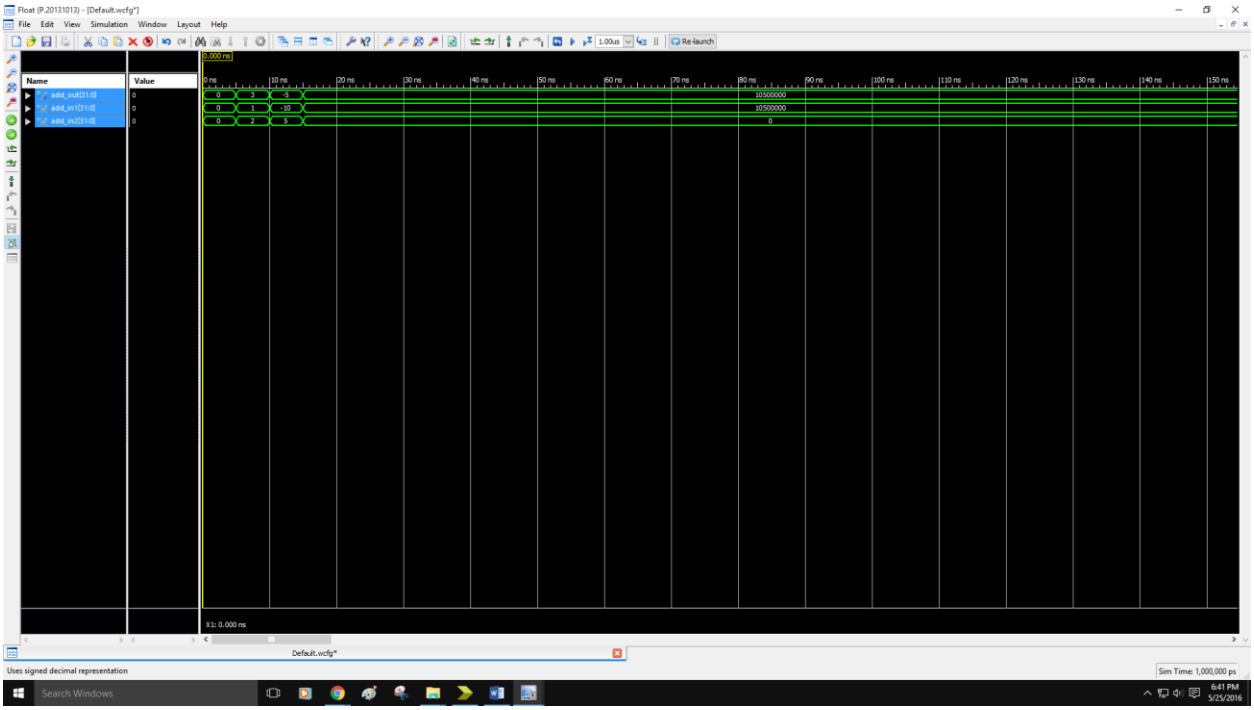
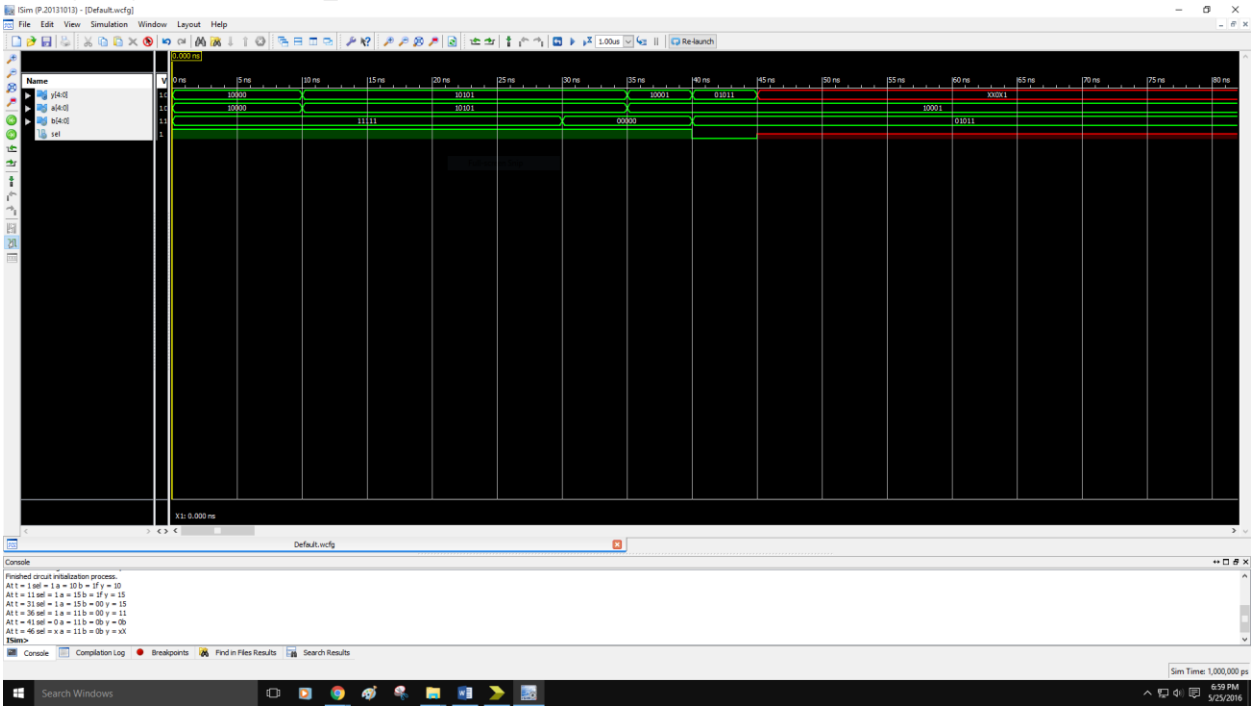
## Timing Diagram for adder



## Timing Diagram for bottom_mux



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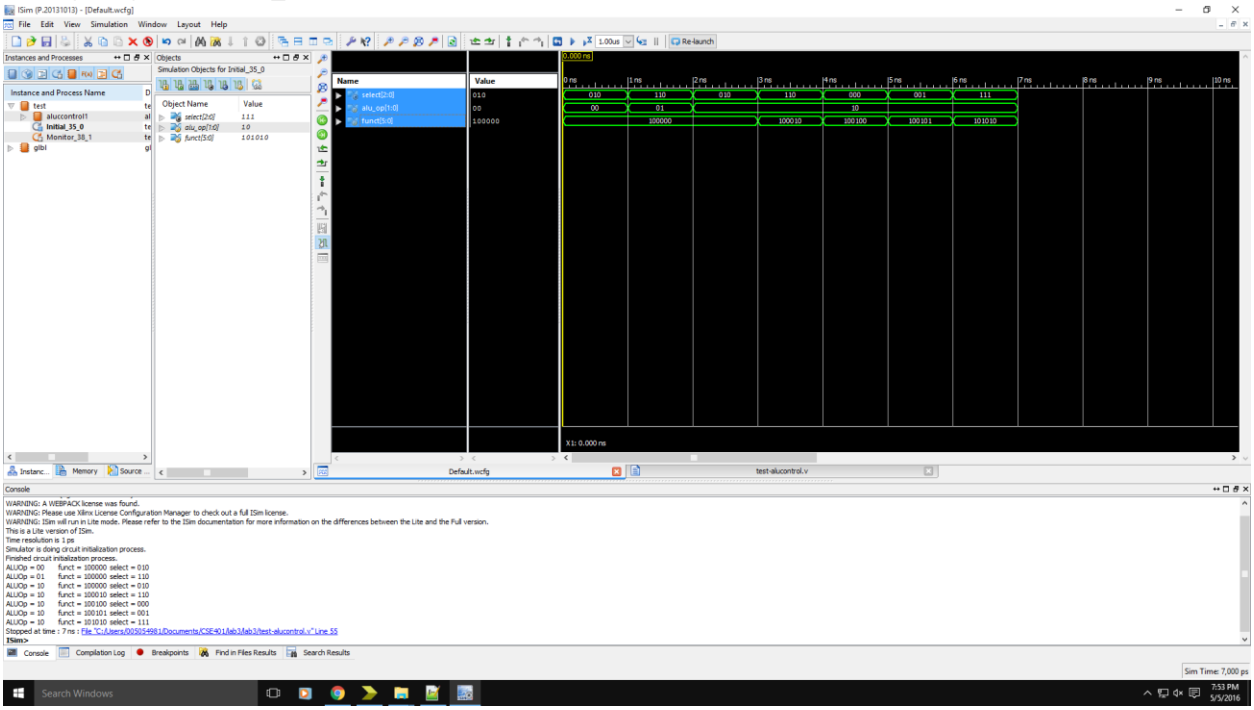
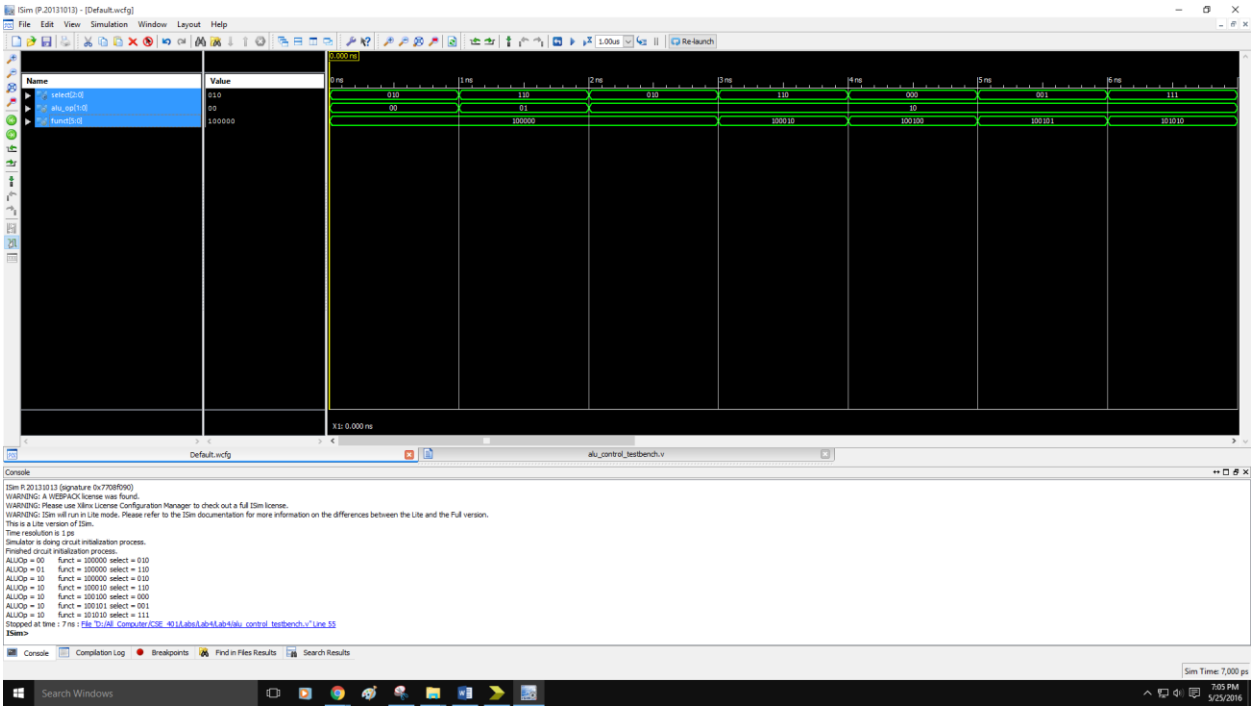
## Timing Diagram for alu_control



## Timing Diagram for alu



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Timing Diagram for Pipeline Execute Stage