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Class: CSE 401
Term: Spring 2016

Lab 4: The MIPS datapath in Verilog: The Memory stage

Introduction: This lab implements the fourth stage of the MIPS five stage pipeline. This stage consists of three components: AND, data_memory, and mem_wb.

AND:

This ANDs (bit-wise) the branch and zero, indicating if a jump to an address is necessary.
The output, PCSrc, goes to mux.v from the Fetch Stage. If PCSrc is true, then there is a branch jump, otherwise there is not.

data_memory:

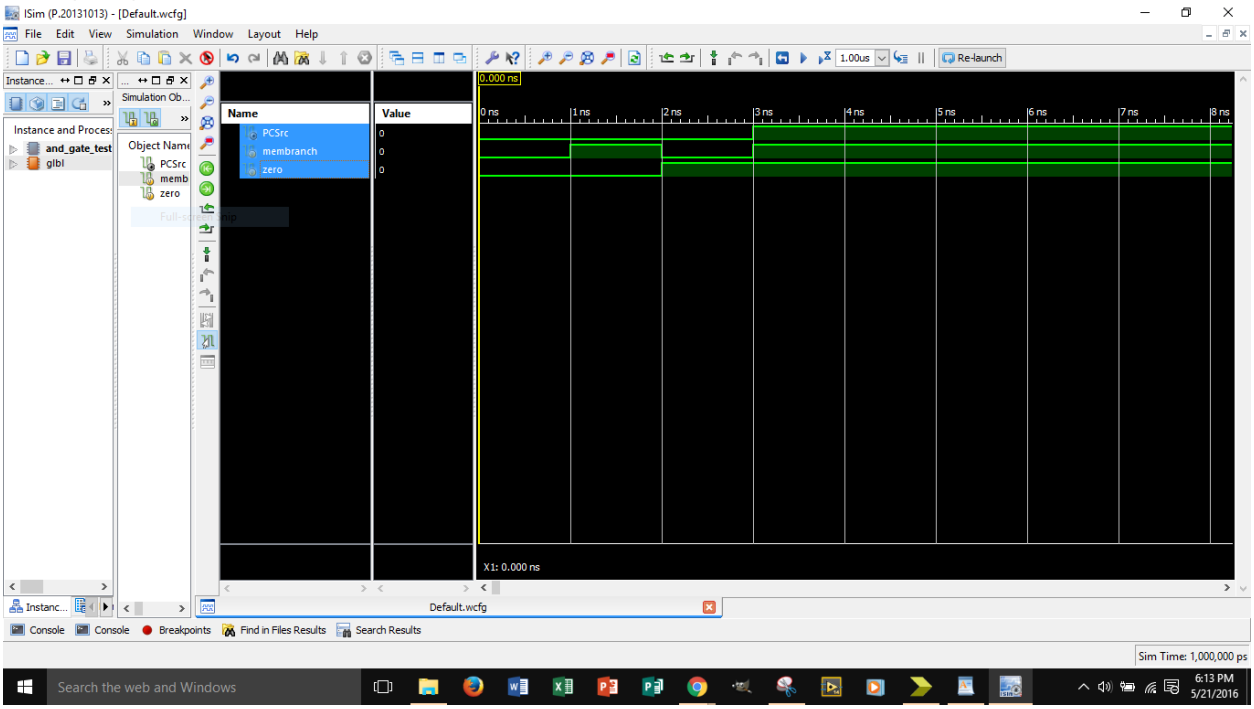
Its inputs are alu_result, rdata2out, memwrite, and memread, which stem from the EX/MEM latch.
The output, read_data, goes to the MEM/WB latch.

If memread is true, then read_data is re-assigned as the value in current address. If memwrite is true, then read_data is unaltered, and instead, the value in the current address is changed to rdata2out.

mem_wb:

This is the latch that receives signals form all the modules of the memory stage. Its outputs go to mux of WRITE-BACK Stage and FETCH.

Timing Diagram for AND



Timing Diagram for data_mem

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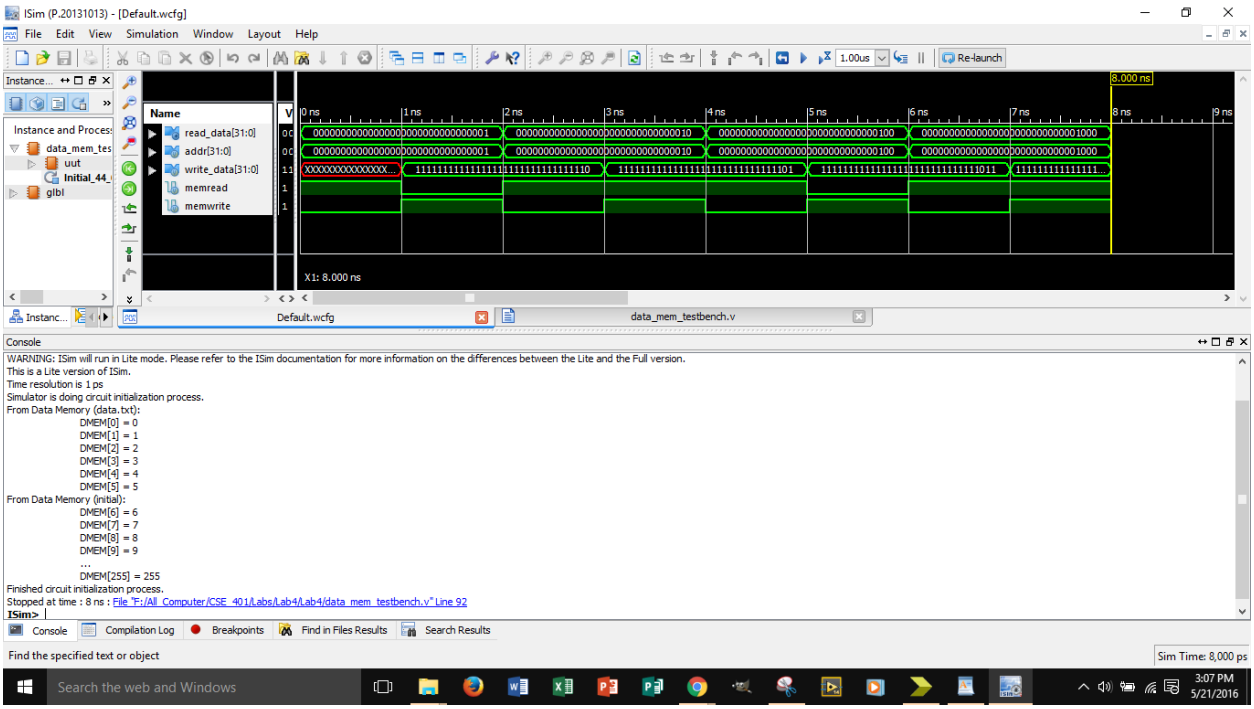

Timing Diagram for Memory_Pipeline