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Term: Spring 2016

Lab 6: The MIPS datapath in Verilog: Testing MIPS datapath stage

Introduction: Implements MIPS datapath by simulating a behavioral model written in Verilog.

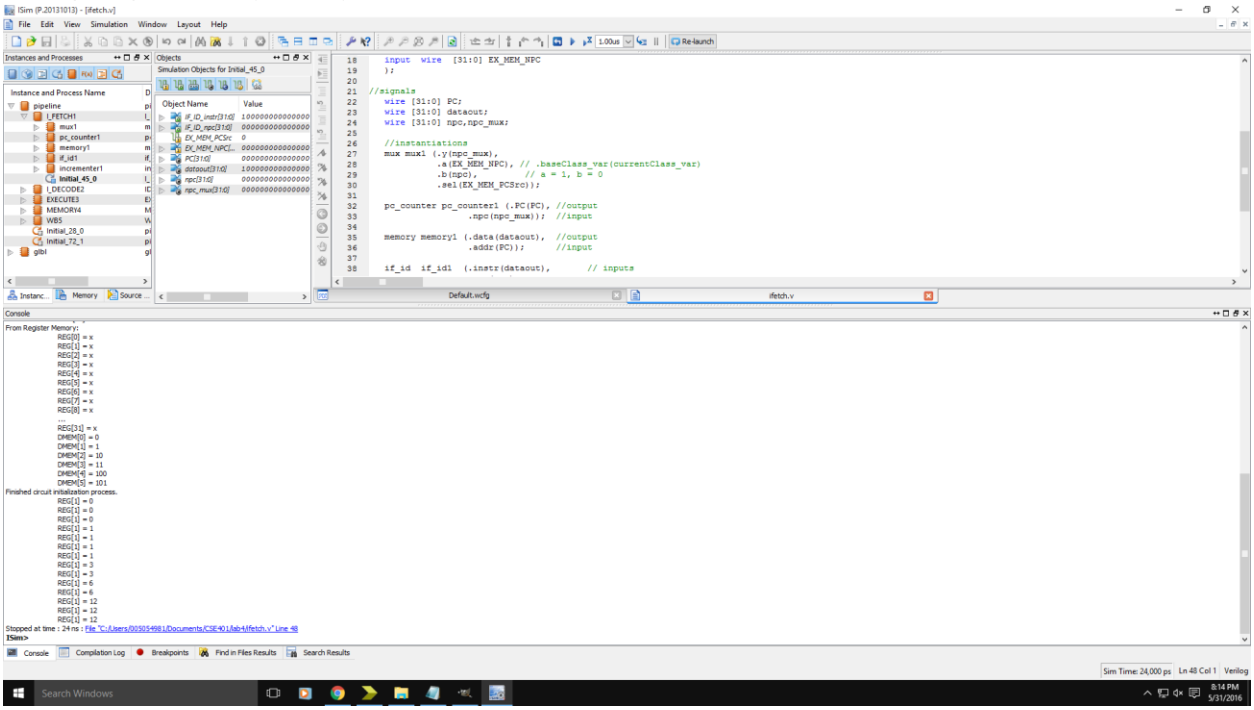
Pipeline:

Creates instances of the IF,ID, EXECUTE, MEMORY, and WB modules. The EX/MEM address input and the select signal for the multiplexer portion
of the IF module will be initialized to 0, while the wires for ID are set based on the overall diagram on Lab 1-2.

For the final implementation of the MIPS datapath, mem.v's memory reads from the added risc.txt file. To verify that the pipeline functions correctly,
within the 24 cycles REG[1] should iterate from 1, 3, 6, and 12.

Altogether the pipeline is dynamic. The connections divvies with functionality ranging from iterator through addresses, selecting when to initiate jumps, accessing and writing to memory, and parsing/decoding instructions in order to finally
execute them.

Timing Diagram for Cycle Sequence of REG[1]



Timing Diagram for Final_Pipeline

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