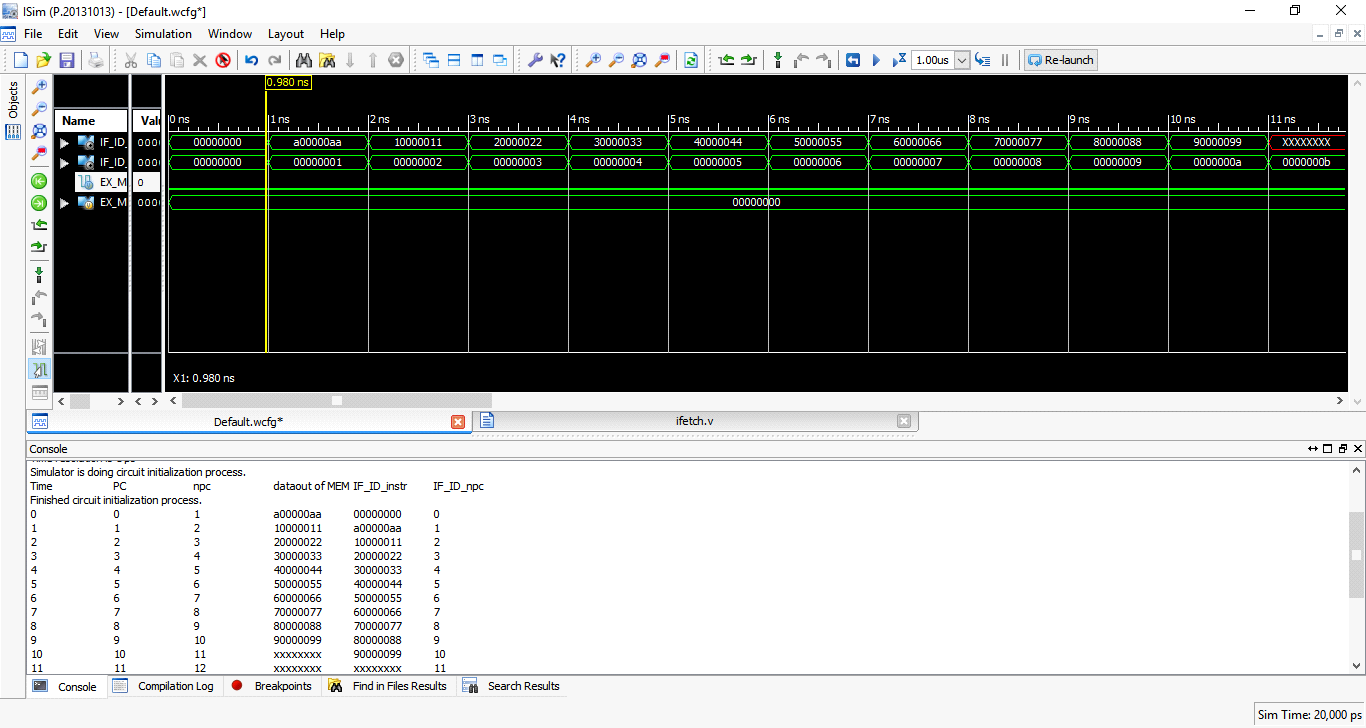
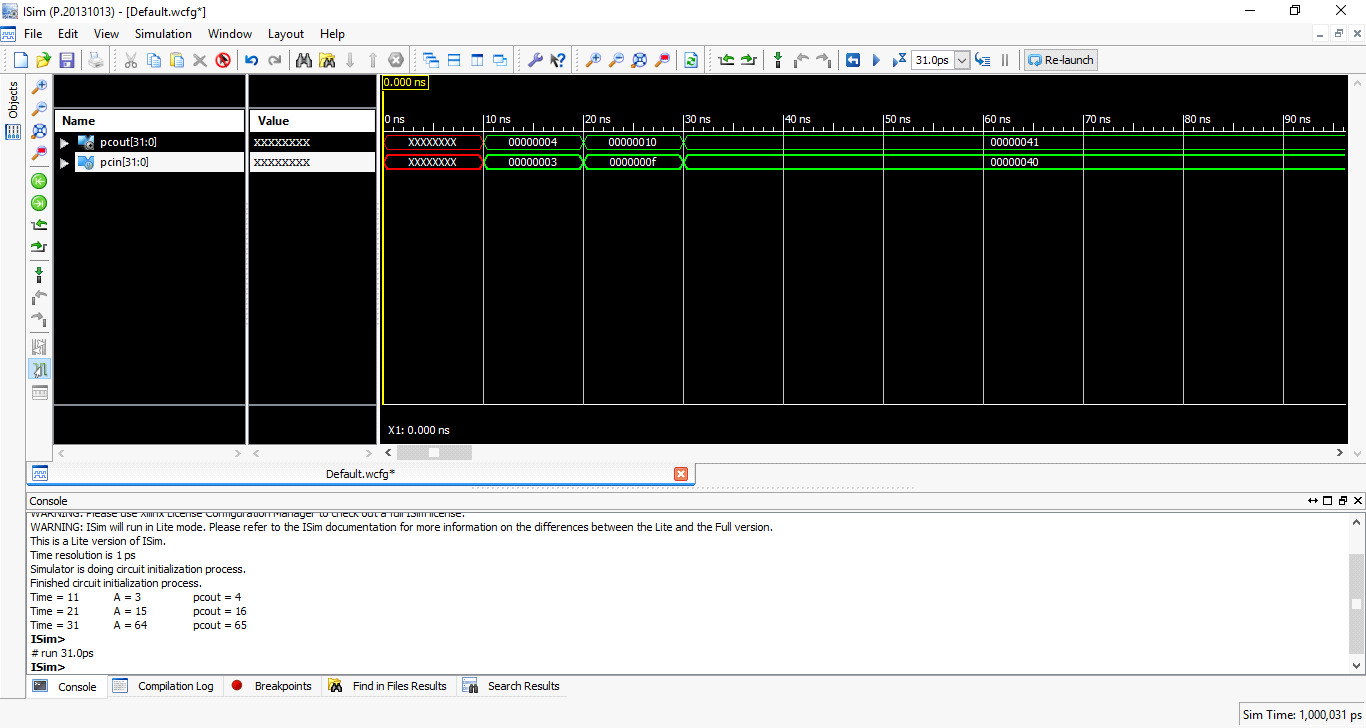
**Lab 1: The MIPS datapath in Verilog: the Instruction Fetch stage**

Review: This lab implements the first stage of the MIPS five stage pipeline. This stage consists of five components: the program counter (PC), instruction memory, multiplexer, incrementer, and the IF/ID pipeline register. In this lab, the instruction memory was initialized to certain values. The select input and the input from the EX/MEM latch for the multiplexer were both set to 0 (static input).

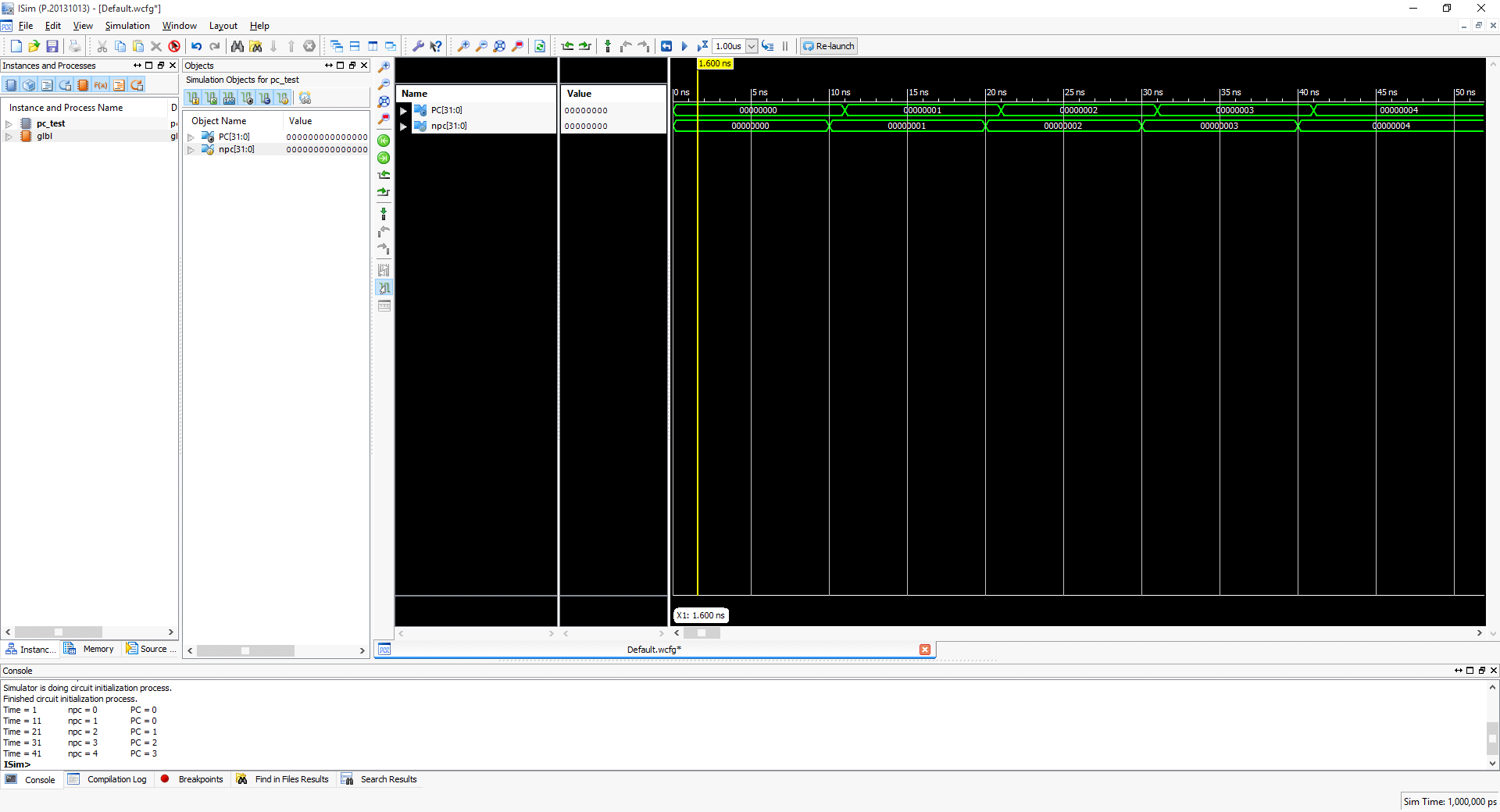
Timing Diagram for Instruction Fetch Latch



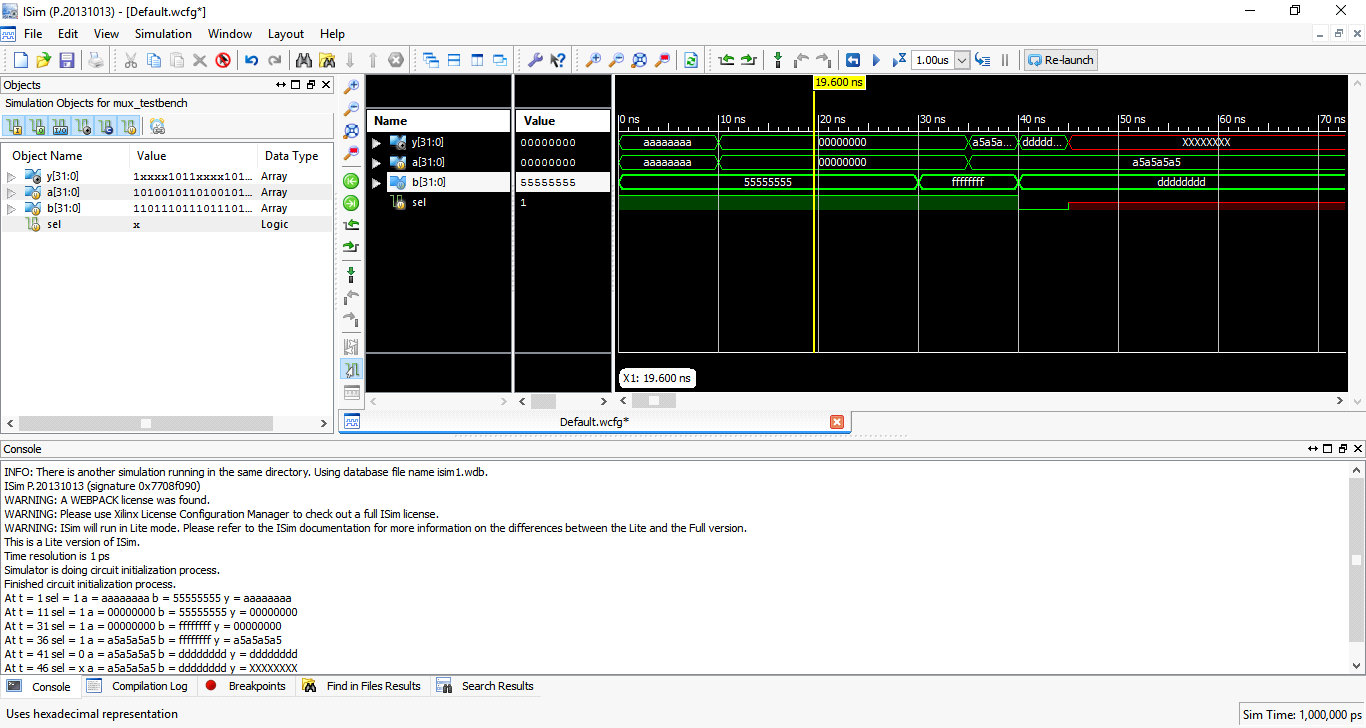
Timing Diagram for Incrementer



Timing Diagram for Program Counter



Timing Diagram for Multiplexer



Timing Diagram for Pipeline Fetch Stage