**Lab 2: The MIPS datapath in Verilog: the Instruction Decode stage**

Introduction: This lab implements the second stage of the MIPS five stage pipeline. This stage consists of four components: control, register, s\_extend, and id\_ex.

**control:**

Receives 6 bits of the instruction code from ifetch.v (originally 32 bits) as an opcode

and divides it into execution/address, memory access, and write-back control lines.

This module applies switch statements and should be used for review.

**register:**

The module populates thirty-two 32-bit addresses/registers with zero. For lab 2, RegWrite

data is unspecified, but eventually it should come from MEM/WB from lab 6. This outputs two 32-bit registers,

A and B. A is the contents of register rs (source) and B is the contents of registers rt (target).

**s\_extend:**

Sign extends 16 bits into 32 bits. This maintains the characteristics of a positive or

negative number.

**id\_ex:**

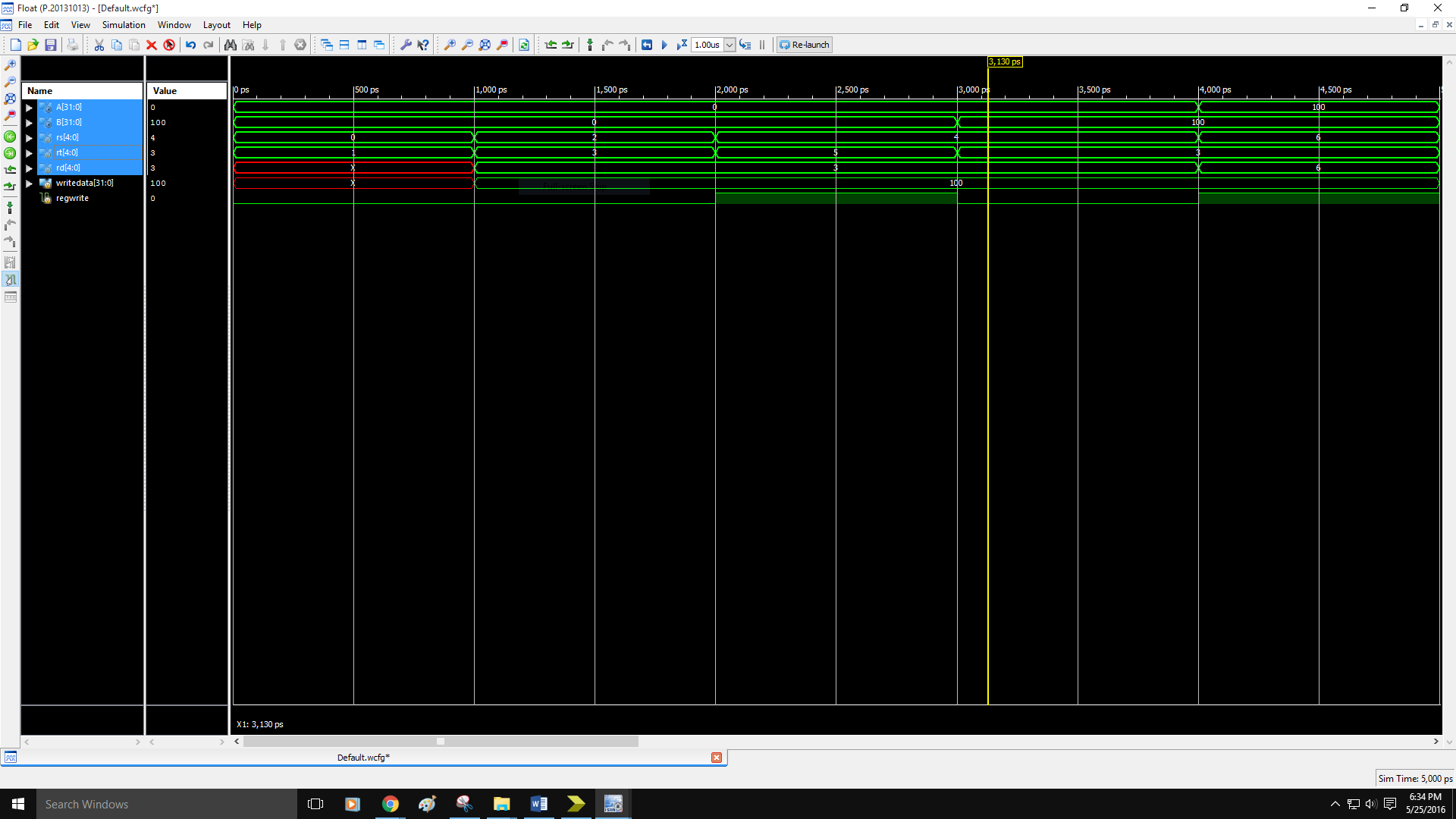
Implements an ID/EX pipeline register that inputs and outputs the program

counter and instruction.

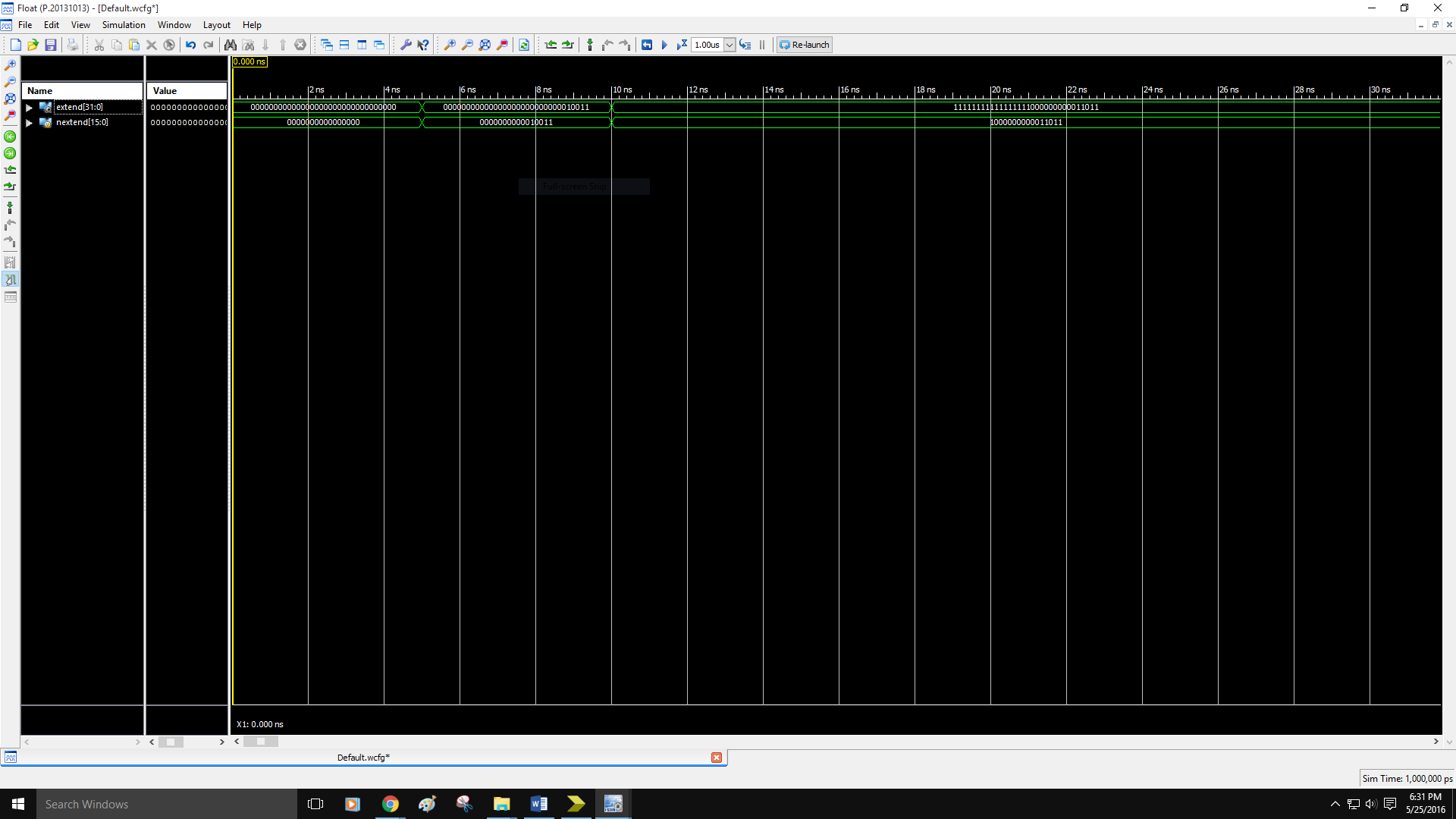
Changes from the diagram: ctlex\_out outputs into regdst[1], alusrc[1], and aluop[2]

This refers to the Execution/Address control lines.

Timing Diagram for register



Timing Diagram for s\_extend



Timing Diagram for Pipeline ID Stage

