**Lab 3: The MIPS datapath in Verilog: The Execute stage**

Introduction: This lab implements the third stage of the MIPS five stage pipeline. This stage consists of six components: adder, bottom\_mux, alu\_control, alu, top\_mux, and ex\_mem.

**adder:**

Adds two 32-bit inputs to output a 32-bit value. Takes in npcout and s\_extendout to

output adder\_out.

**bottom\_mux:**

Implements a multiplexer that selects from two inputs (5 bits), a and b, based

on the sel input. Its inputs are instrout\_1511 and instrout\_2016 from ID/EX latch, and regdst.

The output is muxout, which is sent to EX/MEM latch.

**alu\_control:**

Takes in 6 bit of s\_extendout with alu\_op and outputs select, which is the control.

for alu.v. This bridges machine language with assembly language.

**alu:**

Takes in rdata1 as its input as well as "b," which is the output of top\_mux.

It outputs result, later known as aluout, and zero, which is then aluzero for ex\_mem.v.

This handles the logical and arithmetic correspondence.

**top\_mux:**

Implements a multiplexer that selects from two inputs (32 bits), a and b, based

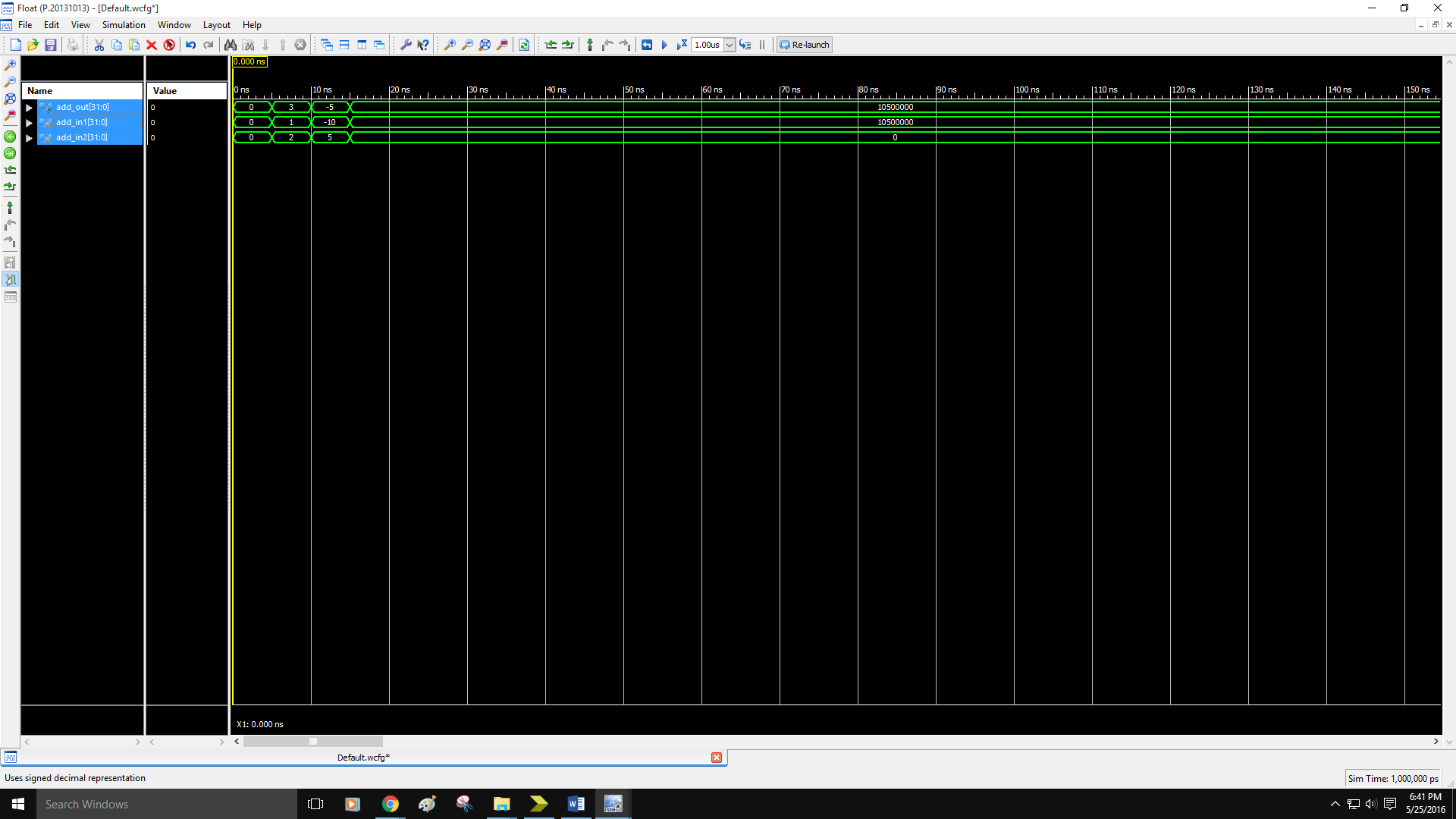
on the sel input. Its inputs are rdata2 ID/EX latch and aluscr from alu\_control.v

The output becomes the b input of alu.v

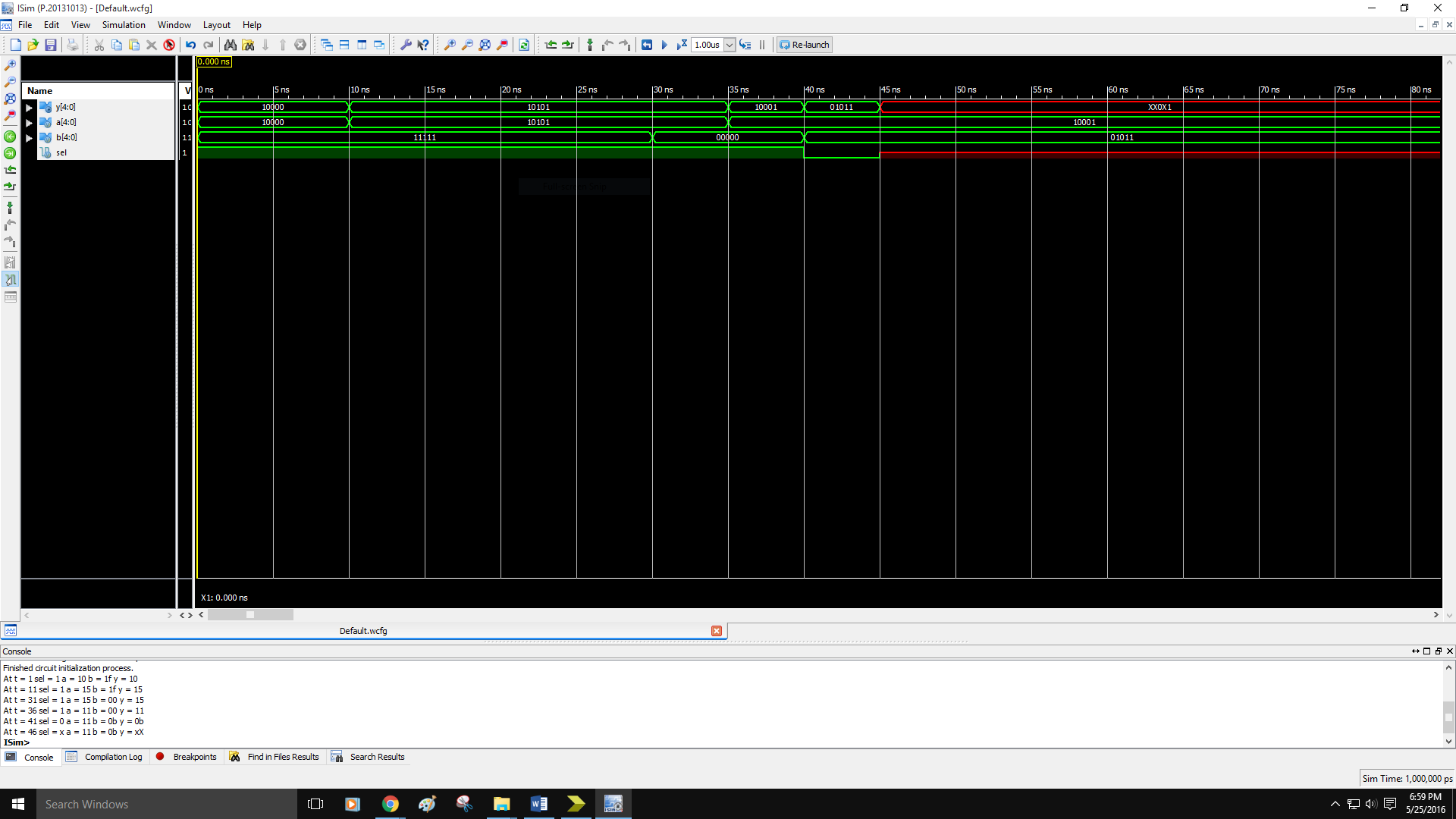
**ex\_mem:**

This is the latch that receives signals form all the modules of the execute stage. Its outputs go to MEM/WB and FETCH.

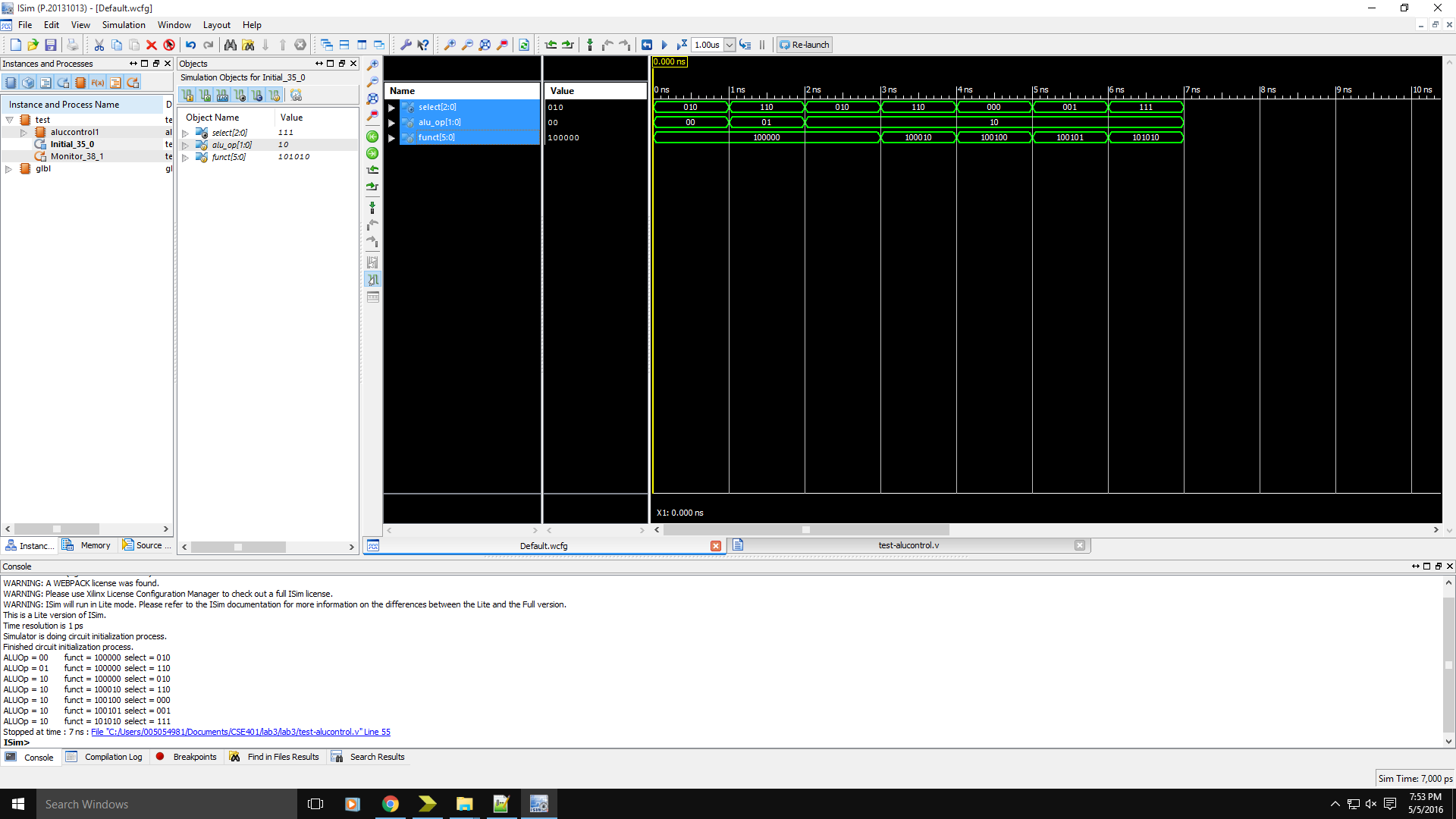
Timing Diagram for adder



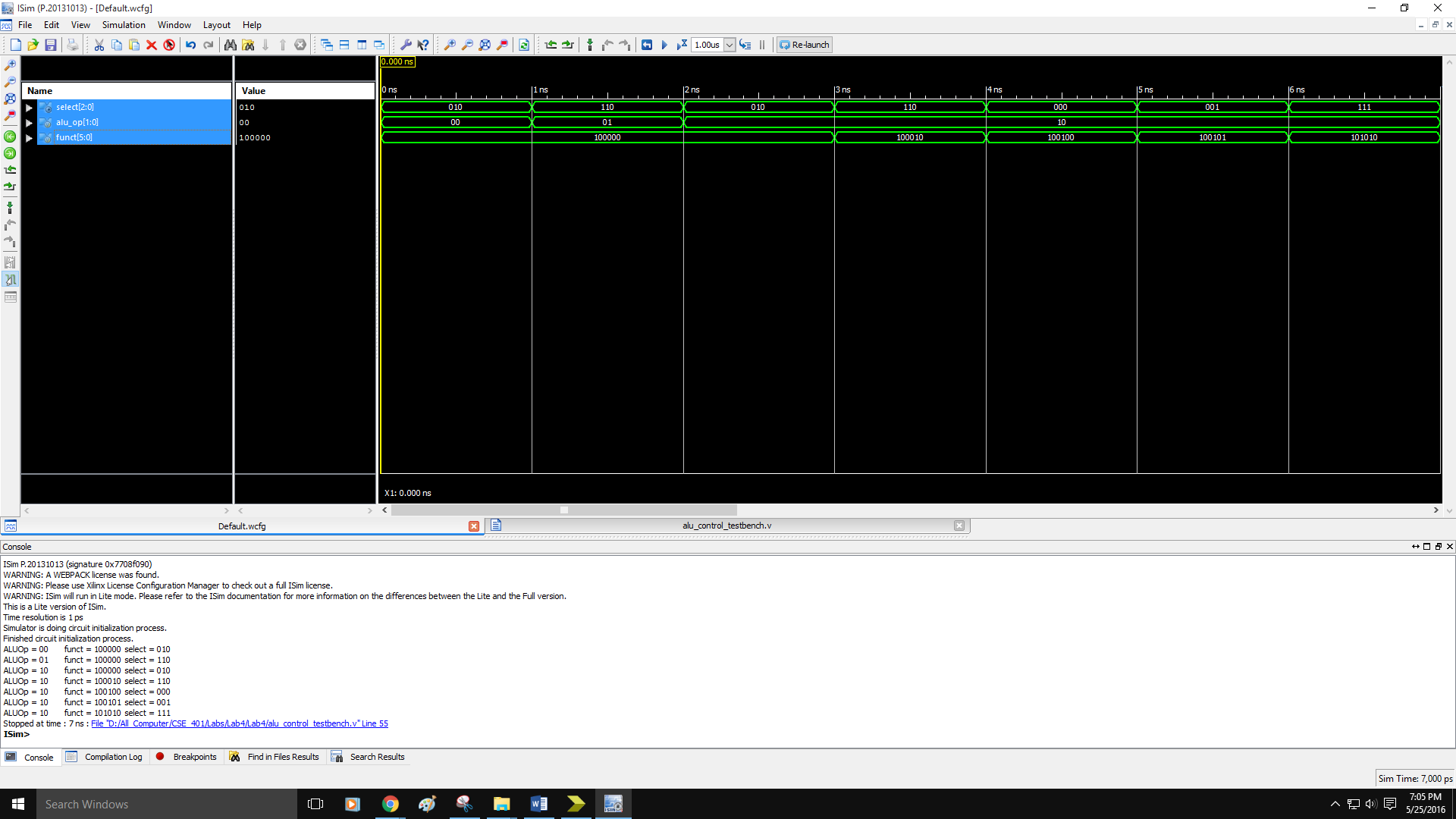
Timing Diagram for bottom\_mux



Timing Diagram for alu\_control



Timing Diagram for alu



Timing Diagram for Pipeline Execute Stage

