**Lab 4: The MIPS datapath in Verilog: The Memory stage**

Introduction: This lab implements the fourth stage of the MIPS five stage pipeline. This stage consists of three components: AND, data\_memory, and mem\_wb.

**AND:**

This ANDs (bit-wise) the branch and zero, indicating if a jump to an address is necessary.

The output, PCSrc, goes to mux.v from the Fetch Stage. If PCSrc is true, then there is a branch jump,

otherwise there is not.

**data\_memory:**

Its inputs are alu\_result, rdata2out, memwrite, and memread, which stem from the EX/MEM latch.

The output, read\_data, goes to the MEM/WB latch.

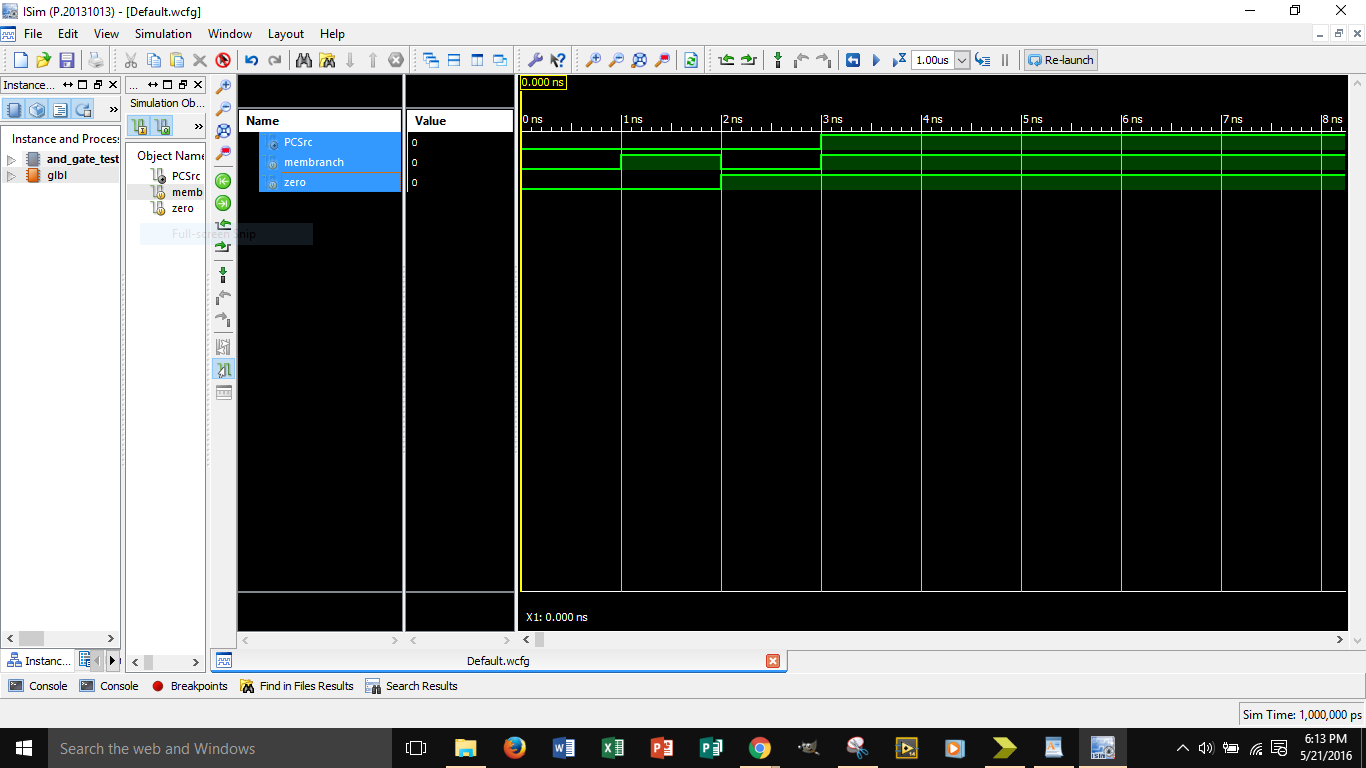
If memread is true, then read\_data is re-assigned as the value in current address. If memwrite is true,

then read\_data is unaltered, and instead, the value in the current address is changed to rdata2out.

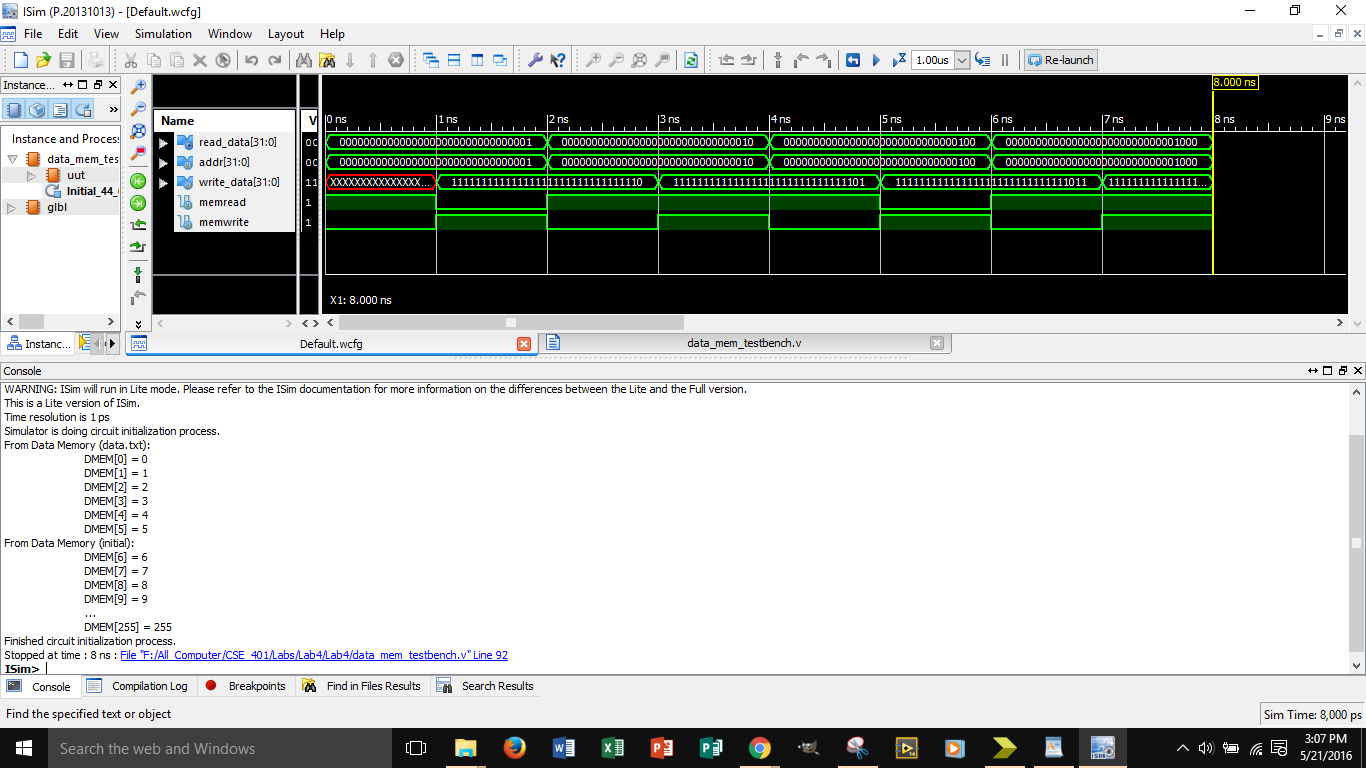
**mem\_wb:**

This is the latch that receives signals form all the modules of the memory stage. Its outputs go to mux of WRITE-BACK Stage and FETCH.

Timing Diagram for AND



Timing Diagram for data\_mem



Timing Diagram for Memory\_Pipeline

