**Lab 5: The MIPS datapath in Verilog: The Write-Back stage**

Introduction: This lab implements the final stage of the MIPS five stage pipeline. This stage consists of only one component: mux

**mux:**

The write-back stage consists of only one module: a multiplexer. Its output goes to reg.v as the input for write\_data of I\_DECODE.

The inputs are mem\_Read\_data, mem\_ALU\_result, and MemtoReg which are the outputs of the MEM/WB latch.

Timing Diagram for WB during the MIPS data\_path testing of Lab 6

