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Electrical schematics for:

product: **STEMLab_125-14**

version: **V1.1**

variant: **STEMLab 125-14**

release date: **13. 9. 2021**



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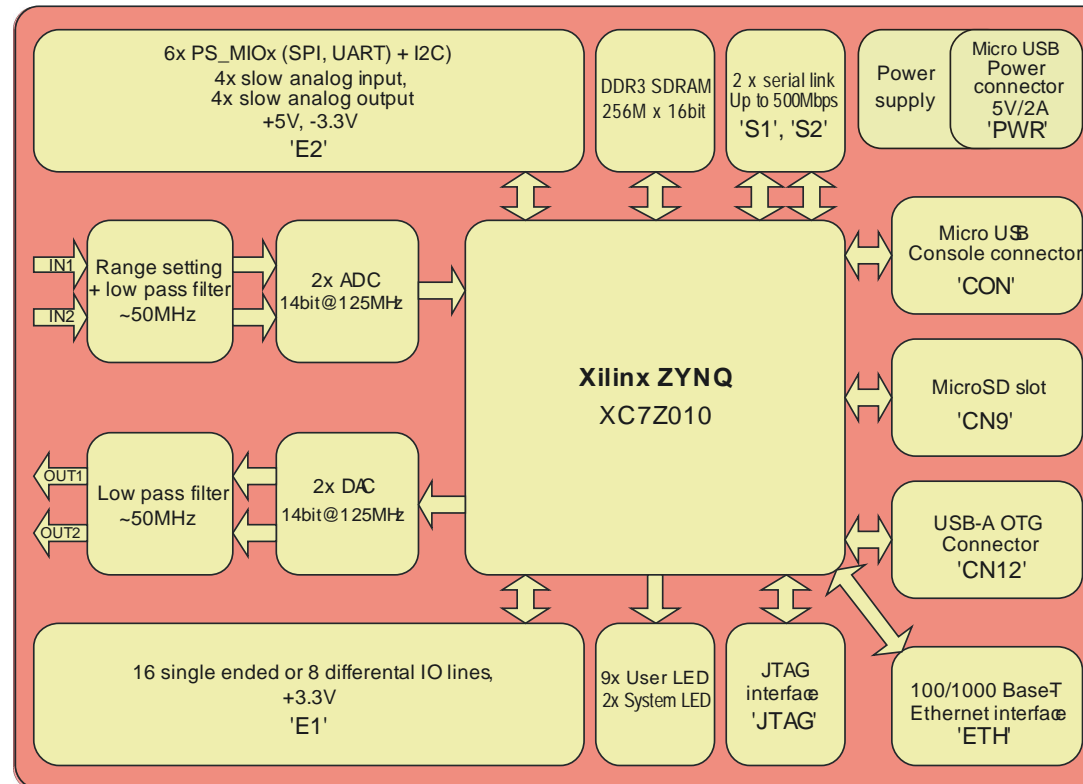
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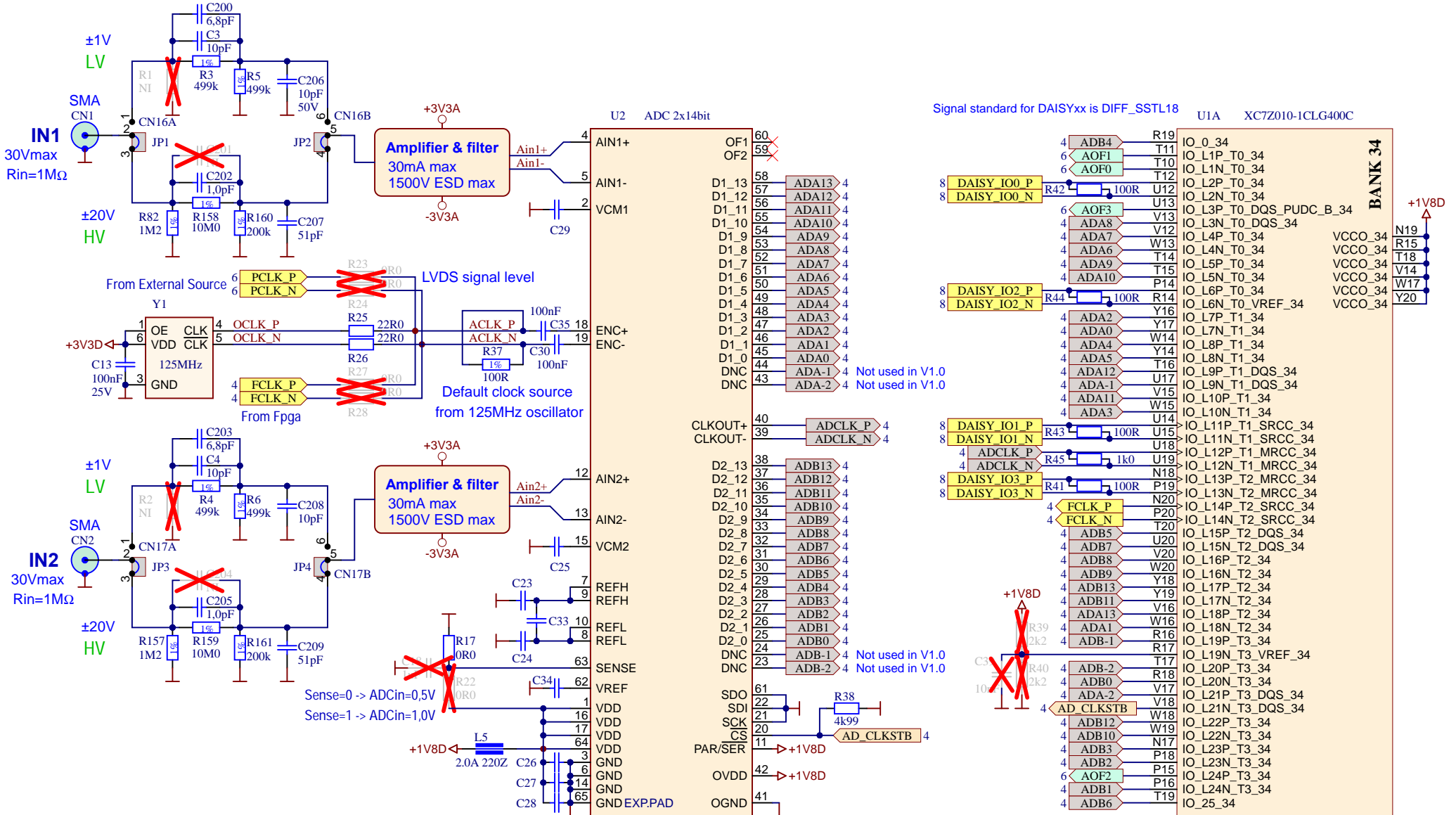
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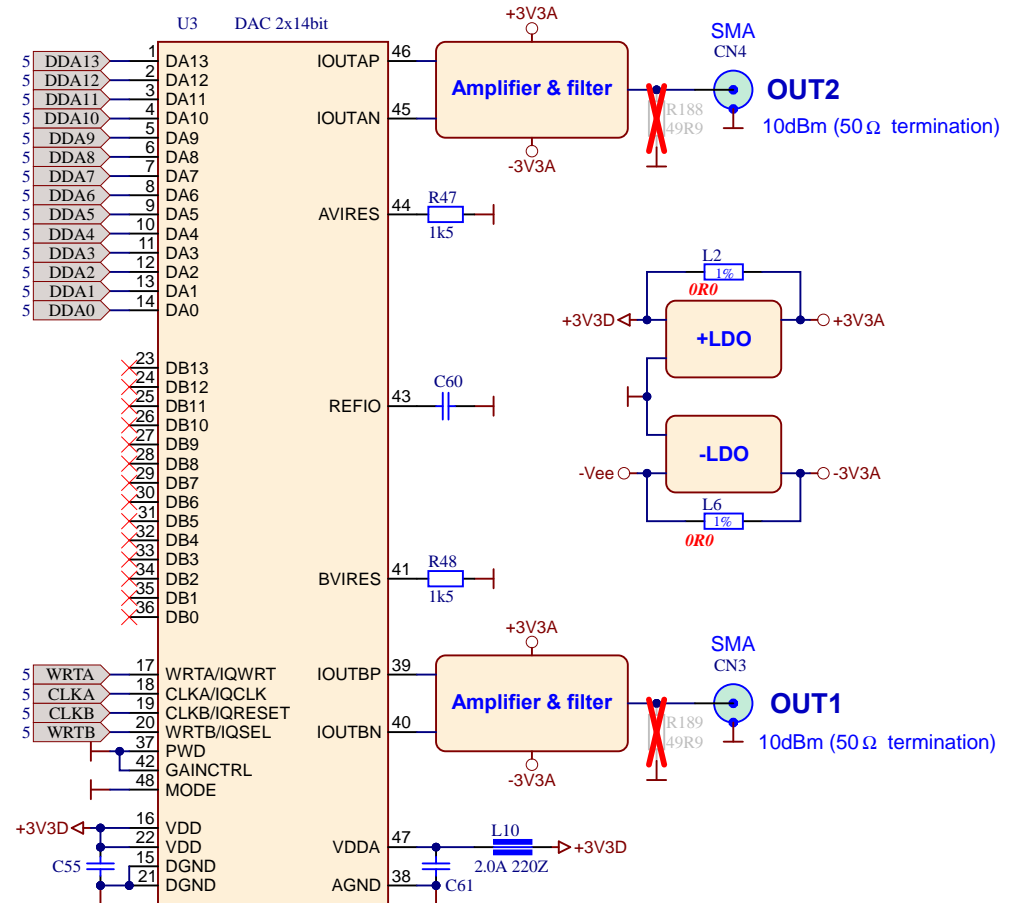
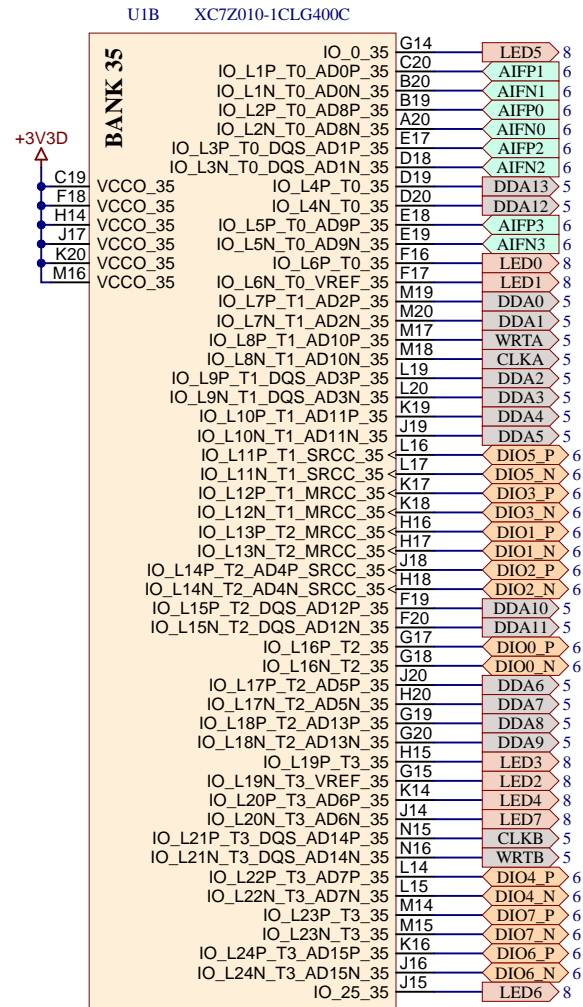
Red Pitaya STEMLab 125-14 V1.1 block schematics



2 Analog front-end and AD converter, Zynq bank 34



3 DA converter and analog back-end, Zynq bank 35



Note: number next to port symbol indicates the sheet where the signal is connected

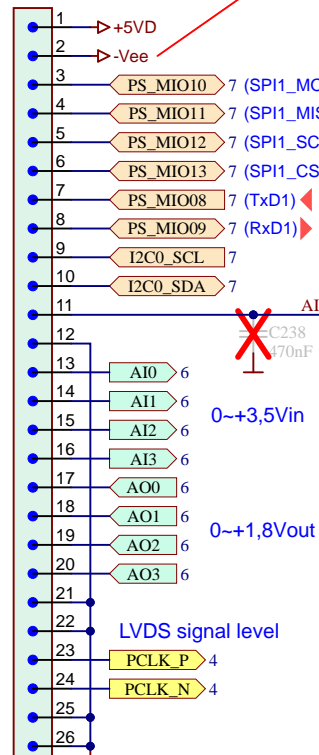
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4 Digital and analog slow I/O, Zynq bank 13

PS_MIO08 is output only and at power-up must be low level (no external pull-ups)!

Negative supply voltage Vee can be -3,3V or -4,2V depends on version!

E2
CN5



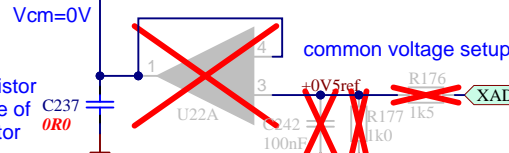
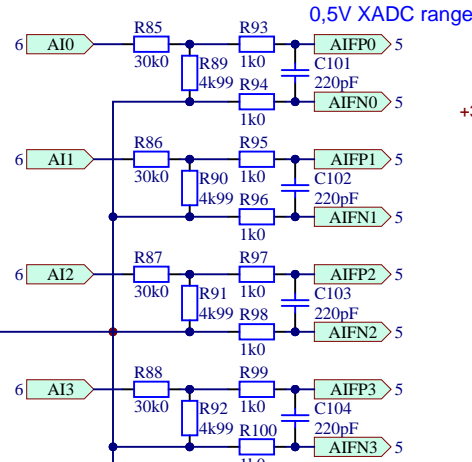
Output only!

Ext com.mode (0~+0,5V)

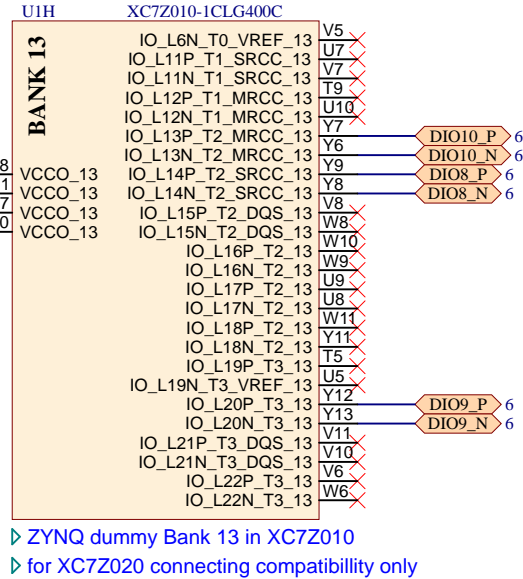
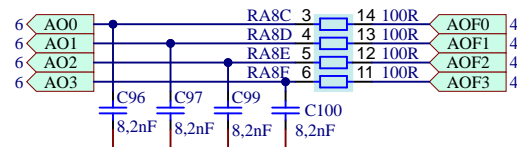
0~+3,5Vin
0~+1,8Vout
LVDS signal level

IDC 2.54mm 26 pin low profile

(alternative ZYNQ function)
3,3V logic levels



Remove if external common mode voltage is used!



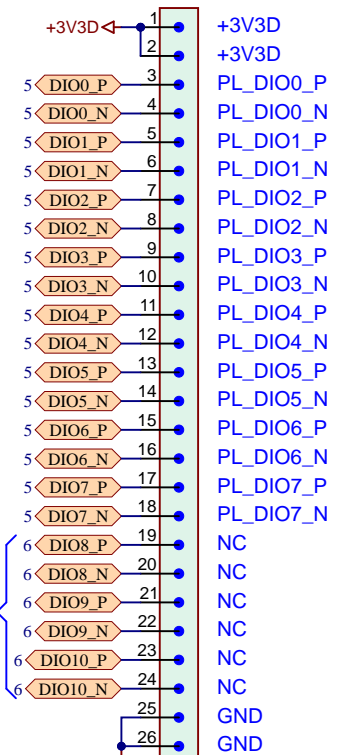
Y ZYNQ dummy Bank 13 in XC7Z010

for XC7Z020 connecting compatibility only

Not connected in XC7Z010

16 single ended or
8 differential digital I/O
with 3,3V logic levels

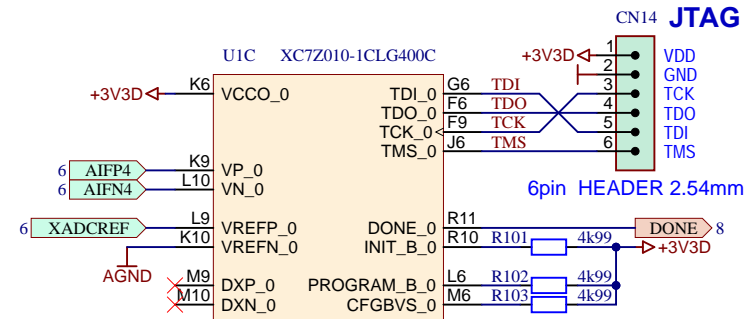
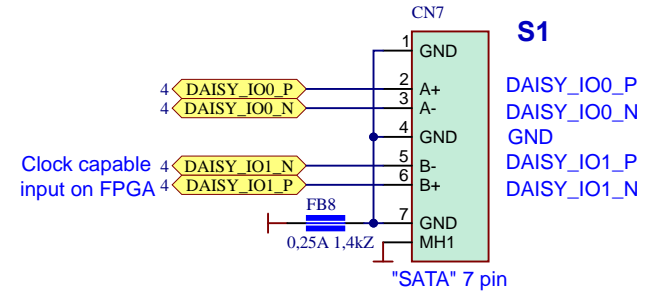
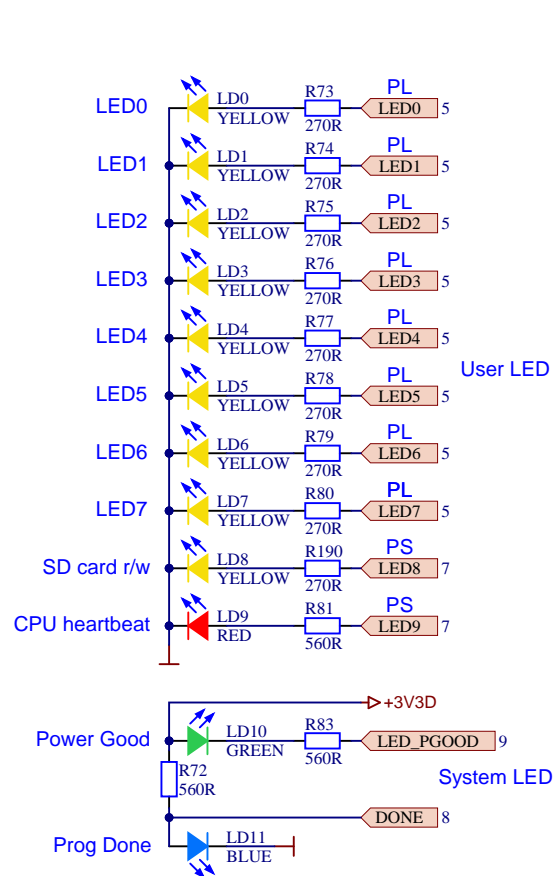
E1
CN6



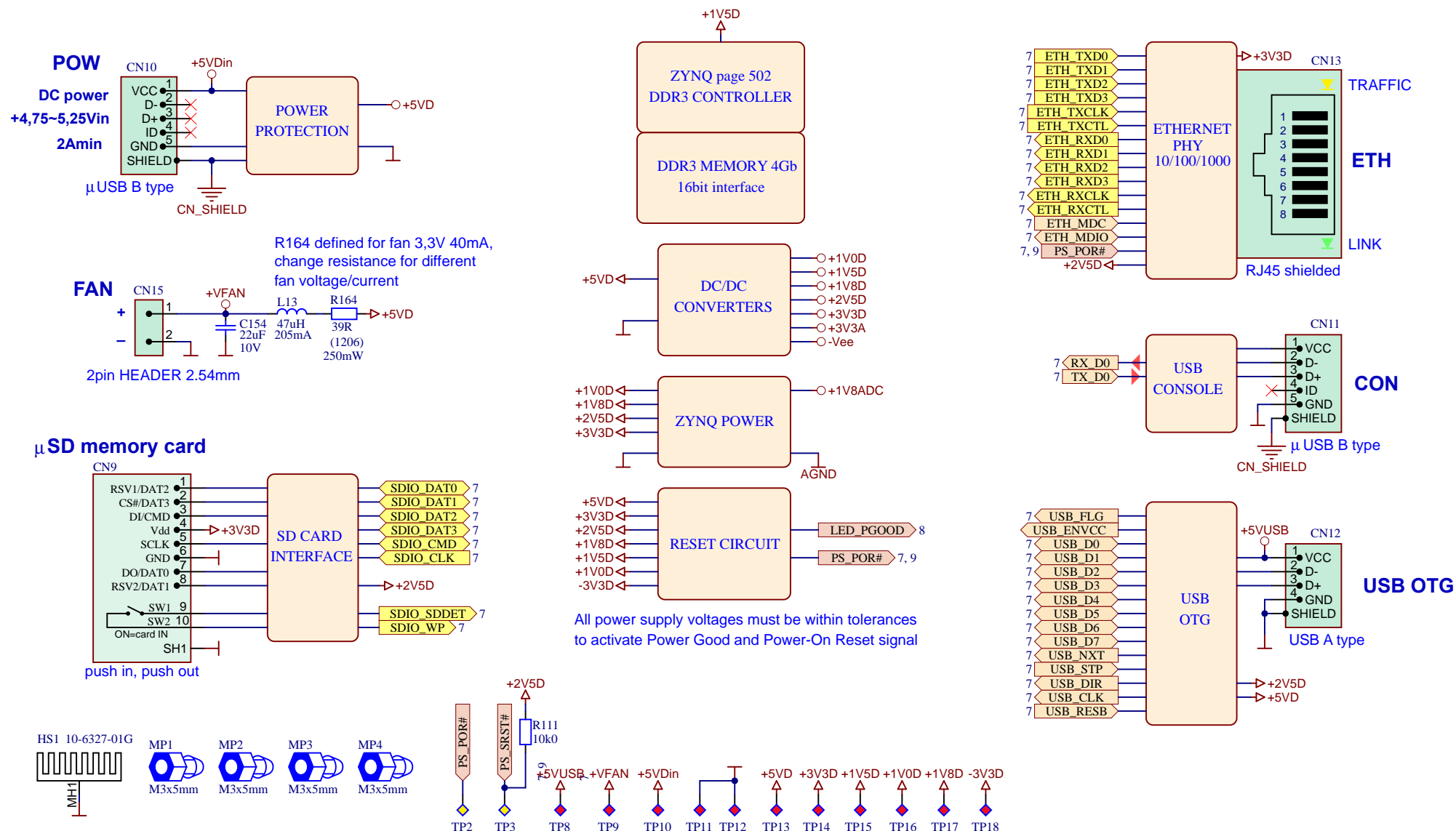
IDC 2.54mm 26 pin low profile



6 LED, Serial interface, JTAG



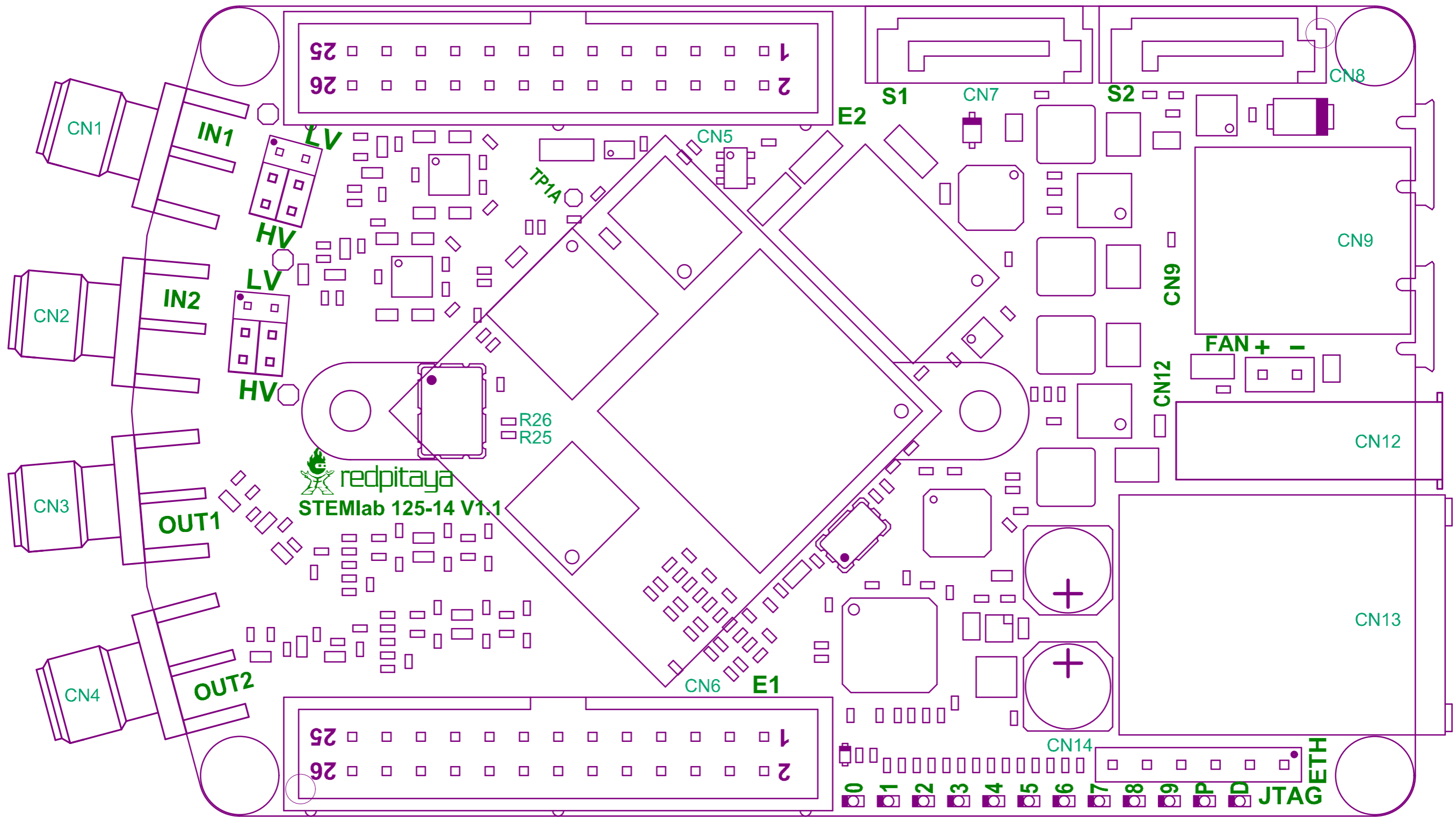
7 Ethernet, memory card, Console, USB OTG, DDR3, Power



Note: number next to port symbol indicates the sheet where the signal is connected

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Top assembly: STEMLab_125-14_V1.1 variant: STEMLab 125-14



Bottom assembly: STEMLab_125-14_V1.1 variant: STEMLab 125-14

