Fabio Carta

Updated: June 27, 2015

CONTACT INFORMATION

Phone number: +1 (646) 361 2971

Email address: fc2383@columbia.edu

Address: Department of Electrical Engineering, Columbia University
500 West 120th Street, Suite 1300
New York, NY, 10025, USA

EDUCATION

PhD: Electrical Engineering — *2011 - July 2015 (Expected)*
Columbia University, NY, USA
GPA 4.0

Master of Science: Nanotechnologies for the ICT — *2008 - 2010*
1st semester at Politecnico di Torino, Italy
2nd semester at Institut Politechinque de Grenoble, France
3rd semester at Ecole Politechnique Federale de Lausanne, Switzerland
Thesis: Structural relaxation in amorphous as deposited GeSbTe

Bachelor Degree: Electronic Engineering — *2002 - 2008*
Universitá degli studi di Cagliari, Cagliari, Italy

RESEARCH EXPERIENCE

Research Assistant at: Columbia University — *2011- at present*
New York, NY, USA
Department of Electrical Engineering
Advisor: Prof. Ioannis Kymissis
a-Si crystallization for BEOL 3D integration
TCAD simulation and integration of polysilicon TFTs for 3D integration
Integration and characterization of OFET digital logic
Investigation of pyroelectric material for actuation

WORKING EXPERIENCE

Founder and CTO of: plugSTRATE — *May 2014 - at present*
Wireless monitoring network for building efficiency
Winner of the PowerbridgeNY contest

Internship at: IBM T. J. Watson Research Center — *June - September 2013*
Yorktown Heights, NY, USA
Mentor: Dr. Stephen M. Gates
Manager: Dr. Daniel Edelstein
TCAD simulation and integration of polysilicon TFTs for 3D integration
Excimer laser amorphous silicon crystallization

Internship at: IBM T. J. Watson Research Center — *March - September 2010*
Yorktown Heights, NY, USA
Mentor: Dr. Simone Raoux
Manager: Dr. William J. Gallagher
Structural relaxation in amorphous as deposited GeSbTe

Internship at: Delft University of Technology — *June - August 2009*
Delft, Netherlands
Department of BioMechanical Engineering
Mentor: Dr. Dedy H. B. Wicaksono
Modelling and simulations of a force sensor for dental drill

PUBLICATIONS

F. Carta, S. Gates, A. B. Limanov, J. Im, D. Edelstein, I. Kymissis; *Sequential Lateral Solidification of Silicon Thin Film on BEOL Integrated Wafer for Monolithic 3D Integration*; **In preparation**.

F. Carta, S. Gates, A. B. Limanov, J. Im, D. Edelstein, I. Kymissis; *Two Shot Laser Crystallized Silicon for Monolithic 3D Integration of VLSI*; **Submitted to Transactions on Electron Devices**.

H. Hlaing, C. H. Kim, F. Carta, C. Y. Nam, R. Barton, N. Petrone, J. Hone, I. Kymissis; *Low-Voltage Organic Electronics Based on a Gate-Tunable Injection Barrier in Vertical Graphene-Organic Semiconductor Heterostructures*; **Nano Letters**; 15 (1); 2015; 69-74.

F. Carta, S. Gates, A. B. Limanov, H. Hlaing, J. Im, D. Edelstein, I. Kymissis; *Sequential lateral solidification of silicon thin films on low-k dielectrics for low temperature integration*; **Applied Physics Letters**; 105; 2014; 242904-1/4.

C. H. Kim, H. Hlaing, F. Carta, Y. Bonnassieux, G. Horowitz, I. Kymissis; *Templating and Charge Injection from Copper Electrodes into Solution-Processed Organic Field-Effect Transistors*; **Applied Material Interfaces**; 5; 2013; 3716-3721.

F. Carta, Y. -J. Hsu, J. Sarik, I. Kymissis; *Bimorph actuator with monolithically integrated CMOS OFET control*; **Organic Electronics**; 14; 2013; 286-290.

CONFERENCES

F. Carta, S. Gates, A. B. Limanov, H. Hlaing, J. Im, D. Edelstein, I. Kymissis; *Excimer laser crystallization of silicon thin films on low-k dielectrics for monolithic 3D integration*; April 06-10; MRS 2015.

F. Carta, H. Hlaing, H. Edrees, S. Yang, M. Seok, I. Kymissis; *Co-development of complementary technology and modified-CPL family for organic digital integrated circuits*; April 06-10; MRS 2015.

F. Carta, S. Gates, A. B. Limanov, V. W. Lee, H. Hlaing, J. Im, D. Edelstein, I. Kymissis; *Excimer laser crystallization of silicon thin films on low-k dielectrics for monolithic 3D integration*; November 5-8; GIT 2014.

H. Hlaing, F. Carta, R. Barton, C. Y. Nam, N. Petrone, J. Hone, I. Kymissis; *Low-power organic electronics based on gate-tunable injection barrier in vertical graphene-organic semiconductor heterostructures*; June 22-25; DRC 2014.

F. Carta, S. Gates, A. B. Limanov, V. W. Lee, J. Im, D. Edelstein, I. Kymissis; *Excimer laser crystallized Si for BEOL 3D integration*; November 17-20; GIT 2013.

C. H. Kim, H. Hlaing, F. Carta, Y. Bonnassieux, G. Horowitz, I. Kymissis; *Solution-Processed Organic Transistor with Chemically Modified Copper Electrodes*; June 2-7; Fpi-11 2013.

F. Carta, Y. -J. Hsu, J. Sarik, I. Kymissis; *Electrostrictor with Monolithically Integrated CMOS TFT Control*; June 10-14; CIMTEC 2012.

F. Carta, Y. -J. Hsu, J. Sarik, I. Kymissis; *Unimorph actuator with monolithically integrated CMOS level shifter*; April 11; CMOC 2012.

D. H. B. Wicaksono, F. Carta, P. J. French, P. Breedveld, J. Dankelman; *Early Feasibility Study for MOMS-based Shear Stress Sensing in Dental Drilling*; November 26-29; SAFE 2009.

PATENTS

F. Carta and other 3 inventors; *OFET including PVDF-TRFE-CFE dielectric*; United States Patent (WO 2013106021 A1).

AWARDS

plugSTRATE startup winner of PowerbridgeNY contest *May 12, 2014*
Awarded with $150,000 for development

Best Student Paper - Second Place *November 20, 2013*
Excimer Laser Crystallized Si for BEOL 3D Integration
Global Interposer Technology Workshop, GIT 2013

RESEARCH SKILLS

- *Integration:* Cleanroom environment, Glovebox environment, Lithography, Wet etching, RIE, ICP, PECVD, PVD, ALD
- *Characterization:* Semiconductor parameter analyzer, Impedance analyzer, SEM, AFM, XRD, Raman spectroscopy, Ellipsometry
- *Simluation software:* Sentaurus Workbench, COMSOL Multiphysics, Cadence Design System, Simulink
- *Software good knowledge:* LabVIEW, Igor, Matlab, LaTeX
- *Software basic knowledge:* VHDL, C, PHP

LANGUAGES SKILLS

Italian: Native language; **English:** Fluent (TOEFL score: 98/120); **French:** Good (A2 level European Standard - Alliance Francaise Grenoble)